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Design and Simulation of Two Stage Wideband CMOS Amplifier in 90 NM Technology

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Abstract

Design and simulation of 7 GHz CMOS wideband amplifier(CMOSWA) using a modified cascode circuit realized in 90-nm CMOS technology is presented here. The proposed system consists of two stages, namely a modified folded cascode and an inductively degenerated common source amplifier. The circuit is experimented with and without a feedback network. This work discusses the performance variation as a function of reactive components, and the initial stage results in 22 dB gain,2.6 GHz bandwidth, and 40GHz unity gain-bandwidth. The circuit without the feedback network exhibits 30.7dB gain,4.8GHz bandwidth(BW), and 10GHz unity-gain bandwidth(UGB). The reactive feedback network's inclusion helped to achieve 38.7 dB gain, 6.95GHz BW, 30GHz UGB, and 55^{o} phase margin. The circuit consumes 1.4mW power from a 1.8V power supply. Simulation results of the proposed circuit are comparable and better than the reported wideband designs in the literature. Realization of our proposed circuit would add value to the area of wideband amplifier design.

Keywords:

Folded Cascode Amplifier(FCA),CMOS Wideband Amplifier(CMOSWA), Unity Gain Bandwidth(UGB), Low Noise Amplifier(LNA), Inductively modified common source amplifier.

I. INTRODUCTION

Design innovations and scaling has led to the reduction in cost of RF microelectronic products. High frequency RF amplifier designs still pose a challenge, in terms of numerous tradeoffs between parameters such as gain, bandwidth, power, supply voltage, linearity, and noise. A broad range of RF amplifiers play significant role in the field of telecommunication. RF engineers are experimenting with different circuit topologies of amplifiers and a distinct variety of process technologies to obtain beneficial results for high frequency applications.

Researchers have proposed a current reusing technique where cascaded complementary common gate and common stage was used to attain wider bandwidth and better linearity[1].There have been reports of using wideband stacked distributed amplifier to improve performance in terms of gain, output power, and bandwidth but compromising chip area and supply voltage[2]. A wideband millimeter-wave low noise amplifier(LNA) was devised using 65 nm technology, which incorporates L-type input matching and T type output matching [3]. This work reports upgraded features in terms of bandwidth and noise figure with an uptick in power consumption and area. The way of generating augmented execution in terms of gain, stability utilizing pseudo-differential common source stage is discussed in [4].Yong Chen et al. reported the design of tunable bandwidth enhancement technique also employing 65 nm technology [5].They have addressed different peaking techniques by which the bandwidth can be improved. The design of a distributed power amplifier which focused on boost in gain over a wide frequency range has been studied in detail [6].Literature reports a circuit applying a dual resonant network whose output is low power with a flat noise figure [7] The design of LNA utilizing active inductors to accommodate impedance matching is discussed where the current reuse technology is utilized to diminish power consumption[8]. Recurring stacking and several peaking procedures are combined in the design of a wideband power amplifier in 65 nm technology has been reported scientists [9].There were reports of another 65nm amplifier designed employing a dual output topology with a combination of higher-order output matching network and cross-coupled differential cascode amplifier stage[10]. The published works discussed above, result in diverging gain over a broad frequency range.Fig.1 shows the block schematic for the proposed work.In Figure.1.a the modified common source amplifier without feedback is cascaded with an initial cascode stage. Since it is an uncompensated system, we incorporate a balancing network to improve phase margin and it is shown in Figure.1.b. The various parameters are adjusted to meet the specified requirements of our wideband amplifier.

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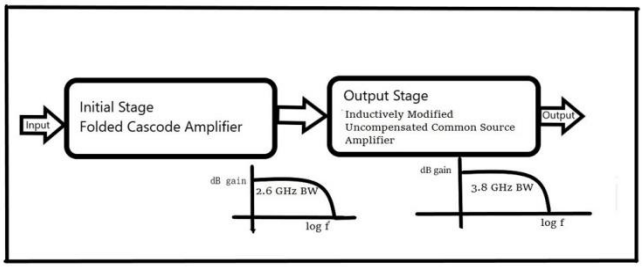
(a)Without compensation



(b)With Compensation

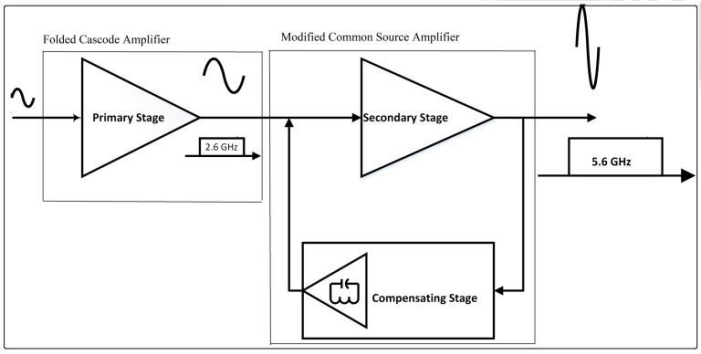


Figure 1. Block diagram description of the proposed system

The design and simulation of a wideband amplifier combining folded cascode topology and modified common source amplifier is discussed in this paper. The presence of inductors in the second stage influences improvement in bandwidth and stability. The gain 38.7dB and bandwidth 6.95GHz that is achieved in this work is better than the results reported in[4][5][8][13].The phase margin obtained in this work is decent compared to the results published and the estimated silicon area is 850μm^2. The different load capacitance values and design steps are trialed to improve the figure of merit than that in the specified literature [13], but with the load capacitance less than pF range, the circuit exhibits good figure of merit and at the same time the flatness is altered and bandwidth reduces. The significance of the proposed circuit is introduced in section 2. Detailed design and analysis is presented in section 3. In section 4, important findings are presented and discussed, and in section 5, the task is completed.

II. PROPOSED CIRCUIT

The proposed circuit cascades a folded cascode topology with a modified common source circuit. A folded cascode circuit topology is selected as the first stage due to its different qualities. Compared to telescopic topology and cascode circuits, FCA has good gain, improved bandwidth, high voltage swing, good common-mode range and stabilization. Furthermore, new cascode topologies like recycling FCA have been studied and compared. An FCA and recycling FCA was found to be beneficial for high-frequency application due to higher gain-bandwidth product, but due to less transistor count and complexity, the conventional folded cascode amplifier is selected for the first stage[17][18] .A common source circuit is selected as the output stage due to high input impedance, moderate voltage gain, low output impedance and good output swing[21]. A common gate topology is considerable due to its good gain, but above-mentioned qualities for an amplifier are not satisfied by the topology[22]. The selected topology is modified by including inductance along with resistive components in drain and source. The drain inductance along with diode-connected NMOS device acts as a load and source inductance in series with triode NMOS device acts as a degenerative component. Further points related to this are discussed in the following sections.

2.1 Folded Cascode Amplifier : First Stage

Cascoded op amp was chosen over two-stage opamp as the first stage due to performance limitations such as inadequate gain, short bandwidth and poor PSRR of the latter[14]. In folded cascode amplifier stage the cascading is arranged in its output stage and merged with a distinctive implementation[15].In folded cascode circuit the impedance at nodes other than at input and output is in the order of gm (low) and thus the speed of the op-amp can be improved[16]. Normally, in differential amplifiers, gain will degrade to half in the case of single-ended output. A folded cascode amplifier answers the aforementioned obstacle and ensures sufficient gain with satisfying bandwidth. According to the rise in load capacitance of first stage, the phase margin hikes and so the folded cascode amplifier(FCA) achieves stability. The load capacitor serves as a short circuit to high-frequency signal, and thus the bandwidth limits as load capacitance rises. This implies that the node capacitance due to parasitics should be reduced to get decent balance between gain,bandwidth and phase margin.

Figure.2 manifests the schematic description of a folded cascode amplifier[14].This topology as first stage overwhelms the limitations of single-ended differential amplifier and two-stage amplifier, which seems complicated to gain optimized performance. The amount of I_3, I_4, I_5 has originated in such a way that the flow in the current mirror of the first stage never more declines to a nullity. The design of current I_4 and I_5 was made to preserve its value within I_3 and $2I_3$ to seize I_6 and I_7 as nonzero. The cascode topology framed by M_9 and M_{11} from the drain of M_7 to ground provokes an up current in M_2 which exhibits very high resistance in the drain of M_5 as in the source of M_7.

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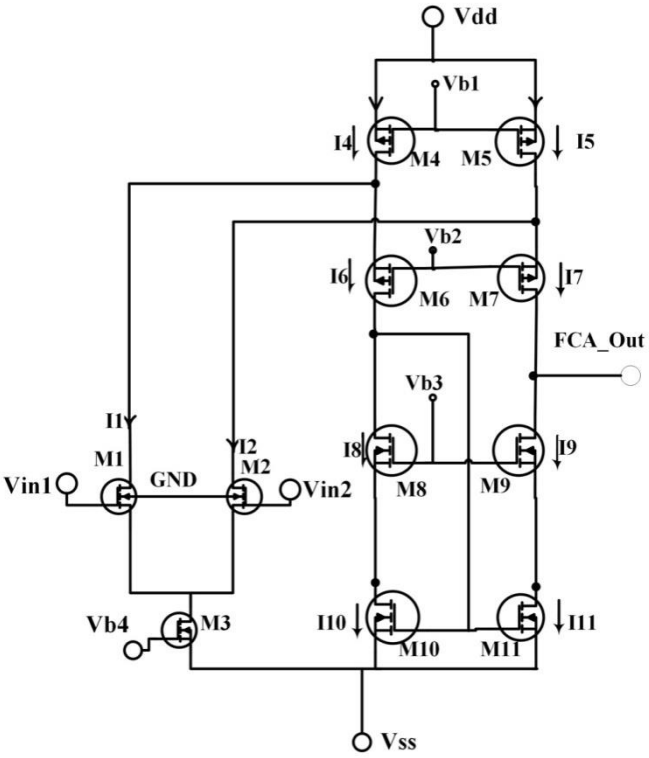

Figure 2. Schematic diagram of First Stage

2.2 Inductively Modified Common Source Amplifier as Second Stage

To ensure a significant additional enhancement in performance parameters, the first stage folded cascode amplifier is cascaded with a refurbished common source amplifier. Even though the common source amplifier manifests low gain, it grants enough input common-mode range, more reliable output swing and an enhanced bandwidth. A simple structure for the following stage is drawn in Figure.3 where a string combination of drain inductance L_d and drain resistance R_d which is replaced with M_{Rd} in triode region is employed as load. Here, stability is one of the significant interests other than bandwidth and gain. The drain inductance L_d controls the phase margin, which is a degree of stability. MOSFET in the drain is configured in the triode region by joining gate and source and by threshold voltage control. This connection contributed resistance in series with L_d; furthermore, this overwhelms difficulty of fabricating resistors in chips. The deployment of degeneration impedance Z_s in series with the source terminal serves as negative feedback, which enhances bandwidth and deteriorates gain. In degeneration impedance, an inductance connected in series with an nMOS M_{Rs} which is configured in triode region to employ this as resistance. The embodiment of inductance L_s caused dependence aloft frequency and through improving speed performance. At high frequency, the inductive reactance will be higher due to their straight relationship, and so the source impedance rises. Thus the voltage drop across Z_s becomes more, and then the negative feedback increases, which enhances bandwidth and degrades gain. In our recommended network, an LC circuitry attached between the drain and gate of M_{out} upgrades stability. Here a series connection of R_f and C_f is parallelly linked with L_f, and this aggregates LC network. This circuit with frequency dependant drain impedance efficiently enhances stability. The junction capacitances C_{gd},C_{gs} and C_{db}, play a significant role in the enhancement of bandwidth. These junction capacitances depend inversely on bandwidth; furthermore, parasitics necessitate to degrade to augment bandwidth. The analysis of our second stage is addressed in the following section.

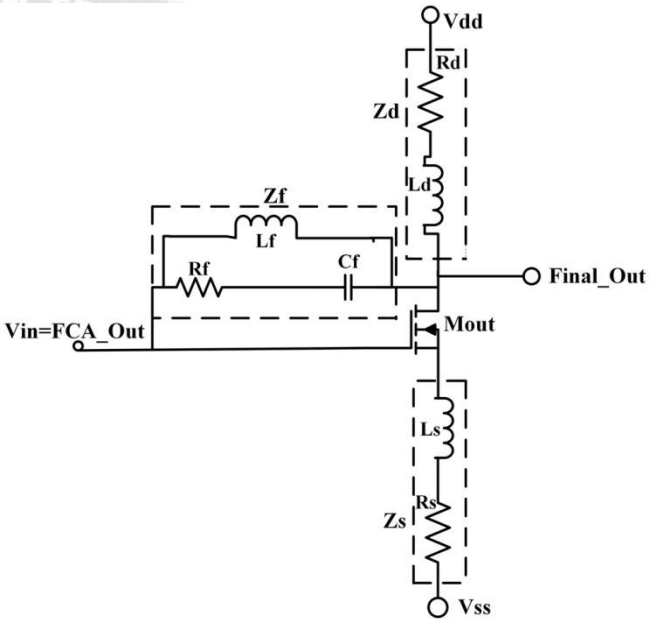

Figure 3. Schematic equivalent diagram of second stage

2.3 Description of proposed system

In our proposed wideband amplifier, a folded cascode amplifier is cascaded with inductively modified common source amplifier as in Figure.4 to enhance performance speed. The recommended circuit incorporates folded cascode topology by renovated common source amplifier to attain refined performance parameters in terms of bandwidth, gain and stability.

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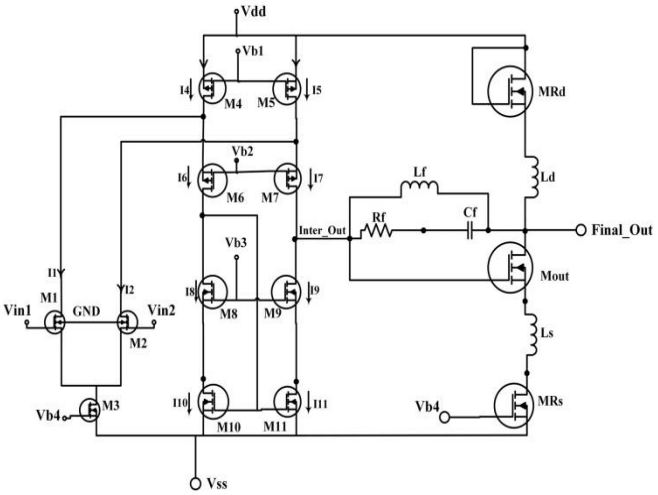

Figure 4. Schematic diagram of proposed system

Based on Equation.6 the output resistance of the initial stage is directly proportional to gain and inversely to bandwidth, and thus its output resistance is reasonably planned to capture quality outcome. According to the value of frequency advances the impedance at the drain Z_d and that at source Z_s rises. Then the inductance values were determined to capture the requisite range of gain and bandwidth.

In this paper, the circuit performances with and without feedback, which comprises a resistor and reactive components have been studied. Due to the direct relationship between frequency and the inductive reactance, the feedback inductor exhibits substantial impedance at high frequency. Therefore the gain enhances further at that frequency, the feedback capacitor shows low impedance, and this improves the stability performance of the circuit.

III. DESIGN AND ANALYSIS

3.1 Analysis of Initial Stage

The folded cascode amplifier's small-signal model, which is our primary stage is presented in Figure.5.

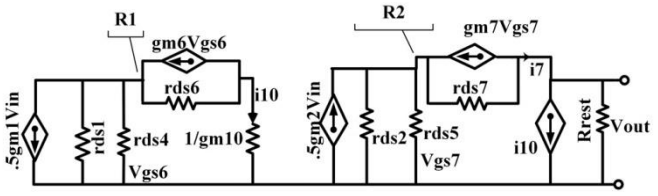

Figure 5. Small Signal model of first stage

R_1& R_2 are the resistances looking into sources of M_6& M_7.

From the model,

$$R_1 = \frac{(r_{ds6}+\frac{1}{g_{m_{10}}})}{1+g_{m_6}.rds_6} = \frac{1}{gm_6} \quad (1)$$

$$R_2 = \frac{rds_7+R_{rest}}{1+gm_7.rds_7} \approx \frac{R_{rest}}{g_{m_7}.r_{ds_7}} \quad (2)$$

where

$$R_{rest} \approx gm_9 . rds_9 rds_{11}$$

The drain current of M_{10} is

$$I_{10}=\frac{-.5gm_1V_{in}(r_{ds1}||r_{ds4})}{(R_1+rds_1||rds_4)} \approx -.5gm_1.V_{in} \quad (3)$$

The drain current of M7 is

$$I7 = \frac{.5gm_2.V_{in}(rds_2||rds_5)}{\frac{R_{rest}}{gm_7.rds_7}+(rds_2||rds_5)}$$

$$\approx \frac{.5gm_2V_{in}gm_7.rds_7}{R_{rest}(gds_2+gds_5)+gm_7.rds_7} \quad (4)$$

where $(rds_2||rds_5) = gds_2 + gds_5$

The net influence of current I_7 and I_{10} is transpiring over Rout; Also it causes an output voltage, indicated below.

$$V_{out} = \left(\frac{.5gm_2V_{in}}{GDS+1} + .5gm_1V_{in}\right)R_{out} \quad (5)$$

$$\frac{V_{out}}{V_{in}} = .5gm_I\, R_{out}\left(\frac{2+GDS}{1+GDS}\right) \quad (6)$$

where $GDS = \frac{R_{rest}(gds_2+gds_5)}{gm_7.rds_7}$

Based on the analysis , output resistance R_{out} is directly proportional to gain and inversely to the dominant pole. Transconductance and thereby output resistance is adjusted to attain proper bandwidth as well as gain according to the relevance. Also, the bandwidth depends inversely on capacitance. The capacitive effects have to be reduced to improve bandwidth without degeneration in gain.

3.2 Inductively modified Common Source Amplifier

The proposed secondary stage's small-signal paradigm is discussed in Figure.6. In this section, we analyses the circuit with and without feedback network indicated in dotted line. For analysis, the MOSFETs are regarded as without channel length modulation. So

Drain impedance, $Z_d = L_d\left(s + \frac{R_d}{L_d}\right)$ (7)

Source impedance $Z_s = L_s\left(s + \frac{R_s}{L_s}\right)$ (8)

Feedback impedance $Z_f = sL_f||(R_f + \frac{1}{sC_f})$

$$= \frac{sR_f(s+\frac{1}{R_fC_f})}{(s^2+s\frac{R_f}{L_f}+\frac{1}{L_f.C_f})} \quad (9)$$

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Table 1 DESIGN PARAMETERS OF THE CIRCUIT

COMPONENTS	VALUES	UNITS
M_1& M_2	12/100	µm
M_3	120/100	µm
M_4& M_5	120/100	µm
M_6& M_7	240/100	µm
M_8& M_9	120/100	µm
M_{10}& M_{11}	120/100	µm
M_{Rd}	120/1	µm
M_{out}	120/110	µm
M_{Rs}	30/3	µm
R_f	10	MΩ
C_f	1	aF
L_f	1	nH
L_d	1	nH
L_s	2.5	µH
C_L	1	pF

Based on equations7,8 & 9, at low frequency, the drain and source impedance are small and at high frequency these are high. Drain impedance and source impedance increase with frequency. But the behavior of feedback impedance is different.

Let us analyze the feedback network.

Usually, in the case of a parallel network, the equivalent impedance is lower than the lowest impedance. In the low frequency of operation, impedance provided by L_f is smaller than the impedance of branch having C_f and L_f. So at this condition, equivalent impedance is lower than the impedance by L_f.

As frequency increases, L_f impedance is becoming higher and C_f impedance is becoming lower. But due to the presence of R_f, there is a minimum impedance R_f in that path. So at that time, the total impedance of the parallel feedback network will increase up to R_f since the path is connected parallel with L_f.

Now let us consider the design without feedback network. The current passing through Z_s is $gm_{out}.V_1$ then employing KVL and KCL yields,

$$V_{in} = V_1(1 + gm_{out}.Z_s) \quad (10)$$

$$V_{out} = -gm_{out}.V_1.Z_d \quad (11)$$

$$\frac{V_{out}}{V_{in}} = \frac{-Zd}{Zs + \frac{1}{gm_{out}}} \quad (12)$$

Based on equation.12 the gain can be improved by increasing gm_{out} and Z_d and by decreasing Z_s. As a result, the Zs value should be kept to a minimum. This can be possible by choosing a lower source inductance. The increment in g_{mout} will improve gain and gain-bandwidth product of the circuit. The transconductance is directly proportional to transistor aspect ratio. i.e, the transconductance gm_{out} can be improved either by increasing width or by decreasing length of the transistor M_{out}. But the increase in width may cause a hike in parasitic capacitance. This will reduce bandwidth. So the width and length of the transistor selected carefully.

Putting the equations 7 & 8 in equation 12, then the gain is

$$\frac{Vout}{Vin} = \frac{L_d\left(s + \frac{R_d}{L_d}\right)}{L_s\left(s + \frac{R_s}{L_s} + \frac{1}{gm_{out}.L_s}\right)} = \frac{-K_L(s + K_{Zd})}{(s + K_{Zs})} \quad (13)$$

Where $K_L = \frac{L_d}{L_s}$; $K_{Zd} = \frac{R_d}{L_d}$; $K_{Zs} = \left(\frac{R_s}{L_s} + \frac{1}{gm_{out}.Ls}\right)$;

Solution to the situation amidst feedback circuitry, Applying Kirchhoff's current law,

$$\frac{(V_{in} - V_{out})}{Z_f} = gm_{out}.V_{in} + \frac{V_{out}}{Z_d} \quad (14)$$

Applying kirchoff's voltage law,

$$V_{in} = V_1(1 + gm_{out}.Z_s) \quad (15)$$

From equations 14 &15,

$$\frac{V_{out}}{V_{in}} = \frac{(Z_f||Z_d)(\frac{1}{Z_f} + gm_{out}.\frac{Z_s}{Z_f} - gm_{out})}{(1 + gm_{out}.Z_s)} \quad (16)$$

The impedances thus derived without considering channel length modulation is,

$$Z_{in} = \frac{(Z_f + Z_d)(Z_s + \frac{1}{gm_{out}})}{Z_d + Z_s + \frac{1}{gm_{out}}} \quad (17)$$

$$Z_{out} = \left(Z_f||Z_s||Z_d\right) \quad (18)$$

The input impedance of an ideal amplifiers should be high, while the output impedance should be low. The input impedance will increase drastically as Z_f increases and the output impedance will reduce as any of the impedance in Z_f,

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Z_d, Z_s decreases. To get high input impedance, the drain impedance and feedback impedance are making high. Also, the low value of source inductance is selected to reduce Zs and thereby low output impedance.

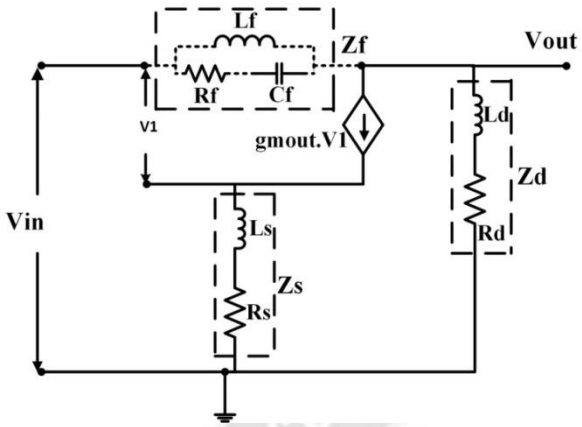


Figure.6.Small signal model of second stage

IV. RESULTS AND DISCUSSIONS

The simulation of the proposed circuit (Figure.4) is done in cadence virtuoso tool. The circuit consists of two stages which are folded cascode, and inductively transformed common source amplifier. The proposed wideband amplifier design is experimented stage by stage to attain reasonable gain, bandwidth and stability. Initially, the folded cascode stage was designed and analyzed based on trial and error method. The width and length of transistors and bias current were swept to obtain reliable performance values. Table I gives the dimensions; width and length of transistors, resistors, capacitors and inductors of the prescribed circuit. The dc analysis was performed to observe threshold voltage, junction capacitances and transconductance values while controlling bias voltage and transistor dimensions that gave the best outcome.

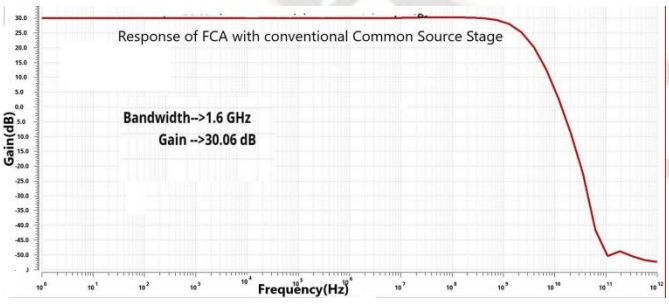
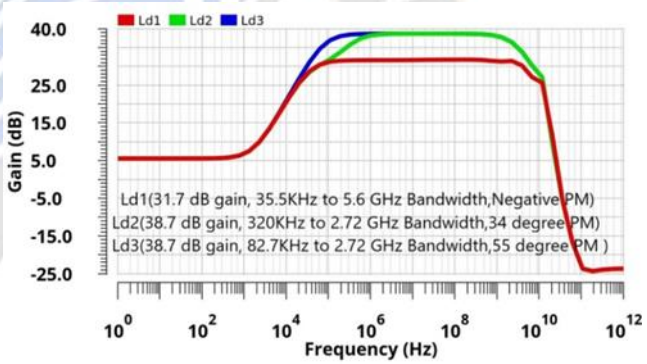


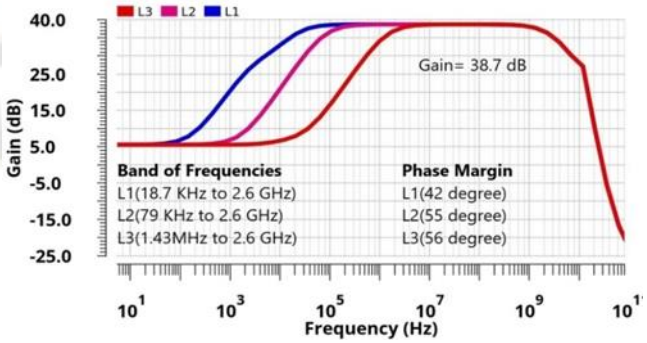
Figure.7.Frequency response of the system with pure common source amplifier as second stage.

After the simulation of the cascode stage, a simple common source amplifier without any inductor and feedback was cascaded, experimented and simulated. Aforementioned work resulted in relatively low bandwidth as 1.6GHz, 30dB gain and 26-degree phase margin as shown in Figure.7.The result obtained after cascading common source as the second stage was not enough to satisfy the requirement as a wideband amplifier and hence a new topology with inductor at source and drain along with some resistance was proposed and designed. The circuit was simulated by varying dimensions of transistor M_{out} and it was fixed at the proper point. The simulations with different inductor values were also performed in this work.

Figure.8.a shows frequency responses based on different drain inductor values. For less than Nano range of inductance values, the bandwidth is in GHz, but the stability is deficient. With increment in drain inductance to a higher range (greater than 1µH) the bandwidth decreased, but it displayed excellent stability.In this for lowest inductance L_{d1},the response is with 30dB gain, from 35.5 kHz to 5.6 GHz band,but it exhibits poor stability. With highest inductance L_{d3} the output is 38.7dB, from 82.7 kHz to 2.72 GHz band and 55-degree phase margin(excellent stability).The reason behind this result is discussed in section.3.With low drain inductance values, the bandwidth improves and gain degrades due to low drain impedance. Similarly, high drain inductance improves gain and degrades bandwidth. This can be observed in the result.



a) for various L_d



b)for different L_f

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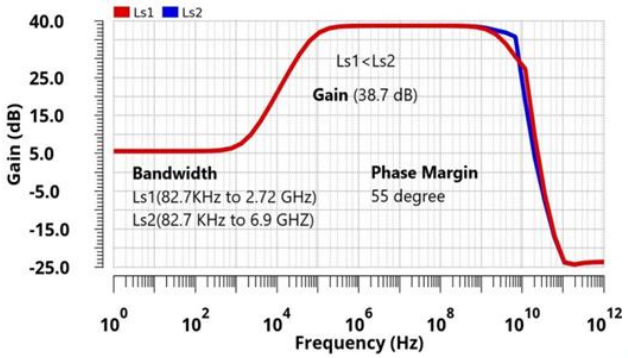
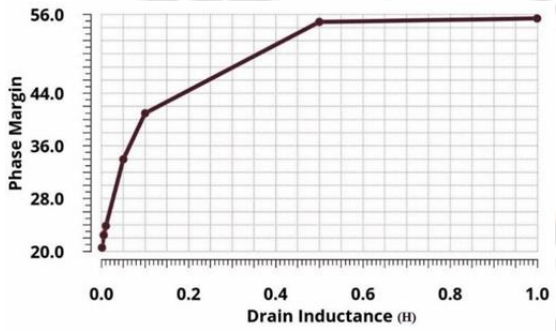


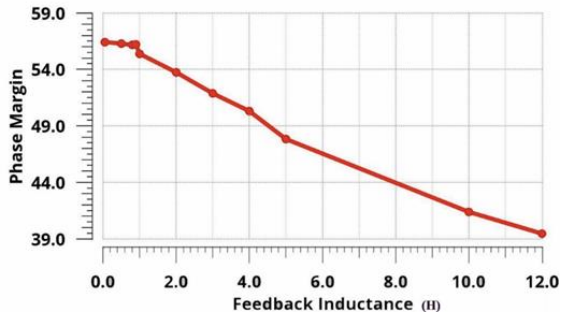
c)for different L_s

Figure.8.Frequency responses on different Inductances

Figure.8b shows the response of the proposed circuit for different feedback inductance values. Here as L_f increased, the bandwidth enhanced and it could be inferred that due to high inductive reactance the lower cut off frequency can be lowered to 0Hz with high inductance value. It may be noted that there was no much improvement in upper cutoff frequency. This bandwidth was not enough to meet our specifications. Hence various values of source inductance were trialed, Figure.8c shows the response for two L_s values among them. As the source inductance increased more than L_{s2}, a spike appeared in the reaction, and at this value of inductance, the optimum output obtained is about 38.7 dB gain,in 82.7KHz to 6.95GHz band and 55-degree phase margin. Figure.9 shows the variation of phase margin according to drain and feedback inductances. It displays a stable performance on higher drain inductance values(Figure.9a) and with small feedback inductance values(Figure.9b).

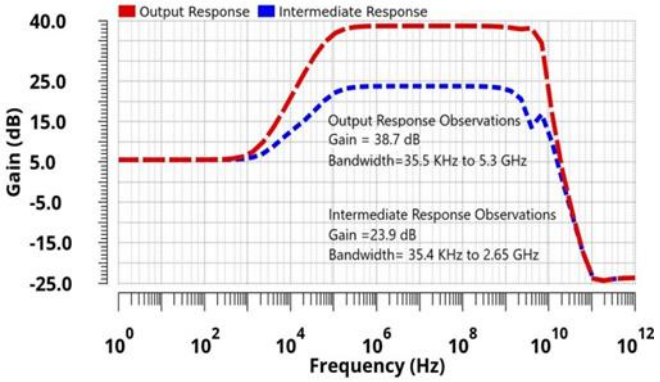


a) on different L_d

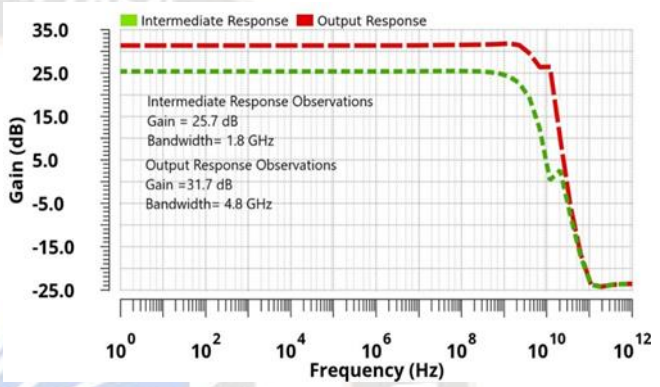


b) on different L_f

Figure.9.Phase Margin Variation



a)with compensation

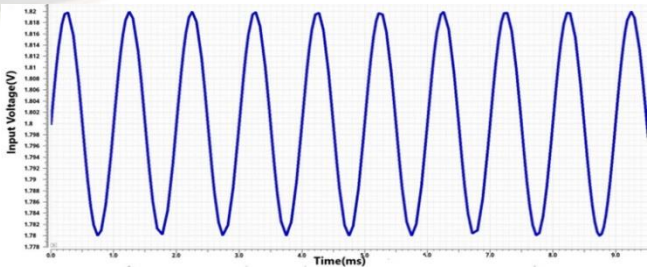


b)without compensation

Figure.10Comparison between responses at first & second stage

Figure.10a shows the response comparison at the output of two stages of the system with feedback. This graph indicates that the second stage improved the gain and bandwidth from 23.9dB, 35KHz - 2.65GHz to 31.7dB, 35KHz - 5.3GHz respectively.Figure.10b indicates that without the feedback circuit,the response is upgraded from 22dB,1.8GHz to 30 dB 4.8GHz.The above results, imply that the gain and bandwidth have simultaneously improved, while by controlling the feedback part, we can modify the band of frequency.

a)Input Signal



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b) Output Signal

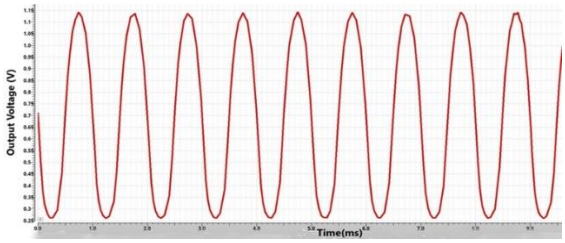

Figure.11.Time domain responses at input and output

Figure.11 the time frequency response just at input & output stages is displayed. Here it is observed that the 30mV input is amplified to 1V signal and the common mode measured is 80dB closely.Figure.12 demonstrates the proposed circuit's optimum magnitude and phase response.

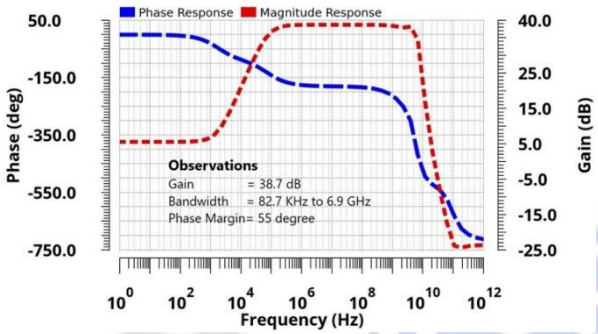

Figure.12.Magnitude and Phase response of the proposed system

The simulated outcomes in this effort are summarized in Table.II.The wideband power amplifier in [4] presents 26 dB gain,4.5 GHz BW(18.8 GHz to 23.3 GHz), 21GHz UGB and 70º phase margin.The evaluated bandwidth in [8] is from 700MHz to 4.6GHz, and its gain is 10.8 dB.

Table II Performance Comparison of proposed circuit

Parameter	K-Band [4]	WFG LNA [5]	Tunable WB [8]	This Work (fb)	This work (No fb)
Techn.	180nm	130nm	65nm	90nm	90nm
Gain(dB)	26	10.8	15.5	38.7	30.7
BW(Hz)	4.5G	3.9G	5.34G	6.95G	4.8G
UGB(Hz)	21G		29G	30G	10G
PM	70º	70º	80º	55º	34º
Pd(W)	---	6.16m	-----	1.3m	1.4m
FOM_L	---	-----	----	8.92	8.6
FOM_S	86.8	.74	5.48	194	301
Area (mm^2)	1.12	.0077	----	.00086	.00082
Flatness	No	No	No	Yes	Yes
Supply (V)	5.6	12	1.4	1.8	1.8

The wideband amplifier that uses a bandwidth extension circuit in [5] measured 15.5 dB gain,5.34 GHz bandwidth from 38GHz to 43.3GHz and UGB of 29GHz.Even though some previous studies reported a high frequency of operation; their gain and phase margin were not adequate. In addition their response is not flat and power consumption is comparatively high[12].Our work, focused on enhancing bandwidth without a severe drop in gain and phase margin. Since the focus is to keep flat band response, high gain and bandwidth there is a challenge to improve the figure of merit [13] with the same design. Different Figure of merit equations are discussed in the literature and it is varied from system to system. This work included two familiar figure of merit calculations. The large signal figure of merit which estimates large-signal performance versus power, $FOML = \frac{S.RxC_L}{I_{suppy}} = \frac{I_{maxL}}{I_{supply}}$,where I_{supply} is the total current consumption. The next is the small signal figure of merit $FOMS = \frac{100xGBWxC_L}{I_{suppy}}$(MHz.pF/μA) which is a measure of small-signal performance versus power[19].and these values are calculated and given in Table.II for easy comparison. Simulation results suggest that the obtained gain, bandwidth and phase margin are superior over those reported in literature. In addition a relatively low power dissipation and a reasonable flat response makes the proposed circuit a superior choice over hitherto reported circuits.

CONCLUSION

The design of a modified wideband amplifier has been analyzed in this paper. The designed amplifier attained better result in terms of gain, bandwidth and phase margin during its simulation. The alteration using inductively modified common source amplifier cascaded with a folded cascode amplifier helped to achieve reliable performance parameters. Uniquely we propose the inclusion of three reactive impedances for getting the most authentic values. The drain impedance, inductance in particular helped to adjust stability to a decent level. The influence of source reactance improved upper cut off frequency and thereby bandwidth has been magnified to outstanding value. The presence of reactive feedback component can be used to adjust lower cutoff frequency and bandwidth. In this work,a well-balanced treatment has been done without impacting other parameters. The circuit with and without feedback has been simulated and obtained 38.7dB gain,6.95GHz bandwidth, 55-degree phase margin and 30.7dB gain ,4.86 GHz bandwidth ,34 degrees respectively. The observed results look promising for a wideband amplifier as compared to previously reported results\cite{RefJ4},\cite{RefJ5},\cite{RefJ8}. In addition the system consumed less power. This work can be extended by replacing inductors with equivalent MOS circuits and this will improve overall performance.

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