

# Energy-Efficient Cyclic-Coupled Ring Oscillator With Delay-Based Injection Locking

Okko Järvinen<sup>1</sup>, Vishnu Unnikrishnan<sup>1</sup>, *Member, IEEE*, Iliia Kempfi, Santeri Porrasmäa, Kari Stadius<sup>1</sup>, *Member, IEEE*, Marko Kosunen<sup>1</sup>, *Member, IEEE*, and Jussi Rynnänen<sup>1</sup>, *Senior Member, IEEE*

**Abstract**—This brief presents a new tristate-based delay cell to realize the recently proposed delay-based injection locking in ring oscillators. The circuit is then applied to implement a cyclic-coupled ring oscillator (CCRO). Compared to an inverter-based CCRO with multi-drive injection, the proposed circuit eliminates the static short-circuit current drawn from the supply when drive circuits are in conflicting logic states, thus reducing the power consumption of the CCRO. The functionality and improved energy efficiency of the proposed circuit is demonstrated with circuit simulations of a CCRO implemented in a 28-nm CMOS process. The CCRO employing the proposed technique achieves up to 25% lower power consumption and over 20% lower power-delay product (PDP) compared to the inverter-based CCRO.

**Index Terms**—Cyclic-coupled ring oscillator (CCRO), time-domain, time resolution, sub-gate-delay, time-to-digital converter.

## I. INTRODUCTION

SCALING of CMOS technology towards deep sub-micron process nodes presents challenges for analog circuits in terms of reducing supply voltages and intrinsic device gains. On the other hand, digital circuits benefit from the scaling to deliver increased operating speed and improved energy efficiency. Time-based circuit techniques aim to leverage on this trend by realizing analog signal processing functions with digital circuits. Consequently, an increasing number of time-based data converter circuits have been proposed in recent years [1], with an aim of addressing the growing demand for energy-efficient high performance data converters. Ring oscillator (RO)-based converters, such as voltage-controlled oscillator (VCO)-based analog-to-digital converters (ADCs) [2], [3] and RO time-to-digital converters (TDCs) [4], are examples of digital-intensive and area-efficient time-based converter architectures.

The time resolution of ring oscillator quantizers is defined by technology-limited inverter delay. This limitation can be circumvented with techniques such as Vernier-method [5], [6], pulse-shrinking [7], passive delay interpolation [8], active

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The authors are with the Department of Electronics and Nanoengineering, School of Electrical Engineering, Aalto University, 02150 Espoo, Finland (e-mail: okko.jarvinen@aalto.fi).

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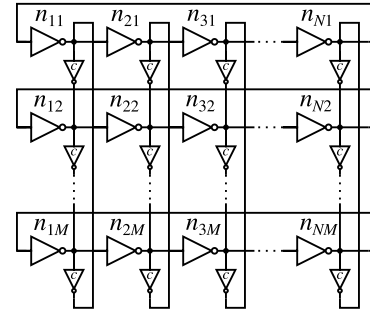


Fig. 1. Inverter-based cyclic-coupled ring oscillator with  $M$  ring oscillators of  $N$  stages.

delay interpolation [9], multi-path ring oscillators [10], [11] or cross-coupled ring oscillators [12]. Cyclic-coupled ring oscillators (CCROs) [13], [14] can be used to realize a robust delay interpolation. We have recently proposed their application in RO quantizers [15], and demonstrated its benefits with measurement results from a state-of-the-art TDC implementation [16].

Fig. 1 shows the schematic of an inverter-based CCRO circuit, where  $M$  ring oscillators, with  $N$  stages each, are coupled in a cyclic configuration. The coupling inverters, denoted with  $c$ , implement multi-drive injection locking. The resulting multi-phase injection locking [17] between adjacent ROs forces equal phase shift between individual oscillators, thus achieving a factor of  $M$  delay interpolation [13]. However, the multi-drive injection in each delay element causes short-circuit currents, resulting in high power consumption.

In this brief, we present a tristate-based delay cell for CCROs with an aim of reducing the power consumption by eliminating the short-circuit current of the inverter-based CCRO. The work is inspired by our recently published delay-based injection locking technique [18], which employs a separate XNOR gate for controlling a tristate inverter to implement locking. The delay cell proposed in this brief combines the control logic and delay modulation into a more simple and energy-efficient circuit. The delay cell is then applied to realize a CCRO, resulting in up to 25% lower power consumption and over 20% lower power-delay product (PDP) compared to the inverter-based CCRO.

The rest of this brief is organized as follows. Section II presents analysis and simulation results of the proposed delay

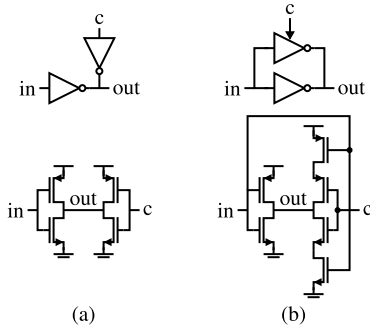


Fig. 2. Delay cell schematics for (a) the inverter-based and (b) the proposed tristate-based implementations, respectively.

TABLE I  
TRUTH TABLE FOR THE DELAY CELL FUNCTION

in	c	out	delay
1 → 0	0	0 → 1	$t_{p,\min}$
1 → 0	1	0 → 1	$t_{p,\max}$
0 → 1	0	1 → 0	$t_{p,\max}$
0 → 1	1	1 → 0	$t_{p,\min}$

cell in terms of delay modulation behavior and current consumption. Section III presents a CCRO implementation using the proposed delay cell, along with simulation results comparing the performance to the inverter-based counterpart. Section IV concludes this brief.

## II. ENERGY-EFFICIENT TRISTATE-BASED DELAY MODULATION

Fig. 2(a) shows the schematic of a delay cell of the inverter-based CCRO in Fig. 1. The delay cell is driven by two inverters: the main inverter and coupling inverter. The main inverter with the input signal “in” is stronger and it defines the state of the output signal “out”. The weaker coupling inverter injects the node with coupling signal “c”, which affects the propagation delay of the main inverter. Table I shows the logic states of “in”, “c” and “out”, and the propagation delay of the main inverter for the delay cell in Fig. 2(a). The output voltage is defined by the signal “in”, whereas the delay switches between two discrete values  $t_{p,\min}$  and  $t_{p,\max}$  depending on the states of “in” and “c”.

A drawback of the inverter-based delay cell in Fig. 2(a) is the short-circuit current drawn between the supplies during conflicting input logic states. The short-circuit current flows directly from supply to ground, and thus it has no effect on the delay of the cell. Consequently, it can be eliminated without affecting the delay cell functionality. Fig. 2(b) shows the proposed method, where a parallel coupling circuit is introduced to provide the delay modulation. The coupling circuit is a parallel tristate inverter with modified control connection, where a common gate voltage is used for the PMOS and NMOS transistors driven by “c” as opposed to inverted gate voltages. When “in” and “c” are in the same logic state, the respective pull-up or pull-down branch of the coupling circuit is conducting, resulting in low delay ( $t_{p,\min}$ ). For conflicting input logic states, both branches of the coupling circuit are off, resulting in high delay ( $t_{p,\max}$ ). Thus, the delay modulation

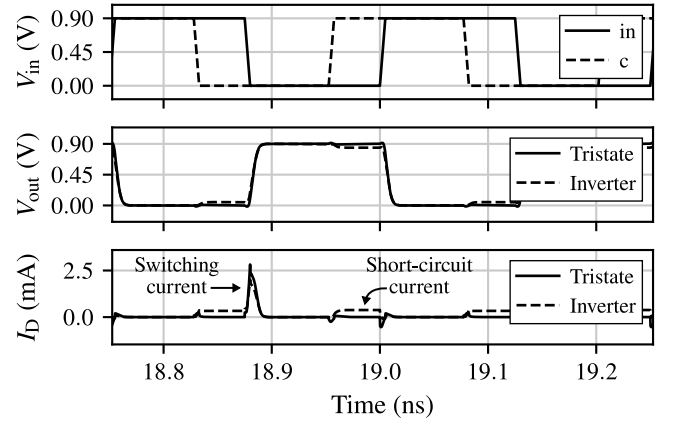


Fig. 3. Pre-layout transient simulation of inverter- and tristate-based delay cells. A single delay cell is excited with a 4-GHz input signal “in” with phase-offset coupling signal “c”.

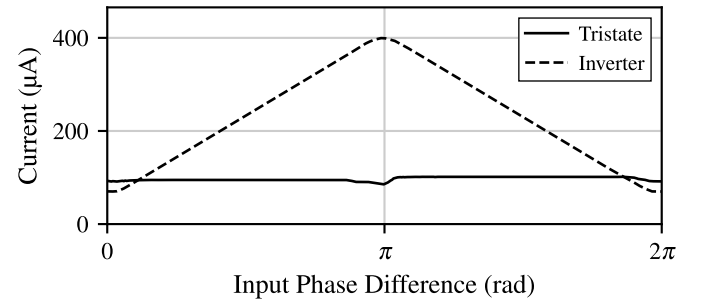


Fig. 4. Pre-layout simulation showing the current drawn by the delay cells as a function of the phase difference between “in” and “c”.

shown in Table I is preserved and the static short-circuit current paths are eliminated.

### A. Current Consumption in Delay Modulation

A pre-layout transient simulation of the two delay cells is presented in Fig. 3. The top figure shows the input voltages “in” and “c” excited with 4-GHz clock signals. The middle figure shows the output voltages, where the delay for both cells is  $t_{p,\min}$  and both cells show glitch-free operation. The bottom figure shows the supply current drawn by each cell along with annotations for the short-circuit current and active switching current. The simulation shows that the tristate-based cell effectively eliminates the short-circuit current.

Fig. 4 shows the simulated average current consumed by a delay cell as a function of the phase shift between “in” and “c”. The current drawn by the inverter-based delay cell increases significantly when the phase difference approaches  $\pi$ , whereas the tristate-based delay cell demonstrates a constant current consumption across all input phase differences. Near the zero phase, the inverter-based cell consumes slightly less current than the tristate cell due to the overhead of the two additional transistors in the tristate cell.

### B. Effective Delay Modulation

This section discusses the delay modulation achieved by the two delay cells in Fig. 2. The difference between the delays  $t_{p,\min}$  and  $t_{p,\max}$  directly determines the strength of injection locking. Here, we develop expressions to predict the effective

delay modulation of the two delay cells using their high-to-low propagation delays. Additionally, the expressions are validated using circuit simulations.

The delay analysis is based on linear approximation of the inverter propagation delay

$$t_p \approx \frac{C_L V_{DD}}{2I_{n/p}}, \quad (1)$$

where  $C_L$  is the load capacitor,  $V_{DD}$  is the supply voltage, and  $I_{n/p}$  is the NMOS/PMOS current charging or discharging the capacitor [19]. The saturation current of an NMOS transistor (ignoring channel length modulation) is

$$I_n = \frac{W_n}{2L_n} \mu_n C_{ox} (V_{GS} - V_{T,n})^2 \propto \frac{W_n}{L_n}, \quad (2)$$

where the current is directly proportional to the NMOS transistor width to length ratio.

The propagation delay of the inverter-based delay cell is affected by both main and coupling inverter currents. Minimum high-to-low delay is achieved when both inverters discharge the load capacitor. In this case, the discharge current in (1) is the sum of main and coupling inverter NMOS currents, which are directly proportional to the NMOS transistor dimensions. Thus, the propagation delay is proportional to the transistor dimensions as

$$t_{p,inv,min} \propto (W_{m,n}/L_{m,n} + W_{c,n}/L_{c,n})^{-1}, \quad (3)$$

where  $W_{m,n}$  and  $W_{c,n}$  are the main and coupling inverter NMOS transistor widths, and corresponding  $L$  are the respective transistor channel lengths. The maximum delay occurs when the PMOS transistor of the coupling inverter causes an opposing current, resulting in

$$t_{p,inv,max} \propto (W_{m,n}/L_{m,n} - W_{c,p}/L_{c,p})^{-1}, \quad (4)$$

where  $W_{c,p}$  and  $L_{c,p}$  are the coupling inverter PMOS width and length, respectively.

Similar expression is derived for the proposed tristate-based delay cell. In the minimum delay case, both pull-down branches of the main inverter and the tristate inverter are active, and the propagation delay is

$$t_{p,tri,min} \propto (W_{m,n}/L_{m,n} + W_{c,n}/(2L_{c,n}))^{-1}. \quad (5)$$

Here, the stacked transistors in the tristate inverter are assumed to be equally sized, which results in halving of the effective width. In the maximum delay case, only the main inverter is discharging the capacitor, which results in

$$t_{p,tri,max} \propto (W_{m,n}/L_{m,n})^{-1}. \quad (6)$$

The respective analysis can be repeated for low-to-high delays easily due to the symmetry of the pull-down and pull-up networks.

We define the effective delay modulation  $\eta$  as the ratio of the maximum delay to the minimum delay. For the inverter-based cell, the ratio is

$$\eta_{inv} = \frac{t_{p,inv,max}}{t_{p,inv,min}} = \frac{W_{m,n}L_{c,p} + W_{c,n}L_{m,n}}{W_{m,n}L_{c,p} - W_{c,p}L_{m,n}}, \quad (7)$$

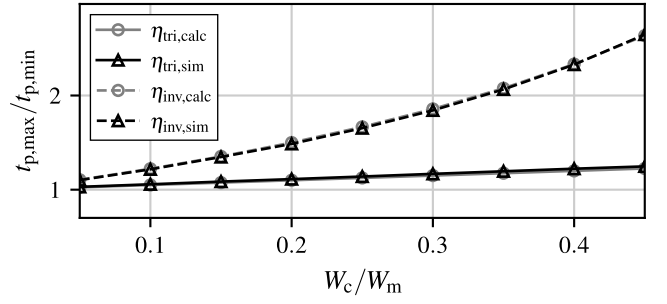


Fig. 5. Pre-layout simulated and calculated effective delay modulation  $\eta$  (ratio between maximum and minimum propagation delays) as a function of ratio of coupling and main transistor widths.

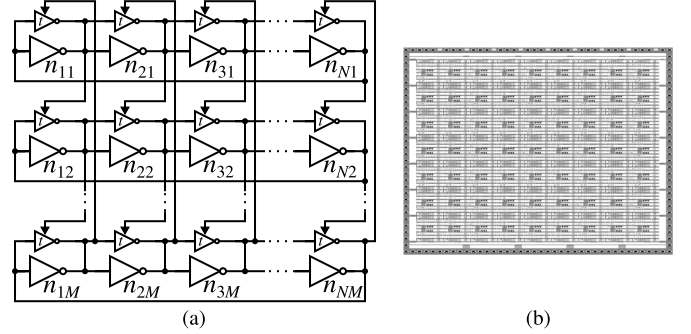


Fig. 6. (a) Schematic of the proposed tristate-based CCRO and (b) a prototype layout of a  $9 \times 7$  implementation with  $104 \times 80 \mu\text{m}^2$  area.

and for the tristate-based cell the ratio is

$$\eta_{tri} = \frac{t_{p,tri,max}}{t_{p,tri,min}} = 1 + \frac{W_{c,n}L_{m,n}}{2W_{m,n}L_{c,n}}. \quad (8)$$

For both inverter- and tristate-based delay cells,  $\eta$  approaches one (no delay modulation), when the coupling transistor width  $W_c$  is minimized. However, when  $W_c$  grows relative to  $W_m$ , the effective delay modulation of the inverter-based cell in (7) grows exponentially, whereas the growth is linear for the tristate-based cell in (8). For the inverter-based cell, the upper boundary of the width ratio is  $W_c = W_m$ , where  $\eta$  approaches infinity. For the tristate-based cell, no such boundary is evident, but in practice over-sizing the tristate inverter causes self-loading and saturates the decrease in propagation delay. Larger value of  $\eta$  corresponds to stronger coupling, which can, for example, enable wider lock range in the case of injection locked ROs [18], and improved mode stability and phase noise in CCROs [14].

Fig. 5 presents the calculated and simulated effective delay modulations for both inverter- and tristate-based delay cells over a range of transistor width ratios. In the simulation, the NMOS and PMOS sizes are equal such that  $W_{m,n} = W_{m,p} = W_m$  and  $W_{c,n} = W_{c,p} = W_c$ , and the device lengths are set to the minimum. The figure shows close agreement between the values calculated from (7) and (8) and the corresponding simulated values.

### III. TRISTATE-BASED CYCLIC-COUPLED RING OSCILLATOR

The proposed tristate-based delay cell is applied to realize a CCRO as shown in Fig. 6(a), where parallel tristate inverters

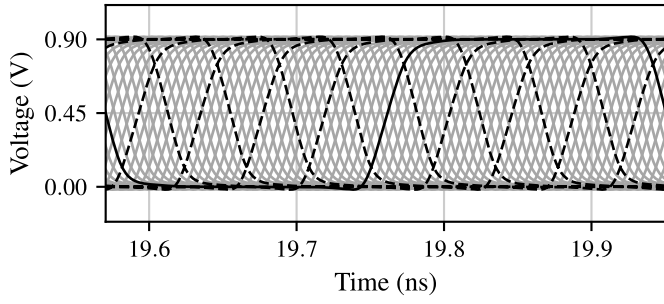


Fig. 7. Pre-layout simulation of a  $9 \times 7$  tristate CCRO. The black line is the voltage of the reference node  $n_{11}$ , and the dashed lines are the other nodes of the respective horizontal ring oscillator ( $n_{21}, n_{31}, n_{41}, n_{51}, n_{61}, n_{71}, n_{81}, n_{91}$ ). The gray lines are the remaining nodes in the CCRO.

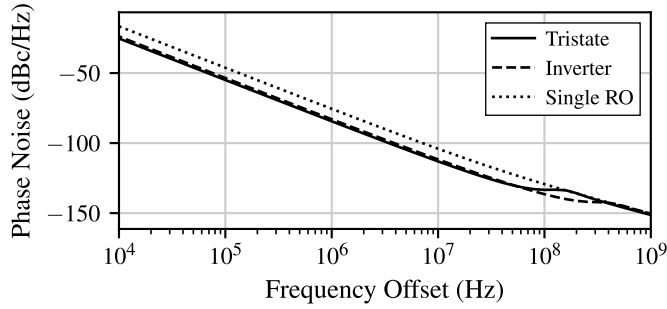


Fig. 8. Pre-layout simulated phase noise of a single ring oscillator and the inverter- and tristate-based CCROs at approximately equivalent frequencies and effective delay modulation factors.

denoted with  $t$  form vertical coupling paths between the oscillators. The functionality and efficiency of the proposed tristate CCRO is evaluated with circuit simulations of a design with dimensions  $N = 9$  and  $M = 7$ . Fig. 6(b) shows the prototype layout. Fig. 7 shows transient waveforms of the CCRO, where  $M - 1$  additional transitions are interpolated between the adjacent nodes in the horizontal ring oscillators (dashed lines). Hence, the minimal time-step in the structure is not the inverter delay, but a sub-gate delay resulting from the interpolation [15]. The operation is the same for the inverter- and tristate-based CCROs.

#### A. Noise and Mismatch

Fig. 8 shows the simulated phase noise of a single RO, inverter-based CCRO and tristate-based CCRO operating at equal frequencies and effective delay modulation factors, such that  $\eta_{inv} \approx \eta_{tri}$ . The CCROs demonstrate a phase noise improvement of approximately  $10 \cdot \log_{10}(M)$  over the single RO [14], and the phase noise between the inverter- and tristate-based CCROs is nearly identical. However, the phase noise of the tristate-based CCRO increases at a lower frequency offset compared to the inverter CCRO, which is a result of slightly lower effective delay modulation.

Delay mismatch is critical for the performance of a time-domain quantizer. Fig. 9 shows a post-layout Monte Carlo simulation with transient noise enabled to evaluate layout and device mismatch in the two CCROs. For each run, a transient simulation is executed and all time steps  $t_q$  are extracted after settling, and the means and standard deviations are

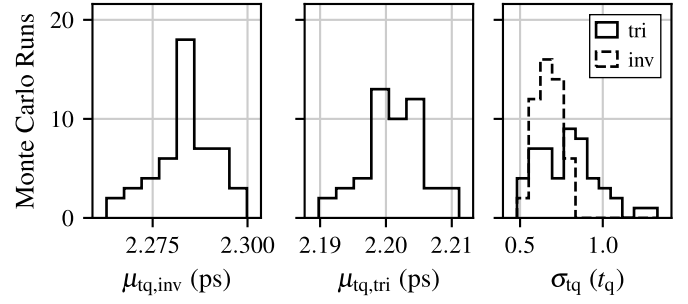


Fig. 9. Post-layout Monte Carlo simulation comparing the mean  $t_q$  values  $\mu_{t_q}$  and their standard deviations  $\sigma_{t_q}$  over 50 iterations.

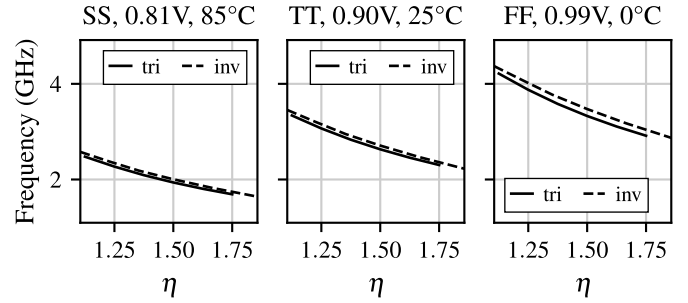


Fig. 10. Pre-layout simulated oscillation frequencies of the CCROs over a range of effective delay modulation factors  $\eta$  in three PVT corners.

calculated. The first two graphs show the distribution of the mean  $t_q$  values  $\mu_{t_q}$  extracted from the Monte Carlo runs, where only little variation is observed. The third graph describes the delay matching, where the standard deviation  $\sigma_{t_q}$  of the delays is slightly larger for the tristate-based CCRO due to the additional transistors.

#### B. Effective Delay Modulation in the CCRO

The speed and power consumption of the proposed CCRO is compared to the inverter-based counterpart over a range of effective delay modulation factors  $\eta_{inv}$  and  $\eta_{tri}$  by sweeping the coupling transistor widths from 100 nm to 600 nm and 500 nm to  $3 \mu\text{m}$ , respectively. The main inverter widths are set to  $W_{m,n} = W_{m,p} = W_m = 2 \mu\text{m}$ , and the device lengths are kept to the minimum, and a 15-fF load capacitor is added to all nodes of the CCROs to model wiring parasitics and external loading. Three symmetrical process, voltage and temperature (PVT) corners are simulated in pre-layout to verify the operation in different conditions.

The simulated stable oscillation frequency of the CCROs is shown in Fig. 10. For the tristate-based CCRO, the two additional transistors result in increased capacitive load compared to the inverter-based CCRO. However, the opposite currents in the inverter-based CCRO reduce its frequency, and hence the two frequencies are approximately equal.

Fig. 11 shows the variation of  $t_q$  as a function of  $\eta$ . The nominal time resolution  $t_q$  is calculated as

$$t_q = (2NM \cdot f_{\text{CCRO}})^{-1}. \quad (9)$$

Both implementations achieve sub-gate-delay resolution by approximately factor of  $M$ .

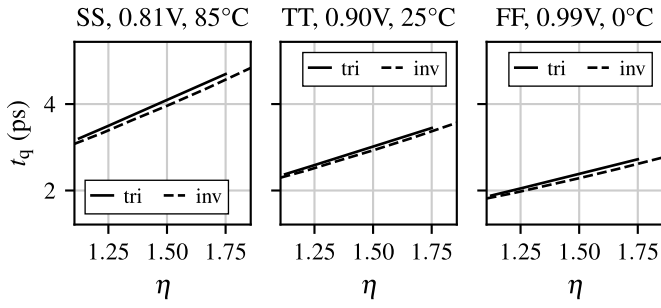


Fig. 11. Pre-layout simulated time resolutions  $t_q$  of the CCROs over a range of effective delay modulation factors  $\eta$  in three PVT corners.

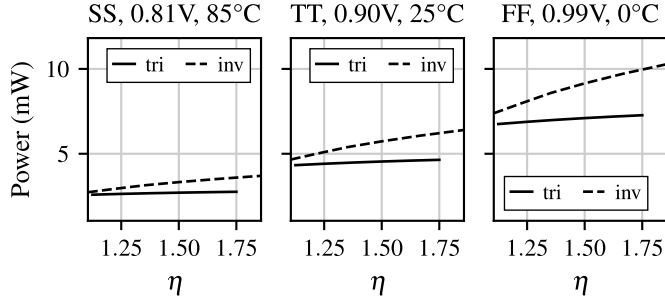


Fig. 12. Pre-layout simulated power consumptions of the CCROs over a range of effective delay modulation factors  $\eta$  in three PVT corners.

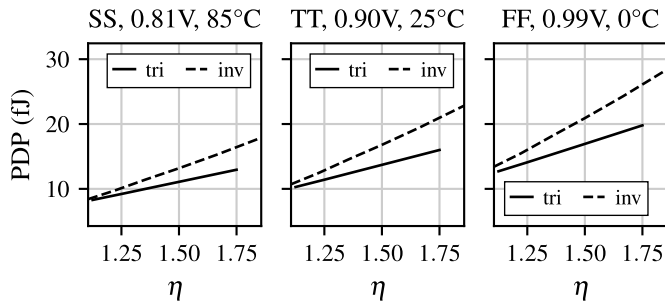


Fig. 13. Pre-layout simulated power-delay-products of the CCROs over a range of effective delay modulation factors  $\eta$  in three PVT corners.

Fig. 12 shows the power consumption of the two CCROs. The tristate-based CCRO achieves reduced power consumption over the range of  $\eta$  with up to 25% less power consumed compared to the inverter-based CCRO. The power saving is increased along with  $\eta$  due to the eliminated short-circuit current, which is larger than the active power overhead of the two additional transistors in the tristate-based delay cell. The energy efficiency of the CCRO is evaluated as the power-delay product,  $PDP = P_{CCRO} \cdot t_q$ . Fig. 13 shows the PDP of the two CCROs, where the tristate-based implementation achieves improved efficiency over a wide range of  $\eta$  with over 20% lower PDP.

#### IV. CONCLUSION

This brief presents a delay-based injection locking technique implemented with a tristate-based delay cell, which eliminates static short-circuit current in an inverter-based multi-drive delay cell. The proposed circuit is analyzed and compared to the inverter-based counterpart in terms of effective delay modulation using circuit simulations in a 28-nm CMOS

process. Furthermore, the circuit is applied to realize a CCRO, which is compared to the inverter-based CCRO. The results indicate up to 25% lower power consumption and over 20% lower PDP, demonstrating the effectiveness of the technique. The proposed cell enables energy-efficient CCROs, and hence lower energy per conversion step in time-based data converters.

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