Design of Cyclic-Coupled Ring Oscillators with Guaranteed Maximal Phase Resolution

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***Abstract*—Cyclic-coupled ring oscillators (CCRO), which consist of M ring oscillators each with N inverting stages, can be used in time-domain data converters to achieve sub-gate-delay resolution and improved phase noise performance compared to a single ring oscillator (RO). However, CCROs can oscillate in several different oscillation modes, where some modes contain overlapping phases. Such in-phase oscillations severely degrade the performance of a time-domain data converter by undermining the sub-gate-delay of the CCRO. This paper presents a design method to avoid the undesired in-phase oscillation modes, and thus achieve guaranteed maximal phase resolution regardless of the oscillation mode, by properly selecting the CCRO dimensions N and M. We show, both theoretically and with transistor-level simulations, that mode-agnostic maximum phase resolution can be ensured by selecting a prime M together with an N which is co-prime with M.**

***Index Terms*—cyclic-coupled ring oscillator, CCRO, phase resolution, prime, coprime, time-to-digital converter, TDC**

I. Introduction

The high data throughput requirements of the next generation wireless receiver systems demand wideband and high resolution analog-to-digital converters (ADC). Additionally, the deep scaling of modern semiconductor processes simultaneously hinders the performance of analog circuitry and enhances the properties of digital solutions. Digital-intensive ADCs can be realized by mapping the analog information to time-domain using voltage-to-time converters (VTC) or voltage-controlled oscillators (VCO). The analog time-domain information is then quantized by a time-to-digital converter (TDC). The resolution and bandwidth of a typical time-domain data converter are dependent on the size of the quantization step t_q of the TDC, which is limited by the minimum gate delay of the semiconductor process. To overcome this limitation, various methods have been proposed for reaching sub-gate-delay resolution, such as delay interpolation [1], pulse-shrinking [2] and Vernier measurement [3]. Additionally, sub-gate-delay can be achieved in oscillator-based converters with multipath ring oscillators [4], where each inverter stage is driven with different phase-taps of the ring oscillator (RO). A similar effect can be achieved by coupling multiple ROs in a cyclic manner, forming a cyclic-coupled ring oscillator (CCRO) [5], [6].

An issue with employing CCROs as time-domain quantizers is that they can assume various modes of oscillation. The oscillation mode is determined during the time before steady oscillation is achieved, and it defines the temporal order of transitions seen in the phase taps of the CCRO. Additionally, in certain oscillation modes, several phase-taps can oscillate in-phase, which results in significant loss of time resolution and diminished conversion resolution. An incorrect CCRO configuration makes in-phase oscillations likely, and thus they should be prevented by design in order to ensure high conversion resolution.

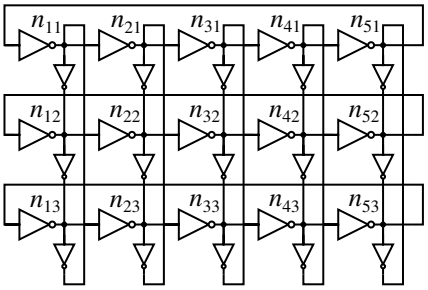

Fig. 1. A cyclic-coupled ring oscillator with $N = 5$ and $M = 3$.

This paper proposes a design method for avoiding oscillation modes with in-phase transitions to ensure maximal phase resolution in a CCRO. The proposed method enables reliable use of CCROs as time-domain quantizers in wideband high-resolution TDCs to fully benefit from the improved delay resolution of the CCRO.

The rest of the paper is structured as follows. Section II introduces the basic properties and operation of a CCRO. In Section III, we describe the conditions in which in-phase oscillations occur and present a design method for preventing such modes. The simulation results in Section IV illustrate the effectiveness of the method. Finally, Section V concludes the work.

II. Cyclic-Coupled Ring Oscillator

Fig. 1 presents the structure of a cyclic-coupled ring oscillator, consisting of $M = 3$ horizontal ring oscillators each with $N = 5$ inverting stages. The horizontal ROs are coupled using nearest-neighbor coupling via weaker coupling inverters, which results in a two-dimensional grid.

Each node in the CCRO receives two input currents: the strong main current I_m and a weak out-of-phase injection current I_c driven by the respective inverters as shown in Fig. 2. The currents interact positively when the input voltages V_m and

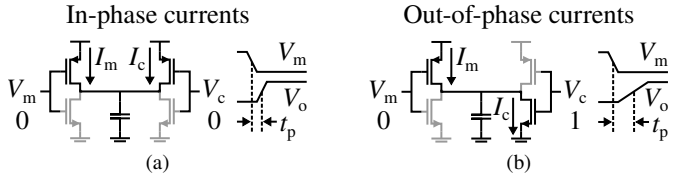

Fig. 2. Node currents for a CCRO node for (a) in-phase and (b) out-of-phase input voltage signals, respectively. The propagation delay from the main input V_m to the output V_o is modulated based on the input phase difference.

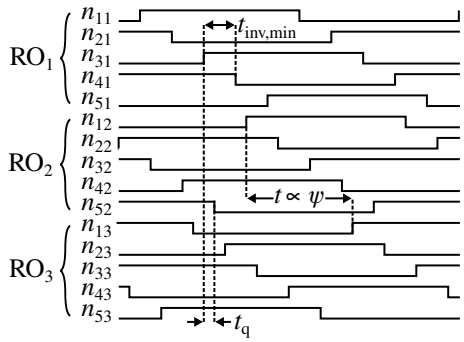

Fig. 3. Time-domain illustration of the $N = 5$, $M = 3$ CCRO waveforms with the inverter delay $t_{\text{inv,min}}$, CCRO time step t_q, and mode-dependent phase offset ψ.

V_c are in the same state, resulting in shorter propagation delay as illustrated in Fig. 2(a). On the other hand, out-of-phase inputs induce opposing currents, which results in increased propagation delay as shown in Fig. 2(b). The current injection acts as a frequency and phase locking mechanism between the horizontal rings, locking each parallel RO to a common frequency. The multi-phase injection locking implements strong coupling between the oscillators, which distributes the transitions at the phase-taps of the CCRO evenly over the full oscillation period, resulting in a reduced time-step between temporally adjacent switching nodes [5].

The time-domain waveforms of the example CCRO (Fig. 1) are illustrated in Fig. 3. The three horizontal ROs are denoted with RO_{1-3}, and the individual nodes are named according to the schematic in Fig. 1. For each horizontal RO, the time step between transitions of physically adjacent nodes, i.e. n_{31} and n_{41}, is determined by the inverter delay of the process $t_{\text{inv,min}}$. However, due to the phase offsets ψ between neighboring ROs, the subsequent transition occurs in RO_2 in node n_{52}. As a result, the minimum CCRO time step t_q is no longer limited by the semiconductor process.

A. Oscillation Modes

The phase offset between consecutive inverters in a RO can be expressed as

$$\phi = \pi + \frac{\pi}{N}, \tag{1}$$

where N is the number of stages in the RO. Assuming $I_m \gg I_c$, the phase offset ϕ follows the behavior of a single RO, where the phase offset over the full cycle of $2N$ stages is 2π radians [6].

From the perspective of the coupling inverters, the injected current is larger than the intrinsic current. Consequently, phase offsets larger than $\pi/2$ are possible. The total phase shift over the vertical loop needs to fulfill a boundary condition, where the phase is a multiple of 2π. The resulting phase offset is

$$\psi_i = \frac{2\pi}{M} \cdot i, \quad 0 < i < M, \tag{2}$$

where i is the oscillation mode of the CCRO. In the cases where i is either 0 or M, all horizontal oscillators are in-phase, making $M-1$ ring oscillators redundant (functionality same as single ring oscillator). Hence, these values are excluded from the range of i. From (2) it can be seen that a CCRO with M coupled oscillators can oscillate in $M-1$ unique modes.

B. CCRO as a Quantizer in Data Converters

The existing methods for achieving sub-gate-delay resolution in TDCs often rely on either stringent tuning and calibration or extended conversion time, both of which have limitations. For example, in Vernier-type converters, the conversion continues after the arrival of the stop signal, which extends the conversion time. On the other hand, CCROs can provide sub-gate-delay resolution and improved phase noise to data converters without extending the conversion time [7], [8]. However, in order to reliably use a CCRO as a quantizer, the order and distribution of all phase-taps has to be known. The mode can be initialized using additional circuitry, which increases the loading and lowers the CCRO performance, or the mode can be detected from the sampled CCRO states. In either case, the stable mode should be one with no in-phase oscillations in order to provide sub-gate-delay resolution. The method proposed in this paper focuses on restricting the set of possible modes to ones with maximal phase resolution, which allows the CCRO to function as a high-performance quantizer irrespective of the startup conditions. Ensuring maximal phase resolution is critical, since in-phase oscillations result in up to $\log_2(M)$-bit loss of converter resolution.

III. Maximal Phase Resolution

The phase resolution of the CCRO is maximized when no in-phase oscillations occur in the system, which results in NM unique phases. Additionally, 180° out-of-phase oscillations are sub-optimal in data converters, since they prevent the encoding of the falling edges in the CCRO. However, in some applications, such as clock generation, the complementary waveforms can be useful. When all phases are unique, and no 180° phase offsets are present, the number of available quantization steps is $2NM$. This situation is referred to as maximal phase resolution in this paper. Maximizing the phase resolution of the CCRO is critical in data converter applications, since it determines the code range and time resolution of the quantizer. This section describes the conditions for maximising phase resolution for all theoretically possible oscillation modes.

A. Selection of M

Correctly selecting M is the initial step in ensuring maximal phase resolution in the CCRO. Three cases of M selections are presented in this section.

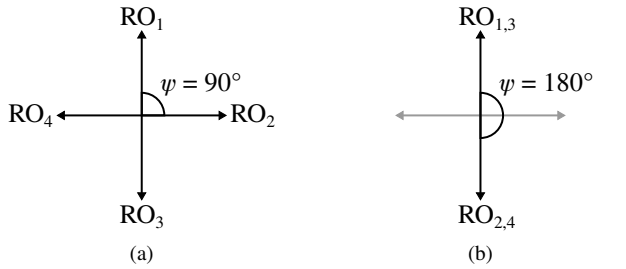

Fig. 4. The phase offsets between horizontal ring oscillators for $M = 4$ in modes (a) $\psi_1 = 90°$ and (b) $\psi_2 = 180°$.

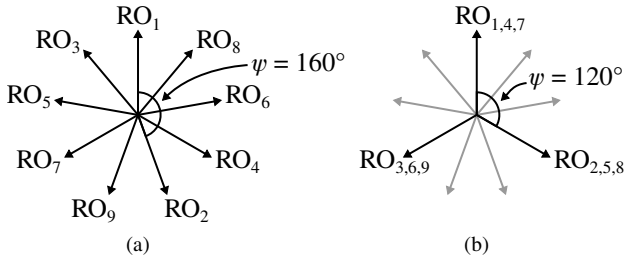

Fig. 5. The phase offsets between horizontal ring oscillators for $M = 9$ in modes (a) $\psi_4 = 160°$ and (b) $\psi_3 = 120°$.

1) Even M: Figs. 4(a) and 4(b) present the phase offsets between horizontal ROs for a CCRO with $M = 4$ in modes $\psi_1 = 90°$ and $\psi_2 = 180°$, respectively. In the first case, all ROs oscillate with unique phases, which allows for maximal phase resolution. However, the phase offset between every other ring oscillator, i.e. RO_1 and RO_3, is $180°$, making the mode sub-optimal in data converters due to overlapping rising and falling edges. In the second case, only half of the phases are unique due to overlapping ψ values.

2) Odd M: Odd values of M prevent all $180°$ phase shifts from occurring. Fig. 5 shows the phase offsets between horizontal ROs for a CCRO with $M = 9$ in two modes. In Fig. 5(a), all nine ROs are out-of-phase, which enables maximum phase resolution. However, in-phase oscillations can still appear in modes where ψ_i is an integer fraction of a full cycle, as illustrated in Fig. 5(b), where the nine ROs appear as three due to overlapping phases.

3) Prime M: To avoid all integer ratios between the mode offset ψ_i and the full cycle, M should be restricted to prime numbers. This is the first step in ensuring maximal CCRO phase resolution for quantization purposes.

B. Selection of N

In addition to selecting a prime M, the selection of N needs to be considered as well. For single-ended ROs, an even N results in a stable state with no oscillation, and thus an odd N has to be chosen. However, when N and M have common factors, in-phase oscillations may arise, as can be seen in

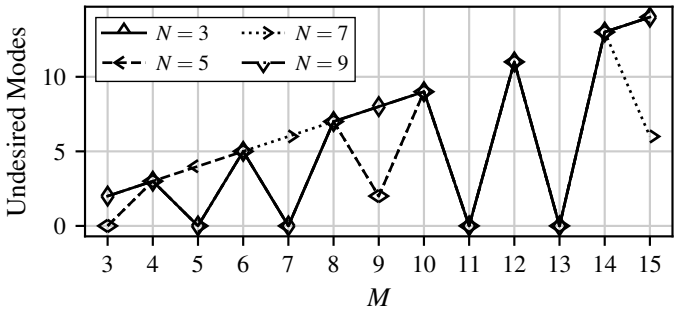

Fig. 6. Calculated total number of undesired modes (with in-phase or $180°$ offset phases) for various configurations of N and M.

$$\mathbf{\Psi}_{N5,M5,i1} = \begin{bmatrix} 0° & 216° & 72° & 288° & 144° \\ 72° & 288° & 144° & 0° & 216° \\ 144° & 0° & 216° & 72° & 288° \\ 216° & 72° & 288° & 144° & 0° \\ 288° & 144° & 0° & 216° & 72° \end{bmatrix}, \quad (3)$$

where the global phases of a $N = M = 5$ CCRO in mode $i = 1$ are shown. For any CCRO with $N = M$, all modes contain in-phase oscillations due to the symmetry.

Therefore, in order to prevent any in-phase or $180°$ shifted phases, N and M must be coprime. Fig. 6 shows calculated curves illustrating the assertion. The number of undesired modes is plotted for several values of N over a range of M. For every even M, all modes contain $180°$ phase-offset nodes, making them non-viable. In cases where M is odd but non-prime, some of the modes contain in-phase oscillations (as in Fig. 5(b)). Maximum phase resolution for all possible modes is achieved in configurations with a prime M, and N coprime with M.

IV. Simulation Results

The effectiveness of the proposed design method is confirmed with transient simulations in a 28 nm CMOS process. Table I shows the simulation results, where five CCRO configurations are simulated in all oscillation modes that sustain stable oscillation. For each mode i, the switching order of the phase-taps, the number of unique phases and the nominal CCRO time step t_q are extracted from the transient simulation. The CCRO modes are set using initial node voltages corresponding to the known mode-dependent phase offsets. The observed mode is extracted by tracking the phase offset between adjacent ROs, and the number of unique phases is calculated based on the time-domain distribution of the transitions. All simulated CCRO configurations have the same inverter sizes with the main inverter sized 6 times larger than the coupling inverter.

The first configuration has $N = 5$ and $M = 5$ corresponding to (3), where the requirement of coprime N and M is violated. Thus, in all modes, a factor of M reduction in phase resolution is observed, and no sub-gate-delay is achieved, resulting in $t_q \approx 10$ ps, which matches the nominal inverter

TABLE I
SIMULATED OSCILLATION MODES FOR SEVERAL CCRO CONFIGURATIONS

	$N=5$, $M=5$			$N=5$, $M=6$			$N=5$, $M=7$			$N=5$, $M=9$			$N=5$, $M=11$		
Mode i	Phases (#/50)	t_q (ps)	Power (mW)	Phases (#/60)	t_q (ps)	Power (mW)	Phases (#/70)	t_q (ps)	Power (mW)	Phases (#/90)	t_q (ps)	Power (mW)	Phases (#/110)	t_q (ps)	Power (mW)
1	10	10.9	5.26	-[a]	-	-	-	-	-	-	-	-	-	-	-
2	10	10.7	3.98	30	3.67	5.53	-	-	-	-	-	-	-	-	-
3	10	8.52	4.01	10	9.63	4.48	**70**[b]	**1.49**	**5.40**	30	3.67	8.30	-	-	-
4	10	7.62	5.09	30	2.67	5.17	**70**	**1.26**	**5.45**	**90**	**1.14**	**6.84**	**110**	**0.99**	**9.17**
5				-	-	-	**70**	**1.11**	**6.39**	**90**	**1.00**	**6.91**	**110**	**0.92**	**8.30**
6							-	-	-	30	2.67	7.76	**110**	**0.82**	**8.37**
7										**90**	**0.85**	**8.92**	**110**	**0.75**	**9.17**
8										-	-	-	**110**	**0.70**	**10.2**
9													-	-	-
10													-	-	-

[a] Cells denoted with a dash refer to unstable oscillation mode, and the corresponding t_q and power numbers are not applicable.
[b] Cases with maximal phase resolution are highlighted with bold font

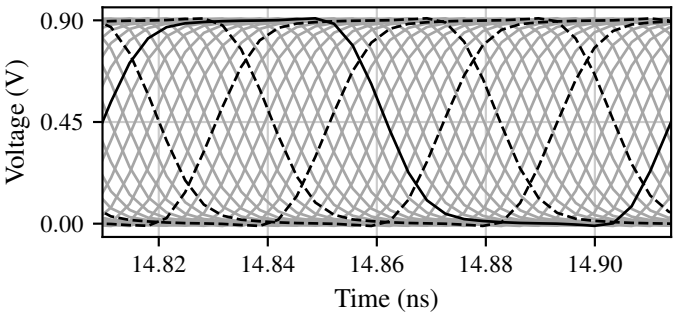

Fig. 7. Simulated time-domain node voltages of the CCRO with $N = 5$ and $M = 7$. The solid line and the dashed lines indicate the nodes of a single horizontal RO, and they grey lines are the remaining phases in the CCRO.

delay. The CCRO consumes at most 5.26 mW from a 0.9 V supply.

The second configuration has an even M. As discussed in Section III-A1, even M allows 180° phase-offset and in-phase oscillations, which result in NM and $2N$ unique phases, respectively. The maximum simulated power consumption is 5.53 mW.

The third CCRO configuration is designed according to the proposed method with $N = 5$ and $M = 7$, resulting in maximal number of unique phases and sub-gate-delay below 1.5 ps in all stable modes with 6.39 mW maximum power consumption. Fig. 7 plots the time-domain node voltages of this configuration in mode $i = 4$, where all 70 threshold crossings are uniformly distributed within the oscillation cycle.

The fourth CCRO with $N = 5$ and $M = 9$ violates the condition of a prime M. Corresponding to Fig. 5, modes $i = 3$ and $i = 6$ contain in-phase oscillations, resulting in only one third of the maximum phase resolution. The maximum simulated power is 8.92 mW.

In the final configuration, the proposed design method is followed again. Similar to the third configuration, all stable modes exhibit maximal phase resolution and sub-gate-delay resolution. The maximum power consumption is 10.2 mW.

The simulation results for cases adhering to the proposed method demonstrate a reliable factor-of-M sub-gate-delay in all modes, with time resolution as low as 1.11 ps and 0.7 ps for $M = 7$ and $M = 11$, respectively.

V. CONCLUSION

This paper proposes a design method to maximize the phase resolution of a CCRO regardless of its oscillation mode, by preventing modes with in-phase or 180° phase-offset phase-taps. The phase resolution of the CCRO is maximized by selecting a prime M, and N coprime with M. The effectiveness of the method is confirmed with transient simulations in a 28 nm CMOS process. Utilizing the proposed design method enables reliable and effective use of CCROs for time-domain quantization, which can enable sub-gate-delay time resolution and faster conversion in time-based data converters.

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