A 6–20 GHz 400-MHz Modulation-Bandwidth CMOS Transmitter IC

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***Abstract*—This paper presents a transmitter IC with two identical signal paths, including base-band amplifier, up-converting mixer, and power amplifier (PA) stages. The design is focused on wide modulation bandwidth, and the use of a resonatorless small die-area class-D power amplifier at cm-wave frequencies. This work also incorporates a local oscillator (LO) signal distribution network with phase tuning elements. The circuit is implemented in a 22-nm CMOS process, and the active die area is 0.8 mm^2. Operation over the 6–20 GHz range of carrier frequencies through the transmission of both continuous wave (CW) and wideband quadrature phase shift keying (QPSK) modulated signals were verified with measurements. Results with 20/40/100, and 400 MHz modulation bandwidths are presented, and for instance for a 20-MHz QPSK modulated input signal the measured adjacent channel leakage ratio (ACLR) of the transmitter is 28 dBc and error vector magnitude (EVM) is 5%.**

***Index Terms*—CMOS, transmitter, 5G, QPSK, wideband modulation, beamforming, power amplifier, class-D.**

I. Introduction

Future 5G and 6G mobile communication will offer a wide variety of applications such as high data-rate communication, sensing and security, industrial 5G/6G, health and medical, and transceivers requiring ultra-low latency and high reliability. Among the techniques to enable all this, operation above classic RF frequencies is widely considered. Within 3GPP standardization of 5G, the frequency range 24.2–52.6 GHz has been defined as the New Radio FR2 band [1], and in Europe also the frequency range 6–24 GHz is under considerations [2]. These frequency ranges pose significant challenges to the design of radio transmitters due to wider signal bandwidths and higher carrier frequencies compared to the prior generations.

Several previously reported transmitters and power amplifiers at RF frequencies [3] and millimeter frequencies [4] have achieved bandwidths up to 40 MHz. The trend towards wider modulation bandwidths up to hundreds of MHz is prominent and calls for active research and consequently new hardware techniques. One solution to extend the bandwidth of the power amplifier stage is to use a differential structure. Driving two devices with opposite-polarity signals forms a series connection between device capacitances, which results in an approximate doubling of the transit frequency (f_T). Secondly, differential design will effectively suppress even-order harmonics at the output spectrum. This results in relaxed requirements for bandwidth limiting linearization networks at the output of the power amplifier.

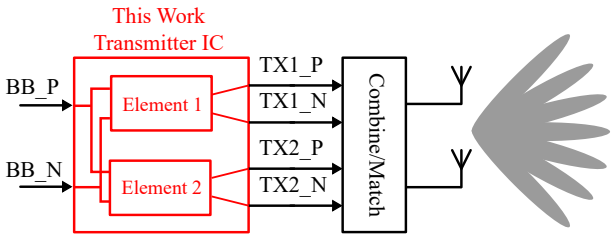

Fig. 1: System-level description of the proposed transmitter.

In this work, we have utilized the above mentioned broadband techniques and we have implemented an integrated transmitter with a switch-mode class-D power amplifier. The output stage is designed in a way that it can directly drive a 50 Ohm load over a wide band without any specific matching network. The transmitter performs the required frequency conversion over a wide range of carrier frequencies (6-20 GHz) through the transmission of a quadrature phase shift keying (QPSK) bandwidths up to 400 MHz. The system-level description of this transmitter is shown in Fig. 1. We have designed a proof-of-concept IC that is fabricated on a 22-nm CMOS process. In Chapter II we describe the transmitter architecture in detail. Chapter III covers the measurements results, and finally, Chapter IV concludes the paper.

II. Transmitter Architecture

Fig. 1 shows the structure of the proposed transmitter IC for tuning an antenna array. It consists of two identical direct conversion TX slices as well as two LO phase tuning blocks corresponding to a two-port antenna. In this paper, we focus on the design and characteristics of one slice.

A. TX slice

The building blocks of each TX slice are depicted in Fig. 2. Each TX slice employs a differential resistive feedback amplifier to take in the baseband input signal and amplify it to a 0.9-V tone signal. The amplified baseband signal is then up-converted to the desired transmission frequency by using a double-balanced passive mixer structure. This topology offers an efficient rejection of amplitude noise in the LO waveform as well as good port-to-port isolation while achieving an

acceptable amount of conversion loss. The last and most important stage of the TX slice is the power amplifier stage which is based on the class-D operation. In a typical class-D, depicted in Fig. 3, NMOS and PMOS transistors are used as switching devices, where the transistors operate in the triode region during the ON state. The power amplifier output is toggled between VDD and 0 controlled by the input square wave signal. Conventionally, the input switching frequency of a class-D PA is equal to the carrier frequency. If the loaded quality factor is sufficiently high, then the voltage across RL will be the fundamental frequency of the input waveform, which surrounds the transmitter carrier frequency. In this case, the output voltage and output power can be calculated as:

$$V_{out} = \frac{2}{\pi} VDD \quad \text{and} \quad P_{out} = \frac{2}{\pi^2} \frac{VDD^2}{RL} \tag{1}$$

which indicates the output power is the same as the power dissipated by the power amplifier, yielding a power efficiency of $\eta = 100\%$ in an ideal case. In practical cases, however, various power loss mechanisms associated with the switch-mode operation will lower the efficiency from the ideal value.

The power dissipation mechanisms of the class-D power amplifiers are mainly due to 1) parasitic capacitances, 2) short-circuit currents during the transitions, and 3) finite on-resistance of switch devices [5]. Considering these losses, it is difficult to simultaneously achieve high gain, wide bandwidth, and large output power with a single-stage amplifier. In order to address these trade-offs, a commonly adopted strategy is to cascade two or more stages, choosing different configurations, transistor sizes, bias and matching conditions for each of them. In this work, we have implemented a 6-stage class-D power amplifier as the output stage of the transmitter. In addition, the proposed multistage power amplifier has been used in a differential configuration to extend the bandwidth of the operation by roughly doubling the f_T. The frequency at which the small signal short circuit current gain of an intrinsic MOS transistor drops to unity is defined as the transit frequency (f_T). The current gain for the single MOS device shown in the Fig. 4 can be calculated as:

$$\left|\frac{I_{out}(\omega)}{I_{in}(\omega)}\right| = \left|\frac{(g_m - j\omega C_{gd})}{j\omega(C_{gs} + C_{gd})}\right| = \frac{\sqrt{g_m^2 + \omega^2 C_{gd}^2}}{\omega(C_{gs} + C_{gd})} \tag{2}$$

By considering unity current gain at the transit frequency, f_T can be calculated as:

$$\omega_{T,single} = 2\pi f_{T,single} = \frac{g_m}{(C_{gs} + C_{gd})} \tag{3}$$

The differential signaling effectively combines the device capacitances in series, thereby roughly doubled f_T compared to the single ended structures can be achieved:

$$\omega_{T,diff} = 2\pi f_{T,diff} = \frac{g_m}{0.5(C_{gs} + C_{gd})} = 2\omega_{T,single} \tag{4}$$

Furthermore, the differential design enables suppression of even-order harmonics. This serves for achieving a certain level of linearity in this design and enables us to employ a broadband structure at the output without using any bandwidth limiting waveform linearization filters. Further linearization can be achieved by adding a dedicated circuitry and/or antenna. In this implementation, the output stage is also designed in a way that it can directly drive a 50 Ohm load over a wide band without any specific matching network. We have utilized the above mentioned broadband techniques to enable an ultra-wideband operation up to 400 MHz.

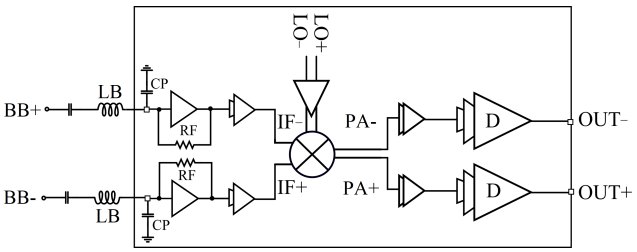

Fig. 2: Top-level demonstration of one TX slice.

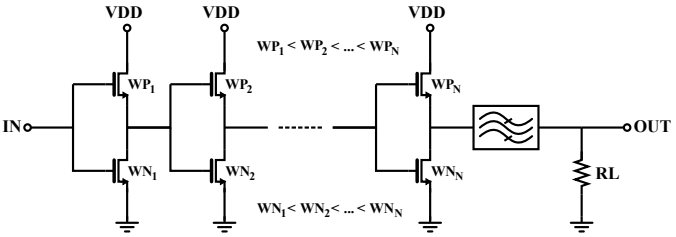

Fig. 3: N-stage class-D power amplifier.

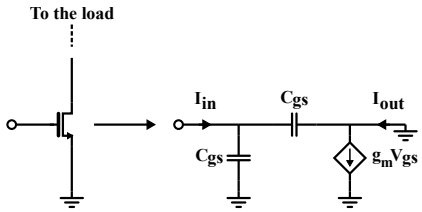

Fig. 4: N-stage class-D power amplifier.

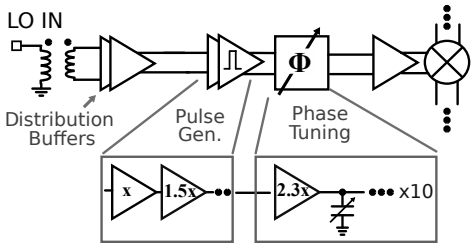

Fig. 5: LO signal chain featuring pulse generation and phase-tuning blocks.

B. LO Chain

Fig. 5 illustrates the block diagram for the LO signal chain. It was designed by applying mixed-signal techniques, so that it can serve us as a step to analyze the feasibility of digital circuits operating above 10 GHz. The LO chain

targets to provide rail-to-rail signals for hard switching of mixers operating between 6–20 GHz LO frequency. It also incorporates varactor-based phase tuning to calibrate phase mismatches and study the possibility of LO phase-tuning for phased arrays. The reference LO signal is fed in through a single-to-differential transformer and distributed across the chip with buffers. Pulse generation consists of a chain of inverters, each inverter drives a load 1.5 times its size. The inverter load has been limited to allow amplification of the LO signal to create pulse-like waveforms. The pulse generator is followed by a phase-tuning element, which is composed of a series of 10 inverter-varactor pairs. The varactors are driven by 2.3 times the minimum-sized inverter to maintain signal integrity at the highest frequency of the range, as well as drive the mixers. Digital controls (0,1) enable 1-bit of tuning control in each pair. The varactor-tuning block can calibrate phase mismatches between LO_P and LO_N signals or it can serve as a phase-tuning method for beamforming applications.

III. Measurements Results

Fig. 6 presents the microphotograph of the chip fabricated on a 22-nm CMOS process. Baseband amplifier, mixer, and power amplifier stages as well as LO related blocks are the main elements of the transmit path and are specified using red colored rectangles in the die microphotograph. The LO input and TX outputs are connected using ground-signal-ground (GSG) probes through the custom designed low parasitic pads. The EM-simulated parasitic capacitance of these mmw pads is only 20 fF. The TX BB inputs, on the other hand, are wire-bonded to the PCB and a micro-strip transmission line pair is employed to route them to the edge SMA connectors. Other lower frequency signals, including DC power supplies and SPIs are also provided through the PCB traces.

The functionality of the implemented transmitter is investigated through the various measurements both for CW input signal and modulated input signal. Fig. 7 shows the measured output power versus LO frequency range with a sinusoidal input signal at 100 MHz. The implemented transmitter can provide an output power of roughly more than 0 dBm for a wide range of carrier frequencies (6-20 GHz). The overall power consumption, including the LO chain, is 100 mW from a 0.9 V supply voltage. The functionality of the implemented transmitter is also studied by applying a wideband QPSK modulated input signal up to 400 MHz bandwidth. Since the common industrial vector signal generators usually can provide only a narrow-bandwidth modulated signal, we have developed our own signal generator for a wideband operation. This QPSK signal generator is realized on a hardware platform based on Zynq-7000 ZC706 FPGA and AD9172 DAC.

The measured output spectrum of the transmitter as well as constellation plots by applying 20/40/100 MHz single carrier QPSK signal at a carrier frequency of 16 GHz are depicted in Fig. 8. As can be seen, the proposed transmitter is able to efficiently pass wideband modulated signals. We have also measured the output spectrum of the proposed transmitter with higher modulation bandwidths up to 400 MHz as shown in

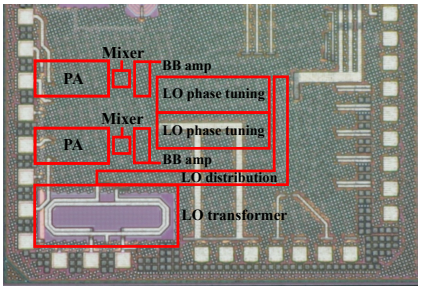

Fig. 6: Microphotograph of the implemented transmitter IC

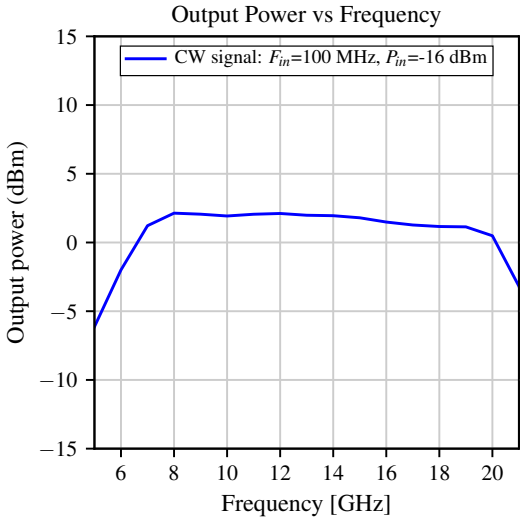

Fig. 7: Measured output power of the proposed transmitter versus frequency range.

Fig. 9. The measurement setup limits us to an IF frequency of 250 MHz at the transmitter input which results in the images folding into the band of interest with degrading the performance metrics in this particular case. Despite this setup related limitation, we are still able to push this ultra wideband signal through the transmitter chain. Regarding the performance metrics, for a 20 MHz QPSK input signal, the measured ACLR of the transmitter is 27.6 dBc and the measured EVM is 5.1%. At bandwidth of 40 MHz ACLR is 23.6 dBc and EVM of 6.6%, and for 100-MHz case values are 19.3 dBc and 12.4%, respectively. Altogether, by considering the 3GPP TS 38.101-1 EVM requirements for different 5G modulation schemes, the measured EVM for 20MHz, 40 MHz, and 100 MHz meet the expectations (EVM less than 17.5%).

Finally, Table I shows the performance summary of the proposed transmitter and compares it to the state of the art. As can be seen, the implemented transmitter can provide state of the art level characteristics over the operating range.

IV. Conclusion

This paper presents a transmitter IC with two identical TX slices including BB amplifier, mixer, and power amplifier stages for each slice. This work also incorporates a LO signal distribution network with phase tuning elements using

TABLE I: PERFORMANCE COMPARISON

	This work	[3] JSSC 2020	[4] JSSC 2018	[6] JSSC 2020	[7] TMTT 2022
Process	22nm FDSOI CMOS	28nm bulk CMOS	28nm bulk CMOS	45nm SOI CMOS	28nm bulk CMOS
Vdd (V)	0.9	1/1.8	0.8/1.05/1.8	1/2	1.1/2.2
Frequency (GHz)	6-20	2.535 (NR-n7)	28	39	26.5
PA structure	6-stage class-D	linear	5-stage linear	linear	2-stage linear
Modulation	QPSK	64 QAM	64 QAM	64 QAM	64 QAM
RF BW (MHz)	20 / 40 / 100	20	20	N/A	100
Out power (dBm)	3	3	3	12.2	12.3
Power (mW)	100	70.5	N/A	N/A	N/A
ACLR (dBc)	27.6 / 23.6 / 19.3	44.4	N/A	25.4	22.2
EVM%	5.09 / 6.6 / 12.32	1.9	2.23	7.16	5.43
Area (mm^2)	0.8	0.31	7.28	2.8	0.165

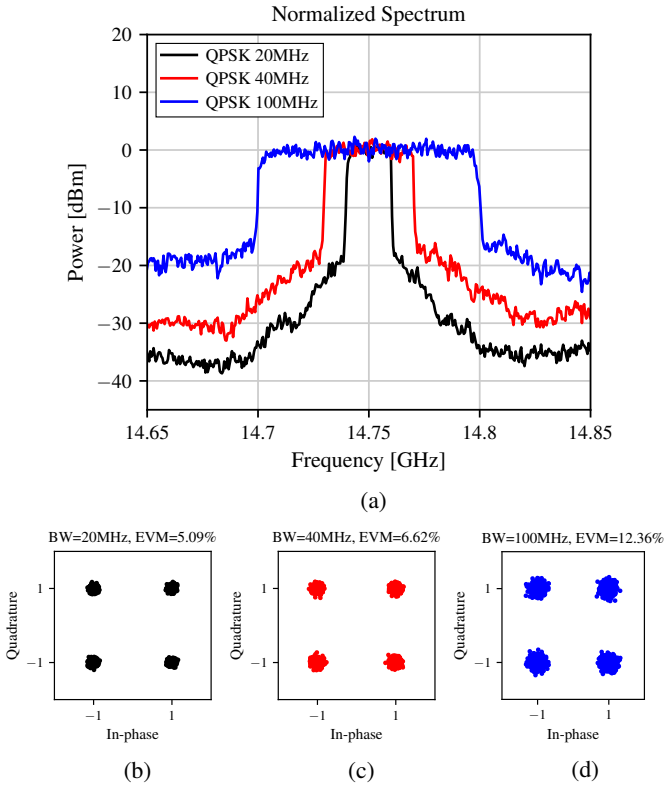

Fig. 8: TX measurements for QPSK modulated input signal (a) Measured spectrum of the proposed transmitter 20/40/100 MHz bandwidths, (b-d) Constellation plot for each bandwidth.

a mixed-signal approach in order to study the performance of the traditional inverter-based techniques in millimeter-wave frequencies. The circuit is implemented in a 22-nm CMOS process, and the active die area is 0.8 mm^2. The on-wafer measurements demonstrate that the implemented chip can efficiently perform the required frequency conversion over a carrier frequency range of 6-20 GHz through the transmission of both CW and wideband quadrature phase shift keying (QPSK) modulated signals up to 400 MHz. For a 100-MHz QPSK input signal, the measured ACLR of the transmitter is 19.3 dBc and the measured EVM is 12.4%.

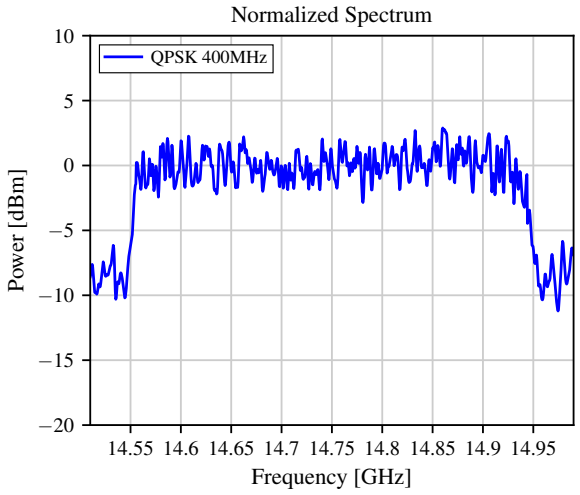

Fig. 9: TX measurements for 400-MHz QPSK modulated input signal. Poor ACLR is due to measurement setup impairment.

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