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Radiation hard 3D silicon pixel sensors for use in the ATLAS detector at the HL-LHC

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Abstract: The High Luminosity LHC (HL-LHC) upgrade requires the planned Inner Tracker (ITk) of the ATLAS detector to tolerate extremely high radiation doses. Specifically, the innermost parts of the pixel system will have to withstand radiation fluences above $1 \times 10^{16}\,\mathrm{n_{eq}cm^{-2}}$. Novel 3D silicon pixel sensors offer a superior radiation tolerance compared to conventional planar pixel sensors, and are thus excellent candidates for the innermost parts of the ITk. This paper presents studies of 3D pixel sensors with pixel size $50 \times 50\,\mu\mathrm{m}^2$ mounted on the RD53A prototype readout chip. Following a description of the design and fabrication steps, Test Beam results are presented for unirradiated as well as heavily irradiated sensors. For particles passing at perpendicular incidence, it is shown that average efficiencies above 96% are reached for sensors exposed to fluences of $1 \times 10^{16}\,\mathrm{n_{eq}cm^{-2}}$ when biased to 80 V.

Keywords: Hybrid detectors; Particle tracking detectors; Performance of High Energy Physics Detectors; Radiation-hard detectors

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Contents

1 Introduction

The current tracker system of the ATLAS detector at CERN's LHC has been performing extremely well, handling high event rates while withstanding radiation fluences up to a few 1×10^{15} $n_{eq}cm^{-2}$ [1]. It is now approaching the end of its lifetime, and a replacement is needed for operation in an environment of unprecedented event rates and background radiation expected at the High Luminosity LHC (the HL-LHC). Significant technological developments are necessary to meet the requirements of the HL-LHC, where the Inner Tracker (the ITk) is conceived to be composed of silicon microstrip and pixel sensors [2, 3]. Particularly challenging is the design of pixel sensors to be placed very close to the interaction region, where fluences in the vicinity of 1×10^{16} $n_{eq}cm^{-2}$ have to be tolerated while maintaining an efficiency of charged particle detection above 96% for particles at a normal incidence with respect to the beam axis [3].

The 3D sensor architecture proposed in 1997 [4] offers an improved radiation hardness compared to conventional planar sensor architectures. Because of the drastically different electrode design, the distance between electrodes can be reduced while still allowing sufficient drift of charge carriers for good signal formation in the active region. The reduction in electrode separation reduces the probability of charge trapping, making this sensor design more radiation tolerant.

In practice, 3D sensor production is extremely challenging, and requires significant investments and development in sensor manufacturing technology. At SINTEF MiNaLab[1] several productions of 3D test devices have taken place. Results from the first production were reported in 2009 [5]. Furthermore, sensors compatible with the ATLAS IBL [6], have been proven to perform (when read out by the FE-I4 chip [7]) with an efficiency of up to 99.9% at bias voltages between 5 V and 15 V [8]

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The purpose of this paper is to present results of efficiency studies of a batch of both unirradiated and irradiated sensor test devices from the SINTEF prototyping Run 4 tested in a pion beam at CERN (section 4.2) and in an electron beam at DESY (section 4.3). In this batch, sensors with a variety of designs were produced with two different thicknesses of the active material, 100 and 50 µm. Most sensors on each wafer were designed for flip-chip bonding to FE-I4 front-end chips and only a very small number of sensors that were adapted to the 'RD53A' chip [9] were included in the wafer design. In sections 2 and 3 the sensor design and fabrication details will be presented. Beam tests of unirradiated and irradiated sensors mounted on RD53A readout chips are presented in section 4.[2]

2 Sensor and wafer layouts

In SINTEF prototype Run 4, eleven 6-inch silicon-on-silicon (Si-Si) wafers were fully processed. The floorplan of the wafers, which includes two RD53-compatible and 20 FE-I4-compatible sensors, is shown in figure 1. This paper presents the test results obtained from tests of RD53A compatible sensors.

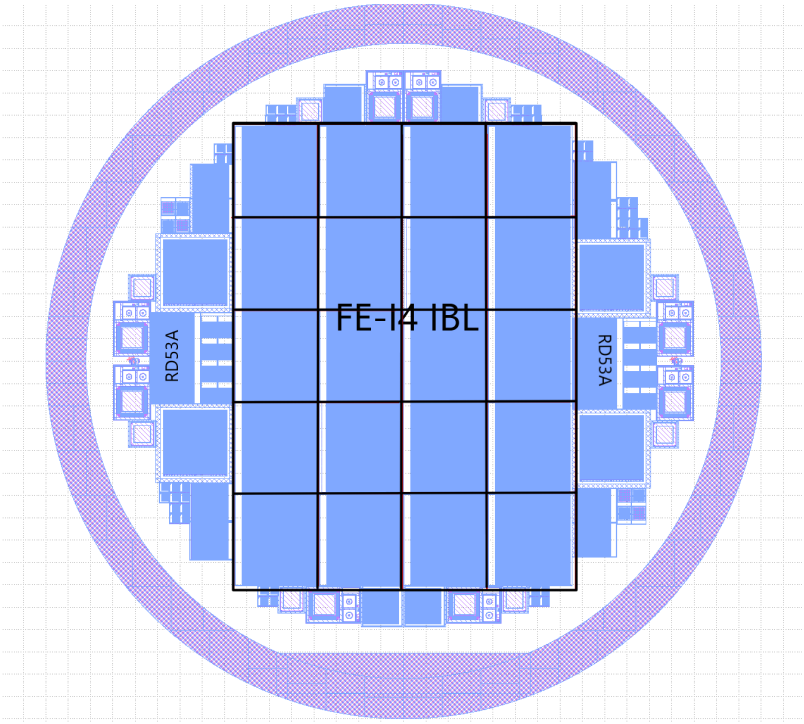

Figure 1. Floor plan of a Run 4 wafer, 20 FE-I4 outlined in black and two RD53A on the sides.

The RD53A compatible pixel sensors have a pixel size of $50 \times 50\,\mu m^2$. Each pixel consists of one n^+-electrode that serves as readout, and four p^+-electrodes for biasing, as shown in figure 2. The readout and biasing electrodes were designed with a diameter of 3 µm. Because of the Si-Si wafer type, the p^+-electrode columns can be contacted on the backside when etched all the way through the high resistivity active layer reaching the low resistivity backside of the wafer, effectively removing the need for high voltage metal on the frontside.

[2]Previous tests of sensors mounted on FE-I4 readout chips can be found in ref. [8].

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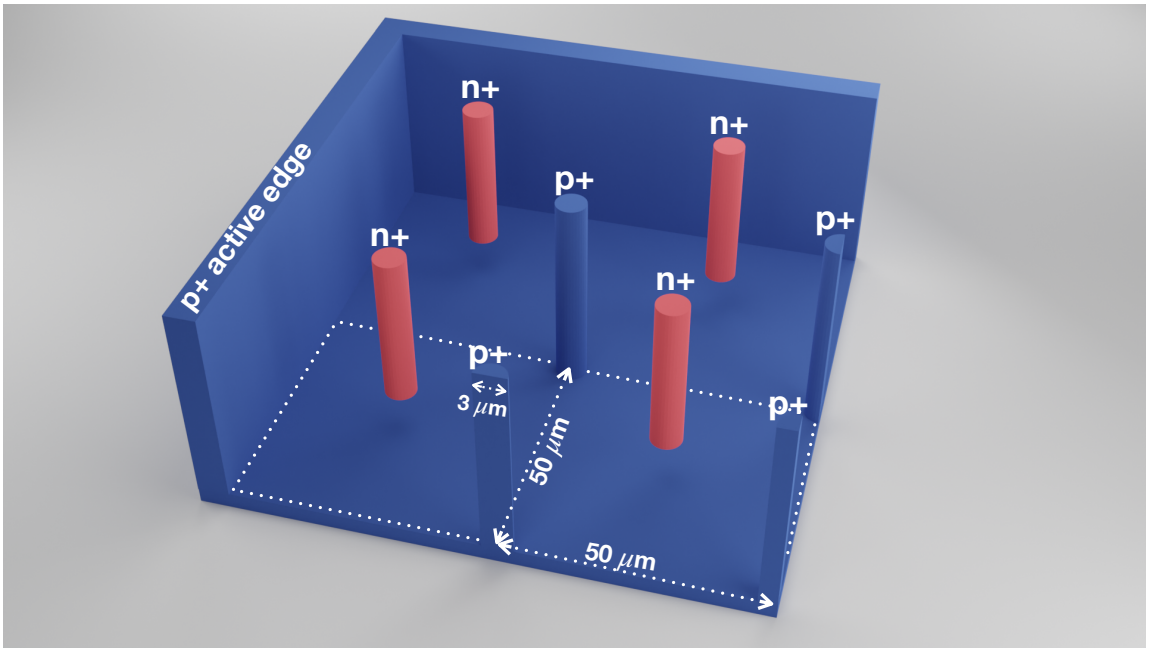

Figure 2. An illustrated 3D view of 4 pixel cells in the top left corner of the sensor. Shown are the electrode columns as well as the active edge. Note that the n^+ readout-electrodes (red) are not etched all the way through the substrate but a small gap remains between the tip of the electrode and the backside wafer. The dotted lines represents the pixel cell of size $50 \times 50\,\mu m^2$.

Also shown in figure 2 is the so-called active edge of the sensor. This is realized as a continuous electrode trench surrounding and encapsulating the active area of the sensor. This design eliminates the need for guard rings and sensor cutting can be done very close to the active edge (approximately 100 µm away from the active edge), reducing the overall sensor chip size by drastically reducing the dead area.

3 Sensor fabrication

The Run 4 fabrication was carried out on 6-inch Si-Si wafers with device layer thicknesses of 100 µm and 50 µm. The device layer is a float zone (FZ), p-type wafer with resistivity of 6000–12000 Ω-cm while the support wafer is a low resistivity p-type wafer. Si-Si wafers, which have no buried oxide between the device wafer and support wafer, offer the capability to contact the p-type electrodes from the backside without additional processing on the support wafer, as compared to Silicon-on-Insulator (SOI) wafers.

A brief summary of the fabrication process is illustrated in figure 3. The fabrication started with p-spray implantation (low dose boron implantation) to electrically isolate n-type and p-type electrodes. This was followed by some annealing, thermal growth of thick oxide, and sputtering of an aluminum layer used as a hard mask for Deep Reactive Ion Etching (DRIE) of 3D electrodes. Next, the n-type columns were made by patterning the aluminum mask using optical lithography and wet etching, followed by reactive ion etching (RIE) of the oxide and DRIE of silicon. The DRIE was stopped at a reasonably safe distance from the support wafer (35 µm) to prevent the merging of phosphorous diffused region from the n-type columns and boron diffused region from the support wafer, which would otherwise cause an early current breakdown. The aluminum mask was stripped off after the

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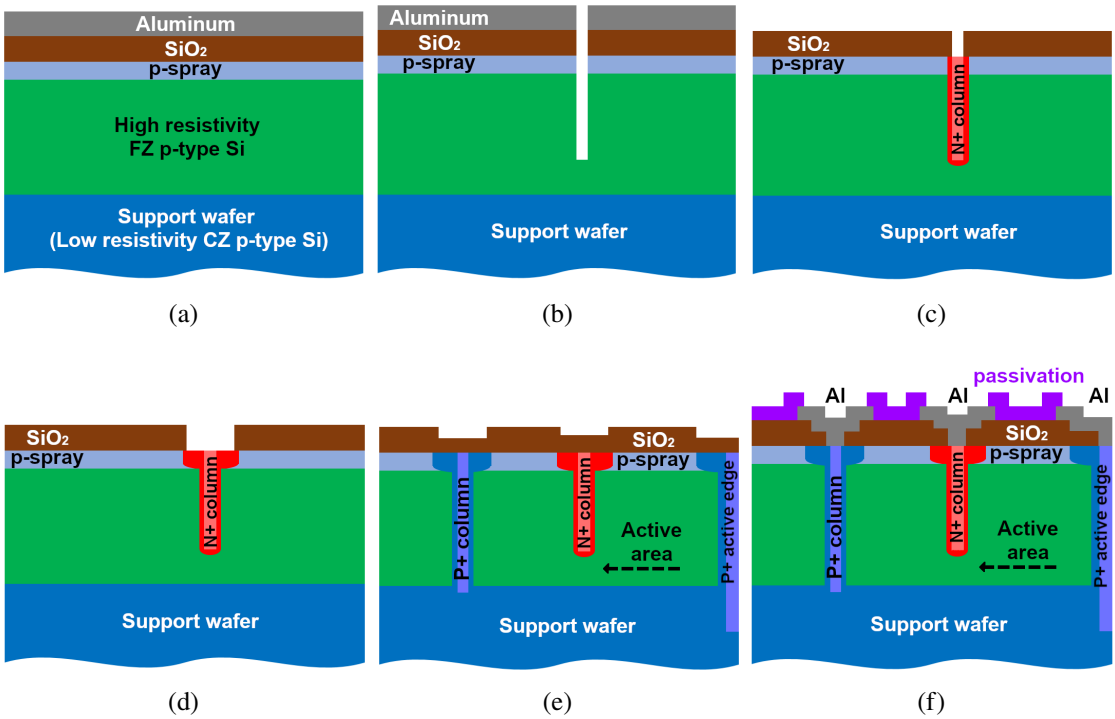

Figure 3. A brief illustration of the sensor fabrication, (a) P-spray implantation, thermal growth of a thick SiO_2 film, deposition of Al mask; (b) Patterning of Al mask (n^+ column lithography), RIE of SiO_2, DRIE of n^+ columns; (c) Doping of n^+ columns, polysilicon deposition, doping of polysilicon, etching of the polysilicon on the surface; (d) Patterning of planar n^+ regions (n^+ surface lithography), n^+ doping of the surface; (e) Similar processing steps (steps b) to (d) were carried out to fabricate p^+ columns and active edge electrodes after another oxidation to cover the n^+ regions and deposition of Al mask; (f) Standard planar processing (opening of contact holes, metallization, and passivation with PECVD SiO_2+SiN_x).

DRIE process was completed, and the columns were doped by gas phase diffusion (POCl3) and filled with phosphorous doped polysilicon to restore the planarity of the wafer so that the subsequent lithographic steps could be carried out. The excess polysilicon deposited on the surfaces of the wafer was removed by RIE. Next, the second lithography process was carried out to etch the oxide around the n-type columns on the wafer surface and dope these surface regions with phosphorous as well to ensure a good electrical contact to n-type columns. Similar processing steps were carried out to fabricate the p-type electrodes and active edge (which are etched all the way down to the support wafer and doped by gas phase boron — BBr3). The sensor fabrication was finished with standard planar processing (contact opening, metallization, and passivation). In total, six wafers with device layer thickness of 100 µm and five wafers with a device layer thickness of 50 µm were completed.

4 Test beam measurements

Sensors equipped with RD53A readout chips were mounted on single-chip cards (SCC) and tested in the H6 pion beam at CERN, as well as in a 4 GeV electron beam at DESY. Sensors with active

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thicknesses of 50 and 100 microns were tested. Devices under test (DUTs), named D59-1 and E9-1 after their wafer origin,[3] were both tested unirradiated. DUTs D61-2 and D62-1 were irradiated to fluences of $n_{eq} = 5 \times 10^{15}$ cm^{-2} and $n_{eq} = 1 \times 10^{16}$ cm^{-2}, respectively, and tested after irradiation.

The RD53A chip is a prototype of the ASIC being developed for reading out pixel sensors in the upgraded ATLAS and CMS trackers. Three regions of the chip are equipped with different preamplifiers: 'synchronous', 'linear' and 'differential'. During data-taking, the regions of the sensor equipped with linear and differential preamplifiers were operated and exposed to the beam. The results reported below are obtained from the region of the sensors that was connected to the FE chip region with the differential amplifier.

4.1 Test beam setups

At CERN and DESY, the devices under test (DUT) were placed in a setup using the EUDET pixel telescope [10]. The six sensor planes of the telescope are composed of Mimosa26 pixel sensors [11] with a pixel pitch of 18.5 µm. Each plane consists of 576 x 1152 pixels. The DUTs were placed in the middle of the telescope assembly (three pixel planes upstream and three planes downstream of the DUTs). Triggering was achieved through the use of upstream and downstream scintillators. In addition to the devices under tests, a planar pixel sensor connected to the FE-I4 readout [7] was used as reference. The schematic test beam setup is shown in figure 4.

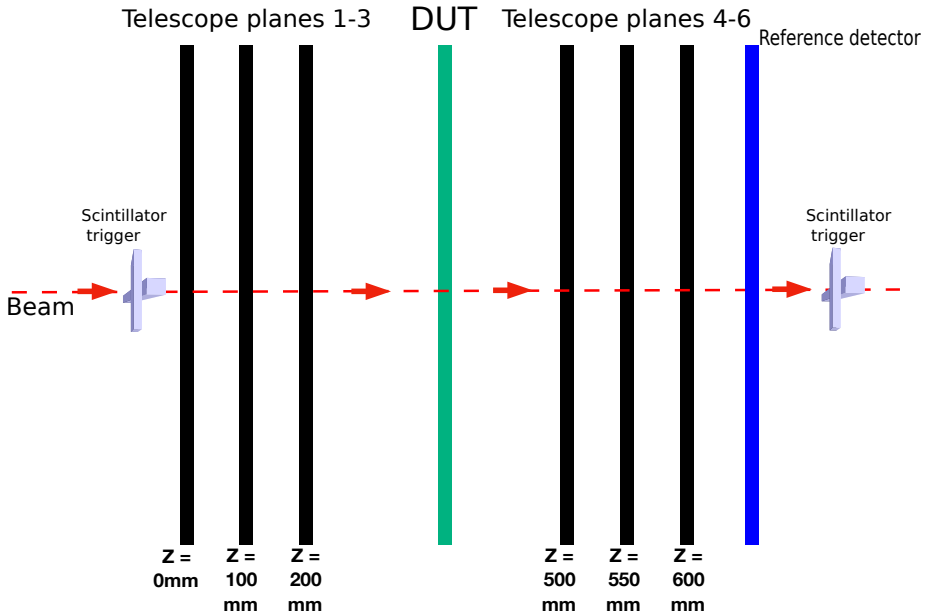

Figure 4. Schematic overview of the testbeam setup. Black lines represent the EUDET telescope planes, the green line represents the DUT, the blue plane shows the placement of the reference detector and scintillation triggers are drawn in at the front and back of the setup. The dashed red line represents the beam. Note that the lateral position of the telescope planes are approximate and only meant as a illustrative example as the separations between planes are adjustable between 10 and 150 µm upstream and downstream of the DUT.

[3]The letter and number preceding the hyphen reference the wafer from which the sensor was extracted and the subsequent number denotes which number it was given on the wafer.

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4.2 Tests in the H6 pion beam at CERN

Unirradiated samples were placed in the 180 GeV H6 pion beamline at CERN. In the following, we report on a sensor with 100 µm active thickness, biased at V_{bias} = 10 V, for triggers with a signal present in the reference sensor that could be associated to the reconstructed track. The presence of a signal in the reference sensor is particularly important in this beam, where two particles may arrive in very close succession, with the second particle causing a new trigger before all tracker data from the previous trigger are cleared. The response of the 100 µm thick sensor, named 'RD53A-D59-1', is shown in figure 5. Here, the hits from neighbouring pixels are grouped together into clusters and their time over threshold (ToT) are summed up. Most clusters consist of just one hit, but a significant fraction of the events consist of two or more hits (about 15%).

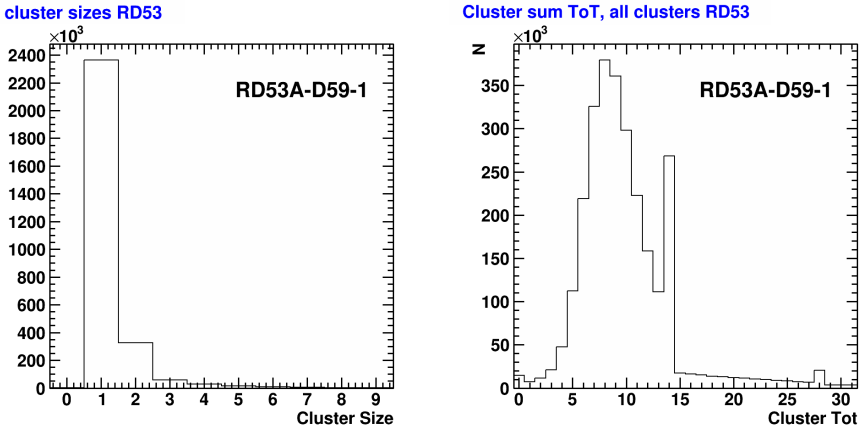

Figure 5. Cluster sizes (left) and summed time over threshold (ToT) for clusters (right) as observed in a pion testbeam, measured at a bias voltage of V_{bias} = 10 V. The rightmost peak in the cluster sum ToT plot, in bin 14, is due to saturation at the highest value for the ToT (14) in a single pixel.

The pointing resolution of particle impact points on the DUTs as reconstructed in the CERN test beam was estimated at less than 6 µm, by the use of distributions of differences between DUT coordinates and track impact predictions, as shown in figure 6. The resolution is sufficient to reveal localized efficiency losses at the locations of the p^+ electrodes, as shown in figure 7.

The n^+ readout electrode is not visible in figure 7 due to the structure of the electrode column. Since this column is not etched all the way through the silicon bulk, charges liberated between the electrode tip and the back side of the sensor are collected. Enough charge is collected that there is no evidence of efficiency loss at the location of the electrode. The average efficiency over a single pixel surface was found to be 98.58%, with a statistical uncertainty of 0.02%. Systematic uncertainties include the effects of particle scattering into and out of windows defined for association of hits to reconstructed tracks in the reference sensor as well as in the tested sensor. Also, in the masking procedures for removing unbonded (dead) and noisy pixels, systematic uncertainties may be introduced. Reasonable variations of the track acceptance-window size, and cuts associated with the definition of noisy pixels, results in total changes in the efficiency estimate well below 0.1%. Therefore, we quote an estimated efficiency of (98.6 ± 0.1)% for this study.

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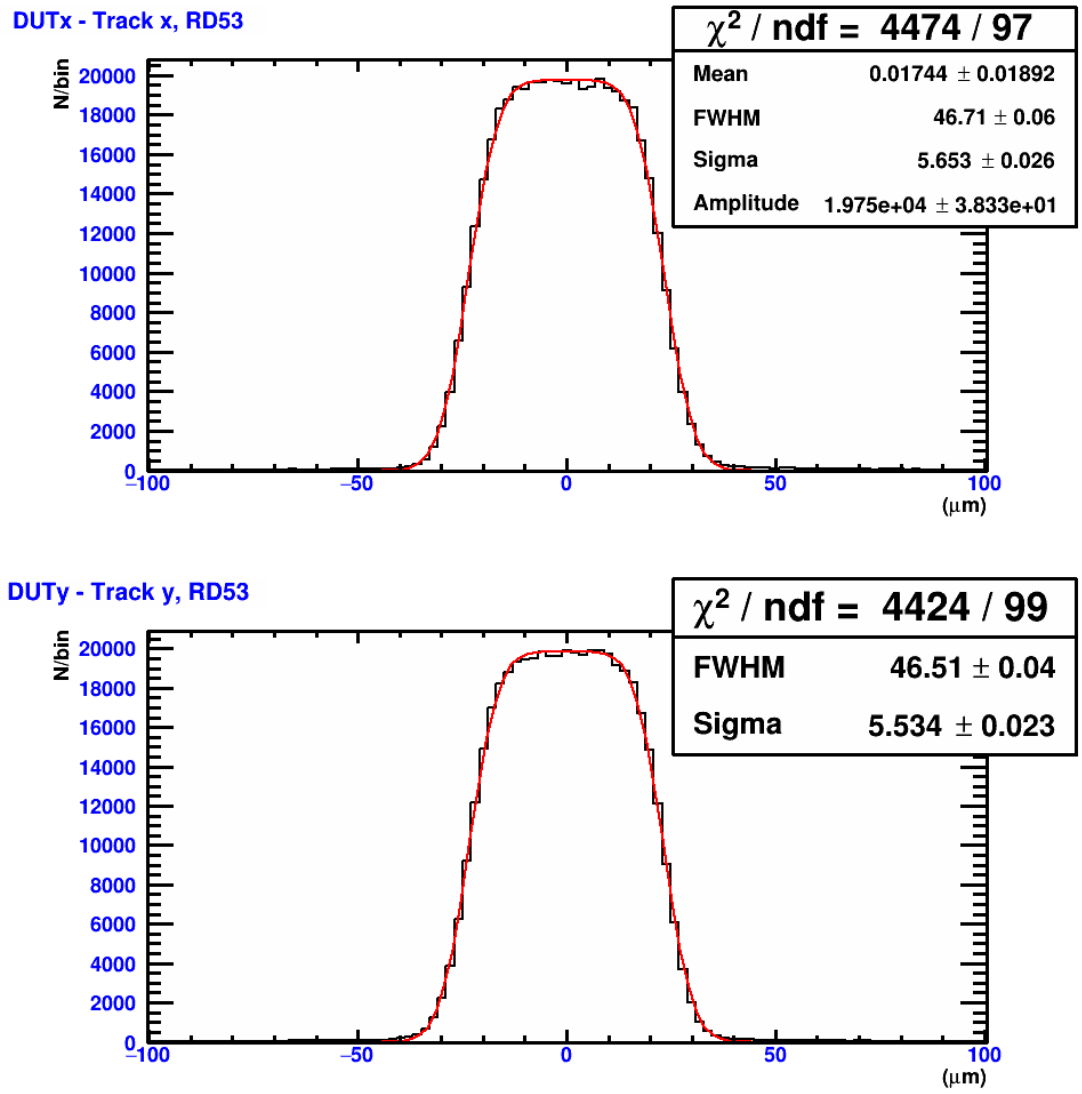

Figure 6. Residuals (difference between track impact position on sensor and the reconstructed track from the beam telescope) in x and y for a Run 4 DUT at CERNs SPS testbeam. The fit is a convolution of a box distribution and a Gaussian, resulting in an error function at both sides, where sigma yields the resolving power of the pixel edges ($< 6\,\mu$m).

4.3 Tests in an electron beam at DESY

At DESY, tests were performed in the 4 GeV electron beam using unirradiated and irradiated sensors. As the irradiated samples had to be cooled to avoid thermal runaway from heat dissipation, they were placed in a styrofoam container with dry ice. This method allows for low ambient temperature inside the container but is not stable and did vary between approximately -40°C and -20°C. The ambient temperature was monitored visually with a thermometer placed inside the container. The sensor temperature was not recorded during the data-taking, but earlier experiments with the same setup resulted in sensor temperatures between -20°C and -10°C.

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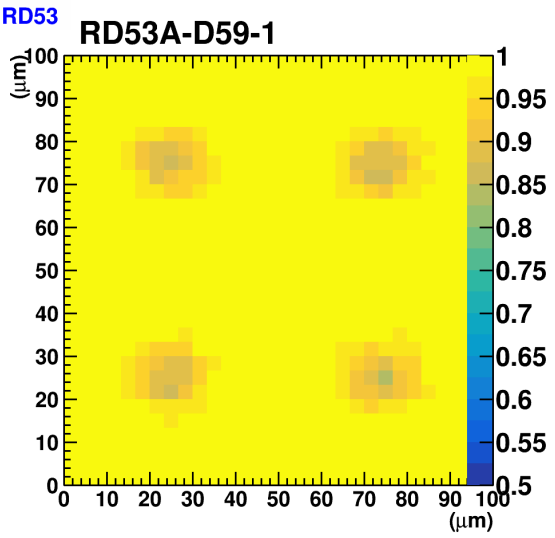

Figure 7. Efficiency map averaged over a region of $100 \times 100\,\mu m^2$, corresponding to an area covered by four pixels, as measured in the 180 GeV pion testbeam at CERN. The size of the inefficient regions due to the p^+ electrodes is consistent with the pointing resolution of the reconstructed tracks.

Care was made taken to minimize the material at the entry and exit points of the electrons passing through the box and the DUTs by cut outs in the box covered with thin tape. The pointing resolution is dominated by multiple scattering in the material placed in the beam. As the scattering effect is sufficiently high, tracks were reconstructed using the GBL (General Broken Line) algorithm available in the EUtelescope software package. This algorithm is adapted to a situation where most of the material is located in discrete positions. The impact point resolution was found to be 25 to 30 µm, depending on the configuration of sensors to be tested, and whether or not the cooling box was present. All the 3D sensors tested at DESY are listed in table 1, together with their corresponding thickness, test parameters, and average efficiencies.

Table 1. List of DUTs measured at DESY testbeam. All DUTS were tuned to a low threshold value between 400-1000 electrons during testbeam.

Overview of DUTs parameters

Name of DUT	Thickness [µm]	Threshold[e^-]	Dose [$n_{eq}cm^{-2}$]	Bias [V]	Efficiency [%]
D59-1	100	400	Unirradiated	10	99.5
E9-1	50	400	Unirradiated	10	98.9
D61-2	100	1000	5×10^{15}	40	above 97
D62-1	100	500	1×10^{16}	80	above 96

4.3.1 Studies on non-irradiated samples

Two non-irradiated sensors, 'E9-1' and 'D59-1', with active thicknesses of 50 and 100 µm were studied at different bias voltages between 2.5 V and 20 V. In order to minimize signal loss and stay above noisy low threshold regions, both sensors were tuned to a threshold value of 400 e^-. Runs

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were performed with two different tilt angles with respect to the beam, perpendicular incidence, and a 15° tilt with respect to normal incidence.

Figure 8 shows the Time-over-Threshold (ToT) for both the sensors perpendicular to the beam. Here, the −20 V bias voltage runs were used to be certain that both of the sensors were fully depleted. As seen in these plots, the ToT was not tuned properly before data-taking on the DUTs for the 400 e^- configuration. This caused the ToT distribution to have its centre above the maximum register value of the chip. Thus, hit saturation leads to an overflow in bin 14, resulting in a high, artificial peak. However, as both the DUTs ToT had not been tuned into a standard Gaussian distribution at lower ToT values, their Front End discharge current registers would be set to the default values. Hence, the energy deposition read out by the ToT values could be compared as it's not tuned to correct for the sensor thickness.

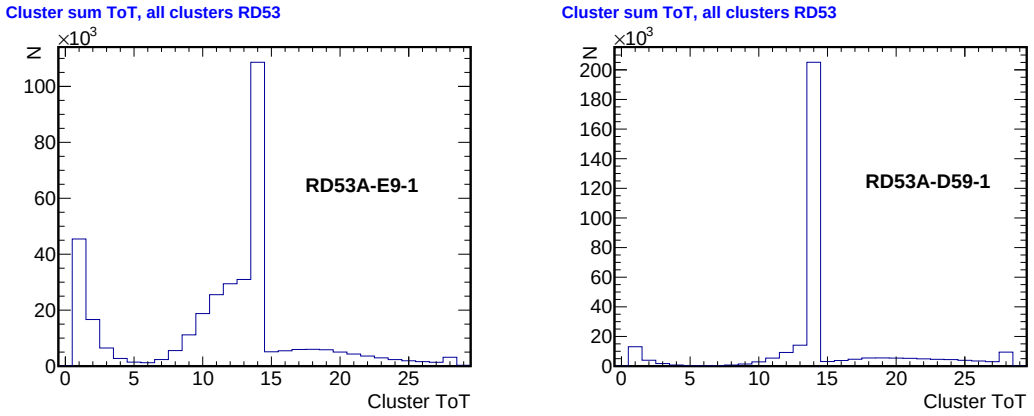

Figure 8. ToT for E9-1 (left) and D59-1 clusters (right) as observed in an electron beam at bias voltage = −20 V. The rightmost peak in the cluster sum ToT plots, in bin 14, is due to saturation at the highest value for the ToT (14) in a single pixel.

Figure 9 shows the cluster sizes for the same sensors but with a 15° tilt with respect to normal incidence. As seen from the two distributions, the thicker sensor (right plot) has a higher relative amount of bigger clusters compared to the thinner sensors (left plot).

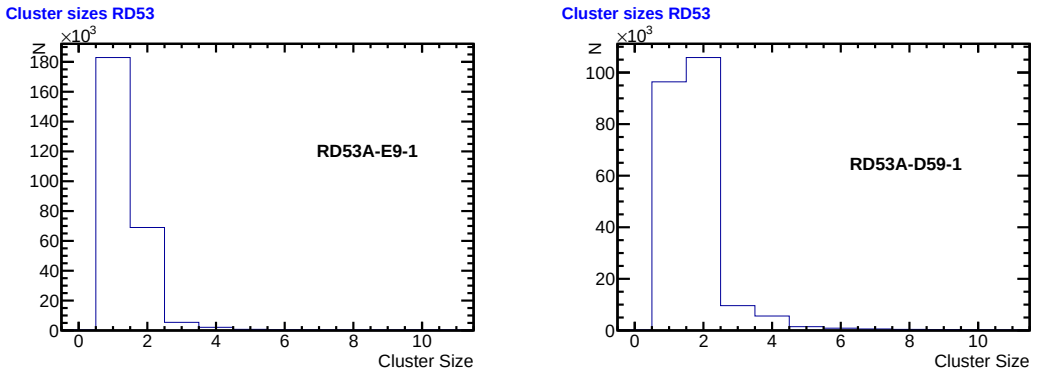

Figure 9. Cluster sizes in number of pixels for E9-1 (left) and D59-1 clusters (right) as observed in an electron testbeam when tilted at 15 degrees with bias voltage = −20 V.

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The overflow in bin 14 led to a non-representative ToT distribution and skewed the average ToT value to a lower number. The ToT of the DUTs, however, can still be compared as the effect was the same in both. Post-analysis estimation of the average ToT bin values shows that the mean bin value increased from 12.11 to 12.35 (±0.01 for both) for the thinner 50 µm 'E9-1' sensor when tilted, while an estimated increase of the mean bin value from 11.328 ± 0.003 to 15.183 ± 0.009 was observed for the 100 µm thick sensor 'D59-1'. This effect can also been seen in the relative cluster size, where the average size of the clusters increased from to 1.246 to 1.368 (±0.003 for both) in the thinner sensor, and from 1.314 ± 0.001 to 1.735 ± 0.003 in the thicker sensor with and without the tilt, respectively.

An increase in the ToT values going from a thinner to a thicker sensor as well as an increase in cluster sizes when tilting the sensors are expected. In both cases, the electrons from the beam have a long path-length in the sensitive region of the sensor, thus, cluster sizes and the summed cluster ToT values increases in both sensors with a tilt of 15°.

Figures 10 and 11 summarize efficiency measurements as functions of bias voltage for sensors of 100 µm and 50 µm, respectively. It is clearly demonstrated that the particle-detection efficiency is higher when the sensor is inclined by 15°. Furthermore, it is seen that the sensors can be operated with high efficiency at a bias voltages as low as 2.5 V. At a bias of 10 V, efficiencies to perpendicular (tilted) tracks are found to be 99.5% (99.8%) for the 100 µm sensor, and 98.9% (99.6%) for the 50 µm sensor. The higher efficiency observed in the data collected at DESY is believed to primarily be due to the DUT being tuned to the high amplification described above in combination with the lower charge collection threshold of 400 e^- at DESY compared to 800 e^- at CERN.

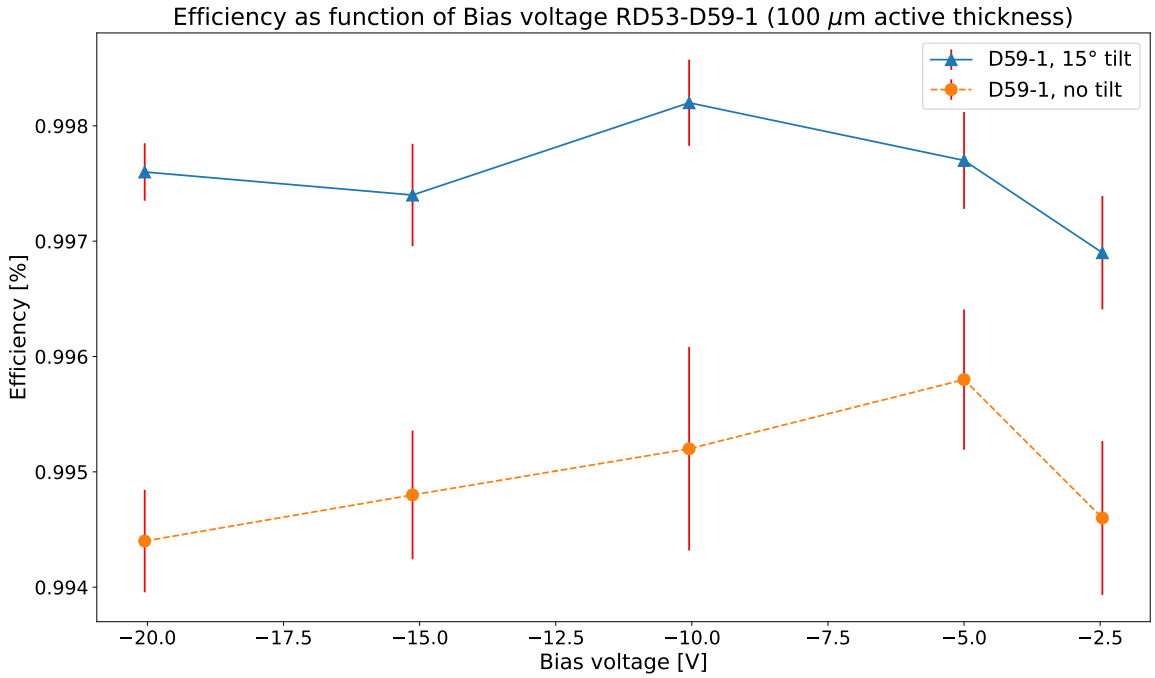

Figure 10. Efficiencies for different bias voltages for a 100 µm thick sensor at perpendicular beam incidence (orange), and an incident angle of 15° (blue).

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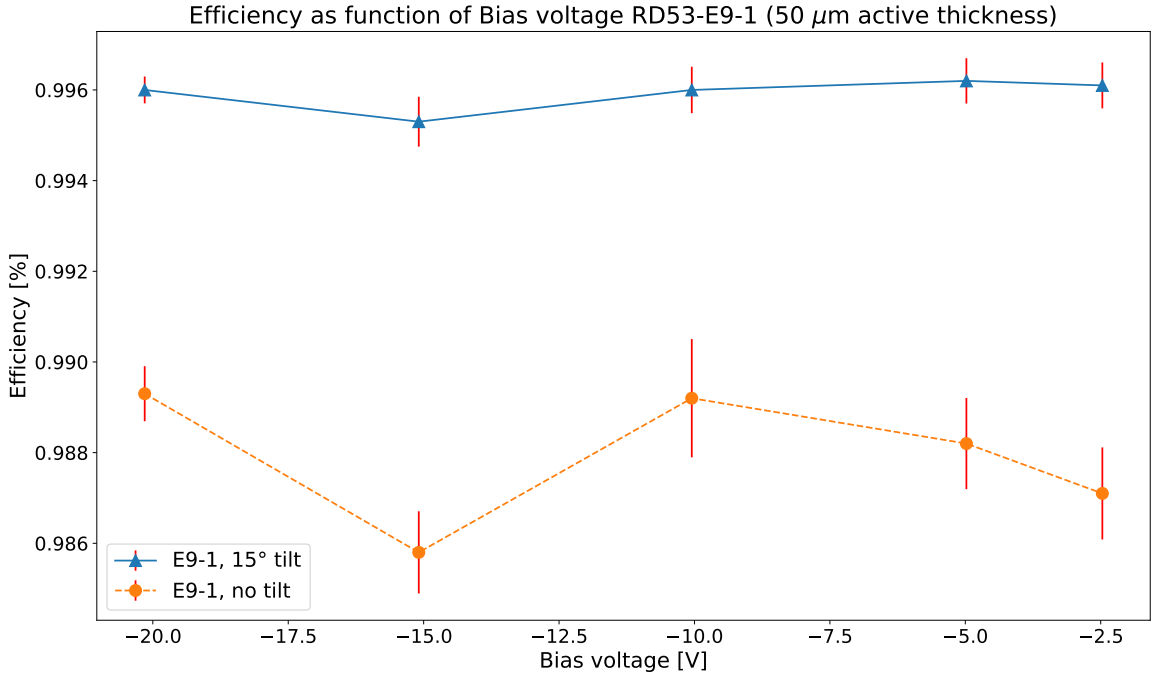

Figure 11. Efficiencies for different bias voltages for a 50 µm thick sensor at perpendicular beam incidence (orange), and an incident angle of 15° (blue).

4.3.2 Studies of irradiated sensors

Samples were irradiated to fluences of 5×10^{15} $n_{eq}cm^{-2}$ and 1×10^{16} $n_{eq}cm^{-2}$, and efficiencies were also studied as functions of bias voltage. In this study, the tracks passed through the sensors at normal incidence. Figure 12 shows the ToT distribution for the DUTs D61-2 (left) and D62-1 (right), with a threshold tuned to 1 ke^- and 0.5 ke^- respectively. The different shapes of the distributions are a consequence of the difference in thresholds where the distribution for D61-2 in figure 12 have been cropped by a too high threshold setting. The saturated bin (bin 14) in both distributions corresponds to a long tail as expected from the Landau-Vavilov distribution.

Figure 13 shows the efficiency as a function of applied bias voltage. An efficiency above 97% is reached for a bias of about 40 V for sensor D61-2 and above 96.5% at about 80 V for D62-1.

5 Summary and conclusions

We have described the production of 3D sensors at SINTEF of the 'RD53A' design, and presented results of subsequent tests in pion and electron beams for unirradiated sensors as well as for sensors irradiated to fluences of 5×10^{15} $n_{eq}cm^{-2}$ and 1×10^{16} $n_{eq}cm^{-2}$. It is demonstrated that unirradiated sensors of 50 µm and 100 µm active thickness can be operated in a high momemntum pion beam at efficiencies above 98.6% for tracks at normal incidence for a bias of 10 V.

According to the technical design report for the ATLAS ITk pixel detector [3], a minimum hit efficiency of 96% is required for pixel sensors in the innermost layer of the ITk after an irradiation to the target fluence of 1×10^{16} $n_{eq}cm^{-2}$ at normal beam incidence and with an applied bias voltage below 150 V. The results presented in this paper show that the tested samples reach an efficiency

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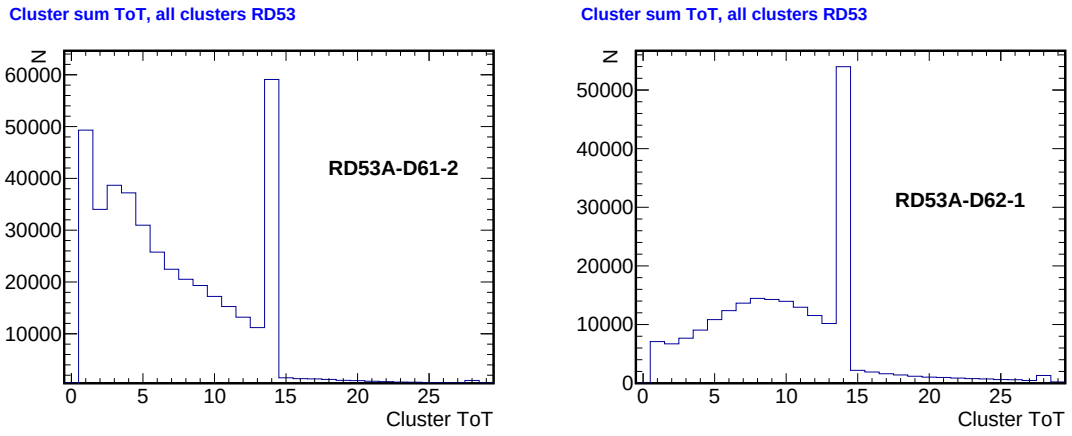

Figure 12. TOT distributions for clusters of the D61-2 (left) and D62-1 (right) sensors, irradiated to fluences of 5×10^{15} $n_{eq}cm^{-2}$ and 1×10^{16} $n_{eq}cm^{-2}$ respectively. The rightmost peaks in the cluster sum ToT plots, in bin 14, are due to saturation at the highest value for the ToT (14) in a single pixel.

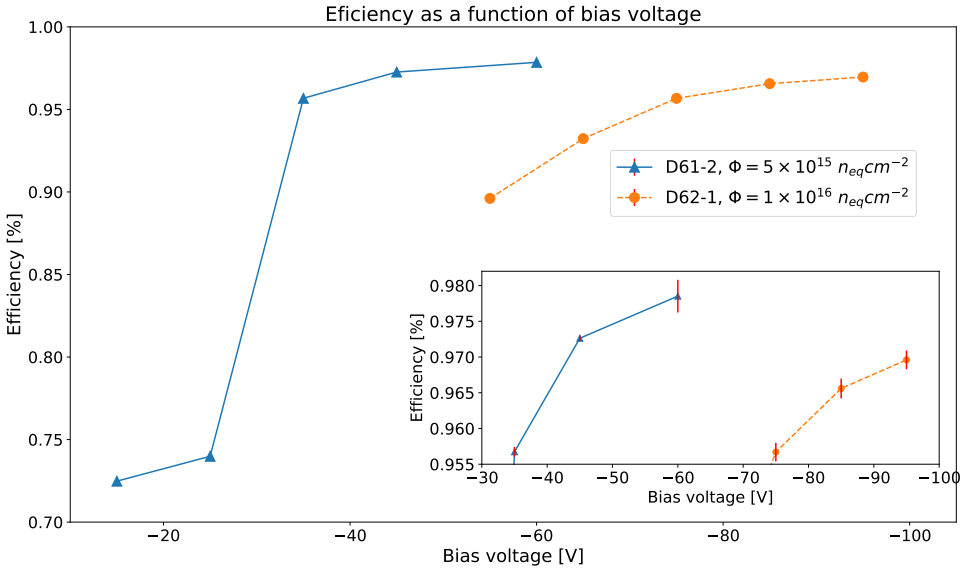

Figure 13. Efficiency as a function of applied bias-voltage for two irradiated sensors. Irradiation to a fluence of $5 \times 10^{15} n_{eq}/cm^2$ (blue), and $1 \times 10^{16} n_{eq}/cm^2$ (orange). The inset is a zoomed view of the last three measurements for each sensor to see the uncertainties.

above 97% for an irradiation of 5×10^{15} $n_{eq}cm^{-2}$ with a bias voltage of $V_{bias} = 40$ V, and above 96.5% with a bias voltage of $V_{bias} = 80$ V after an irradiation of 1×10^{16} $n_{eq}cm^{-2}$, thus meeting the requirements for the ITk phase II upgrade.

Acknowledgments

This work was funded by the Research Council of Norway (RCN).

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The measurements leading to these results have been performed at the Test Beam Facility at CERN Geneva (Switzerland) and at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

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