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Design, Fabrication, and Characterization of Conjugated Polymeric Electrochemical Memristors as Neuromorphic/ Integrated Circuits

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Design, Fabrication, and Characterization of Conjugated Polymeric Electrochemical Memristors as Neuromorphic/Integrated Circuits

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Abstract

Organic materials are promising candidates for future electronic devices compared to the complementing inorganic materials due to their ease of processability, use, and disposal, low cost of fabrication, energy efficiency, and flexible nature toward implementation as flexible and non-conformal devices. With that in mind, electrochemical materials have been widely demonstrated with commercial use as sensors, displays, and a variety of other electronic devices. As Moore's law predicts the increase in the density of transistors on a chip, the requirement to create either smaller transistors or the replacement of the transistor device entirely is apparent. Memory resistors, coined "memristor", are variable resistive tuning devices that are capable of information processing and data storage in one device. This work focuses on the embodiment of a non-volatile conjugated polymeric electrochemical memristor. Three-terminal memristive systems are fabricated and studied using various electrochemicals (a self-doped PEDOT derivative, a polypyrrole, and a dithienopyrrole derivative) and are tested for their electronic properties and biomimicking capabilities. Optical absorbance properties are studied in order to verify the electrochemical material's redox tuning potential for their respective oxidized and reduced chemical forms. The three-terminal device employed a post-synaptic "read" channel where conductivity of the electrochemical material was equated to synaptic weight and was electronically decoupled from the pre-synaptic programming electrode by means of a polymeric gel electrolyte. Basic electronic characteristics are exhibited for these three devices such as state stability and retention, non-volatile voltage-driven conductivity tuning, input parameter characteristic trends, and power consumption per input program. Biological synapses consume, on the order of, 1 - 100 fJ of energy per synaptic energy. The electrochemical materials used in this study, at their most optimized input parameters, were capable of demonstrating a 4.16 fJ/mm^2 power consumption per input pulse and lead to a promising candidate for implementation as future artificial neural networks. Biological mimicry was displayed for these devices in the form

of paired-pulse facilitation and paired-pulse depression, both a form of short term memory which observes the effect the timescale between two incoming inputs has on the change in the final output signal. Toward the indication for the replacement of transistors with three-terminal memristors, basic circuit operations are achieved and demonstrated for these devices. These operations include both Boolean and elementary algebra, key features that demonstrate data processing and storage in-memory where the physical states of the conjugated polymer film represent either logical statements or arithmetic counting variables. The Boolean algebra demonstrated the use of a single memristive device equal to a variety of single logic gates (AND, NAND, OR and NOR) where, by wiring several devices in series, more advanced combinational logic gates can be achieved. Furthermore, each device was capable of displaying elementary algebra for the basic arithmetic functions of addition, subtraction, multiplication, and division. In regards to thin film deposition techniques, the self-doped PEDOT device employed roll-to-roll gravure printing, a high speed and high resolution commercially used deposition technique. The polypyrrole device was fabricated implementing an *in-situ* polymerization technique, referred to as vapor phase polymerization, and demonstrated the use of this technique toward non-conformal devices. The dithienopyrrole derivative was polymerized through the same vapor phase polymerization technique as the polypyrrole and used in tandem with screen printing in order to construct the final device, including the oxidant film, the silver electrodes, and the polymeric gel electrolyte.

Dedication

This work is dedicated to my loving and supportive family, my parents, Marty and Martha Grant, and my brother and sister-in-law, Adam and Kaitlyn Grant. It is all thanks to their continued support that I made it to this point. To my mom and dad, you pushed me to become the best version of myself, always inspiring me to think creatively and to take on as many new adventures in life as possible. To my brother and sister-in-law, thank you for being a home for me to escape to, to enjoy, explore, rest, and relax.

I want to thank my lifelong friends Nicolas, Noah, and Lou. Thank you for the countless amount of trips you made to visit me. Thank you for always having my back, always supporting me, and always answering the phone. Thank you for always inspiring my creative side, especially with music. I cherish the music we have made together and often find myself listening to those songs. I also want to thank all of the friends I've made along this journey. To Shane and Anna, Sean and Emily, and Boii George, you made my undergraduate experience at Clemson remarkable with memories I'll never forget. And to Matt, Sarah, Adam, Haley, Travis, Taylor, and Addy, you all made my time here in graduate school very special. I always felt very welcomed and comforted by our encounters. There are so many lessons I've learned from each and every one of you. Best of luck to all of you with your future endeavors.

Acknowledgments

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Chapter 1

Introduction

1.1   Introduction

Memory resistors, a device now referred as memristors, was theoretically established by Dr. Leon Chua in 1971 [1–3]. The memristor is described as the fourth passive circuit element, in relation to the resistor, capacitor, and inductor (*cf.* **Figure 1.1**), which functions as a nonvolatile tunable resistor [1, 4]. The first notable experimental implementation was achieved by Hewlett Packards labs in 2008 based on a metal/oxide/metal architecture envisioned as a two-terminal device [4]. The oxide film reported, specifically the inorganic material TiO_2, exhibited a pinched hysteresis current-voltage curve demonstrating a unique system capable of bistable switching. In the inorganic's oxidized (doped) form, TiO_2, it is an electrical insulator with a high resistance to any electrical current flow present. Through fabricating a reduced (dedoped), oxygen-poor TiO_2 thin film, referred as TiO_{2-x}, oxygen vacancies are present in the crystal lattice and reduce the resistance of the material. The oxide film for the device is stacked with the oxidized TiO_2 over the reduced TiO_{2-x}, sandwiched between to platinum electrodes. By biasing the device with an electric current, oxygen vacancies act as mobile charge carriers across the doped and dedoped films, where the resistance of the device is calculated as the sum of the contributions from these two layers. The movement of these oxygen vacancies into or out of each respective layer creates a physical rearrangement of the crystal lattice, shifting the boundary line between the doped and dedoped layers, which therefore adjusted the resistance of this device. At a specific threshold (voltage or current), the device's response drastically switches from a low-resistance state (LRS) to a high-resistance state (HRS). These two distinct responses are

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analogous to a binary switching system referred as the "1" and "0" state (in relation to a transistor's ON and OFF state). Since the memristors origin, there has been a vast majority of inorganic and organic devices developed and reporting, dating all the way back to 1960's as resistive switching systems [5].
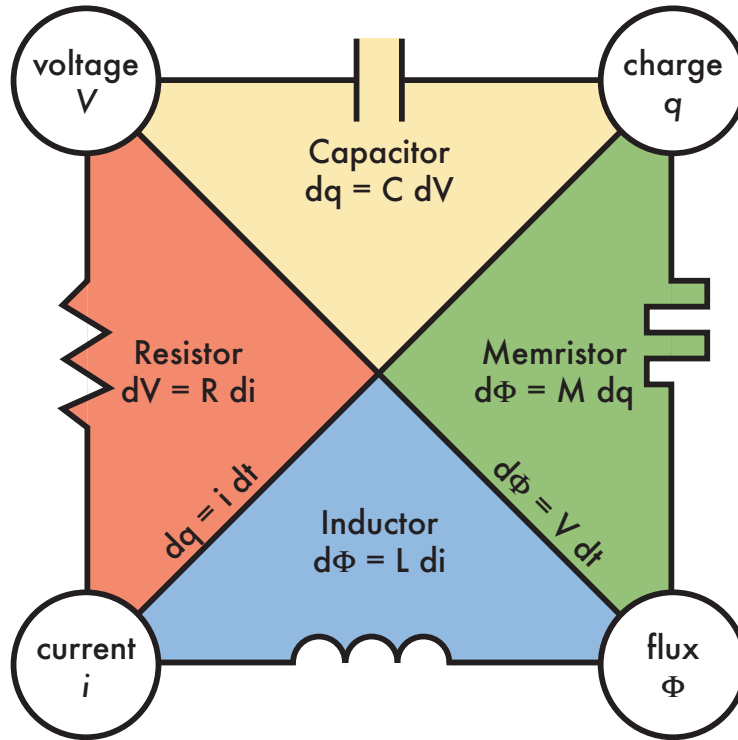
Figure 1.1:   The four fundamental passive circuit elements and their relations.

A key application for memristors is that they act as variable resistors. The analogy to understand how a memristive device operates is explained in regards of a water hose [6]. The water flowing through the hose represents the electric charge of the system, the pressure of the incoming water represents voltage, and the rate of flow represents electrical current. For a simple resistor, the obstruction of electronic charge is similar to the hose's diameter, where a narrow pipe leads to higher resistance and a wide pipe leads to lower resistance. However, while a resistor has a fixed value, the memristor can change the pipes diameter based on the amount and direction of electronic charge present as a function of integration time. As water flows through the pipe in one direction, the pipe expands dynamically and becomes less resistive. By reversing the waters direction, the pipe shrinks and becomes more resistive. By removing any flowing water, the pipe retains its diameter

from where water last went through it, expressing the static memory effect that a memristor can portray.

Figure 1.2:   Electronic circuit models for **(a)** two-terminal and **(b)** three-terminal memristors.

While many of the reported memristor devices are fabricated as two-terminal based systems [4, 7–10], three-terminal systems have demonstrated similar memristive qualities [10–17]. The electronic circuit models are shown in **Figure 1.2** for both two- and three-terminal based memristors. In regards to their programming sequence, two-terminal based systems rely on a small "read" voltage pulse followed after each subsequent "write" voltage pulse application (*cf.* **Figure 1.3a**). The small "read" bias measures the resistance state of the device without appreciably altering the state. This design leads to long wait times between programming states and will impede on fast switching speeds or fast reading requirements for future technologies. The three-terminal system overcomes this effect where one electrode, often referred to as the gate (G) or pre-synaptic electrode, is the "writing" or programming electrode and the other two electrodes, referred to as drain and source (DS) or post-synaptic electrode, can continuously "read" the systems properties without interfering with each respective films state (*cf.* **Figure 1.3b**).
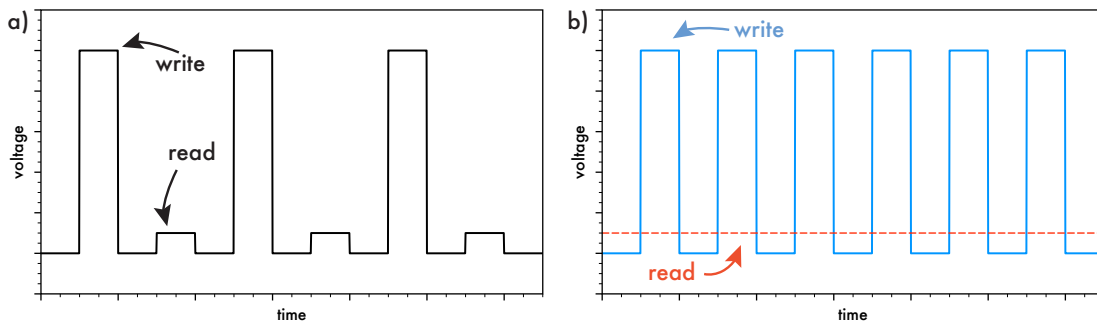
Figure 1.3:   Example of voltage-driven biases for **(a)** two-terminal and **(b)** three-terminal systems.

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1.2 Memory Resistive Devices

The memristor was predicted to be a two-terminal device with dynamic resistance that is determined by the integral of current flowing through it [1]. As an integral relationship, applying zero current would result in a constant charge, thus leaving the resistance constant. This proves that the theorized memristor possesses the ability to retain a resistance value even after the power source is removed from the device. Unlike the capacitor and inductor, this is not an energy storage device, so the voltage must equal zero whenever the current goes to zero. This causes the current-voltage (i-V) curve to produce a pinched hysteresis loop, revealing that the device has a memory effect associated with it. As the fourth circuit element, the memristor is a relation established between electronic charge (q) and magnetic flux (ϕ). The theory of the memristor states that memristance (M) value can either be controlled by electronic charge (q) or by magnetic flux (ϕ). When discussing a memristive system that is controlled by electronic charge:

$$M(q) = \frac{d\phi}{dq} \tag{1.1}$$

knowing that

$$\phi = \int V\, dt \tag{1.2}$$

and

$$q = \int i\, dt \tag{1.3}$$

memristance can be correlated as a voltage- or current-driven system such that:

$$M(q(t)) = \frac{V(t)}{i(t)} \tag{1.4}$$

The memristor was considered nothing more than a mathematical curiosity until the first successful fabrication of a memristive device was published in 2008 [4]. Mathematically, a memristor can be defined by its static (Equation 1.5) and dynamic (Equation 1.6) states using the state variables for voltage (V), current (i), resistance (R), time (t), and a set of state variables (w).

$$V = R(w, i)i \tag{1.5}$$

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$$\frac{dw}{dt} = f(w, t) \qquad (1.6)$$

The value of w controls the resistance state of the memristor, where both OFF and ON states correlate to two (or more) distinct values of w.

Of the vast majority of memristor studies, the main principles discussed envelop the following physical- or chemical-based classifications: filamentary conduction [18–22], ionic conduction [23, 24], charge transfer [25–27], space charge and traps [28–31], conformational shape change [7, 32–37], phase change material [38–41], redox-active electrochemicals [14, 16, 42–50], and other niche classifications or hybrid combinations of these listed. Filamentary conduction occurs as metallic pathways begin to localize between electrodes from the flow of current. This pathway can either be a bridge formed of solid metal or a conglomeration of nanoparticles and effects the electric field in order to manipulate the conductivity as a metallic bridge within the film forms. Ionic conduction occurs as ions move through defects in a crystal lattice from one site to another. As a result, device's exhibit conductivity switching due to electrochemical reactions doping in the host matrix, creating a p-n junction. Charge transfer occurs from electron donor/acceptor pairs as electronic charge is transferred between the donor molecule to the corresponding acceptor molecule. By tuning the properties of the materials used for the donor and acceptor and the bias pattern applied, the resulting electrostatic interaction manipulates the system's conductivity state. Space charge and traps utilizes an energy barrier created by these defects (traps) in the system to prevent the mobility of charge carriers. After a certain threshold of energy is applied, charge carriers fill in the traps which modulates the conductivity by lowering the energy barrier of mobility in the system. Conformational shape change occurs as macromolecules realign their chemical structure under environmental stimuli (i.e. temperature, pH, light, voltage). Certain alignments produce an environment where the charge carrier mobility is more or less favorable, leading to the manipulation of conductivity states. Phase change materials rely on the transition of the active material from one state to another (or several states, based on the material's capability) in order to manipulate the device's conductivity. Redox-active electrochemical materials employ a chemical change in the redox species in order to alter the conductivity between it's oxidized (doped) and reduced (dedoped) state. All of these principles have been shown to exhibit reversible bistable resistive switching, if not multi-state switching capabilities. Typically, by applying a reverse bias of a similar amplitude

and duration, these operations are reversible where a device can switch back from the HRS to LRS, or vice versa. This dissertation puts an emphasis on the application of redox-active electrochemical materials in order to fabricate memristive-based systems.

1.3 Electrochemical Materials

A variety of organic polymers have been demonstrated to exhibit redox potential properties as electro-active macromolecules that contain localized sites or group that can undergo a transfer of electrons, notably oxidation (loss of electrons) or reduction (gain of electrons) [43]. These electrochemical redox materials have been widely used as biosensors [51–53], electrochromic devices [54], energy storage devices [43], organic electrochemical transistors [14, 51, 52, 55, 56], and neuromorphic computers [14, 50, 57]. The main classes of electrochemical materials that demonstrate redox potentials consist of conjugated, free radical-containing, and carbonyl-functionalized polymers [58]. The focus of this dissertation puts an emphasis on conjugated polymers for their use as possible biomimetic emulators and advanced functional electronic operations. The three most commonly used and well known redox-active conjugated polymers are poly(3,4-ethylenedioxythiophene) (PE-DOT) [59, 60], polypyrrole (PPy) [61, 62], and polyaniline (PANI). [62–65] (*cf.* **Figure 1.4**). This list is not exclusive as there are a variety of derivatives and new redox-active organic compounds being synthesized based on tailoring the chemical structure, essential to the desired application for the material's electronic and optical properties. The three presented conjugated polymers have a conductive polymer backbone, however this is not always the case as certain species are designed with an insulating polymer backbone that is attached with a redox-active conductive pendant moiety [66]. The working principal of conjugated polymer electrochemical materials involve organics in the form of cyclic ring structures that are conjugated with double bonds along the polymer backbone or pendant side group [43]. By doping (oxidizing) or dedoping (reducing) these structures, (either by chemically, optically or electronically stimulating the structure), the conjugation (double bonds) will relocate around the cyclic ring and propagate along the redox-active group. When the double bonds are in their "expected" positions, the chemical structure is defined in its oxidized state, whereas when the conjugation propagates along the polymer backbone, it moves towards its reduced state. Redox-active conjugated polymers have drawn a lot of interest as they possess ease of processability with large-scale production, high electrical conductivity, flexibility, low weight, and low cost

for synthesis [43, 58, 66]. From their origin, PANI was extensively used for rechargeable batteries [67], supercapacitors [68], and photochromic devices [69]. However, with the major drawbacks of poor chemical and thermal stability and low solubility or insolubility to suspend in most common solvents [70], PANI was abandoned for a superior analog, PEDOT. PEDOT has excelled from the commercial standpoint as it displayed high chemical and thermal stability, high conductivity ($\sigma >$ 3000 S/cm), and use as a transparent active layer or electrode for optical displays [43, 71]. PEDOT is a p-type material, p-type meaning the electronic conductivity is due to the mobility of positive holes, and often contains the addition of a polystyrene sulfonate (PSS) dopant. The PSS additive acts as a counter ion, supplying a negative charge to the positively charged PEDOT species and aids in maintaining and stabilizing the electroneutrality of the p-type conjugated polymer [72]. A result of tuning the polymer's redox (doping) states, charged defects (in particular polarons and bipolarons) become present in the redox-active groups and are responsible for varying the electronic conduction potential of these materials [73].
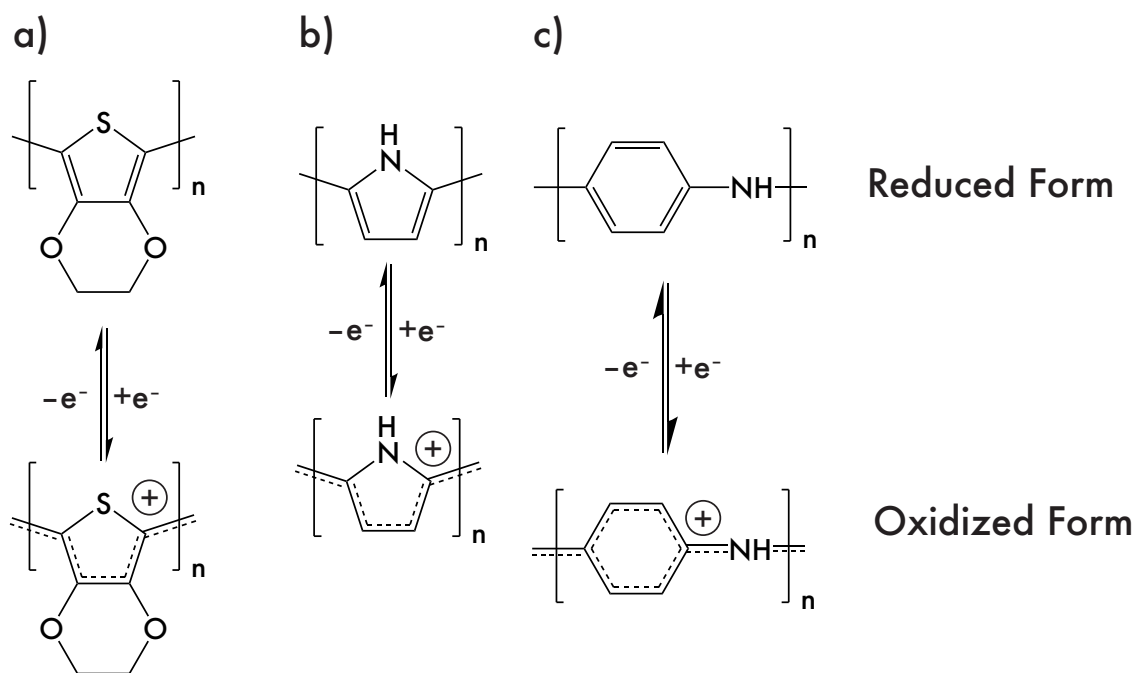
Figure 1.4:   Common redox-active electrochemical conjugated polymers in their reduced (top) and oxidized (bottom) forms: **(a)** poly(3,4-ethylenedioxythiophene) (PEDOT); **(b)** polypyrrole (PPy); and **(c)** polyaniline (PANI).

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1.4　Thin Film Deposition Techniques

The list of film depositions includes chemical (dip coating, spin coating, electrochemical polymerization, and chemical vapor deposition) and physical (printing sputtering, ion plating, and thermal evaporation) deposition techniques. This section will focus on the primary thin film deposition techniques that are used throughout this dissertation in order to fabricate electronic devices.

a) Solution Deposition　b) Rotational Spinning　c) Solvent Evaporation
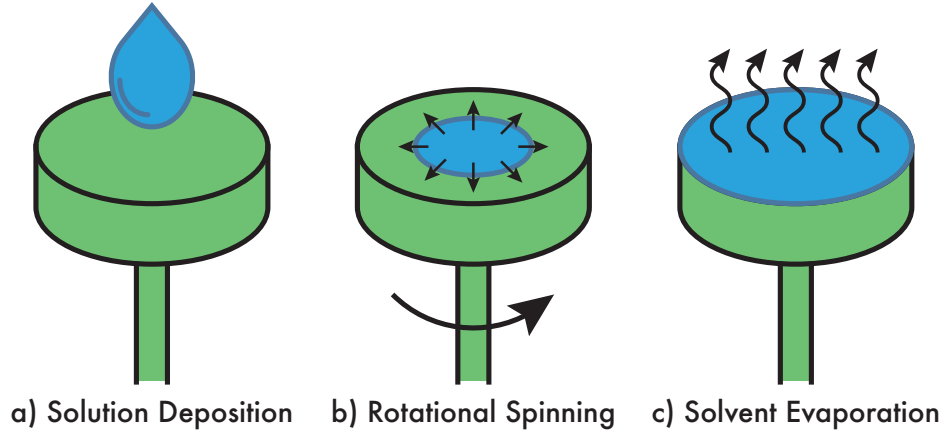
Figure 1.5:　Spin coat procedure including the following steps: **(a)** solution deposition of solution-processable material; **(b)** rotational spinning to shear-thin the solution over the desired substrate; and **(c)** film evaporation to remove residual solvent, either in air, in a vacuum, or by annealing the substrate.

Spin coating is a widely used technique reported for many lab-based small batch samples as it is tedious and takes a long time to make a lot of samples [74]. Spin coating uses the centrifugal force of rotation in order to create thin and uniform films on flat and smooth substrates or targets [75]. The final products are used in a wide range of applications including optical or electronic devices, surface processing, resist coatings, and coating primer or photochromic solutions [76]. This is a simple technique that mainly contains three steps: 1) solution deposition, 2) rotational spinning, and 3) solvent evaporation. During the first step, solution deposition (*cf.* **Figure 1.5**a), a microsyringe or pipette is used to drop the desired solution over a stationary or rotating platform holding the substrate at a specific accelerated speed. The amount of solution dropped is critical where in excess of solution, a critical height or thickness of the film will be met. This is a major disadvantage for this film deposition technique due to the loss of material required to coat. As the substrate is initially coated with the solution, a finite amount is actually covering, or "wetting", the substrate's surface. The substrate can be inoculated with the solution in various ways, either a) an excess amount that

inundates the entirety of the substrate, b) a large bolus to the center of the substrate or various smaller boluses to the corners of the substrate (if the substrate is rectangular), or c) a consistent stream of solution at an elevated delivery position for an initial amount of time during the ramp sequence. The second step is when the platform and substrate are accelerated up to the desired rotational speed (*cf.* **Figure 1.5**b). As the sample holder accelerates, centrifugal force is applied to the solution, spreading out the solution over the entire substrate's surface to make a coated film. In the initial ramp up to the desired rotational speed, excess solution is expelled from the substrate's surface by this rotational movement. Following the ramp up sequence, the substrate and platform reach the desired speed and the solution is thin enough that viscous shear drag exactly balances rotational accelerations. As the platform and substrate spin at a constant rate, viscous fluid forces dominate fluid thinning behavior. This step is characterized by gradual fluid thinning of the solution. Fluid thinning is generally quite uniform, though only with solutions containing volatile solvents. Edge effects are often seen because the fluid flows uniformly outward and forms droplets at the edge as the solutions is cast off. Thus, depending on the surface tension, viscosity, rotation rate, etc., there may be a small bead of coating thickness difference around the rim of the final film [76]. The final step, solvent evaporation (*cf.* **Figure 1.5**c), is a necessary film drying stage in order to get the result of a smooth and even thin film coating. The rate of evaporation of the solution's solvent can be controlled by adjusting the ventilation environment (in a fume hood or vacuum chamber) or by annealing the sample at or above the solvent's boiling point. The final thickness of the film depends on the solutions viscosity, the rotational speed of the platform, the rotations acceleration ramp rate, and the ventilation environment of the chamber. Advantages of this technique include the ease of adjusting final film thickness by changing ramp rate, spin speed, or switching solvent or solution concentration to a different viscosity, along with the low cost of operation with fast sequencing times. The key advantages of spin coating is the ability for the films to become progressively more uniform as it thins out during the rotational spinning sequence. When the film becomes completely uniform during the spin, the film will remain uniform for the duration of the process. While the disadvantages are few, they are important as cost of materials rise and as substrate size increases. Substrates with large dimensions can not be spun at high rates in order to fabricate thin films. The biggest disadvantage of this technique is the lack of material use or reclaiming efficiency. Typically, this process only utilizes 2 - 5% of the material cast onto the substrate, where the remaining 95 - 98% is cast off into the spin coaters bowl and is deemed as waste [76].

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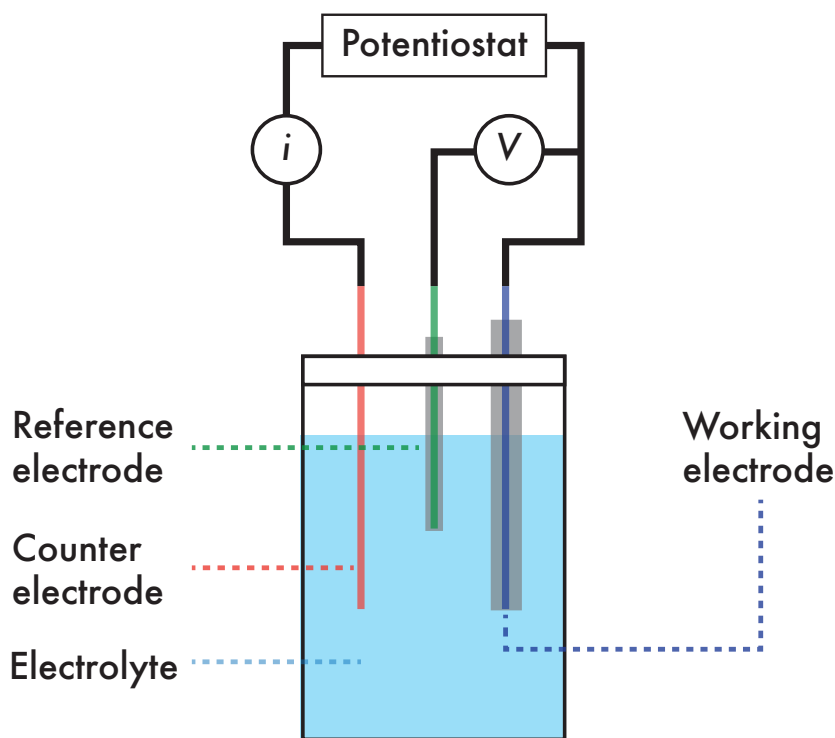
Figure 1.6:   Three-terminal cell electrochemistry procedure including the following components: a reference electrode; a counter electrode; and a working electrode.

A common technique to polymerize and fabricate conjugated polymer films is referred to as electrochemical polymerization (ECP). This technique often involves the use of a three-terminal liquid cell consisting of a working electrode, a reference electrode, and a counter electrode submerged in a liquid supporting electrolyte (*cf.* **Figure 1.6**) and measures the flow of electrons as a function of chemical (redox) changes [77–80]. Typical electrode materials used include glassy carbon, platinum, silver, gold, and ITO for the working electrode; platinum wire and glassy carbon rod for the counter electrode; and silver / silver chloride ($Ag/AgCl_3$) encased in a saturated potassium chloride (KCl) solution, a standard hydrogen electrode (SHE), a saturated calomel electrode (SCE), and a silver / silver nitrate ($Ag/AgNO_3$) encased in 0.01 M acetonitrile [77]. The supporting electrolyte needs to meet three criteria: 1) the electrolyte must be highly soluble in the chosen solvent; 2) the electrolyte must be chemically and electrochemically inert in the given conditions of experimentation; and 3) the electrolyte solution must be capable of purification (often achieved by purging the solution with an inert gas) [77]. Supporting electrolyte solutions (often in the order of 0.1 M in solvent) act as

a way to balance the charge of the system. As electron transfer occurs at the surface of the electrodes, the presence of the electrolyte will migrate to balance the charge and complete the electronic circuit. With that in mind, large supporting electrolyte concentrations are a requirement in order to limit analyte (i.e. solvent) migration. To ensure that lack of migration of the analyte, high electrolyte concentration ensures that it is statistically more probable that the electrolyte will migrate rather than the analyte in order to charge balance the electrode surface [77]. Ammonium salts have easily become the electrolyte of choice when experiments are performed in organic solvents. For organic solvents such as dichloromethane or acetonitrile, tetrabutylammonium salts ($^+$NBu$_4$) have been commonly reported. Tetrahexylammonium ($^+$NHx$_4$), another widely used ammonium salts, becomes necessary for use when attempting to solubilize in less polar solvents, such as benzene. While ammonium salts are a standard for the cation of these electrolytes, the counter anion is less standardized due to the redox potential window for measurements. Common counter anions used include dimethylanilinium ($[B(C_6F_5)_4]^-$), hexafluorophosphate ($[PF_6]^-$), tetrafluoroborate ($[BF_4]^-$), and perchlorate ($[ClO_4]^-$) [77]. The purity of the electrolyte is paramount due to the required high concentration present as any slight impurity can interfere with the electrical test and measurement of the system [78]. The advantages of this technique include the small amount of materials required (only 10 - 50 mg of monomer to perform repeated experiments), rapid analyses of the chemical's properties and characteristics, and accuracy and precision with easily repeatable and reproducible final products [78]. In regards to the electrodes used in this system, the working electrode (WE) carries out the electrochemical event of interest. The potential applied to the WE is supplied via a potentiostat where the potential of the WE is a function of the potential of the reference electrode (RE). The most important feature of a WE is the necessity for the WE's surface to be extremely clean and inert to redox potentials, especially in the range of the redox-active species being tested. The RE has a well defined and stable equilibrium potential. The purpose of the RE is to serve as a reference point against which the potential of all other electrodes are measured in the electrochemical cell. The RE's, specifically Ag/AgCl and Ag/AgNO$_3$ are encased and separated from the electrolyte solution by a porous tube. To verify the stability and reference potential of the RE, an internal standard can be used for calibration, specifically using ferrocene (Fc) as this inorganic species has well reported oxidation (ferrocenium, Fc$^+$) and reduction (ferrocene, Fc) potentials. The counter electrode (CE) is used in order to complete the three-terminal cell such that current is recorded as a function of electronic flow between the WE and the CE. To ensure that the kinetics of the reaction

occurring at the CE do not inhibit those occurring at the WE, the surface area of the CE is greater than that of the surface area of the WE. When analyzing a reduction peak present at the WE, an oxidation peak occurs at the CE. As such, the CE should be chosen to be as inert as possible to redox potentials. By introducing a small amount of monomer into the supporting electrolyte (typically 10 - 50 mg at a concentration of 0.01 M), film fabrication can be achieved over the WE. Conjugated polymers can be synthesized by two applied methods: cyclic voltammetry (sweeping voltages within a set range) or fixed potentiometry (constant voltage or current supplied at a single biased value) [81]. Both of these methods are highly controllable and capable of creating pristine, uniform, thin films [80–82]. The general drawbacks of this technique are the small batch sizes that create, most often, insoluble polymers. The insolubility of the polymers makes characterization with standard analytical techniques (NMR, GPC, etc.) near impossible. Unlike other chemical synthesis techniques, in electrochemical polymerization, electrons are not transferred directly between atoms, ions, or molecules but via the electronically-conducting circuit. This phenomenon is what distinguishes an electrochemical reaction from other conventional chemical reactions.
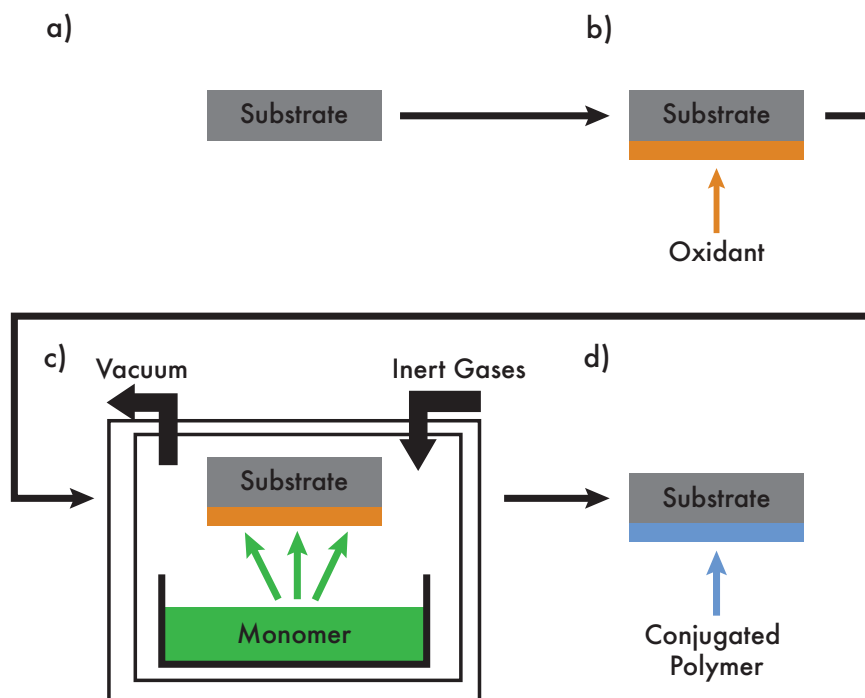
Figure 1.7: Vapor phase polymerization procedure including the following steps: (a) pretreatment of the substrate's surface; (b) coating the substrate with an oxidant; (c) exposing the oxidant-coated substrate to vaporized monomer under vacuum; and (d) post-treatment cleaning of the conjugated polymer film.

Vapor phase polymerization (VPP), also referred to as vapor deposition polymerization (VDP) or chemical vapor deposition (CVD), closely follows the operational mechanism of standard oxidative polymerizations [83–85]. Oxidative polymerization is a technique in which desired monomer is reacted with an oxidizing species, commonly being iron chloride ($FeCl_3$), typically in the form of a step-growth polymerization [83, 86]. In regards to oxidative polymerization using $FeCl_3$ and a 3,4-ethylenedioxythiophene (EDOT) monomer, cation radical formation is the limited rate determining reaction, forming positive ions spatially around the EDOT monomer. This is followed by the combination of cation radical-doped species and forms conjugated bonds through deprotonation (loss of the free radical cations). Polymerization continues in this form from a dimer out to the polymer state. Doping of the counter anion from the oxidant occurs as a simultaneous *in-situ* process [86]. While oxidative polymerization occurs as a step-growth phenomena, VPP follows a chain-growth polymerization reaction which occurs at the surface of the substrate [85].

The technique for VPP is similar to oxidative polymerization, however, instead of a wet chemical synthesis, VPP utilizes a thin film of an oxidant species (typically an iron-salt) exposed to monomer vapor in order to polymerize a thin film of the desired conjugated polymer [83–85] (*cf.* **Figure 1.7**). This technique has been demonstrated for photovoltaics [87], organic light emitting diodes [88], electrocatlysts [89], organic field-effect transistors [90], electrochromic devices [91], bio- and chemical-sensors [92], and neuromorphic computers [93]. VPP is a two-step process in which 1) an oxidizing agent is first deposited onto a substrate (*cf.* **Figure 1.7**b) and 2) the oxidant-coated substrate is exposed to monomer vapor inside an enclosed chamber (*cf.* **Figure 1.7**c), either at ambient pressure or under controlled low pressure vacuum that results in monomer sublimation and polymer film synthesis [83–85]. The deposited film is post-treated by washing with alcohol to remove any unreacted oxidant, adsorbed monomer, and other byproducts (*cf.* **Figure 1.7**d). The procedure for VPP often includes a thick-walled metal vacuum chamber, a manifold to feed in inert gas, a heat source or a variation of these components [85]. The key advantage to this technique is that, where many conjugated polymers are insoluble after polymerization [94, 95], VPP can fabricate films as-needed via this *in-situ* technique onto the final product or substrate without the need to solution-process after a conventional polymerization [83, 96, 97]. Common oxidants for this procedure include iron chloride, iron *p*-toluenesulfonate, iron dodecylbenzenesulfonate, iron trifluoromethanesulfonate, copper chloride, ammonium persulfate, along with many more which have been reported [83, 93]. The oxidants can either be cast or printed prior to gaseous monomer exposure or have been shown

to display promising film fabrication results with a co-vapor exposure of both oxidant and monomer vapors [83]. Through co-vapor exposure, pristine polymer films are created without the need for washing and drying post-processing treatment in order to remove prior residual oxidant. The key number of benefits for this technique include conformality, grafting, low temperature processing, and substrate independence [83, 85]. These benefits are bolstered by the advantages of the chamber used based on the modularity and ability to accommodate a wide range of low-to-high volatile compounds, making this technique ideal for testing new monomers and new vapor phase chemistries [85].
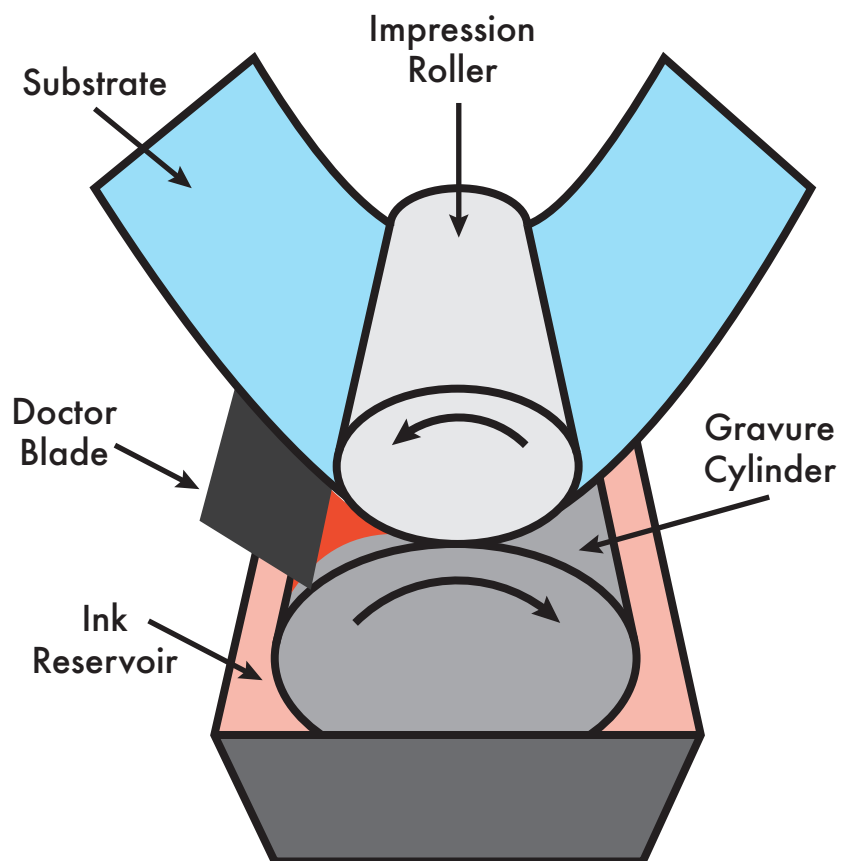
Figure 1.8: Roll-to-roll gravure printing procedure including the following components: a patterned gravure cylinder with well-defined cavities; a reservoir supply of ink for depositing onto the substrate; a doctor blade to restrict how much ink is deposited; and the substrate to be coated and patterned.

The term "printing" for optical or electronic devices often refers to a variety of techniques encompassing inkjet printing, aerosol jet printing, flexographic printing, rotary roll printing, gravure printing, and screen printing to list the majority. While each technique has its advantages and disadvantages, this report puts an emphasis on both roll-to-roll gravure and screen printing as use for

depositing thin films. Roll-to-roll gravure printing is an attractive technique which allows for high speed manufacturing with high resolution and repeatable prints. This technique has been implemented toward solar cells [98], field-effect transistors [93], lighting displays [91], and neuromorphic computers [57, 99] for electronic devices while this is a standard for fabrication of newspapers, magazines, catalogues and packing [100]. Gravure printing is a continuous process that relies on the deposition of an ink solution, supplied from a reservoir, onto the substrate via a gravure cylinder, engraved with the desired pattern (*cf.* **Figure 1.8**). Typically, a doctor blade is used to reclaim and continuously fill the engraved cavities on the gravure cylinder. The gravure cylinder, filled with ink, is brought into proper contact with the substrate A rubber impression roller, moving in the opposite direction of the gravure cylinder, aids to feed through the substrate as contact and imprinting is achieved by the gravure cylinder. A key feature of gravure roll-to-roll printing is the techniques capability to print low viscosity inks and excels with high deposition processing speeds (up to 15 m/s) [74]. This technique allows for patterning over non-planar surfaces in addition to upscaling fabrication to large scale manufacturing standards [100].
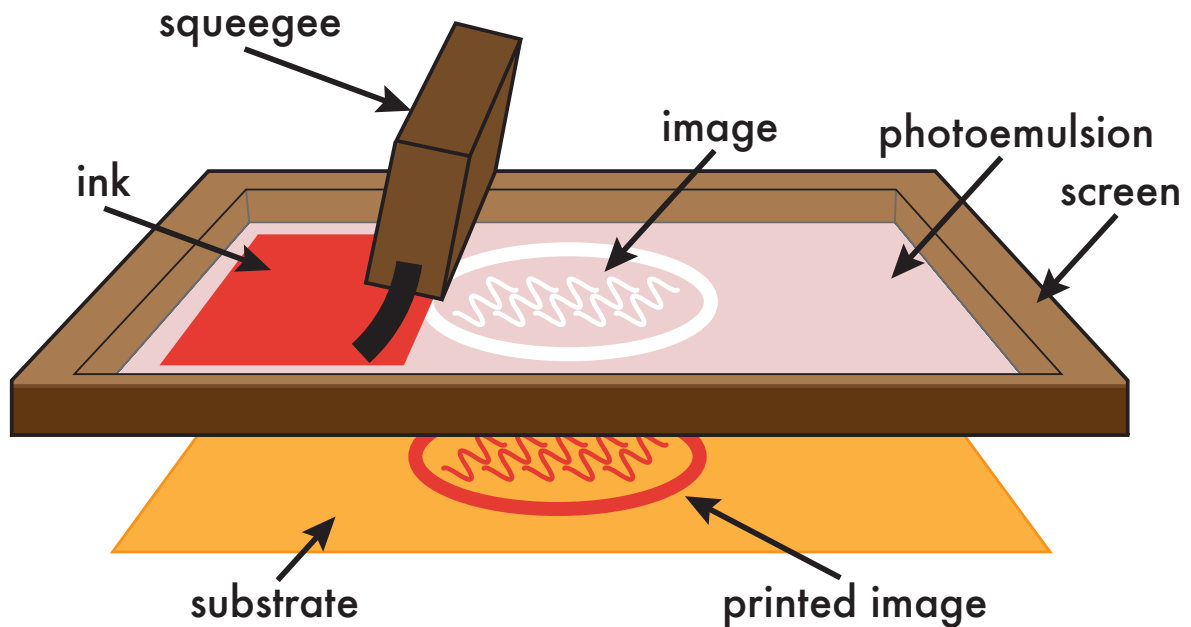
Figure 1.9:   Screen printing procedure including the following steps: **(1)** deposition of photoemulsion to pattern the screen; **(2)** applying ink onto the screen to deposit onto desired substrate; and **(3)** squeegeeing the ink over the screen to deposit onto the substrate.

Screen printing is a versatile technique that is capable of mass production of printed electronics that involves direct physical contact in order to transfer ink from a stenciled screen to the desired substrate [101]. Screen printing has been widely used to produce various electronic devices, including biofuel cells [102], RFID tags [103], supercapacitors [104], corrosion monitors [105], bio-analytical sensors [106], energy storage devices [107], lighting displays [108], and neuromorphic computers [109], along with many other facets of devices. The general procedure for screen printing is demonstrated in **Figure 1.9** and involves stretching the screen material, either woven fabric or metal, and coating with a photo-curable emulsion material in order to create the stencil for printing. The stencil is impressed onto the photo-emulsion after a curing process and washed out, leaving blocked and unblocked pores on the screen where the unblocked pores depict the stencil. These unblocked pores allow transfer of the ink from the screen onto the substrate. The screen is mounted over the substrate, ink is generously poured over the screen, and a squeegee is swept over the surface to squeeze ink through the unblocked pores to imprint the stenciled design onto the substrate. A variety of substrates are utilized with the printed technique, whether it be flexible or rigid surfaces. The viscosity of the ink is of grave importance for screen printing where thixotropic traits are desired, i.e. ink viscosities must exhibit a decrease to viscosity with an increase in shear rate [110]. Ink solutions with a high viscosity are often a prerequisite for this technique in order to avoid spreading and proper adhesion or cohesion for surface wetting to occur [100]. Another methodology to overcome the solution from spreading over the substrate is through pretreatment to the substrate. These pretreatments can include polishing and surface smoothing, plasma exposure, and temperature annealing treatments [111]. Screen printing is a versatile technique that is considered economical and easy to use with high reproducibility and incorporation of various materials in the design of an ink solution [111].

1.5 Overview

The chapters in this dissertation will discuss the following:

Chapter 1 introduces the topic of two- and three-terminal based memristor systems from the theoretical origin in 1971 to many experimentally designed inorganic and organic based systems. This chapter highlights the use of redox-active organic polymers toward the application of three-terminal conjugated polymeric electrochemical memristors (cPECMs). The theory and materials used for

these memristors are supplemented with a detailed description of common thin film fabrication techniques and how they can be used for developing these types of devices.

Chapter 2 examines the synthesis of a water-soluble, self-doped poly(sodium 4-((2,3-dihydrothieno [3,4-b][1,4]dioxin-2-yl)methoxy)butane-2-sulfonate) (S-PEDOT) derivative implemented as a cPECM. Through the development of this roll-to-roll printed device with a counter-redox architecture, the S-PEDOT cPECM is capable of highly distinct analog resistive tuning. By designing sophisticated voltage patterns, this device demonstrated its use as an operational Boolean logic gate, along with exhibiting elementary algebra (addition, subtraction, multiplication, and division) and synaptic mimicrking characteristics. This work has been previously published: [57] Benjamin Grant, Yuriy Bandera, Stephen H. Foulger, Jarmila Vilčáková, Petr Sáha, and Jiří Pfleger. Boolean and Elementary Algebra with a Roll-to-Roll Printed Electrochemical Memristor. *Advanced Materials Technologies*, 2021.

Chapter 3 introduces the technique of vapor phase polymerization in order to deposit the redox-active electrochemical species referred to as polypyrrole (PPy). By employing an oxidant-coated substrate, polymerization of any conjugated polymer can be achieved in a simple two-step process: 1) cover the desired substrate with an oxidant material, and 2) expose the oxidant-coated substrate to monomer vapor in order to polymerize. This technique paves the way forward for designing and fabricating electronic devices over conformal and non-conformal substrates, allowing for the theology of creating smart technology into every item in the world around us. This PPy-based cPECM achieves low-power consumption, on the order of 4.16 fJ/mm^2, while demonstrating basic memristive characteristics, along with Boolean and elementary algebra.

Chapter 4 builds upon the results of Chapter 3 by utilizing the vapor phase polymerization technique to develop devices utilizing another class of electrochemical materials, notably a dithienopyrrole (DTP)-based derivative. Two film deposition techniques are employed, vapor phase polymerization and screen printing, to create a uniquely designed DTP-based cPECM. This device displayed not only simple Boolean and elementary algebra, but was used to demonstrate a combinational logic gate, composed of only two printed devices with no additional components.

Chapter 5 concludes with an overview of the achieved success of the various designed, fabricated, and characterized cPECM devices. This is supplemented with discussion and suggestions for all future directions this effort can lead toward.

Other work pertaining to this effort have been published and are listed here: [112] Stephen

H. Foulger, Yuriy Bandera, Benjamin Grant, Jarmila Vilčáková, and Petr Sáha. Exploiting Multiple Percolation in Two-Terminal Memristor to Achieve a Multitude of Resistive States. *Journal of Materials Chemistry C*, 9:8975 - 8986, 2021. [**113**] Yuriy Bandera, Haley W. Jones, Benjamin Grant, Sarah Mell, and Stephen H. Foulger. Synthesis, Electropolymerization and Functionalization via Click Chemistry of *n*-Alkynylated Dithieno[3,2-b:2',3'-d]pyrrole. *RSC Advances*, 12:29187 - 29196, 2022.

Chapter 2

Boolean and elementary algebra with a roll-to-roll printed electrochemical memristor

2.1 Introduction

Inorganic/organic memristors have experienced vigorous research activity since 2008 with the verified existence of Chua's 1971 proposed fourth basic element [4, 114]. Nonetheless, the majority of memristive systems rely on some form of a stochastic creation/disruption of percolative paths inside a matrix to give rise to a binary (or abrupt) form of current switching. These systems were predominately developed to serve as a memory component in a von Neumann computer architecture [115] and have, especially in the case of inorganic systems, proven to be suitable for storing and processing information with numerous excellent attributes [114].

The memory requirements for a von Neumann computer architecture differ greatly from biologically inspired synaptic functions, where synaptic weights are modulated by the number and frequency of homogeneous spikes and take a continuity of values. A number of review papers [15, 116–119] have been presented that focus on memristors intended for neuromorphic applications and all share the common theme, that in this role, memristors must exhibit reliable analog properties including non-abrupt switching transitions, continuously variable resistance states, and

a predictable response. Compared to their inorganic counterparts, organic materials have several advantages when it comes to fabrication and implementation as a neuromorphic device. Organic materials can be integrated to large-scale production with low-cost manufacturing processes and high resolution lithography patterning along with tailoring the chemistry to desired chemical, electrical and mechanical properties [15, 119]. These traits allow memristor devices to provide a simple and effective route for fabricating physical artificial neural networks which are independent of software programming [4, 120].

Over the past few decades, organic electrochemical transistors (OECTs) have been explored as potential bioelectronics [51, 121], printed circuits [122], and neuromorphic devices [15, 50, 123]. A recent embodiment of an OECT was a non-volatile conjugated polymer-based electrochemical memristor (cPECM) that exhibited characteristics of an artificial synapse and could be useful for neuromorphic computing [50]. In this 3-terminal device, the redox state and conductivity of poly(3,4-ethylenedioxythiophene):poly(4-styrenesulfonate) (PEDOT:PSS) between two terminals was controlled by a third terminal, which allowed the state of conductance to be decoupled from the barrier for changing states. Neuromorphic devices based on electrochemical materials, such as PEDOT:PSS, have been shown to emulate essential artificial neuronal and synaptic plasticities for learning and memory behaviors [13, 50, 124–126], though other conjugated polymers have been utilized. For example, synapse-like behavior was demonstrated by a three-terminal light-stimulated organic field-effect transistor (OFET) which employed a p-type donor-acceptor conjugated polymer channel (poly(thienothiophene-*co*-1,4-diketopyrrolo[3,4-c]pyrrole) (PDBT-*co*-TT)) doped with an ionic additive (tetrabutylammonium perchlorate (TBAP))[127].

PEDOT:PSS has achieved widespread implementation into a host of organic devices due to its electrical conductivity and commercial availability as an aqueous dispersion of colloidal particles [128–130]. Specifically, PEDOT:PSS exhibits high electrical conductivity (1000 S/cm) coupled with optical transparency and has been exploited in a wide range of applications where a transparent conductive electrode is desirable and indium tin oxide is not preferred [131, 132]. Nonetheless, PEDOT:PSS has various technical issues that present challenges in its application. These issues largely stem from the use of PSS as external ions to compensate the positive charges on PEDOT. To achieve a water dispersible system, a hydrophobic PEDOT core is coated with a shell of excess hydrophilic PSS, yielding a colloidal particle with a diameter of several tens of nanometers [131], which presents difficulties in forming layers thinner than the colloidal particle size [133]. In addition,

the neat PEDOT:PSS dispersion requires a number of additives (e.g., ethylene glycol, dimethyl sulfoxide, and sorbitol) to achieve high levels of conductivity[59, 134, 135]. While these additives are known to improve the film's conductivity, they can create a more complex processing parameter inter-relationship and present challenges to achieving highly uniform printed films[136].

A key advantage of conductive polymers is their amenability to being printed into devices, where various printing techniques have been demonstrated [137–139]. Printing is a process which converges in on traditional manufacturing techniques with the advent of functional, processable nanoscale materials [138]. The art is rapidly becoming a science and inherently demonstrates a vast range of scalability from nearly microscopic to incredibly large and high-throughput, with a specific implementation being roll-to-roll (R2R) printing. R2R printing techniques have been employed in the creation of a range of electronic devices [74], such as large area photovoltiac devices [128, 140], memory devices [141], and sensors [139]. Recent advances in R2R printing achieved structures with a minimum internal linewidth of 3 μm at print speeds of 0.2 m/s [142]. Continued developments in printing electronic devices with a smaller feature size at higher printing speeds will require the development of semiconducting polymers that exhibit both high intrinsic conductivities and charge carrier mobilities without the need of additives prior to being formulated in printable "inks" [138]. To that end, a recently presented water-soluble self-doped PEDOT (S-PEDOT) with an electrical conductivity as high as 1089 S/cm without use of additives [143] was employed in the current effort in the R2R printing of a flexible cPECM.

2.2 Results and Discussion

Figure 2.1a presents a schematic of the cPECM sandwich device. The top layer forms the presynaptic electrode, which is composed of a conjugated polymer layer that sits atop of an electrolyte layer, which in turn sits atop a layer composed of the conjugated polymer and polyethyleneimine (PEI). The latter layer forms the postsynaptic electrode where a (D)rain and (S)ource electrode are attached to it. A synaptic weight is equated to the conductivity of the channel (i.e., oxidation state of S-PEDOT) between the D and S electrode, while the conductivity of the channel is programed through voltage pulses (synaptic events) to the (G)ate electrode attached to the presynaptic layer.

In the current embodiment of a cPECM, the self-doped and water-soluble form of poly(3,4-
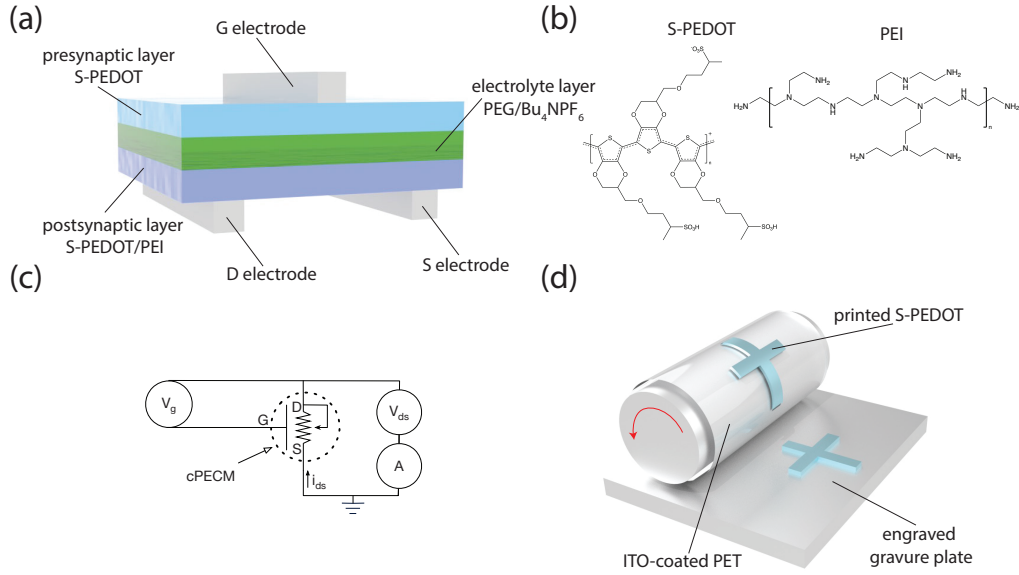
Figure 2.1: **(a)** Sandwich construction of a conjugated polymer electrochemical memristor (cPECM). **(b)** Structure of self-doped poly(3,4-ethylenedioxythiophene) (S-PEDOT) and polyethyleneimine (PEI). **(c)** Circuit representation for programming and reading the conductance state of cPECM. **(d)** Schematic of a gravure roll-to-roll printing configuration.

ethylenedioxythiophene) (PEDOT) is employed in the construction of the device, namely S-PEDOT (cf. **Figure 2.1b**). This conjugated polymer is synthesized from the monomer sodium 4-[(2,3-dihydrothieno[3,4-b][1,4]dioxin-2-yl)methoxy]butane-2-sulfonate (S-EDOT), a novel EDOT derivative bearing a sodium alkylsulfonate side chain [143]. The presynaptic layer is composed of S-PEDOT, while the postsynaptic layer is composed of S-PEDOT and a vapor-deposited PEI. PEI is an alkyl chain with primary, secondary, and tertiary amines and only a portion of the amines of PEI are typically protonated. This results in PEI having a high proton buffering capacity. PEDOT has been indicated to have an inherent nature to oxidize with ambient oxygen [12, 144] and its oxidation within a device will impede on state retention, cycle stability, and overall device performance for long-term applications [123, 145]. The use of PEI with PEDOT has been shown to stabilize the PEDOT, with PEI acting as a reductant by donating electrons to the oxidized PEDOT [146]. This process assists in stabilizing the neutral form of S-PEDOT and, with the electron blocking nature of the poly(ethylene glycol) (PEG)/tetrabutylammonium hexafluorophosphate (Bu$_4$NPF$_6$) electrolyte layer, maintain the oxidation state of the postsynaptic layer. With no driving bias applied to the device, the electrolyte prevents any electron recombination reactions by decoupling the electron

transfer between the presynaptic and postsynaptic layers [50].

The circuit implemented for programing synaptic events and reading synaptic weights of the cPECM device is presented in **Figure 2.1c**. The current flowing in the channel between the D and S electrodes (i_{ds}) under a constant DC voltage (V_{ds}) is converted to conductance, which is equated to the synaptic weight of the circuit. To program the device, a potential pulse applied at the G electrode (V_g) alters the conductance of the channel and synaptic weight of the circuit. Positive voltage pulses ($+V_g$) to the G electrode tune the carrier concentration of the S-PEDOT:PEI channel by protonating the PEI by a chain of events that results in a decrease in channel conductivity, while negative voltage pulses ($-V_g$) result in an increase in channel conductivity.

The devices were fabricated through a roll-to-roll (R2R) gravure printing process schematically presented in **Figure 2.1d**. R2R printing refers to a range of manufacturing technologies that involves the continuous processing of a pliant substrate as it traverses between two moving rolls of material. Advances in the R2R manufacturing process have made it the likely candidate for economically producing large format multifunctional systems at scale, such as printed electronics [138, 139]. The S-PEDOT was dissolved in a 2:1 methanol:water mixture and was deposited at a ca. 0.2 m/s rate onto flexible indium tin oxide (ITO)-coated polyethylene terephthalate (PET) sheets using a commercial proofing R2R printer. Prior to printing, the ITO sheets were templated to form the top G electrode and split D and S electrode assemblies. Once printed, PEI was evaporated onto the postsynaptic layer, the PEG/Bu$_4$NPF$_6$ electrolyte was deposited on the postsynaptic layer, and then the two synaptic layers were mated to form the sandwich structure presented in **Figure 2.1a**.

Figure 2.2a presents the multitude of conductive states, or synaptic states, available to the cPECM when programmed with voltage pulses. In this curve, a single programming step is a square-wave pulse with a ±1000 mV magnitude of 500 ms duration follow by a 500 ms 0 mV period which is applied to the G electrode (V_g). Each full cycle consists of 500 steps of the +1000 mV pulse followed by 500 steps of a -1000 mV pulse. During the programming cycles, a current read across the channel is made every 66 ms from a potential of -100 mV (V_{ds}) applied across the D and S electrodes. The channel conductivity (σ) between 30×10^3 to 100×10^3 read measurements is presented in **Figure 2.2a** to demonstrate the reproducibility of the device, where the total differential in conductivity from peak maximum to minimum is ca. 68 μS. The changes in conductance between successive programming steps is relatively linear for the first few hundred pulses, but as the S-PEDOT approaches a "fully" oxidized or reduced state, the system becomes saturated and
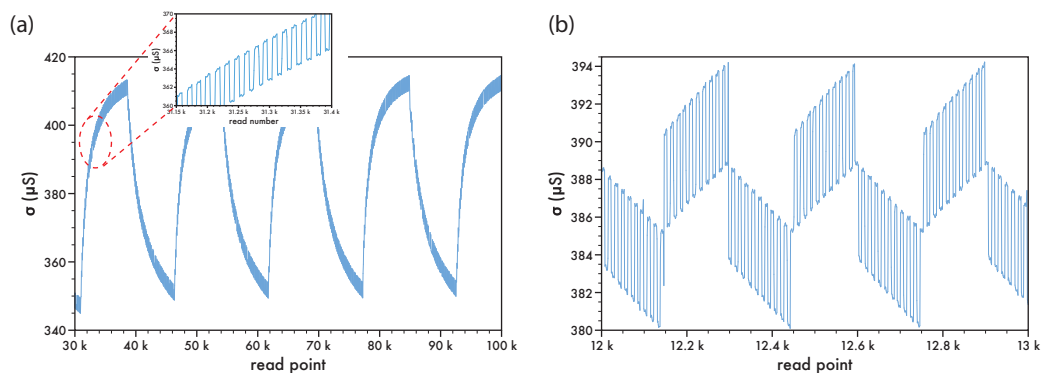
Figure 2.2: **(a)** Voltage-driven conductance tuning of S-PEDOT electrochemical memristor depicting 500 distinct states per potentiated or depressed cycle. The gate electrode is programmed with a 500 ms voltage pulse of ± 1000 mV (V_g) while monitoring the drain current i_{ds} with a channel voltage -100 mV (V_{ds}). **(b)** Current-driven conductance tuning of electrochemical memristor depicting 10 potentiated and depressed conductivity states per cycle.

the changes in conductance begin to diminish between successive impulses. As indicated earlier, a positive potential during a programming operation results in the movement of a cation (proton) from the presynaptic layer through the electrolyte layer into the postsynaptic layer where it protonates the PEI. For charge neutrality, electrons flow from the external circuit into the postsynaptic layer reducing the S-PEDOT, resulting in a decrease in σ of the channel and an increase in the observed current flow. During the "read" operation, a constant value of σ was observed at the new conductivity level and was stable for a 24 minute observation period with a 0.0175% (0.040 μS) decrease over this time. This process was reversible, where a subsequent train of opposite voltage pulses returns the device to its initial conductance. Similarly, **Figure 2.2b** presents the tuning of the channel through 10 potentiated/depressed states with the substitution of V_g (cf. **Figure 2.1c**) with a current source and employing a square-wave current pulse of ± 1 μA for 500 ms. In this case, current flowing out of the G electrode results in cations flowing from the postsynaptic layer to the presynaptic layer and increases the conductivity of the channel. From **Figure 2.2b**, the linear change in conductance between each successive current pulse is clearly discernible.

The specific conductivity state of the channel can be tuned by varying the duration and/or amplitude of the applied square-wave voltage (or current) pulse since the oxidation state of the S-PEDOT in the postsynaptic layer is a function of the total charge that is transferred in or out of this layer. Remembering that a positive voltage pulse to the G electrode resulted in a decrease in the channel conductivity and that positive and negative voltage pulses of equal magnitude result in

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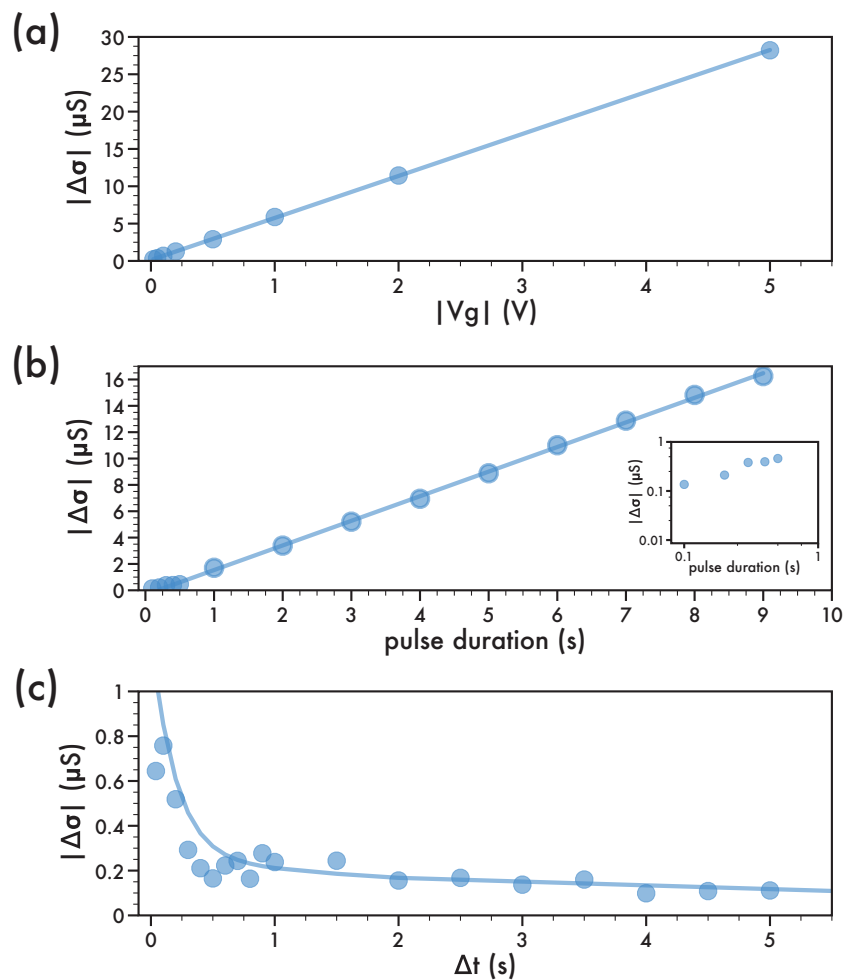
Figure 2.3: The change in channel conductance of the cPECM as a function of **(a)** pulse amplitude with a 500 ms duration and **(b)** pulse duration with a +2500 mV amplitude (inset presents shorter time regime). **(c)** Paired-pulse facilitation (PPF) of the cPECM with a pair of square-wave V_g pulses (+1000 mV, 500 ms) separated by a time interval (Δt).

the same absolute conductance change, **Figure 2.3a,b** presents the change in conductivity of the channel with increases in voltage pulse amplitude and duration, respectively. A linear trend in the increase of the absolute value of $\Delta\sigma$ is evident by increasing pulse amplitude as well as duration. For example, with a +2500 mV pulse of 100 ms duration, a 0.136 μS resolution in conductivity change is realized. A pulse magnitude of +2500 mV insured charge flow for short pulse durations. The predictable increase is a direct result of the linear change in the number of cations that depart the presynaptic electrode with a positive voltage pulse. A similar trend is seen when voltage pulses with a negative amplitude are employed. The linearity in conductivity changes of the cPECM to differing

parameters of the voltage pulses to the gate electrode affords a simplicity in devising sophisticated decision responses which will be discussed later concerning Boolean algebra.

The mechanism of the cPECM to read, write, and erase is akin to that of the human nervous system. With the gate and channel electrodes mimicking that of the pre- and post-synapses, the synaptic weight is modulated based on the current flow through the doped conjugated polymer channel. Paired-pulse facilitation (PPF), a biological mechanism in the short-term plasticity regime, was used to demonstrate the neuromorphic functionality of the S-PEDOT cPECM. PPF is a phenomena that measures the response characteristics between two biological stimuli (in this case, electrical pulses) based on the timescale between the pulses being fired (Δt) and is presented in **Figure 2.3c**. A pair of square-wave V_g pulses (+1000 mV, 500 ms) separated in time from 40 ms to 5000 ms (Δt) were applied to the device while monitoring the channel current i_{ds} at a constant V_{ds} (-100 mV). The absolute value of the difference in the observed conductivities ($|\Delta\sigma|=|\sigma_2 - \sigma_1|$) for a set of paired pulses was employed in evaluating the PPF relationship.

The PPF response was modeled with a dual exponential of the form:

$$PPF = C_1 \exp(t/\tau_1) + C_2 \exp(t/\tau_2)$$

and gave values for τ_1 and τ_2 of 13.34 ms and 518.0 ms, respectively, with $C_1 = 0.6536$ and $C_2 = 0.2208$. The S-PEDOT cPECM displays a rapid phase relaxation of $\tau_1 = 13.34$ ms and a slow phase relaxation of $\tau_2 = 518.0$ ms, resulting in a minimal potentiation difference for pulse separations greater than 600 ms (cf. **Figure 2.3c**). These time characteristics are comparable to that of biological synapses[147]. In terms of other cPECM devices, it is speculated for pulse intervals less than the slow phase relaxation time, protons can accumulate at the electrolyte/channel interface before the second stimuli is applied which does not allow for proper electronic state decoupling. At time scales greater than the slow phase relaxation time, these mobile protons can relax and decouple prior to the second stimuli, resulting in a smaller change in postsynaptic current between paired-pulses[148].

Basic capabilities required in a memristor where neuromorphic properties are desired include the ability to perform elementary algebra. The simplest operations in this field of mathematics include addition, subtraction, multiplication, and division. With the cPECM device, positive voltage pulses increase the channel current and represent addition while negative pulses decrease the channel current and represent subtraction. **Figure 2.4** presents a typical addition and subtraction operation
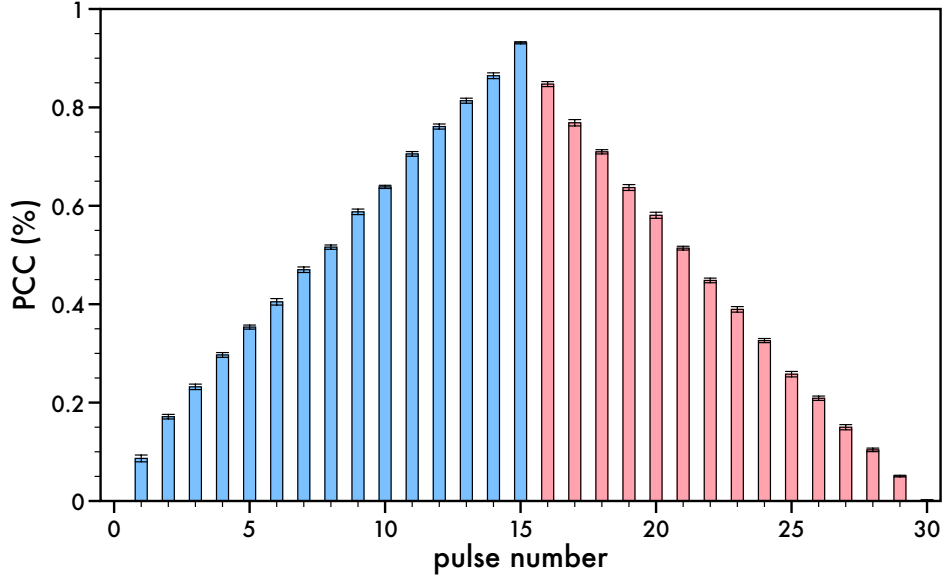
Figure 2.4: Addition and subtraction: **A - B = 0** [+15 + -15= 0]. Error bars represent standard deviation of 8 unique calculation cycles.

in the form of **A** - **B** = 0 [+15 + -15 = 0]. **A** has the numerical value of "+15" and is represented by 15 square-wave +1000 mV, 500 ms pulses applied to the G electrode. The conductivity of the channel increases for each pulse and the current change from the baseline value at the onset of the operation is defined as the percent current change (PCC), where PCC = $(i - i_\circ) \cdot (100/i_\circ)$. Each square-wave pulse of the form of +1000 mV and 500 ms duration raises the PCC on average by 0.048%, with 15 pulses, i.e. the number "+15", being represented by a PCC value of 0.720%. Applying a square-wave pulse of the form of -1000 mV and 500 ms duration results in a decrease of the PCC on average of 0.048%. The addition of the number "-15" in the form of 15 -1000 mV pulses to the PCC value of 0.720% ("+15") results in a final PCC value of 0.0005%, effectively the number "0". Within our laboratory-bench devices, the variability in PCC values for the representation of "15" from device to device was typically less than $|\Delta\text{PCC}| = 0.01\%$, though this could be reduced in a true manufacturing environment. In **Figure 2.4**, the standard deviation for 8 unique arithmetic runs are presented as error bars at each calculation step.

Multiplication is often referred to as repeated addition with equal groupings. **Figure 2.5a,b** presents multiplication through the addition of multiple sets of pulses where **A** x **B** = **B** x **A** = **C** [3 x 5 = 5 x 3 = 15]. In this case, "3 x 5" implies 3 sets of 5 square-wave pulses (+1000 mV,
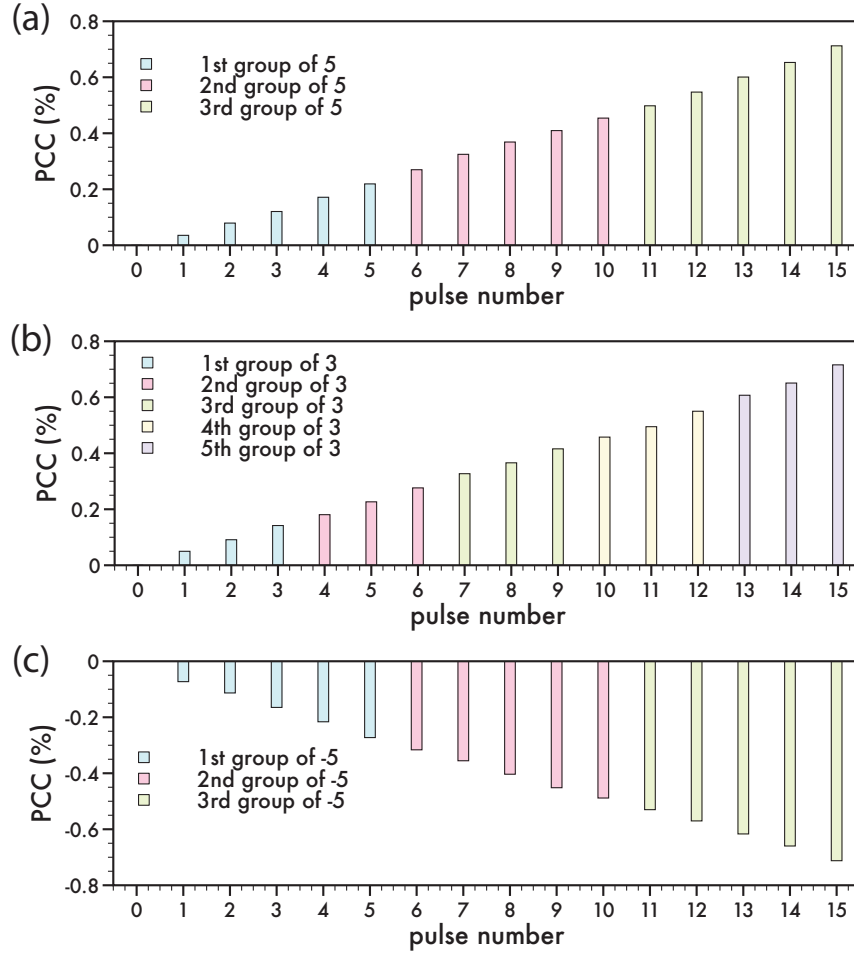
Figure 2.5: Multiplication as a repeated addition with equal groupings: $\mathbf{A} \times \mathbf{B} = \mathbf{B} \times \mathbf{A} = \mathbf{C}$ [3 x 5 = 5 x 3 = 15]. (a) 3 x 5, (b) 5 x 3, and (c) 3 x -5.

500 ms) with a 2000 ms delay between each multiplication set. Upon pulsing the device, "3 x 5" resulted in a PCC of ca. 0.712% while performing "5 x 3" resulted in the same PCC value of 0.712%, demonstrating the associative property in multiplication. In addition, **Figure 2.5c** presents $\mathbf{A} \times \mathbf{B}$ where $\mathbf{A} = 3$ and $\mathbf{B} = -5$ and "3 x -5" is represented by 3 sets of 5 negative amplitude square-wave pulses (-1000 mV, 500 ms), giving a final PCC value of -0.712%, or its numerical value of "-15".

Division, i.e. $\mathbf{A} \div \mathbf{B} = \mathbf{C}$, can be demonstrated through a "division as repeated subtraction method" [149, 150] and is presented for $\mathbf{A} = 15$ and $\mathbf{B} = 6$ in **Figure 2.6**. Initially, the value of the integer quotient n_1 is found that results in the remainder (r_1) to be $r_1 < \mathbf{B}$ for $r_1 = \mathbf{A} - n_1 \cdot \mathbf{B}$. In the present case, $n_1 = 2$ satisfies this criteria with 15 - 2 · 6 = 3. The number 15 is initially represented by a PCC value of 0.712%, then 2 groups of 6 negative amplitude pulses (-1000 mV,

500 ms) are applied to the G electrode of the cPECM device. This lowers the PCC value to 0.149%, the numerical equivalent of 3. To find the remainder in a decimal format, the remainder (r_1) is then replaced by $r_2 = r_1 + r_1 \cdot 9 = 3 + 27 = 30$. To achieve this, 3 groups of 9 positive amplitude pulses (+1000 mV, 500 ms) are applied to the G electrode of the cPECM device to raise the PCC to 1.410%, or the numerical equivalent of 30. The successive subtractions with the integer quotient (n_2) in the decimals place are performed for $r_3 = r_2 - n_2 \cdot \mathbf{B}$ until $r_3 = 0$. If $r_3 \neq 0$, repeat $r_2 = r_1 + r_1 \cdot 9$ and $r_3 = r_2 - n_2 \cdot \mathbf{B}$ until $r_3 = 0$. In the present case, $n_2 = 5$ satisfies this criteria with 30 - 5 · 6 = 0 and the division is complete. To achieve this, 5 groups of 6 negative amplitude pulses (-1000 mV, 500 ms) are applied to the G electrode of the cPECM device to lower the PCC to 0.00003%, or the numerical equivalent of 0. The final quotient (Q) is the sum of the integer quotients $Q = n_1 + 0.n_2 = 2 + 0.5 = 2.5$.
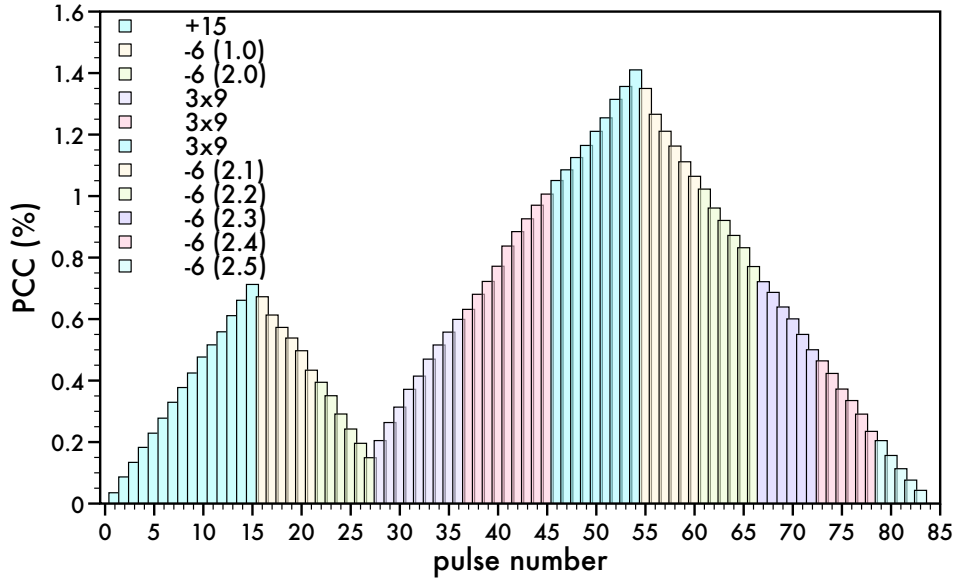
Figure 2.6: Division as repeated subtraction method: $\mathbf{A} \div \mathbf{B} = \mathbf{C}$ [15 ÷ 6 = 2.5]

Boolean algebra includes those logic operations that employ Boolean values which take on the values of either TRUE or FALSE, often represented by a *1* and *0*, respectively. Boolean algebra is a vital capability for any memristor that might be used in neuromorphic computing and can be demonstrated for the S-PEDOT-based cPECM with the logic operations of AND, OR, NOR, and NAND, where **Table 2.1** presents their truth tables.

With a cPECM device, the square-wave voltage pulses sequentially applied to the G elec-

			truth table			
AND	input	A	F	T	F	T
		B	F	F	T	T
	output		F	F	F	T
OR	input	A	F	T	F	T
		B	F	F	T	T
	output		F	T	T	T
NAND	input	A	F	T	F	T
		B	F	F	T	T
	output		T	T	T	F
NOR	input	A	F	T	F	T
		B	F	F	T	T
	output		T	F	F	F

Table 2.1:   Truth table for AND, OR, NAND, and NOR logic gates.

gate	logic	parameters	
		voltage (mV)	duration (ms)
AND	FALSE	-500	500
	TRUE	1000	500
OR	FALSE	-500	500
	TRUE	2000	500
NAND	FALSE	500	500
	TRUE	-1000	500
NOR	FALSE	500	500
	TRUE	-2000	500

Table 2.2:   Definition of voltage inputs corresponding to each logic gate *TRUE* and *FALSE* statement.

trode have specific amplitudes and durations in order to represent a TRUE or FALSE value within a specific logic gate and are presented in **Table 2.2**. For example, with the AND gate, a FALSE value is passed to the memristor with a square-wave pulse of -500 mV and 500 ms duration, while a TRUE value is passed as a pulse of +1000 mV with the same duration.

Figure 2.7a presents the AND truth table generated by the cPECM device. The initial state of current in the channel is measured giving a baseline absolute value $|i_{ds,\circ}| = 71.188$ μA, which is employed in defining future logical outputs of the device. The output logic is configured such that for $|i_{ds}| > 71.188$ μA results in a TRUE output, otherwise, for $|i_{ds}| < 71.188$ μA the output is FALSE. In the cPECM device, the channel conductivity was evaluated by monitoring the current flow in the channel to a -100 mV potential across the D and S electrodes. Therefore, a positive voltage pulse to the G electrode resulted in an increase in the channel current and a decrease in the channel conductivity. Following each set of logical inputs, a "reset" sequence occurs where the
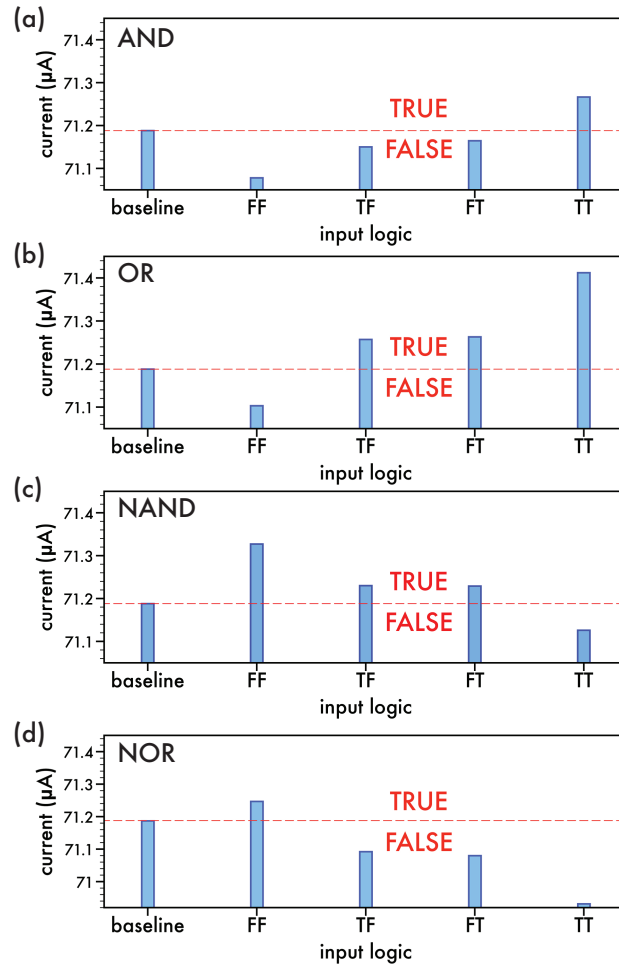
Figure 2.7: Boolean algebra: Logic gates **(a)** AND, **(b)** OR, **(c)** NAND, and **(d)** NOR.

previous input pulse pattern is driven at a reverse bias in order return the device back to the state prior to programming. For example, a A = TRUE and B = FALSE logic computation using the AND gate was initiated by passing a TRUE to the device with a +1000 mV, 500 ms pulse followed by a FALSE -500 mv, 500 ms pulse. After this sequence of pulses was sent to the G electrode, a current read of the channel was made that gave $|i_{ds}| = 71.15$ μA, an absolute value less than the baseline current and thus the computation resulted in a FALSE value. As **Figure 2.7a** indicates, the cPECM device exhibits logic computations for all the combinations of the A and B inputs that are consistent with an AND gate. The associative property to differing input values previously discussed is evident by the similarity of current outputs for input values that are either FALSE *then* TRUE or TRUE *then* FALSE.

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The predictable and linear response to the sign, amplitude, and duration of the input voltage pulses (cf. **Figure 2.3**) allowed for the relatively straightforward determination of the sequence of pulses that must be applied to the cPECM to create a number of logic gates. The basic digital logic gates of AND and OR have TRUE outcomes for positive voltage impulses and FALSE outcomes for negative voltage impulses, while their negated equivalents of NAND and NOR have an opposite sign multiplied to their input pulses. The characteristics of the square-wave voltage pulses required to represent a TRUE or FALSE value within a specific logic gate are presented in **Table 2.2**, while the logical computations for the OR, NAND, and NOR gate are presented in **Figures 2.7b,c,d**, respectively.

Important considerations in the design of an artificial synapse are the voltage pulse magnitude/duration and energy requirements to trigger a synaptic event. Biological neuromorphic systems achieve energy consumption per operation that is an extremely small amount of energy, on the order of 1-10 fJ per synaptic event. The cPECM device utilized in this study employs a large 12×20 mm active area with a 100 μm spacing between the D and S electrodes. This model system could be quickly optimized to reduce device size and power requirements. For example, the consecutive changes in the resistance (synaptic events) were accomplished by an unoptimized ± 500 mV pulse of 500 ms which has an energy requirement of ca. 42 pJ/mm^2 (E $= V \times i \times t = 500$ mV $\times$ 40 nA $\times$ 500 ms), though synaptic events could be programed by lowering the voltage magnitude and impulse duration to ± 50 mV pulse and 100 ms to give an energy requirement of ca. 0.31 pJ/mm^2, an almost 100% drop in energy requirements. Recent advances in R2R printing have allowed for the reliable printing of 20 μm structures with a minimum internal linewidth of 3 μm at print speeds 0.2 m/s [142]. Employing these advanced printing techniques to our cPECM device could allow for energy requirements on the order of 0.1 fJ for a 20 μm device, a value similar to recently presented three-terminal artificial synapses [50, 151].

2.3 Conclusions

In summary, a fully water-soluble, self-doped PEDOT was synthesized and fabricated into electrochemical neuromorphic organic devices that demonstrates high conductivity linearity over 500 distinct states per potentiated or depressed cycle, low-energy consumption (0.31 pJ/mm^2), and ease of scalability due to low-cost materials and fabrication techniques. Roll-to-roll (R2R) printing

fabrication allowed for the ease of mass production of such devices that function as information storage and processing units with neuromorphic capabilities. This is a demonstration of the first steps towards the implementation of this device as an artificial neural network (ANN).

2.4 Experimental

2.4.1 Materials

All reagents were purchased from Alfa Aesar, TCI America, and used without further purification.

2.4.2 Synthesis of Monomer S-EDOT

Sodium 4-((2,3-dihydrothieno [3,4-b][1,4]dioxin-2-yl)methoxy)butane-2-sulfonate has been previously prepared in literature[143].

2.4.3 Synthesis of Polymer S-PEDOT

S-EDOT (0.2 g, 0.61 mmol) was dissolved in deionized (DI) water (4 mL) then iron(III) chloride hexahydrate (0.1 g, 0.37 mmol) was added into solution. The obtained solution was stirred and degassed with nitrogen before an aqueous solution of sodium persulfate (0.33 g, 1.21 mmol in 4 mL of water) was added dropwise into the main solution under nitrogen. This mixture was stirred for 20 hrs at room temperature. After, the solution was diluted with water (4 mL) and treated with Amberlyst 15 cation exchange resin following by Diaion (WA30) anion exchange resin. The obtained solution was evaporated under vacuum to give a pure polymer. Yield 0.128 g (69%), dark blue paste.

2.4.4 Device Fabrication

Devices were fabricated on substrates of indium tin oxide (ITO)-coated polyethylene terephthalate (PET) (Aldrich Chemistry) with resistance of 60 Ω/sq. Gate electrodes were templated using polyimide tape to mask the desired ITO electrode (12 mm wide). An acid-etch process is used to remove the unwanted ITO with hydrochloric acid (36%, VWR, CAS Number: 7647-01-0) and zinc powder (Fischer Scientific, CAS Number: 7440-66-6). The bottom electrodes are templated using

HPR 504 photoresist (Arch Chemicals, Inc.,) spin coated at 4000 RPM for 40 s using a Specialty Coating Systems Spincoat G3P-8 and annealed at 105 °C for 15 min on a hot plate prior to exposure of UV light using a Kepro UV model BTX-200A for 5 min with the appropriate lithography template. After photo-templating the pattern, the slides were developed with OPD 4262 (Arch Chemicals, Inc., CAS Number: 75-59-2) for 20 s before being rinsed with DI water. The films were dried at 105 °C for 15 min and then at 120 °C for 15 min. Once dried, the same acid-etch process as stated above was used to remove the unwanted ITO. The slides were then submerged in Microstripper 2001 (Arch Chemicals, Inc., CAS Number: 872-50-4) to remove the photo-etched HPR 504 film to expose the desired ITO pattern. In this work, the channel length between drain and source electrode was 100 μm unless otherwise stated. Prior to any coating, all substrates were washed with DI water, acetone (Fischer) and isopropyl alcohol (Fischer) in a sonicator for 15 min each and then plasma cleaned in a Harrick PDC-32G plasma cleaner on high for 15 min.

The S-PEDOT polymer was coated from a 2:1 methanol:water solution at a concentration of 5 mg/mL. Printing of devices was preformed on PET substrates with a RK K Printing Proofer attached with a gravure head at a speed of ca. 0.2 m/s. After coating, the bottom electrode was de-doped with an ionic conducting material, polyethylenimine (PEI) ($M_W = 800$, Sigma Aldrich, CAS Number: 25987-06-8), via vapor-doping at 250 °C for 8 min in a sealed chamber at atmospheric pressure. Using a KLA Tencor Step Height Profilometer, film thickness of the printed films for S-PEDOT and S-PEDOT:PEI were measured to be ca. 130 nm and 225 nm, respectively. To prepare the polymeric electrolyte gel, first a solution of 1.5 g tetrabutylammonium hexafluorophosphate (Bu_4NPF_6) (Sigma Aldrich, CAS Number: 3109-63-5) was added to 20 mL of propylene carbonate (Acros, CAS Number: 108-32-7) and dissolved for 12 hrs. Then 500 μL of polyethylene glycol methacrylate (PEGMA) ($M_n = 360$, Aldrich, CAS Number: 25736-86-1), 50 μL of polyethylene glycol dimethacrylate (PEGDMA) ($M_n = 550$, Aldrich, CAS Number: 25852-47-5), and 5 μL of 2,2-diethoxyacetophenone (DEAP) (Fluka, CAS Number: 6175-45-7) were added to 1 mL solution of Bu_4NPF_6 in propylene carbonate and mixed. The electrolyte solution was vortexed prior to use. The top and the bottom substrates were sandwiched with a 125 μm thick parafilm spacer placed between the two PET sheets. The electrolyte solution was injected into the 12 × 20 mm space and photo-polymerized under a UV-light for 8 min per side in 2 min intervals using a ELC-500 Light Exposure System.

2.4.5 Device Characterization

Electrical characterization of the devices was done using a HP4145A Semiconductor Analyzer to apply the voltage- or current-pulse train to the gate electrode. A Keithley 2440 5a Sourcemeter was used to monitor the current across the drain and source channel electrodes. The HP4145A Semiconductor Analyzer was interpreted with custom HTBasic code and the Keithley 2440 5a Sourcemeter used LabView.

Chapter 3

Non-Conformal Electrochemical Memristor through Vapor Phase Polymerization of Polypyrrole

3.1 Introduction

Memristors were initially theorized in 1971 as a fundamental passive 2-terminal electronic device that functions as a non-volatile tunable resistor[1]. Recent efforts have reported on memristive devices that are based on field-effect transistors (FETs) [152–154] and organic electrochemical transistors (OECTs) [155–157]. These transistors have a 3-terminal device geometry with gate, drain, and source electrodes and one or two active layers separated by a dielectric (FET) or electrolyte (OECT). The working principle of an OECT is that with voltage applied to the gate, the drain and source (channel) active layer is electrochemically (de)doped to modulate the resistance (or conductivity) state [158–160]. By slightly modifying the OECT design approach, many neuromorphic-capable OECTs have been reported[50, 123, 161]. Analogously to biological nervous systems where neurons and synapses are the building blocks for computation and memory, memristive devices can perform similar complex operations with low power consumption [17].

Biologically inspired synaptic architectures function based on synaptic weights that are modulated by either the number or frequency of incoming stimuli [4]. Similar to biological synapses, mem-

ristors have been shown to share a common role in which they exhibit reliable and repeatable analog tuning properties which include non-abrupt switchable transitions, continuously programmable resistance states, and predictable and well established responses[4, 15, 119, 120]. Biological neurons and synapses function as an integrated system to perform learning and memory through a highly energy-efficient mechanism of modulating their synaptic weights in response to any and all biological inputs. This drives forward the need to create new low-energy neuromorphic-capable devices where operation is < 10 fJ per stimuli [4]. Many organic memristor systems have been reported where key parameters, such as device reproducibility, state stability, scalability, power consumption and speed, often are lacking compared to many inorganic-based systems[119]. For this reason, redox-based systems are being studied as they satisfy many of these base requirements for neuromorphic computation [162].

The ability to deposit semiconducting films is crucial where the reliability of thin, even coatings are necessary. Most commonly used film deposition procedures involve solution-processable spin coating, dip coating, or various printing techniques, however, conjugated polymers (CPs) are typically difficult to suspend in solution making uniform films difficult to form [96]. To this end, polymer derivatives have been established with either varying side chain groupings [143, 163–165] or doping of various polyelectrolyte materials [166–169] playing the role of a solubilizer while impacting the performance of the material's electronic properties or adding more complexity to processing parameters. To resolve these issues, synthesis through a chemical oxidative $in-situ$ polymerization technique has been established for various CPs [96, 97, 144, 170, 171] referred to as vapor phase polymerization (VPP). This technique is often achieved via coating the substrate with an oxidant by solvent-processed spin coating and subsequently exposing the oxidant-coated substrate to monomer vapor. The freedom of design leads to the ability to overcoat more complicated surface geometries and architectures where other techniques do not succeed. Ferric p-toluenesulfonate (FeToS) is a well-suited oxidant used in previous efforts for VPP CPs [172] where, after deposition and cleaning, trace amounts of sulfonate are present and essential for the conducting nature for these CPs [96]. By controlling the crystallite formation of FeToS post-spin-coating, a versatile route for fabricating both smooth and highly conductive films is achievable [96].

Through the process of VPP, the vaporized monomer is delivered onto the desired substrate to chemically form a smooth and uniform polymer film, functionalizing the materials surface [96, 173]. The ease of this fabrication process, along with the capability to scale up, leads to the ability to

form complex devices over arbitrary substrates with conformal and non-conformal substrates without running into common surface wetting or surface tension issues from solution-based processing [173–175]. VPP films are capable of widespread application across many facets where the need for highly mechanically rigid films with uniform smooth coatings are required. A recent report details the use of an electronic-capable conformal substrate based on a nanocellulose composite [176]. The nanocellulose composite provides a robust, transferable template that can adhere to most biological surfaces for use as a flexible display, environmental tags, micro-aeronautics, or biological sensors. These are significant steps leading toward the integration of electronics into everyday items to transform common appliances and utilities into smarter technologies.

In recent literature, a 3-terminal electrochemical neuromorphic organic device reports synaptic-like behavior via a counter-redox reaction across their architecture [50]. By varying the (de)doping levels of each layer, various redox-active species can be implemented into these 3-terminal synaptic-like memristive devices, which will exhibit neuromorphic computation attributes. Another recent report presents a 3-terminal conjugated polymeric-based electrochemical memristor (cPECM) where, utilizing a PEDOT derivative that is self-doped and water-soluble, both Boolean algebra and elementary algebra were implemented to demonstrate the device's potential as a candidate for neuromorphic computers [57]. To that end, a 3-terminal conjugated polymeric organic synaptic memristor is presented in this effort that utilizes a VPP deposition of polypyrrole (PPy) over conformal and non-conformal substrates. The PPy-based synaptic memristor is capable of achieving highly distinct and symmetric linear conductivity states, which can be tailored into neuromorphic and advanced operational techniques.

3.2 Results and Discussion

3.2.1 Film characterization

Figure 3.1a represents the current embodiment of the polypyrrole (PPy)-based synaptic memristor and the electronic circuit to implement it. This 3-terminal device contains two active layers; both deposited via a vapor phase polymerization (VPP) technique for PPy. The top synaptic electrode is separated from the bottom bifurcated synaptic electrode via a polymeric gel electrolyte. The electrolyte used is tetrabutylammonium hexafluorophosphate (Bu_4NPF_6) encapsulated in a PEG-based gel network. The electrolyte layer acts as an energy barrier to decouple electron/hole
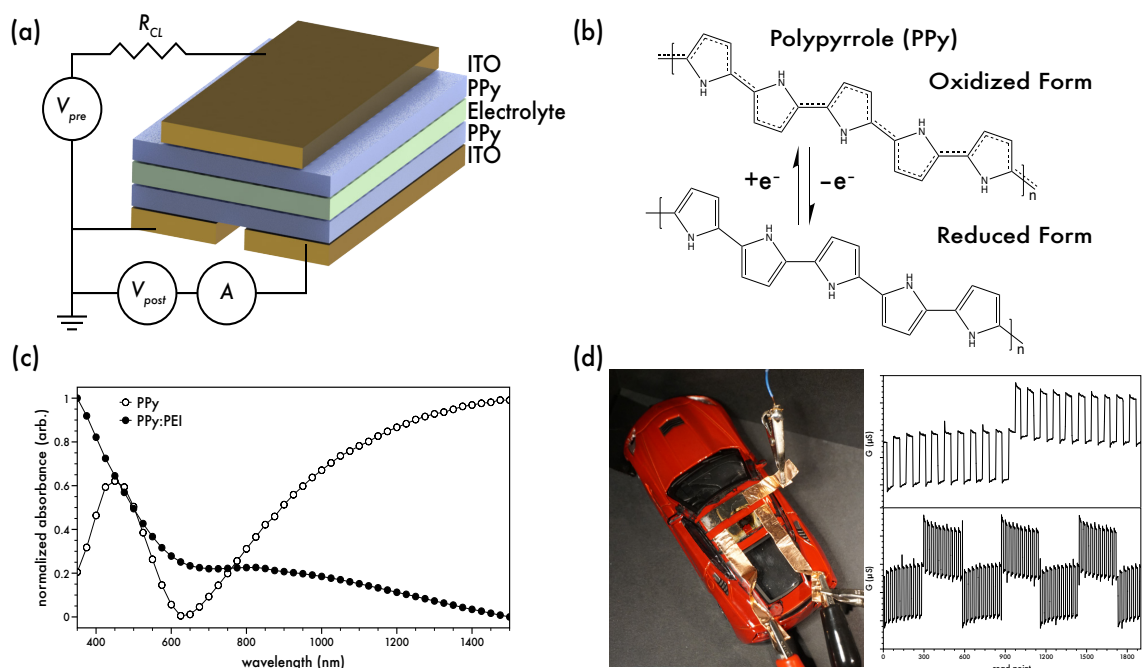
Figure 3.1: **(a)** 3D schematic for the PPy-based 3-terminal synaptic device and the equivalent circuit. **(b)** Chemical structure of polypyrrole in its oxidized and reduced form. **(c)** Optical photo-physical properties of an oxidized (○) and reduced (●) PPy thin-film. **(d)** Optical image of a toy car turned into a device with 3 aluminum electrodes, vapor polymerized PPy, and over-coated with a polymeric gel electrolyte. Copper tape is used to connect alligator clips for testing to the 3 terminals. Data presented on the top demonstrates the conductivity of the toy-based device for a single cycle of 10 +V_{pre} pulses followed by 10 -V_{pre} pulses programmed to the top synaptic electrode. Conductivity is measured across the bottom synaptic electrode with a -0.1 V potential. Data presented on the bottom demonstrates the symmetry of the device over repeated cycle testing.

migration and recombination from the top synaptic input and the bottom synaptic terminal. In regards to biological synapses, each conducting layer can be considered a synapse (pre- and post-synaptic terminals) where the gel electrolyte is the synaptic cleft. By modulating the potential redox states of the post-synaptic terminal, a linear, non-volatile memristor can be achieved. PPy films are synthesized using a VPP technique where the substrate is first coated with an oxidant material, specifically ferric p-toluenesulfonate (FeToS) spun cast in a methanol (MeOH) solution, and soft-baked to remove some residual solvent. The coated films are almost immediately loaded into a vacuum oven such that the films face down with a supply of pyrrole (Py) monomer below them. Once proper vacuum and temperature are reached, Py vaporizes and deposits over the FeToS film, where the polymerization reaction occurs to form PPy as a green-purple film. The residual oxidant is rinsed off with pure methanol post-polymerization prior to any testing or use. **Figure**

3.1b presents the fully oxidized and fully reduced chemical structure of PPy where **Figure 3.1c** displays the optical properties of these respective thin films. For the oxidized PPy film, there is a maximum absorption at 453 nm, which is characteristic of the PPy polymer [177]. The broadband absorption tail past ca. 600 nm is an attribute of a highly oxidized species [73]. By exposing a PPy film to polyethyleneimine (PEI) vapor, a commonly used reductant [178], the film is chemically dedoped and the broadband absorption past ca. 600 nm is diminished. The shallow absorption past ca. 600 nm is a characteristic of a reduced conjugated material [73].

In regards to polymerization over non-conformal shapes and substrates, **Figure 3.1d** demonstrates the use of this polymerization technique on a toy car turned into a memristive synaptic-capable device. While the density of chips on print circuit boards (PCBs) has drastically increased over the past few decades with the use of surface-mounted devices (SMDs) and well-established fabrication methods [179], PCBs suffer from their rigid substrate and planar design. The demand for the design of non-uniform and non-conformal devices affords a path forward to implement smart technology into common-place objects in the world around us. The toy car was templated with polyimide tape and aluminum (Al) electrodes were deposited via a high vacuum thermal evaporator. Following Al electrode deposition, PPy was vapor phase polymerized after dipping the car's roof in a FeToS/MeOH solution and dried under vacuum for 5 minutes prior to VPP. Following all film depositions, the polyimide tape is removed and the PEG-based gel electrolyte is placed on top such that the gel physically connects the top and bottom synaptic electrodes. As a demonstration tool, the toy car was capable of simple potentiation and depression mechanics by applying a constant potential to the bottom synaptic terminals and pulsing the top gate terminal. This effect is analogous to short-term memory in biological systems [180].

3.2.2   Device performance

For device operation, a voltage pulse (V_{pre}) drives electrons/holes across the top synaptic electrode, through the gel electrolyte and into the bottom synaptic electrodes. A small voltage (V_{post}) simultaneously biases the bifurcated bottom synaptic electrode and continuously reads the current state of the device (i_{post}) every ca. 60 msec. For this circuit, a resistor is used in series prior to the top synaptic electrode in order to ensure proper current loading to the device. Monitoring the current load distributed across the device (i_{pre}) (cf. **Figure 3.2a**), a drastic decrease of current can be observed by increasing the resistor's value. While this strictly follows Ohm's law, there is an
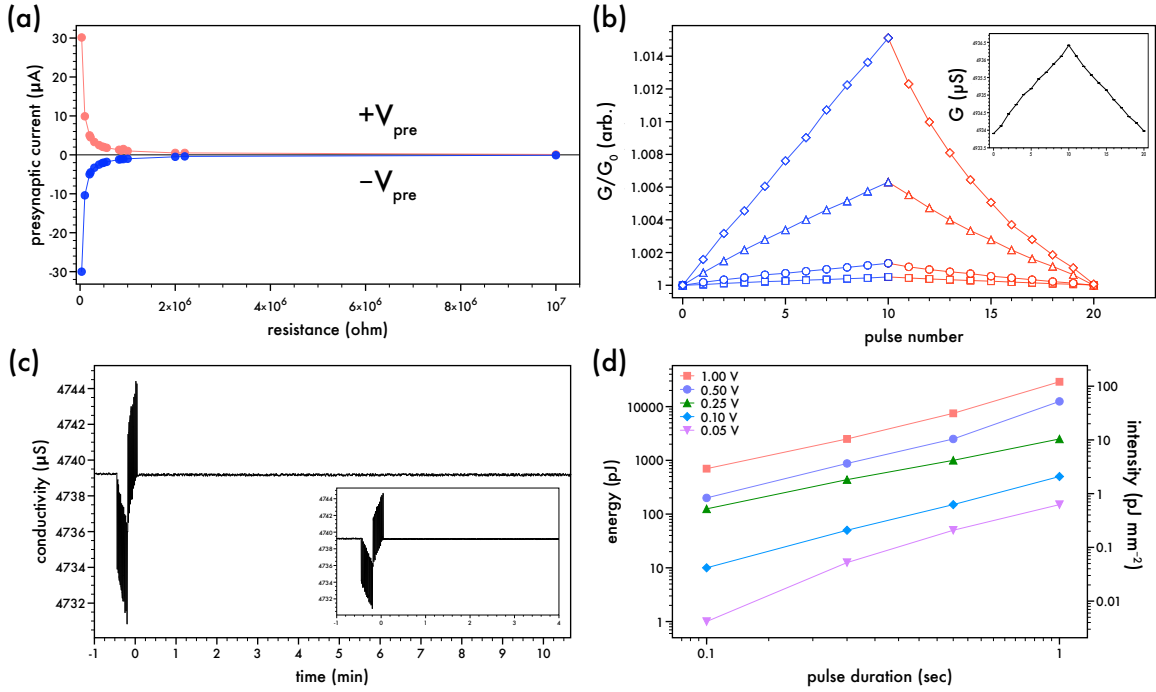
Figure 3.2: **(a)** Presynaptic current with regards to varying the input current limiting resistor (R_{CL}). Red implies positive voltage, $+V_{pre}$, and blue implies negative voltage, -Vpre. R_{CL} values vary from 33 kΩ up to 10M Ω. **(b)** Postsynaptic conductivity response (normalized to $G/G_\circ$) with regards to varying the input resistance, R_{CL}. R_{CL} values tested are 33 kΩ (◇), 100 kΩ (△), 470 kΩ (○), and 1 MΩ (□). Inset shows linear and symmetric response when R_{CL}=1 MΩ. **(c)** Retention properties of the device after a single cycle of 10 pulses/bias monitored for 10 minutes with a constant bias to V_{post}. Inset is a snapshot of the first 4 min after pulsing. **(d)** Power consumption characteristics of the device.

asymmetric deviation to the amount of current loaded to the device at lower resistor values ($R_{CL} <$ 50kΩ). Over a certain threshold ($R_{CL} > 100k$), the current value is symmetric over repeated pulsing and equally weighted for varying bias polarity, whereas lower resistor values provide variability of current, leading to an asymmetric device. The current load at lower resistor values ensues with improper decoupling of the top and bottom synapse, where electrochromic behavior begins to be observed and memristive attributes are diminished. For the case of $R_{CL} = 33$ kΩ, during the application of 10 $+V_{pre}$ pulses ($V_{pre} = 1$ V, $t_{pulse} = 1$ sec, $t_{off} = 1$ sec), i_{pre} is observed where the first pulse drives the device at a load of 31.7 μA. At the tenth pulse, the current drops down and drives the presynaptic electrode with 28.6 μA. In the reverse bias, the first -V_{pre} pulse ($V_{pre} = -1$ V) drives the current at a value of -31.6 μA and the tenth pulse drops down to -28.6 μA. For the case of $R_{CL} = 500$ kΩ, V_{pre}'s application drives i_{pre} at a consistent ± 2 μA based on the polarity of the bias.

By applying 10 -V_{pre} square wave pulses followed by 10 +V_{pre} square waves, the current response of the device (i_{post}) is recorded and normalized to the device's initial conductivity state (G/G$_\circ$). **Figure 3.2b** represents this voltage paradigm while varying resistor values at the input from 33 kΩ to 1 MΩ. As seen in the inset of **Figure 3.2b** with a resistor value of 1 MΩ, the input current is limited and drives the device at a constant ±1 μA. Each voltage pulse (V_{pre}) steps up or down the conductivity state in increments of ca. 0.2452 μS. It is important to note that a +V_{pre} will increase current but decrease conductivity, whereas a -V_{pre} will decrease current but increase conductivity. This is visually represented where blue implies -V_{pre} pulsing and red implies +V_{pre}. After 10 -V_{pre} pulses, the device conductivity steps up from 4933.91 μS to 4936.42 μS, for a ΔG of 2.51 μS or a percent change of 0.051%. The device demonstrates its symmetric nature after the application of 10 +V_{pre} pulses, which returns to a conductivity of 4933.97 μS for a ΔG of ca. 0.06 μS or a percent change of 0.0014% from its initial state. In regards to mathematical functions, the procedure of applying +V_{pre} and -V_{pre} pulses is synonymous with addition and subtraction, respectively. Further elementary algebra operations (multiplication and division) can also be achieved and have been recently reported for a similar device [57].

The device's retention and state stability is demonstrated in **Figure 3.2c**. This pulse data portrays the characteristic signal response exhibited prior to extrapolating each current or conductivity state. Retention is measured after a cycle of 10 +V_{pre} followed by 10 -V_{pre} pulses with a continuous V_{post} application of -0.1 V. Within the first 10 sec after pulsing, there is a 0.002483% drift and 10 min after pulsing, there is a 0.0073% drift. To prove the efficiency of the device, energy (pJ) can be calculated as P = i x V x t. The device's active area is 240 mm^2 and can be used to convert power to intensity or energy consumption (pJ mm^{-2}) where E = P/Active Area. Applying V_{pre} amplitude of ±1 V and a width of 1 sec for the input, the energy consumption for the device is E = (0.029 μA x 1 V x 1 sec) / 240 mm^2 = 120.83 pJ mm^{-2} (cf. **Figure 3.2d**). When analyzing a more optimized input regime (amplitude of 50 mV and 100 msec duration), the energy consumption is reduced to 4.16 fJ mm^{-2}, an almost 100% decrease in energy consumed per pulse state.

To understand the tunability of the organic synaptic memristor, the bottom synaptic electrode can demonstrate near-linear response when varying either the pulse duration and/or the pulse amplitude. This is due to the artifact where the oxidation state of the PPy conjugated polymer is a function of the total charge programmed in or out of this layer. Remembering that +V_{pre} will increase current but decrease conductivity, and vice versa, **Figure 3.3a,b** presents the change in

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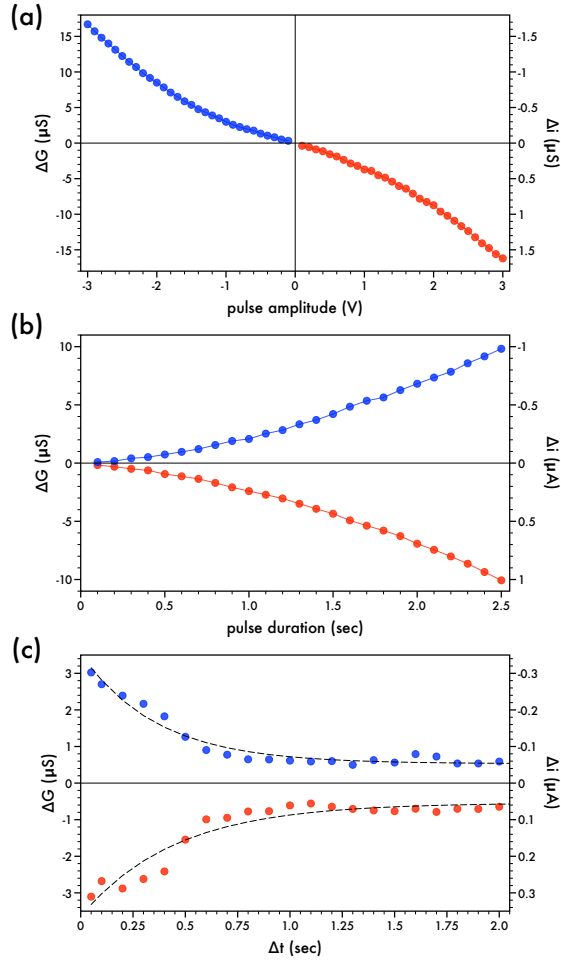
Figure 3.3: **(a)** Device response to voltage pulsing at a constant amplitude, $V_{pre} = \pm 1$ V, while varying the pulse duration. **(b)** Device response to voltage pulsing at a constant duration, $t_{pre} = 1$ sec, while varying the pulse amplitude. **(c)** Paired-pulse facilitation (PPF) (red) and depression (PPD) (blue). Dashed lines represent fitted curves based on data.

conductivity (ΔG) of the bottom synaptic electrode with varying the input V_{pre} pulses amplitude or duration, respectively. A near-linear trend in the increase of ΔG for -V_{pre} pulses is evident with the same trend for the decrease of ΔG occurs for +V_{pre} pulses. This predictable change in conductivity is addressed by the departure of cations from the presynaptic top electrode flowing into the bottom synaptic electrode for the case of +V_{pre} pulses. The near-linear tunability of this device affords a simple design in devising Boolean and elementary algebra operations by modulating the input voltage parameters and will be presented subsequently.

3.2.3 Neuromorphic trends

The mechanism for this 3-terminal device to read, write and forget is similar to a biological nervous system [57]. With the top and bottom synaptic electrodes imitating that of a pre- and post-synapse, the device's response (i_{post}) is modulated based on the current flow through the conjugated polymer covering the bottom synaptic electrode, analogous to modulating synaptic weight. Paired-pulse facilitation (PPF) and paired-pulse depression (PPD) are both short-term memory mechanics that measure(s) the response characteristic based on two stimuli inputs (V_{pre}) and the timescale that separates them (Δt). Remembering that a -V_{pre} will decrease current but increase conductivity and vice versa for +V_{pre}, PPF is achieved with -V_{pre} pulsing while PPD is pulsed with +V_{pre}. The PPF response was modeled to a dual exponential of the form:

$$PPF/PPD = C_1 \exp(t/\tau_1) + C_2 \exp(t/\tau_2)$$

and is observed as a dashed line in figure **Figure 3.3c** In the equation, τ represents the relaxation time constant and C represents a unitless amplitude. A pair of square-waves with an amplitude of ± 1 V and duration of 1 sec are applied to the device while monitoring the bottom synaptic electrodes conductivity (synaptic weight) at a constant V_{post} (-0.1 V). The timescale between the two stimuli (Δt) are separated in increments from 50 msec up to 2 sec. The difference in conductivity states is observed for a set pair of pulses and is calculated by $\Delta G = G_2 - G_1$ where G_1 and G_2 are the conductivity of the state immediately after each voltage pulse stimulus. Following PPF (-V_{pre}), values for τ_1 and τ_2 are 0.000373 msec and 275.923 msec, respectively with $C_1 = 0.5289$ and $C_2 = 3.011$. For PPD (+V_{pre}), values for τ_1 and τ_2 are 0.011623 msec and 223.885 msec, respectively with $C_1 = 3.1051$ and $C_2 = 0.5421$. This suggests there is a rapid phase relaxation for τ_1 of 0.000373 and 0.011623 msec, respectively for PPF and PPD and a slow phase relaxation for τ_2 of 275.923 and 223.885 msec.

3.2.4 Hardware implementation

Elementary algebra or simple mathematical operations are an essential capability requirement for future neuromorphic computers. To that end, the operation of division can be achieved through loops of repeated subtractions to quantify a quotient, C, for the equation A $\div$ B = C presented for the case of A = 13 and B = 4 knowing 13 $\div$ 4 = 3.25 (cf. **Figure 3.4a**). The value of
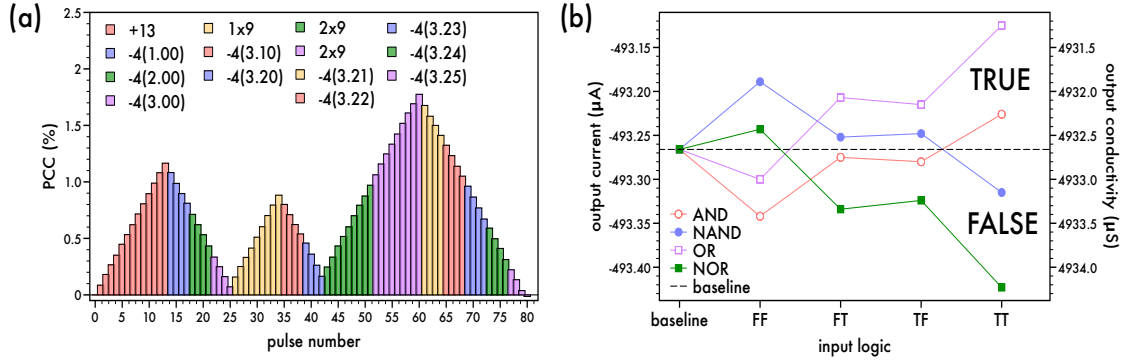
Figure 3.4: **(a)** Division operation based on a subtraction-replace-subtraction method for $13 \div 4 = 3.25$. **(b)** Basic logical operation output for the cases of AND (red), NAND (blue), OR (green) and NOR (lavender). The dashed line represents the baseline current and conductivity state of the device prior to any pulse stimuli and is used to determine logical output.

the integer quotient n_1 is found that results in the remainder (r_1) such that $0 < r_1 < B$ for $r_1 = A$ - n_1 x B. In this context, $n_1 = 3$ satisfies this requirement with $r_1 = 13 - 3 \times 4 = 1$. The number 13 is initially programmed to the device via 13 sequential +1 V, 1 sec square-wave pulses that is then represented by a percent conductivity change (PCC) value of 1.1655%. The PCC is calculated as the difference in conductivity between the initial baseline state (G_0) and the respective programmed voltage-pulsed state (G_n), represented as PCC = (G_n - G_0) x (100 / G_0). It is important to note that, for elementary algebra, multiplication can be thought of as addition/subtraction with equal groups. Simply put, the case of D x E = F implies D groups of E inputs lead to the value F. The first section of the repeated subtraction method then begins with a multiplication step where 3 groups of 4 negative pulses (-1 V, 1 sec) are applied to the top synaptic electrode. This lowers the PCC value to 0.07142%, the equivalent numerical value of 1. To find the remainder in the decimals format, the remainder (r_1) is then replaced by $r_2 = r_1 + r_1 \times 9$ where $r_2 = 1 + 1 \times 9 = 10$. To program this, 1 group of 9 positive pulses (+1 V, 1 sec) are applied to the top synaptic electrode to raise the PCC to 0.88256%, or the equivalent value of 10. The consecutive subtractions with the first decimal quotient (n_2) are performed for $r_3 = r_2 - n_2 \times B$ until the criteria $r_n = 0$ is satisfied. For the present case, $r_3 \neq 0$ as $r_3 = 10 - 2 \times 4 = 2$, therefore another sequence of subtraction-replace-subtraction will take place such that $r_4 = r_3 + r_3 \times 9 = 2 + 2 \times 9 = 20$ followed by $r_5 = r_4 - n_3 \times B = 20 - 5$ x 4 = 0. To achieve this, 2 groups of 4 negative pulses (-1 V, 1 sec) are applied to the top synaptic electrode to lower the PCC to 0.1646%, or the equivalent value of 2. This is followed by the second series of decimal replaced-subtraction by 2 groups of 9 positive pulses (+1 V, 1 sec) to raise the

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PCC to 1.7749%, or the equivalent value of 20. This further proves the linearity and tunability of the device where the PCC for the numerical value of 20 is almost exactly doubled that for the PCC of the value 10. The division is completed by subtracting 5 groups of 4 negative pulses (-1 V, 1 sec) to lower the PCC to -0.01407%, or the equivalent value of 0, within the standard deviation of the device. The final quotient (Q) is the sum of the counted integer quotients to the form of $Q = n_1 + 0.n_2 + 0.0n_3 = 3.25$.

Table 3.1: Logic-based truth table for various single gate logic.

			truth table			
AND	input	A	F	T	F	T
		B	F	F	T	T
	output		F	F	F	T
NAND	input	A	F	T	F	T
		B	F	F	T	T
	output		T	T	T	F
OR	input	A	F	T	F	T
		B	F	F	T	T
	output		F	T	T	T
NOR	input	A	F	T	F	T
		B	F	F	T	T
	output		T	F	F	F

Table 3.2: Voltage pulse parameters for each logical *FALSE* and *TRUE* inputs.

gate	logic	parameters	
		amplitude (V)	duration (sec)
AND	F	-1.0	1.0
	T	+0.5	1.0
NAND	F	+1.0	1.0
	T	-0.5	1.0
OR	F	-0.5	1.0
	T	+2.0	1.0
NOR	F	+0.5	1.0
	T	-2.0	1.0

The demand for future neuromorphic computational devices requires the ability to simultaneously process and store information within a single device. Boolean logic operations demonstrate the capability of data processing and storage in-memory of a single device, where the physical states of the semiconducting polymer films making up the electronic device represent logic states and op-

erations [181, 182]. Boolean logic employs the logical values often represented as either TRUE (T) or FALSE (F). **Table 3.1** presents the operational truth tables for the logic gates of AND, NAND, OR and NOR. For the PPy-based synaptic memristor, tuning the specific amplitudes or durations of the square-wave input pulse represents a TRUE or FALSE value that can lead to the desired output case (cf. **Table 3.2**). For the case of the OR gate, a TRUE value is programmed to the device with a square-wave pulse amplitude of +2 V and 1 sec duration, while a FALSE value is programmed as a pulse amplitude of -0.5 V with the same duration. **Figure 3.4b** presents the output current of the device based on the truth table generated for all logical gate cases. The initial current state of the bottom synaptic electrode is measured as the baseline, which is employed in defining the output logic of the device. Here, a baseline current of $i_{post,\circ}$ = -493.26 μA and is shown as the dashed line in **Figure 3.4b**. The definition of the output logic is configured such that for $i_{post,\circ}$ > -493.26 μA, results in a TRUE output, otherwise $i_{post,\circ}$ < -493.26 μA the output is FALSE. For this device, the bottom synaptic electrode's current is monitored by a -0.1 V constant potential, therefore, a positive voltage pulse to the top synaptic electrode results in an increase in the electrode current and a decrease in the conductivity. Following each logical input sequence (FF, FT, TF, TT), a reset sequence is programmed where the previous input program is driven at a negative bias polarity in order to return the device to its initial baseline state preceding the following logical inputs. The math rule of associative property is evident based on the similarity of the output current states where the input application follows either FALSE then TRUE (FT) or TRUE then FALSE (TF) programs. Similarly, this can be achieved for all simple logic gates AND, NAND, OR and NOR. It is also important to note that NAND and NOR are the negative operations of AND and OR, respectively.

3.3 Conclusions

In summary, a simple vapor phase polymerization of polypyrrole is implemented to fabricate an organic electrochemical-based synaptic memristor. The device demonstrates high conductivity tunability and linearity over a range of distinct states based on input potentiation or depression parameters. The device, at a more optimized voltage scheme, has ultra-low energy consumption of 4.16 fJ mm^{-2}, mimicking that of actual synaptic and neuronal responses. Implementing current state-of-the-art depositing and printing techniques, such a roll-to-roll and lithography, such devices

can be easily mass-produced as well as scaled down in size to further decrease energy consumption. This is a major step towards future neuromorphic computers that exhibit high-end information storage and processing for artificial neural networks.

3.4   Experimental

3.4.1   Materials

All chemical materials were purchased from Fisher Scientific, VWR, Alfa Aesar and Sigma Aldrich and used without further purification or processing. Deionized water (DI-H_2O) exhibited a resistivity value of 10^{18} Ohm^{-1} cm^{-1} from a Nanopure System.

3.4.2   Vapor phase polymerization of polypyrrole

Prior to any coatings, all substrates were cleaned in a sonication bath of DI-H_2O followed by acetone and then isopropyl alcohol for 10 min each, dried under N_2 gas, and then plasma cleaned for 10 min in a Harrick PDC-32G plasma cleaner on high. Vapor phase polymerization (VPP) techniques for various conjugated polymers have been previously reported [83, 96, 171, 174, 175]. Herein, a simple procedure for the polymerization of pyrrole (Py) via VPP is reported. Ferric p-toluenesulfonate hexahydrate (FeToS) was mixed in methanol (MeOH) at a concentration of 250 mg/mL and shaken until fully in solution. The FeToS/MeOH solution is spun cast onto the substrates at a speed of 3000 RPM for 40 sec. Following spin coating, the substrates are soft-baked at 90 °C for 3 min. The films appear as a yellow color and transition to orange after the soft-bake. The oxidant-coated substrates are mounted over a small vial containing 200 μL of Py and loaded inside a model 5851 National Appliance Co. vacuum oven. The oxidant coated slides are exposed for 2 hours under ca. 25 inch of Hg pressure at a temperature ca. 90 °C. After the vaporization of Py liquid to a gas phase, the orange oxidant films transitions to a green-purple film, indicative of the formation of an oxidative species. To remove the oxidant, the slides are fully submerged in a MeOH bath for 3 min before drying with N_2 gas. This process is repeated twice to ensure proper removal of the FeToS oxidant.

3.4.3 Film characterization

All films were characterized via UV-Vis spectroscopy and thin-film profilometry. Removal of the FeToS oxidant from the PPy film was verified using UV-Vis spectroscopy. A Perkin Elmer Lambda 950 was used for all UV-Vis spectroscopy experiments with a glass substrate used as the reference and sample substrate. Chemical reduction of a PPy film was done via a secondary vapor doping of polyethyleneimine (PEI, $M_W = 800$) on a hot plate at 250 °C for 10 min and sealed with a large glass petri dish cover at atmospheric pressure. To characterize film thickness, a KLA Tencor Step Height Profilometer was used with the same glass substrates. The spun cast FeToS oxidant film, the VPP PPy film, and the rinsed PPy film were measured to be ca. 0.9 μm, 1.0 μm, and 100 nm thick, respectively. Film thickness reported is an average thickness of 10 scans over a 12.7 x 25.4 x 0.7 mm coated-glass slide.

3.4.4 Device fabrication

Similar device fabrication has been previously reported [57]. In short, indium tin oxide (ITO)-coated glass (Part Number: CG-50IN-S107) was purchased from Delta Technologies, Limited with a sheet resistance of 8-12 Ω/sq. In order to remove any unwanted ITO, both the top and bottom synaptic electrodes were acid-etched using hydrochloric acid (36%) poured over zinc metal. The top synaptic electrode was patterned using polyimide tape (12 mm wide). The bottom synaptic electrode was templated using a positive photoresist such that a channel length of 100 μm separation bifurcates a single substrate into two separate ITO electrodes. After the top and bottom synaptic electrodes were properly over-coated with PPy, the substrates were mated with a 125 μm parafilm spacer. The parafilm had a well cut out with dimensions 12 x 20 mm, defining the devices active area as 240 mm^2. The well is filled in with a PEG-based gel containing a tetrabutylammonium hexafluorophosphate (Bu$_4$NPF$_6$) electrolyte [57]. The electrolyte is photo-polymerized with a ELC-500 Light Exposure System to properly seal and mate the top and bottom slides. The aluminum (Al) electrodes used on the toy car device were deposited via a Denton DV-502a thermal evaporator after templating and masking the car with polyimide tape. All other fabrication steps were repeated the same for the toy car device as the ITO-based devices.

3.4.5   Device characterization

Electrical characterization of the devices was done using a Keithley 236 Source Measurement Unit (SMU) to apply any required voltage-pulse scheme to the top synaptic electrode (V_{pre}) and a Keithley 2440 5a SourceMeter was used to supply a constant voltage supply to the bottom bifurcated synaptic electrode (V_{post}) while constantly monitoring the current. The Keithley 236 SMU was programmed using HTBasic by TransEra and the Keithley 2440 was programmed in LabVIEW. All testing is done in an ambient environment at room temperature (ca. 21 °C).

Chapter 4

Cascaded Logic Gates with Printed Electrochemical Memristors

4.1 Introduction

The demand for biologically inspired circuits stems from the need to reinvent current von-Neumann architectures, where a central processing unit (CPU) is combined with memory that is mainly composed of inorganic-based CMOS technology. This successful architecture ultimately leads to a bottleneck effect where a fetch sequence and an operation sequence cannot be achieved in tandem as these functions operate through a common data transfer pathway. To mitigate this bottleneck, memristive devices [1] are a potential replacement candidate as they can function both as data storage and information processing by working as a form of nonvolatile resistive memory [183, 184]. Within this class of device, memristors that employ redox-active conjugated polymeric electrochemical materials (ECMs) have been recently reported [50]. ECMs have been widely studied as electrochromic [91], biological sensors [185], neuromorphic computers [112], transistors [109], and energy storage devices [186] with promising results. The main attraction for polymeric ECMs arises from the ability to actively modulate their electronic and optical properties through a dynamic change in the material's redox state [159, 187]. For example, organic electrochemical transistors (OECTs) have been reported to display synaptic and neuromorphic features such as spike-timing-dependent-plasticity (STDP) [109], short- and long-term memory [57], and Pavlovian learning be-

haviors [50]. These neuromorphic-capable devices operate by programming pulses to the top gate electrode, ions migrate into (or out of) the bottom channel (drain and source) electrode in order to tune the channel's conductivity state [17, 50]. The ability to vary the device's conductivity in this manner imitates the modulating effect of synaptic weight for neurons through biological neuronic impulses.

Standard film deposition techniques, including spin- or dip-coating, require a solution-processable material in order to deposit a uniform film. ECMs, such as poly(3,4-ethylenedioxythiophene) (PEDOT), polypyrrole (PPy), and polyaniline (PANI), have the drawback of being insoluble once polymerized chemically or electrochemically [94] without the use of various additives [169, 188] or modifications to the chemical structure [143, 189]. These modifications add further complexity to the material's processability while impacting the material's conductive nature or chemical mechanism of operation. To this end, an *in-situ* chemical vapor polymerization deposition technique, referred to as vapor phase polymerization (VPP), has been employed [83, 91, 93, 96, 171, 174, 175] to overcome this challenge to planar film formation as well as to polymerize ECM films over arbitrary and non-conformal surface geometries. This *in-situ* technique utilizes an iron-based salt oxidant-coated surface to polymerize the desired monomer through a simple two-step process of (1) depositing the oxidant over the desired substrate and then (2) exposing the coated substrate to a monomer vapor [96]. The VPP technique can be combined with screen printing to create devices with complex geometries over rigid, flexible, or non-conformal substrates with the added virtue of ease of scalability and high resolution [93].

Screen printing (SP) is a mass-producible technique that has been used for printed electronics since the early 1980s [101]. This film fabricating technique involves depositing printable inks over a wide range of substrates through a stencil-coated screen. Screens are coated with a photo-reactive emulsified material to create a templated design that can transfer ink through the stenciled openings onto a substrate with high precision and reproducibility. High fidelity of printed structures relative to the screen's template is achievable with SP using optimized viscosities of the solution and mesh count of the screens and can surpass other deposition techniques. SP offers high-resolution printing with the routine deposition of 40 μm lines [93, 101] and can be further improved by varying the screen mesh count (60 - 500 threads per inch) or the screen material (polyester, nylon, polypropylene, fluorocarbon, or stainless steel) in addition to tuning the ink solution with additives or the screen emulsion material [190].

While common ECMs have been widely studied for their memristive properties [50, 57, 109], a redox-active conjugated polymer based on the heterocyclic dithienopyrrole (DTP) moiety has yet to be reported as a three-terminal synaptic emulator. Recently, a two-terminal device employed a polyDTP derivative with a carbazole moiety attached to the DTP backbone [112]. This dual percolative network between the electron-rich DTP backbone and electro-active pendant carbazole moieties was able to achieve continuous analog resistive switching and was capable of synaptic emulation with 100 fJ per programmed stimulus. Additionally, a synthetic modification of the polyDTP pendant groups has been achieved through a Cu(I)-catalyzed azide-alkyne cycloaddition (CuAAC) and is an important and simple route to alter the energetic characteristics of the resulting polymer [113].

Based on a three-terminal transistor configuration, an organic synaptic-emulating memristor is presented where the fundamental architecture is focused on a counter redox-stacked reaction [50]. This device operates by electronically (de)doping the redox state of the ECM to modulate the conductivity of the reduced channel via voltage- or current-driven programming stimuli through the oxidized gate. With this design approach, ECMs can be utilized in a similar device configuration to achieve various neuromorphic-capable computers. In the current embodiment, the utilization of the VPP and SP techniques allowed for the creation of a three-terminal synaptic-emulating memristor based on the polymer of 4-(6-hexyl)-4H-dithieno[3,2-b:2',3'-d]pyrrole (p6DTP). This is the first report of the VPP technique used for any DTP-based monomers, along with an in-series configuration for implementing advanced hardware operations (cascaded combinational logic). This device demonstrates operational programs, such as simple mathematics (addition, subtraction, multiplication, and division) and various logical operations (single and combinational logic gates), and biological memory emulation, such as the paired-pulse neuromorphic effect.

4.2 Results and Discussion

4.2.1 Film characterization

A combination of deposition techniques utilizing screen printing (SP) with vapor phase polymerization (VPP) was used to fabricate three-terminal electrochemical memristors (*cf.* **Fig. 3.1a**). VPP is a necessary step since dithienopyrrole-based polymers (polyDTPs) [94], as well as other electrochemical polymers [95], are insoluble after chemical or electrochemical polymerization.

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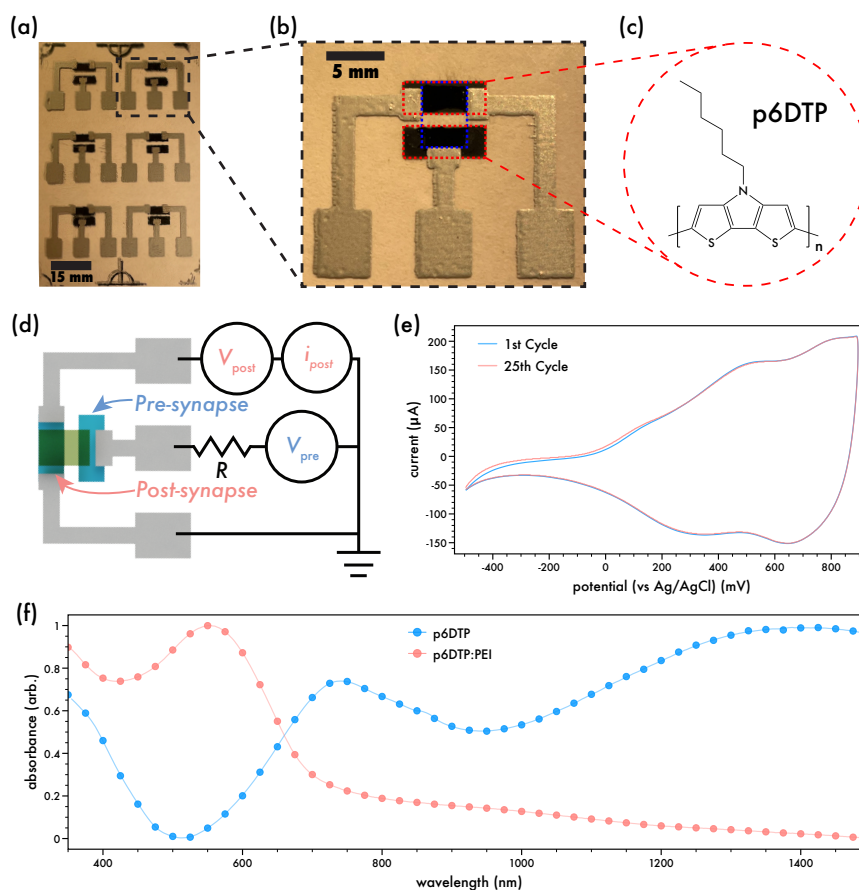
Figure 4.1: **(a)** Optical image of a screen printed array with varying device active areas. **(b)** Inset of a single device with an active area of 18.75 mm^2 and channel length of 1.45 mm. **(c)** Structure of poly(4-(6-hexyl)-4H-dithieno[3,2-b:2',3'-d]pyrrole) (p6DTP). **(d)** Schematic for the p6DTP-based three-terminal synaptic device and its equivalent circuit. **(e)** Cyclic voltammetry of VPP p6DTP films. Electrolyte is 0.1 M Bu$_4$NPF$_6$ in MeOH with a sweep scan rate of 100 mV/s. **(f)** Optical photo-physical properties of p6DTP thin films in the oxidized (blue) and chemically reduced (red) state.

Various oxidants (iron-based salts) have been reported for obtaining VPP electrochemical films, such as iron chloride (FeCl$_3$) [83, 96], iron trifluoromethane sulfonate (FeOtf) [91, 93], and iron tosylate (FeToS) [83, 93]. For this effort, FeToS was mixed with methanol (MeOH) at a concentration of 250 mg/mL followed by the addition of 30 wt% of a triblock copolymer, PEG-PPG-PEG, to create a printable ink [91, 93]. A PET sheet (75 x 50 mm) was used to print an array of 6 devices with varying active areas (AA) from 25.2 mm^2 down to 15.5 mm^2. All electronic data presented is tested with an AA of 18.75 mm^2 (*cf.* **Fig**. **3.1b**) and a channel length of 1.45 mm. The first layer printed was the oxidant ink which, after printing and annealing, was over-coated by VPP with 4-(6-hexyl)-4H-dithieno[3,2-b:2',3'-d]pyrrole (6DTP) (*cf.* **Fig**. **3.1c**) into a polymerized electrochemical film in its

oxidized state. After cleaning the iron-based salt from the VPP polymer film of 6DTP, referred to as p6DTP, the substrates were aligned based on registration marks and printed with the second layer, a commercial silver nanoparticle ink. The final layer printed is a gel electrolyte to encapsulate and electronically connect the p6DTPs pre- and post-synaptic films. After printing the gel electrolyte, the whole substrate is exposed to a UV-light source to photo-polymerize and crosslink the electrolyte, completing device fabrication.

The electronic schematic diagram is presented in **Figure 3.1d** for this three-terminal device. The input programming bias (V_{pre}) drives the pre-synaptic terminal of the device to modulate the current response (i_{post}) of the post-synaptic terminal, monitored at a constant voltage (V_{post}). The response of i_{post} is further used to calculate the conductivity (G) of the post-synaptic terminal (i_{post} = V_{post} x G) and is analogous with the synaptic weight of a neuron [57]. A 1 MΩ resistor is used in series with the pre-synaptic input to limit the device's driving force (i_{pre}). This resistor also aids in adequately disconnecting the two terminals by slowing down the electrochemical draining process [50].

To characterize the electrochemical films, cyclic voltammetry (CV) is first measured for a VPP p6DTP fabricated over an ITO-coated glass acting as the working electrode in conjunction with a Ag/AgCl reference and Pt wire counter electrode. CV is performed in a 0.1 M Bu_4NPF_6/MeOH electrolyte solution with cyclic sweeps performed from -500 to +900 mV in increments of 100 mV/s. **Figure 3.1e** presents the reversible oxidative nature from the 1st to the 25th cycle, where the oxidation and reduction peaks are re-traced, indicating no degradative processes are occurring with cycling. The onset potential (E_0) of the oxidation peak, ca. 40 mV, is used to estimate the ionization potential (IP), which is analogous to the highest occupied molecular orbital (HOMO). Assuming the energy at vacuum level is 0.0 [191], HOMO can be equated as IP (eV) = E_0 + 4.40, giving p6DTP an energy level of 4.44 eV, comparable to other reported p6DTPs that are polymerized by chemical [192] or electrochemical [112] means.

The optical properties of the VPP produced p6DTP films are presented in **Figure 3.1f**. The as-fabricated film (oxidized) has a maximum absorption (λ_{max}) at ca. 740 nm, corresponding to the polymer DTP backbone [94, 112], and a broadband absorption past ca. 944 nm. To fabricate a reduced film, VPP p6DTP films are exposed to a secondary vapor doping of polyethyleneimine (PEI) [178]. The reduced film has a drastically diminished absorption in the longer wavelength region with a λ_{max} blue shifted towards ca. 553 nm. The characteristic of broadband absorption

(oxidized) and diminished broadband absorption (reduced) are common traits of electrochemical conjugated polymers [73]. The reduced film absorption peak's onset begins at ca. 710 nm which is used to demonstrate the observed optical electronic bandgap (ΔE_{UV}). From the onset (observed as a tangent between the rising absorption and a background baseline), the p6DTP film demonstrates an ΔE_{UV} of 1.75 eV. Coupling the optical bandgap with the HOMO, a derived lowest unoccupied molecular orbital (LUMO) can be obtained in the form LUMO = HOMO - ΔE_{UV} and is estimated to be 2.69 eV. Density functional theory (DFT) was used to investigate and verify the experimental energy levels of p6DTP. It has been reported that DFT calculations converge and saturate for energy levels between 4-6 repeating units [193–195]. Energetic properties are calculated based on a three-parameter hybrid exchange (B3LYP) with a 6-31G* basis set with the pentamer of 6DTP demonstrating a value of 4.353 eV. Pairing the theoretical HOMO value with ΔE_{UV}, a LUMO value of 2.603 eV is obtained. The experimental values compare closely to the theoretical values, proving the efficiency of the VPP technique in creating p6DTP films. This methodology can further be applied for other DTP derivatives toward future experiments utilizing the VPP technique.
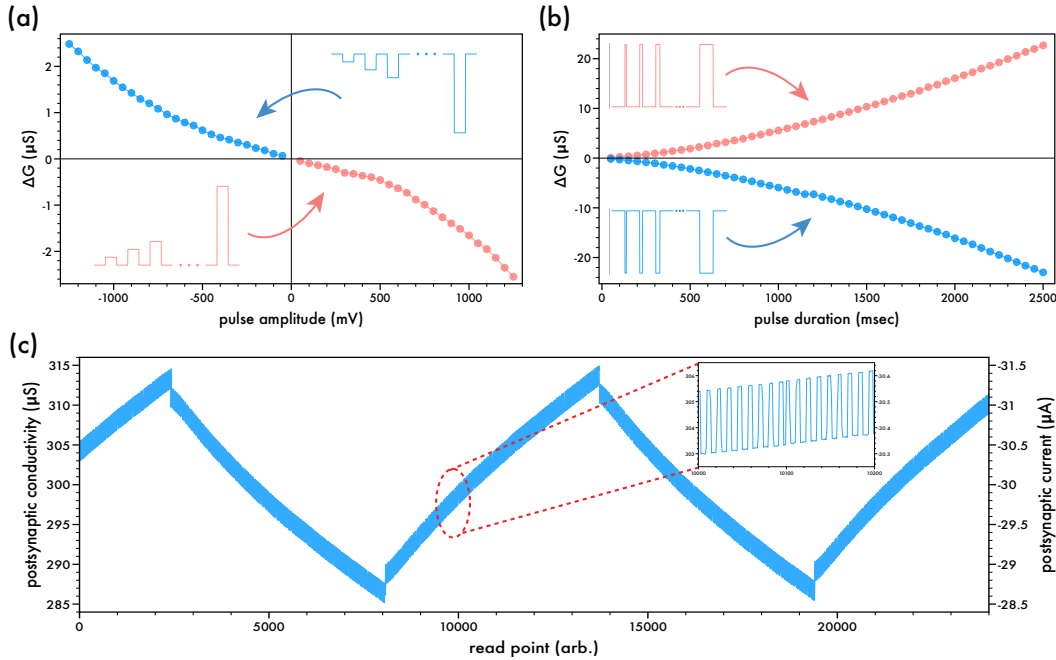
Figure 4.2:   Characteristic device response for the post-synaptic terminal based on the pre-synaptic input voltage pulse at **(a)** constant duration (t_{pre} = 100 msec) and **(b)** constant amplitude (V_{pre} = ±500 mV). **(c)** Distinct analog conductivity tuning of long-term potentiated and depressed cycles. An input of 500 voltage-driven pulses (V_{pre} = ±500 mV, 100 msec) is applied while monitoring the post-synaptic terminal with a bias voltage of -100 mV (V_{post}). Inset shows a snapshot of analog tuning through the potentiated cycle (-V_{pre}).

4.2.2 Device performance

The principal operation for the p6DTP-based device is that the programmed input bias (V_{pre}) will drive ions across the pre-synaptic terminal, through the gel electrolyte, and into the post-synaptic terminal, modulating the current, resistance, and its reciprocal (conductivity) concurrently. The gel electrolyte acts as an electronic barrier that decouples the pre-synaptic and post-synaptic terminals when no V_{pre} bias is applied. A small -100 mV bias is constantly applied to read the post-synaptic terminal (i_{post}) and is used to measure any changes in the p6DTP layer between the post-synaptic terminal and the ground. The operational characteristic of the device is demonstrated in **Figure ??a,b** by modulating the amplitude or the duration of the V_{pre} input while keeping the opposite parameter (duration or amplitude) constant. To elaborate, **Figure ??a** presents varying V_{pre}'s amplitude from ±50 mV to 1250 mV while keeping the duration constant ($t_{pulse} = 100$ msec). A near linear trend in the change in conductivity (ΔG) can be observed and this predictable response can be exploited in various mathematical and logical operations, which will be presented in subsequent sections. In regards to long-term potentiation (LTP) and depression (LTD) effects, similar to biological memory, **Figure ??c** demonstrates the devices tunability with 500 steps per cycle by applying ±500 mV pulses with a duration of 100 msec on and 200 msec off to V_{pre} while monitoring i_{post}. The monitored outcome of this voltage application shows distinct analog and tunable steps from ca. 286 μS up to 314 μS for an average step height of ±0.056 μS per synaptic input.

Analyzing 10 V_{pre} pulses per bias (short-term potentiation and depression) (*cf.* **Fig. ??a**), a linear analog tuner is envisioned. It is important to note that $+V_{pre}$ (red) input pulses will increase i_{post} while decreasing the conductivity (G), while a corresponding reverse response is achieved with $-V_{pre}$ (blue) inputs. The resolution of this program shows steps of ±0.04 μS per synaptic input with an average standard deviation of 0.009 μS, derived from analyzing 10 cycles with pulse parameters of $V_{pre} = \pm500$ mV, $t_{pulse} = 100$ msec on and 200 msec off. The initial starting i_{post} is measured before any programmed V_{pre} is applied at a conductivity of 297.77 μS. After 10 $-V_{pre}$ pulses, the device's conductivity is driven up to 298.17 μS, for a total change (ΔG) of 0.40 μS. Following the 10 $-V_{pre}$ pulses, 10 $+V_{pre}$ pulses are applied and returns the device to a conductivity of 297.76 μS for a ΔG of 0.01 μS off of the initial baseline state. Through the application of $\pm V_{pre}$ synaptic inputs, the mathematical operations of addition and subtraction are implemented where, in regards
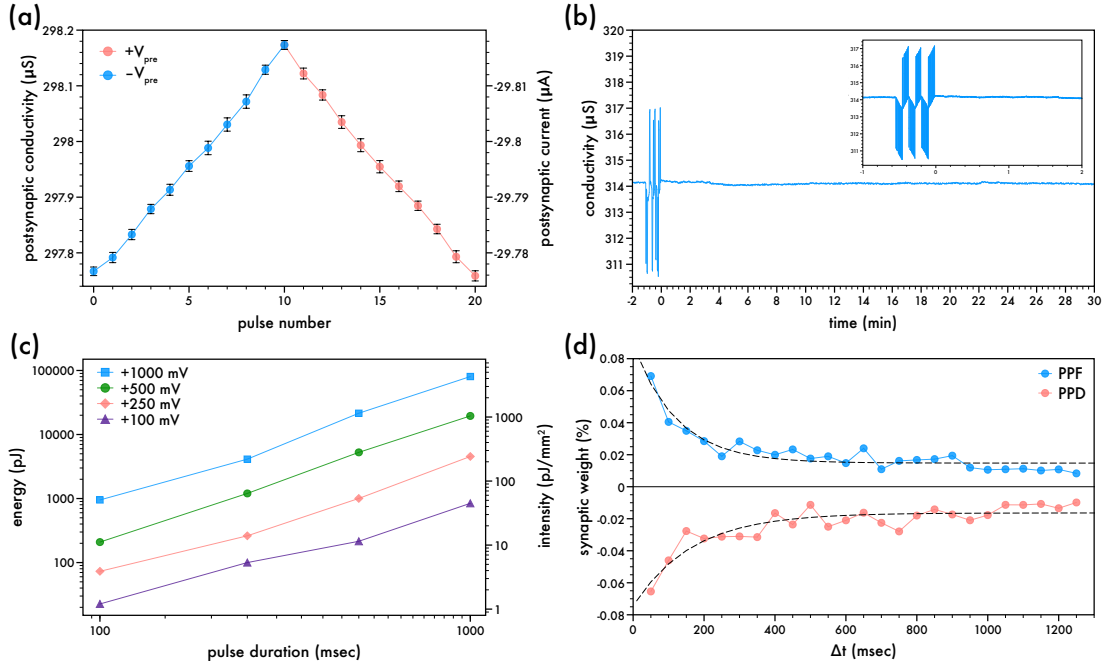
Figure 4.3: **(a)** Post-synaptic conductivity and current response depicting 10 distinct states per potentiation (-V_{pre}) (blue) and depression (+V_{pre}) (red) cycle. Standard deviation shown is an average of 10 cycles. **(b)** Retention characteristics after three cycles of potentiation/depression monitored for 30 minutes with a constant V_{post} bias. Inset displays the first 2 min. after programming. **(c)** Power consumption per pre-synaptic input characteristics of the device. **(d)** Paired-pulse facilitation (PPF) (blue) and paired-pulse depression (PPD) (red). Dashed lines represent data fitted curves.

to measuring G, -V_{pre} emulates addition and +V_{pre} emulates subtraction. In **Figure ??b**, retention of the device is measured by programming 3 cycles of 10 pulses per bias at the same input parameters as **Figure ??a** while i_{post} is monitored for 30 minutes after application with no V_{pre} bias. Within 15 seconds after the pre-synaptic pulses are applied, the post-synaptic terminal decreases by only 0.016% from the last pulses i_{post} state, and after 30 minutes, a decrease of 0.068% is observed. This demonstrates the device's excellent state stability and retention as a nonvolatile neuromorphic computational and operational device for long-term use. It is speculated that the device's state will hold within a 5% tolerance for a period of well over 36 hours.

4.2.3 Neuromorphic trends

Power consumption of a biological synapse range on the order of 1 - 100 fJ per synaptic event [151] and for synthetic equivalents to achieve some level of parity their energy consumption must be on the same order for future neuromorphic computers [196]. **Figure ??c** demonstrates the power

consumption requirements for the current embodiment of the p6DTP-based synaptic memristor. At the current state of operation (*cf.* **Fig**. **??a**), the energy consumed per synaptic input draws below 1000 pJ. Here, energy (P) is calculated as P (pJ) = i x V x t and intensity (E) as E (pJ/mm^2) = P / AA with an AA of 18.75 mm^2. Through optimization of the input pulse parameters, dropping the amplitude down to 100 mV, only 22.5 pJ, or nearly 1 pJ/mm^2, of energy is consumed per input. This can be further optimized by either modifying the electrochemical films with additives [50], tuning the material properties by adding an electro-active species off the DTP backbone [112, 113], or adjusting the pre-synaptic input parameters [57].

In regards to biological systems, the operation of this device emulates the mechanisms of writing, reading, and forgetting. **Figure ??d** demonstrates the operation of paired-pulse facilitation (PPF) (blue) and depression (PPD) (red), where the percent change in conductivity is referred to as the modulation of the synaptic weight of a neuron. PPF and PPD are short-term memory effects measuring the response of the post-synapse based on two incoming pre-synaptic stimuli and the timescale between their application [197]. Here, two ±500 mV V_{pre} pulses are programmed with a pulse duration of 100 msec while varying the timescale (Δt) between each pulse from 50 msec up to 1250 msec. The post-synaptic terminal (V_{post}) is biased with a -100 mV amplitude while monitoring the response where the first response is defined by the state G_1 and the second state as G_2 per each varied timescale input series. The characteristic synaptic weight response (%) is calculated as (G_2 - G_1) x (100 / G_1) and can be further fitted to the form of a dual exponential:

$$PPF/PPD = C_1 \exp(\Delta t/\tau_1) + C_2 \exp(\Delta t/\tau_2)$$

where C is a unitless amplitude and τ is the relaxation time constant for two distinct phases: (1) rapid phase and (2) slow phase. Biological synapses are reported to exhibit this paired-pulse phenomena with the characteristic response well fitting this dual-exponential equation presented [197]. For the p6DTP-based devices, -V_{pre} causes a positive change in synaptic states per pulse (PPF), while +V_{pre} leads to a negative change (PPD). PPF has an observed τ_1 of 0.833 msec and τ_2 of 612.55 msec while PPD displays a τ_1 of 1.003 msec and τ_2 of 827.79 msec. The unitless amplitude, C, is observed as C_1 of -0.0164 and C_2 of -0.05833 for PPF while PPD displays a C_1 of 0.0149 and C_2 of 0.0747. Again, this effect can be tuned by modifying either film with additives [50], the chemical structure [112, 113], or the pulsing parameters [57].
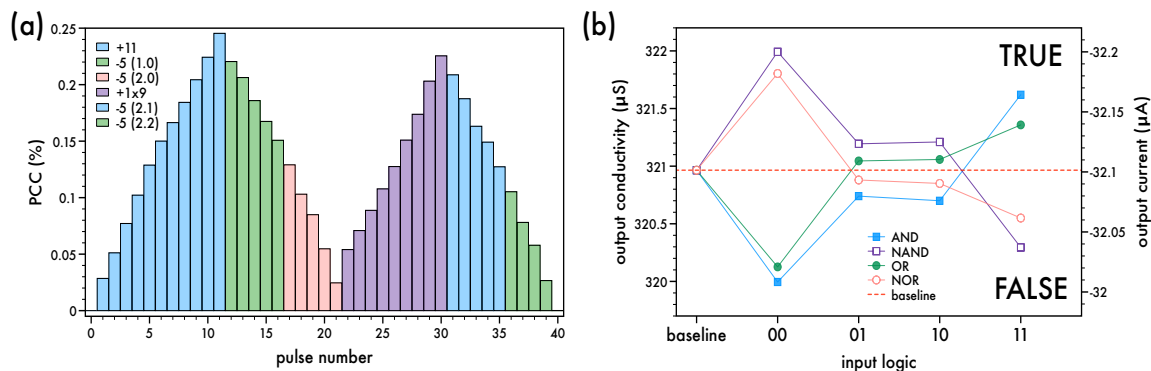
Figure 4.4: **(a)** Division operation for $11 \div 5 = 2.2$. **(b)** Logical operation output for various single gate logic (AND, NAND, OR, NOR). The dashed line represents the baseline state prior to any programmed logical input.

4.2.4 Arithmetic & logic operations

The presented analog tunable p6DTP-based device can perform various mathematical operations of addition and subtraction, multiplication, and division. With over 500 distinct programmable states (*cf.* **Fig. ??c**), operations containing multiple loops of numerical indexing and re-indexing can be achieved. For example, the division operation for $11 \div 5$ is demonstrated in **Figure ??a**. The mathematical division operation is achieved in the form $A \div B = C$ where $A = 11$, $B = 5$, and C is the quotient (Q) derived by counting the application of sequential subtraction operations, defined as n. To quantify the change, the percent conductivity change (PCC) is reported in the form of (G_n - G_0) x (100 / G_0), where G_0 is the initial baseline conductivity and G_n is the conductivity at each operational step. A series of 11 V_{pre} pulses are programmed to the device's input with -500 mV and 100 msec parameters, increasing the device's conductivity by a PCC of 0.2454%. This is then followed by a subtractive-multiplication step of n_1 groups of -5 in the form of 11 - (n_1 x -5) such that a remainder, r, satisfies $0 < r < 5$. The operation is complete for $n_1 = 2$ for a total subtraction of 2 x -5 = -10. This is achieved by applying a total of 10 +500 mV, 100 msec input pulses to the device, decreasing the PCC to a value of 0.02459%. This provides an integer quotient of 2 (based on the n_1 value) and a numerical remainder, r, of 1. Since the current numerical remainder, 1, is smaller than the divisor, $B = 5$, the next operation is to add r x 9, or 1 x 9, to the current device's conductivity remainder state. This is done by adding 9 -500 mV, 100 msec input pulses, raising the numerical count to 10 and a PCC of 0.2255%. The final subtraction is then performed by the equation 10 - (n_2

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x 5) where n_2 is satisfied by $n_2 = 2$. To perform the final operation, 10 +500 mV, 100 msec pulses are programmed to the device and the final PCC decreased to 0.0001%, the numerical equivalent of 0 for this operation. The two sequential subtraction steps across this whole operational program are counted and equate to Q = n_1 + 0.n_2 = 2 + 0.2 = 2.2.

Table 4.1: Single gate logic truth table.

			truth table			
A•B	input	A	0	1	0	1
		B	0	0	1	1
	output		0	0	0	1
¬A•B	input	A	0	1	0	1
		B	0	0	1	1
	output		1	1	1	0
A+B	input	A	0	1	0	1
		B	0	0	1	1
	output		0	1	1	1
¬A+B	input	A	0	1	0	1
		B	0	0	1	1
	output		1	0	0	0

Table 4.2: Input parameters for each corresponding single gate logical *1* (*TRUE*) and *0* (*FALSE*) statement.

gate	logic	voltage parameters	
		amplitude (mV)	duration (msec)
A•B	0	+500	1000
	1	-500	500
¬A•B	0	-500	1000
	1	+500	500
A+B	0	+1000	500
	1	-500	200
¬A+B	0	-1000	500
	1	+500	200

Memristive devices are envisioned to overcome current von-Neumann architecture drawbacks due to their ability to act as both a processing and storage unit. Recently reported ECM-based three-terminal devices have supported that notion [57, 109, 150], with the current device capable of extending this approach from single gates into a cascaded combinational logical circuit. For example, by adjusting the voltage parameters of the input (amplitude and duration) (*cf*. **Fig**. **??a,b**), various single logic gates can be programmed for a single device [57, 150]. **Figure ??b** demonstrates the

use of a single device (*cf.* **Fig**. **3.1d**) that encompasses various single logic gates. The four gates are presented in the following boolean algebraic terms: AND is defined as A•B, while its negative form, NAND, is defined as ¬A•B, and OR is defined as A+B, while its negative form, NOR, is defined as ¬A+B. In short, a series of two inputs are programmed to the pre-synaptic terminal that is represented as *0* or *1*, also referred to as *FALSE* or *TRUE*, statements. The truth table for all four single logic gates is presented in **Table 3.1**, where A and B are the inputs that are programmed to the pre-synaptic terminal before deriving the logical output of the post-synaptic terminal. For this p6DTP-based device, **Table 3.2** presents the designed voltage parameters for all single logic gates for their *0* and *1* inputs. Through the application in the series of *00*, *01*, *10*, and *11*, the output conductivity is modulated to demonstrate the expected logical output for all four single gates (*cf.* **Fig**. **??b**). A baseline current is defined prior to any logical input and is defined for the device as 320.965 μS. Any final conductivity state > 302.965 μS is defined as *1 (TRUE)* and any state $<$ 302.965 μS is defined as *0 (FALSE)*. The linear analog tuning capability of this device allows for these operations to be achieved where, after each logic input series (*00*, *01*, *10*, and *11*), a reset operation is programmed such that oppositely biased pulses are applied, returning the conductivity state to the device's original baseline.

While there have been reports on two-terminal memristors as cascaded logic in the form of modeled circuits [198–201], no physical representation has yet to be achieved. This article presents the first implementation of a synaptic-emulating memristor that demonstrates cascading logical computations with only two p6DTP-based devices and no additional components. **Figure ??a** presents the cascaded Boolean circuit incorporating two devices in series in order to achieve this operation. To demonstrate, each device is tested as an AND gate where the output of the first AND gate feeds into the input of the second AND gate. The Boolean algebra for the input of this cascade can be expressed as (A•B)•D. **Figure ??b** shows the equivalent circuit for this experiment where the first p6DTP-based AND device (D_1) has the post-synaptic terminal tied into the pre-synaptic terminal of the second AND device (D_2). This connection provides the electronic cascade pathway from D_1 to D_2. **Table ??** presents the logical input and output cases based on the Boolean logic circuit presented in **Figure ??a** for this D_1•D_2 cascade. The inputs for D_1 are defined by the variables A and B with an output of C, whereas D_2 is defined by the inputs C and D, defining the final logical output for the cascaded gates. **Figure ??c** shows the raw output data for D_2 throughout the entire logical programming operation (*000*, *001*, *010*, *011*, *100*, *101*, *110*, and *111*).
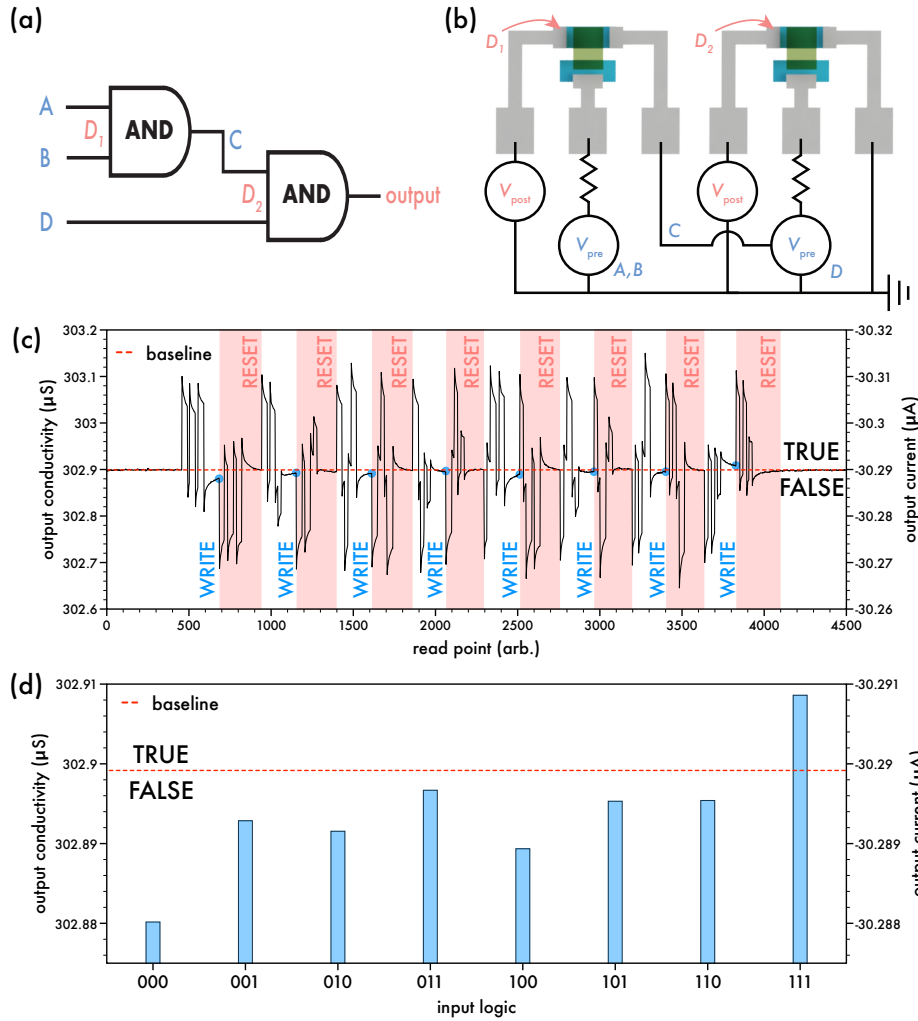
Figure 4.5: **(a)** Combinational logic gate of two AND gates. **(b)** 3D schematic for the p6DTP-based combinational logic gate and the equivalent circuit. **(c)** Output data after applying all cases of logical inputs and reset operations. The dashed line (red) represents the baseline conductivity and current prior to any programmed logical input. The circles (blue) indicate the final logical output after applying each logical input series. **(d)** Extrapolated data showing the logical outputs for the device after the combinational programming sequence. The dashed line (red) represents the baseline conductivity and current prior to any programmed logical input.

Just like the single logic gate, the same negative application of each input operation is programmed to reset the device to its baseline state (*cf.* **Fig**. **??c**). After each logical operation, a 3 sec wait is held before the conductivity is determined as the final logical output. The 3 sec wait is sufficient to allow the baseline conductivity to stabilize as D_2 is disconnected from D_1's post-synaptic terminal. **Table ??** presents the voltage parameters for each device's logical input sequence, and **Figure ??d** shows the final logical output data after the series of all logical inputs. The voltage program pulses

are kept the same for D_1 as the single gate AND, whereas D_2 has been slightly modified such that the *0* input is the same and the *1* input amplitude is decreased by half (-250 mV). This parameter modification is necessary due to the modulation effect that D_2 has on the final output, increasing or decreasing the conductivity more than the response from D_1 based on this in-series configuration. With a baseline conductivity of 302.9 μS, the application of the 3 inputs (A, B, and D) are able to tune the conductivity of D_2 such that the final state > 302.9 μS defines the logical output of *1* *(TRUE)* and < 302.9 μS defines the logical *0 (FALSE)* output.

Table 4.3: Combinational $D_1 \bullet D_2$ logical truth table. C is an intermediate input based on the output defined from A$\bullet$B.

			truth table							
		A	0	0	0	0	1	1	1	1
	input	B	0	0	1	1	0	0	1	1
$D_1 \bullet D_2$		D	0	1	0	1	0	1	0	1
	intermediate	C	0	0	0	0	0	0	1	1
	output		0	0	0	0	0	0	0	1

Table 4.4: Input parameters for D_1 and D_2 devices logical *1* *(TRUE)* and *0* *(FALSE)* statement.

device	input	logic	voltage parameters	
			amplitude (mV)	duration (msec)
D_1	A$\bullet$B	0	+500	1000
		1	-500	500
D_2	D	0	+500	1000
		1	-250	500

To perform the cascaded combinational logic operation, following the parameters in **Table ??** and **Table ??** and the schematic diagram in **Figure ??b**, the series of logical inputs are applied, followed by a negatively biased reset operation between each series. To elaborate, the first input series, *000*, is achieved where D_1 is programmed with two *0* inputs ($V_{pre} = +500$ mV, 1000 msec) fed electronically into D_2's input via D_1's output terminal. The two initial D_1 inputs (*00*) modulate D_2's output such that the conductivity is driven down from 302.9 μS to 302.86 μS (read after a 100 msec wait). The final input of the *000* series is a +500 mV, 1000 msec pulse programmed at the input of D_2. This decreases D_2's output where, after a wait time of 3 sec, the final output is measured as 302.88 μS for this input series, resulting in a final logical outcome of *FALSE*. The device is reset through the application of the negative *000* series. This is shown in **Figure ??c**, where two

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-500 mV, 1000 msec pulses are applied to D_1 followed by a single pulse of -500 mV, 1000 msec to D_2. After a 3 sec wait, the device returns to the baseline conductivity of 302.9 μS. These operations (write and reset) are applied for all logical input series to achieve a fully functional cascaded combinational $D_1 \bullet D_2$ circuit with only two three-terminal p6DTP-based devices. Extending this approach to other logic gates (*cf.* **Fig**. **3.2** and **Fig**. **??b**) or to deeper-nesting cascades is straightforward.

4.3   Conclusions

A three-terminal synaptic device is fabricated using screen printing (SP) and vapor phase polymerization (VPP) techniques. The poly(4-(6-hexyl)-4H-dithieno[3,2-b:2',3'-d]pyrrole) (p6DTP) VPP films electronic energy levels are experimentally derived utilizing cyclic voltammetry and photo-physical measurements and demonstrates energy levels comparable to similar dithienopyrrole derivatives. The use of the VPP technique for generating a p6DTP which is energetically similar to standard chemical and electrochemical polymerization routes is verified by comparison of the experimentally-derived energetic properties of the polymer with DFT-derived theoretical values. This organic synaptic-emulating p6DTP-based device is capable of power consumption on the order of 1 pJ/mm^2 per synaptic input. The power requirements can be further decreased by varying the voltage parameters of the input or by tuning the chemical or device architecture. The device is proven to exhibit reproducible analog conductivity tuning traits, leading to its use as a future neuromorphic computer. Along with the ability to perform information processing (mathematical and logical operations), this is the first implementation of a memristive device as a cascaded combinational logic circuit. This configuration is a significant demonstration toward deeper-nesting cascaded logical circuits for memristive devices.

4.4   Experimental

4.4.1   Materials

All chemical materials were purchased from Alfa Aesar and Sigma Aldrich and used without further purification or processing. The monomer synthesis of 4-(6-hexyl)-4H-dithieno[3,2-b:2',3'-d]pyrrole (6DTP) has been previously reported [202]. Deionized water (DI-H$_2$O) exhibited a resistivity value of 10^{18} Ohm^{-1} cm^{-1} from a Nanopure System.

4.4.2 Screen preparation

Polyester screens used to print were mounted and stretched to fit a 12" x 12" ID frame. These screens were loaded under ca. 20 N/cm of force (tension) across the surface prior to adhering to the screen frame. All screens were cleaned via scrubbing a chemical abrader/degreaser (ICC 858) to remove any impurities and grease from the screens surface. This cleaning is followed by a quick rinse in water and then scrubbed with another chemical degreaser (ICC 837) and rinsed with water. Clean screens were placed in a fume hood until fully dried prior to templating.

4.4.3 Screen templating

Transparencies of designs were printed using a shadow mask using Kodak SquareSpot Imaging Technology. The cleaned screens were misted with warm water to adhere capilex films onto the bottom surface (screen print side down). Capilex 50 was used for all printing screens. Once the screens were properly coated and dried, the desired template is photo-etched on the surface of the capilex using a Kepro Circuit Systems Inc. model BTX-200A ultra-violet exposure frame. For the capilex-coated screens, the template/light was exposed for 250 seconds. Following exposure, the screen was washed with warm water to remove the unwanted capilex. Three screens were templated and used throughout this research in the following order: 1) the oxidant ink layer at 230 mesh, 2) the silver (Ag) ink electrodes at 305 mesh, and 3) the electrolyte ink layer at 230 mesh. Once the capilex film was templated and dried, the remaining open areas of the screen are covered and masked with painters tape.

4.4.4 Screen printing

A Hary Manufacturing Inc. MSP-088 manual bench top screen printer was used for all prints. The oxidant layer screen was mounted and printed first in this series. A test sheet was printed to adjust for alignment between screens with predefined registration marks. Ink was generously placed on one side of the screen above the design and a 6.5" 70 Shore A squeegee was used to sweep across and fill ink in the pores of the screen. The screen then was lowered over the substrate and the squeegee was swept across the surface to deposit the ink onto the substrate at 45° in reference to the screen. Following each print, the coated substrates were annealed or further processed prior to applying other layers. This process was then repeated for the subsequent screens and film depositions.

4.4.5 Vapor phase polymerization of 4-(6-hexyl)-4*H*-dithieno[3,2-*b*:2',3'-*d*]pyrrole

Prior to the first print coating, flexible PET substrates (0.05" thick) were cleaned in a sonication bath of DI-H_2O, acetone, then isopropyl alcohol for 10 min each, dried by N_2 gas, and then plasma cleaned in a Harrick PDC-32G plasma cleaner on high for 5 min. Polymerization of various conjugated polymers through a vapor phase technique have been previously reported [83, 96, 171, 174, 175], however, this is the first known example of this technique used for any dithienopyrrole-based monomers. Herein, a simple procedure for the polymerization of 6DTP via VPP is reported. Iron (III) tosylate (FeToS) hexahydrate was mixed in methanol (MeOH) at a concentration of 250 mg/mL and stirred for 2 hours. To make the solution into a screen printable ink, 30 wt% of PEG-PPG-PEG ($M_n = 2,900$) was added and the solution was stirred at 300 RPM for 12 hours. After printing the oxidant layer, the substrate was annealed at 90 °C for 5 min to remove residual solvent. The films appeared as a yellow color and transitioned to orange during the anneal. The printed oxidant layer had a thickness of ca. 1.8 μm. The oxidant-coated substrates were mounted over a small petri dish containing ca. 20 mg of 6DTP monomer and loaded inside a model 5851 National Appliance Co. vacuum oven. The oxidant coated slides were exposed to monomer for 3 hours under ca. 20 inch of Hg at a temperature of 90 °C. After the vaporization of 6DTP solid to a gas phase, the orange oxidant films transitioned to a dark blue-purple film, indicative of the formation of an oxidized species. To remove the oxidant, the slides were fully submerged in a MeOH bath for 5 min before drying with N_2 gas. The poly(4-(6-hexyl)-4*H*-dithieno[3,2-*b*:2',3'-*d*]pyrrole) (p6DTP) film had a thickness of ca. 6.9 μm.

4.4.6 Device fabrication

Following the VPP of oxidant-to-p6DTP step, Ag electrodes were printed over. The Ag ink, purchased from Henkel (Loctite ECI 1011), was annealed at 120 °C for 3 min and checked with a multimeter for conductivity (R < 1.0 Ohm). The printed electrode layer had a thickness of ca. 17.7 μm. The last print was to encapsulate the device with a polymeric electrolyte gel. The electrolyte ink solution used has been previously reported [57]. In short, the electrolyte ink contains tetrabutylammonium hexafluorophosphate (Bu_4NPF_6) mixed in 2,2-diethoxyacetophenone (DEAP), polyethylene glycol dimethacrylate (PEG-DMA), and polyethylene glycol methacrylate (PEG-MA).

After printing, the electrolyte was photo-polymerized for 5 min with a ELC-500 Light Exposure System to polymerize and crosslink the gel film. The printed electrolyte layer had a thickness of ca. 8.3 μm. To ensure proper connection and longevity of testing, the gel electrolyte ink layer print was repeated 5 times and gave a final thickness of ca. 53.5 μm. The devices tested in this experiment had an active area of 5.0 x 3.75 mm (length x width) or 18.75 mm^2.

4.4.7 Electrochemical characterization

Electrochemical characteristics of p6DTP films were investigated through cyclic voltamme-try (CV) and used to estimate the HOMO energy level. ITO-coated glass (sheet resistance of 8 Ω/sq) was cleaned with the same steps as mentioned above prior to coating. The oxidant ink was spun cast at 5000 RPM for 40 sec using a Specialty Coating Systems Spincoat G3P-8 and annealed at 90 °C for 5 min prior to VPP. After the VPP, the p6DTP film was rinsed for 1 hour in a 1:1 vol% MeOH:DI-H$_2$O bath before drying with N$_2$ gas. The oxidant film and the p6DTP film had thicknesses of ca. 67 nm and 210 nm, respectively. CV was performed using a Ag/AgCl reference, Pt wire counter, and ITO/p6DTP working electrode in a 0.1 M Bu$_4$NPF$_6$/MeOH solution at room temperature. The solution was purged with N$_2$ for 30 min prior to testing. CV data is presented in IUPAC standard for the redox voltage and current convention. The experimental HOMO energy level was measured based on tangents drawn from the onset of the first oxidation potential (E$_0$) and a baseline from the background current. The experimental LUMO energy level was calculated based on the observed electronic absorption band edge and the CV-derived HOMO level (LUMO = HOMO - E$_{UV}$).

4.4.8 Film characterization

All films were characterized via UV-Vis spectroscopy and through thin-film profilometry. Removal of the FeToS oxidant from the p6DTP film was verified using UV-Vis spectroscopy. A p6DTP film was chemically reduced via vapor doping of branched-polyethyleneimine (PEI) (M$_W$ = 800) at 250 °C for 12 min on a hot plate in ambient environment. A Perkin Elmer Lambda 900 was used for all experiments with a glass slide used as the sample and reference substrate. The observed electronic absorption band edge (E$_{UV}$) was estimated for the reduced p6DTP (p6DTP:PEI) film from the onset of the absorption peak (observed as a tangent from the rising absorption and the

baseline). A KLA Tencor Step Height Profilometer was used to characterize film thickness with the same glass slides. Film thickness reported was an average of 10 scans over a coated-glass slide.

4.4.9 Electronic structure simulation

Geometry optimization of the 6DTP pentamer was accomplished using both Molecular Orbital PACkage (MOPAC) semi-empirical software with a PM3 Hamiltonian followed by QChem ab initio calculator utilizing a 6-31G* basis set. Electronic properties of the 6DTP pentamer was calculated by using DFT method optimized with a 6-31G* basis set and the three-parameter hybrid exchange functional B3LYP.

4.4.10 Device characterization

Electrical characterization for single device operations was done using a Keithley 236 Source Measurement Unit (SMU) to apply any required voltage scheme to the presynaptic electrode. A Keithley 2440 SourceMeter was used to supply a constant voltage supply to the post-synaptic electrodes while constantly monitoring the current. For the combinational logic gate, the Keithley 236 was substituted with a HP 4145a Semiconductor Analyzer to apply various voltage pulses across two different SMU channels (D_1 and D_2). Two Keithley 2440 SourceMeters were used where one to applied a bias to the first device (D_1) and the other to apply a bias and read the current across the second device (D_2). The Keithley 236 and HP 4145a were programmed using HTBasic by TransEra and the Keithley 2440 was programmed in LabVIEW. All testing is done at room temperature (ca. 22 °C) in an ambient environment.

Chapter 5

Conclusions and Discussion

5.1 Summary

The specific aim of the presented dissertation began with the investigation of redox-active electrochemical polymers for the development of three-terminal based conjugated polymeric electrochemical memristor systems. Redox-active electrochemicals constitute a class of capable synaptic-emulating materials through synthesis and tuning of the redox potential to modulate their electrical properties. Modulation of the redox potential varies based on the chemical structure and the stimulus applied, where moving electrons across the species can either oxidize or reduce the chemical system. In this work, a variety of synthesis strategies and fabrication techniques are implemented in order to create fully synaptic-emulating conjugated polymeric electrochemical memristors that also demonstrate various electronic operations. The following summary details a highlight of each chapter based on the electrochemical materials used and different fabrication techniques for implementation as these three-terminal electronic devices:

Fabrication and characterization of roll-to-roll printed memristors. An electrochemical derivative of the widely used PEDOT, referred to as a self-doped poly(sodium 4-((2,3-dihydrothieno [3,4-b][1,4]dioxin-2-yl)methoxy)butane-2-sulfonate) (S-PEDOT) was synthesized by means of an oxidative polymerization technique. This polymer was water soluble due to the attached sulfonic acid group off of the polymer backbone and was suspended in a water:methanol mixture in order to deposit as a thin film. Absorbance measurements of the polymer confirm a near-perfect spectral overlap of the S-PEDOT polymer to its commonly used commercial self,

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PEDOT:PSS. The low cost and ease of synthesis aid itself to the novelty of this polymer, where additives, such as polystyrene sulfonate (PSS), are not necessary while retaining its key features. Employing a roll-to-roll gravure printing technique, thin films of the S-PEDOT were deposited with this high-speed, mass-producible approach. While only a few samples were made per batch, nearly thousands of devices could be processed and fabricated in accordance to this report. After roll-to-roll printing over two flexible PET substrates coated and templated with indium tin oxide (ITO), a transparent electrode, a counter-redox stacked device was envisioned with an as-fabricated oxidized S-PEDOT film and a S-PEDOT film chemically reduced by means of vapor doping with branched polyethyleneimine (PEI). The counter-redox device was finalized by mating the oxidized and reduced films over a gel electrolyte containing a PEG-based network and tetrabutylammonium hexafluorophosphate (Bu_4NPF_6) electrolyte. This gel electrolyte acts as an energy barrier to prevent electronic recombination between the top oxidized film and the bottom reduced film. As voltage- or current-biasing passes through the single top electrode (referred to as the gate or the pre-synaptic input), the energy barrier is drastically decreased, allowing ions to migrate from the top electrode, across the gel electrolyte, and into the bifurcated bottom electrodes (referred to as the drain and source electrodes, i.e. the channel, or the post-synaptic outputs). As ions migrate from the gate into the channel, the channel's redox potential and conductivity were modulated. When no bias is applied to the gate electrode, there is a high energy barrier that decouples the gate from the channel, ensuring no change to the redox potential or conductivity state of the channel. The counter-redox stacked architecture acts as a reservoir of electrons (or holes) to change each respective films reduction (or oxidation) state and establishes a fully reversible system.

Stacking the roll-to-roll printed oxidized S-PEDOT film and the reduced S-PEDOT:PEI film over a gel electrolyte film, this device was capable over over 500 distinct tunable states by voltage pulsing the gate at ± 1 V with a pulse duration of 1 sec. demonstrating a resolution of ± 0.136 μS of change per input. This work presented the linear tunability of a counter-redox reaction by varying the input voltage parameters. The predictable trend of conductivity states this device exhibited lead to the ease of design for implementing common integrated circuit operations. With the demand of device's with low power consumption per input, this S-PEDOT device demonstrated an energy of 0.31 pJ/mm^2 at optimized voltage pulsing. While not nearly comparable to that of biological synaptic power consumption, it is theorized that advanced printing techniques could lead to a power consumption on the order of 0.1 fJ for a 20 μm S-PEDOT-based device. Biological mimicry, in

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the form of the short-term memory mechanism referred to as paired-pulse facilitation/depression, was implemented to demonstrate the synaptic emulation capabilities of the S-PEDOT-based device. This paired-pulse phenomena is a biological characteristic measuring the effect the timescale between two incoming stimuli have on the strength of output signal. The S-PEDOT-based device exhibited a higher change in its conductivity state with a short timescale between the two pulses and a low change in conductivity with a relatively large timescale between pulses, a similar trait to that biological synapses. Along with device characteristics and biological mimicry, the S-PEDOT device was used to demonstrated simple elementary algebra, specifically the operations of addition, subtraction, multiplication and division. Addition and subtraction are achieved for this S-PEDOT device where positive voltage input pulses programmed to the gate (+V increases current and decreases conductivity) is analogous to addition, whereas subtraction is realized with negative voltage pulsing. Multiplication can be described as repeated addition/subtraction steps with equal groupings. Lastly, while division proved to be less straightforward than addition, subtraction and multiplication, it was implemented through a counting of the repeated units of subtraction method. To display more applications, the S-PEDOT device was used to demonstrate the Boolean logic gates of AND, OR, NAND and NOR where one single S-PEDOT device can function as all four gates based on the voltage parameters input to the device. This data points to three-terminal electronic devices based on redox-active electrochemical materials as key candidates for future neuromorphic computers or integrated circuit systems.

Development of non-conformal memristive devices. Extending the research established with the three-terminal conjugated polymeric electrochemical memristor design, a simple two-step vapor phase polymerization technique was employed to fabricate conformal and non-conformal devices. The vapor phase polymerization was achieved with an iron-salt oxidant of iron (III) *p*-toluenesulfonate hexahydrate coating over either an ITO-coated glass or a commercially purchased toy car in order to oxidatively polymerize polypyrrole (PPy) as the electrochemical species. Unlike the ITO-coated glass, the toy car was templated with aluminum (Al) electrodes via thermal evaporation and final connections were ensured using copper tape tied to the Al electrodes. By coating any substrate with an iron-salt oxidant, oxidative polymerization can be achieved in the form of vapor phase polymerization after exposing the oxidant-coated substrate to monomer vapor. Reported electrochemical monomers are vaporized around 90 °C under approximately 30 inch of Hg pressure. This technique was used to demonstrate the application for the electrochemical material known as

PPy for both conformal (glass slide) and non-conformal (toy car) substrates. With a high demand to integrate smart technology into the day-to-day world around us, demonstration of varying electronic devices over non-conformal substrates are necessary. To implement this, a PPy-based three-terminal device is fabricated by vapor phase polymerization over the non-conformal, commercially purchased toy car. The toy car device was capable of simple potentiation and depression cycling and, therefore, addition and subtraction operations. As for the ITO-based PPy device, an ultra-low power consumption on the order of 4.16 fJ/mm^2 was achieved per input pulse (V = ± 50 mV, t$_{pulse}$ = 100 msec.), mimicking that of actual biological synaptic and neuronal responses. Implementing current state-of-the-art depositing and printing techniques, such a roll-to-roll and lithography, such devices can be easily mass-produced as well as scaled down in size to further decrease energy consumption. While this device does not employ a counter-redox architecture, the stack of PPy/electrolyte/PPy still operates in a similar manner to that of its S-PEDOT counterpart. Without the asymmetry of the counter-redox architecture, the device does not exhibit a perfect linear trend when varying its input parameters, however, there is still a predictable response that can be utilized in designing Boolean and elementary algebra operations. This PPy-based three-terminal device exhibits a resolution of ± 0.2452 μS per input pulse with parameters of ± 1 V pulsing at a 1 sec. duration. A slight deviation from the device design for the S-PEDOT-based system was necessary for the PPy-based system where a 1 MΩ resistor is tied in series to the input voltage electrode. This resistor acts as a current limiter to the input bias. At lower resistance, this device exhibited electrochromic behavior with full transitions of its optical state, from transparent to opaque observed within one single pulse, as well as exhibiting an asymmetric tuning behavior. To aid in this effort, a high resistor value is chosen to properly limit the current and ensure the driving force of the device is capable to tuning the redox potential across the device's architecture rather than overloading the system.

Implementation of flexible memristors toward advanced operational integrated circuits. Building upon the results of the device architecture of the three-terminal S-PEDOT device and the vapor phase polymerization technique for PPy, a dithienopyrrole-based monomer, notably referred to as 4-(6-hexyl)-4H-dithieno[3,2-b:2',3'-d]pyrrole (6DTP), was synthesized and used for further testing. To verify the success of this technique, both theoretical calculations and experimental results were used in order to confirm the accuracy of polymerization as this was the first report of any DTP species synthesized via vapor phase polymerization. Theoretical calculations using density functional theory (DFT) determined the energy levels for 6DTP's monomer, trimer,

and pentamer units for its highest occupied- and lowest unoccupied molecular orbital (HOMO and LUMO). The pentamer repeating unit for 6DTP was chosen as a sufficient candidate for DFT calculations as reports state energy levels converge and saturate, leading to similar resulting energies for any system past 4 - 6 repeating units. The HOMO and LUMO energy levels were experimentally derived using cyclic voltammetry to analyze oxidation and reduction peaks (to obtain HOMO) and UV-Vis spectroscopy to measure the photo-physical absorbance (to obtain ΔE_{UV}, further used to calculate LUMO) of the vapor phase polymerized p6DTP thin films. As expected, the theoretical energy levels were near-perfect matches in comparison to that of the observed experimental values, confirming the success of this technique in the creation of p6DTP films. Device fabrication of a three-terminal system employed both vapor phase polymerization techniques for creating the p6DTP films in addition to screen printing the silver (Ag) electrodes and the gel electrolyte layer. This electronic synaptic-emulating p6DTP-based device demonstrated a power consumption of 1 pJ/mm^2 per synaptic input at parameters of ± 100 mV with a pulse duration of 100 msec. While this does not meet the requirement of perfect synaptic emulation, this result could be further decreased by either varying the voltage parameters of the input terminal (V $< \pm 100$ mV, t$_{pulse} < 100$ msec.), tuning the polymer species (addition of electro-active moieties off of the polymer backbone), or tuning the device architecture (configuring toward a counter-redox architecture). The device was proven to exhibit reproducible analog conductivity tuning traits with over 500 distinct and linear states and a resolution of ± 0.04 μS per input, leading to its use as a future neuromorphic computer. Along with the ability to perform information processing (Boolean and elementary algebra) like the S-PEDOT- and PPy-based devices, this was the first implementation of any memristive system used as a combinational logic circuit in current literature at the time. Knowing that a single three-terminal conjugated polymeric electrochemical memristor can demonstrate single Boolean logic gate behavior with the correct input parameters, a combination of two devices tied in series was demonstrated to perform the function of two AND gates tied in series with each other. To achieve this, the output terminal of the first AND gate device was tied to the input of the second AND gate device. By properly modifying the voltage input parameters, the combinational logic gate was achieved for this p6DTP-based system. While this achieved advanced integrated circuit operation, there is much work left to be done before we see the current memristive systems implemented into actual commercial based technologies.

5.2 Theoretical Implications and Recommendations for Further Research

The need to circumvent or re-invent current von-Neumann-based architecture is implicitly based on the physical limitations of current state-of-the-art transistor technology. Recently, IBM has designed chips with a 2 nm design per transistor, nearly reaching the physical limitation where atomistic transistors will be the limiting factor. While the amount of transistors on a chip has approximately doubled every two years based on Moore's law, this has lead to a drastic increase to the processing power consumed per device. Memristors are a possible candidate for the transistors replacement as memristors can perform information processing and data storage in one device, emulating that of biological systems. Memristors operate as nonvolatile resistive tuners where, when no bias is applied, the last programmed state is retained (data storage) and the application of changing states can be related to short-term and long-term memory effects (information processing). While many reports focus on the design and characterization of memristive systems, there is a demand for pushing the boundary and designing fully functional integrated chip packages or further advanced operational applications for these devices. To that end, screen printing and other printing techniques can be utilized to print either chip packages or neural networks. While many memristive systems have been shown to demonstrate neuromorphic capabilities, such as pair-pulse facilitation, spike-timing-dependent-plasticity, and Pavlovian learning behaviors, there is still the demand to display the actual use of these devices in order to replace their transistor counterparts. Neuromorphic devices will have an impact on future biomedical devices, desired due to their biocompatibility, soft mechanical properties, and inherent sensitivity. Coupling biological systems and organic active layers pave the way forward toward adaptive neuromorphic systems that demonstrate direct feedback and control from its environment. This implies the desire for smart neuromorphic biosensors that can sense, control, and respond to different stimuli from the environment in an optimized and predictable manner. This desire is driven by the demand for smart drug delivery systems and smart neuroprosthetics.

Organic materials, specifically the classification of redox-active electrochemical conjugated polymers, are a primary candidate for future two- and three-terminal based memristive systems. Three-terminal based electrochemical memristors allow for an added degree of freedom for a different variety of applications in comparison to their two-terminal counterparts. These three-terminal

systems excel at endurance and reliability of their conductivity state as the write and read operations are decoupled and provide low-energy operations for these processes without any interference between each other. Organic redox electrochemical polymers can be tuned between their oxidized (doped) and reduced (dedoped) state, leading to a wide range of conductive switching analog tuners. The ability to rationally design these conjugated polymers allows the adjustment of the switching voltage, switching speeds, endurance, and shelf life of these materials, which are often inferior to that of their inorganic analogs. With this in mind, design of future redox-active polymers are required where tailoring their properties are a key requirement for research as materials scientists. Theoretical and predictive design can be achieved through density functional theory (DFT) calculations and machine learning, where tuning the electronic bandgap (and therefore HOMO and LUMO energy values) will provide future possible avenues to designing neuromorphic computers. To that end, strictly referring to DTP-based chemistries, electro-active species can be chemically attached to the polymer backbone in order to adjust the base-materials properties. It has already been demonstrated for a DTP polymer backbone attached with a carbazole moiety that was capable of emulating spike-timing-dependent-plasticity in the form of a two-terminal device. This is only the beginning step, where many other possible moieties can be attached to further decrease the device's power consumption or increase the biocompatibility where connections between organic electronic devices will couple to that of biological systems. It is imperative to rationally design and tailor redox-active electrochemical conjugated polymers with the device's architecture and configuration in mind.

Appendices

Appendix A   Glossary

LRS, low-resistance state;

HRS, high-resistance state;

0, OFF *or* FALSE;

1, ON *or* TRUE;

G, gate;

D, drain;

S, source;

DS, channel;

DS, channel (drain / source);

q, electronic charge;

ϕ, magnetic flux;

M, memristance;

V, voltage;

i, current;

R, resistance;

t, Δt, t_{pulse}, time;

w, set of state variables;

Redox, oxidation-reduction potential;

PEDOT, poly(3,4-ethylenedioxythiophene);

PPy, polypyrrole;

PANI, polyaniline;

ECP, electrochemical polymerization;

Ag/AgCl$_3$, silver/silver chloride;

KCl, potassium chloride;

SHE, standard hydrogen electrode;

SCE, saturated calomel electrode;

Ag/AgNO$_3$, silver/silver nitrate;

NBu$_4$, tetrabutylammonium;

$[B(C_6F_5)_4]^-$, dimethylanilinium;

$[PF_6]^-$, hexafluorophosphate;

$[BF_4]^-$, tetrafluoroborate;

$[ClO_4]^-$, perchlorate;

WE, working electrode;

RE, reference electrode;

CE, counter electrode;

Fc, ferrocene;

Fc^+, ferrocenium;

VPP, vapor phase polymerization;

VDP, vapor deposition polymerization;

CVD, chemical vapor deposition;

$FeCl_3$, iron (III) chloride;

EDOT, 3,4-ethylenedioxythiophene;

cPECM, conjugated polymeric electrochemical memristor;

OECT, organic electrochemical transistor;

PEDOT:PSS, poly(3,4-ethylenedioxythiophene):poly(4-styrenesulfonate);

OFET, organic field-effect transistor;

PDBT-*co*-TT, poly(thienothiophene-co-1,4-diketopyrrolo[3,4-c]pyrrole;

TBAP, tetrabutylammonium perchlorate;

R2R, roll-to-roll;

S-PEDOT, poly(sodium 4-((2,3-dihydrothieno [3,4-b][1,4]dioxin-2-yl)methoxy)butane-2-sulfonate);

PEI, polyethyleneimine;

S-EDOT, sodium 4-[(2,3- dihydrothieno[3,4-b][1,4]dioxin-2-yl)methoxy]butane-2-sulfonate;

PEG, poly(ethylene glycol);

Bu_4NPF_6, tetrabutylammonium hexafluorophosphate;

i_{ds}, channel current;

V_{ds}, channel voltage;

V_g, gate voltage;

ITO, indium tin oxide;

PET, polyethylene terephthalate;

σ, conductivity;

PPF, paired-pulse facilitation;

τ_1, τ_2, relaxation timescale;

C_1, C_2, unitless magnitude;

PCC, percent current change *or* percent conductivity change;

A, B, mathematical input value;

C, mathematical output value;

r_1, r_2, r_3, r_4, r_5, remainder values;

n_1, n_2, n_3, counting values;

Q, quotient.

ANN, artificial neural network;

DI, deionized;

PEGMA, polyethylene glycol methacrylate;

PEGDMA, polyethylene glycol dimethacrylate;

DEAP, 2,2-diethoxyacetophenone;

FET, field-effect transistor;

CP, conjugated polymer;

FeToS, iron(III) p-toluenesulfonate hexahydrate;

Py, pyrrole;

MeOH, Methanol;

N_2, nitrogen;

V_{pre}, pre-synaptic terminal voltage;

V_{post}, post-synaptic terminal voltage;

PCB, printed circuit board;

SMD, surface mounted device;

Al, aluminum;

i_{pre}, pre-synaptic terminal current;

i_{post}, post-synaptic terminal current;

R_{CL}, current limiting resistor;

t_{pulse}, t_{off}, Δt, time;

G, G_o, G_n, ΔG, conductivity;

PPD, paired-pulse depression;

T, TRUE;

F, FALSE;

DI-H_2O, deionized water;

SMU, source measurement unit;

CPU, central processing unit;

ECM, electrochemical material;

STDP, spike-timing-dependent-plasticity;

SP, screen printing;

DTP, dithienopyrrole;

6DTP, 4-(6-hexyl)-4H-dithieno[3,2-b:2',3'-d]pyrrole;

pDTP, poly(dithienopyrrole);

FeOtf, iron trifluoromethane sulfonate hexahydrate;

FeToS, iron tosylate hexahydrate;

PEG-PPG-PEG, Polyethylene glycol-$block$-polypropylene glycol-$block$-polyethylene glycol;

AA, active area;

p6DTP, poly(4-(6-hexyl)-4H-dithieno[3,2-b:2',3'-d]pyrrole);

CV, cyclic voltammetry;

E_0, onset potential;

IP, ionization potential;

HOMO, highest occupied molecular orbital;

λ_{max}, maximum absorption;

E_{UV}, optical electronic bandgap;

LUMO, lowest unoccupied molecular orbital;

LTP, LTD, long-term potentiation/depression;

P, energy;

E, intensity;

A•B, AND gate;

¬A•B, NAND gate;

A+B, OR gate;

¬A+B, NOR gate;

D_1, D_2, device 1 and 2;

Appendix B   NMR Monomer Characterization
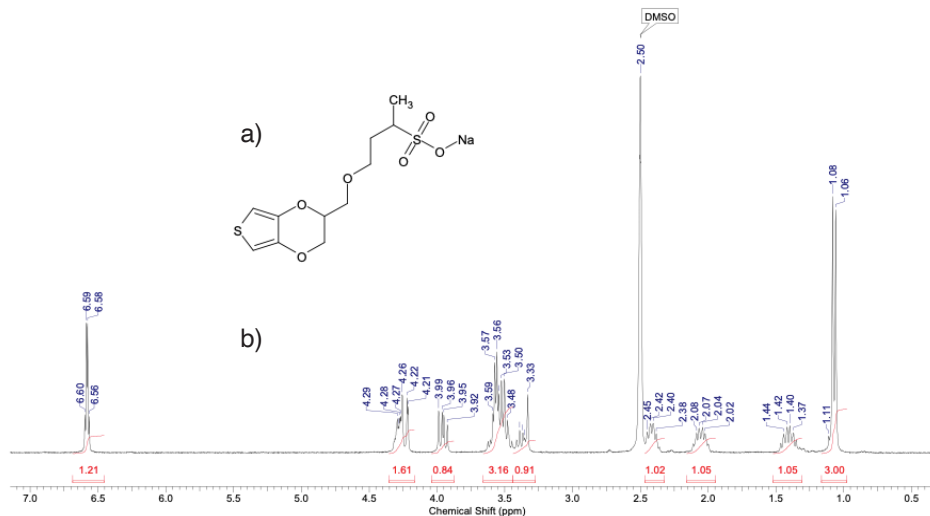
Figure 1:   NMR characterization of S-EDOT monomer: **a)** Chemical structure of S-EDOT monomer and **b)** ^{1}H NMR.

All the solvents used for reactions were distilled under argon after drying over an appropriate drying reagent. ^{1}H NMR spectra were recorded on a JEOL ECX-300 spectrometer. Chemical shifts for protons are reported in parts per million downfield from tetramethylsilane and are referenced to residual protium in the NMR solvent (CDCl$_3$: δ 7.26 ppm) (*cf.* **Figure 1**). Yield 69%, dark blue paste.
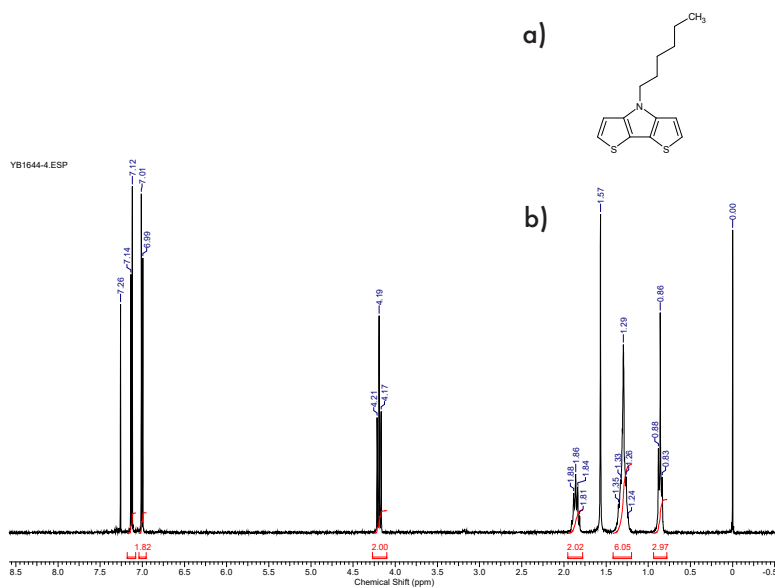
Figure 2: NMR characterization of 6DTP monomer: **a)** Chemical structure of 6DTP monomer and **b)** ^{1}H NMR.

All the solvents used for reactions were distilled under argon after drying over an appropriate drying reagent. ^{1}H NMR spectra were recorded on a JEOL ECX-300 spectrometer. Chemical shifts for protons are reported in parts per million downfield from tetramethylsilane and are referenced to residual protium in the NMR solvent (*cf.* **Figure 2**). ^{1}H NMR (CDCl$_3$, δ, ppm): 0.86 (t, 3H, $J = 6.9$ Hz), 1.29 (m, 6H), 1.86 (m, 2H, $J = 7.2$ Hz), 4.19 (t, 2H, $J = 7.2$ Hz), 7.01 (d, 2H, $J = 5.2$ Hz), 7.12 (d, 2H, $J = 5.2$ Hz). Yield 92%, yellow solid powder.

Appendix C   Various S-PEDOT Characteristic Experiments
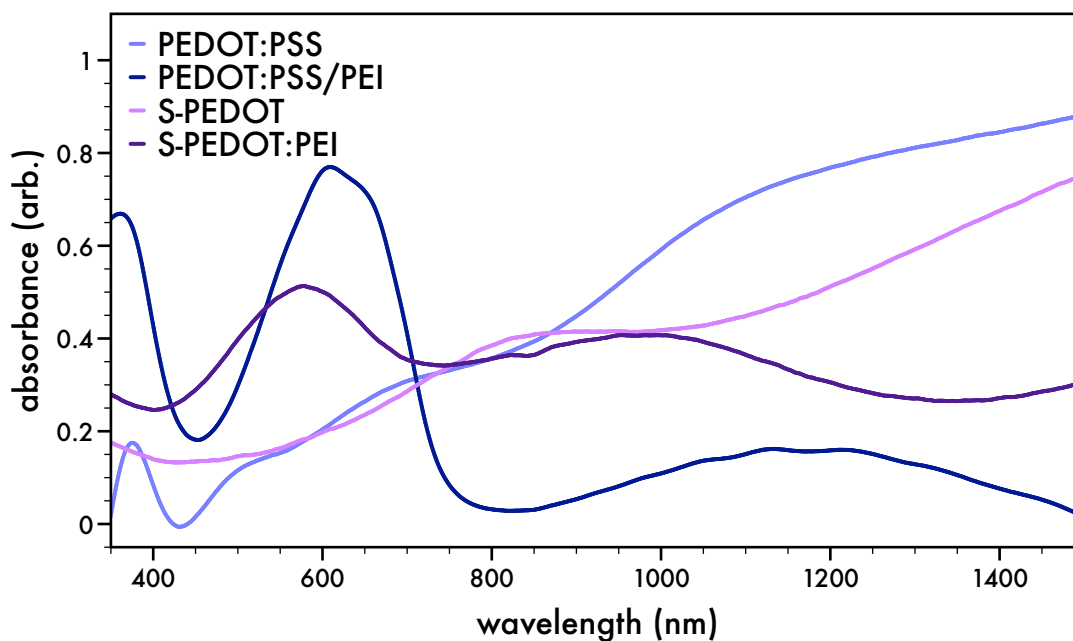
Figure 3:   Absorbance measurements of commercial PEDOT:PSS (light blue), chemically reduced PEDOT:PSS doped with PEI (dark blue), S-PEDOT (light purple), and chemically reduced S-PEDOT doped with PEI (dark purple).

The photo-physical optical behavior for both the commercially purchased PEDOT:PSS and S-PEDOT are shown in **Figure 3**. Both PEDOT:PSS and S-PEDOT films are spun cast and had a final film thickness of ca. 200 nm. Another set of PEDOT:PSS and S-PEDOT are chemically reduced by exposing to vapor of branched polyethyleneimine (PEI) at 250 °C for 10 min. The oxidized films PEDOT:PSS and S-PEDOT exhibit broadband absorption past ca. 800 nm and is indicative of a highly oxidized system. The reduced films display a diminished effect to the broadband absorption and have a maximum peak appear at 608 and 576 nm, respectively for PEDOT:PSS:PEI and S-PEDOT:PEI. This was a demonstration to display the redox potential for the S-PEDOT polymer compared to its commercial analog.
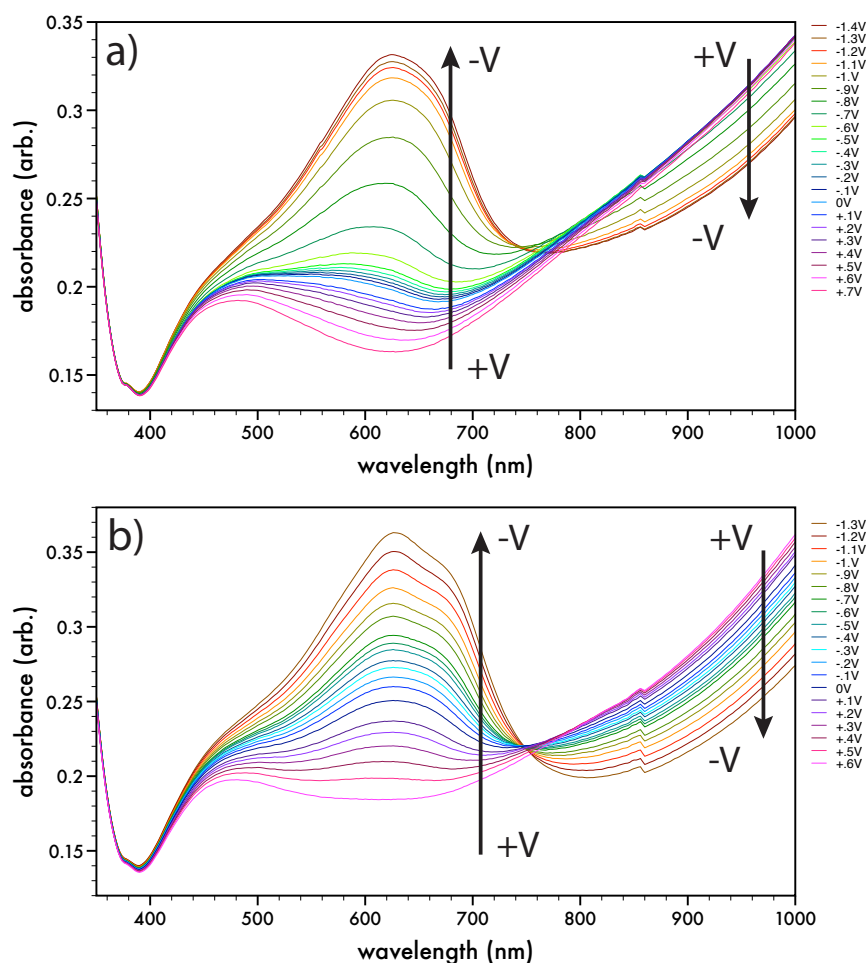
Figure 4: Absorbance measurements for **a)** ITO / electrolyte / S-PEDOT / ITO and **b)** ITO / electrolyte / S-PEDOT:PEI / ITO devices exhibiting electrochromic behavior.

The electrochromic behavior for both the S-PEDOT (oxidized) and S-PEDOT:PEI (reduced) films are demonstrated in **Figure 4**. In a two-terminal configuration (ITO/electrolyte/polymer/ITO), one ITO electrode is tied to ground while the other is applied with a voltage, sweeping from positive to negative values. At the positive values, both devices exhibit a low absorbance value around This is a demonstration of the redox potential tunability of each film where the maximum -V displays the film's reduced form and the maximum +V displays the film's oxidized form. The S-PEDOT film (*cf.* **Figure 4**a) has a maximum absorbance value (-1.4 V applied) of ca. 620 nm. The S-PEDOT:PEI film (*cf.* **Figure 4**b) exhibits a maximum absorbance (-1.3 V applied) red shifted toward ca. 630 nm with a shoulder at ca. 670 nm.

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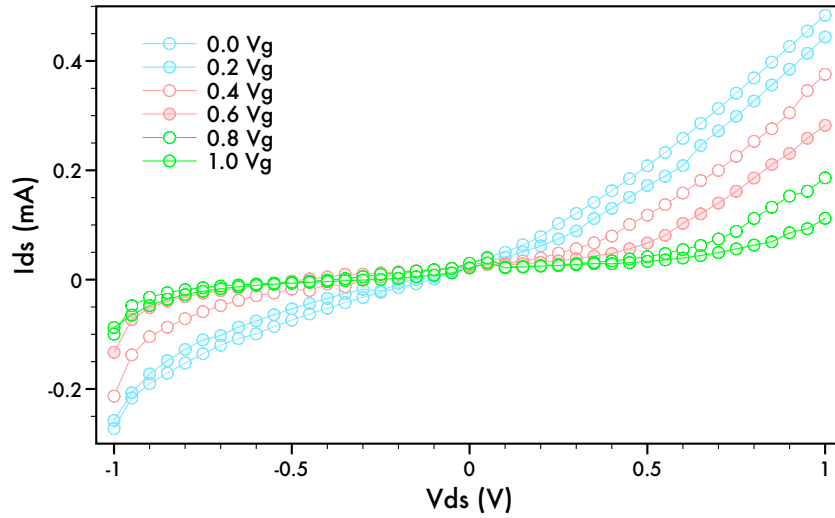
Figure 5: Organic Electrochemical Transistor Characteristics: i_{ds}-V_{ds} output characteristics for varying positive V_g potentials.

The output curve for the S-PEDOT is demonstrated in **Figure 5**. While holding the gate voltage (V_g) at a constant potential (ranging from 0 V to 1 V in increments of 0.2 V), the current response across the channel (i_{ds}) is monitored while sweeping the voltage of the channel (V_{ds}) from -1 V up to +1 V. It is observed that with no bias to the gate (blue) the device exhibits a fairly linear behavior, similar to that of a resistor. With increasing bias to the gate, the change in i_{ds} is diminished but has curvature while demonstrating a rapid increase to i_{ds} at higher V_{ds} values. This demonstrates that the current embodiment of the S-PEDOT device operates in depletion mode, meaning the device is considered to be ON when there is no gate bias applied and considered OFF when there is a bias applied to the gate.
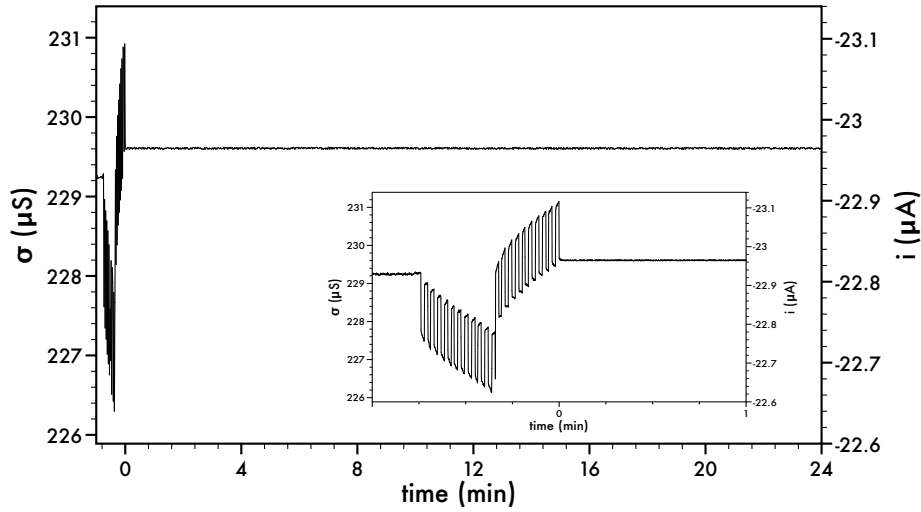
Figure 6: S-PEDOT Retention Characteristics: Retention time observed for 24 min after a single set of 10 -500 mV for 1000 msec pulses to the gate electrode (V_g), while the inset presents an expanded view. Over 24 min, there is a 0.0175% decrease in the channel current, i_{ds}, observed after the last pulse applied.

The S-PEDOT device's retention and state stability are demonstrated in **Figure 6**. This pulse data portrays the characteristic signal response exhibited prior to extrapolating each current or conductivity state. Retention was measured after a cycle of 10 +V_g followed by 10 -V_g pulses with a continuous V_{ds} application of -100 mV. After the application of -500 mV pulses with a duration of 1000 msec., the device was held with a constant V_{ds} to observe state stability over a 24 min. time period. Within the first 10 sec. after pulsing, there was a 0.002483% drift, a 0.0073% drift after 10 min., and a 0.0175% drift after 24 min. after pulsing.

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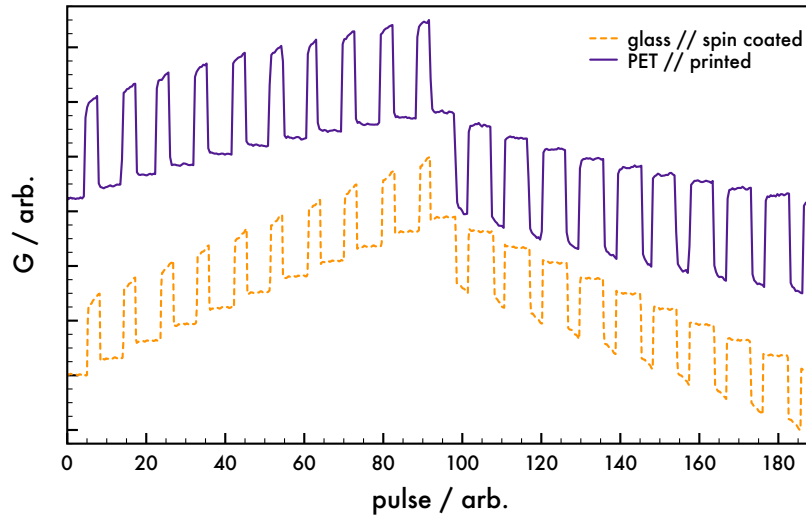
Figure 7: Varying device substrate: Glass spin coated (orange) and PET R2R printed (purple) with S-PEDOT.

Device's with the counter redox architecture (S-PEDOT/electrolyte/S-PEDOT:PEI) were fabricated via spin coating over ITO-templated glass and roll-to-roll gravure printing over PET flexible substrates. **Figure 7** demonstrates the similarity of the two device's plotted as a normalized conductivity measured across the drain and source polymer film (S-PEDOT:PEI). These two different devices demonstrate a similar linear change to their conductivity state, the observed amplitudes appear different. This is well within benchtop fabricated device tolerance as device variations appear from human error or changes in fabricated environment (relative humidity, room temperature, etc.).

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