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Enhancing the Performance of Poly(3-Hexylthiophene) Based Organic Thin-Film Transistors Using an Interface Engineering Method

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ENHANCING THE PERFORMANCE OF POLY(3-HEXYLTHIOPHENE) BASED ORGANIC THIN-FILM TRANSISTORS USING AN INTERFACE ENGINEERING METHOD

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ABSTRACT

An original design and photolithographic fabrication process for poly(3-hexylthiophene-2, 5-diyl) (P3HT) based organic thin-film transistors (OTFTs) is presented. The structure of the transistors was based on the bottom gate bottom contact OTFT. The fabrication process was efficient, cost-effective, and relatively straightforward to implement. Current–voltage (I-V) measurements were performed to characterize the primary electronic properties of the transistors. The measured mobility of these transistors was significantly higher than most results reported in the literature for other similar bottom gate bottom contact P3HT OTFTs. The higher mobility is explained primarily by the effectiveness of the fabrication process in keeping the interfacial layers free from contamination, as well as the proper annealing of the P3HT.

An interface engineering method is investigated to further enhance the performance of the OTFTs. Three interfacial materials were used for this purpose: graphene oxide (GO), poly(oligo (ethylene glycol) methyl ether methacrylate- glycidyl methacrylate- lauryl methacrylate) (P(OEGMA-GMA-LMA)) or POGL, and a composite of GO and P(OEGMA-GMA-LMA) or GO-POGL. The OTFTs with a GO interfacial layer were observed to have a higher drain current and field-effect mobility than the OTFTs with no interfacial layer. The enhanced drain current and mobility are associated with the particular structure of the P3HT layer on the dielectric surface and the reduction in the contact resistance between the GO-covered electrodes and the P3HT. The OTFTs with a POGL interfacial layer were observed to have a smaller threshold voltage than the OTFTs with no interfacial layer. The POGL OTFTs were also observed to have much more ideal drain

current saturation characteristics with very small I-V curve slope. This is explained by the deep trap states on the POGL surface and the reduction of the contact resistance at the electrode/organic semiconductor interface. The OTFTs with a GO-POGL composite layer were observed to have a higher drain current and mobility, and a smaller threshold voltage than the OTFTs without an interfacial layer, which is the optimum case for these two device parameters. The higher drain current and field-effect mobility are attributed to the larger interconnecting grains of the P3HT that is deposited onto the GO-POGL surface and the smaller interfacial tension between the GO-POGL and the P3HT. The smaller threshold voltage is attributed to the deep trap states on the GO-POGL layer and the smaller contact resistance between the GO-POGL modified electrodes and the P3HT. Furthermore, experiments that could be performed to advance this research work and enhance the performance of the OTFTs even further are proposed.

DEDICATION

I would like to dedicate this dissertation to my parents, Negussie Tarekegn and Hamelmal Yigzaw, and my brother, Rediet N. Tarekegn. I am extremely grateful for their unconditional love, patience, and encouragement. I cannot imagine doing this without their support. I am forever indebted to them.

I also would like to dedicate this dissertation to my uncle, Dr. Mulugeta Tarekegne. He has been a big supporter of my education from the very beginning. I am immensely grateful and blessed to have him in my life, and I am a better person because of it.

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CHAPTER ONE

INTRODUCTION

1.1 Introduction

Organic thin-film transistors (OTFTs) are attractive because of their enormous potential in applications where low cost, large surface area, and flexible structures are required. Some of the most widely used applications of OTFTs are flat panel displays [1], sensors [2], radio frequency identification (RFID) tags [3], and medical device applications [4]. OTFTs have come a long way since they were first reported in 1986 [5], and particularly in the past two decades there has been significant progress in the fabrication process and performance of OTFTs. However, their performance is still not on a par with their inorganic counterparts. In particular, the field-effect mobility and switching speed of OTFTs are lower, and the interfacial stability at the dielectric/semiconductor and electrode/semiconductor interfaces is much lower than in Si-based devices, especially with regards to trapped charge and interface states. Thus, it is clear that the interfaces in these devices have a crucial effect on their operation and stability.

The primary objective of this work was to investigate the effects of different interfacial layers, at the electrode/organic semiconductor and dielectric/organic semiconductor interfaces, on the operation and performance of OTFTs. The initial goal was to design a fabrication process for poly(3-hexylthiophene-2, 5-diyl) (P3HT) based OTFTs that is efficient, cost-effective, and relatively straightforward to implement. Once consistent and high performing OTFTs were produced, the main objective was to

investigate the performance of the OTFTs using an interface engineering method. We have investigated three different interfacial materials to enhance the performance of OTFTs: graphene oxide (GO), poly(oligo (ethylene glycol) methyl ether methacrylate- glycidyl methacrylate- lauryl methacrylate) or P(OEGMA-GMA-LMA), and a composite of GO and P(OEGMA-GMA-LMA) (GO–P(OEGMA-GMA-LMA)). The GO interfacial layer improved the field-effect mobility of the devices. The P(OEGMA-GMA-LMA) layer significantly improved the threshold voltage of the devices. The GO–P(OEGMA-GMA-LMA) composite interfacial layers improved both the mobility and the threshold voltage of the devices. The details of these results are reported in this dissertation.

The dissertation is structured as follows. In Chapter 2, we discuss organic semiconductors. Organic semiconductors were discovered in 1976 [6]. They are based on sp^2 hybridization of carbon chains. Charge transport in organic semiconductors is different from its inorganic counterpart. The most widely accepted charge transport models are the variable range hopping model, the multiple trapping and release model, and the polaron model. The charge transport theory for each of these models is discussed in this chapter. Furthermore, the classification of organic semiconductors is discussed. Organic semiconductors are classified based on their structures as small molecules or polymers. They are also classified based on the type of charge they transport as n-type or p-type organic semiconductors.

In Chapter 3, the operating principles of OTFTs are discussed. The main performance parameters of OTFTs are threshold voltage, field-effect mobility, current on/off ratio, and subthreshold slope. The most attractive characteristics of OTFTs are low

threshold voltage, high mobility, low subthreshold slope, and high on/off current ratio. Each of these parameters are discussed in detail in this chapter. Moreover, we discuss the different models that are used to describe OTFTs. In particular, we discuss the compact DC model, the charge drift model, and the charge drift model for the subthreshold region.

In Chapter 4, the different structures of OTFTs are discussed. The most widely known structures are single gate, dual gate, vertical channel, and cylindrical gate OTFTs. The single gate OTFTs are further classified based on the location of the gate and the location of the source and drain contacts with respect to the organic semiconductor layer. These structures are known as top gate top contact (TGTC), top gate bottom contact (TGBC), bottom gate top contact (BGTC), and bottom gate bottom contact (BGBC). The top contact OTFTs usually have a better performance than the bottom contact OTFTs. This is because the top contact devices have a larger charge injection area and a lower contact resistance. However, the geometry of the bottom contact devices is the one that is most convenient for industrial applications.

In Chapter 5, we discuss interface engineering of OTFTs. Some of the most important interfaces in OTFTs are the source-drain electrode/organic semiconductor, dielectric/organic semiconductor, organic semiconductor/organic semiconductor, and organic semiconductor/environment interfaces [7, 8]. The two interfaces that play a critical role in the performance of OTFTs are the electrode/organic semiconductor and the dielectric/organic semiconductor interfaces [8]. The impact of these two interfaces is discussed in detail in this chapter. The electrode/organic semiconductor interface is responsible for the injection of charges from the electrode into the organic semiconductor,

and the dielectric/organic semiconductor interface is responsible for the transport of charge carriers in the channel of the device. Modifying these two interfaces by adding an extra material layer can increase the efficiency of the charge injection process from the electrode into the organic semiconductor and the charge transport across the conductive channel of the device. Furthermore, the interfacial materials that have been used for engineering the interfaces of OTFTs, as well as the interfacial materials used in this work, are presented.

In Chapter 6, an original design for a P3HT based OTFTs is presented. The materials and chemicals that are used to fabricate the OTFTs are also presented. The preparation of the P3HT solution and the reasons for the selection of the electrode material are discussed in detail. The interfaces of the OTFTs were modified to enhance their performances. Thus, a design for the modified OTFTs is also presented in this chapter.

In Chapter 7, We presented a photolithography fabrication process for P3HT based OTFTs. The first section describes the need for the photolithography fabrication process. The second section lists all the instruments that are used to fabricate the devices. The remaining four sections describe the fabrication processes. Specifically, the deposition of the gate contact, the deposition and patterning of the drain and source contacts, the deposition of the P3HT, and the patterning of the P3HT to form a conductive channel.

In Chapter 8, the electrical characterization results of the P3HT based OTFTs are presented and discussed. The threshold voltage and the field-effect mobility of the devices are extracted. The measured mobility of the transistors was significantly higher than most results reported in the literature for similar bottom gate bottom contact P3HT based OTFTs.

The higher mobility is explained primarily by the effectiveness of the fabrication process and the annealing of the P3HT.

In Chapter 9, the effects of a GO interfacial layer on the performance of P3HT based OTFTs are investigated. The devices with the GO interfacial layer are observed to have a higher drain current and mobility than the devices with no interfacial layer. This is explained by the larger grain size of the P3HT deposited onto the SiO_2 surface which was previously covered with GO and the compatibility of the GO-modified electrodes with the P3HT.

In Chapter 10, the effects of a P(OEGMA-GMA-LMA) interfacial layer on the performance of P3HT based OTFTs are investigated. The devices with a P(OEGMA-GMA-LMA) interfacial layer are observed to have a lower threshold voltage than the devices with no interfacial layer. The P(OEGMA-GMA-LMA) devices also showed much more ideal drain current saturation characteristics with a smaller I-V curve slope in the saturation region. These results are explained by the deep trap states on the P(OEGMA-GMA-LMA) surface and the reduction of the contact resistance at the electrode/organic semiconductor interface.

In Chapter 11, the effects of a GO–P(OEGMA-GMA-LMA) or GO-POGL composite interfacial layer on the performance of P3HT based OTFTs are investigated. The devices with the GO-POGL interfacial layer are observed to have a lower threshold voltage, a higher drain current, and a higher mobility than the devices without an interfacial layer. The lower threshold voltage is explained by the deep trap states on the GO-POGL layer and the reduction of the contact resistance at the electrode/organic semiconductor

interface. The higher drain current and mobility are attributed to the particular morphology of the P3HT when deposited onto the GO-POGL layer on top of the SiO_2 surface, and also attributed to the interface interaction of the P3HT with the GO-POGL layer.

In Chapter 12, the final chapter, the results from previous chapters are summarized. Future work to enhance the performance of the OTFTs even further are proposed. Some of the proposed research works are investigating the effects of the channel length on the performance of the devices, and the effects of organic solvents on the crystallinity of P3HT.

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CHAPTER TWO

ORGANIC SEMICONDUCTORS

2.1 Introduction to Organic Semiconductors

Conductive polymers (or organic semiconductors) were discovered in 1976 [1]. They were discovered by H. Shirakawa, A. G. MacDiarmid and A. J. Heeger, which they received a Nobel Prize for in 2000 [2]. The discovery of organic semiconductors has attracted many researchers to a new era of research in organic electronics. Organic electronics is a branch of modern electronics that investigates and develops organic materials, and devices that contain organic materials as their main component [3]. Organic electronics have an immense potential in applications where flexible, large surface area, low-cost, solution processable and printed electronic devices are required [4-9]. The most successful organic electronics are organic photovoltaics [10-12], organic light emitting diodes [13-15], and organic thin-film transistors [16-18]. Other successful conductive polymer-based devices include polymer capacitors [19-21], organic photodiodes [22-24], and biosensors [25, 26].

Organic photovoltaics (OPV) is a type of photovoltaic that uses an organic material to absorb light and transport charges. The first working OPV cells were developed in the 1980s [27]. OPVs have a potential to provide electricity at a low-cost using earth-abundant materials. However, their efficiency is not yet at the level of their inorganic counterpart, and their operational lifetime is lower than their inorganic counterpart. The organic light emitting diode (OLED) is a light emitting diode that uses an organic material for its

emissive electroluminescent layer. The first efficient OLED was developed by C. W. Tang and S. A. VanSlyke at the research laboratory in Eastman Kodak in 1987 [28]. The large surface area of organic materials, as well as the ability to make them very thin, provide OLEDs an advantage over inorganic LEDs, such as thin light-fixture profiles, low light-source glare, uniform diffuse lighting, and high color rendering index [29]. The one thing that is keeping OLEDs from widespread commercial application is high cost. Currently a lot of research is being performed to reduce the cost of OLEDs [30, 31].

The organic thin-film transistor (OTFT) is a thin-film transistor whose active layer is made of an organic semiconductor. The first OTFT was reported in 1986, where polythiophene was used as the active material [32]. One of the advantages of OTFTs as compared to their inorganic counterparts is that their fabrication process is less expensive and complex. Most of the fabrication processes occur at room temperature and atmospheric pressure with less complex photolithographic patterning steps. However, the performance of OTFTs is still not on a par with their inorganic counterpart. Currently a lot of research is being performed to improve their performance. The focus of this dissertation is also to improve the performance of OTFTs.

Organic semiconductors are based on sp^2 hybridization of carbon chains. Carbon, as an element, has six electrons. The first two electrons fill the $1s^2$ orbital and are closely tied to the nucleus of the element. The remaining four electrons are known as valence electrons and are found in $2s^2 2p^2$ orbitals. In a carbon molecule, the valence orbitals hybridize to create a lower energy orbital known as hybrid orbital. There are three possible hybrid orbitals in carbon molecules: sp^3, sp^2, and sp orbitals. Organic semiconductors exhibit sp^2

hybridization. In sp^2 hybridization, out of the four valence electrons, three of them are located in the sp^2 orbital, and the fourth electron is located in the *2p* orbital, also known as the p_z orbital. The sharing of the sp^2 orbitals between two carbon atoms in a molecule results in the formation of a strong bond known as the σ bond. Since there are three sp^2 orbitals for the three valence electrons, we have three σ bonds spread in a shared plane with an angle of 120˚ between them [33]. The σ bonds hold the molecule together. The sharing of the two p_z orbitals, which are perpendicular to the plane formed by the three σ bonds, result in the formation of a weaker bond known as π bond. The electron configuration of the sp^2 hybridization is illustrated in Figure 2.1. The σ and π bonds have corresponding σ^* and π^* antibonds, respectively. The overlap between the bonding, σ and π, molecular orbitals and antibonding, σ^* and π^*, molecular orbitals result in their corresponding energy levels to split, leading to the formation of energy bands [33]. The gap between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) (These are analogous to the top of the valence band and the bottom of the conduction band in inorganic semiconductors, respectively) is known as the band gap energy (Eg). The band gap of organic semiconductors typically ranges from 1 to 4.9 eV [34]. The formation of the band gap in the p_z orbitals is illustrated in Figure 2.2. The π* state exists at a higher energy level than the π state as shown in the figure, and therefore $2p_z$ electrons occupy the π state (the lower energy level).

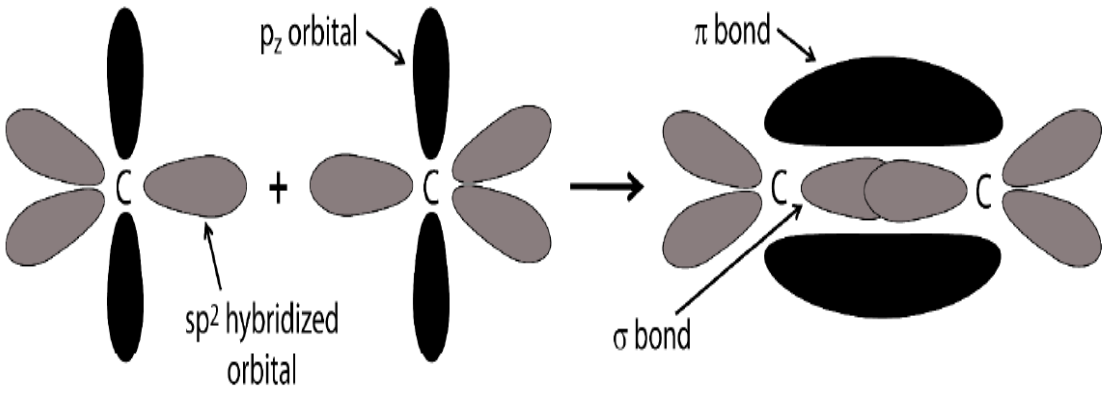

Figure 2.1: sp^2 hybridization of two carbon atoms [33]

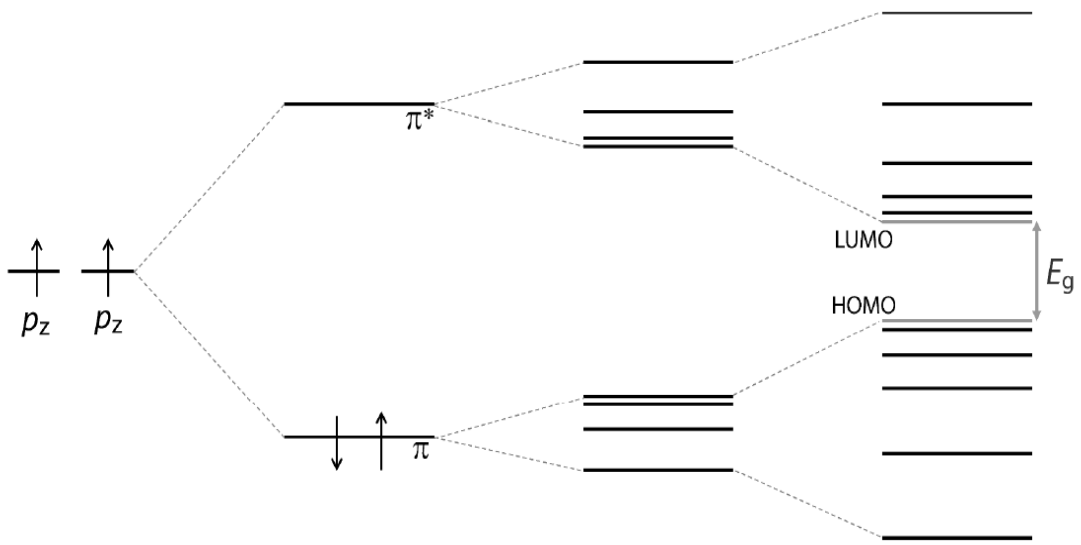

Figure 2.2: Schematic structure of the band gap energy in the p_z orbitals [33]

2.2 Charge Transport in Organic Semiconductors

The charge transport models of organic semiconductors are adapted and extended from amorphous inorganic materials due to their similar characteristics. The charge transport in organic semiconductors is affected by the morphology of the polymer chains, surface roughness, chemical impurity, and chemical interaction with the dielectric surface [33]. Thus, structural and energetic disorder is important in describing the charge transport model of organic semiconductors. Several charge transport models have been proposed for organic semiconductors, but the most accepted ones are variable range hopping model, multiple trapping and release model, and polaron model.

2.2.1 Variable Range Hopping Model

Organic semiconductors have a disordered molecular structure, similar to that of inorganic amorphous semiconductors such as amorphous silicon (a:Si). The molecules of organic semiconductors are held together by a weak intermolecular bond known as the Van der Waals force. Due to the weak intermolecular force and molecular disorder, the charge transport is restricted by traps in the localized states. This means that the charge carriers need to be thermally activated [35]. Thus, the charge carrier transport in organic semiconductors occurs by jumping from one localized state into another. This mechanism of charge transport is known as variable-range hopping (VRH). The concept of variable-range hopping was developed by M. Vissenberg and M. Matters in 1998, where a charge carrier jumps over a small distance with a high activation energy or jumps over a long distance with a low activation energy [36]. The schematic diagram of hopping charge

transport is illustrated in Figure 2.3. When a charge carrier jumps from one localized state into another, the energy difference is accommodated by either emitting or absorbing phonons [34, 35]. If the jump is from a lower state into a higher one, phonons are absorbed; if the jump is from a higher state into a lower state, phonons are emitted. Thus, charge transport in organic semiconductors is phonon assisted, while charge transport in metals and conventional semiconductors is limited by phonon scattering.

The intrinsic transition rate of a charge carrier hoping from a site p to an empty site q, γ_{pq}, is given by [37],

$$\gamma_{pq} = \gamma\left(R_{pq}, E_p - E_q\right) \tag{2.1}$$

where R_{pq} is the distance between the initial site p and the empty site q, E_p and E_q are the energy levels for sites p and q, respectively. The average transition rate between the two sites, Γ_{pq}, is given by [37],

$$\Gamma_{pq} = \langle n_p\left(1 - n_q\right)\gamma_{pq}\rangle \tag{2.2}$$

where n_p and n_q are the occupation numbers for sites p and q, respectively. The angular brackets represent an average over time.

The energy dependance of the intrinsic transition rate of charge carriers was developed by A. Miller and E. Abrahams [38], which is expressed as,

$$\gamma_{pq} = v_0 exp\left(-2\varphi R_{pq} - \frac{\theta(E_p - E_q}{K_B T}\right) \tag{2.3}$$

where v_0 is the attempt-to-jump frequency, φ is the inverse localized length of the inverse wave function, K_B is Boltzmann's constant, T is the temperature, and $\theta(x) = x\varepsilon(x)$ where $\varepsilon(x)$ is the step function.

The hopping of charge carriers in organic semiconductors is affected by the energy distribution among the trap states and the hopping distance [34]. At low bias, most of the charge carriers are trapped in the localized states. Thus, the system can be described by a network of resistors along with a conductance between sites p and q (G_{pq})[39], where $G_{pq} = G_0 e^{-S_{pq}}$. The system can be mathematically expressed as [36],

$$S_{pq} = 2xR_{pq} + \frac{|E_p - E_F| + |E_q - E_F| + |E_p - E_q|}{2K_B T} \tag{2.4}$$

where x is an effective overlapping parameter, E_F is the fermi level energy, and E_p and E_F are the corresponding energy levels for sites p and q. The first right hand side term describes the tunneling process between sites p and q, and the second term describes the activation energy that is required to jump from site p to site q.

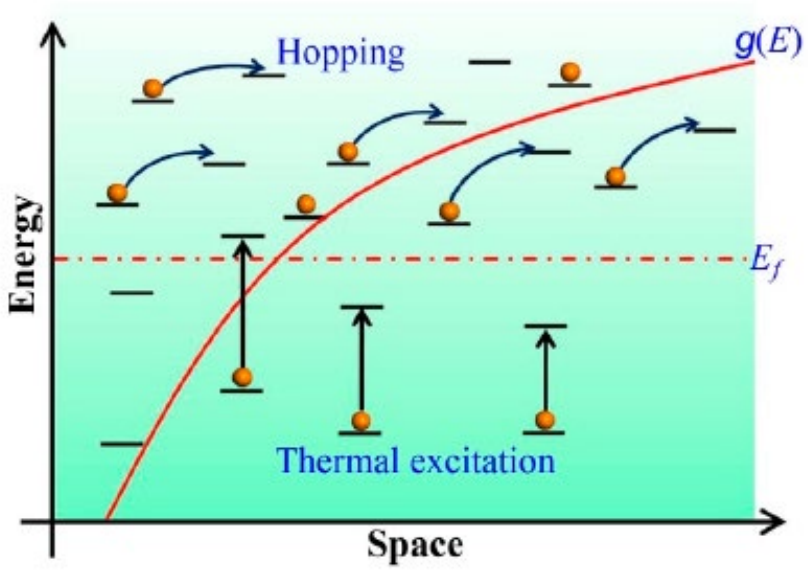

Figure 2.3: Schematic diagram of hopping charge transport with the density of states [35]

2.2.2 Multiple Trapping and Release Model

The multiple trapping and release (MTR) model was first reported in 1984 to describe the mobility of hydrogenated amorphous silicon (a-Si:H) [40]. It was later used to describe the charge carrier transport in organic semiconductors due to their similar structural and molecular disorders [41]. The MTR model is based on the following three assumptions: the trap sites are highly localized and the charge carriers trapped in these localized states cannot move easily from these states in the energy bandgap; charge carriers arriving at the trap sites are immediately captured with a probability close to one; and the release of the trapped charge carriers is a thermally activated process [42]. The charge transport occurs in the extended states (or transport band) and if the energy level of the traps is slightly lower than the mobility edge (or band edge), the extended states act as shallow traps and charge carriers can be released by a thermal excitation [35]. If the trap energy is far below the band edge energy, then the extended states act as deep traps, and the charge carrier cannot be released by a thermal excitation. The multiple trapping and release model is illustrated in Figure 2.4.

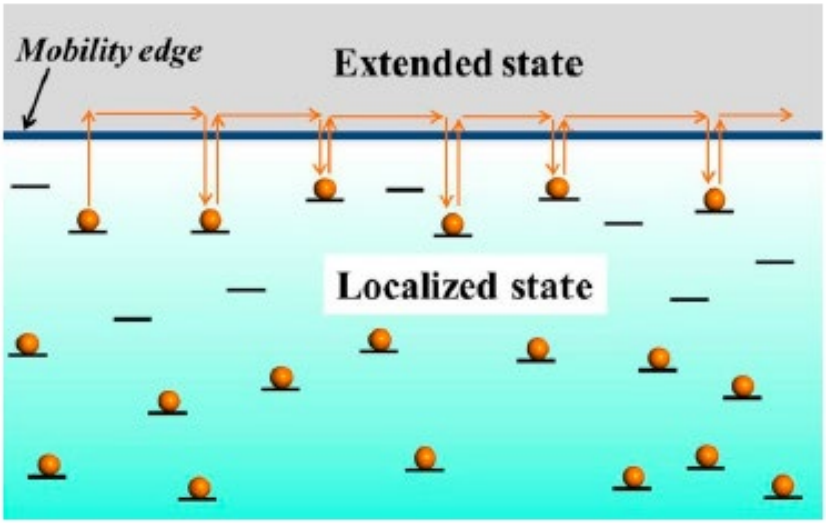

Figure 2.4: Schematic diagram of multiple trapping and release transport model [35].

In the MTR model, the total charge carrier concentration, n_{total}, is the sum of the free charge carrier concentration, n_f, and the trapped charge carrier concentration, n_T. Thus, the total charge carrier concentration is expressed as [43]

$$n_{total} = n_f + n_T \tag{2.5}$$

where n_f and n_T are given by:

$$n_f = N_C exp\left[\frac{-(E_C - E_F)}{K_B T}\right] \tag{2.6}$$

$$n_T = N_T exp\left[\frac{-(E_T - E_F)}{K_B T}\right] \tag{2.7}$$

where N_C is the effective density of states at the conduction edge, N_T is the effective density of states for the trap sites, E_C is the energy level of the conduction band, E_T is the energy level of the trap, and E_F is the fermi energy level.

In the field-effect transistors, which are one of the applications of organic semiconductors, the effective mobility of charge carriers in the MTR model depends on

the gate voltage [42]. When a voltage is applied at the gate, a potential develops at the organic semiconductor/dielectric interface, which shifts the fermi level towards the mobility edge (or band edge). Shifting the charge carrier energy towards the band edge helps to release the trapped charge carriers through thermal excitation. Thus, the effective charge carrier mobility, μ_{eff}, is given by,

$$\mu_{eff} = \mu_0 \frac{N_C}{N_T} \left[\frac{C_{ox}(V_{GS}-V_{Th})}{qN_T}\right]^{\frac{T_C}{T}-2} \tag{2.8}$$

where μ_0 is the mobility in the extended state or mobility in the absence of traps, C_{ox} is the gate insulator or dielectric capacitance per unit area, V_{GS} is the gate voltage, V_{Th} is the threshold voltage, q is the elemental charge, and T_C is the characteristic temperature which describe the distribution of traps.

2.2.3 Polaron Model

A polaron is a quasiparticle which is composed of a charge and its surrounding field of polarization [44]. The general concept of a polaron was first introduced by L. D. Landau in 1933 [45], but it was T. Holstein in 1959 who introduced polaron motion for the single and polycrystalline organic materials [46]. The polaron is generated with a deformation of the chain under the action of charge in organic conjugated polymers. Conjugated polymers are materials that are characterized by a backbone chain of alternating single and multiple bonds [47]. Molecules in organic semiconductors interact with their polarizing neighbor molecules during condensation, which reduces their energy. Phonon absorption by organic molecules generates an excitation that dissociates into charge carriers [34]. The interaction

between the excited electron and hole forms a bound electron-hole pair. The binding energy is given by [46],

$$E_b = \frac{A^2}{2M\omega_0^2} \tag{2.9}$$

where ω_0 is the frequency, A is a constant, and M is the reduced mass of each molecular site.

Organic semiconductors tend to localize charge carriers on individual molecules because of the weak Van der Waals intermolecular force. The localized states are formed by means of defects and chain deformation. Thus, charge transport occurs when a polaron is localized in single molecule and jumps from one molecule to another.

2.3 Types of Organic Semiconductors

Organic semiconductors can be broadly classified into two categories: small molecules and polymers. Small molecules are further classified as pigments and dyes [48]. Pigments are not soluble in organic solvents, whereas dyes are soluble. Polymers are formed by the repetition of many single units, or monomers. Polymers are soluble in organic solvents, and thus they are solution processable. Polymer layers can be deposited onto various surfaces using spin coating or dip coating processes, whereas small molecules are deposited in a vacuum environment using thermal deposition. Polymers have a larger molecular weight than small molecules; therefore, small molecules have higher mobility than polymers.

Organic semiconductors are further classified based on the type of charge they transport, i.e., p-type for hole charge transport and n-type for electron charge transport. p-

type organic semiconductors have a better charge carrier mobility and environmental stability than n-type organic semiconductors. Most n-type organic semiconductors are not stable in air, which is dependent on the free energy of activation associated with the chemical reaction with either water or oxygen [34]. Furthermore, in device applications the energy level of p-type organic semiconductors is closer to the work function of most metal contacts as compared to n-type organic semiconductors. For example, in organic thin-film transistors, the work function of most metals that are used for electrodes are closer to the HOMO energy level of p-type polymers than the LUMO energy level of n-type polymers. Thus, most research efforts have been devoted to p-type polymers, resulting in high performance p-type organic semiconductor devices. However, in order to realize complementary circuit designs, we need both n- type and p-type materials with comparable performances. Therefore, n-type organic semiconductors need to be given equal attention.

2.3.1 Dominant Organic Semiconductors

Some of the well-known p-type and n-type organic semiconductors are listed in Table 2.1. However, in this work we are focused on p-type organic semiconductors because of their superior performance. From p-type organic semiconductors, the most widely researched and used organic semiconductors are pentacene and poly(3-hexylthiophene) (P3HT). Pentacene and P3HT are discussed in the following two sections.

Table 2.1: Examples of p-type and n-type organic semiconductors

Type of organic semiconductor	Name of organic semiconductor	Reference
p-type	pentacene	49
p-type	poly(3-hexylthiophene) (P3HT)	50
p-type	poly(3-octylthiophene) (P3OT)	51
p-type	poly-9,9' dioctyl-fluorene-co-bithiophene (F8T2)	52
n-type	poly(benzobisimidazobenzophenanthroline) (BBL)	53
n-type	N,N'bis-(octyl-)-dicyanoperylene-3, 4, 9, 10-bis(dicarboximide) (PDI-8CN_2)	54
n-type	[6,6]-phenyl-C_{61}-butyric acid methyl ester (PCBM)	55
n-type	N,N'-Ditridecyl-3, 4, 9, 10-perylenetetracarboxylic Diimide (PTCDI-C_{13})	56

2.3.2 Pentacene

Pentacene is a small molecule organic semiconductor. It is in the family of acenes and is formed by five linearly-fused benzene rings. Its chemical structure is illustrated in Figure 2.5. Pentacene has a high mobility and environmental stability compared to any other p-type organic semiconductor. It has a good interface interaction with metal electrodes typically used in electronics, such as gold and aluminum [57]. However, pentacene cannot be easily dissolved in many organic solvents, making it difficult for solution processing applications. Therefore, most of the pentacene thin-films are obtained by thermal evaporation, organic vapor phase deposition, or molecular beam deposition under a vacuum environment [58-60]. The vacuum deposited films display three different phases: amorphous phase, single phase, and double phase [61]. The amorphous phase is highly disordered, whereas the single and double phases are highly ordered.

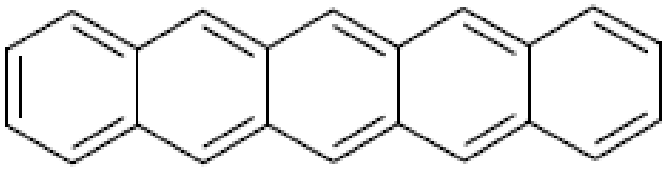

Figure 2.5: Chemical structure of pentacene [62].

2.3.3 Poly(3-hexylthiophene)

Poly(3-hexylthiophene) (P3HT) is a π–conjugated oligomer p-type organic semiconductor. The first synthesis of P3HT was reported in 1992 [63]. The chemical structure of P3HT is illustrated in Figure 2.6. As shown in the figure, the alkyl group is

characterized by 6 carbon atoms and 13 hydrogen atoms. P3HT can be synthesized in two forms, regioregular (rr-) and regiorandom (rra-) [64]. In regioregular, the alternating position of the alkyl side chains are regular, whereas in regiorandom the side chains are not positioned regularly. The strong interactions between the side chains of regioregular P3HT result in a three-dimensional lamellar structure in which the thienylene moieties are held in coplanarity [65]. The coplanarity of the thienylene moieties increases the ability to form a well-ordered lamellar structure in regioregular P3HT, whereas regiorandom P3HT films are amorphous. Thus, regioregular P3HT is more highly ordered than its regiorandom counterpart. Consequently, regioregular P3HT materials exhibit a higher mobility than regiorandom P3HTs, and therefore, regioregular is used more in electronics. The chemical structure of regioregular and regiorandom P3HT is illustrated in Figure 2.7.

P3HT has lower mobility than pentacene; however, it has the highest mobility and best electrical properties among the p-type polymers. P3HT has a better solubility behavior than pentacene, which makes it suitable for the solution processing fabrication technique. The most common organic solvents that are used to dissolve P3HT are chloroform, chlorobenzene, 1,2-dichlorobenzene, and dichloromethane [66, 67]. P3HT thin-films can be obtained by spin coating, dip coating, drop casting, or inkjet printing. In this work, we have chosen regioregular P3HT, with a regioregularity greater than or equal to 90% and an average molecular weight of 50,000 - 70,000 gram/mole as an organic semiconductor to fabricate OTFTs. The excellent solubility and good mobility properties of the regioregular P3HT makes it an ideal candidate for fabricating OTFTs on a substrate. In addition, P3HT

has been shown to have excellent field-effect characteristics when deposited on appropriate substrates [68-71].

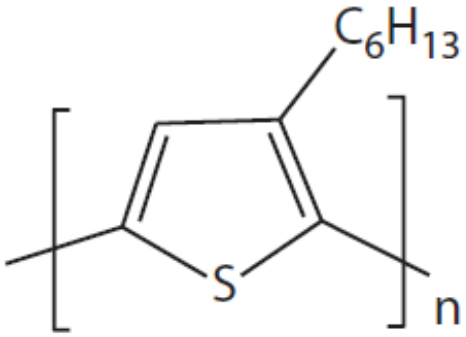

Figure 2.6: Chemical structure of P3HT [72]

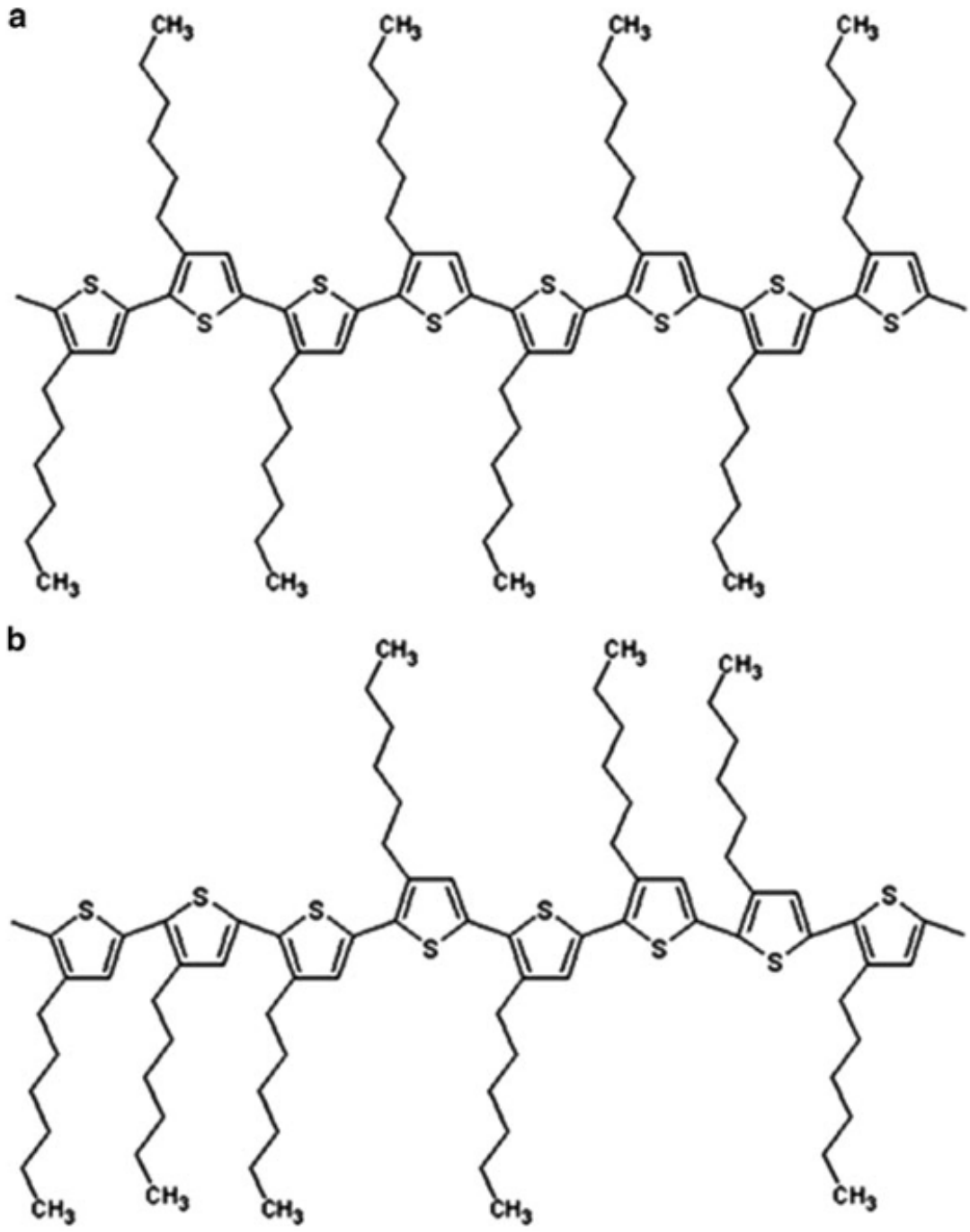

Figure 2.7: Chemical structure of (a) regioregular P3HT and (b) regiorandom P3HT [64]

2.4 References

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CHAPTER THREE

ORGANIC THIN-FILM TRANSISTORS

3.1 Introduction to Organic Thin-Film Transistors

An organic thin-film transistor (OTFT) is a field-effect transistor that uses an organic semiconductor in its channel. It is one of the most widely used organic electronic device. The first OTFT was reported in 1986, where polythiophene was used as an organic semiconductor [1]. Since then, there has been tremendous progress in the fabrication, structure, and performance of OTFTs. The main advantage of an organic transistor as compared to its inorganic counterpart is that the fabrication process is less expensive and complex, since most of the fabrication processes are done at room temperature and atmospheric pressure. Moreover, the substrates of organic transistors can be flexible and have larger surface area, which makes them viable for lightweight and flexible electronics applications. Some of the materials that have been used as a substrate in OTFTs are plastics [2], glasses [3], and fibers [4]. Even though organic transistors have the aforementioned benefits, their performance is not yet at the level of their inorganic counterpart. The mobility and switching speed of OTFTs are still smaller than for inorganic transistors. However, OTFTs have great potential in applications where low-cost, large surface area, and flexible structures are required, such as flat panel displays [5], sensors [6], radio frequency identification (RFID) tags [7], and medical device applications [8].

An OTFT is a layered structure device that consists of three electrodes (source, drain, and gate), an organic semiconductor, and a dielectric layer. The basic schematic

structure of an OTFT is shown in Figure 3.1. As shown in the figure, it is a three-terminal device. OTFTs essentially operate by applying a gate voltage of appropriate polarity and magnitude which accumulates majority charge carriers at the dielectric/organic semiconductor interface, thereby forming a conducting channel between the source and the drain. Charge carriers are injected from the source electrode into the organic semiconductor (or channel) and extracted from the organic semiconductor into the drain electrode by applying a voltage at the drain terminal with respect to the source. This operation principle of OTFTs is essentially similar to the metal-oxide-semiconductor field-effect transistors (MOSFETs). The main difference being in OTFTs the conducting channel is formed by accumulation of the charge carriers in the organic semiconductor layer near the dielectric surface, whereas in MOSFETs the conducting channel is formed by the inversion process at the semiconductor/dielectric interface.

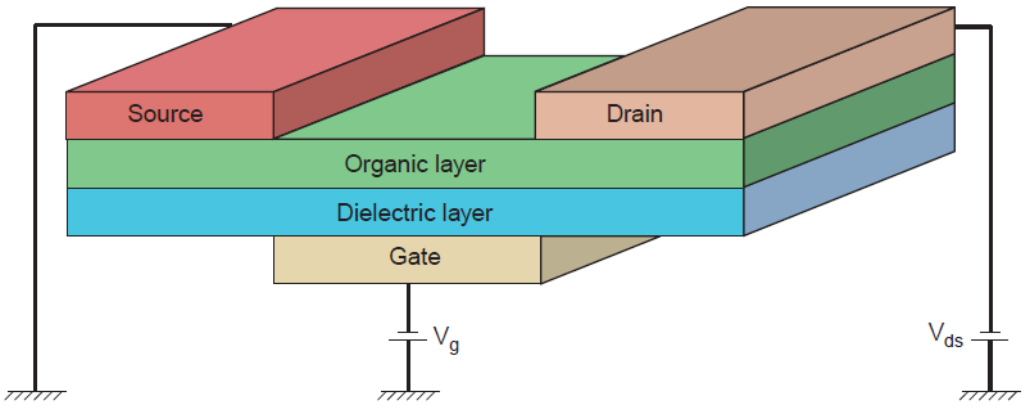

Figure 3.1: Schematic structure of an OTFT [9].

There are two major operating regions in OTFTs (as well as in MOSFETS), the linear region and the saturation region. In the linear region, the drain current (I_{DS}) increases linearly with the drain voltage (V_{DS}) at a constant gate voltage with the source normally grounded. This relation between the drain current and the drain voltage can be obtained from the I_{DS}-V_{DS} measurements, which is known as the output characteristics of OTFTs. In Figure 3.2, we show the ideal I-V characteristics of an OTFT. As shown in this figure, the linear region is the region where the drain current increases with the drain voltage. The charge carrier concentration in this region is uniform across the channel. The saturation operating region is a region where the drain current starts to saturate and approximately remain constant as the drain voltage keeps increasing while the gate is still biased at a constant voltage and the source is grounded. In this region, the charge carrier concentration is non-uniform across the channel. The I-V characteristics of an OTFT in the saturation region is also illustrated in Figure 3.2 with ideal I-V curves. The details of these two operating regions are discussed later in this chapter.

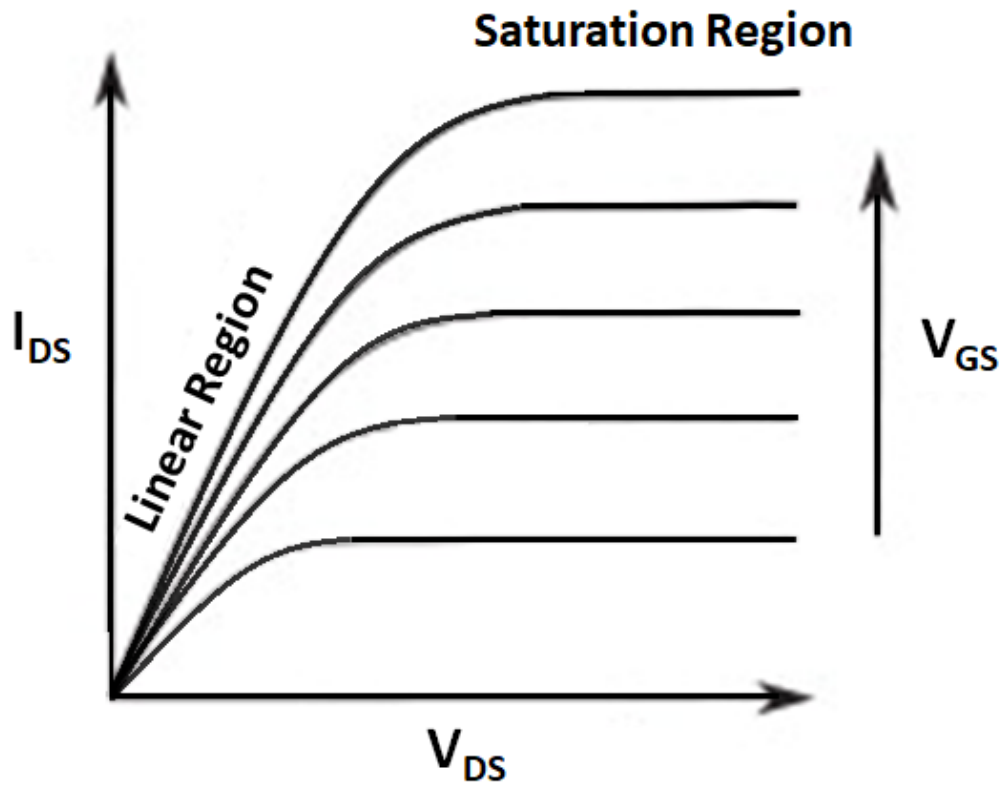

Figure 3.2: Ideal I-V characteristics of an OTFT. (Adapted from [10])

OTFTs can be classified based on the type of organic semiconductor used in the device, as n-type or p-type OTFTs. For n-type OTFTs, the semiconductor is n-type, and the device is turned on by applying positive gate voltages, as the electrons are the majority charge carriers in the channel. Whereas for p-type OTFTs, the semiconductor is p-type, and the device is turned on by applying negative gate voltages, as the majority charge carriers are holes. p-type OTFTs have a higher performance and air stability than n-type OTFTs [11, 12, 13, 14] since p-type organic semiconductors are more developed and

stable, as discussed in the previous chapter. However, we need the integration of both devices to enable complementary circuits.

3.2 Performance Parameters of Organic Thin-Film Transistors

The performance of OTFTs is analyzed by evaluating different transistor parameters. Some of the key performance parameters are threshold voltage, field-effect mobility, current on/off ratio, and subthreshold slope. These parameters are influenced by the device geometry, structural dimensions, and physical and chemical property of the materials, to name a few. The values for the performance parameters are obtained by performing several current-voltage (I-V) measurements. In general, the most desirable characteristics of transistor parameters are low threshold voltage, high mobility, low subthreshold slope, and high on/off current ratio. These parameters are discussed in the following sections.

3.2.1 Threshold Voltage

Threshold voltage is the minimum gate voltage needed to accumulate majority charge carriers at the organic semiconductor/gate insulator interface to form a conducting channel between the source and the drain [15]. It is usually affected by the thickness of the organic semiconductor and gate insulator layers, dielectric constant of the gate insulator, channel length, and doping concentration. Threshold voltage is one of the most important parameters needed to determine the operating voltage of the transistor as well as to model and characterize them. It is preferable for transistors to have a relatively low threshold

voltage since a lower threshold voltage results in a lower power consumption. A lower threshold voltage can be obtained by using a gate insulator with a high dielectric constant and a smaller thickness [16, 17]. Therefore, it is crucial to accurately extract the threshold voltage of a transistor.

The threshold voltage is not necessarily constant for organic transistors [11]. When OTFTs are operated for a long period of time, the threshold voltage can shift from its original value. The threshold voltage shift can be observed on the time scale of current-voltage measurements with current hysteresis. This behavior has a negative impact on the applicability of OTFTs, since the stability of the performance parameters is important for the operation of OTFTs [18, 19, 20]. However, this shift in threshold voltage has one potential application for OTFTs. It has been shown that a threshold voltage shift that is induced by polarization of a ferroelectric gate insulator can be used for organic memory devices [21]. So, even though the threshold voltage shift behavior is not ideal for most OTFT applications, it can be used for memory device applications.

There are several methods for extracting the threshold voltage of OTFTs. Some of the methods are based on the linear operation region of the drain current, while others are based on the saturation operation region of the drain current. A few examples of the threshold voltage extraction methods are extrapolation in the linear region (ELR) [22, 23], extrapolation in the saturation region (ESR) [22], transconductance extrapolation in the linear region (GMLE) [24, 25], second-derivative method (SD) [26], ratio method (RM) [27, 28, 29, 30], corsi function method [31], and transition method [32]. Out of these

methods, the most accurate and widely accepted methods are extrapolation in the linear region and extrapolation in the saturation region.

3.2.1.1 Extrapolation in the Linear Region

In this method, the threshold voltage is extracted using a linear extrapolation of the drain current (I_{DS}) vs. the gate voltage (V_{GS}) curve applying a drain voltage (V_{DS}) that biases the device into the linear region, which is referred to as the transfer characteristics [22, 23, 33, 34]. The extrapolation is normally taken at the maximum slope of the I_{DS}-V_{GS} curve. The slope of the I_{DS}-V_{GS} curve is known as a transconductance (g_m) and is given by,

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \tag{3.1}$$

where I_{DS} is the drain to source current and V_{GS} is the gate to source voltage. The threshold voltage is then given by [35]:

$$V_{Th} = V_{GSi} - {}^{V_{DS}}/_{2} \tag{3.2}$$

where V_{Th} is the threshold voltage, V_{DS} is the drain to source voltage, and V_{GSi} is the V_{GS} axis intercept.

The main drawback of this method is the uncertainty of the maximum slope point (or transconductance). This is because of the gate leakage current at the source and drain electrodes that cause a deviation in the I_{DS}-V_{GS} curve from the ideal straight line [23].

3.2.1.2 Extrapolation in the Saturation Region

In this method, the threshold voltage is extracted using a linear extrapolation of the square root of the drain current ($I_{ds}^{1/2}$) vs. the gate voltage (V_{GS}) curve applying a drain voltage (V_{DS}) that biases the device into the saturation region [22, 33-35]. The extrapolation is taken at the maximum slope of the $I_{ds}^{1/2}$-V_{GS} curve. Thus, the threshold voltage is equal to the gate voltage axis intercept of the extrapolation line ($V_{Th} = V_{GSi}$).

3.2.2 Mobility

Mobility is a measure of how fast charge carriers can move in the conducting channel per unit electric field. It determines the switching speed of the transistor. The higher the mobility, the faster the device operates. Field-effect mobility is dependent on the gate voltage [36]. The accumulation of the charge carriers at the dielectric/organic semiconductor interface increases with the gate voltage. The accumulated charges first fill the lower states of the organic semiconductor near the dielectric, then any additional accumulated charge carriers in the channel will occupy the states at relatively high energies [36]. Thus, the additional charge carriers will require smaller activation energy to hop from one site to another, which results in a higher mobility with an increasing gate voltage. The field-effect mobility dependence on gate voltage can be expressed with the following equation [37]:

$$\mu = \mu_0 (V_{GS} - V_{Th})^{\alpha} \tag{3.3}$$

where μ is the field-effect mobility, μ_0 is the extended state mobility of an organic semiconductor determined at a very low gate voltage (~0.5 V), and α is the mobility enhancement factor and usually lies in the rage of 0.2-0.5 [38].

The primary transport model that relates the drain current to the drain and gate voltages in OTFTs is the compact DC model. The compact DC model is discussed in the subsequent sub-section (3.3.1). The field-effect mobility equation is extracted from the drain current equation of the compact DC model. The OTFT drain current has two operating regions: the linear region and the saturation region. The field-effect mobility in the linear region is given by [11, 39],

$$\mu_{lin} = \frac{L}{WC_{OX}V_{DS}} \frac{\partial I_{DS}}{\partial V_{GS}} \tag{3.4}$$

where L is the channel length, W is the channel width, and C_{ox} is the gate insulator or oxide capacitance per unit area. From Equation (3.1), $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$, therefore, the field-effect mobility in the linear region can be rewritten as,

$$\mu_{lin} = \frac{L}{WC_{OX}V_{DS}} g_m \tag{3.5}$$

The maximum value of g_m must be used in Equation (3.5) to obtain the field-effect mobility in the linear region.

The field-effect mobility in the saturation region is given by [11, 39],

$$\mu_{Sat} = \frac{2L}{WC_{OX}} \left(\frac{\partial \sqrt{I_{DS}}}{\partial V_{GS}} \right)^2 \tag{3.6}$$

Therefore, the field-effect mobility of OTFTs for the linear and saturation operation regions can be extracted using Equations 3.5 and 3.6, respectively. The field-effect mobility in the linear and saturation regions are not always the same. The mobility in the

saturation region tends to be larger than in the linear region. This is because the integrated resistance of the channel is higher in the saturation region than in the linear region, which makes the contact resistance less noticeable in the saturation region [12].

3.2.3 Subthreshold Slope

Subthreshold slope is a measure of how fast the transistor switches from the off-state to the on-state in the exponential current increase region [12]. The exponential current increase region, also known as subthreshold region, is a region in the drain current that is above the onset voltage (or switch-on voltage) and below the threshold voltage. Subthreshold slope is measured in mV/decade and can be expressed as [40],

$$S = \frac{\partial V_{GS}}{\partial \log_{10} I_{Ds}} \tag{3.7}$$

The subthreshold slope of an OTFT can also be expressed as [39],

$$S = \frac{nK_BT}{q} ln10 \tag{3.8}$$

where K_B is Boltzmann's constant, T is the temperature, q is the elementary charge, and n is the ideality factor and is determined by the density of the trap states at the semiconductor /dielectric interface and the dielectric capacitance. The ideality factor is given by [39],

$$n = 1 + \frac{qN_{it}}{C_{OX}} \tag{3.9}$$

where N_{it} is the density of trap states. Substituting Equation (3.9) into Equation (3.8), the subthreshold slope can be rewritten as,

$$S = \frac{K_BT}{q} ln10 \left(1 + \frac{qN_{it}}{C_{OX}}\right) \tag{3.10}$$

Because of the high quality of the Si/SiO_2 interface, silicon based MOSFETs have an ideality factor that is close to one, resulting in a subthreshold slope that is approximately 60 mV/decade [39], since Nit is very low. The organic semiconductor/dielectric interface of OTFTs is of lower quality than the Si/SiO_2 interface, and therefore the subthreshold slope for organic transistors is larger than their inorganic counterpart. The larger subthreshold slope in OTFTs indicates a large concentration of shallow traps [12]. The subthreshold slope determines the quality of the organic semiconductor/dielectric interface, impurity concentration, and the presence of interface traps. However, the subthreshold slope is not only affected by the interface quality, but also by the device geometry, operating conditions, and measurement apparatus [12]. Therefore, when comparing subthreshold slope between devices, these three conditions also need to be considered.

3.2.4 Current On/Off Ratio

Current on/off ratio is the ratio of the on-state drain current at a particular gate voltage to the off-state drain current. It is important to keep the off-state current as low as possible to avoid any leakage current, and the on-state current as high as possible. The on-state current is dependent on the mobility of the organic semiconductor and the capacitance of the gate insulator [11]. The off-state current is affected by the gate leakage current and the bulk conductivity of the organic semiconductor. Thus, the off-state current is dependent on the conductivity and dimensions of the conductive channel, such as length, width, and thickness, and can be expressed as [15],

$$I_{OFF} = \frac{W}{L} t_{osc} V_{DS} \sigma \tag{3.11}$$

where t_{osc} is the thickness of the organic semiconductor, and σ the conductivity of the organic semiconductor. The current on/off ratio is given by [15],

$$\frac{I_{ON}}{I_{OFF}} = \frac{C_{OX}\mu(V_{GS}-V_{Th})^2}{t_{osc}V_{DS}\sigma} \tag{3.12}$$

The current on/off ratio can be enhanced by reducing the thickness of the dielectric layer, which increases the on-state current, and reducing the thickness of the organic semiconductor layer, which decreases the off-state current. The organic semiconductor thickness has a stronger impact on the current on/off ratio than the dielectric thickness. It was shown in [41] that decreasing the organic semiconductor (P3HT) thickness from 160 nm to 20 nm resulted in an enormous increase in the current on/off ratio, from 10 to 2 x10^9. This is because of the larger decrease in the off-state current as the thickness of the P3HT layer decreases. Moreover, the on/off current ratio can be increased by using a gate insulator with high dielectric constant along with a low doping concentration for the organic semiconductor.

3.3 Models of Organic Thin-Film Transistors

There is no one single model that fully describes the operation of OTFTs. Almost all reported models that describe the operation of transistors are based on a particular charge transport theory or are developed for a particular OTFT structure [38, 42-44]. Most of the models developed for OTFTs are adapted from MOS transistor models due to their similar operating principles. The first OTFT model was reported in 1992 [45]. This model was based on thin-film metal-insulator-semiconductor field-effect transistors (MISFETs)

with poly(3-hexylthiophene) as the organic semiconductor. The model included bulk leakage current and contact resistance, but it did not fully describe OTFTs.

Even though there are some similar current-voltage characteristics between OTFTs and MOS transistors, there are also some differences in electrical and material characteristics. Some of the basic differences are bulk leakage current, contact resistance, bias dependent mobility, interface state traps, and morphological disorder [46, 47]. Thus, the models for OTFTs must be modified to include these and some other inherent characteristics of organic materials. The common point in most OTFT models is the field-effect mobility, which is dependent on the gate voltage [46, 48, 49]. This field-effect mobility dependence on the gate overdrive voltage was given in Equation 3.3, which is $\mu = \mu_0(V_{GS} - V_{Th})^{\alpha}$. Some of the most widely accepted models of OTFTs are the compact DC model, the charge drift model, and the charge drift model for the subthreshold region.

3.3.1 Compact DC Model

The Compact DC model is a charge transport model that relates the drain current to the drain and gate voltages. It was first developed to analyze the dc behavior of MOS transistors. The drain current in this model is expressed as [39, 46, 47, 50],

$$I_{DS} = \frac{W}{L} C_{ox} \mu \left[(V_{GS} - V_{Th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{3.13}$$

where W is the channel width, L is the channel length, and C_{ox} is the gate insulator capacitance per unit area. The gate insulator capacitance per unit area is given by,

$$C_{OX} = \frac{\varepsilon_i \varepsilon_o}{t_{ox}} \tag{3.14}$$

where t_{ox} is the gate insulator thickness, ε_i is the dielectric constant of the gate insulator, and ε_o is the permittivity of free space.

The compact dc model shown in Equation (3.13) describes the drain current for gate voltages above the threshold voltage. As discussed earlier, the OTFT drain current has two operating regions, the linear region and the saturation region. For the linear region, $V_{DS} << (V_{GS} - V_{Th})$. Therefore, Equation (3.13) can be simplified for the linear region with small V_{DS} and can be written as,

$$I_{DS} = \frac{W}{L} C_{OX} \mu_{lin} (V_{GS} - V_{Th}) V_{DS} \tag{3.15}$$

For the saturation region, $V_{DS} \geq (V_{GS} - V_{Th})$. The onset of saturation occurs when $V_{DSsat} = (V_{GS} - V_{Th})$. Therefore, at the point of saturation, Equation (3.13) can be written as,

$$I_{DSat} = \frac{W}{2L} C_{OX} \mu_{sat} (V_{GS} - V_{Th})^2 \tag{3.16}$$

To first order, the drain current (I_{DS}) remains approximately constant at the saturation value (I_{DSat}) as the drain to source voltage (V_{DS}) exceeds V_{DSsat}. However, in most fabricated OTFTs, there is a finite slope to the I-V curve past saturation.

3.3.2 Charge Drift Model

The Charge drift model is one of the most widely used models to describe the operation of OTFTs. It is based on tail-distributed traps [51] and variable range hopping [36]. Using the well-established concept of charge drift, the current per unit channel width is given by [46],

$$\frac{I_{DS}}{W} = \mu_x q_x |E_x| \tag{3.17}$$

where x is a position in the channel, $0 \leq x \leq L$, $|E_x|$ is the electric field and is given by,

$$|E_x| = \frac{\partial V_x}{\partial x} \tag{3.18}$$

q_x is the arial charge density and is given by,

$$q_x = C_{OX}(V_{GS} - V_{Th} - V_x) \tag{3.19}$$

where Vx is the voltage at a point x, with respect to the source.

The field-effect mobility at point x in the channel can be expressed as [47, 51],

$$\mu_x = \mu_0(V_{GS} - V_{Th} - V_x)^{\alpha} \tag{3.20}$$

where μ_0 is the zero-field mobility.

Since we have defined all the terms in Equation (3.17), i.e., E_x, q_x, and μ_x, we can rewrite the drain current by substituting Equation (3.18), (3.19), and (3.20) into Equation (3.17), which yields,

$$\frac{I_{DS}}{W} = \mu_0(V_{GS} - V_{Th} - V_x)^{\alpha} C_{OX}(V_{GS} - V_{Th} - V_x)\frac{\partial V_x}{\partial x} \tag{3.21}$$

Integrating the drain current along the channel length, from 0 to L,

$$\frac{1}{W}\int_0^L I_{DS}dx = \mu_0 C_{OX}\int_0^L (V_{GS} - V_{Th} - V_x)^{\alpha}(V_{GS} - V_{Th} - V_x)\frac{\partial V_x}{\partial x}dx, \tag{3.22}$$

$$where\ \frac{\partial V_x}{\partial x}dx = dV_x$$

$$I_D\frac{L}{W} = \mu_0 C_{OX}\int_{V_S}^{V_D}(V_{GS} - V_{Th} - V_x)^{\alpha+1}dV_x \tag{3.23}$$

where V_D is the voltage of the channel at the drain side of the OTFT, and V_S is the voltage of the channel at the source side of the OTFT. Integrating equation 3.23, we obtain,

$$I_D\frac{L}{W} = -\mu_0 C_{OX}\left[\frac{(V_{GS}-V_{Th}-V_D)^{\alpha+2}}{\alpha+2} - \frac{(V_{GS}-V_{Th}-V_S)^{\alpha+2}}{\alpha+2}\right] \tag{3.24}$$

Therefore, the Drain current equation becomes,

$$I_D = \frac{W\mu_0 C_{OX}}{L(\alpha+2)}[(V_{GS} - V_{Th} - V_S)^{\alpha+2} - (V_{GS} - V_{Th} - V_D)^{\alpha+2}] \quad (3.25)$$

The final drain current equation, Equation (3.25), only applies in the linear region of the transistor, which is above the threshold voltage ($V_{GS} > V_T$). Therefore, we need to modify Equation (3.25) to include the subthreshold region.

3.3.3 Charge Drift Model for the Subthreshold Region

The subthreshold region is not usually included in generic OTFT models; however, it can easily be incorporated using an asymptotic interpolation function. The drain current in the subthreshold region can be expressed as [46],

$$I_{DS} = \frac{W\mu_0 C_{OX}}{L} \times \frac{[f(V_{GS}-V_{Th}-V_S)]^{(\alpha+2)} - [f(V_{GS}-V_{Th}-V_D)]^{(\alpha+2)}}{\alpha+2} \quad (3.26)$$

where $f(V_{GS}, V)$ is the asymptotical interpolation function. At $V = V_D$ or $V = V_S$, the function $f(V_{GS}, V)$ is regarded as an overdrive voltage ($V_{overdrive}$) and is given by,

$$V_{overdrive}(V) = f(V_{GS}, V) = V_{sub} ln\left[1 + exp\left(\frac{V_{GS}-V_{Th}-V}{V_{sub}}\right)\right] \quad (3.27)$$

where V_{sub} is the subthreshold slope voltage, which corresponds to the steepness of the curve. By substituting the overdrive voltage from Equation (3.27) into Equation (3.26), the drain current in the subthreshold region can be written as,

$$I_{DS} = \frac{W\mu_0 C_{OX} V_{sub}^{(\alpha+2)}}{L} \times \frac{\left[ln\left\{1+exp\left(\frac{V_{GS}-V_{Th}-V_S}{V_{sub}}\right)\right\}\right]^{(\alpha+2)} - \left[ln\left\{1+exp\left(\frac{V_{GS}-V_{Th}-V_D}{V_{sub}}\right)\right\}\right]^{(\alpha+2)}}{\alpha+2} \quad (3.28)$$

To make this model more complete, another parameter that needs to be added is the channel length modulation. This mechanism is what leads to a linear increase in drain current in the "saturation" region. At the saturation point of a transistor, $V_{DS} = V_{DSat} = V_{GS}$

– V_{Th}, which means the charge at the drain end (at x = L) becomes much smaller than the charge at the source end. As the drain voltage increases beyond V_{Dsat}, the charges at the drain end become essentially zero, and the effective length of the channel decreases. This condition is known as Pinch-off. The length of the channel that is pinched-off is ΔL, and thus, the effective channel length is L - ΔL. The relationship between the drain voltage and the effective channel length or pinched-off length is given by [46, 47],

$$L - \Delta L = L\left(1 - \frac{\Delta L}{L}\right) = L[1 - \beta(V_{DS} - V_{sat})] \approx \frac{L}{1+\beta|V_{DS}-V_S|} \tag{3.29}$$

where β is the channel length modulation coefficient. The charge drift model shown in Equation (3.25) can be modified to include channel length modulation and becomes,

$$I_D = \frac{W\mu_0 C_{OX}(1+\beta(V_{DS}-V_S))}{L(\alpha+2)}[(V_{GS} - V_{Th} - V_S)^{\alpha+2} - (V_{GS} - V_{Th} - V_D)^{\alpha+2}] \tag{3.30}$$

In principle, this modification for channel length modulation can be adapted to any of the OTFT models to explain the non-zero slope often observed in measured I_D-V_D curves in the saturation region.

In this work, we have chosen the compact DC model to characterize our fabricated OTFTs. The Compact DC model can fully describe the dominant behavior of OTFTs. The field-effect mobility's dependence on the gate voltage is described very well in this model. The Compact DC model reflects the symmetrical structure of OTFTs, which makes the model simpler and allows for the source and drain contacts to be used interchangeably. It is also upgradable and reducible [46], making it possible to replace or add different relations and dependences into the model. Using this model, it is straight forward to

compare OTFTs to other FETs without major recalculation of major parameters [46]. It is also easy to derive the compact DC model, since it does not have complex expressions.

3.4 References

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CHAPTER FOUR

STRUCTURES OF ORGANIC THIN-FILM TRANSISTORS

4.1 Introduction to Structures of Organic Thin-Film Transistors

The desire to improve the performance of OTFTs has led to the development of new device structures throughout the years. The first classification used to describe these various structures is based on whether a device has one gate or two gates, which are named accordingly as single gate and dual gate OTFTs. Single gate OTFTs are further classified based on the location of the gate, as top or bottom gate OTFTs. Single gate OTFTs are further classified based on the location of the source and drain contacts with respect to the organic semiconductor, as top or bottom contact OTFTs. The desire to control the threshold voltage and reduce the channel length have led to the development of a dual gate and vertical channel OTFTs, respectively. The application of OTFTs in wearable devices and smart textiles has pushed OTFTs to be smaller in size and higher in packing density, which has resulted in the development of a cylindrical gate OTFT. In the following sections, we will discuss these different structures of OTFTs, and present the reasons for our choice of overall device design for this work.

4.2 Single Gate Organic Thin-Film Transistors

Single gate OTFT structures are classified based on the location of the gate. If the gate is at the top it is called a top gate OTFT, and if the gate is at the bottom it is called a bottom gate OTFT. The top and bottom gate structures are further classified based on the location

of the source and drain contacts with respect to the organic semiconductor layer. In a bottom gate structure, if the source and drain contacts are above the organic semiconductor layer, as illustrated in Figure 4.1, the structure is referred to as a bottom gate top contact (BGTC) device, whereas if the source and drain are in direct contact with the gate insulator, as illustrated in Figure 4.2, the structure is referred to as a bottom gate bottom contact (BGBC) device. For top gate OTFTs, there are corresponding classifications for the position of the contacts. If the source and drain contacts are below the organic semiconductor without any direct contact to the gate insulator, the structure is referred to as a top gate top contact (TGTC) device, and if the source and drain contacts are just below the gate insulator, then the structure is referred to as a top gate bottom contact (TGBC) device. The top gate top contact and top gate bottom contact structures are illustrated in Figure 4.3 and Figure 4.4, respectively.

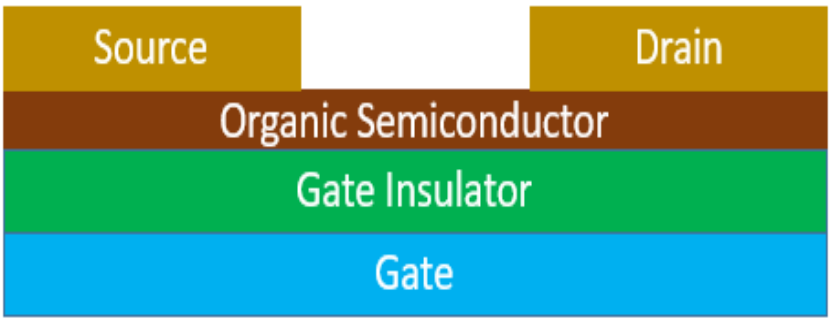

Figure 4.1: Structure of bottom gate top contact (BGTC) OTFT

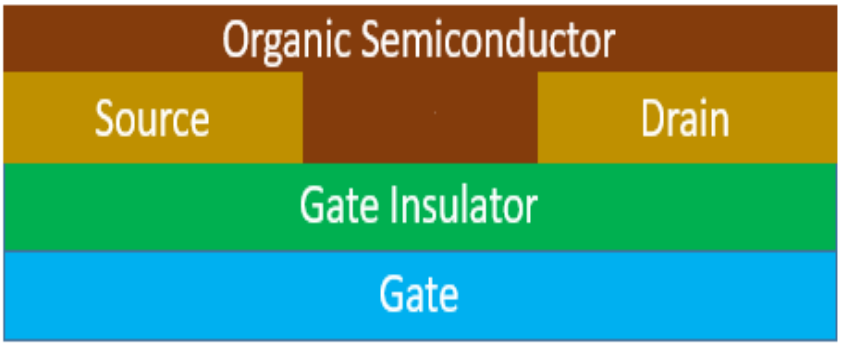

Figure 4.2: Structure of bottom gate bottom contact (BGBC) OTFT

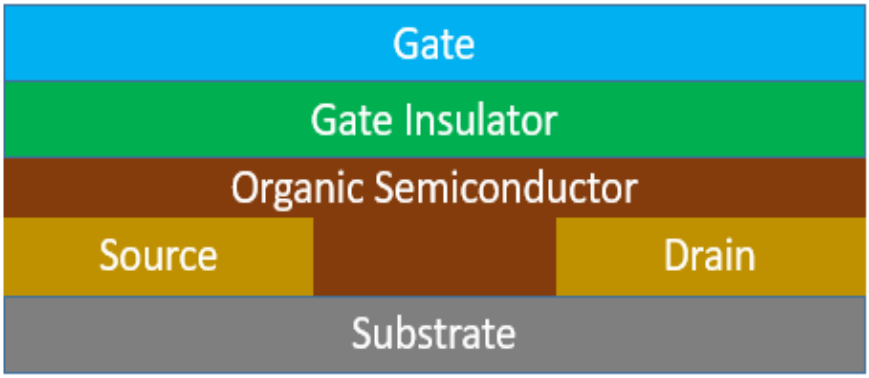

Figure 4.3: Structure of top gate top contact (TGTC) OTFT

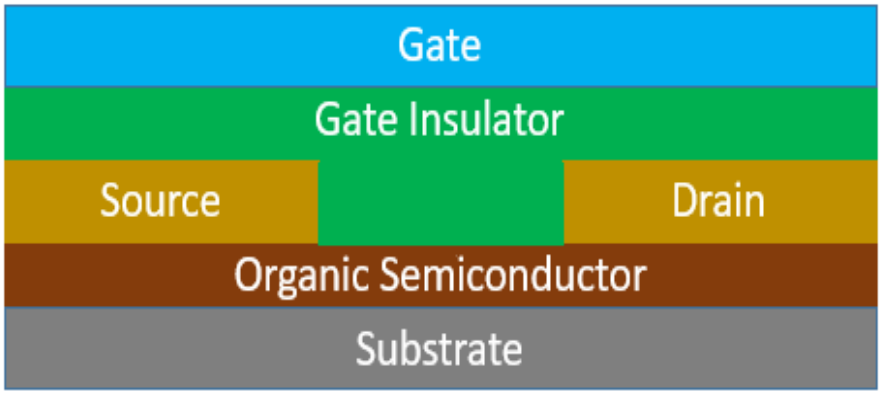

Figure 4.4: Structure of top gate bottom contact (TGBC) OTFT

The performance and fabrication complexity of single gate OTFTs are not the same. It varies from one structure to another. In a top gate OTFT fabrication process, the organic semiconductor is deposited before the gate insulator, which makes the fabrication process a little challenging. Furthermore, the deposition of the top gate metal can create contamination into the organic semiconductor layer at high temperature, which degrades the performance of the device [1]. Because of this, the bottom gate structure is preferred over the top gate structure.

Even within the bottom gate OTFTs, there is a performance variability between bottom contact and top contact OTFTs. Bottom gate top contact (BGTC) OTFTs usually have a better performance than bottom gate bottom contact (BGBC) OTFTs. This is because the source and drain of the BGTC OTFTs are deposited on top of the organic semiconductor, which results in a larger charge injection area and a lower contact resistance than the BGBC OTFTs. However, the fabrication process for BGTC structures is not as convenient for industrial applications [1]. Therefore, BGBC structures are more attractive for efficient and cost-effective fabrication process in standard Si-based CMOS facilities. Based on these considerations, the design for the devices in this work is based on BGBC OTFT structure.

4.3 Dual Gate Organic Thin-Film Transistors

The first dual gate thin-film transistor was developed in 1981 with Cadmium Selenide (CdSe) as the semiconductor [2]. However, the first dual gate organic thin-film transistor was developed in 2005 with pentacene as the organic semiconductor [3]. A dual

gate OTFT consists of two gate electrodes, two corresponding gate insulator layers, an organic semiconductor, and source and drain electrodes. The two gates in dual gate OTFTs are located at the bottom and top of the device. The schematic structure of a dual gate OTFT is shown in Figure 4.5. The bottom gate forms a conductive channel at the bottom gate insulator/organic semiconductor interface, and the top gate increases the conductivity of the channel and modifies the charge carrier distribution electrostatically [4, 5]. In addition to increasing the conductivity of the primary channel, the top gate forms a secondary conductive channel at the top gate insulator/organic semiconductor interface, contributing to the overall enhancement of the drain current [4, 6].

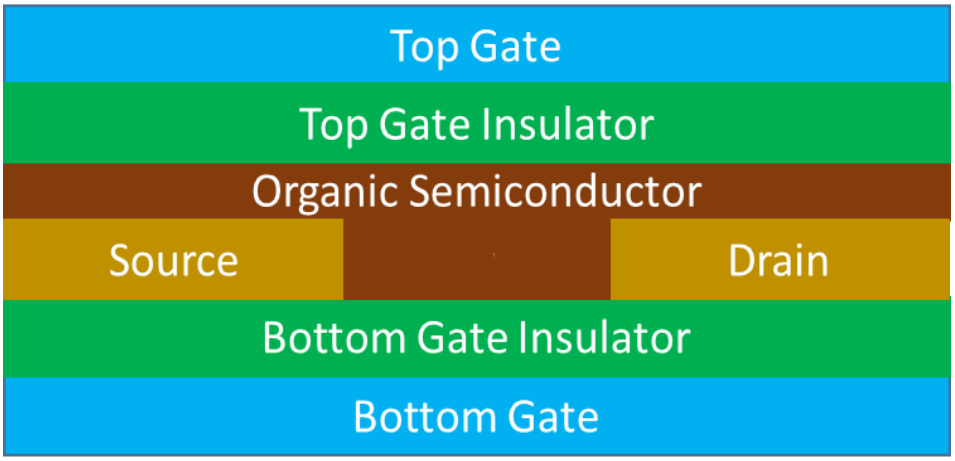

Figure 4.5: Schematic Structure of a dual gate OTFT

The driving force for developing a dual gate OTFT was the desire to control the threshold voltage and increase the drive current [7, 8]. Controlling the threshold voltage helps in lowering the operating voltage of the device, which is important for low power

application of OTFTs. The drive current is important for increasing the drain current. The drive current can be defined as the on current per unit channel width. It has been shown that adding a second gate at the top results in a better control of the threshold voltage and enhancement of the drive current [7, 8, 9]. In addition to this, dual gate OTFTs are more environmentally stable than single gate OTFTs. The performance of single gate OTFTs can be affected by the ambient since the organic semiconductor layer is exposed to the environment. With dual gate OTFTs, however, the top gate insulator can be used as a passivating layer to protect the organic semiconductor from the environment [7].

Because of the aforementioned benefits, dual gate OTFTs perform better than single gate OTFTs. They usually have a lower threshold voltage, and a higher drain current, mobility, current on/off ratio and transconductance(g_m) than single gate OTFTs [4, 8, 10, 11]. One of the drawbacks of dual gate OTFTs is that the deposition of the top gate insulator and gate electrode may lead to some damage to the organic semiconductor or create defects in the organic semiconductor [9]. In addition, the extra fabrication process steps and extra materials in dual gate OTFTs results in an additional cost as compared to single gate OTFTs.

4.4 Vertical Channel Organic Thin-Film Transistors

One of the challenges of lateral OTFTs, where the source and drain contacts are in the same plane, is reducing the channel length. Short channel devices improve the device performance by increasing the cut-off frequency and the current density, which are useful for applications in organic light emitting transistors [12]. In addition, short channel devices

are useful for low power applications, since they can operate at low voltages with a sizeable current density output [12]. However, it is very challenging and expensive to achieve a channel length that is less than ten microns for lateral OTFTs using a simple lithography or shadow mask process. Therefore, vertical channel OTFTs were developed in order to reduce the channel length and realize short channel OTFTs. There are several designs of vertical channel OTFTs. Some of the well-known structures of vertical channel OTFTs are the V-shaped channel OTFTs [13], static induction transistor (SIT) OTFTs [14], and vertical OTFTs (VOTFTs) [15]. The schematic structure of a vertical OTFT is shown in Figure 4.6.

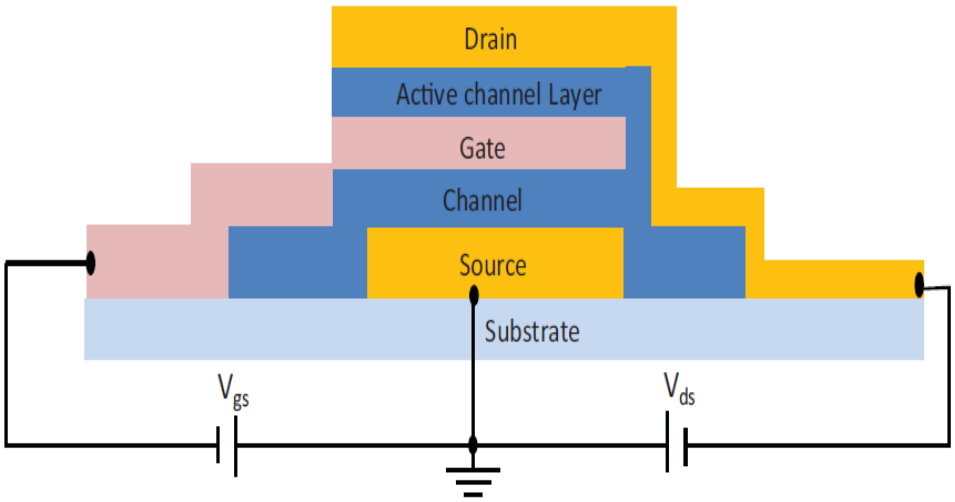

Figure 4.6: Schematic structure of the vertical organic thin-film transistor [1]

It is shown in [16] that vertical channel OTFTs with a P3HT organic semiconductor and a channel length of 5 μm performed better than lateral OTFTs. The mobility for the

vertical channel top contact OTFTs were increased by a factor of 3.3 and the on/off current was increased by a factor of 11 compared to the lateral bottom contact OTFTs. The vertical channel bottom contact OTFTs were also compared, and the mobility for the vertical channel bottom contact OTFTs were improved by a factor of 1.1 and the on/off current were improved by factor of 3.6 compared to the lateral bottom contact OTFTs. Therefore, both top and bottom contact vertical channel OTFTs showed a higher performance than the lateral bottom contact OTFTs. This is mainly because of the lower contamination and the low contact resistance in the vertical channel OTFTs.

As the channel lengths keep reducing, vertical channel OTFTs are facing challenges. One of the main challenges is the tunneling effect. The tunneling effect reduces the control ability of the gate bias and increases the leakage current of the devices [1, 17]. One way to suppress the tunneling effect is by employing a meshed structure for the source electrode [17]. In this structure, the fringing field-effect generated by the gate bias around the source electrode can reduce the leakage current.

4.5 Cylindrical Gate Organic Thin-Film Transistors

The mechanical and electrical properties of OTFTs enabled the development of cylindrical gate OTFTs (CG-OTFTs), which are key components in applications of wearable devices, e-papers, and smart textiles [18, 19]. Cylindrical gate structures are useful in reducing the size and increasing the packing density of OTFTs [20]. Furthermore, cylindrical gate OTFTs have a better control of the gate over the channel potential, thus improving the subthreshold characteristics of the device [21].

Fabrication of a cylindrical gate OTFT starts with a metal core of yarn that is used as a gate electrode [18]. Then, a thin insulating layer is deposited onto the yarn, followed by deposition of an organic semiconductor onto the insulator layer. The source and drain contacts are deposited onto the organic semiconductor using a thermal evaporation or soft lithography process. The schematic structure of a cylindrical gate OTFT is illustrated in Figure 4.7.

One of the main applications of cylindrical gate OTFTs is in the e-textile industry. The cylindrical gate OTFTs reported in [18, 19, 21] showed promising results for e-textile applications. It is reported in [19] that pentacene based cylindrical OTFTs, with photocurable poly(vinyl cinnamate) (PVCN) and poly(4-vinyl phenol) (PVP) gate dielectrics, showed high performance operation without any hysteresis effect. Because of the good flexibility behavior of PVCN, the devices with the PVCN dielectric showed higher mobility and bending stress durability than PVP devices. The bending radius of the PVCN transistors was comparable to the minimum value reported for lateral OTFTs. Thus, cylindrical OTFTs have a huge potential for commercial use in the e-textile industry.

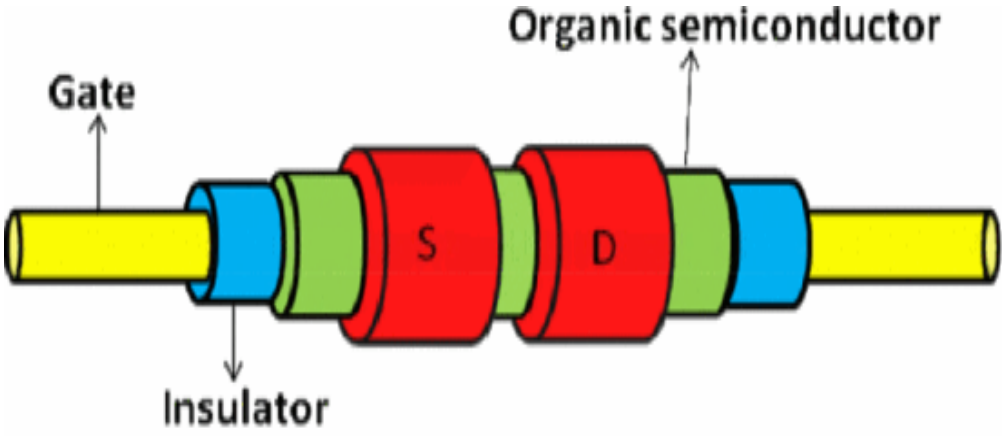

Figure 4.7: Schematic structure of a cylindrical gate OTFT [22]

In conclusion, we presented the different structures of OTFTs. Each device structure has its own advantages and disadvantages. The driving force for developing new device structures was the desire to improve the performance of OTFTs. Single gate OTFTs are the first type of OTFT structures. They have less complicated structures and fabrication processes. Dual gate OTFTs improved the control ability of the threshold voltage and the drive current. Vertical channel OTFTs were critical in reducing the channel length and realizing short channel OTFTs. Whereas Cylindrical OTFTs were useful in reducing the size and increasing the packing density of OTFTs. The devices in this work are designed based on the bottom gate bottom contact (BGBC) structure. BGBC structure was chosen because it is convenient for an efficient and cost-effective fabrication process, which is attractive for industrial applications.

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CHAPTER FIVE

INTERFACE ENGINEERING OF ORGANIC THIN-FILM TRANSISTORS

5.1 Introduction to Interface Engineering

The performance and lifetime of OTFTs are not only dependent on the properties of the materials that are used to make them, but also on the interfaces between the materials. The most critical processes in OTFT operation are charge carrier injection and transport. These two processes occur at the interfaces of the device. So, the interfaces play a critical role in the device operation of OTFTs. As Nobel laureate Herbert Kroemer famously put it, “the interface is the device”, referring to the essential role the transition region or the interface between materials play in the device action [1].

The most important interfaces in OTFTs are the source-drain electrode/organic semiconductor, dielectric/organic semiconductor, organic semiconductor/organic semiconductor, and organic semiconductor/environment interfaces [2, 3]. The source-drain electrode/organic semiconductor interface is responsible for the injection of charges from one electrode into the organic semiconductor, and the extraction of charges from the organic semiconductor into the other electrode. The main factors that affect the injection of charges at this interface are energy barrier, injection area, and contact resistance [3]. The dielectric/organic semiconductor interface is responsible for the transport of charge carriers in the channel of OTFTs. The main factors that affect the transport of charge carriers at this interface are surface energy, surface roughness, and trap density of the dielectric layer [3]. The organic semiconductor/organic semiconductor interface is formed by introducing two

organic semiconductors in the channel of the device and creating a heterojunction [3, 4]. This interface can be used to achieve field-effect and light-emitting operation in the same channel, which is important for developing an organic light-emitting field-effect transistors (OLEFET) [5, 6]. This interface is also used for developing ambipolar OTFTs using a bi-layer of p-type and n-type organic semiconductors [5, 7]. The organic semiconductor/environment interface is important for device stability and sensing applications [4]. OTFTs can be used for sensing applications by exposing the organic semiconductor surface to the environment that is being analyzed [8-10].

In this chapter, we focus on the first two interfaces, the source-drain electrode/organic semiconductor and the dielectric/organic semiconductor interfaces. These two interfaces are illustrated in Figure 5.1 for a bottom gate bottom contact OTFT. Modifying these interfaces by inserting an extra material between the two layers can increase the efficiency of the charge injection process from the electrode into the organic semiconductor and the charge transport across the conductive channel which is primarily at the dielectric/organic semiconductor interface. Thus, careful consideration and design of these two interfaces is crucial in order to optimize the device operation and improve the device performance. This is often referred to as interface engineering [2, 3, 11].

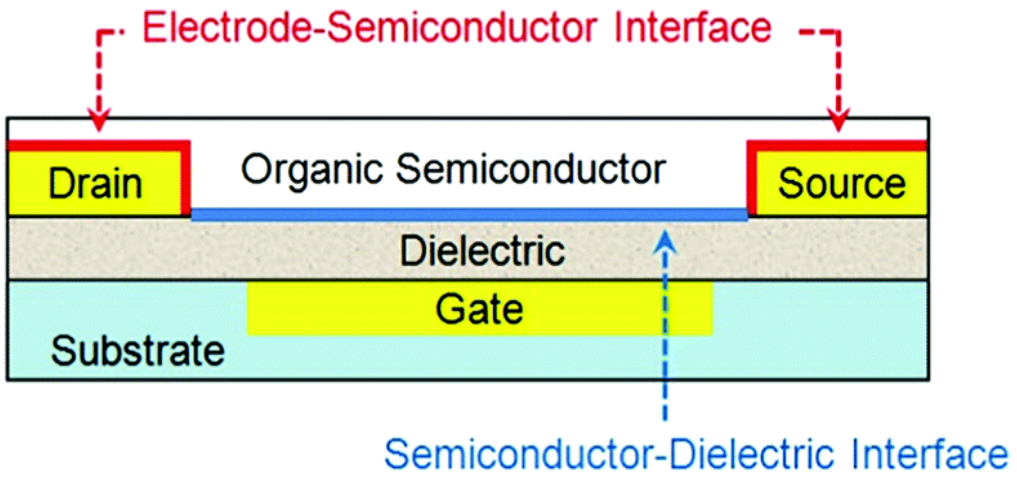

Figure 5.1: Schematic structure of a bottom gate bottom contact OTFT with the two critical interfaces highlighted [2]

5.2 Source-Drain Electrode/Organic Semiconductor Interface

Charge carriers are injected from the source electrode into the organic semiconductor and extracted from the organic semiconductor into the drain electrode at the interfaces. This charge injection process can be affected by the energy levels of the electrode and the organic semiconductor, and the structure of the device. For an efficient charge injection process, the work function of the electrode must align, or be very close, to the energy band level of the organic semiconductor. Thus, ideally the work function of the electrode should match the highest occupied molecular orbital (HOMO) energy level of a p-type organic semiconductor or the lowest unoccupied molecular orbital (LUMO) energy level of an n-type organic semiconductor [2]. The mismatch in the two energy levels creates an energy barrier, and this barrier limits the charge injection from the electrode into the organic semiconductor.

Introducing an interfacial layer between the electrode and the organic semiconductor can reduce the energy barrier to injection [3, 4, 12]. In pentacene OTFTs with aluminum electrodes, the energy barrier from the aluminum electrode to the pentacene was 1 eV [12]. However, when a metal oxide, MoO_3, was inserted between aluminum and pentacene, the energy barrier was reduced to approximately 0.3 eV. This reduction in energy barrier led to a significant improvement in the mobility of the device. The mobility increased from $2.8 \times 10^{-3} cm^2 V^{-1} s^{-1}$ to $0.4\ cm^2 V^{-1} s^{-1}$. In addition to this, the insertion of the interfacial layer prevents the metal atoms from penetrating into the organic semiconductor during the metal deposition. In another example of a pentacene OTFT but with a gold electrode [13], the insertion of a copper phthalocyanine (CuPC) interfacial layer reduced the energy barrier and enhanced the mobility of the device from $0.11\ cm^2 V^{-1} s^{-1}$ to $0.21\ cm^2 V^{-1} s^{-1}$ and the current on/off ratio from 5.0×10^5 to 1.0×10^6.

The structure of the device also affects the injection of charge carriers into the channel. Top contact devices, where the electrode is deposited on top of the organic semiconductor, perform better in terms of charge injection as compared to bottom contact devices, where the organic semiconductor is deposited on top of the electrode. This is because top contact devices have larger contact surface area than bottom contact devices, which results in low contact resistance. Contact resistance affects the injection of charges; increasing the contact resistance reduces the amount of charge carriers injected into the semiconductor. However, top contact devices are not convenient for photolithographic fabrication processes. Because of this most OTFTs, including the devices reported in this work, are bottom contact OTFTs.

The contact resistance in bottom contact devices can be lowered by increasing the injection area, and the injection area can be increased by increasing the roughness of the electrode surface. In bottom contact pentacene OTFTs with copper electrodes [14], the copper electrode surface was modified with nanometer-sized copper tetracyanoquinodimethane (Cu-TCNQ), resulting in a roughness of about 50-100 nm. This corresponds to a 2-5 times increase in the surface area of the electrode as well as the charge injection area at the electrode/organic semiconductor interface, which resulted in the reduction of the contact resistance by a factor of 20 at a gate voltage of -40 V. The decrease in the contact resistance led to an increase in the mobility of the device by a factor of three. The mobility of the device without the dense Cu-TCNQ nanostructure was $0.1\ cm^2V^{-1}s^{-1}$, but after the modification of the electrodes with Cu-TCNQ nanostructure the mobility was $0.31\ cm^2V^{-1}s^{-1}$. This reduction in contact resistance and improved performance is not only applicable for the bottom contact devices, but also for the top contact devices. In top contact pentacene OTFTs with a gold electrode [13], inserting a CuPC interfacial layer reduced the contact resistance form $4.71 \times 10^{-3}\Omega\ cm$ to $1.55 \times 10^{-3}\Omega\ cm$ at a gate voltage of -75 V, and improved the performance of the device significantly.

Introducing an interfacial layer at the electrode/organic semiconductor interface also reduces the surface energy of the electrode. In bottom contact OTFTs, the poor chemical compatibility between the metal electrodes and the organic semiconductor results in the reduction of the organic semiconductors grain size that are around the source and drain electrodes compared to the ones in the channel [3]. Therefore, introducing a self-

assembled monolayer (SAM) at the electrode/organic semiconductor interface enlarges the grain size and reduces the surface energy of the metal electrode, and consequently improves the performance of the device. In pentacene OTFTs with gold electrodes [15], the addition of a thiol-based SAM (1-hexadecanethiol) led to an increase in the grain size of pentacene on the electrode, which results in a decrease in trap density. Thus, the mobility of the device was improved from $0.16\,cm^2V^{-1}s^{-1}$ to $0.48\,cm^2V^{-1}s^{-1}$. In another example [16], in pentacene OTFTs with palladium electrodes, the mobility was improved from $0.15\,cm^2V^{-1}s^{-1}$ to $0.55\,cm^2V^{-1}s^{-1}$ using another thiol-based SAM (4-nitrobenzenethiol). Therefore, proper engineering of the electrode/organic semiconductor interface is essential for lowering the energy barrier, contact resistance and surface energy, resulting in an optimal device performance.

5.3 Dielectric/Organic Semiconductor Interface

Once the charge carriers are injected into the organic semiconductor, they are transported across the channel near the dielectric/organic semiconductor interface. Since most of this transport occurs within a few molecular layers of the organic semiconductor near the dielectric surface [2], the dielectric surface can have a significant impact on charge carrier transport. During the deposition of the organic semiconductor, the surface roughness and the surface energy of the dielectric profoundly influences the structure of the organic semiconductor layer, i.e., the molecular ordering, molecular orientation, and morphology of the organic semiconductor [2]. High dielectric surface roughness negatively impacts the device operation. Increasing the surface roughness of the dielectric layer

decreases the grain size of the organic semiconductor and increases the density of the grain boundaries and trap states, which ultimately decreases the mobility of the device [17]. The surface energy of the dielectric influences the growth mode and the morphology of the organic semiconductor. It is shown in [18] that the surface energy mismatch between pentacene and octadecyltrichlorosilane (OTS)-treated SiO_2 dielectric leads to pentacene aggregation, resulting in degradation of device performance and stability. In another work [19], it is shown that the grain size of pentacene increases with the surface energy of the poly(imide-siloxane) dielectric, which in turn affects the device performance. Thus, the surface roughness and the surface energy of the dielectric influences the morphology of the organic semiconductor and thereby, the device performance.

The morphology of the organic semiconductor is also affected by the film-growth rate. Controlling the film-growth rate of the organic semiconductor helps to control its grain size and the grain boundary depth [20]. The grain boundary depth is a vertical distance from the upper layer into the inner layer along the gap of the grain boundary [20]. It is preferred for the grain size to be large and the grain boundary depth to be small. Large grain size means there is a small potential barrier between the grains of the organic semiconductor, and small grain boundary depth means O_2/H_2O cannot easily penetrate the channel and cause electron trapping. Therefore, optimizing the film-growth rate contributes to a stable and high performance OTFT.

The air stability of OTFTs is affected by the surface trap density at the dielectric layer, which also affects the device performance. Air stability is an issue in OTFTs, especially, for n-type OTFTs. Most n-type OTFTs work in a vacuum (or inert atmosphere),

because under ambient condition O_2 and H_2O can act as oxidants and/or electron traps that affect the current in the channel of the device [20-22]. It is shown in [21] that the air stability of n-channel OTFTs with N, N'-dioctyl-3, 4, 9, 10-perylene tetracarboxylic diimide (PTCDI-C8) organic semiconductor were improved when the dielectric (SiO_2) surface was modified using a hydroxyl-free polymer insulator, such as poly(methyl methacrylate) (PMMA) and poly-α-methylstytene (PαMS). These two polymers have a hydrophobic nature, which prevents the protonation of siloxyl groups (SiOH) and consequently electron trapping groups (SiO^-) [23]. The hydrophobic nature of the polymer surfaces restricts the absorption of humidity as compared to the SiO_2 surface, and slows down the degradation of the n-type organic semiconductor under ambient conditions. So, the air stability of n-type OTFTs can be improved by inserting a hydrophobic polymer interfacial layer at the dielectric/organic semiconductor interface.

5.4 Examples of Interfacial Layer Materials

There are a variety of materials that have been used for engineering the interfaces of OTFTs. The most widely used materials are self-assembled monolayers (SAM) [15, 16, 24-26]. SAMs are 2D molecular assemblies of organic molecules forming spontaneously on surfaces using chemisorption [2]. SAMs provide versatile approaches to modulate the interfacial properties of OTFTs, which enhances the stability and performance of the device [2, 25]. In addition, there are other materials that have been used to modify these interfaces, such as transition metal oxides [12] and 7,7,8,8-Tetracyanoquinodimethane (TCNQ) [14, 27]. Transition metal oxides are usually used to modify the metal/organic semiconductor

interface, and they are used to control the work function of the metal. Inserting a transition metal, such as MoO_3, between aluminum and pentacene reduces the contact resistance and provides protection against metal diffusion into the organic semiconductor [12]. TCNQ has also been used as an interfacial layer to enhance device performance. Modifying copper electrodes with nanometer-sized copper TCNQ increases the electrode/organic semiconductor contact area and reduces the contact resistance [14].

In this work, we have investigated three interfacial materials for engineering the interfaces of OTFTs. These are virgin graphene oxide (GO), poly(oligo (ethylene glycol) methyl ether methacrylate- glycidyl methacrylate- lauryl methacrylate) (P(OEGMA-GMA-LMA)), and a composite of GO and P(OEGMA-GMA-LMA). These interfacial materials were used to modify both the electrode and the dielectric surfaces of the device. The reasons for choosing these materials are discussed in the following paragraphs.

The first interfacial material we investigated was virgin graphene oxide (GO). GO was chosen as an interfacial material because it is chemically compatible with organic semiconductors [28], and it is a suitable surface for the deposition of organic semiconductors. GO is also compatible with gold electrodes. Gold is used as a source and drain electrode in the devices reported in this work, which is discussed in the next chapter. GO surfaces possess a high surface energy [28], which shows good wetting properties with polar and non-polar solvents. Furthermore, GO is relatively inexpensive, has low toxicity, and is compatible with photolithographic fabrication processes. It has also been shown that using covalently linked GO-Au electrodes improves the charge injection process of OTFTs [28]. To this date, scientific publications have reported the employment of either

chemically modified/anchored GO or reduced GO (RGO) for the modification of BGBC OTFT interfaces. To the best of our knowledge, there are no published reports where virgin GO was employed for this purpose. In this work, we have investigated the impact of a virgin ("as-received") GO localization at the electrode/organic semiconductor interface and the dielectric/organic semiconductor interface.

The second interfacial material we investigated was poly(oligo (ethylene glycol) methyl ether methacrylate- glycidyl methacrylate- lauryl methacrylate), which is denoted as P(OEGMA-GMA-LMA). P(OEGMA-GMA-LMA) is a cross-linkable amphiphilic copolymer that can form a covalent bonding with surfaces. It is synthesized in the lab through a radical polymerization method in a solution environment [29]. The chemical structure of P(OEGMA-GMA-LMA) is shown in Figure 5.2. As shown in this figure, it is prepared from three monomers: oligo (ethylene glycol) methyl ether methacrylate (OEGMA), glycidyl methacrylate (GMA), and lauryl methacrylate (LMA). OEGMA is a polar monomer and ensures the water solubility of the molecule [30]. GMA is insoluble in water and performs as a reactive part [31]. LMA is a hydrophobic monomer that is used to balance the hydrophilic/hydrophobic characteristic of the copolymer [32]. P(OEGMA-GMA-LMA), as far as we know, has never been used before as an interfacial layer in OTFTs. It is used in this work as an interfacial layer at both electrode/organic semiconductor and dielectric/organic semiconductor interfaces, and its impact on the performance of devices is investigated.

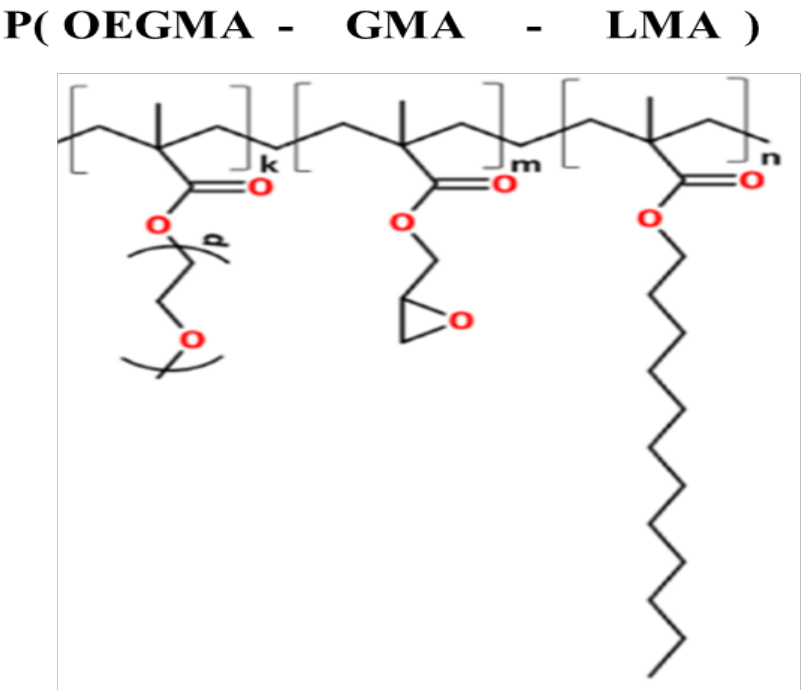

Figure 5.2: Chemical structure of P(OEGMA-GMA-LMA).

The third interfacial material investigated was a composite of GO and P(OEGMA-GMA-LMA). In the GO–P(OEGMA-GMA-LMA) solution, the OEGMA monomer enhances the water solubility of the molecule since it is a polar monomer [30], the GMA monomer reacts with the functional groups of GO through its epoxy groups [31], and the LMA monomer allows for the modified GO sheets to attach to the non-polar polypropylene and balances the hydrophilic/hydrophobic characteristic of the copolymer [32]. The P(OEGMA-GMA-LMA) solution, which is soluble in water, can chemically attach to GO to make it compatible with both hydrophilic and hydrophobic materials. During the composite preparation, a nanolayer of P(OEGMA-GMA-LMA) envelopes the GO sheets, which could elevate the dispersion of the GO in the polymer matrix. It also yields chemical

bonding between the modified GO sheets and the surrounding matrix, which will improve the load transfer and consequently the mechanical properties of the composites. The GO–P(OEGMA-GMA-LMA) composite, as far as we know, has not been used before as an interfacial layer in OTFTs. In this work, we are using it to modify both the electrode and the dielectric surfaces of the devices.

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CHAPTER SIX

DESIGN OF ORGANIC THIN-FILM TRANSISTORS

6.1 Introduction

The goal of this research work is to design, fabricate, and characterize organic thin-film transistors (OTFTs) with various interfacial layers. We present an original device design and photolithographic fabrication process for OTFTs with poly(3-hexylthiophene-2, 5-diyl) (P3HT) as the organic semiconductor material. The fabrication process is efficient, cost-effective, and relatively straightforward to implement. Most of the fabrication steps are performed at room temperature and atmospheric pressure, with the only exceptions being the high temperatures used for annealing the films and the low pressures used for depositing the metal contacts. The fabricated devices are characterized electrically by performing current-voltage (I-V) measurements and extracting primary device performance parameters. In particular, the threshold voltage and the field-effect mobility of the devices were extracted from the linear operation region of the drain current. The morphology of the P3HT was analyzed using atomic force microscopy (AFM). The fabrication process resulted in devices that have a relatively high mobility in comparison to many other P3HT based OTFTs. The devices are repeatable, and consistent over multiple wafers. The fabrication process is presented in detail in Chapter 7, and the electrical measurement results of the devices are presented and discussed in Chapter 8.

The ultimate goal of this research work is not just to develop a fabrication process and characterize devices, rather, to enhance the performance of OTFTs using an interface

engineering method. We investigate the performance of P3HT based OTFTs with an extra material layer deposited at the interface. The interfacial material was inserted at the electrode/organic semiconductor and dielectric/organic semiconductor interfaces, modifying both the electrode and dielectric surfaces. We have investigated three different interfacial materials: GO, P(OEGMA-GMA-LMA), and a GO–P(OEGMA-GMA-LMA)) composite. The GO interfacial layer resulted in an increased field-effect mobility, the P(OEGMA-GMA-LMA) interfacial layer resulted in a decreased threshold voltage, and the GO–P(OEGMA-GMA-LMA) interfacial layer resulted in an increased field-effect mobility and a decreased threshold voltage of the device. The increased field-effect mobility and the decreased threshold voltage are the optimum characteristics of these transistors. Since high mobility results in fast device operation, and small threshold voltage leads to low power consumption. These results are explained in detail in Chapters 9, 10, and 11. However, in this chapter we will present the device design and the materials chosen for the OTFTs.

6.2 Device Design

The design for the OTFTs is based on the bottom gate bottom contact (BGBC) structure. The BGBC structure is chosen because of its geometry that is suitable for a straightforward and cost-effective photolithographic fabrication process. The devices were fabricated on a 500 μm thick degenerately doped p-type silicon wafer with a resistivity in the range of 0.001 – 0.005 Ω-cm. The degenerate doping was chosen in order to form a high-quality, low resistance ohmic contact to the gate metal. The gate insulator was a

300 nm thick, thermally grown SiO_2 layer that was deposited on top of the degenerately doped silicon substrate. The gate contact was aluminum and was deposited onto the backside of the wafer. The organic semiconductor was P3HT, which was deposited onto the oxide layer. The schematic structure of the device is illustrated in Figure 6.1. The thickness of each layer is illustrated in the figure. A thin layer of chromium is also shown in the figure. The chromium layer is used as an adhesion layer between the gold and SiO_2. The P3HT is shown to overlap over the electrodes. The device structure is designed this way to ensure complete coverage of the channel area, and the electrode side walls.

The source and drain contacts were gold, deposited onto the front side of the wafer with a thin adhesion layer of chromium. The top view of the source and drain contacts are illustrated in Figure 6.2. In the electrodes design, there are two big gold square surfaces (2 mm x 2 mm) with small gold rectangle extensions (1 mm x 0.5 mm) in the middle. The two big square surfaces are used to make an external connection to the source and drain electrodes. During measurement the probe tips will land on these surfaces. The width of the small rectangles is used to determine the channel width of the device, which is 500 μm. The space between the two rectangles determines the channel length of the device, which is 50 μm, thus achieving a channel width to length ratio of 10. As shown in the drain current equation of the compact DC model in chapter 3, it is good for transistors to have as high channel width to length ratio as possible since it leads to high drain current.

To enhance the performance of the OTFTs, the devices were modified using an interface engineering method. The interfaces of the devices were engineered by inserting an interfacial material at the electrode/organic semiconductor and dielectric/organic

semiconductor interfaces. The interfacial material is essentially deposited underneath the P3HT, onto the SiO_2 surface and the source/drain sidewalls. The schematic structure of the device with an interfacial layer is illustrated in Figure 6.3.

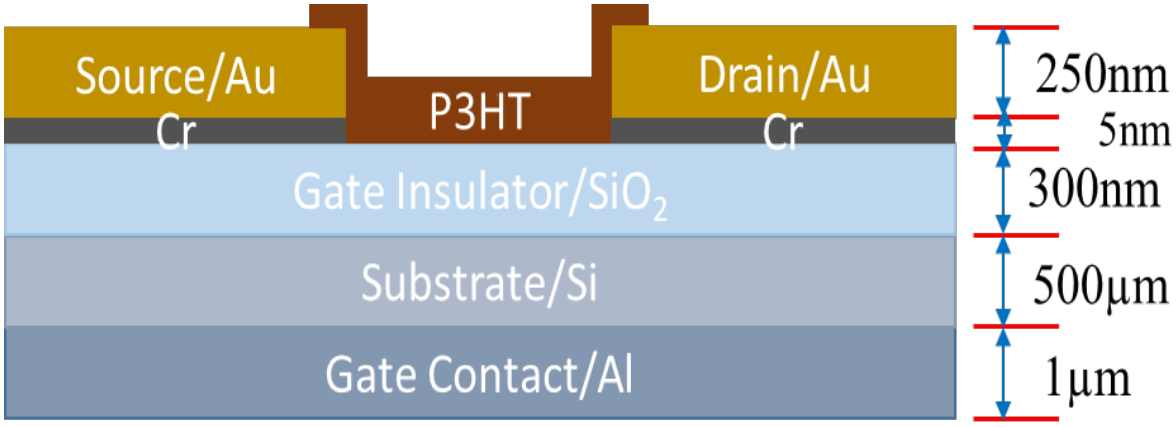

Figure 6.1: Schematic structure of P3HT based OTFT

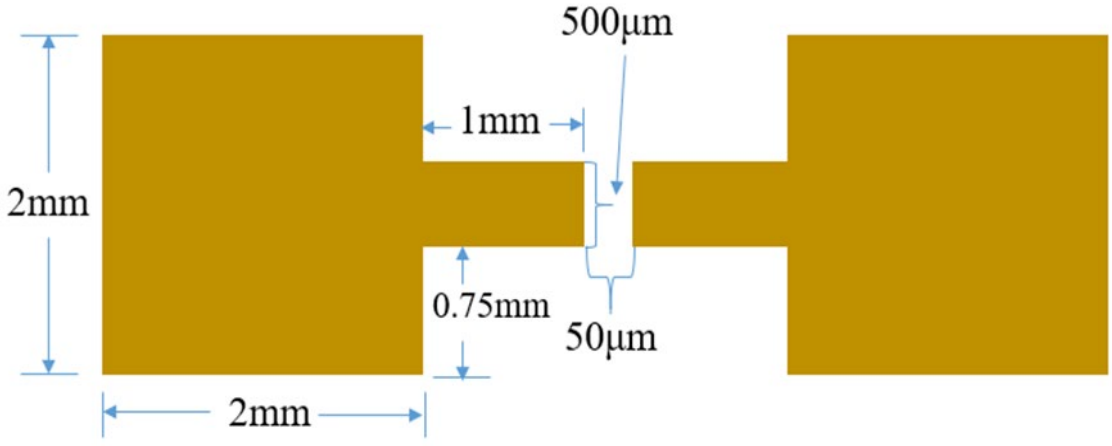

Figure 6.2: Top view of the source and drain contacts with their dimensions.

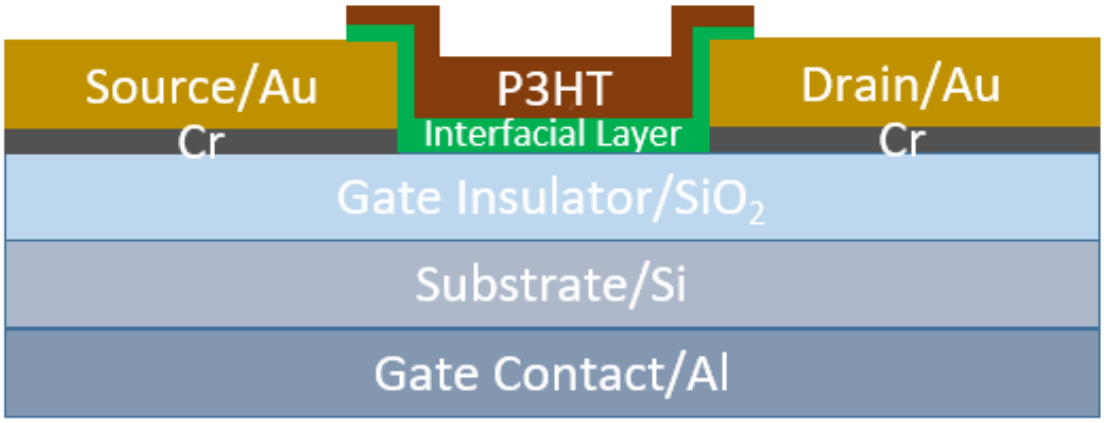

Figure 6.3: Schematic structure of P3HT based OTFT with an interfacial layer

6.3 Preparation of P3HT

As discussed in Chapter 2, P3HT has the highest mobility and the best electrical properties among p-type polymers. Its electrical properties, as well as its chemical and environmental stability, have improved tremendously since its original synthesis in the 1990s [1]. P3HT is also soluble in organic solvents, which makes it suitable for solution processing. Thus, P3HT was selected as the organic semiconductor material in this work.

We used Poly(3-hexylthiophene-2, 5-diyl), regioregular Electronic grade with regioregularity greater than or equal to 90%. It was obtained from Rieke Metals in powder form. According to the manufacturer, the average molecular weight was 50,000 – 70,000 gram/mole. Chloroform was used to dissolve the powder and form a P3HT solution; 25 grams of chloroform was applied for 0.12 gram of P3HT, resulting in a solution of 0.48 wt. %.

6.4 Selection of Electrode Materials

In general, there are three electrodes in OTFTs: source, drain, and gate. The source and drain electrodes are typically made with the same material. Some of the materials that have been used to fabricate the source and drain contacts are gold [2], aluminum [3], silver [4], copper [5], and palladium [6]. The gate can be made with the same material as the source and drain [7], or with a different material [2, 4]. The particular choice of the electrode material is crucial to obtain high performance transistors. Selecting the proper electrode material helps in lowering the contact resistance and the interface potential barrier at the electrode/organic semiconductor interface. Low contact resistance and interface barrier height at the source-drain electrode/organic semiconductor interface results in a high injection of charge carriers from the electrode into the organic semiconductor. Therefore, the electrode materials must be selected carefully to enable maximum performance of transistors.

When selecting a source and drain metal contact, the work function of the metal must align as closely as possible to the HOMO energy level of a p-type organic semiconductor or the LUMO energy level of an n-type organic semiconductor [8]. The mismatch between the work function of the metal and the HOMO or the LUMO energy level of the organic semiconductor creates an energy barrier. This energy barrier limits the injection of charge carries from the electrode into the organic semiconductor. For the OTFTs fabricated in this work, we chose gold to be the source and the drain electrode. Gold has a work function of 5.1 eV [9]. Since P3HT is used as the organic semiconductor material, which is a p-type organic semiconductor with a HOMO energy level of 5.2 eV

[10], the interface barrier between gold and P3HT is 0.1 eV. Because of this small interface barrier, gold is an optimum choice for the source and drain electrode. The energy band diagram of gold and P3HT are illustrated in Figure 6.4. The fermi energy level of gold is illustrated in the figure, which is used to determine the work function of gold. The work function is essentially the energy difference between the fermi level and the vacuum level, which is a reference point at zero potential energy.

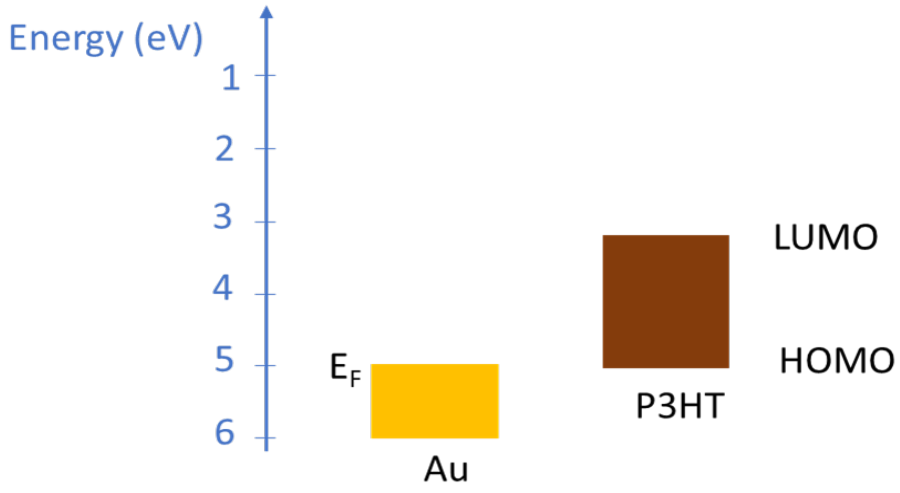

Figure 6.4: Energy band diagram of gold and P3HT

The gate electrode is deposited onto a degenerately doped silicon substrate. In order to make a good ohmic contact, the work function of the gate electrode must be closer to the work function of the degenerately doped silicon substrate. The gate electrode also needs to have a good adhesion property with the silicon substrate to ensure a proper gating. Aluminum was selected for the gate electrode. The work function of aluminum is 4.28 eV [9]. The work function of the degenerately doped silicon substrate is 3.9 eV [11]. This

results in an interface barrier that is less than 1 eV, specifically 0.38 eV in this case. Therefore, aluminum was chosen as the gate electrode in this work.

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CHAPTER SEVEN

DEVELOPMENT OF AN EFFICIENT ORGANIC THIN-FILM TRANSISTOR FABRICATION PROCESS

7.1 Introduction to the Fabrication Process

An initial fabrication process for OTFTs was developed in Clemson University's main campus laboratories, located in Sirrine and Rhodes Halls, using relatively crude equipment. The fabrication yielded functional OTFTs with reasonably good electrical characteristics. However, the results were inconsistent since we could not control the device geometry very well. The fabrication was performed in an open environment, which made the devices susceptible to contamination. Furthermore, the fabrication was performed on pieces of wafers, limiting the fabrication to a maximum of 4 devices per sample. Therefore, developing a new fabrication process was necessary in order to fabricate devices that are repeatable, consistent throughout the wafer, and have high-performance characteristics. In addition, we wanted to develop a fabrication process that has a capability of wafer level production and could be applied at the industry level.

Therefore, we developed a photolithography fabrication process in a cleanroom laboratory at the Advanced Materials Research Laboratory (AMRL) at Clemson University to produce consistent OTFTs. The fabrication process can be divided into four stages. The first stage is removing the native oxide layer from the back of the wafer and depositing the gate contact (aluminum). The second stage is depositing the source and drain contacts (gold) and patterning them. The third stage is depositing the organic semiconductor (P3HT). The fourth and final stage is patterning the conducting channel (P3HT). In the

next few sections, we will discuss each stage of the fabrication process including the instruments used for the fabrication process.

7.2 Instruments Used for Fabrication

Several instruments were used to fabricate the OTFTs in the cleanroom laboratory. The primary instruments include the Semitool Spin Rinse Dryer (SRD), Cee-Brewer Science spin coater and developer, Cee-Brewer hot plates, Tencore Alpha Step 200 Profilometer, Plasma-Therm Versaline ICP, GCA 5:1 Reduction i-line Optical Stepper, Neutronix-Quintel 1x Aligner, and CHA Mark 40 Electron Beam Evaporator.

The Semitool SRD was used to clean the wafers using DI water rinsing and N_2 drying. The Cee-Brewer Science spin coater was used to spin coat both the negative and positive photoresists and the P3HT. The Cee-Brewer Science developer was used to develop the photoresists. The hot plates were used to anneal the films (both the photoresists and the P3HT). The Tencore Alpha Step 200 Profilometer was used to measure the thickness of the P3HT. The Plasma-Therm Versaline ICP was used to clean the wafers and dry etch the P3HT by applying an oxygen plasma to the wafers. The GCA 5:1 Reduction i-line Optical Stepper was used to perform 5x reduction photolithography steps. The Neutronix-Quintel 1x Aligner was used to perform 1x reduction photolithography steps. The CHA Mark 40 Electron Beam Evaporator was used to deposit the metal contacts: Aluminum for the gate contact and Gold for the drain and source contacts.

7.3 Deposition of the Gate Contact

The devices were fabricated on thermally oxidized silicon wafers, obtained from UniversityWafer, Inc., with a diameter of 100 mm. In order to deposit the aluminum gate contacts onto the back side of the wafer, the native oxide layer normally found on silicon wafers was removed using hydrofluoric (HF) acid. This ensures the aluminum metal will have a direct contact with the degenerately doped silicon resulting in a good ohmic contact. Prior to the HF etching, the front side of the wafer was coated with a positive photoresist, AZ 701, to protect the oxide layer from damage. The photoresist was spin coated at an acceleration of 2000 rpm/sec until a maximum speed of 1000 rpm was reached and maintained for 5 seconds. This was immediately followed by an acceleration of 2500 rpm/sec until a maximum speed of 3000 rpm was reached and maintained for 45 seconds, resulting in a thickness of 965 nm. The photoresist was then baked on a hot plate at 95 ˚C for 90 seconds.

Since the front side of the wafer at this point is covered with the photoresist, the oxide from the back side of the wafer can be removed using HF without any damage to the front side. To remove the oxide layer, the wafer was inserted in a buffered oxide etch (5:1) solution for 5 minutes until the back surface of the wafer transformed from hydrophilic to hydrophobic, which indicates the removal of the oxide layer. Silicon surfaces are hydrophobic in nature, whereas SiO_2 surfaces are hydrophilic [1, 2]. Once the oxide layer was completely removed from the back side, the wafer was rinsed with DI water several times in three different beakers to remove the HF, and then dried with a N_2 jet. The wafer was then placed in an SRD tool for a final cleaning process. Once HF was rinsed from the

wafer surfaces, the wafer was placed in an Electron Beam Evaporator, CHA Mark 40, to deposit a 1 μm thick layer of aluminum at a pressure of 4.7 x 10^{-7} Torr. The positive photoresist, that was on the front side of the wafer, was then removed using acetone, which will not damage or contaminate the aluminum.

7.4 Deposition of the Drain and Source Contacts

In order to deposit the drain and source contacts, the wafer was first cleaned with methanol to remove coarse dusts and dried with a N_2 jet. The wafer was then exposed to an oxygen plasma for 20 seconds in a Plasma-Therm Versaline ICP, at 25 W of RF bias power and 800 W of ICP power, to remove impurities and contamination from the front surface of the wafer. In order to optimize the oxygen plasma etching time to clean the wafer, we experimented with longer time durations, up to 3 minutes. However, the longer etching times resulted in more than cleaning the wafers, they also etched the SiO_2 and resulted in a significant leakage current through the SiO_2 layer. Thus, after experimenting with different oxygen plasma times, we found that the optimal time to clean the wafers is less than 40 seconds with low bias powers. Therefore, we applied an oxygen plasma for 20 seconds before depositing the source and the drain contacts, as well as another 20 seconds later in the process just before depositing the P3HT layer, for a total of 40 seconds.

Once this cleaning process was completed, a Lift-off resist, LOR 3A, was spin coated onto the front side of the wafer at an acceleration of 250 rpm/sec until a maximum speed of 500 rpm was reached and maintained for 5 seconds. This was immediately followed by an acceleration of 750 rpm/sec until a maximum speed of 1500 rpm was reached and

maintained for 30 seconds. The LOR-3A was then baked on a hot plate at 175 ˚C for 5 minutes. After a reasonable time for the wafer to cool down, a negative photoresist, AZ 5510, was spin coated on top of the LOR-3A at an acceleration of 5000 rpm/sec until a maximum speed of 1000 rpm was reached and maintained for 2 seconds. This was immediately followed by an acceleration of 2000 rpm/sec until a maximum speed of 3000 rpm was reached and maintained for 45 seconds. The negative photoresist was then baked on a hot plate at 95 ˚C for 60 seconds and subsequently cooled down for 2 minutes.

To pattern the source and drain structures, photolithography was performed using a GCA 5:1 Reduction i-line Stepper. The reticle that was designed for this purpose was made of quartz with dimensions of $5 \times 5 \times 0.09$". The pattern on the reticle is shown in Figure 7.1a, where the top half represents the pattern for the top metal contacts (source and drain) and the bottom half represents the pattern for the channel (P3HT). Close-up images of the top half and the bottom half of the reticle are shown in Figures 7.1b and 7.1c, respectively. There are also alignment marks on the top half of the reticle to align the wafer to the reticle during the second photolithography step. These marks are so small and cannot be seen in the figure. Since the stepper is a 5x reduction stepper, all the dimensions on the reticle are five times larger than the dimensions of the pattern ultimately produced on the wafer. The dark features that are shown in Figure 7.1 represent chrome on the quartz reticle, meaning when UV light shines on the reticle, the chrome features block the light from going through the reticle and onto the wafer below.

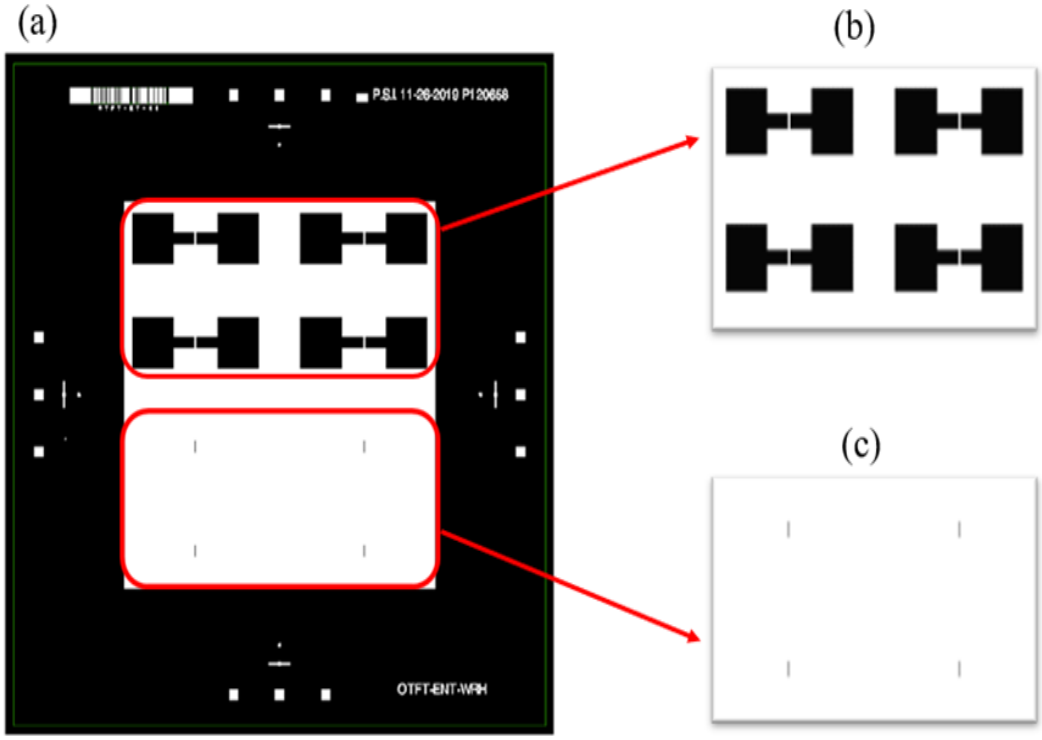

Figure 7.1: (a) Reticle pattern for the top metal contacts (source and drain) and the channel (P3HT), (b) close-up pattern for the top metal contacts, and (c) close-up patttern for the channel.

The photoresists were exposed to UV light for 0.3 seconds at a focus offset of 0.15 µm. This exposure was performed through the top half of the reticle since we were only patterning the top metal contacts, as illustrated in Figure 7.1b. The bottom half of the reticle was covered using blades. After the exposure was completed, the photoresists were baked at 110 ˚C for 60 seconds and subsequently cooled down for 2-minutes. The photoresists were then developed using a developer solvent, AZ 300 MIF, for 90 seconds. Since we used a negative photoresist on top of the wafer, the exposed regions of the photoresist remained on the wafer and the unexposed regions were dissolved away during the

development process. The alignment marks were also printed in this photolithography step as they were located on the top half of the reticle. The wafer was then placed in an Electron Beam Evaporator to deposit the top metal contacts. A 5 nm layer of chromium was first deposited as an adhesion layer between the gold and SiO_2, and subsequently a 250 nm layer of gold was deposited on top of the chromium. Both the gold and chromium depositions were performed at a pressure of 6×10^{-6} Torr.

The whole wafer was covered by the chromium/gold deposition at this point in the fabrication process. However, since we had a patterned photoresist underneath the chromium, lift-off was performed to obtain the desired source and drain patterns. To perform the lift-off, the wafer was inserted into an Ultrasonic NMP (1-Methyl-2-Pyrrolidinone) solution at 65 ˚C. The regions of the chromium/gold that had photoresist underneath were lifted-off, whereas the regions that did not have any photoresist underneath remained on the wafer. The alignment marks were also patterned during this process. The schematic structure of the device after the lift-off process was completed is illustrated in Figure 7.2. As illustrated in the figure, the chrome/gold layers were patterned, and the channel area was just bare SiO_2.

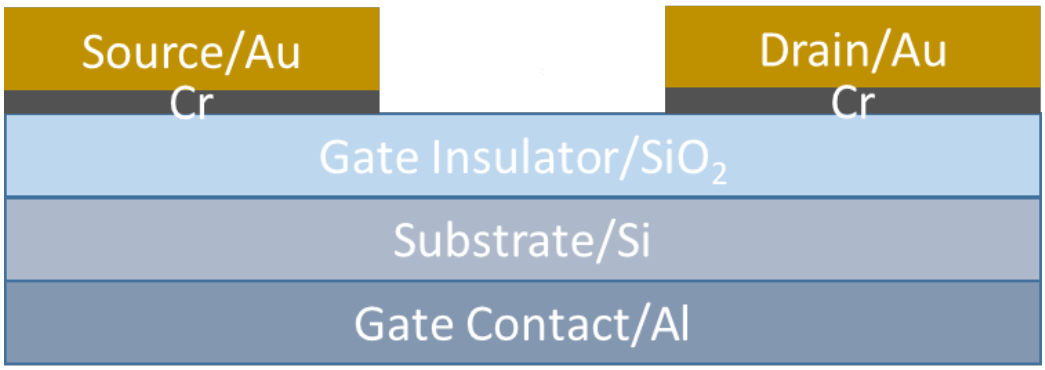

Figure 7.2: Schematic structure of the device after the top contacts (chrome/gold) were deposited and patterned.

7.5 Deposition of P3HT

To deposit the P3HT and define the channel dimensions of the transistors, the wafer was first cleaned using acetone and methanol, and dried with a N_2 jet. Then the wafer was exposed to an oxygen plasma for 20 seconds to clean the front surface of the wafer of any contamination or impurities.

After the cleaning process was completed, P3HT was spin coated onto the wafer at an acceleration of 1000 rpm/sec until a maximum speed of 2000 rpm was reached and maintained for 60 seconds, and subsequently baked at 110 ˚C for 1 hour. After sufficient time for the wafer to cool down, the thickness of the P3HT was measured using a Tencore Alpha Step 200 Profilometer, and the thickness was found to be 58 nm. A positive photoresist, AZ 701, was then spin coated on top of the P3HT at an acceleration of 2000 rpm/sec until a maximum speed of 1000 rpm was reached and maintained for 5 seconds. This was immediately followed by an acceleration of 2500 rpm/sec until a

maximum speed of 3000 rpm was reached and maintained for 45 seconds. Subsequently, the photoresist was baked on a hot plate at 95 ˚C for 60 seconds. After sufficient time for the wafer to cool down, a second photolithography step was performed using the GCA 5:1 Reduction i-line Stepper to define the channel dimensions of the transistors. Prior to the UV exposure, the wafer was aligned to the reticle using the alignment marks printed on the wafer during the first photolithography step. This avoids any misalignment between the source/drain patterns and the P3HT pattern. The positive photoresist was the exposed to UV light for 0.3 seconds at a focus offset of 0.15 μm. The reticle used for this exposure was the same reticle as shown in Figure 7.1. However, this time the exposure was performed through the bottom half of the reticle as shown in Figure 7.1b, which is the pattern for the P3HT channel. The top half of the reticle was covered using blades. After the UV light exposure was completed, the wafer was baked at 110 ˚C for 60 seconds and then developed using the AZ 300 MIF developer for 45 seconds. Since we used a positive photoresist, the regions that were exposed to the UV light were dissolved away by the developer, whereas the regions that were not exposed to the UV light remained on the wafer. The schematic structure of the device after the photoresist was patterned is illustrated in Figure 7.3. As illustrated in the figure, the photoresist that was on top of the P3HT was patterned, and the P3HT was covering the whole wafer.

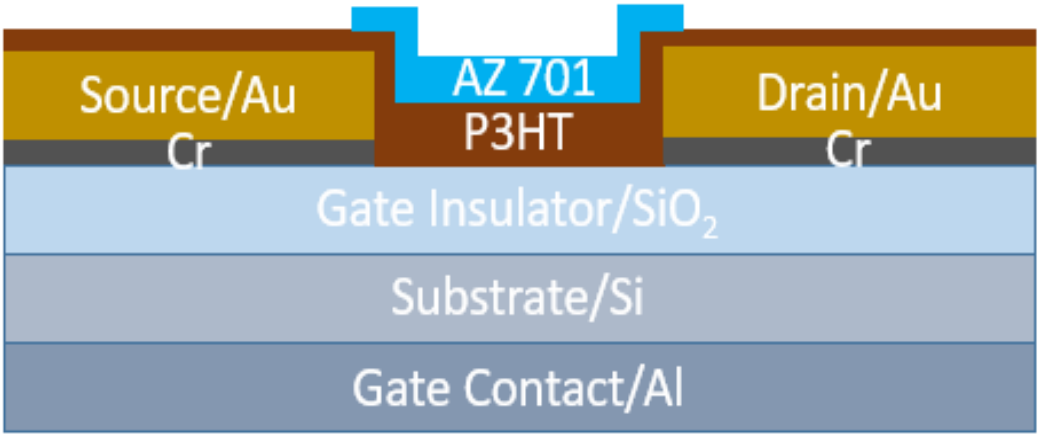

Figure 7.3: Schematic structure of the device after the photoresist was patterned for the channel.

7.6 Formation of the Conducting Channel

To remove the P3HT located outside of the channel areas, an oxygen plasma was applied for 30 seconds using a Plasma-Therm Versaline ICP at 25W of RF bias power and 800W of ICP power. The P3HT covering the channel area was protected by the photoresist and defined by the second photolithography step. The oxygen plasma etches the photoresist as well, but it was not powerful or long enough to etch through the 965 nm thickness of the photoresist. The schematic structure of the device after the P3HT located outside the channel areas was removed is illustrated in Figure 7.4. As illustrated in the figure, the P3HT was patterned but there was a layer of photoresist on top of the P3HT that needed to be removed. To remove this photoresist, the third and final photolithography step was performed. The photoresist was exposed to UV light using a contact printer, Neutronix-Quintel 1x Aligner, without a mask for 24 seconds, and subsequently developed using AZ

300 MIF developer for 45 seconds and removed the remaining photoresist. The 1x Aligner was used for flood exposure only. We attempted using acetone to remove the photoresist prior to developing this photolithography step; however, even though the acetone removed the photoresist effectively, it also removed the P3HT from some parts of the channel areas across the wafer.

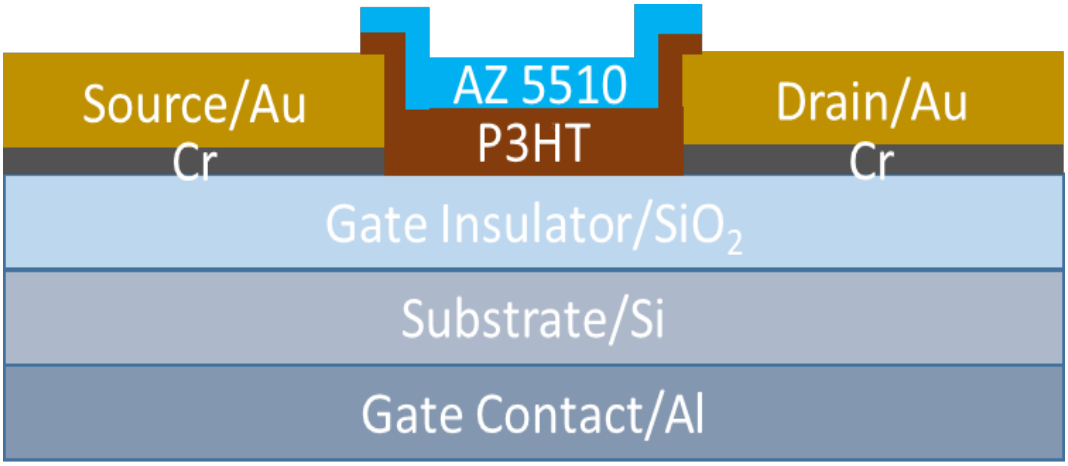

Figure 7.4: The schematic structure of the device after the P3HT channel was patterned

After the development process was completed, the wafer was annealed at 110 ˚C for 1-hour on a hot plate to evaporate any water or developer solvent the P3HT might have absorbed during the development process. The thickness of the P3HT was measured again to ensure that it was not dissolved by the photoresist or developer solvent, and the thickness obtained was practically the same as the measurement result obtained prior to the photoresist coating on top of the P3HT. The wafer was then annealed again at 110 ˚C for 2-hours; however, this time the annealing was performed in a nitrogen air environment

using an oven. The purpose of this anneal is to improve the electrical characteristics of the P3HT. It is shown that annealing increases the size of polymer crystals (grains), and thereby, the mobility [3, 4]. The morphology of the P3HT after the extended annealing was examined using AFM, and the resulting image is shown in Figure 7.5. It appears that the P3HT structural grains have good interconnectivity with each other, which is good for a current flow in the channel of the transistors [5].

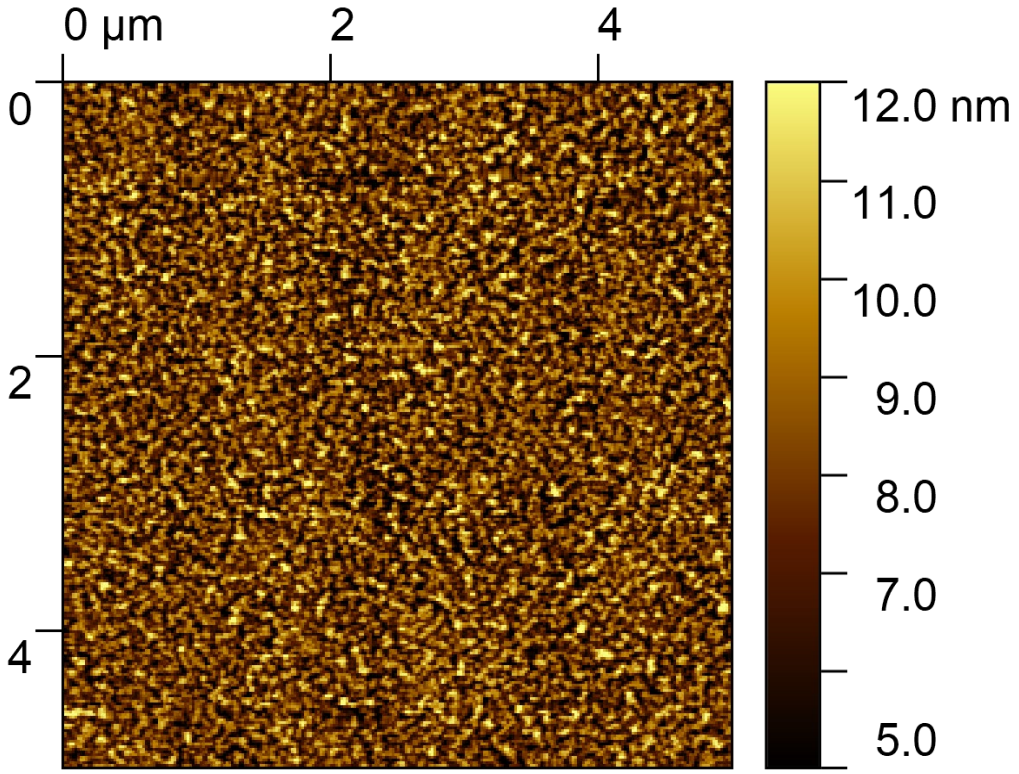

Figure 7.5: AFM image of P3HT on SiO_2.

The schematic structure of the device after the fabrication process was completed is illustrated in Figure 7.6. In Figure 7.6, we illustrate that the P3HT was not only limited

to the channel area (between the edges of the drain and the source) but has a slight overlap over the source/drain electrodes. The reticle for the P3HT was designed this way to ensure complete coverage of the channel and the source/drain sidewalls as well in order to create a larger contact area between the electrode and the organic semiconductor [5]. Increasing the contact area results in lower contact resistance and higher injection rate of charge carriers into the channel, which improves the performance of the device [6, 7].

An image of the wafer taken after the fabrication process was completed is shown in Figure 7.7. As can be seen in the figure, more than 226 transistors were fabricated on a single wafer. It is difficult to see the conductive channel from this figure, but the conductive channel has a length of 50 μm and a width of 500 μm, yielding a width to length ratio of 10.

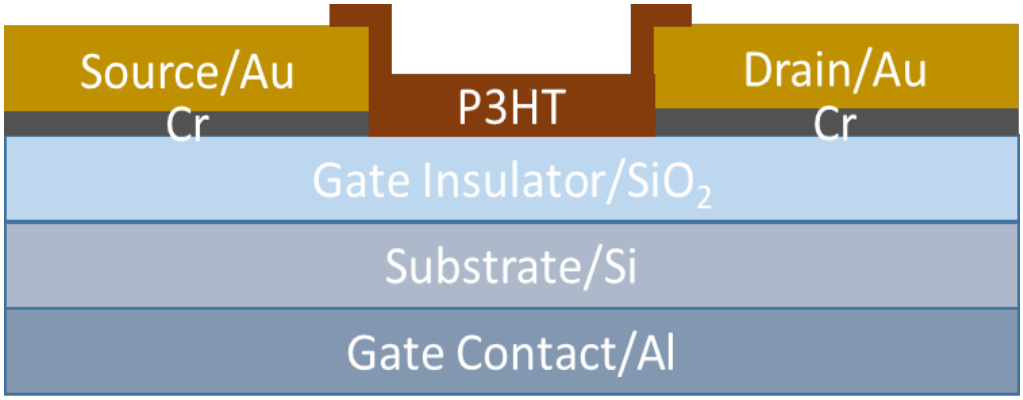

Figure 7.6: Schematic structure of the device after the fabrication process was completed

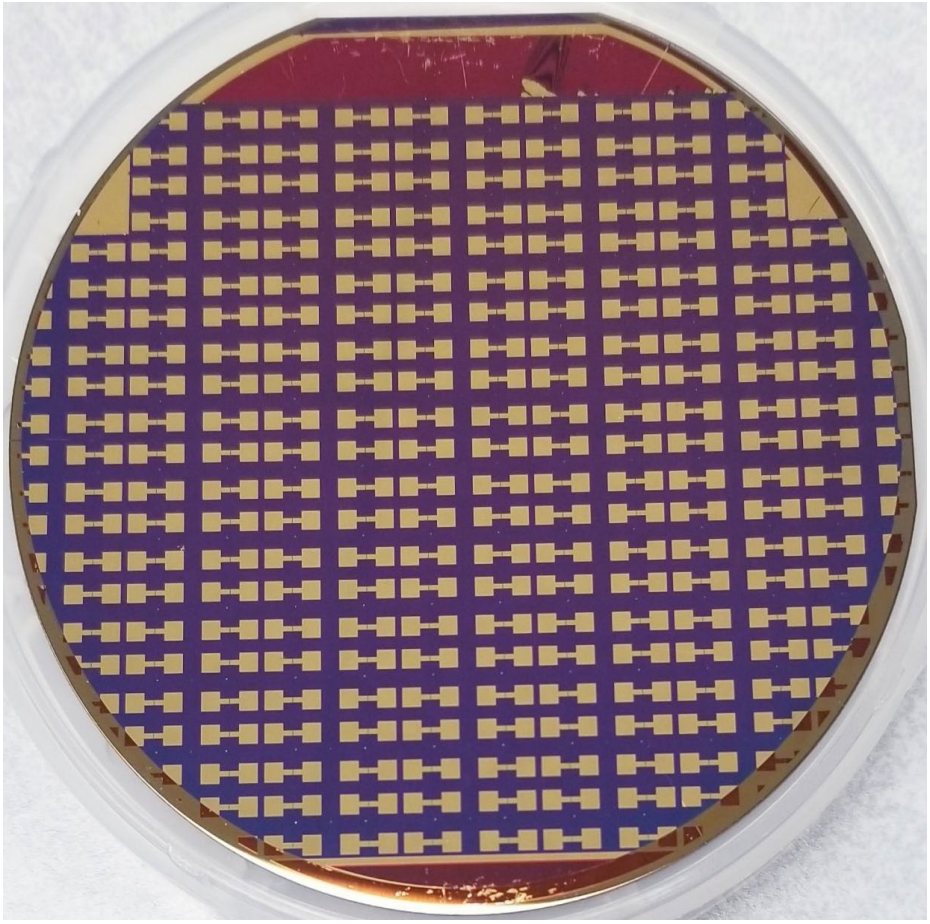

Figure 7.7: Image of a wafer after the fabrication process was completed. More than 226 transistors can be fabricated on a single wafer.

7.7 Conclusions

A photolithographic fabrication process for P3HT based OTFTs was developed. The structure of the devices was based on the bottom gate bottom contact OTFT. The fabrication process followed four stages. The first stage was deposing the gate contact. The second stage was depositing and patterning the source and drain contacts. The third stage

was depositing the P3HT. The fourth stage was patterning the P3HT. The fabrication process was cost-effective and straightforward to implement. Most of the fabrication process occurred at room temperature and atmospheric pressure. The electrical characteristics of the devices were subsequently found to be consistent, and repeatable over multiple wafers. These results will be presented in the next chapter. The fabrication process allowed us to perform a wafer level mass production of more than 226 devices per wafer based on the device geometry.

7.8 References

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CHAPTER EIGHT

POLY(3-HEXYLTHIOPHENE) BASED ORGANIC THIN-FILM TRANSISTORS WITH HIGH MOBILITY

8.1 Introduction

The photolithography fabrication process described in the previous chapter was used to fabricate bottom gate bottom contact (BGBC) P3HT based OTFTs. The fabrication process was efficient, cost effective, and relatively straightforward to implement. More than 226 devices were fabricated on a single wafer. The fabricated devices are characterized electrically by performing current-voltage (I-V) measurements and extracting primary device performance parameters. In particular, the threshold voltage and the field-effect mobility of the devices are extracted from the linear operation region of the drain current. The mobility of the measured devices is significantly higher than most results reported in the scientific literature for other similar BGBC P3HT based OTFTs. The higher mobility of the devices is associated with the effectiveness of the fabrication process and the annealing of the P3HT.

8.2 Electrical and Material Characterization

Current-voltage (I-V) measurements were performed using an HP-4156B Semiconductor Parameter Analyzer. The drain current vs. drain voltage (I_{DS}-V_{DS}) measurements were performed by applying a drain voltage from 0 V to -70 V with an increment of -0.5 V while biasing the gate with voltages ranging from 0 V to -60 V with an increment of -20 V. The applied drain and gate voltages were negative because P3HT

is a p-type semiconductor, hence negative bias is necessary to turn on the devices and pass significant current through the channel. From this measurement, we can obtain the I_{DS}-V_{DS} plot, which shows the output characteristics of OTFTs. The output characteristics show the linear and saturation operating regions of the transistors, which were discussed in Chapter 3. The drain current vs. grate voltage (I_{DS}-V_{GS}) measurements were performed by applying a gate voltage from 0 V to -60 V with an increment of -0.5 V while biasing the drain at -5 V. The drain is biased at -5 V because -5 V biases the device into the linear region. This is found from the output characteristics of the devices. From this measurement, we can obtain the I_{DS}-V_{GS} plot, which relates the drain current response to the applied gate voltage and shows the transfer characteristics of OTFTs. Using the transfer characteristics, we can obtain the gate voltage at which the transistor starts to conduct significant current, which is essentially the threshold voltage of the device.

8.3 Results and Discussion

Out of the 226 organic thin-film transistors that were fabricated, electrical measurements were performed on more than 24 devices (selected randomly). The measurement results were approximately identical for the vast majority of the 24+ devices. The output characteristics, I_{DS}-V_{DS}, of one of the devices is shown in Figure 8.1, which is representative of the majority of the devices measured. In this plot, we show the variation of the drain current with the applied drain voltage for various gate voltages ranging from 0 V to -60 V with an increment of -20 V. The increase in the magnitude of the drain current with the magnitude of the gate voltage along with the negative polarity of the drain current

confirms the gating property of the transistor and the p-type behavior of the P3HT, respectively.

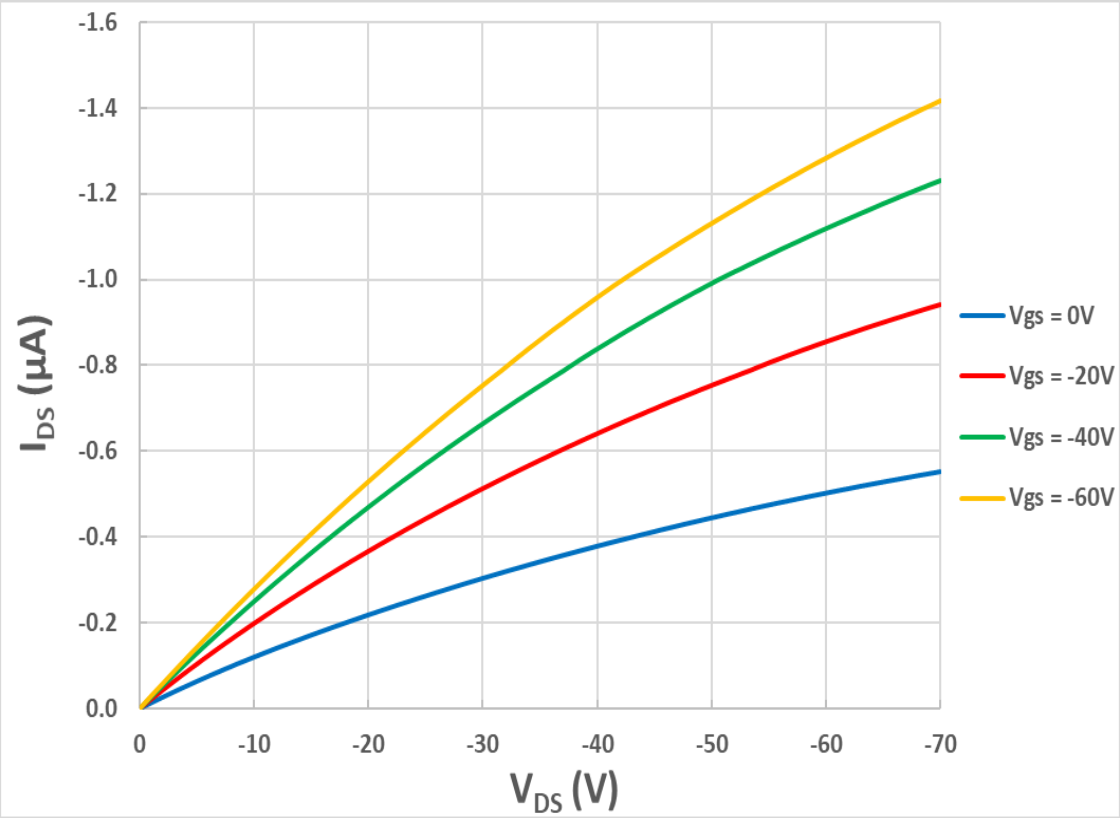

Figure 8.1: I_{DS} - V_{DS} output characteristics of an OTFT at different values of V_{GS}

The output characteristics of the I-V measurements (I_{DS} -V_{DS}), as well as the transfer curves (I_{DS} -V_{GS}), can be used to determine the performance parameters of the transistor. Two of the key performance parameters are calculated from these measurements, the threshold voltage and the field-effect mobility. As explained in Chapter 2, threshold voltage is the minimum gate voltage needed to accumulate a sufficient density of charge carriers at the organic semiconductor/gate insulator interface to form a

conducting channel between the source and the drain [1]. The threshold voltage is extracted using the extrapolation in the linear region (ELR) method [2-4]. In this method, an I_{DS}-V_{GS} curve, referred to as the transfer characteristics, measured at a constant value of V_{DS} that biases the device into a linear region, is linearly extrapolated. An I_{DS}-V_{GS} curve at V_{DS} = -5 V is shown in blue in Figure 8.2, which was measured on the same device as that in Figure 8.1. The extrapolation is normally taken at the maximum slope of the I_{DS}-V_{GS} curve. The equation for calculating the slope of the I_{DS}-V_{GS} curve, the transconductance (g_m), was given in Equation 3.1 and repeated here for reference,

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \tag{3.1}$$

The equation for extracting the threshold voltage was also given in Equation 3.2 and repeated here for convenience:

$$V_{Th} = V_{GSi} - {}^{V_{DS}}/_{2} \tag{3.2}$$

where V_{Th} is the calculated threshold voltage and V_{GSi} is the V_{GS} axis intercept and is obtained from the extrapolation line shown in red in Figure 8.2. For our device, the threshold voltage was found to be V_{Th} = 30.8 V. This threshold voltage is relatively high and not optimal for low power devices. This could be due to a contact resistance between the electrode and the organic semiconductor.

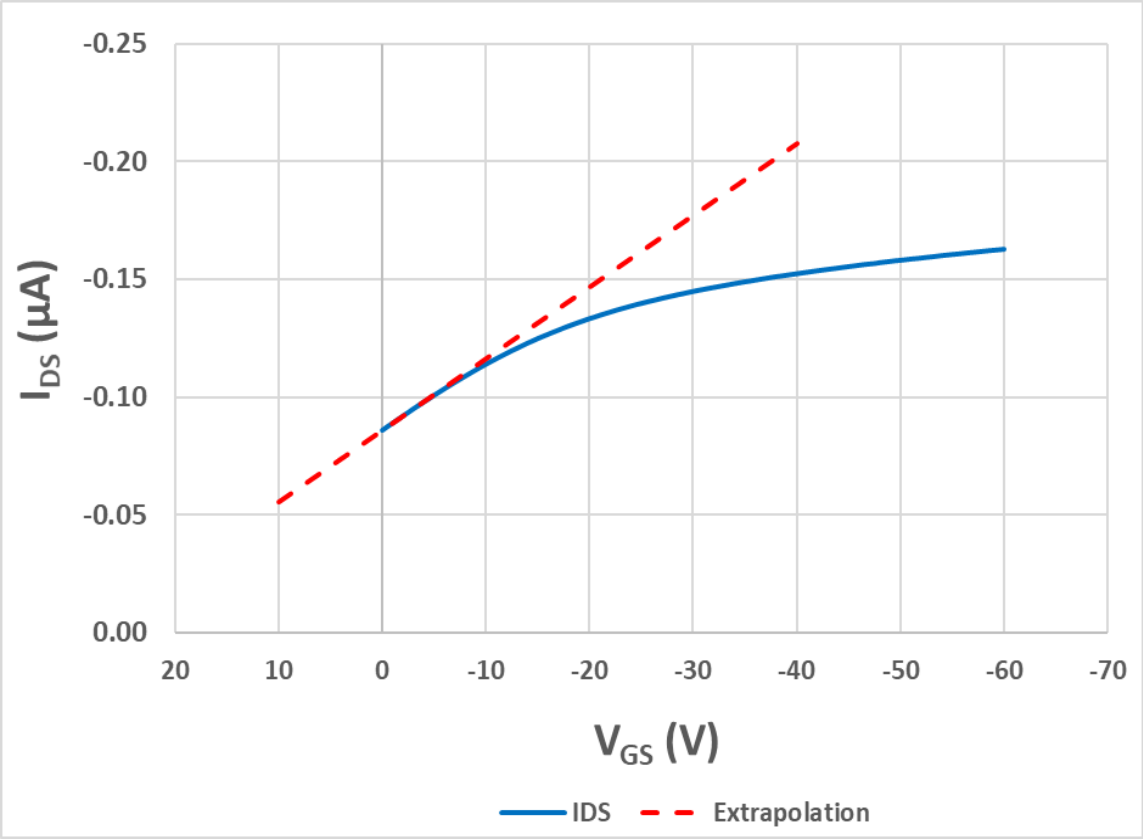

Figure 8.2: Transfer characteristics (I_{DS}–V_{GS}) of an OTFT at V_{DS} = -5 V, along with the linear extrapolation of the I_{DS} – V_{GS} curve at the maximum transconductance.

The mobilities of the devices were also extracted. Mobility is a measure of how fast charge carriers can move across the conducting channel per unit applied electric field. The field-effect mobility in the linear operation region was calculated using Equation 3.5, which is rewritten here for convenience

$$\mu_{lin} = \frac{L}{WC_{OX}V_{DS}} g_m \tag{3.5}$$

where μ_{lin} is the field-effect mobility in the linear region, L is the channel length, W is the channel width, and C_{ox} is the oxide capacitance per unit area. In order to determine the

mobility, we must use the maximum value of g_m in Equation 3.5 which can be extracted from Figure 8.2, and was found to be $g_m = 3.18 \times 10^{-9}\ S$. Thus, using Equation (3.5) for maximum transconductance, the field-effect mobility in the linear region for the device was found to be $5.5 \times 10^{-3}\ {cm^2}/{V_S}$. This result is larger than most values reported in the scientific literature for other bottom gate bottom contact P3HT based OTFTs. For example in [5], the mobility of a bottom gate bottom contact P3HT based OTFT, with the same channel length as our device (50 μm), but different channel width (2 mm) and P3HT thicknesses (23 nm, 41 nm, 86 nm, and 195 nm), is reported to be $2 \times 10^{-4}\ {cm^2}/{V_S}$ to $9 \times 10^{-4}\ {cm^2}/{V_S}$, which is about an order of magnitude smaller than the result reported here. In another example [6], the mobility for a bottom gate bottom contact P3HT based OTFT, again with the same channel length as our device (50 μm), but different channel width (2 mm) and P3HT thickness (20 nm – 30 nm), is reported to be $1.85 \times 10^{-4}\ {cm^2}/{V_S}$, also an order of magnitude smaller.

In both examples above, the gate insulator was SiO_2 with a thickness of 300 nm, and the source and drain contacts were gold, similar to the devices reported in here. However, the devices reported here had a significantly higher mobility. One of the reasons for this high mobility could be due to the fabrication process used in Chapter 7. Namely, the fabrication process was designed to minimize the contamination of the surfaces of the oxide layer and other interfacial layers. Furthermore, optimized temperature and time for annealing the P3HT layer was employed, which had a positive effect on the polymer molecular conformation. In Figure 7.5, we showed an AFM image of P3HT after the

extended annealing. Figure 7.5 is shown below again for convenience. As shown in this figure, the P3HT structural grains are interconnected very well with each other. It has been reported that a good interconnection between the grains of organic semiconductors results in an efficient charge transport in the channel of OTFTs [7]. Thus, we suggest that the interconnectivity contributes to a better current flow in the channel and therefore a higher mobility.

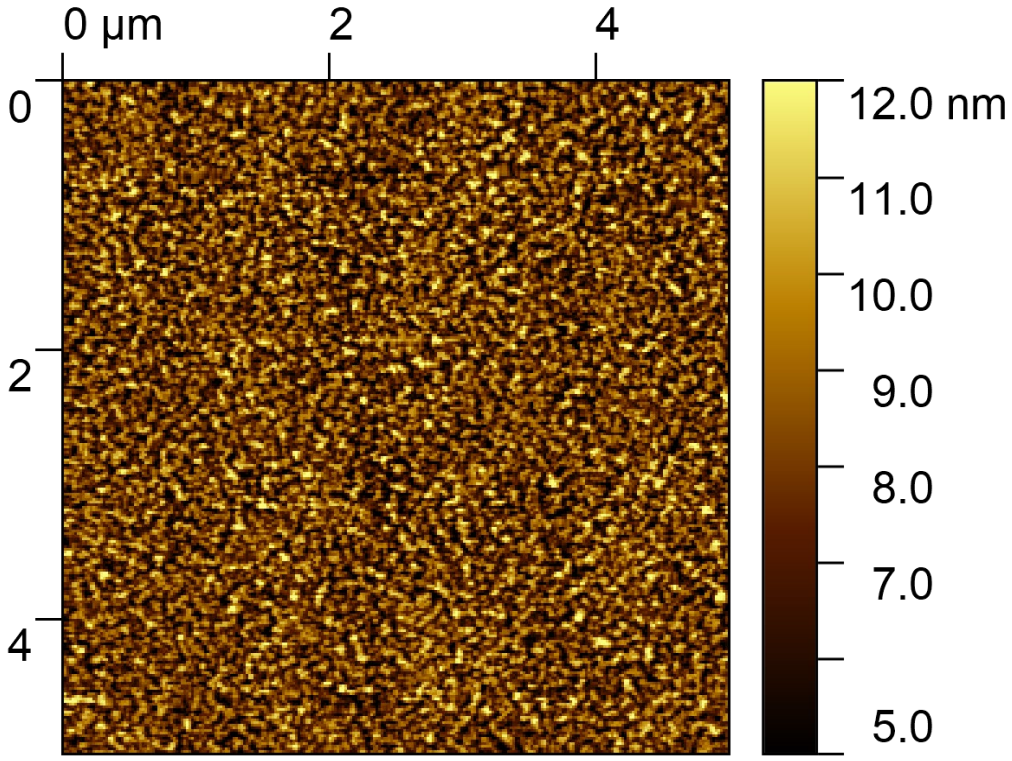

Figure 7.5: AFM image of P3HT on SiO_2.

In Figure 8.3, we show the mobility distribution of the measured 24 devices. From this result, we see that more than 50% of the extracted mobilities are in the range of $4.0 - 6.0 \times 10^{-3}\ {cm^2}/{Vs}$, and the remaining 20% and 25% are in the range of $2.0 - 4.0 \times 10^{-3}\ {cm^2}/{Vs}$ and $6.0 - 8.0 \times 10^{-3}\ {cm^2}/{Vs}$, respectively. This illustrates the consistency and uniformity of the devices across the wafer and therefore the consistency of the fabrication process. The fabrication process presented in the previous chapter and the results reported in this chapter have been published in [8].

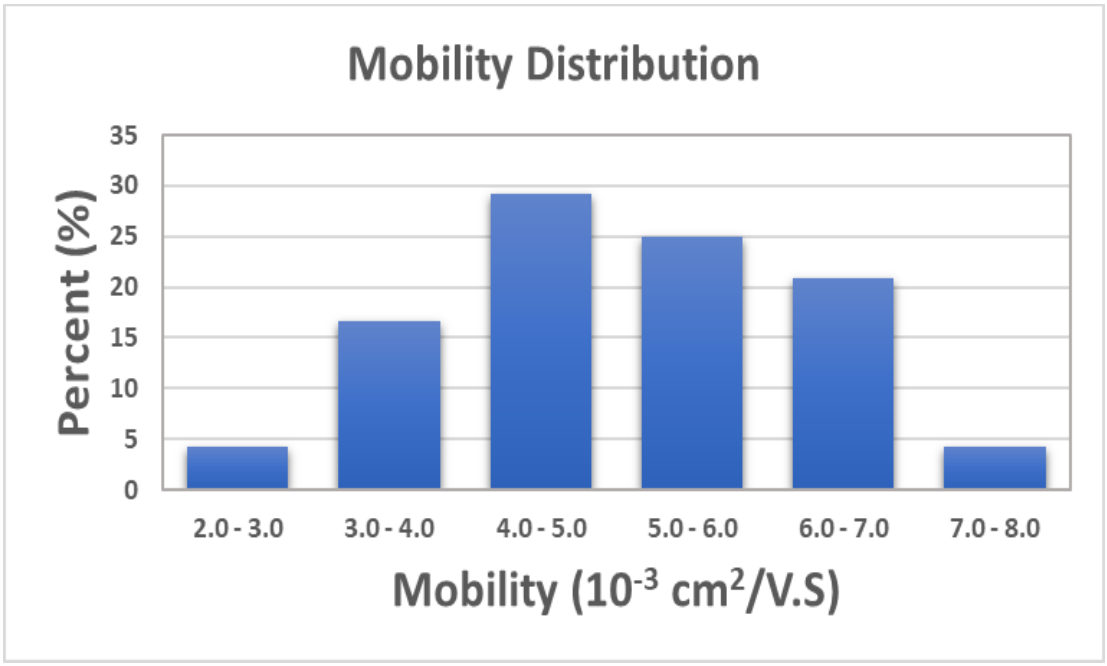

Figure 8.3. Mobility distribution of 24 P3HT based OTFTs.

In addition to the two examples above, we have compared the mobility of our devices with values reported for a number of P3HT based OTFTs that are both bottom gate bottom contact and bottom gate top contact. Characteristics of these devices are shown in Table 1, where the mobility of 12 devices have been summarized along with the specifications of the dielectric material, structure, and width to length ratio. The mobility values extracted from the devices reported in this chapter are higher than most of the values shown in Table 1, except for one device (top contact) that has a slightly higher mobility than the average value reported here; however, this published result has a different device design, specifically a Top Contact.

Table 8.1: Field-effect mobility values of P3HT based OTFTs reported in the literature

Organic Semiconductor Material	**Dielectric Material**	**Structure**	**Width/Length**	**Mobility** (cm^2/Vs)	**Reference**
Poly(3-hexylthiophene-2, 5-diyl) (P3HT)	SiO_2	BGBC	500 µm/50 µm	$\mu_{lin} = 5.5 \times 10^{-3}$	This work [8]
	SiO_2	BGBC	2000 µm/50 µm	$\mu_{lin} = 6.7 \times 10^{-5}$ $\mu_{sat} = 1.85 \times 10^{-4}$	9
	Poly(methylmethacrylate) (PMMA)	BGTC	100 µm/10,000 µm	$\mu_{sat} = 2.27 \times 10^{-3}$	10
	SiO_2	BGBC	1000 µm/ 30 µm	$\mu_{sat} = 3.2 \times 10^{-4}$	11
	SiO_2	BGBC	4000 µm/25 µm	$\mu_{sat} = 1.6 \times 10^{-4}$	12
	SiO_2	BGTC	1000 µm/50 µm	$\mu_{sat} = 7.7 \times 10^{-3}$	13
	SiO_2	BGBC	4000 µm/200 µm	$\mu_{sat} = 3.81 \times 10^{-4}$	14
	SiO_2	BGTC	4000 µm/200 µm	$\mu_{sat} = 5.05 \times 10^{-4}$	14
	SiO_2	BGBC	24,300 µm/65 µm	$\mu_{sat} = 1.15 \times 10^{-3}$	15
	SiO_2	BGBC	10,000 µm/ 10 µm	Spin coating $\mu_{sat} = 5 \times 10^{-4}$ Spray coating $\mu_{sat} = 4 \times 10^{-4}$	16
	SiO_2	BGBC	10,000 µm/ 20 µm	$\mu_{lin} = 1.1 \times 10^{-5}$ $\mu_{sat} = 2 \times 10^{-5}$	17
	HfO_X	BGBC	15,200 µm/20 µm	$\mu_{sat} = 1 \times 10^{-3}$	18

There are other P3HT based OTFTs with higher mobilities than the results reported in this chapter [19-22]. However, there are fundamental differences between these devices and the devices reported here. Specifically, the device structures were different (BGTC and TGBC), the solvent used to dissolve the P3HT in one of the devices was different (dichloromethane), and the interfaces in the device were engineered. Device structure affects the performance of the device, especially in injecting charge carriers from the electrode into the channel [23], and using a different solvent changes the orientation and crystallinity of the P3HT [19]. Furthermore, engineering the interfaces of the device affects the performance of the device: engineering the electrode/organic semiconductor and dielectric/organic semiconductor interfaces affect the charge carrier injection and transport in OTFTs, respectively [23]. Therefore, the difference in device structure, P3HT solvent, and interface engineering will most likely lead to the higher mobilities reported for the devices mentioned above. In the next three chapters, we also present our investigation on further enhancing the performance of the devices reported in this chapter by engineering the interfaces with different interfacial materials.

8.4 Conclusions

A photolithography fabrication process was used to fabricate P3HT based OTFTs with a BGBC structure. The fabricated devices were uniform in both electrical characteristics and geometry. The fabricated devices were characterized by performing I-V measurements. The threshold voltage and the field-effect mobility of the devices were extracted from the linear region of the device. The threshold voltage of one of the devices was determined to be 30.8 V and the mobility was determined to be $5.5 \times 10^{-3}\ {}^{cm^2}/_{Vs}$. The mobility was shown to be higher than most values reported in literature for other BGBC P3HT based OTFTs. The consistency and uniformity of the devices across the wafer was illustrated using mobility distribution of 24 devices. The high mobility and consistent characteristics of the devices across the wafer is primarily attributed to the developed fabrication process and careful annealing of the P3HT polymer.

8.5 References

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CHAPTER NINE

EFFECTS OF A VIRGIN GRAPHENE OXIDE INTERFACIAL LAYER ON THE PERFORMANCE OF ORGANIC THIN-FILM TRANSISTORS

9.1 Introduction

To further enhance the performance of the OTFTs reported in Chapter 8, we modified the interfaces of the OTFTs by inserting an interfacial material. One of the interfacial materials that was used to modify the interfaces was virgin ("as received") graphene oxide (GO). GO was used to modify both the electrode/organic semiconductor and the dielectric/organic semiconductor interfaces. This was possible due to the compatibility of GO with the gold electrode [1,2] and the P3HT [3]. In addition, GO has good wetting properties with polar and non-polar solvents [1]. GO is also compatible with our photolithographic fabrication process, and is relatively inexpensive and has low toxicity, which makes it attractive for mass production. It has also been demonstrated that using a covalently linked GO-Au electrode [1] and a highly reduced GO (RGO)-Au electrode [2] improve the charge injection process of OTFTs. Other scientific publications have also reported the employment of either chemically modified/anchored GO or reduced GO for the modification of OTFT interfaces [3-4]. However, to the best our knowledge, no one has ever used virgin GO for modifying the interfaces of P3HT based OTFTs with a BGBC structure. Therefore, in this chapter we investigate the effects of a virgin GO interfacial layer on the performance of P3HT based OTFTs.

To investigate the effects of a GO interfacial layer, we fabricated devices with and without a GO interfacial layer. The devices were then electrically characterized by

performing current-voltage measurements, using the same methods described in Chapter 8. The key materials that affect the operation of the OTFTs are analyzed using different material characterization techniques. Atomic force microscopy (AFM) was used to analyze the morphology of the GO and P3HT layers. Surface energy measurements were performed to study the spreading of P3HT on GO and SiO_2 surfaces and the interface interactions of P3HT/SiO_2 and P3HT/GO. Differential scanning calorimetry (DSC) was used to study the thermal behavior of GO, P3HT, P3HT/GO, P3HT/SiO_2, and P3HT/GO/SiO_2. The electrical characterization results showed that the drain current and the field-effect mobility of the OTFTs were significantly increased by the modification of the interfaces with the GO nanoscale layer. We attribute this enhanced performance to the resulting structure of the P3HT layer when deposited onto the GO surface and also to the reduced contact resistance between the GO-modified Au electrodes and the P3HT.

9.2 Fabrication of OTFTs with a GO Interfacial Layer

The fabrication of the OTFTs with a GO interfacial layer followed a nearly identical fabrication process as the devices without an interfacial layer, except for the addition of a GO layer underneath the P3HT. The fabrication process for the OTFTs without an interfacial layer was discussed in detail in Chapter 7, and these devices will hereinafter be referred to as standard OTFTs. The devices fabricated with a GO interfacial layer will be referred to as GO OTFTs. For the experiments reported in this chapter, the standard and GO OTFTs were fabricated simultaneously, on separate wafers, under similar environmental conditions. To fabricate the GO OTFTs, first, an aqueous dispersion of GO

was obtained from Goographene, Inc. It was received with a concentration of 5 mg/ml in water. According to the manufacturer, the dimensions of the GO sheets ranged from several hundred nanometers up to several micrometers in the XY plane and 0.7–1.2 nm in thickness. The GO suspension was first diluted to 0.25 mg/ml with DI water and then to 0.5 mg/ml until a desired thickness was achieved, which was between 1.3 nm and 1.6 nm.

Once the gate, drain and source contacts were deposited in the same way as the standard OTFTs, the GO solution was agitated in an ultrasonic bath for 4 minutes and immediately spin-coated onto the wafer. The spin coating was performed at an acceleration of 500 rpm/sec until a maximum speed of 1000 rpm was reached and maintained for 60 seconds, and subsequently baked at 110 ˚C for 40 minutes. The thickness of the GO was measured from an AFM image and determined to be 1.5 nm. The P3HT was then spin coated on top of the GO layer at an acceleration of 1000 rpm/sec until a maximum speed of 2000 rpm was reached and maintained for 60 seconds, and subsequently baked at 110 ˚C for 1 hour. Both the GO and the P3HT layers were then patterned together in the same way as the lone P3HT layer was for standard devices. The dimensions of the conductive channel were essentially identical to that the standard devices. More than 226 GO OTFTs were fabricated on a single wafer. The same number of standard OTFTs were also fabricated on another wafer. The schematic structure of the GO device is illustrated in Figure 9.1, and it is identical to the standard devices except for the GO interfacial layer. As illustrated in Figure 9.1, the P3HT/GO was not limited to the channel area only, but has a slight overlap onto the source/drain electrodes. As explained for the standard devices in Chapter 7, these devices were designed this way in order to increase the contact area

between the Au and P3HT/GO, which will increase the injection rate of charge carriers into the channel of the device [5].

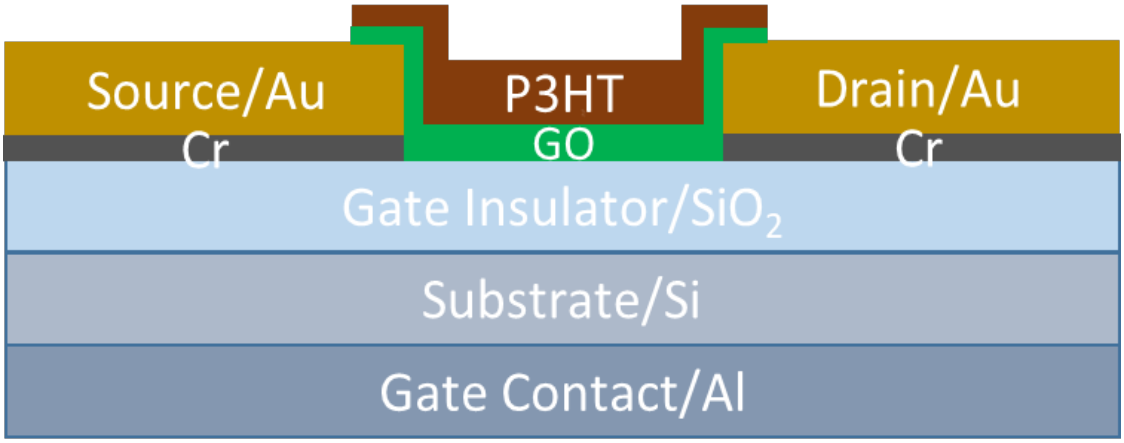

Figure 9.1: Schematic structure of P3HT based OTFT with a GO interfacial layer

9.3 Electrical and Material Characterization

Current-voltage (I-V) measurements were performed on both standard and GO OTFTs using an HP-4156B Semiconductor Parameter Analyzer. The drain current vs. drain voltage (I_{DS}-V_{DS}) measurements were performed by applying a drain voltage from 0 V to -70 V with an increment of -0.5 V while biasing the gate with voltages ranging from 0 V to -60 V with an increment of -20 V. The drain current vs. grate voltage (I_{DS}-V_{GS}) measurements were performed by applying a gate voltage from 20 V to -60 V while biasing the drain at -5 V.

Atomic force microscopy (AFM, Dimension 3100, Veeco Digital Instruments, Inc.) was used in tapping mode to investigate the morphology of the GO and P3HT layers. Contact angle measurements of the immersion liquids (hexadecane and water) were

performed using a KRUSS DSA 10 Drop Shape Analyzer at 20 seconds after droplet deposition on the SiO_2, GO and P3HT surfaces. Differential scanning calorimetry (DSC) (Model 2920; TA Instruments) was carried out at a heating/cooling rate of 20 ˚C/min and a temperature range of -100 ˚C to 150 ˚C. Model samples for DSC studies were prepared by addition of SiO_2, GO, or SiO_2-GO dispersion in chloroform to a P3HT-chloroform solution, sonication of the mixture for 1 hour at room temperature (RT), drying at RT, and annealing at 110 ˚C for 2 hours. The obtained materials had the following composition in terms of the weight ratios: P3HT:SiO_2/1:1, P3HT:GO/1:1, and P3HT:GO:SiO_2/1:1:1. To prepare the materials, SiO_2, GO, or SiO_2-GO dispersions in water were dried and redispersed in chloroform using an ultrasound bath. Sonication was conducted for 1 hour at room temperature. Silicon oxide powder, particle diameter 0.5 microns, was used from Alfa Aesar to prepare the materials.

9.4 Results and Discussion

Out of the 452 OTTFs (226 standard OTFTs + 226 GO OTFTs) that were fabricated, more than 48 devices (24 standard devices + 24 GO devices) were randomly selected to perform electrical measurements. In Figure 9.2, the output characteristics of a standard and a GO OTFT are shown, which are a representative of the majority of the devices measured. In this plot, the drain current is measured as a function of the drain voltage at various gate voltages. The broken lines in the figure are from a standard device and the solid lines are from a GO device. Clearly from Figure 9.2, the drain current for the GO device is higher than for the standard device at all drain voltages and gate voltages.

This shows that the channel for the GO device has a higher conductivity than the standard device.

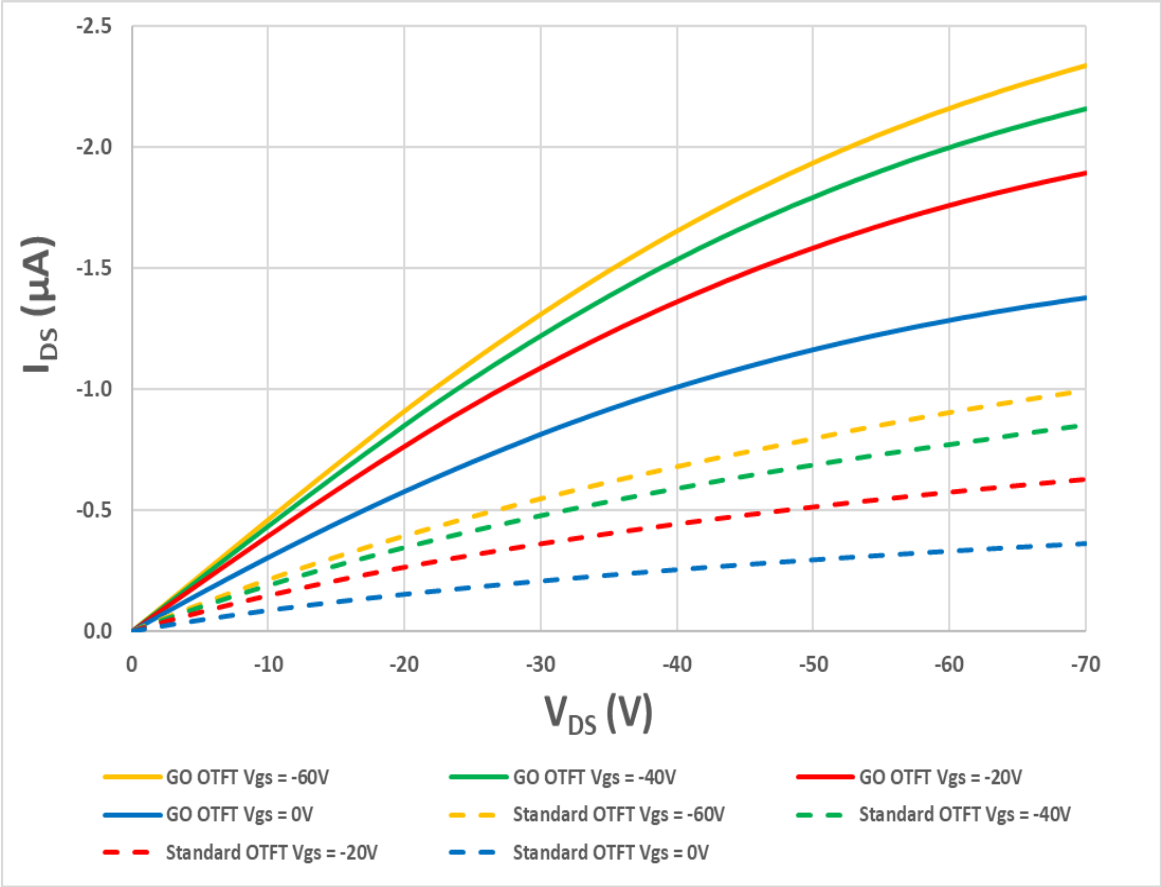

Figure 9.2: I_{DS} - V_{DS} output characteristics of a standard OTFT vs. a GO OTFT at different values of V_{GS}. The broken lines are for a standard OTFT, and the solid lines are for a GO OTFT.

The transfer characteristics of a standard and a GO OTFT, which were measured on the same devices as in Figure 9.2, are shown in Figure 9.3. The transfer curve (I_{DS}-V_{GS}) of a standard OTFT at V_{DS} = -5 V is shown with a broken blue line in the figure. The

extrapolation line for this curve is shown with a broken red line. The transfer characteristic of a GO OTFT at V_{DS} = -5 V is also shown in the figure. The transfer curve is shown with a solid blue line and its extrapolation line is shown with a solid red line. Using these plots in Figure 9.3, as well as the output plots in Figure 9.2, the threshold voltage and the field-effect mobility of both standard and GO OTFTs were extracted using the same methods as described in Chapter 8.

The threshold voltage was extracted using an extrapolation in the linear region method (ELR). Using this method, the threshold voltage for the standard OTFT was found to be 26.09 V, and for the GO OTFT it was found to be 47.24 V. The threshold voltage for the GO OTFT is significantly higher than the standard OTFT. This high threshold voltage for the GO OTFT is not optimal for low power device applications.

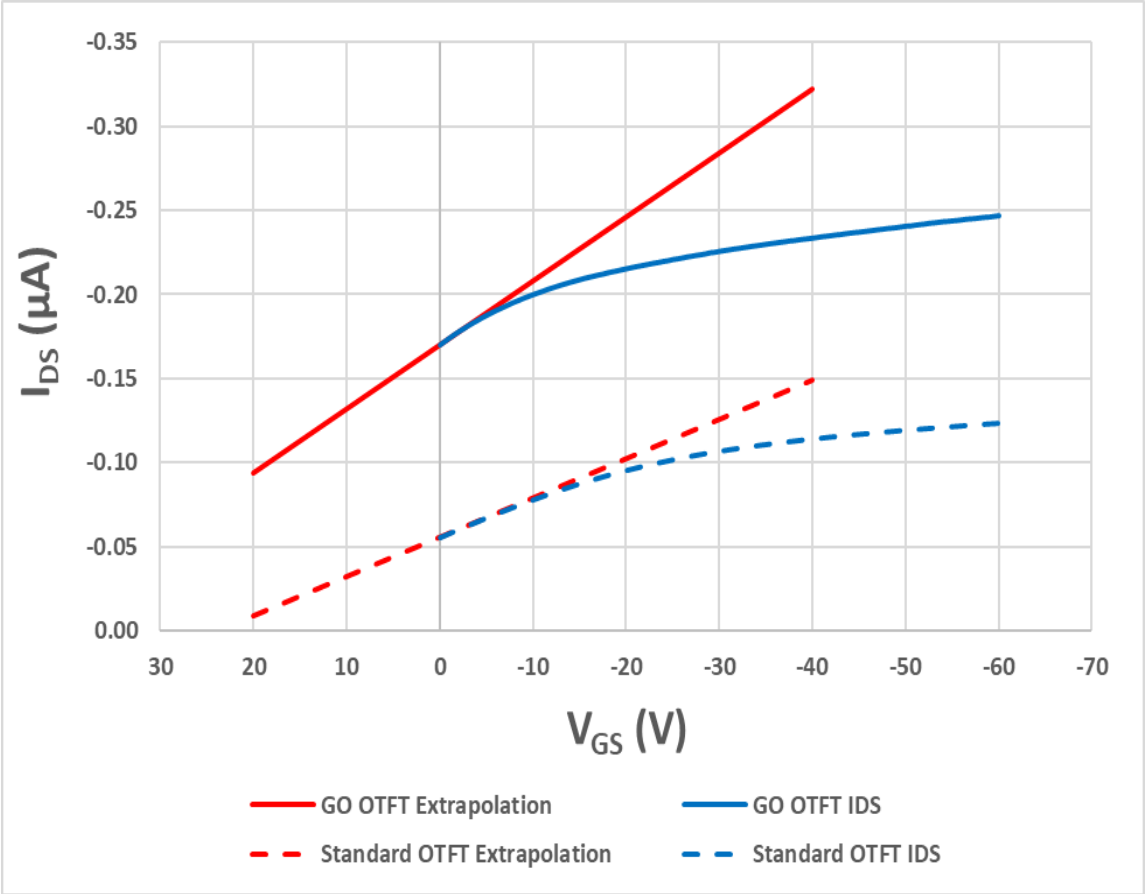

Figure 9.3: Transfer characteristics of a standard and a GO OTFT at V_{DS} = -5 V, along with the linear extrapolation of the curves at maximum transconductance. The broken lines are for a standard OTFT, and the solid lines are for a GO OTFT.

The field-effect mobilities of both standard and GO OTFTs were also extracted. The field-effect mobility was determined in the linear operation region using Equation 3.5, which is rewritten here for convenience.

$$\mu_{lin} = \frac{L}{WC_{OX}V_{DS}} g_m \tag{3.5}$$

The field-effect mobility in the linear region of the standard device was found to be $4.21 \times 10^{-3}\ {cm^2}/{Vs}$, and for the GO device it was found to be $7.3 \times 10^{-3}\ {cm^2}/{Vs}$. This result indicates that devices with a GO interfacial layer have higher mobility than devices with no interfacial layer. As demonstrated in chapter 8, the mobility result reported for the standard OTFTs was higher than most BGBC P3HT based devices reported in the literature [5]. Therefore, the mobility reported for the GO OTFT is even higher than most BGBC P3HT based OTFTs reported in the literature [6-9].

9.4.1 Impact of the GO Layer on the Dielectric Surface of the OTFTs

From Figure 9.2 and the above mobility results, it is clear that the devices with the GO interfacial layer have a higher drain current and mobility than the standard devices. One of the reasons for this is the morphological and structural changes of the P3HT when it is deposited on top of the GO nanoscale layer. A topographical and phase AFM image of a GO layer deposited onto a silicon wafer using a spin coating method is shown in Figure 9.4. From this AFM image, we can see that the GO coats the wafer quite uniformly, where most of the surface is covered with 1-2 nanosheets forming a continuous percolated layer. We note that a small fraction of the surface is not coated with GO. The topographical AFM image of GO is shown in Figure 9.4a. The quantitative AFM bearing analysis of the topographical image showed that about 80-90% of the wafer is covered with the nanosheets. We investigated the thickness of the single nanosheets from a cross-sectional analysis of the topographical image and found that their thickness is about 0.8-1.2 nm, close to the thickness provided by the manufacturer [10]. Root-mean-square roughness of

the GO layer was about 0.7 nm. The low value of the roughness confirms the uniform and even coverage of the substrate with the nanosheets. The phase AFM image of GO is shown in Figure 9.4b. The phase image, which is sensitive to surface heterogeneity [11], indicates that the GO nanosheets are uniform on the micron/submicron scale. The imaging data also shows the edges of the GO plates, which constitutes a minute fraction of the GO layer surface. It is well-known that the edges of the GO sheets have a different chemical composition than the basalt plane of the sheets [12]. In general, we can summarize that the overwhelming majority of the P3HT macromolecules deposited on the GO layer are in contact with the basalt plane of the nanosheets. Only a small fraction of P3HT chains contact the SiO_2 surface and the GO edges.

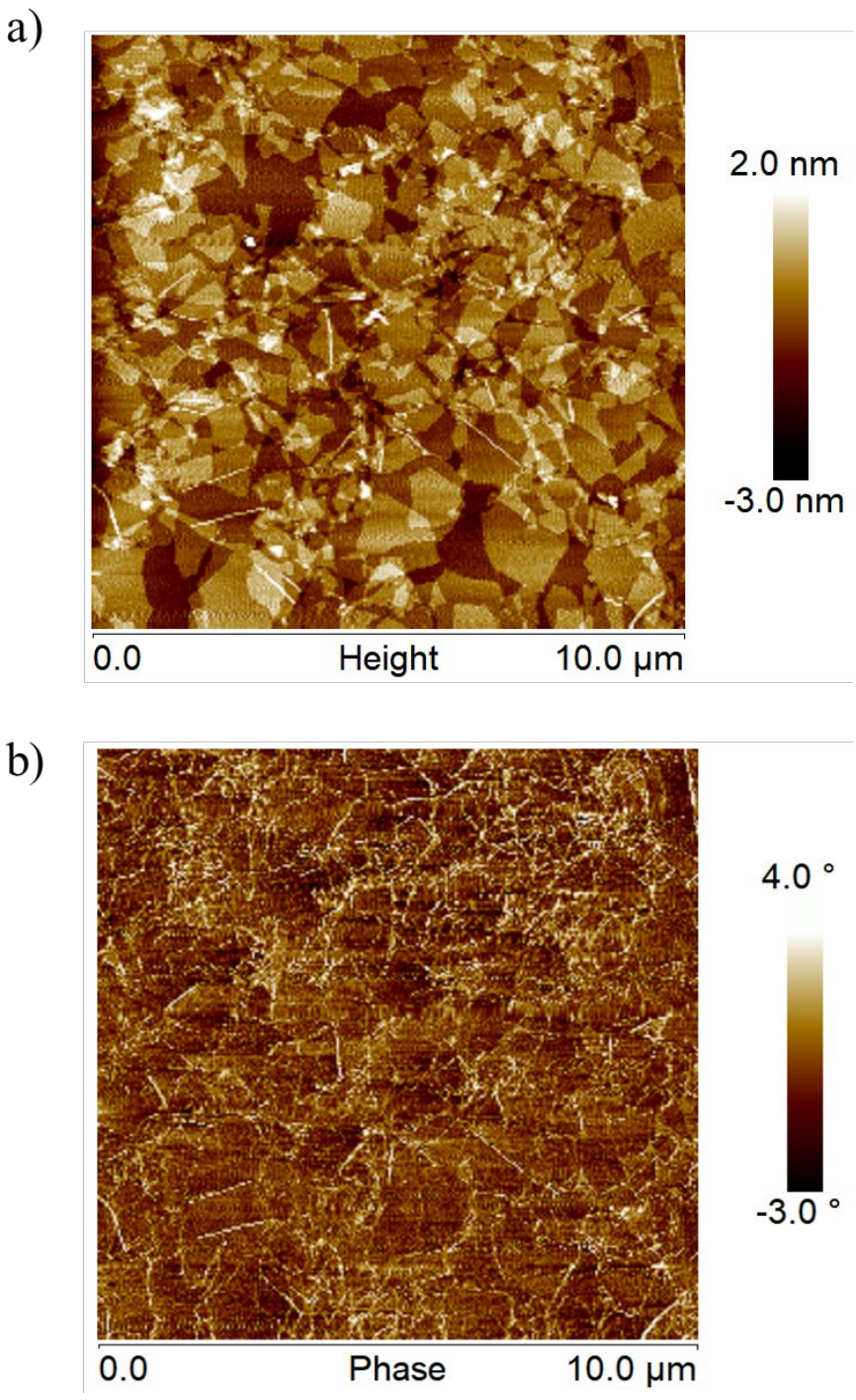

Figure 9.4: AFM topographical (a) and phase (b) images of a GO layer on a SiO_2 layer.

In Figure 9.5, AFM images of a sample of a P3HT layer deposited onto a pure SiO_2 surface compared to a sample of a P3HT layer deposited onto a GO layer, previously deposited onto SiO_2, are shown. The major purpose of the imaging was to examine the P3HT layer in terms of its submicron structure of grain formation and evenness of surface coverage. The grain size of P3HT on the SiO_2 surface, shown in Figure 9.5a, is clearly smaller than the grain size of P3HT on the GO surface shown in Figure 9.5c. It has been shown that the difference in grain size significantly impacts the movement of charge carriers in the channel of the transistors [13-15]. The small grain size of organic semiconductors leads to a high density of grain boundaries, which results in the formation of trap sites that hinder the movement of charge carries along the channel of the device. The total mobility of charge carriers in the channel can be divided into two components: mobility in the grain and mobility in the grain boundary [16]. These two mobility components are connected in series, and the resulting effective mobility can be written as [17]:

$$\frac{1}{\mu} = \frac{1}{\mu_g} + \frac{1}{\mu_b} \tag{9.1}$$

where μ_g and μ_b are the mobility in the grain and in the grain boundary, respectively. According to Equation 9.1, the mobility in the grain boundary limits the overall mobility of the organic semiconductor. Materials with a distribution of small grain sizes will have significantly more grain boundaries compared to materials containing larger grain sizes. Therefore, the effective mobility of transistors based on active polymers containing small grain sizes will be lower than those containing larger grain size polymers. So, the larger

grain size of the P3HT channel in the GO OTFTs can contribute to the higher field-effective mobility compared to the standard OTFTs.

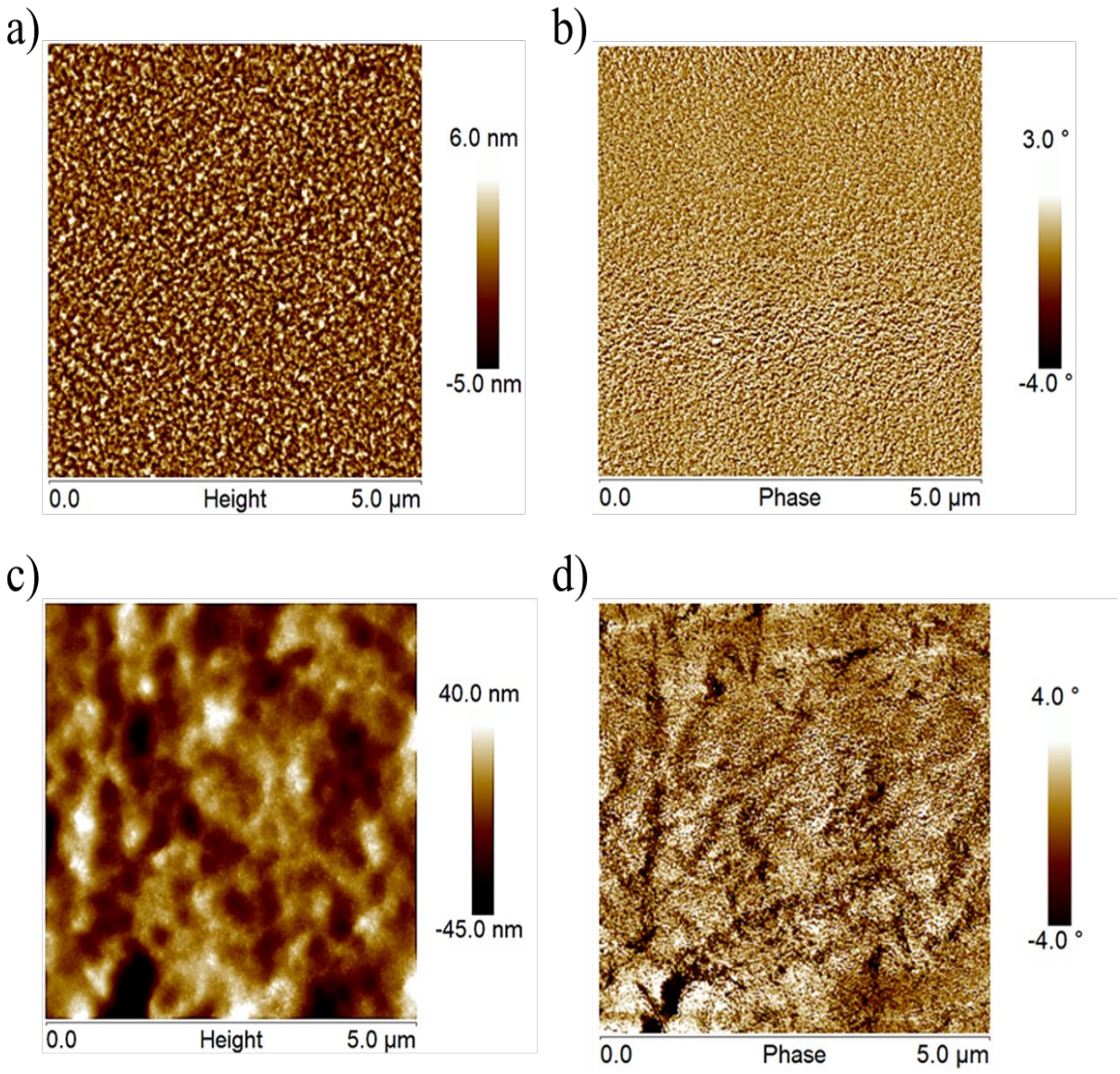

Figure 9.5: AFM topographical and phase images of P3HT on SiO_2 and GO surfaces, where the GO was deposited onto the SiO_2 layer. Topographic (a) and phase (b) images of P3HT on SiO_2 surface. Topographic (c) and phase (d) images of P3HT on GO surface.

It appears that the surface of the P3HT layer deposited onto the SiO_2 surface has a well-developed grainy structure, as shown in Figure 9.5a. A cross-sectional and particle analysis of the topographical image reveals that the grain size is on the level of 80-200 nm. RMS roughness of the layer is ~ 2 nm indicating that the apparent grain height is about 4 nm. Since the thickness of the layer is about 58 nm (which is smaller than the lateral grain size), we suggest that the grains are the major structural element of the P3HT layer in standard OTFTs. The phase AFM image of the P3HT layer deposited on SiO_2 is shown in Figure 9.5b. At first approximation, the phase image mostly follows topographical features on the surface. However, smaller-scale, "ripple-like" surface corrugations are also observed. The cross-sectional analysis of the phase images indicated that the lateral size of the corrugations is about 30-60 nm (as measured by AFM). We suggest that the corrugations reflect the packing of P3HT macromolecules on the surface into lamellar structures, as reported elsewhere [18-22].

The P3HT layer deposited onto the GO layer has entirely different structural features, as shown in the topographical AFM image in Figure 9.5c. Specifically, larger grains merging into continuous ribbon-like structures are observed. The grain size (and lateral size of the ribbon) is on the level of 300-600 nm, as determined from the cross-sectional analysis of the images. RMS roughness of the ribbon-like layer is ~12 nm indicating that the height of the surface structures is about 24 nm. As for the P3HT/GO phase image shown in Figure 9.5d, it mostly follows topographical features on the surface and, in addition, the "ripple-like" surface corrugations (lamellar structures with 40-60 nm lateral dimensions) are observed as well. We note that for the standard and GO OTFTs, the

height of the domains is significantly smaller than the thickness of the P3HT layer. Thus, the surface of the dielectric is covered with the polymer. So, we suggest that the larger grain size of the P3HT channel of the transistors containing the GO interfacial layer is one of the P3HT layer parameters that lead to higher effective mobility than that of the standard OTFT.

It was not obvious why there was so dramatic a difference in the morphology of P3HT layers deposited onto the SiO_2 and GO surfaces. One of the possibilities is that the initial stages of P3HT dewetting cause the formation of the grains from the dielectric substrates during the annealing procedure. Thus, the dielectric and P3HT surface energies can be significant factors that affect the morphology of the P3HT layer and, consequently, the device's performance. An important parameter in this regard is the spreading coefficient, which can be expressed as [23]

$$S_{1-2} = \gamma_1 - \gamma_2 - \gamma_{1-2} \tag{9.2}$$

where S_{1-2} is the spreading coefficient, γ_1 is the surface energy of a substrate, γ_2 is the surface energy of a polymer deposited on the surface, and $\gamma_{1\text{-}2}$ is the interfacial energy for the polymer-substrate contact. From thermodynamical considerations, $S_{1\text{-}2}$ must be positive for the spontaneous spreading of a polymer liquid over a substrate. If the spreading coefficient is negative, a polymer liquid will bead up (dewet) on the surface. To estimate $S_{1\text{-}2}$ we determined the surface energy of SiO_2, GO, and P3HT layers using the Owens-Wendt model. In the Owens-Wendt model [24, 25], the surface energy is divided into two components: a polar component and a dispersive component of non-polar interaction. Therefore, the surface energy is given by:

$$\gamma_S = \gamma_S^d + \gamma_S^P \tag{9.3}$$

where γ_S is the surface free energy of a solid, and γ_S^d and γ_S^P are the dispersive and polar components of the surface free energy of a solid, respectively. The dispersive and polar components of the surface free energy of a solid can be determined using the following equation [24, 25]:

$$\gamma_L(1 + cos\theta) = 2\sqrt{\gamma_S^d \gamma_L^d} + 2\sqrt{\gamma_S^P \gamma_L^P} \tag{9.4}$$

where γ_L is the surface free energy of an immersion liquid, γ_L^d and γ_L^P are the surface free energy of the dispersive and polar components of an immersion liquid, respectively, and θ is the contact angle of the immersion liquid on the solid surface. In Equation 9.4, since the values for γ_L^d, γ_L^P and γ_L (where $\gamma_L = \gamma_L^d + \gamma_L^P$) are known [26] and θ can be measured, we have only two unknowns, γ_S^d and γ_S^P; therefore, we need two contact angles from two different liquids to solve for the two unknowns. Equation 9.4 can be re-written for the two liquids as follows:

$$\gamma_{L1}(1 + cos\theta 1) = 2\sqrt{\gamma_S^d \gamma_{L1}^d} + 2\sqrt{\gamma_S^P \gamma_{L1}^P} \tag{9.5}$$

$$\gamma_{L2}(1 + cos\theta 2) = 2\sqrt{\gamma_S^d \gamma_{L2}^d} + 2\sqrt{\gamma_S^P \gamma_{L2}^P} \tag{9.6}$$

The two liquids that were used to measure the contact angles on the SiO_2, GO, and P3HT surfaces were hexadecane ($C_{16}H_{34}$) and water. Hexadecane was chosen for its non-polar nature, and water was chosen for its polar nature. The surface free energy of the dispersive and polar components of hexadecane and water are shown in Table 1.

Table 9.1: Surface free energy of the dispersive and polar components of hexadecane and water (taken from [26])

	Water	Hexadecane
γ_L^d (mN/m)	21.8	26.35
γ_L^P (mN/m)	51	0
γ_L (mN/m)	72.8	26.35

The contact angle measurement results of water on the SiO_2, GO, and P3HT surfaces were 28.2°, 0, and 96.1°, respectively. The contact angle measurement results of hexadecane on SiO_2 and GO surfaces were 0, and 16.9° on the P3HT surface. The dispersive and polar components of the surface free energy of SiO_2, GO, and P3HT were determined using Equations 9.5 and 9.6, and the results are shown in Table 2. The surface free energy (γ_S) of SiO_2, GO, and P3HT are determined using Equation 9.3, and the results are also shown in Table 2.

Table 9.2: Surface free energy of SiO_2, GO, and P3HT

	SiO_2	GO	P3HT
γ_S^d (mN/m)	26.35	26.4	25.3
γ_S^P (mN/m)	38.9	46.8	1.7
γ_S (mN/m)	65.25	73.2	27.0

The second parameter that we need to calculate in order to determine the spreading coefficient of P3HT is the interfacial energy (γ_{1-2}) of the polymer-substrate contact. The interfacial energy between two materials can be calculated using the following equation [27]**:**

$$\gamma_{1-2} = \gamma_1 + \gamma_2 - \frac{4\gamma_1^d\gamma_2^d}{\gamma_1^d+\gamma_2^d} - \frac{4\gamma_1^p\gamma_2^p}{\gamma_1^p+\gamma_2^p} \quad (9.7)$$

Using the surface energy values shown in Table 2, the interfacial energy of the P3HT/SiO_2 and P3HT/GO interfaces were determined using Equation 9.7, and the results are shown in Table 3.

Table 9.3: Interfacial energy of P3HT/SiO_2 and P3HT/GO

	P3HT/SiO_2	P3HT/GO
$\gamma_{1-2}(\mathrm{mN/m})$	34.12	41.96

Now that we have all the necessary values to calculate the spreading coefficients (S_{1-2}), S_{1-2} for P3HT on SiO_2 and GO surfaces is determined using Equation 9.2. The S_{1-2} for SiO_2 and GO surfaces are found to be 4.13 mN/m and 4.24 mN/m, respectively. The positive spreading coefficient values for SiO_2 and GO surfaces indicate that the P3HT has no tendency to dewet from either surface. The closeness of the values indicates that there is no significant P3HT spreading difference between the two surfaces.

Since there is no thermodynamic tendency for dewetting of P3HT from GO, we suppose the surface morphology of the GO layer is the decisive factor in the formation of

the P3HT layer with significant surface roughness. In fact, from careful observation of the phase image for the P3HT/GO layer (Figure 9.5d), one can see that the elevations on the surface originate from the "line-like" depressions. These features reflect the presence of the nanosheet edges on the GO layer. Therefore, we suggest that the origin of the relatively rough P3HT/GO layer is the surface topography. Namely, the edges of the GO nanosheets, to a certain extent, guide the spreading of the polymer solution during spin-coating. In fact, it is well established that topographical features on the surface, along with wettability, solution concentration, and spin speed/duration, affect the morphology of the spin-coated polymer films [28].

It is known that the interfacial interaction between a dielectric surface and P3HT can play an important role in the behavior of the organic semiconductor and, therefore, OTFT performance [29, 30]. In fact, carrier transport occurs in the conductive channel within a few molecular layers near the dielectric boundary [18, 19, 31-33]. However, it is necessary to point out that the interface interaction plays a significant role in OTFT fabrication even before the device is in use. Specifically, during the formation of the deposited P3HT layer, the attraction between the polymer and substrate influences the structurization of the layer during the annealing. In the layer deposited in the course of spin-coating, where solvent is rapidly evaporating, the polymer chains are not at an equilibrium state. The equilibration occurs during the thermal treatment of the layer above the polymer's glass transition temperature. The interaction between the polymer and substrate can significantly affect the equilibration process. Namely, as the interfacial interaction is high, chain rearrangement can be restricted by the surface/polymer affinity.

The level of P3HT/substrate thermodynamic interaction can be estimated via interfacial tension, where higher tension values can be related to the lower level of the attraction between substrate and polymer [23, 34]. The interfacial energies for P3HT/SiO_2 and P3HT/GO interfaces are shown in Table 3, which are 34.12 mN/m and 41.96 mN/m, respectively. The calculations indicate that P3HT has a higher affinity to the SiO_2 surface. Thus, it is the first indication that we can associate the smaller size of the grains for the P3HT/SiO_2 layer with difficulty forming the larger grains because of decreased diffusivity of the macromolecules physically connected to the substrate.

To put this argument in a molecular-level perspective, we estimated the size of the P3HT macromolecules (end-to-end distance, R) and compared the obtained value with the thickness of the polymer layer [35]:

$$R = \sqrt{C}_\infty \sqrt{n}\, l_0 \tag{9.8}$$

where C_∞ is the characteristic ratio (C_∞=12), n is the number of monomeric units in a P3HT chain (n =361 for our polymer having molecular weight of ~60,000 g/mol), and l_0 is length of one 3HT monomer (l_0 = 0.39 nm). We calculated R to be 26 nm. Thus, the P3HT layer used in the devices here (thickness ~58 nm) has dimensions on the level of 2 macromolecular layers. Thus, about half of the polymer chains constituting the layer are in physical contact with the substrate surface, and the movement of their segments is restricted [36, 37].

It is necessary to point out that P3HT/substrate interaction at the molecular level between SiO_2 and GO can be quite significant. It has been previously shown that Si-OH functionalities located on the SiO_2 surface can induce a certain P3HT chain orientation,

which tends to be perpendicular to the insulator substrate (edge-on structure) [18, 19, 32]. This orientation is caused by the repulsive forces between π-electron clouds of the thienyl backbone and unshared electron pairs of – OH functionality and are shown to have higher carrier mobility than face-on orientation, where thienyl rings are orienting parallel to the surface. On the other hand, the absorbed water molecules and irregularly located Si-OH groups on the SiO_2 surface can lead to interface trapping and hysteresis [38]. Conversely, GO nanosheets have a distinctive mosaic structure containing disordered oxygen-containing and ordered graphitic regions [12]. The oxygen-containing species are a mixture of hydroxyl, carbonyl, carboxyl, and epoxy functionalities. The typical content of graphitic sp^2 carbon regions is about 40%. The regions have a size of mainly 1–10 square nm [39, 40], which is much smaller than the size of a P3HT macromolecule with the end-to-end distance of ~26 nm and projection on the surface of about 530 nm^2. Therefore, each P3HT macromolecule is in contact with various surface functionalities and cannot adopt a certain preferred conformation and structurization as shown for the SiO_2 surface and thus can have (from a molecular level consideration) a higher level of diffusivity during the annealing.

To assess the difference in mobility of polymer chains in contact with SiO_2 and GO on a qualitative level, we prepared three model materials and investigated their thermal behavior with DSC between -100 ˚C and 150 ˚C. Indeed, it has been demonstrated elsewhere that the glass transition, T_g, of polymers, which is associated with the coordinated movement of the polymer chain segments, is significantly affected by the presence of a solid boundary [36, 37, 41, 42]. Specifically, when there is a certain level of attraction between polymer chains and the surface, T_g for the bonded chain segments is

higher than that for the macromolecules not located near the surface. The transition for the bonded chain segments often cannot be detected in an experiment because of the severe restriction in their mobility [37, 41].

The model materials were mixtures of SiO_2 submicron particles and GO nanosheets with P3HT as follows: P3HT/SiO_2 (1:1 weight ratio), P3HT/GO (1:1 weight ratio), and P3HT/GO/SiO_2 (1:1:1 weight ratio). The latter sample was prepared by premixing SiO_2 and GO in water, drying the mixture, and its redispersion in chloroform (not a good dispersive media for polar SiO_2 particles). Then the dispersion in chloroform was mixed with a P3HT solution and dried. Since the surface of GO nanosheets is orders of magnitude higher than that of the particles, we envisioned that the sample represents a situation where the SiO_2 surface is shielded with GO. The materials were annealed at 110 ˚C prior to the DSC measurements to replicate the thermal conditions used to prepare OTFTs. We added a large amount of SiO_2 and GO fillers to the polymer matrix to maximize the extent of contact between the macromolecules and the surface. For instance, straightforward geometrical calculations [43] using the size of SiO_2 particles (diameter 500 nm) and densities of P3HT (1.1 gram/cm^3) [44] and SiO_2 (2 gram/cm^3) [36] show that the distance between the particles in the P3HT/SiO_2 mixture is on the level of 100 nm. So about 40% - 60% of the polymer chains are in contact with the surface. It is close to the situation estimated for the P3HT layer in the standard OTFTs. Certainly, for GO, having a significantly higher surface-to-volume ratio, practically all polymer chains are in the vicinity of the nanosheets in our model materials. Thus, a large fraction of macromolecular segments physically contacts the GO surface.

The DSC data for the model materials, as well as for pure P3HT and GO nanosheets (annealed under the same conditions), is presented in Figure 9.6. We did not conduct measurements for pure SiO_2 particles since DSC data for them is available from the scientific literature [45]. First of all, we note that GO does not have any thermal transitions in the temperature region studied. For the pure P3HT, a typically found thermal behavior with a quite broad glass transition region is observed. The T_g reported in the scientific literature for P3HT varies from –113 ˚C to 106 ˚C depending on chemical structure, synthetic procedure, and sample preparation method [46-50]. For our pure P3HT sample, the glass transition occurs between -90 ˚C and -14 ˚C. Similar thermal behavior of the polymer in the Tg region is found for all model samples studied here. Therefore, the diffusion of a significant number of the macromolecular segments in the P3HT matrix is not restricted by the presence of the SiO_2 and GO solid boundary. When P3HT is mixed with SiO_2 particles, there is an additional broad and shallow endothermic peak at higher temperatures. It was reported elsewhere that SiO_2 particles between 40 ˚C and 180 ˚C can demonstrate an endothermic peak originating from the volatilization of water on the surface of particles [45]. Similar behavior is seen in our DSC scan for the P3HT/SiO_2 mixture. For the P3HT/GO samples, we note an additional T_g-like second order transition at about 120 ˚C. The transition is not present in pure P3HT and P3HT/SiO_2 samples. We associate this transition with the onset of movement of macromolecule segments that are in contact with the GO surface. The same transition was found for the P3HT/GO/SiO_2 mixture. This transition is even more pronounced for this mixture since the concentration of P3HT is lower in this case, and more chain segments are in contact with the GO surface. Based on

the DSC measurements we can qualitatively conclude that P3HT chain segments are more mobile when in contact with GO than when they are in contact with SiO_2. As mentioned above, we associate this increased mobility with formation of larger P3HT grains in GO OTFTs and therefore, better electrical performance of GO OTFTs.

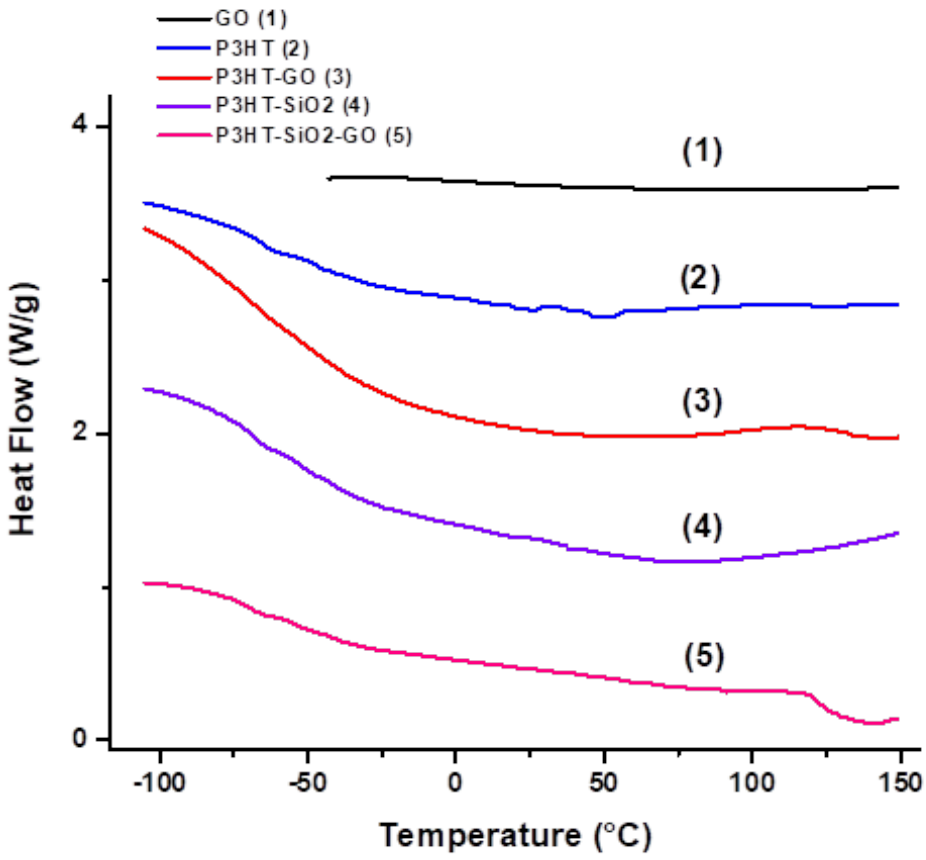

Figure 9.6: DSC curves for the model materials.

9.4.2 Impact of the GO Layer on the Electrode Surface of the OTFTs

The GO interfacial layer did not only modify the dielectric surface, but also the electrode surfaces. The discussions up to now are focused on the modification of the dielectric surface; however, the modified source-drain electrodes also affect the operation of the transistors. There must be a good compatibility between the electrodes and the organic semiconductor interface in OTFTs; otherwise, the contact resistance at the interface and the molecular ordering of the organic semiconductor will reduce the injection efficiency of charge carriers into the organic semiconductor. It has been shown that Au is more compatible with GO than both p-type and n-type organic semiconductors [1]. An organic semiconductor deposited onto a GO-modified Au electrode will have less contact resistance and better molecular ordering than on a pristine Au electrode [1]. Therefore, the devices with the GO interfacial layer will have a higher injection rate of charges into the organic semiconductor because of the compatibility of GO with the Au source and drain electrodes, which ultimately contributes to the enhanced drain current and field-effect mobility.

One final possibility that could contribute to the higher drain current of the GO OTFTs is the electrical conductivity of the GO layer. GO is typically considered an electrical insulator, but its conductivity depends on the degree of reduction [12, 51, 52]. For example, reducing GO using thermal, chemical, electrochemical, or photochemical processes results in reduced GO (RGO), which is far more conductive than GO [12, 51-53]. In this work, we used virgin GO "as-received" from the supplier without any reduction or chemical modification. However, to verify that the GO used here had no significant

conductance and working in parallel with the P3HT, we performed an experiment by fabricating devices with GO as the only active layer, without any P3HT. The schematic structure of this device is illustrated in Figure 9.7. The thickness of the GO deposited was the same as that used to form an interfacial layer in the GO devices. I-V measurements were performed on these transistors and no significant drain current was observed. Therefore, the enhanced drain current and field-effect mobility for the devices with the GO interfacial layer was not due to GO conductivity. This gives further evidence that the observed enhanced transport properties are due to the morphology changes to the P3HT in the channel and the compatibility of GO with the Au electrodes.

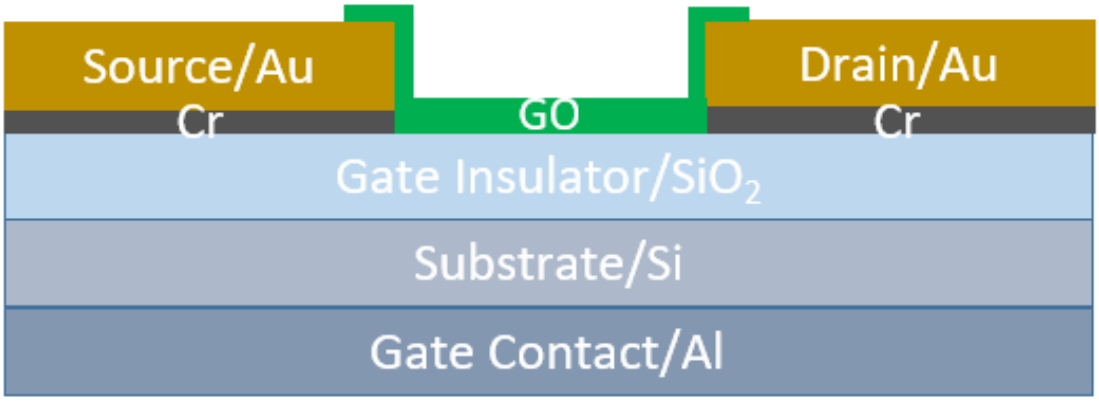

Figure 9.7: Schematic structure of OTFT with GO as the active layer

9.5 Conclusions

A P3HT based OTFTs with a virgin GO interfacial layer were investigated. GO was used to modify both the electrode/organic semiconductor and the dielectric/organic semiconductor interfaces. The I-V measurements showed that the GO OTFTs have a higher drain current and field-effect mobility than the standard OTFTs. The increased drain current and mobility of the GO devices is explained by the particular structure of the P3HT layer on the dielectric surface [54]. The P3HT layer deposited on the GO surface has larger interconnecting polymer grains compared to the P3HT deposited on the SiO_2 surface. From a thermodynamic and molecular standpoint, it is suggested that this specific morphology is formed owing to increased mobility of the macromolecular segments in the vicinity of the solid boundary. This increased segment mobility was confirmed via DSC measurements. Furthermore, we attributed the enhanced performance of the GO OTFTs with the decrease in the contact resistance of the GO-modified Au electrodes and P3HT. These results have been published in [54].

9.6 References

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CHAPTER TEN

EFFECTS OF A COPOLYMER INTERFACIAL LAYER ON THE PERFORMANCE OF ORGANIC THIN-FILM TRANSISTORS

10.1 Introduction

The second interfacial material that was investigated to enhance the performance of the OTFTs was a copolymer. The copolymer material used for this purpose was Poly(oligo (ethylene glycol) methyl ether methacrylate- glycidyl methacrylate- lauryl methacrylate), or P(OEGMA-GMA-LMA). The P(OEGMA-GMA-LMA) was used to modify both the electrode and the dielectric surfaces of the device. P(OEGMA-GMA-LMA) was synthesized in the laboratory through a radical polymerization method in a solution environment [1]. It is a cross-linkable amphiphilic copolymer that can form a covalent bonding with surfaces. As reported earlier in Chapter 5, it is prepared from three monomers: oligo (ethylene glycol) methyl ether methacrylate (OEGMA), glycidyl methacrylate (GMA), and lauryl methacrylate (LMA). To the best of our knowledge, P(OEGMA-GMA-LMA) has never been used before to modify the interfaces of organic transistors. Therefore, in this chapter we investigate the effects of a P(OEGMA-GMA-LMA) interfacial layer on the performance of P3HT based OTFTs.

Hereinafter P(OEGMA-GMA-LMA) is referred to as POGL. To investigate the effects of a POGL interfacial layer on the operation of OTFTs, we fabricated OTFTs with and without a POGL interfacial layer. The OTFTs with a POGL interfacial layer are referred to as POGL OTFTs, and the OTFTs without a POGL layer are referred to as standard OTFTs. The key interfaces and materials that affects the operation of the OTFTs

were analyzed using various material characterization methods. Atomic force microscopy (AFM) was used to examine the morphological structure of the POGL and P3HT layers. Surface energy measurements were performed to study the spreading coefficient of P3HT on a POGL surface and the interface interaction of P3HT/POGL. Current-voltage (I-V) measurements are performed to characterize the primary electronic properties of the transistors. The results from the I-V measurements showed that the OTFTs with the POGL interfacial layer have a lower threshold voltage than the standard devices, while maintaining a relatively high field-effect mobility. In addition, the POGL OTFTs showed much more ideal drain current saturation characteristics than the standard devices. We associate this enhanced performance of the POGL OTFTs with the deep trap states on the POGL surface and the reduction of the contact resistance at the electrode/organic semiconductor interface.

10.2 Fabrication of OTFTs with a POGL Interfacial Layer

The fabrication of the POGL OTFTs followed a nearly identical fabrication process as the standard OTFTs (which was reported in Chapter 7), except for the addition of a POGL layer underneath the P3HT. The fabrication of both standard and POGL devices occurred at the same time, on separate wafers, under similar environmental conditions. To fabricate the POGL OTFTs, the POGL solution was synthesized by the solution free-radical polymerization method [1]. The synthesis was performed by Mastooreh Seyedi in Dr. Igor Luzinov's laboratory. The materials used to synthesize the POGL are: 2-butanone (MEK), Glycidyl methacrylate (GMA, 97%,), oligo (ethylene glycol) methyl ether

methacrylate (OEGMA, average M_n 950), lauryl methacrylate (LMA), azoisobutyronitrile (AIBN) initiator, and inhibitor removers (replacement packing for removing hydroquinone and monomethyl ether hydroquinone (MEHQ), and replacement packing for removing tert-butylcatechol). The 2-butanone (MEK) was purchased from VWR International, LLC, and the rest of the materials were purchased from Sigma-Aldrich, Inc.

The molar ratio of the feed OEGMA:GMA:LMA monomers was 60:20:20. Each of the monomers were first mixed with the inhibitor removers for 30 minutes. Then, 0.2463 gram of AIBN, 88 ml of OEGMA, 1 ml of GMA, and 2.2 ml of LMA were added to 58.8 ml MEK in a 250 ml flask and stirred for 45 minutes at room temperature. The solution was kept under nitrogen purge for the entire time to remove oxygen from the solution. The flask was then transferred to a water bath with a temperature of 50℃ and stirred for another 90 minutes. The resulting polymer was purified by precipitating in diethyl ether and dissolving in MEK to remove unreacted monomers and the initiator. This purification process was repeated three times.

Once the gate, drain, and source contacts were deposited in the same way as the standard OTFTs, the copolymer was ready to be deposited. The POGL solution was agitated in an ultrasonic bath for 4 minutes and immediately spin coated onto the wafer at an acceleration of 1000 rpm/sec until a maximum speed of 2000 rpm was reached and maintained for 60 seconds, and subsequently baked at 110 ˚C for 40 minutes. The P3HT was then spin coated on top of the POGL layer and baked afterward using the same spinning and baking recipe as for the standard OTFTs, which was described in Chapter 7. The POGL and P3HT layers were then patterned together in the same way as the standard

OTFTs. More than 226 POGL OTFTs were fabricated on a single wafer. The same number of standard OTFTs were also fabricated on another wafer. The schematic structure of the POGL device is illustrated in Figure 10.1. It is essentially identical to the standard device apart from the POGL interfacial layer. The dimensions of the conductive channel were also similar to the standard devices in Chapter 7; the channel length was 50 μm and the channel width was 500 μm.

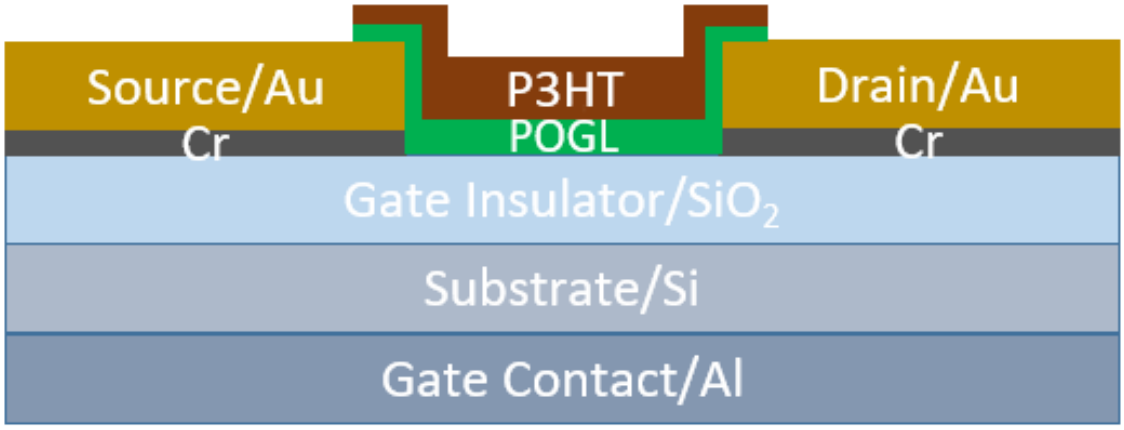

Figure 10.1: Schematic structure of POGL OTFT

10.3 Electrical and Material Characterization

Current-voltage (I-V) measurements were performed using a Semiconductor Parameter Analyzer (HP-4156B). The drain current vs. drain voltage (I_{DS}-V_{DS}) measurements, output characteristics, were performed by applying a drain voltage from 0 V to -70 V with an increment of -0.5 V while biasing the gate with voltages ranging from 0 V to -60 V with an increment of -20 V. The drain current vs. grate voltage (I_{DS}-V_{GS}) measurements, transfer characteristics, were performed by applying a gate voltage from 20

V to -60 V while biasing the drain electrode at -5 V. Atomic force microscopy (AFM, Dimension 3100, Veeco Digital Instruments, Inc.) was used in tapping mode to investigate the morphology of the POGL and P3HT layers. Contact angle measurements of the immersion liquids (hexadecane and water) were performed using a KRUSS DSA 10 Drop Shape Analyzer at 20 seconds after droplet deposition on the POGL surface.

10.4 Results and Discussion

The electrical measurements were performed on about 50 OTFTs; 25 standard OTFTs and 25 POGL OTFTs. In Figure 10.2, we show the output characteristics of one of the standard OTFTs, which is a representative of the majority of the devices measured. In Figure 10.3, we show the output characteristics of one of the POGL OTFTs, which is representative of the majority of these devices. In both figures, the drain current is plotted as a function of the drain voltage at various gate voltages. Comparing the I-V characteristics of both devices in Figures 10.2 and 10.3, we see that the POGL OTFT displays much more ideal drain current saturation characteristics, with a much smaller I-V curve slope in the saturation region. The drain current for the POGL OTFT saturates at a lower drain voltage than that of the standard OTFT. Furthermore, the drain current magnitude for the POGL OTFT is lower than for the standard OTFT at all gate and drain voltages. So, it appears that adding the POGL interfacial layer has a significant effect on the device characteristics.

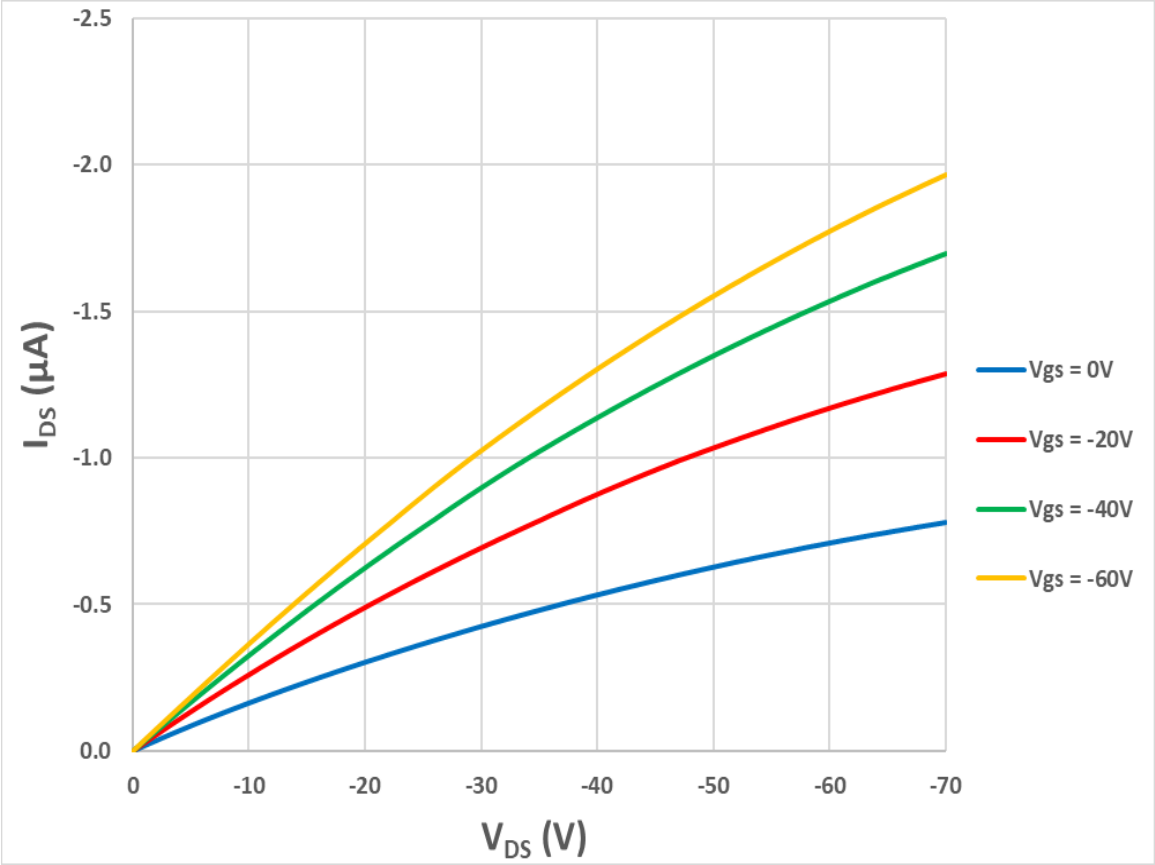

Figure 10.2: I_{DS} - V_{DS} output characteristics of a standard OTFT at different values of V_{GS}.

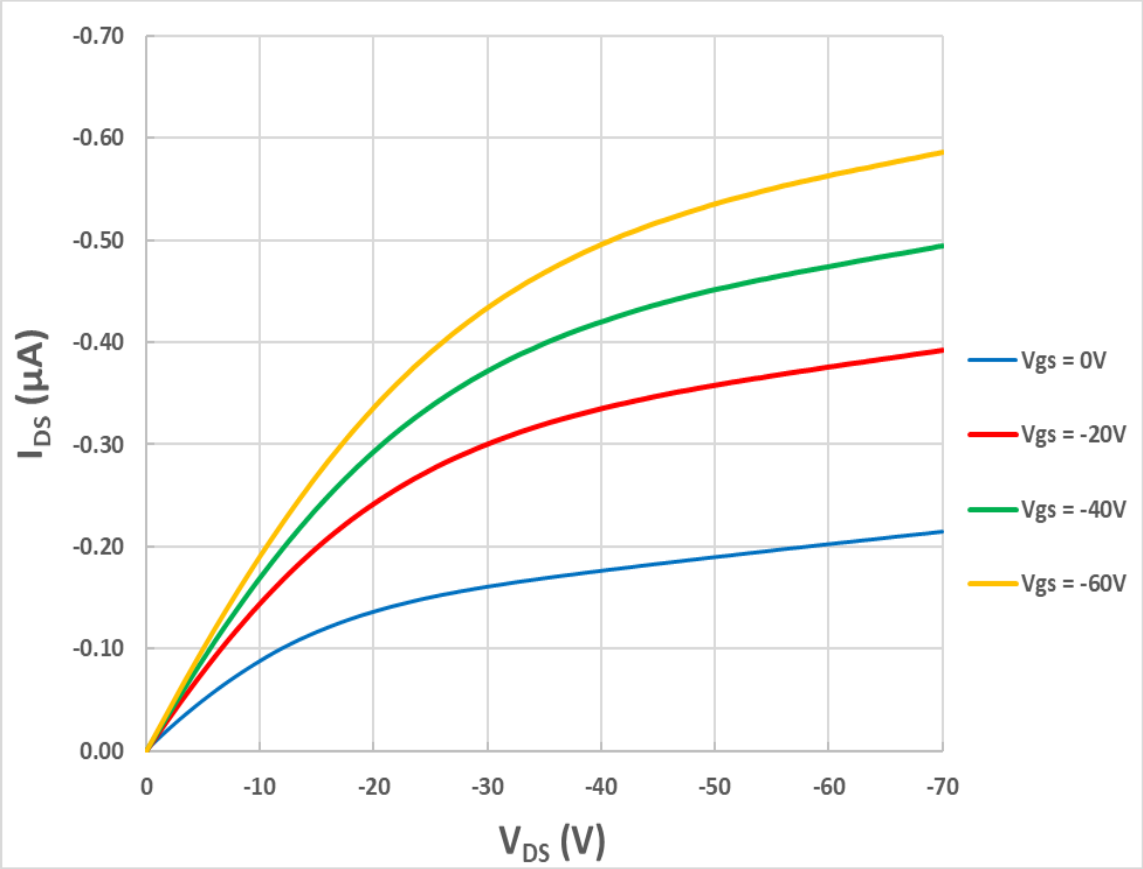

Figure 10.3: I_{DS} - V_{DS} output characteristics of a POGL OTFT at different values of V_{GS}.

In Figure 10.4, we show the transfer characteristics of a standard and a POGL OTFT, measured on the same devices as in Figure 10.2 and 10.3, respectively. These transfer curves were used to extract the threshold voltage and field-effect mobility of both standard and POGL OTFTs. The I_{DS}-V_{GS} curve of the standard OTFT at V_{DS} = -5 V is shown with a broken blue line in Figure 10.4, and its extrapolation line is shown with a broken red line. The I_{DS}-V_{GS} curve of the POGL OTFT at V_{DS} = -5 V is also shown in the figure with a solid blue line. The extrapolation line for this curve is shown with a solid red line.

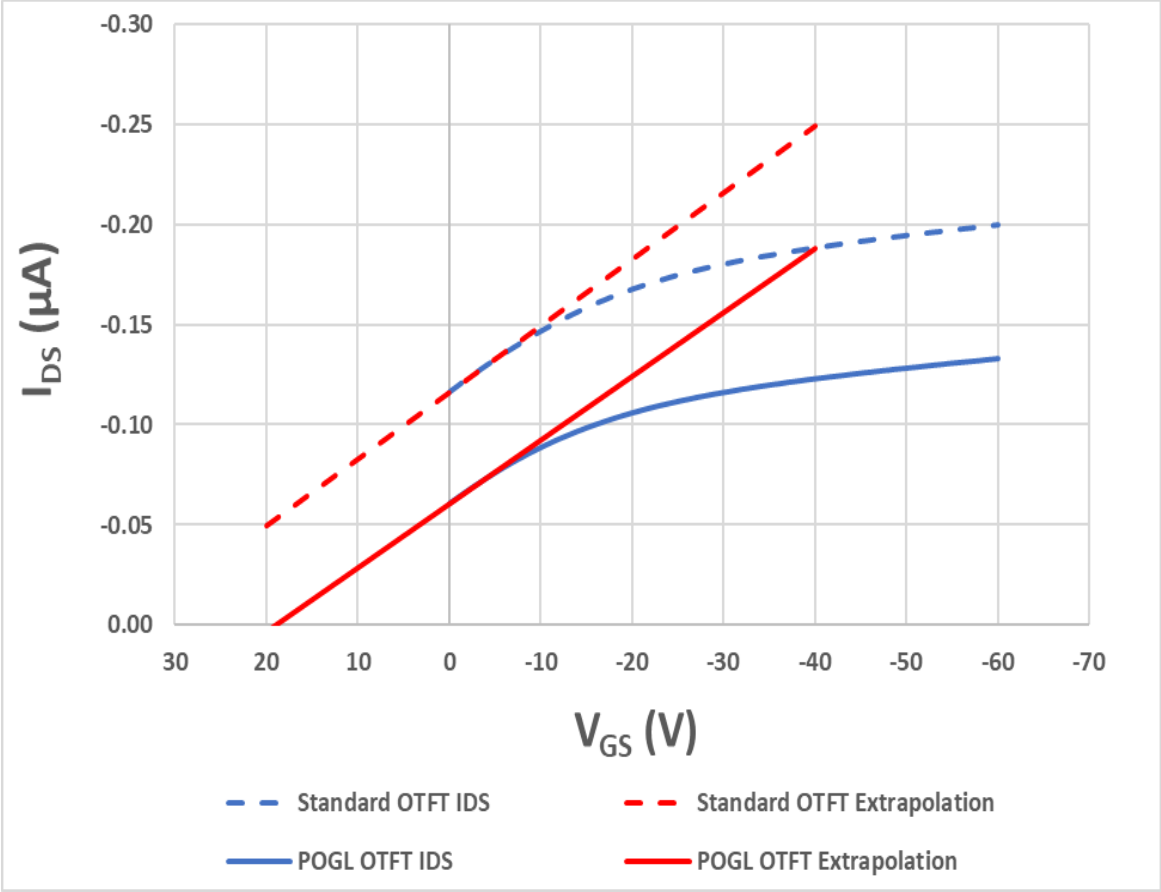

Figure 10.4: Transfer characteristics of a standard and a POGL OTFT at V_{DS} = -5 V, along with the linear extrapolation of the curves at maximum transconductance. The broken lines are for a standard OTFT, and the solid lines are for a POGL OTFT.

The threshold voltage for both devices was determined using an extrapolation in the linear region method (ELR). Using this method, the threshold voltage for the standard and POGL OTFTs were determined to be 37.33 V and 21.52 V, respectively. From these results, it is clear that the threshold voltage for the POGL OTFT is significantly smaller than that for the standard OTFT. It is preferable for OTFTs to have a relatively low

threshold voltage as this results in lower power consumption. This makes the POGL OTFTs potentially attractive for low power applications.

The field-effect mobilities in the linear region of both standard and POGL OTFTs were also determined. The field-effect mobility for the standard and POGL OTFTs was determined to be $6.02 \times 10^{-3}\, cm^2/_{Vs}$ and $5.74 \times 10^{-3}\, cm^2/_{Vs}$, respectively. The mobility for the POGL OTFT is slightly smaller than for the standard OTFT; however, this reduction in mobility is well within the mobility distribution of the standard OTFTs shown in Figure 8.3 of Chapter 8. Furthermore, both of these mobility values are higher than most P3HT based OTFTs reported in the scientific literature with bottom gate bottom contact structures [2].

10.4.1 Impact of the POGL Layer on the Threshold Voltage of the OTFTs

The lower threshold voltage of the POGL OTFT is related to its I-V characteristics, which are closer to the ideal case. Comparing the I-V curves in Figure 10.2 and 10.3, we can see that the drain current for the POGL OTFT saturates much better with a lower slope than for the standard OTFT. To investigate this behavior, we need to first consider how drain current saturates in an OTFT. When $V_{DS} << V_{GS} - V_{TH}$, a uniform charge carrier concentration exists across the channel of a transistor, and I_{DS} increases linearly with V_{DS}. This region in the drain current characteristics is known as the linear region, and its charge carrier concentration profile is illustrated in Figure 10.5(a). As V_{DS} increases, the charge carrier concentration in the channel changes from a uniform to a non-uniform profile. In Figure 10.5(b), a non-uniform concentration profile is illustrated for the special case of

$V_{DS} = V_{GS} - V_{TH}$. At $V_{DS} = V_{GS} - V_{TH}$, the channel region of the OTFT that is nearest to the drain becomes "pinched-off" and marks for the onset of saturation. As V_{DS} continues to increase ($V_{DS} > V_{GS} - V_{TH}$), the pinch-off point moves further towards the source electrode, and the drain current, to first order, should remain constant at its saturation value. This region in the I-V curve is known as the saturation region, and its charge carrier profile is illustrated in Figure 10.5(c), where the device is well beyond saturation. Essentially, the externally applied gate voltage, V_G, is equal to the sum of the gate-to-channel potential V_{G-ch}, which charges the channel at some particular point in the channel, and the local channel potential, which is the voltage between that particular point in the channel and a reference point which we will assume is ground. If we consider the channel point at the drain, then V_{G-ch} becomes V_{G-D}. In saturation, when $V_{DS} > V_{GS} - V_{TH}$, then V_{G-D} is below threshold and the channel region becomes depleted near the drain, so the charge in the channel does not extend all the way to the drain (pinched off). The ever-growing electric field in the channel depletion region sweeps the charge carriers across the depleted region, from the pinch-off point to the drain electrode [3].

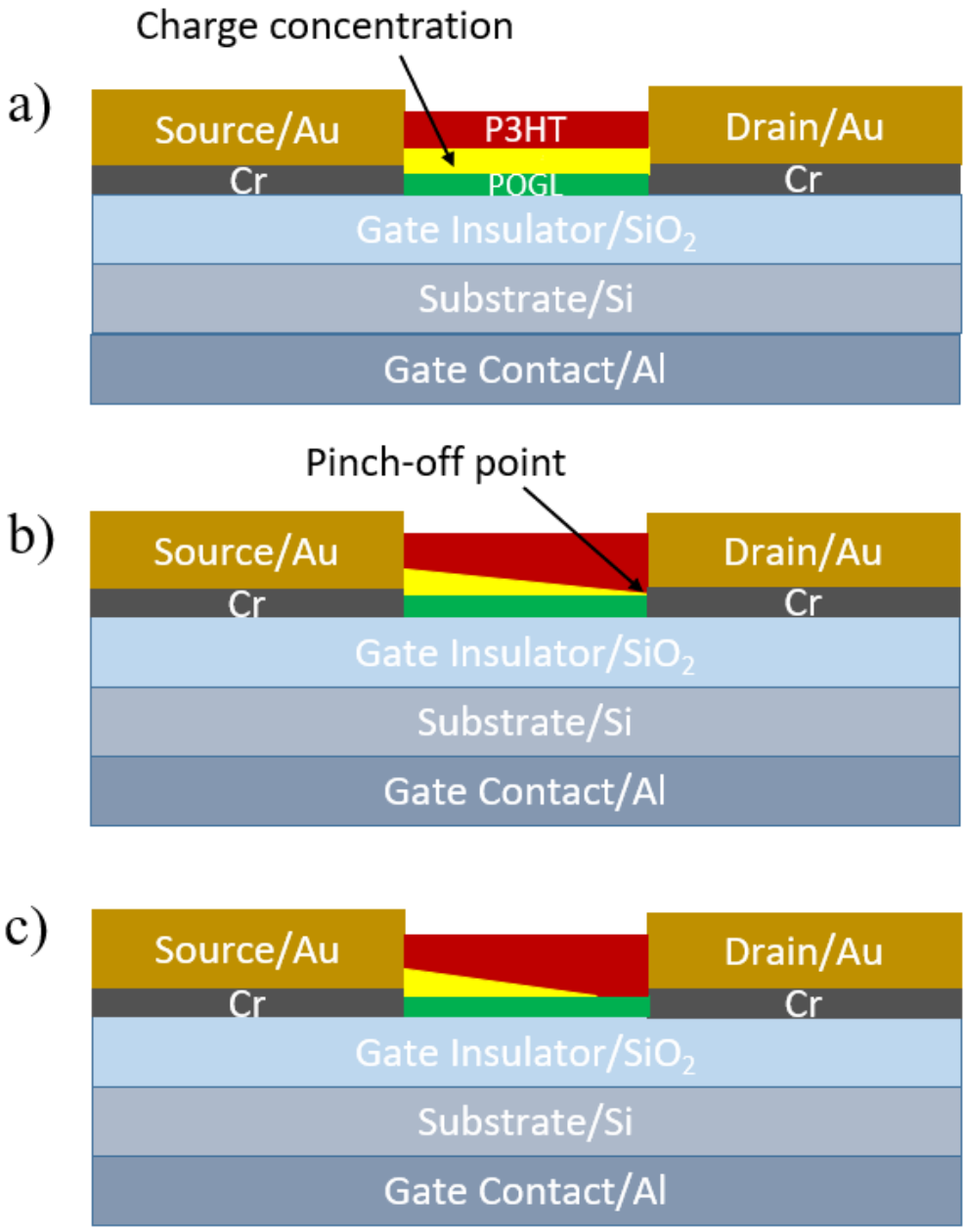

Figure 10.5: Charge carrier concentration profile of an OTFT for different operation regions: a) linear region, b) when $V_{DS} \cong V_{GS} - V_{TH}$, c) saturation region

The drain current in most OTFTs, however, appears to increase in the saturation region [4, 5, 6], as also observed in our standard OTFTs. Two of the main reasons for the finite slope of the $I_{DS} – V_{DS}$ curve past the onset of saturation are the shallow trap states on the surface of the dielectric and the contact resistance between the source-drain electrodes and the organic semiconductor. In OTFTs, there are shallow and deep level trap states that immobilize some charge carriers for as long as the measurement time [3, 7]. As V_{GS} increases, at some point most of the shallow trap states become full and no longer trap other charge carriers, resulting in a continuously increasing drain current with a finite $I_{DS} – V_{DS}$ curve slope. The mobility in the saturation region also increases with the gate voltage since the traps are filled and unavailable to trap subsequent charge carriers [3]. The POGL OTFTs, however, were observed to have much more ideal drain current saturation characteristics with relatively small $I_{DS}–V_{DS}$ curve slope (Figure 10.3). This can be explained by the deep trap states on the POGL surface of the POGL OTFTs. An AFM image of a POGL layer deposited onto a blank silicon wafer is shown in Figure 10.6. From this figure, we can see that the POGL surface is not a smooth surface. According to this AFM image, the RMS surface roughness is 1.33 nm. There are many bright spots on the AFM image, which indicate a variation in the thickness of the POGL. These bright spots are the POGL aggregates. The thickness of most of the large aggregates ranges from 4.8 nm to 9.4 nm. These aggregates can form deep trap states and trap most of the free charge carriers that were not trapped by the shallow traps [8]. This results in a drain current that saturates very well and also begins to saturate at a lower drain voltage (V_{DSsat}). Thus, the improved drain current saturation characteristics and the significant threshold voltage

reduction of the POGL OTFTs can primarily be attributed to the deep trap states on the POGL surface.

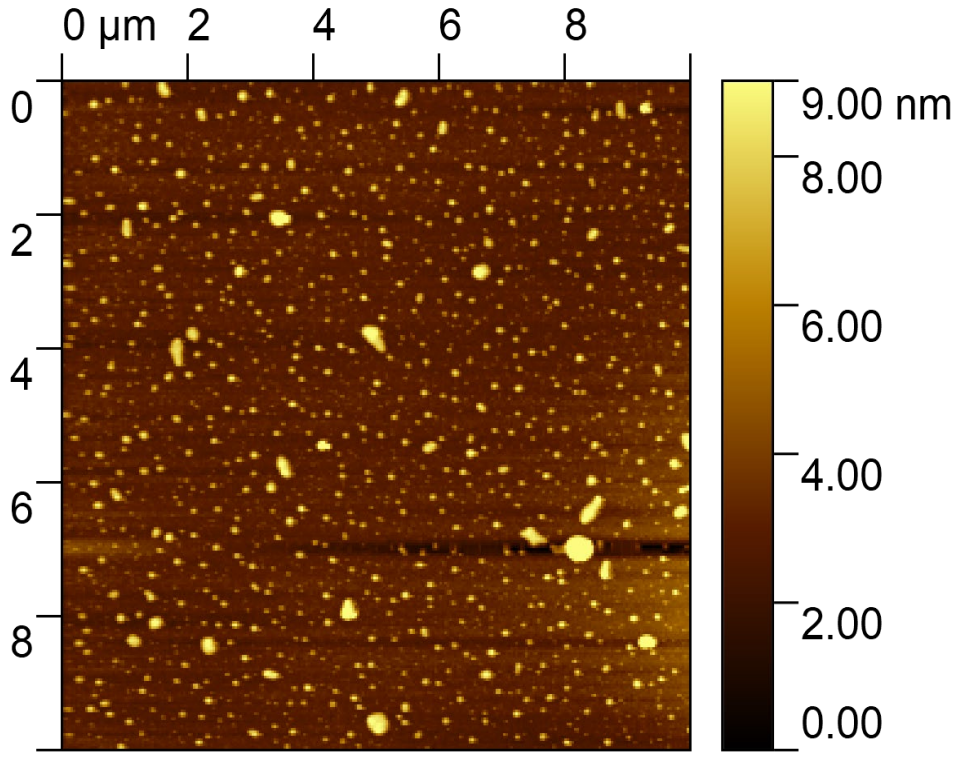

Figure 10.6: AFM image of POGL on a silicon wafer

In addition to the deep trap states, contact resistance between the electrode and the organic semiconductor also affects the drain current saturation characteristics as well as the threshold voltage of the OTFTs. It has been shown in the literature that reducing the contact resistance lowers the threshold voltage of the device, and thereby improves the overall performance of the device [9, 10]. The contact resistance between the source-drain electrodes and the organic semiconductor can be reduced by increasing the contact surface

area. The contact surface area can be increased by increasing the roughness of the electrode surface [11]. In the POGL OTFTs, the POGL layer increases the roughness of the electrode, as shown for the silicon surface in Figure 10.6, and thereby, increases the contact surface area which results in a decrease in the contact resistance. This reduction of the contact resistance at the electrode/organic semiconductor interface contributes to the reduction of the threshold voltage for the POGL OTFTs.

10.4.2 Impact of the POGL Layer on the Field-Effect Mobility of the OTFTs

From Figure 10.2 and 10.3, as well as from the mobility results obtained, we can see that the POGL OTFT has a smaller drain current and a slightly smaller mobility than the standard OTFT. One of the reasons for this is the surface roughness of the dielectric, which is affected by the POGL layer. Most of the charge carrier transport in OTFTs occurs in the first few molecular layers of the organic semiconductor, near the dielectric surface [12]. Thus, carrier transport in OTFTs is affected by the dielectric properties; particularly, the dielectric roughness and surface energy. Dielectric roughness can affect the charge transport in the channel of the device directly by forming trap sites, or indirectly by influencing the growth mode of organic semiconductors [13-15]. An SiO_2 surface with POGL on top is much rougher than a typical pure thermally oxidized SiO_2 surface. The AFM image of a POGL surface shown in Figure 10.6 illustrated this. As mentioned earlier, the RMS roughness is 1.33 nm, and the POGL aggregates form trap states (or roughness valleys) on the surface of the dielectric. The trap states on the dielectric surface immobilize many of the free charge carriers and reduce charge transport in the channel of the device.

The electric field from the drain electrode cannot significantly contribute to a vertical charge carrier movement that is directed away from the dielectric surface, out of the trap states [14]. The drain electric field assists horizontal charge carrier movement that is along the surface of the dielectric. The trapped charges can only move out by diffusion or by drift along a local horizontal potential gradient caused by roughness variations [14]. So, increasing the dielectric roughness decreases the drain current as well as the free charge carrier mobility [15, 16]. Therefore, the surface roughness of the dielectric layer increased by the POGL contributes to the lower drain current of the POGL OTFTs. The field-effect mobility is consequently also reduced, but not significantly in our results: it is in fact well within the mobility distribution of the standard OTFTs shown in Chapter 8. So, the POGL interfacial layer results in a significant beneficial reduction in threshold voltage at the cost of a slight reduction in mobility. However, we should point out that the mobility values reported for the POGL OTFT, as well as for the standard OTFTs, are actually higher than most P3HT based OTFTs with similar structures [2].

In addition to creating traps on the dielectric surface, the increased dielectric surface roughness influences the growth mode of organic semiconductors and thereby, their morphology [13, 15]. AFM images of P3HT deposited on both pure SiO_2 and POGL surfaces, where the POGL was previously deposited onto the SiO_2, are shown in Figure 10.7a and b respectively. From these AFM images, we can see that the morphology of the P3HT on a POGL surface is significantly different from the morphology of the P3HT on a SiO_2 surface. Our primary observations are that a high density of large voids exists between the grains of P3HT on the POGL surface, the P3HT structural grains on the POGL surface

are loosely interconnected with each other, and the grain size of P3HT on the POGL surface appears to be larger than the P3HT on the SiO_2 surface. The high density of voids and the non-uniform coverage of the P3HT on the POGL surface can arise from the defect sites on the POGL surface prior to P3HT deposition, which was illustrated in the AFM image of a POGL surface in Figure 10.6. These voids in the P3HT layer can limit the current transport in the channel of the device [17]. A good interconnection and tight packing between the grains of organic semiconductors can contribute to a higher current in the channel of a device [17]. Thus, the high density of voids and the loose interconnection between the P3HT grains also contribute to the lower drain current of the POGL OTFTs. However, the benefits that can arise from the lower threshold voltage, such as low power consumption, outweigh the relatively small negative impacts that can arise from the lower drain current, such as lower on/off current ratio. So, there is a design tradeoff between the threshold voltage and the drain current. The POGL OTFTs can provide a low threshold voltage at the cost of a lower drain current and thus a slightly reduced mobility.

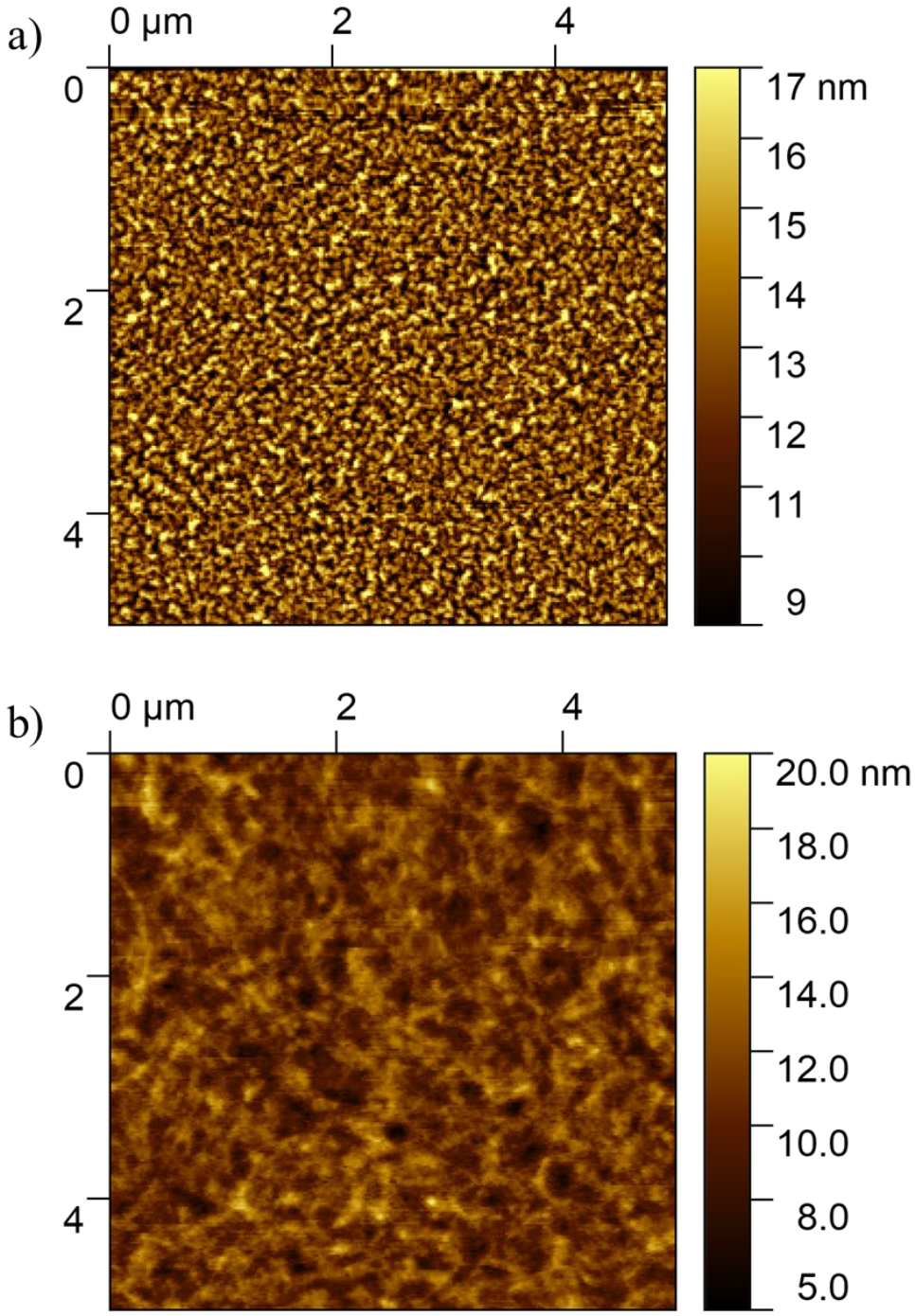

Figure 10.7. AFM images of P3HT on: a) SiO_2 surface and b) POGL surface where the POGL was previously deposited onto SiO_2

The other factor that affects the charge carrier transport in the channel of OTFTs is the surface energy of the dielectric and the P3HT. The surface energy has an impact on the growth mode as well as the morphology of organic semiconductors [18-20]. It is reported that the grain size of organic semiconductors is affected by the surface energy of the dielectric surface [17]. This is because when organic semiconductors are spin coated onto a dielectric surface the spreading of the organic semiconductor is dependent on the surface energy of the dielectric and the organic semiconductor itself. Therefore, it is important to determine the spreading coefficient of P3HT to investigate the effect of the surface energy of the dielectric on the crystal structure of P3HT, and how this is affected by a POGL interfacial layer. The equation for determining the spreading coefficient was given in Equation 9.3 of Chapter 9, which is rewritten here for convenience,

$$S_{1-2} = \gamma_1 - \gamma_2 - \gamma_{1-2} \tag{9.3}$$

The spreading coefficient of P3HT on a SiO_2 surface was determined in Chapter 9 and was found to be 4.13 mN/m. To determine the spreading coefficient of P3HT on a POGL surface, first the surface energy of POGL and P3HT need to be calculated. The surface energy of P3HT was determined in Chapter 9 and was found to be 27.0 mN/m. The dispersive and polar components of the P3HT surface energy were also calculated and found to be 25.3 mN/m and 1.7 mN/m, respectively. Determining the surface free energy of a POGL surface is a little different from the method we used for SiO_2 and P3HT surfaces. We did not use contact angel measurements to determine the POGL surface energy. Due to the different side chains of POGL that were exposed to the surface, the contact angle measurements were not consistent. The POGL can expose its hydrophobic or hydrophilic

sidechains to the test liquids depending on the substrate that the POGL is coated on, resulting in different contact angel measurements. Therefore, the rule of the mixture is applied to determine the surface energy of POGL. We assumed that the surface energy of POGL is mainly affected by the POEGMA and PLMA side chains, neglecting the PGMA side chain. The surface energy of POEGMA and PLMA is approximated by Polyethylene glycol (PEG) and Polyethylene-linear (PE), respectively [21]. Thus, POEGMA makes up 92.78% of the total weight of the POGL and PLMA makes up the remaining 7.22%. The results for the surface energy of POEGMA, PLMA, and POGL are shown in Table 2.

Table 10.1: Weight percentage and surface free energy of POEGMA, PLMA, and POGL.

Material	Weight Percent (%)	γ_S^d (mN/m)	γ_S^P (mN/m)	γ_S (mN/m)
POEGMA	92.78	30.9	12	42.9
PLMA	7.22	35.7	0	35.7
POGL	100	31.3	11.1	42.4

In addition to the surface energy of POGL and P3HT, we need the interfacial energy (γ_{1-2}) of the P3HT/POGL interface to calculate the spreading coefficient of P3HT on a POGL surface, as shown in Equation 9.3. The interfacial energy of P3HT/POGL was determined using Equation 9.8 that was given in Chapter 9 and rewritten below for convenience,

$$\gamma_{1-2} = \gamma_1 + \gamma_2 - \frac{4\gamma_1^d\gamma_2^d}{\gamma_1^d+\gamma_2^d} - \frac{4\gamma_1^p\gamma_2^p}{\gamma_1^p+\gamma_2^p} \quad (9.8)$$

Using the above equation, the interfacial energy of P3HT/POGL was determined to be 7.54 mN/m. The spreading coefficient of P3HT on a POGL surface was then determined using the surface energy of POGL in Table 2, the surface energy of P3HT found in Chapter 9 (27.0 mN/m), and the interfacial energy of P3HT/POGL found above (7.54 mN/m). The spreading coefficient was determined to be $S_{1-2} = 7.86\,\mathrm{mN/m}$. Under thermodynamic considerations, the spreading of the polymer liquid occurs when the spreading coefficient is positive. When the spreading coefficient is negative, the polymer liquid forms globules or dewets on the surface. Since the spreading coefficients of P3HT on both SiO_2 and POGL surfaces are positive, we can say that P3HT has no tendency to dewet from either surface. Thus, we suggest that the topography of the POGL layer is the primary reason for the roughness of P3HT on the POGL surface.

Another important factor that could affect the charge carrier transport in the channel of OTFTs is the interfacial interaction between the substrate and P3HT. The interfacial tension for P3HT/POGL was calculated above and was found to be 7.54 mN/m. The interfacial energy for P3HT/SiO_2 was calculated in Chapter 9 and was found to be 34.12 mN/m. The results indicate that the P3HT has a lower interfacial tension to the POGL surface. This means that the P3HT has a higher affinity to the POGL surface than the SiO_2 surface. This contributes to a better charge carrier transport in the channel of the device. However, this did not translate very well because of the defects and traps that are in the interfacial layer. Therefore, if we can eliminate the traps and defects at the interfacial layer and avoid the voids in the P3HT layer, we can significantly increase the charge carrier transport in the channel of the POGL OTFTs. We are currently working toward this goal.

We are investigating different ways to remove the traps at the interfacial layer as well as to increase the uniform coverage of P3HT on the POGL surface.

10.5 Conclusions

The effects of a POGL interfacial layer on the performance of P3HT based OTFTs were investigated. We fabricated OTFTs with and without a POGL interfacial layer. Current–Voltage (I-V) measurements were performed to characterize the performance of the OTFTs. The threshold voltage and the field-effect mobility of the devices were extracted. The POGL OTFTs were observed to have a significantly lower threshold voltage than the OTFTs with no interfacial layer. The POGL OTFTs also showed much more ideal drain current saturation characteristics with a smaller I-V curve slope in the saturation region. This is primarily explained by the deep trap states on the POGL surface and the reduction of the contact resistance at the electrode/organic semiconductor interface. Because of this significantly low threshold voltage, the POGL OTFTs can be considered for low power electronic devices. The POGL OTFTs were also observed to have smaller drain current and a slightly smaller field-effect mobility than the standard OTFTs. This is likely a side effect of the surface roughness of the dielectric caused by the POGL layer. The drain current, and thereby the mobility, can be enhanced by reducing the voids and increasing the interconnection between the grains of the P3HT. The results in this chapter have been partially published in [8].

10. 6 References

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CHAPTER ELEVEN

EFFECTS OF A COMPOSITE INTERFACIAL LAYER ON THE PERFORMANCE OF ORGANIC THIN-FILM TRANSISTORS

11.1 Introduction

The third interfacial material that was investigated to enhance the performance of the OTFTs was a composite of GO and P(OEGMA-GMA-LMA), which is denoted as GO-POGL. The GO-POGL was used to modify both the electrode and the dielectric surfaces. The GO-POGL solution was synthesized in the laboratory. It is prepared from virgin GO and POGL solutions. The GO solution was used as received from the supplier, and the POGL solution was synthesized in the laboratory through a radical polymerization method [1] as reported in Chapter 10. To the best of our knowledge, there are no published reports where GO-POGL was used as an interfacial material in OTFTs. So, in this chapter we investigate the impact of a GO-POGL composite interfacial layer on the performance of P3HT based OTFTs.

In this investigation, OTFTs with and without a GO-POGL interfacial layer were fabricated. The OTFTs with a GO-POGL interfacial layer are referred to as GO-POGL OTFTs, while the OTFTs without a GO-POGL layer are referred to as standard OTFTs. I-V measurements were performed on both devices, and the primary device performance parameters were extracted. Atomic force microscopy (AFM) imaging was performed to analyze the morphology of the GO-POGL and P3HT layers. Contact angle measurements were performed to analyze the surface energy and interface interaction of the GO-POGL and P3HT layers.

According to the I-V measurements and extracted parameters, the GO-POGL OTFTs have a higher performance than the standard OTFTs. Specifically, we determined that the drain current and the field-effect mobility of the OTFTs were increased, and the threshold voltage was reduced by modifying the dielectric and electrode surfaces with the GO-POGL layer. The increased drain current and mobility of the GO-POGL OTFTs is associated with the larger grain size of the P3HT on the GO-POGL surface and the lower interface tension between the GO-POGL and P3HT layers. The reduction of the threshold voltage is associated with the deep trap states on the GO-POGL surface and the reduction of the contact resistance at the Au/P3HT interface.

11.2 Fabrication of OTFTs with a GO-POGL Interfacial Layer

The fabrication of the GO-POGL OTFTs followed a similar fabrication process as the POGL OTFTs described in Chapter 10. The only difference being we used a GO-POGL composite interfacial material instead of pure POGL. The GO-POGL solution was synthesized in the laboratory. It was synthesized by Mastooreh Seyedia and Andrii Tiiara in Dr. Igor Luzinov's laboratory. The solution was prepared by mixing GO and POGL solutions. The GO was obtained from Goographene, Inc, with a concentration of 5 mg/ml in DI water. The dimensions of the GO sheets were several hundred nanometers up to several micrometers in the XY plane and 0.7 – 1.2 nm in thickness, according to the manufacturer. The POGL solution was synthesized using a radical polymerization method as reported in Chapter 10. The GO and the POGL solutions were mixed in a 1:2.5 mass ratio in an aqueous environment. The GO suspension was added to the POGL solution

dropwise to inhibit stacking of GO sheets by bridging one POGL chain between multiple sheets. The mixture was vigorously shaken for 15 minutes and stirred for more than 4 hours to give enough time for the POGL chains to attach to the GO sheets.

After the GO-POGL solution was prepared, it was spin coated onto a wafer with the gate, drain, and source contacts previously deposited and patterned in the same way as the standard OTFTs. The fabrication process for the standard OTFTs was described in detail in Chapter 7. Prior to spin coating the GO-POGL solution, the solution was agitated in an ultrasonic bath for 4 minutes to reduce the aggregates in the solution, and immediately spin coated at an acceleration of 1000 rpm/sec until a maximum speed of 2000 rpm was reached and maintained for 60 seconds, and subsequently baked at 110 ˚C for 40 minutes. The P3HT was then spin coated on top of the GO-POGL layer and baked afterward using the same spinning and baking recipe as for the standard OTFTs. The GO-POGL and the P3HT layers were then patterned together in the same way as the standard OTFTs. More than 226 GO-POGL OTFTs were fabricated on a single wafer. The same number of standard OTFTs were also fabricated on another wafer at the same time under similar environmental conditions. The schematic structure of the GO-POGL OTFT is illustrated in Figure 11.1. The structure of the device and the dimensions of the conductive channel were essentially identical to the standard devices with the exception of the GO-POGL interfacial layer.

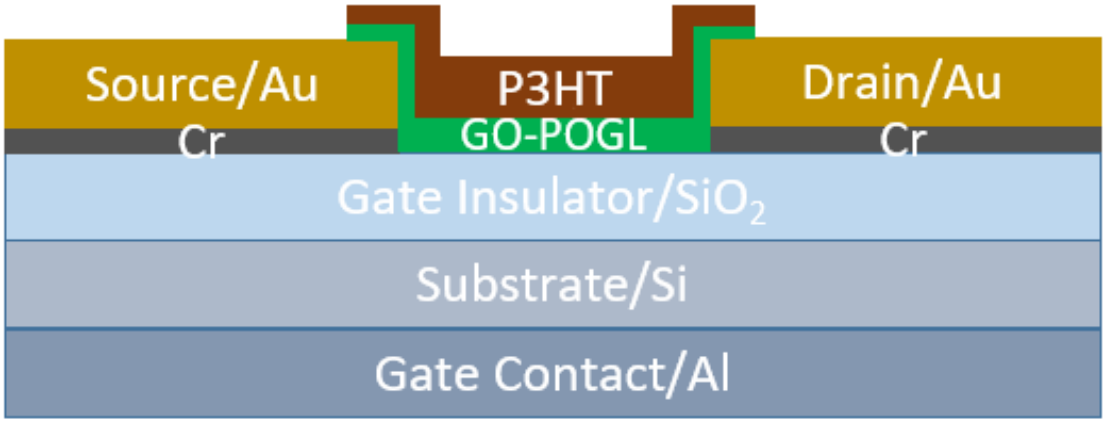


Figure 11.1. Schematic structure of the GO-POGL OTFT

11.3 Electrical and Material Characterization

I_{DS}-V_{DS} measurements were performed by applying a drain voltage from 0 V to -70 V with an increment of -0.5 V while biasing the gate with voltages ranging from 0 V to -60 V with an increment of -20 V. I_{DS}-V_{GS} measurements were performed by applying a gate voltage from 20 V to -60 V while biasing the drain electrode at -5 V. AFM imaging was performed in tapping mode to investigate the morphology of the P3HT and GO-POGL layer. To determine the surface energy of GO-POGL, contact angle measurements of the immersion liquids (hexadecane and water) were performed at 20 seconds after droplet deposition on the GO-POGL surface.

11.4 Results and Discussion

The electrical measurements were performed on both standard and GO-POGL OTFTs. Measurements were performed on a total of 42 devices; 21 standard OTFTs and 21 GO-POGL OTFTs. Out of these devices we have selected two devices: one device that can

represent standard OTFTs and another device that can represent GO-POGL OTFTs. The output characteristics of a standard and GO-POGL OTFTs are shown in Figures 11.2 and 11.3, respectively. In both figures, the drain current is plotted as a function of the drain voltage at various gate voltages. Comparing the I-V characteristics of the devices in both figures, we can see that the drain current magnitude for the GO-POGL OTFT is higher than for the standard OTFT at all gate and drain voltages. In addition, the GO-POGL OTFT displays I-V curves with a smaller slope in the saturation region than the standard OTFT, which means the drain current for the GO-POGL OTFT saturates at a lower drain voltage than that of the standard OTFT. So, inserting the GO-POGL interfacial layer has significantly changed the I-V characteristics of the OTFTs.

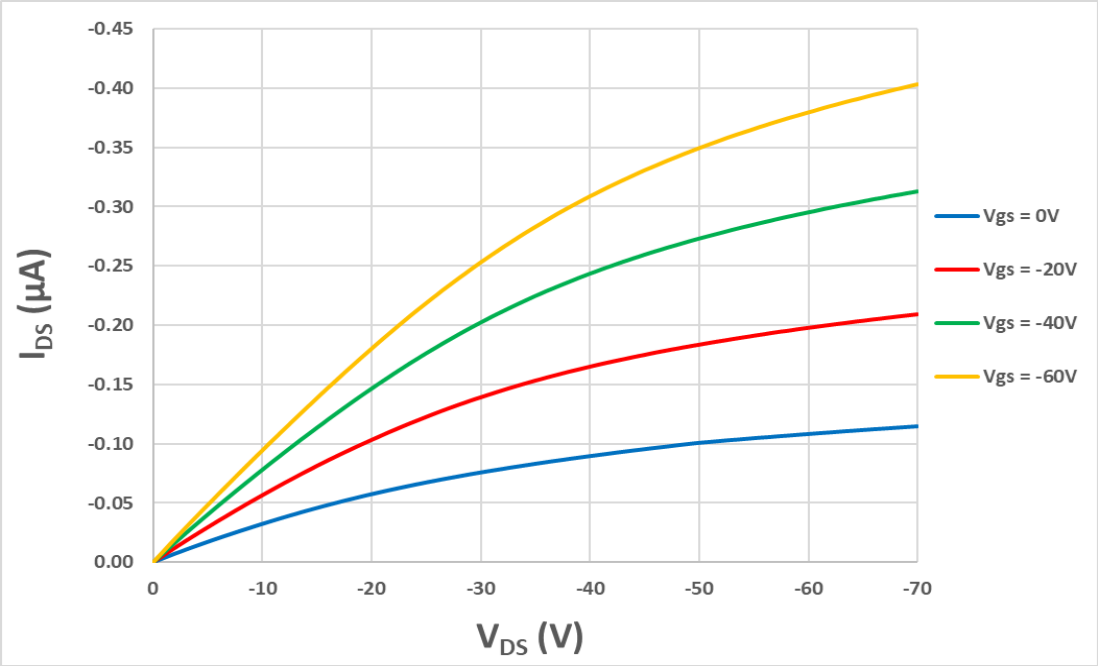


Figure 11.2. I_{DS} - V_{DS} output characteristics of a standard OTFT at different values of V_{GS}.

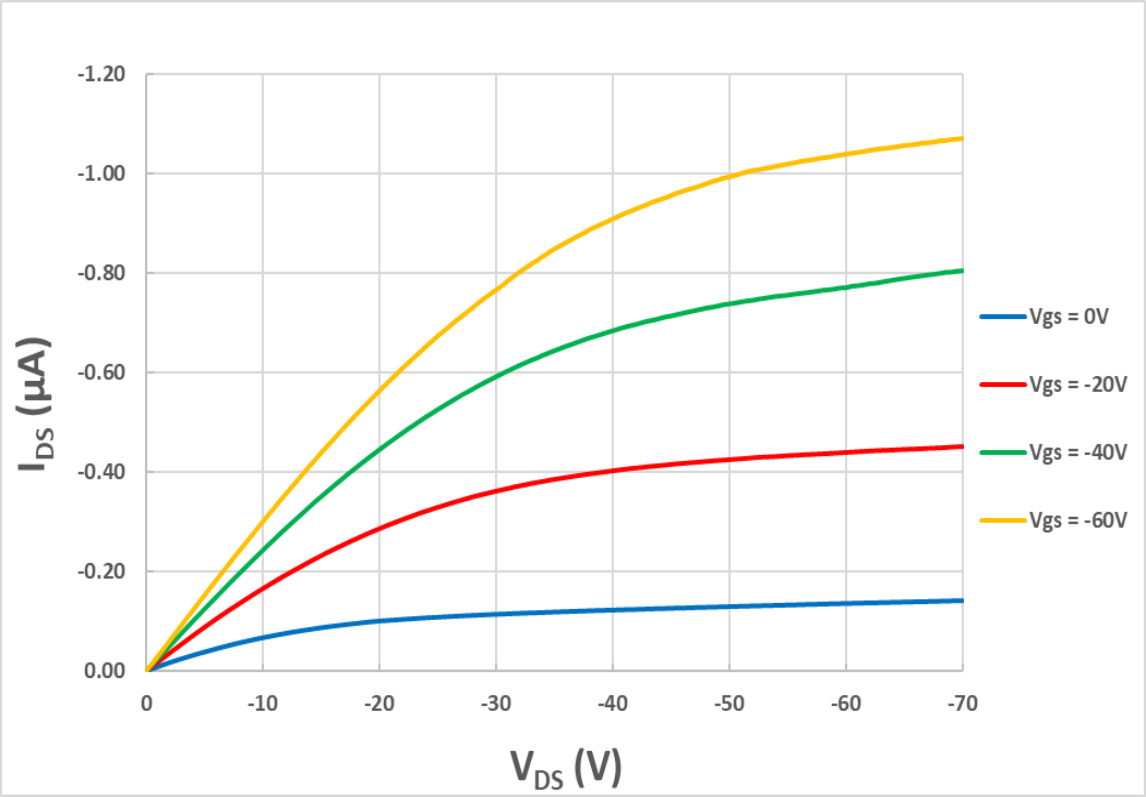
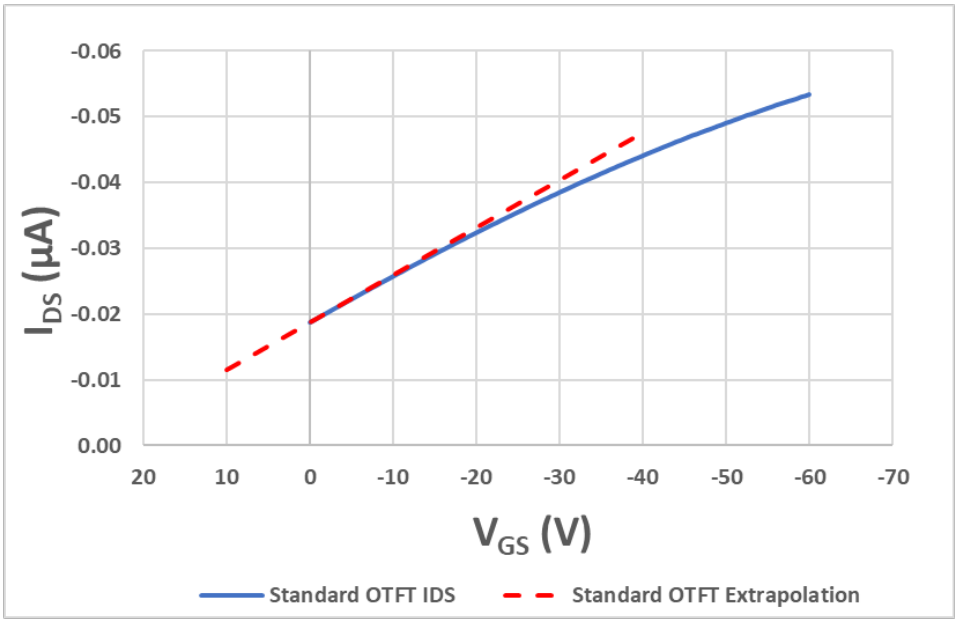


Figure 11.3. I_{DS} - V_{DS} output characteristics of a GO-POGL OTFT at different values of V_{GS}.

The transfer characteristics (I_{DS}-V_{GS}) of standard and GO-POGL OTFTs are shown in Figures 11.4a and b, respectively. The threshold voltage and the field-effect mobility of these devices were extracted using the transfer curves. An extrapolation in the linear region method (ELR) was used to determine the threshold voltage of both devices. The threshold voltage for the standard OTFT was determined to be 28.47 V, and the threshold voltage for the GO-POGL OTFT was determined to be 14.54 V. The threshold voltage of the GO-POGL OTFT is significantly smaller, almost halved, compared to the standard OTFT. This

significantly smaller threshold voltage is attractive as it results in a lower power consumption. The field-effect mobilities in the linear region of both devices were also extracted. The field-effect mobilities in the linear region of the standard and GO-POGL OTFTS were determined to be $1.25 \times 10^{-3}\, cm^2/_{Vs}$ and $2.82 \times 10^{-3}\, cm^2/_{Vs}$, respectively. This mobility for the GO-POGL OTFT is more than double that of the standard OTFT. Thus, employing the GO-POGL interfacial layer has enhanced the performance of the OTFTs both in terms of the threshold voltage, which was nearly cut in half, and the mobility, which was more than doubled.

a)



b)

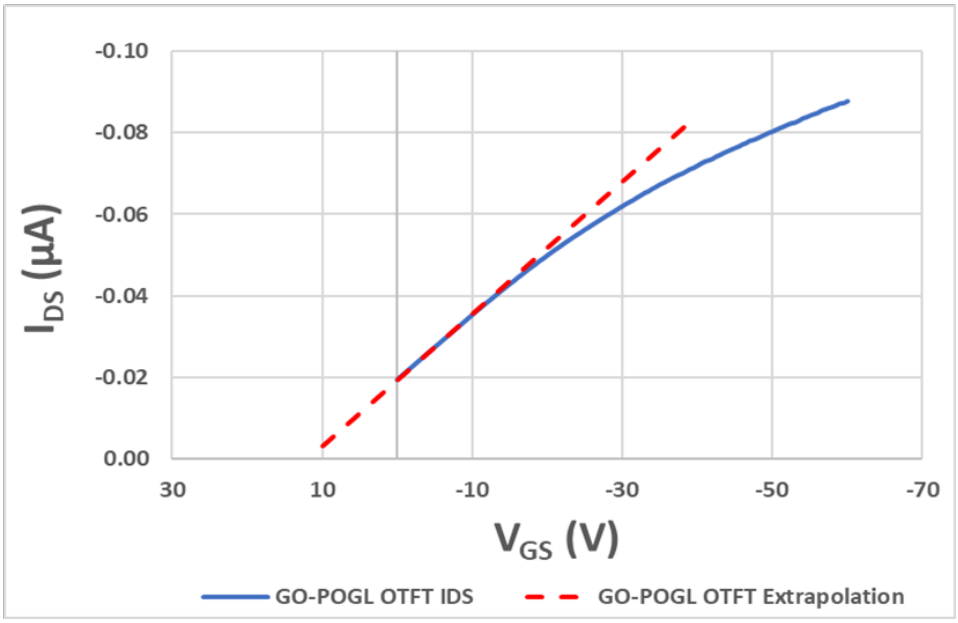


Figure 11.4. Transfer characteristics of a) standard and b) GO-POGL OTFTs at V_{DS} = -5 V, along with the linear extrapolation of the curve at maximum transconductance.

The threshold voltage and mobility of the standard OTFTs shown above are a little lower than the values reported in the previous chapters for standard OTFTs. One of the main reasons for this is a tool change. The spin coater that was used for depositing the P3HT in previous fabrications was replaced with another coater during the fabrication of the OTFTs reported in this chapter. In addition, we used a different batch of P3HT. These changes can affect the coating of the P3HT and its crystal structure, and consequently, the electronic properties of the devices. However, since both the standard and the GO-POGL OTFTs reported in this chapter were fabricated simultaneously with the same tools under similar environmental conditions, it is valid to compare these two devices.

Even with the values reported in the previous chapters, there is always some natural variation with each batch of the standard device fabrication. The variations are mainly because of the current environmental conditions and tool chamber variations. As it is well known, cleanroom tools breakdown frequently, and they don't always return to their previous condition. The changes in the tool can affect some of the processes in the fabrication; particularly, the metal deposition and dry etch. These changes could potentially affect the properties of the materials and ultimately, the device characteristics. However, in this work the focus of our investigation is the change in the performance parameters of the OTFTs between the standard and the modified devices, which were fabricated simultaneously under the same environmental conditions

11.4.1 Impact of the GO-POGL Layer on the Drain Current and Mobility of the OTFTs

Comparing Figures 11.2 and 11.3 and the mobility results reported above, it is clear that the GO-POGL OTFT has a higher drain current and mobility than the standard OTFT. This can be explained by the morphology change of the P3HT when it is deposited onto a GO-POGL layer rather than a pure SiO_2 layer. In Figure 11.5, we show the AFM images of P3HT deposited onto a pure SiO_2 surface and P3HT deposited onto a SiO_2 surface covered with a GO-POGL layer. The grain size of P3HT on the GO-POGL surface, shown in Figure 11.5b, is larger than the grain size of P3HT on the SiO_2 surface shown in Figure 11.5a. This difference in grain size affects the movement of charge carriers in the channel of the transistors. It has been demonstrated in the scientific literature that a small grain size of polymer crystals in organic transistors results in a high density of grain boundaries in the channel of the transistor [2, 3, 4]. A high density of grain boundaries is known to form a high density of trap states that block the movement of charge carriers in the channel of the transistor, decreasing the probability of charge scattering. The mobility of charge carriers in the channel of organic transistors can be divided into two components, mobility in the grain and mobility in the grain boundary [5]. Since these two mobility components are connected in series, the mobility value for one of the components affects the total mobility of charge carriers in organic semiconductors. This means if there is a high density of grain boundaries in the organic semiconductor, the mobility in the grain boundaries becomes small, and the total mobility of charge carriers in the organic semiconductor will be reduced. Since the P3HT on the GO-POGL layer has larger grains than the P3HT on the

SiO_2 layer, the P3HT on the GO-POGL layer has less grain boundaries and therefore, the GO-POGL OTFTs will have a higher drain current and mobility than the standard OTFTs.

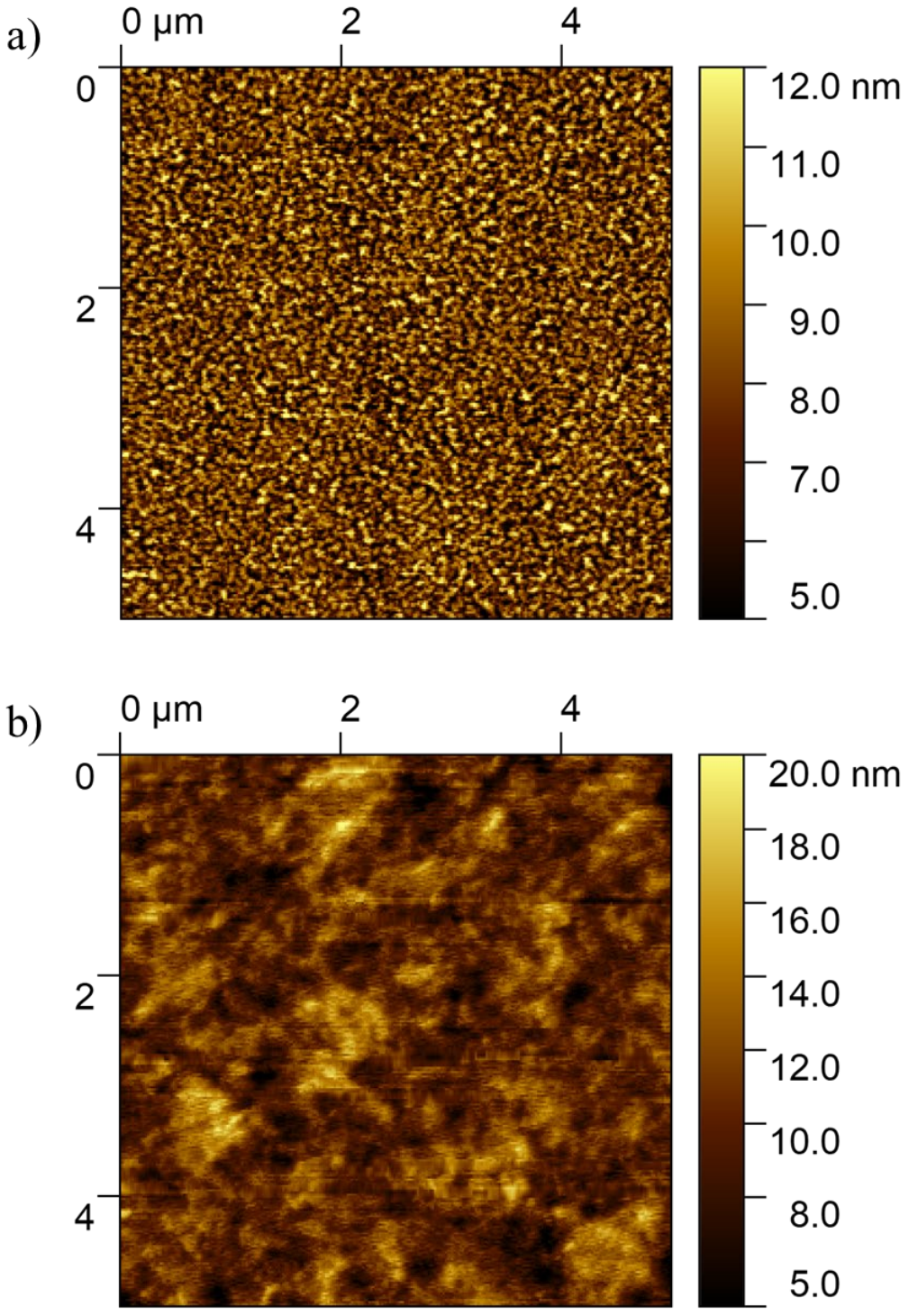


Figure 11.5. AFM images of P3HT on a) SiO2 and b) GO-POGL Surfaces

From Figure 11.5, in addition to the larger grain size of P3HT on the GO-POGL surface, we can observe that the P3HT structural grains on the GO-POGL surface are more closely interconnected than the P3HT grains on the SiO_2 surface, despite a few vacant spots. This close interconnection can improve the contact surface area between the grains of the P3HT. A good interconnection and a high contact surface area between the grains of organic semiconductors result in an efficient charge transport and enhanced drain current in the channel of the organic transistors [6]. Thus, the close interconnection and increased contact surface area between the P3HT grains can contribute to the high drain current and mobility observed in the GO-POGL OTFTs.

The morphology change of P3HT on the GO-POGL layer can be related to the interfacial interaction between P3HT and GO-POGL layers. In addition, most of the charge carrier transport in OTFTs occurs within a few molecular layers of the organic semiconductor near the dielectric surface [7-9]. Thus, the interfacial interaction between the dielectric and the organic semiconductor layers plays a critical role in the transport of charge carriers in the channel of the transistors. To this end, we estimated the interfacial tension of the P3HT/GO-POGL interface and compared it to the interfacial tension of the P3HT/SiO_2 interface that was determined in Chapter 9. The interfacial tension for the P3HT/GO-POGL interface was determined using Equation 9.7, which is also given below for convenience,

$$\gamma_{1-2} = \gamma_1 + \gamma_2 - \frac{4\gamma_1^d\gamma_2^d}{\gamma_1^d+\gamma_2^d} - \frac{4\gamma_1^p\gamma_2^p}{\gamma_1^p+\gamma_2^p} \tag{9.7}$$

To determine the interfacial energy of the P3HT/GO-POGL (γ_{1-2}) interface, we need to first determine the surface energy of GO-POGL and P3HT, as shown in the equation above.

The surface energy of P3HT was estimated in Chapter 9 and found to be 27.0 mN/m with dispersive and polar components of 25.3 mN/m and 1.7 mN/m, respectively. The surface energy of GO-POGL was also estimated using the same model, the Owens-Wendt model [10, 11]. The details of the surface energy calculations using this model were shown in Chapter 9, where the surface energy for the SiO_2 and GO surfaces were calculated. The surface energy calculation for the GO-POGL surface followed essentially the same steps. First, the contact angles of water and hexadecane on a GO-POGL surface were measured. The contact angle of water and hexadecane on a GO-POGL surface was measured to be 50.94° and 0, respectively. Then, the dispersive and polar components of the surface energy of GO-POGL were calculated using Equations 9.5 and 9.6, which are also given below for convenience,

$$\gamma_{L1}(1 + cos\theta 1) = 2\sqrt{\gamma_S^d \gamma_{L1}^d} + 2\sqrt{\gamma_S^P \gamma_{L1}^P} \tag{9.5}$$

$$\gamma_{L2}(1 + cos\theta 2) = 2\sqrt{\gamma_S^d \gamma_{L2}^d} + 2\sqrt{\gamma_S^P \gamma_{L2}^P} \tag{9.6}$$

The dispersive and polar components of the surface free energy of GO-POGL were estimated to be 26.4 mN/m and 24.5 mN/m, respectively. The total surface energy (γ_S) of GO-POGL, which is found by adding the two components, is 50.9 mN/m. Therefore, using this surface energy value of GO-POGL and the P3HT found in Chapter 9 (27.0 mN/m), the interface energy for P3HT/GO-POGL is determined to be 19.9 mN/m, which is smaller than the interfacial energy for P3HT/SiO_2 (34.12 mN/m). The smaller interfacial tension between the GO-POGL and P3HT layers indicates a higher level of attraction between the two layers [12, 13]. This means that the P3HT has a higher affinity to the GO-POGL

surface than the SiO_2 surface. We suggest this lower interfacial tension between the P3HT and the GO-POGL layers contributes to the enhanced drain current and mobility of the GO-POGL OTFTs, as most of the charge carrier transport occurs near the GO-POGL surface.

We also checked the spreading coefficient of P3HT on a GO-POGL surface to determine if it has any impact on the morphology of P3HT. The spreading coefficient of P3HT on a GO-POGL surface was determined using Equation 9.3, which is rewritten below for reference.

$$S_{1-2} = \gamma_1 - \gamma_2 - \gamma_{1-2} \tag{9.3}$$

The spreading coefficient of P3HT on a GO-POGL surface was determined to be 4.04 mN/m, which is close to the spreading coefficient of P3HT on a SiO_2 surface (4.13 mN/m). Since the spreading coefficient of P3HT on a GO-POGL surface is positive, there is no tendency to dewet from the GO-POGL surface, and no significant impact on the morphology of the P3HT as its value is very close to the spreading coefficient of P3HT on a SiO_2 surface.

11.4.2 Impact of the GO-POGL Layer on the Threshold Voltage of the OTFTs

In addition to the enhanced drain current and mobility, the GO-POGL interfacial layer resulted in a lower threshold voltage for the GO-POGL OTFTs, which results in a lower power consumption. To investigate this result, we investigated the surface roughness of the dielectric layer, as the dielectric surface influences the structure of the organic semiconductors and the transport of charge carriers in the channel of OTFTs [14, 15]. A

topographic AFM image of a GO-POGL layer deposited onto a blank silicon wafer is shown in Figure 11.6. Since GO-POGL is a composite of GO and POGL, its structure is influenced by both GO and POGL molecular structures. The influence of GO can be seen in the sheet-like structure of the GO-POGL, and the POGL aggregates can be seen in the bright spots of the GO-POGL. The thickness of the POGL layer was measured from a cross-sectional analysis of the AFM image and found to be 4.6 nm. The root-mean-square roughness was also obtained from the AFM image and found to be 2.8 nm. For the most part, the GO-POGL has a uniform coverage of the silicon wafer, except for a few vacant spots. The RMS roughness value is also indicative of these vacant spaces, or roughness valleys. The roughness valleys can form deep trap states and trap most of the free charge carriers that were not trapped by the shallow traps [16]. We suggest this results in a drain current that saturates with a relatively small slope and begins to saturate at a lower drain voltage. Therefore, the enhanced drain current saturation characteristics and the threshold voltage reduction of the GO-POGL OTFTs can be attributed to the deep trap states on the GO-POGL surface.

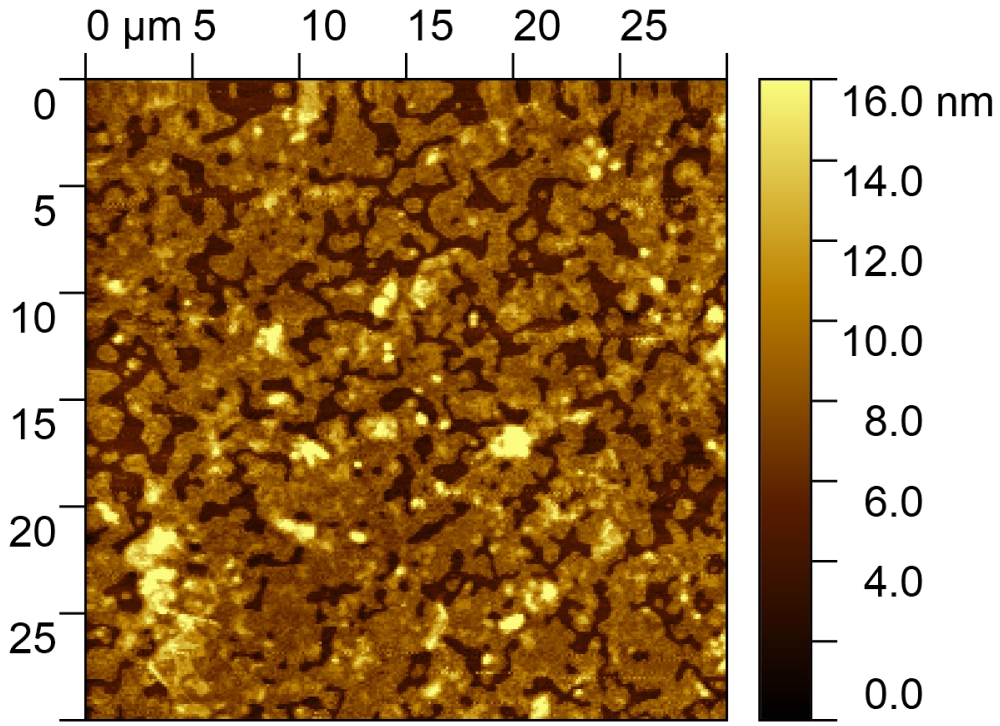


Figure 11.6: AFM image of GO-POGL on a silicon wafer

The GO-POGL interfacial layer was also present at the source-drain electrode/organic semiconductor interfaces and thus, the modification of the electrode surface is also responsible for the reduction of the threshold voltage and enhancement of the drain current and mobility of the GO-POGL OTFTs. For an efficient charge injection process from the electrode into the organic semiconductor, there must be a good compatibility between the electrode and the organic semiconductor. One of the main components of the GO-POGL composite is GO. GO has been demonstrated to have a good interface interaction with Au [17], which is the source and drain electrode material for the devices in this work. The GO-modified Au electrodes have smaller contact resistance with organic semiconductors compared to pure Au electrodes [17]. Thus, the GO component of

the GO-POGL composite can contribute to a better interface interaction between GO-POGL and P3HT, which can result in a lower contact resistance between Au and P3HT.

In addition to the compatibility between GO-POGL and Au, another important factor that can contribute to a lower contact resistance is an increased contact surface area. One of the methods of increasing the contact surface area is by increasing the roughness of the interfacial layer [18]. In Figure 11.6 we showed a silicon wafer covered with GO-POGL. In this figure we can clearly see that the surface roughness of the silicon wafer was increased because of the GO-POGL layer. In fact, the RMS roughness from the AFM image was found to be 2.8 nm. In the same way, the modification of the Au electrode with the GO-POGL can increase the roughness of the Au electrode and thereby, its contact surface area with the P3HT, which can result in a lower contact resistance between the two layers. A lower contact resistance between an electrode and an organic semiconductor has been shown to decrease the threshold voltage [19, 20] and increase the mobility of organic transistors [18, 21]. Thus, we suggest that the reduction in the contact resistance between the Au and P3HT layers, due to the addition of the GO-POGL layer, can contribute to the lower threshold voltage and higher mobility observed in the GO-POGL OTFTs.

11.5 Conclusions

A composite material, synthesized from GO and P(OEGMA-GMA-LMA) solutions, was used as an interfacial material for P3HT based OTFTs. This material is denoted as GO-POGL. The effects of a GO-POGL interfacial layer on the operation of

P3HT based OTFTs were investigated. The OTFTs with and without a GO-POGL interfacial layer were fabricated. The devices were then characterized electrically, and the primary performance parameters were extracted. We determined that the OTFTs with the GO-POGL interfacial layer have a lower threshold voltage, higher drain current, and higher mobility than the standard OTFTs. The higher drain current and mobility are attributed to the larger grain size of P3HT deposited onto the GO-POGL surface and the lower interfacial tension between the GO-POGL and P3HT layers. The lower threshold voltage is attributed to the deep trap states on the GO-POGL layer and the smaller contact resistance between the GO-POGL modified Au electrodes and P3HT.

The OTFTs with the GO interfacial layer were observed to have a higher mobility than the OTFTs with no interfacial layer, but the threshold voltage of these OTFTs was also increased. The OTFTs with the POGL interfacial layer had a significantly lower threshold voltage but their mobility did not improve. The OTFTs with the GO-POGL interfacial layer, however, had a lower threshold voltage and a higher mobility, which is the optimum case for both parameters. Therefore, the POGL interfacial layer enhanced the performance of the OTFT in both measured parameters.

11.6 References

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CHAPTER TWELVE

SUMMARY AND FUTURE WORK

12.1 Summary

In this dissertation, we investigated the performance of organic thin-film transistors (OTFTs) by employing different interfacial materials. First, we designed and developed a photolithographic fabrication process for P3HT based OTFTs. The structure of the transistors was based on the bottom gate bottom contact OTFT. We presented an optimized fabrication method that is applicable in typical silicon-based fabrication facilities. The fabrication process resulted in many devices in a single wafer that were uniform and consistent in both electrical characteristics and geometry. The fabrication process was cost effective and relatively straightforward to implement, as most of the fabrication steps were performed at room temperature and atmospheric pressure.

The fabricated OTFTs were characterized electrically by performing I-V measurements. We extracted the threshold voltage and the field-effect mobility in the linear operation region. The threshold voltage and mobility of one of the OTFTs, which was a representative of the majority of the devices, was determined to be 30.8 V and $5.5 \times 10^{-3}\ {cm^2}/{Vs}$, respectively. The mobility was shown to be higher than most values reported in the literature for other bottom gate bottom contact P3HT based OTFTs. The consistency and uniformity of the transistors across the wafer was illustrated by the mobility distribution of 24 randomly selected devices. More than half of the devices had mobilities that were in the range of $4.0 - \ 6.0 \times 10^{-3}\ {cm^2}/{Vs}$. This high mobility, and its

consistency across the wafer, was primarily attributed to the developed fabrication process and the careful annealing of the P3HT polymer.

Interface engineering was then performed to investigate the effects on the performance of the OTFTs. Three interfacial materials were investigated for this purpose: graphene oxide (GO), P(OEGMA-GMA-LMA), and a composite of GO and P(OEGMA-GMA-LMA). Virgin GO "as received" from the supplier was used to modify both the electrode/organic semiconductor and the dielectric/organic semiconductor interfaces of the OTFTs. The OTFTs with a GO interfacial layer were demonstrated to have a higher performance than the devices without an interfacial layer. In particular, the drain current and the field-effect mobility of the OTFTs were considerably increased by the modification of the Au and the SiO_2 surfaces with virgin GO nanoscale layers. We also observed that the threshold voltage for the GO OTFTs were higher than the OTFTs with no interfacial layer, which is not optimal for low-power devices. We primarily attributed the enhanced drain current and mobility to the particular morphology of the P3HT, where larger interconnecting P3HT grains were formed on the GO layer deposited on SiO_2 surface. The larger P3HT grains on the GO-modified SiO_2 surface was explained by the interface interaction of the P3HT/GO and the topography of the GO surface. The organic semiconductors with large grain sizes have been demonstrated to have a higher mobility than the organic semiconductors with smaller grain sizes due to the smaller grain boundary density [1-3]. This result was confirmed by the DSC measurements in this work. In addition to the larger P3HT grain sizes, we attributed the enhanced performance of the OTFTs with the decrease in contact resistance between the GO-modified Au electrode and the P3HT.

The second interfacial material investigated was a copolymer known as P(OEGMA-GMA-LMA), or POGL. POGL is a cross-linkable amphiphilic copolymer that can form a covalent bonding with surfaces. It was synthesized in the laboratory through a radical polymerization method using three monomers, oligo (ethylene glycol) methyl ether methacrylate (OEGMA), glycidyl methacrylate (GMA), and lauryl methacrylate (LMA). POGL was used to modify both the electrode and the dielectric surface of the OTFTs. The OTFTs with a POGL interfacial layer were observed to have a significantly lower threshold voltage than the OTFTs with no interfacial layer. In addition, the OTFT with a POGL interfacial layer showed much more ideal drain current saturation characteristics with a smaller I-V curve slope in the saturation region. This is explained by the deep trap states on the POGL surface and the reduction of the contact resistance at the electrode/organic semiconductor interface. The POGL OTFTs were also observed to have smaller drain current and a slightly smaller field-effect mobility than the OTFTs with no interfacial layer. This was explained as a side effect of the surface roughness of the dielectric caused by the POGL layer.

The third and final interfacial material that was investigated was a composite of GO and P(OEGMA-GMA-LMA), or GO-POGL. The GO-POGL solution was prepared in the laboratory by mixing GO and POGL solutions. GO-POGL was used to modify the electrode/organic semiconductor and the dielectric/organic semiconductor interfaces. The OTFTs with a GO-POGL interfacial layer were observed to have a better performance than the OTFTs with no interfacial layer. Specifically, we determined that the OTFTs with a GO-POGL interfacial layer have a higher drain current and mobility, as well as a lower

threshold voltage than the OTFTs with no interfacial layer. We associated the higher drain current and mobility of the GO-POGL OTFTs with the larger grain size of the P3HT and the lower interfacial tension between the GO-POGL and the P3HT layers. The lower threshold voltage is associated with the deep trap states on the GO-POGL layer and the reduced contact resistance between the GO-POGL modified Au and P3HT.

In conclusion, we have used three interfacial materials to enhance the performance of P3HT based OTFTs. The GO interfacial layer increased the drain current and the field-effect mobility of the OTFTs but did not reduce the threshold voltage. The POGL interfacial layer reduced the threshold voltage of the OTFTs but did not improve the mobility. The GO-POGL interfacial layer reduced the threshold voltage, increased the drain current, and increased the field-effect mobility of the OTFTs. Therefore, by mixing the GO and POGL solutions into a composite material, we were able to obtain the best of both "worlds", which resulted in enhancing the performance of the OTFTs in all measured parameters, i.e., drain current, threshold voltage, and field-effect mobility.

12.2 Future Work

Even though we enhanced the performance of the OTFTs using the interface engineering method summarized above, there is still room for further enhancement of the performance of the OTFTs. To this end, we suggest three research ideas that could be performed to further advance this research work. The first research could be further investigating the interfaces of the devices. We performed interface engineering at the electrode/organic semiconductor and dielectric/organic semiconductor interfaces, and

improved the performance of the devices; however, we can still reduce the density of the interface states and the voids in the P3HT for a better optimization of the OTFTs. In addition, in our investigation we did not investigate these interfaces separately. For the devices reported in this dissertation, the interfacial material was deposited and patterned using a single reticle for both the electrode and the dielectric surfaces, thus the interfacial layer was present on both the electrode and the dielectric surfaces. This prohibited us from independently investigating the effects of the interfacial material on each interface separately. Therefore, instead of using one reticle to pattern the interfacial material, we would need to design two new reticles: one for the dielectric surface and another for the electrode surface. The reticle for the dielectric surface would be used to pattern the interfacial material on the dielectric surface of the channel, which is between the edges of the source and the drain electrodes without touching the sidewalls of the electrodes as illustrated in Figure 12.1. The reticle design for the electrode would be used to pattern the interfacial material on the electrode surface only without touching the dielectric surface, which is illustrated in Figure 12.2. Thus, we could investigate the two interfaces separately. This would also make it possible to apply two different interfacial materials in a device: one at the electrode/organic semiconductor interface and another at the dielectric/organic semiconductor interface. Therefore, careful consideration and design of the interfaces in OTFTs is crucial to optimize the operation of the devices and improve their performance.

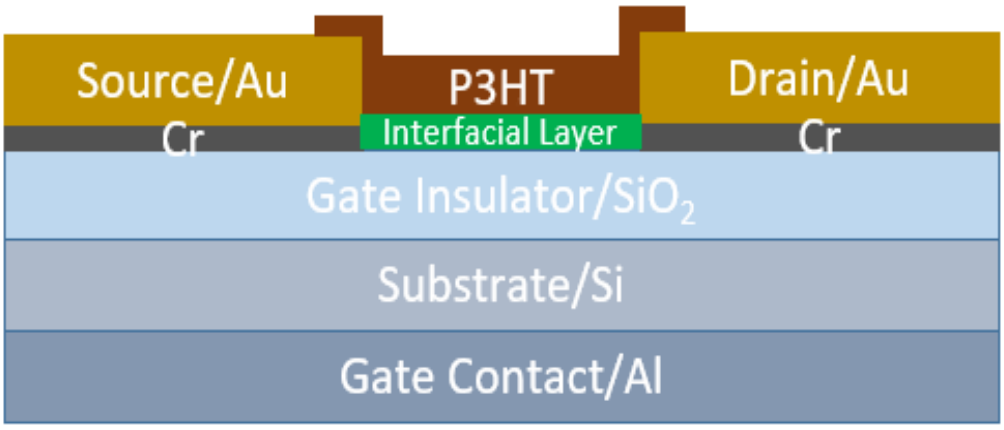

Figure 12.1: Schematic structure of OTFT with an interfacial layer at dielectric/organic semiconductor interface

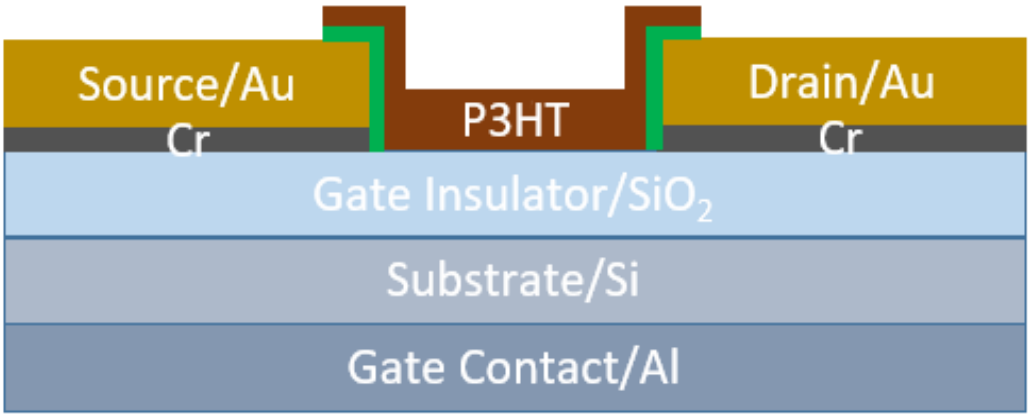

Figure 12.2: Schematic structure of OTFT with an interfacial layer at the electrode/organic semiconductor interface

The second research could be investigating the optimal channel length of the OTFTs. All the devices reported in this dissertation have essentially identical dimensions. In particular, the dimensions of the conductive channel length and width of the devices were 50μm and 500μm, respectively. This resulted in a width to length ratio of 10. It has been shown in the literature that the channel length affects the contact resistance of the device and ultimately the performance of the OTFTs [4-7]. For example, in reference [4], when the channel length of a bottom contact benzanthracene based OTFT was reduced from 20μm to 2.5μm, the field-effect mobility of the devices increased and the threshold voltage magnitude decreased. In another example [5], the threshold voltage magnitude of a pentacene based OTFT decreased as the channel length was reduced from 40 μm to 5 μm for both top and bottom contact devices. The highest mobility for the top contact OTFTs was reported at 5 μm and it decreased as the channel length increased to 20 μm and remained constant until 40 μm, which was the longest channel length investigated. In contrast, the mobility for the bottom contact OTFT increased with the channel length. From the above two specific examples and some additional examples [6, 7], it is clear that varying the channel length affects the performance parameters of OTFTs. Hence, it is important to investigate channel length effects on device performance, and ultimately to obtain an optimal channel length for the devices.

The third research could be investigating the effects of organic solvents on the crystallinity of P3HT. There are several solvents that can be used to dissolve P3HT, such as, chloroform, chlorobenzene, 1,2-dichlorobenzene, and dichloromethane. For the devices in this work, we have used chloroform as the solvent to dissolve P3HT. However, it has

been shown in the literature that solvents can influence the crystallite morphology of P3HT [8, 9, 10]. For example, in reference [8], P3HT based OTFTs with both dichloromethane and chloroform solvents were compared. The OTFT with a dichloromethane solvent resulted in a higher field-effect mobility than the OTFT with a chloroform solvent. The result was explained by a better orientation and crystallinity of the P3HT in the dichloromethane. This indicates that organic solvents can influence the crystallinity of organic semiconductors, hence investigating various solvents can lead to a higher performing OTFTs.

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APPENDICES

Appendix A

Publications

1. **E.N. Tarekegn**, M. Seyedi, A. Tiara, I. Luzinov, and W.R. Harrell, "Enhancing the Performance of P3HT Based Organic Thin-Film Transistors with a Composite Interfacial Layer," in preparation.
2. **E.N. Tarekegn**, M. Seyedi, I. Luzinov, and W.R. Harrell, "Reducing the Threshold Voltage of Organic Thin-Film Transistors with a Copolymer Interfacial Layer," in preparation.
3. **E.N. Tarekegn**, M. Seyedi, I. Luzinov, and W.R. Harrell, "Poly(3-hexylthiophene)-based Organic Thin-Film Transistors with Virgin Graphene Oxide as an Interfacial Layer," *Polymers,* vol. 14, no. 23, 2022.
4. **E.N. Tarekegn**, M. Seyedi, I. Luzinov, and W.R. Harrell, "The Effect of a Copolymer Interfacial Layer on the Performance of Organic Thin-Film Transistors," *ECS Meeting Abstracts*, vol. MA2022-02, no.35, 2022.
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10. T. ElAli and **E. Tarekegn**, "A State Space Approach to Analog Computer Design & Simulation." *International Journal of Engineering and Management Research*, vol. 5, no. 5, pp. 299-303, Oct 2015.

Appendix B

Reticle Information and Stepper Program Setup

- GCA 5:1 reduction i-line stepper was used to perform 5x reduction photolithography steps.
- The reticle used in the stepper was made of quartz with dimensions of $5 \times 5 \times 0.09"$.
- The reticle had two parts as shown in Figure 7.1, which is also shown below for convenience:
    - The top half of the reticle had the pattern for the top metal contacts of the OTFTs and three alignment marks, i.e., global alignment, dark field alignment system (DFAS) and micro DFAS.
    - The bottom half of the reticle had the pattern for the channel of the OTFTs.
- The reticle field had a design of four devices, effectively printing four devices at one step.
- The patterns were made with chrome on the quartz reticle, which are shown as dark features in Figure 7.1 below.
- The dimensions of the patterns on the reticles were five times larger than the dimensions of the patterns ultimately printed on the wafer as the stepper was a 5x reduction stepper.
- A program (or job) was created in the stepper to perform the photolithography steps.

- The program had four parts:

  First part:

  - In this part of the program, the wafer diameter, step size and number of dies on the wafer are defined.
  - The exact location of the global alignment mark and the alignment dies on right and left edge of the wafer are also defined in this part of the program.

  Second part:

  - This part of the program gives instruction for exposing UV light through the top half of the reticle.
  - Expose time and focus offset are defined for the UV light exposure.
  - The dimension for covering the bottom half of the reticle using the blades are defined in this part of the program.

  Third part:

  - This part of the program gives instruction for exposing UV light through the bottom half of the reticle.
  - Expose time and focus offset are defined for the UV light exposure.
  - The dimension for covering the top half of the reticle using the blades are defined in this part of the program.

Fourth part:

- This part of the program is used to map the wafer using the alignment marks printed in the first exposure, before the second exposure is executed.
- This mapping stage ensures that the wafer during the second exposure is in the same location as it was during the first exposure.
- The exact location of the DFAS and micro DFAS alignment marks are defined in this part of the program.

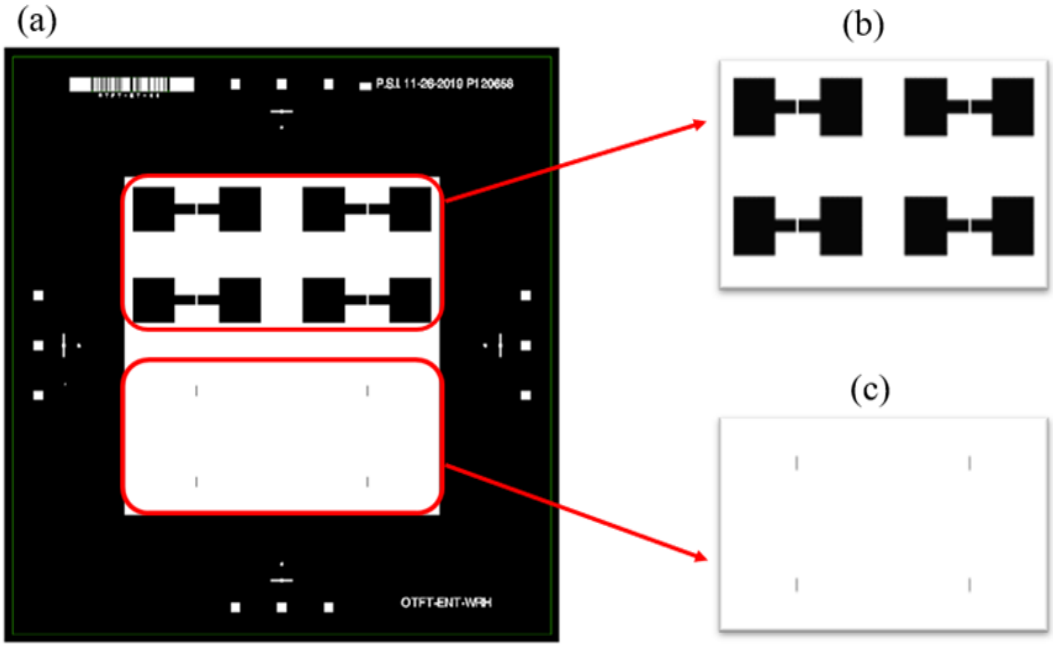

Figure 7.1. (a) Reticle pattern for the top metal contacts (source and drain) and the channel (P3HT), (b) close-up pattern for the top metal contacts, and (c) close-up patttern for the channel.

Appendix C

Fabrication Procedure for P3HT Based OTFTs

Gate Contact Deposition

[1] Rinse the wafer with methanol and dry with N_2 jet to remove coarse dusts from the wafer.

[2] Spin-coat the front side of the wafer with a positive photoresist, AZ 701.

a. Spin recipe

Table C1: Spin coating recipe for AZ 701

Step	Acceleration (rpm/sec)	Speed (rpm)	Time (sec)
1	2000	1000	5
2	2500	3000	45

b. AZ 701 thickness = 0.965 μm.

[3] Bake the photoresist on a hot plate at 95 ˚C for 90 seconds.

[4] Insert the wafer in a buffered oxide etch (5:1) solution for 5 minutes until the back surface of the wafer transformed from hydrophilic to hydrophobic

[5] Rinse the wafer with DI water several times in three different beakers to remove the buffered oxide etch

[6] Place the wafer in a Spin Rinse Dryer (SRD) tool to ensure the buffer oxide etch is completely removed from the wafer.

[7] Place the wafer in an Electron Beam Evaporator, CHA Mark 40, and deposit a 1 μm thick layer of aluminum.

[8] Remove the positive photoresist that was on the front side of the wafer by rinsing it with acetone.

Source/Drain Contact Deposition

[9] Rinse the wafer with methanol and dry with N_2 jet to remove coarse dusts from the wafer.

[10] Apply O_2 plasma for 20 seconds to remove impurities and contamination from the front surface of the wafer.

a. RF bias power = 25W

b. ICP power = 800W

[11] Spin-coat the wafer with a lift-off resist, LOR 3A.

a. Spin recipe

Table C2: Spin coating recipe for LOR 3A

Step	Acceleration (rpm/sec)	Speed (rpm)	Time (sec)
1	250	500	5
2	750	1500	30

b. Thickness of LOR 3A = 0.5 μm.

[12] Bake the LOR 3A on a hot plate at 175 ˚C for 5 minutes.

[13] Spin-coat a negative photoresist, AZ 5510, on top of the LOR 3A.

a. Spin recipe

Table C3: Spin coating recipe for AZ 5510

Step	Acceleration (rpm/sec)	Speed (rpm)	Time (sec)
1	5000	1000	2
2	2000	3000	45

b. AZ 5510 thickness = 0.9 μm.

[14] Bake the AZ 5510 on hot plate at 95 ˚C for 60 seconds.

[15] Expose the wafer to UV light through the top half of the reticle in a stepper, GCA 5:1 reduction i-line stepper.

a. Expose time = 0.3 seconds

b. Focus offset = 0.15 μm

[16] Bake the wafer on a hot plate at 110 ˚C for 60 seconds.

[17] Develop the wafer for 90 sec using AZ 300 MIF.

a. Spin recipe

Table C4: Spin developing recipe for AZ 300 MIF

Step	Acceleration (rpm/sec)	Speed (rpm)	Time (sec)	Dispense Di Water onto the backside of the wafer	Dispense Di water onto the frontside of the wafer	Dispense AZ 300 MIF onto the frontside of the wafer
1	1000	500	3	No	No	No
2	250	500	3	Yes	No	No
3	250	500	90	Yes	No	Yes
4	500	500	45	Yes	Yes	No
5	1000	2500	60	No	No	No

[18] Deposit 5 nm thick layer of chromium followed by a 250 nm thick layer of gold using an Electron beam evaporator.

a. The chromium is used as adhesion between the gold and SiO_2.

[19] Insert the wafer in ultrasonic NMP(1-Methyl-2-Pyrrolidinone) solution at 65 ˚C for a Cr/Au lift-off.

a. The lift-off should be done in 4 minutes.

[20] Rinse the wafer with fresh NMP, acetone, and methanol, while drying the wafer with N_2 jet after each solvent rinse.

Active Material Deposition

[21] Apply O_2 plasma for 20 seconds to ensure the wafer is clean before deposing the active material.

a. RF bias power = 25W

b. ICP power = 800W

[22] Spin-coat the wafer with P3HT.

a. Spin recipe

Table C5: Spin coating recipe for P3HT

Step	Acceleration (rpm/sec)	Speed (rpm)	Time (sec)
1	1000	2000	60

b. P3HT thickness = 58 nm

[23] Bake the P3HT on a hot plate at 110 ˚C for 1hr.

[24] Spin-coat the wafer with a positive photoresist, AZ 701, on top of the P3HT.

a. The spin coating recipe for the AZ 701 is the same as the recipe in Table C1, which given below again for convenience.

Table C1: Spin coating recipe for AZ 701

Step	Acceleration (rpm/sec)	Speed (rpm)	Time (sec)
1	2000	1000	5
2	2500	3000	45

b. Thickness of AZ 701 = 0.965 µm.

[25] Bake the photoresist on a hot plate at 95 ˚C for 60 seconds.

[26] Map the wafer in the stepper using the alignment marks printed in the first exposure.

[27] Expose the wafer to UV light through the bottom half of the reticle.

a. Expose time = 0.3 seconds

b. Focus offset = 0.15 µm

[28] Bake the wafer on a hot plate at 110 ˚C for 60 seconds.

[29] Develop the wafer for 45 seconds using AZ 300 MIF.

a. Spin recipe

Table C6: Spin developing recipe for AZ 300 MIF

Step	Acceleration (rpm/sec)	Speed (rpm)	Time (sec)	Dispense Di Water onto the backside of the wafer	Dispense Di water onto the frontside of the wafer	Dispense AZ 300 MIF onto the frontside of the wafer
1	1000	500	3	No	No	No
2	250	500	3	Yes	No	No
3	250	500	45	Yes	No	Yes
4	500	500	45	Yes	Yes	No
5	2500	4000	30	No	No	No
6	2500	6000	20	No	No	No

[30] Apply O_2 plasma for 30 seconds to etch the P3HT located outside of the channel areas.

a. RF bias power = 25W

b. ICP power = 800W

[31] Flood expose the wafer, without a mask, to UV light using a contact printer, Neutronix-Quintel 1x Aligner, for 24 seconds.

[32] Develop the wafer for 45 seconds using AZ 300 MIF.

a. The spin developing recipe for the AZ 300 MIF is the same as the recipe in Table C6, which is given below again for convenience.

Table C6: Spin developing recipe for AZ 300 MIF

Step	Acceleration (rpm/sec)	Speed (rpm)	Time (sec)	Dispense Di Water onto the backside of the wafer	Dispense Di water onto the frontside of the wafer	Dispense AZ 300 MIF onto the frontside of the wafer
1	1000	500	3	No	No	No
2	250	500	3	Yes	No	No
3	250	500	45	Yes	No	Yes
4	500	500	45	Yes	Yes	No
5	2500	4000	30	No	No	No
6	2500	6000	20	No	No	No

[33] Bake the wafer on a hot plate at 110 ˚C for 1hr.

[34] Bake/Anneal the wafer for an addition 2 hr at 110 ˚C in an oven with N_2 environment.

Appendix D

Fabrication Procedure for P3HT Based OTFTs with an Interfacial Layer

Gate Contact Deposition

[1] Rinse the wafer with methanol and dry with N_2 jet to remove coarse dusts from the wafer.

[2] Spin-coat the front side of the wafer with a positive photoresist, AZ 701.

a. The spin coating recipe for the AZ 701 is the same as the recipe in Table C1

b. AZ 701 thickness = 0.965 μm.

[3] Bake the photoresist on a hot plate at 95 ˚C for 90 seconds.

[4] Insert the wafer in a buffered oxide etch (5:1) solution for 5 minutes until the back surface of the wafer transformed from hydrophilic to hydrophobic

[5] Rinse the wafer with DI water several times in three different beakers to remove the buffered oxide etch

[6] Place the wafer in a Spin Rinse Dryer (SRD) tool to ensure the buffer oxide etch is completely removed from the wafer.

[7] Place the wafer in an Electron Beam Evaporator, CHA Mark 40, and deposit a 1 μm thick layer of aluminum.

[8] Remove the positive photoresist that was on the front side of the wafer by rinsing it with acetone.

Source/Drain Contact Deposition

[9] Rinse the wafer with methanol and dry with N_2 jet to remove coarse dusts from the wafer.

[10] Apply O_2 plasma for 20 seconds to remove impurities and contamination from the front surface of the wafer.

c. RF bias power = 25W

d. ICP power = 800W

[11] Spin-coat the wafer with a lift-off resist, LOR 3A.

a. The spin coating recipe for the LOR 3A is the same as the recipe in Table C2.

b. Thickness of LOR 3A = 0.5 μm.

[12] Bake the LOR 3A on a hot plate at 175 ˚C for 5 minutes.

[13] Spin-coat a negative photoresist, AZ 5510, on top of the LOR 3A.

c. The spin coating recipe for the AZ 5510 is the same as the recipe in Table C3

d. AZ 5510 thickness = 0.9 μm.

[14] Bake the AZ 5510 on hot plate at 95 ˚C for 60 seconds.

[15] Expose the wafer to UV light through the top half of the reticle in a stepper, GCA 5:1 reduction i-line stepper.

c. Expose time = 0.3 seconds

d. Focus offset = 0.15 μm

[16] Bake the wafer on a hot plate at 110 ˚C for 60 seconds.

[17] Develop the wafer for 90 seconds using AZ 300 MIF.

a. The spin developing recipe for the AZ 300 MIF is the same as the recipe in Table C4.

[18] Deposit 5 nm thick layer of chromium followed by a 250 nm thick layer of gold using an Electron beam evaporator.

a. The chromium is used as adhesion between the gold and SiO_2.

[19] Insert the wafer in ultrasonic NMP(1-Methyl-2-Pyrrolidinone) solution at 65 ˚C for a Cr/Au lift-off.

a. The lift-off should be done in 4 minutes.

[20] Rinse the wafer with fresh NMP, acetone, and methanol, while drying the wafer with N_2 jet after each solvent rinse.

Active Material Deposition

[21] Apply O_2 plasma for 20 seconds to ensure the wafer is clean before deposing the interfacial material.

a. RF bias power = 25W

b. ICP power = 800W

[22] Agitate the GO, POGL, or GO-POGL solutions in ultrasonic for 4 minutes.

[23] Spin-coat the wafer with GO, POGL, or GO-POGL.

a. Spin coating recipes

Table D1: Spin coating recipe for GO

Step	Acceleration (rpm/sec)	Speed (rpm)	Time (sec)
1	500	1000	60

Table D2: Spin coating recipe for POGL

Step	Acceleration (rpm/sec)	Speed (rpm)	Time (sec)
1	1000	2000	60

Table D1: Spin coating recipe for GO-POGL

Step	Acceleration (rpm/sec)	Speed (rpm)	Time (sec)
1	100	2000	60

[24] Bake the GO, GO-POGL, or POGL on a hot plate at 110 ˚C for 40 min.

[25] Spin-coat the wafer with P3HT on top of the interfacial layer.

a. The spin coating recipe for the P3HT is the same as the recipe in Table C5

b. P3HT thickness = 58 nm

[26] Bake the P3HT on a hot plate at 110 ˚C for 1hr.

[27] Spin-coat the wafer with a positive photoresist, AZ 701, on top of the P3HT.

a. The spin coating recipe for the AZ 701 is the same as the recipe in Table C1.

b. Thickness of AZ 701 = 0.965 µm.

[28] Bake the photoresist on a hot plate at 95 ˚C for 60 seconds.

[29] Map the wafer in the stepper using the alignment marks printed in the first exposure.

[30] Expose the wafer to UV light through the bottom half of the reticle.

c. Expose time = 0.3 seconds

d. Focus offset = 0.15 µm

[31] Bake the wafer on a hot plate at 110 ˚C for 60 seconds.

[32] Develop the wafer for 45 seconds using AZ 300 MIF.

a. The spin developing recipe for the AZ 300 MIF is the same as the recipe in Table C6.

[35] Apply O_2 plasma for 30 seconds to etch the P3HT located outside of the channel areas.

a. RF bias power = 25W

b. ICP power = 800W

[33] Flood expose the wafer, without a mask, to UV light using a contact printer, Neutronix-Quintel 1x Aligner, for 24 seconds.

[34] Develop the wafer for 45 seconds using AZ 300 MIF

a. The spin developing recipe for the AZ 300 MIF is the same as the recipe in Table C6.

[35] Bake the wafer on a hot plate at 110 ˚C for 1hr.

[36] Bake/Anneal the wafer for an addition 2 hr at 110 ˚C in an oven with N_2 environment.

Appendix E

Electrical Measurements

- HP-4156B Semiconductor Parameter Analyzer was used for electrically characterizing the OTFTs.
- The HP-4156B was connected to a micromanipulator probe station using three triaxial cables. A picture of the probe station is shown in Figure E1. The prob station has two main components: chuck and micromanipulator probes.
- The chuck is where a wafer is placed, it is made of an electric conductive material with vacuum holes on it to hold the wafer steady. The chuck is shown in Figure E1.
- The micromanipulator probes are used to make electrical contact to the electrodes of the OTFTs. In Figure E1, we show four probes on either side of the chuck. The tips for each of these probes are made of gold.
- For our measurements, we used three of the probes only.
    - The first two probes were connected to the source and drain contacts: one probe tip lands on each contact.
    - The third probe was connected to the chuck. Since the chuck is conductive, there will be a direct electric connection between the probe tip and the gate contact, which is the backside of the wafer
- The other ends of the probes were connected to the triaxial cable, which were connected to the SMU terminals of the HP-4156B.

- The SMU terminals were assigned appropriate channels based on their respective probe connection to the OTFT electrodes.
- For the drain current vs. drain voltage ($I_{DS} - V_{DS}$) measurements, 0 V to -70 V was applied at the drain terminal with an increment of -0.5 V while biasing the gate terminal with voltages ranging from 0 V to -60 V with an increment of -20 V.
    - The source terminal was grounded throughout this measurement.
- For the drain current vs. gate voltage ($I_{ds} - V_{gs}$) measurements, 0 V to -60 V was applied voltage at the gate terminal with an increment of -0.5 V while biasing the drain at -5 V.
    - The source terminal was grounded throughout this measurement.

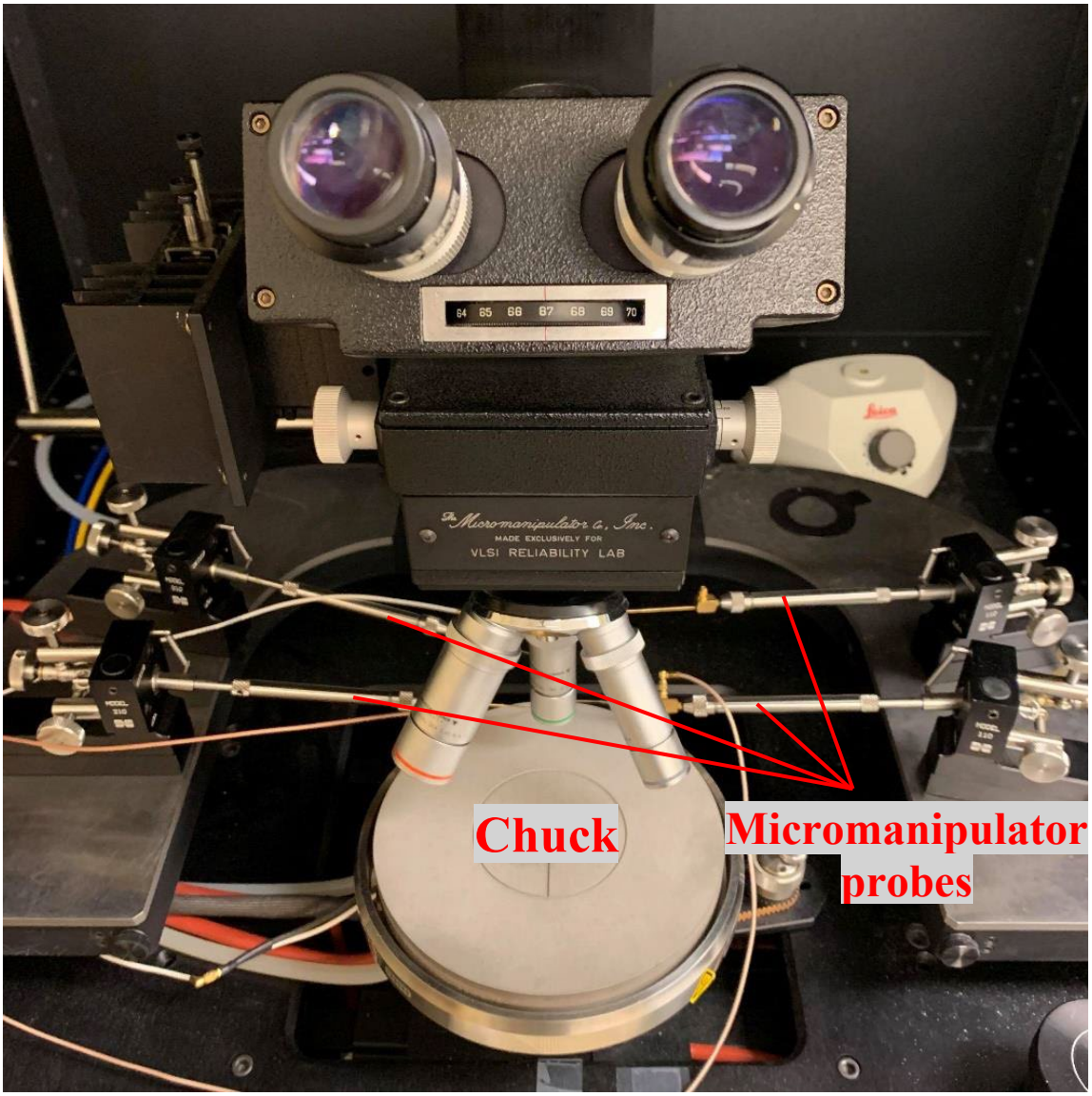

Figure C1: Micromanipulator probe station