An Analog Pixel Front-End for High Granularity Space-Time Measurements

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PhD Thesis Summary

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An important aspect to consider is that the front-end channel is part of a large multichannel system. This aspect influences the single channel design by imposing constrains arising from the pixel-matrix configuration. The channel must fit inside a limited pixel-area, while leaving room for the implementation of the other pixel dedicated circuits. The area limitation will also constraint the total power budget available to the analog front-end. Moreover, a certain degree of uniformity is required across the pixel matrix. These challenges have been addressed with novel architectural solutions. First, a new very first-end scheme as been designed in order to reduce the time fluctuations within the available power budget. Second, a discrete time technique has been implemented in order to equalize the channels while limiting the area and power consumption needed for this task.

The author's work was not only limited to the core channel. Given the system-like nature of the project, design and test work was also carried out on a system level. The author is one of the three lead designers of the ASIC. Therefore, a crucial role has been covered in the definition of the pixels and matrix architectures and floor-plans. The main contribution was the integration of the full analog part of the pixel-matrix, including all the service and configuration blocks used to operate it. As a result, the whole pixel matrix can be operated by providing only one reference signal configured via a digital interface.

The main application for this type of ASIC is in future experiments in High Energy Physics (HEP). In this field, particles properties and trajectories are reconstructed by large detectors composed of many sensitive layers. The information gathered on the innermost layers is used to reconstruct the particle track in the process named tracking. This process is based on the particle hits positions and is used to date. However, HEP experiments such as the ones in Conseil Européen pour la Recherche Nucléaire (CERN), are planning to increase their accelerator nominal luminosity. In case of the Large Hadron Collider (LHC), this upgraded is scheduled din 2029. The luminosity boost will increase the chance of observing rare events by increasing the event rate. The downside of this approach is that the number of spurious events is also expected to rise, making current tracking techniques ineffective. This issue can be solved by adding a

time measurement capability to the inner layers of the detector achieving what is called 4D-tracking. In principle, future detectors require a time resolution of at least 100 ps at the level of pixels tens of micrometers large. 4D-tracking demands therefore the research and development of new pixel-front ASICs with timing measurement capability.

The construction of this type of detectors is beyond the sole scope of ASIC level design. In fact, in order to reach the required space-time resolution, the whole system must be tailored around this goal. The TimeSPOT project (Time and SPace real-time Operating Tracker) by the Italian institute for nuclear physics (Istituto Nazioanle di Fisica Nucleare INFN) aims to research and develop a demonstrator detector suitable for high-luminosity HEP experiments. The demonstrator will be realized via a small-scale telescope that will include the pixel sensor matrix, the pixel front-end ASIC, and the readout electronics. The work presented in this thesis is actually part of the development of the Timespot ASIC family. The ASIC is researched in tandem with its sensor and readout in order to achieve the target specifications in terms of: space-time resolution, maximum event rate, data throughput, power consumption and radiation tolerance. The project time resolution specification has been defined on the basis of what is achieved by its sensor: 20 ps or better.

The 28 nm CMOS technology node was chosen over more conventional nodes for the field due to its superior jitter performance over power consumption. It also opens up the possibility to integrate more features in the same silicon area. The radiation hardness of this node is on par with the best results achieved in 65 nm and 130 nm nodes. The complexity of this technology has determined an additional challenge in terms of ASIC design.

Other applications for this ASIC can be found in other fields that require a granular space-time measurement such as: detector for space application, medical equipments and in general detector for imaging applications.