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An Interleaved High Step-Up DC-DC Converter with Built-in Transformer-Based Voltage Multiplier for DC Microgrid Applications

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***Abstract*—This paper proposes a high step-up DC-DC converter with a built-in transformer (BIT)-based voltage multiplier (VM) that is suitable for integrating low-voltage renewable energy sources into a DC microgrid. A three-winding BIT is combined with the switched-capacitor (SC) cells to extend the voltage gain and reduce the voltage stress on the switches. The current-falling rates of the diodes are controlled by the leakage inductances of the BIT, alleviating the reverse-recovery problem of the diodes. The operating modes and steady-state analysis are presented. Additionally, the validity of the proposed converter is confirmed by the simulation and experimental results of a 400 W converter with an input voltage of 20 V and output voltage of 400 V. Moreover, a comparison study is presented to verify the superiority of the proposed converter over the closest existing topologies in the literature.**

Keywords—Interleaved high step-up DC-DC converter, high-voltage gain, switched-capacitor (SC) cell, voltage multiplier (VM), renewable energy, DC microgrid, photovoltaic (PV), fuel cell (FC).

I. INTRODUCTION

Recently, the integration of renewable energy sources (RESs) into the DC microgrids has significantly increased. Photovoltaic (PV) and fuel cells are among the RESs [1-4]; however, their output voltage (e.g., 20 V) is much lower than the DC voltage (e.g., 400 V) required by the microgrid' DC bus. Thus, a DC-DC converter is required to step up the voltage of the RESs and draw a continuous input current with a small ripple. Operating at extremely high duty cycles, the conventional non-interleaved and interleaved DC-DC boost converters can theoretically achieve a high voltage gain; however, their practical voltage gain is limited due to the parasitic elements of components, also they suffer from the high voltage stresses on the semiconductors, severe reverse-recovery problem of the output diode, and low efficiency [5]. To overcome these issues, many high step-up DC-DC converters have been introduced in the literature, which are based on the integration of the voltage multipliers (VMs) with conventional boost converters [6]. The high step-up DC-DC converters in [7-9] have employed the VMs based on the switched-capacitor (SC) cells. They offer high voltage gains and low voltage stresses on the semiconductors without extremely high duty cycles; however, due to the direct energy exchange among the capacitors, they suffer from high transient currents on the circuit. Additionally, many diodes and capacitors are used to extend the voltage gain, which deteriorates the converter efficiency. To solve these problems and further increase the voltage gain with reduced voltage stresses on the semiconductors, an interesting alternative is to combine the SC-based VMs with the coupled inductor (CI) or built-in transformer (BIT) [10]. Using either CI or BIT, another degree of freedom is added to adjust the voltage gain; that is, the voltage gain can be adjusted with two parameters that are the duty cycle of the switches and turns-ratio of CI or BIT. In addition, due to the presence of the leakage inductances, the current-falling rates of diodes are controlled, which leads to the alleviation of diodes' reverse-recovery problems. Also, the energy of the leakage inductances is passed into the load side through the VM, causing a further increase in the voltage gain [11]. The high step-up DC-DC converters in [12-16] are based on the VMs consisting the CI and SC cells, and the converters in [17-20] were developed using the VMs based on the BIT and SC cells. The advantage of the BIT over the CI is that the core saturation is avoided in the BIT because the average currents of all the windings of the BIT are zero, leading to the inherent balanced operation of the flux density in the magnetic core [21]; thus, the BIT can be designed with low flux density, meaning that its core magnetic cross section and volume can be reduced, and the converter power density can be increased [22].

In this paper, an interleaved high step-up DC-DC converter using a VM stage comprising of SC cells and a three-winding BIT is proposed, which is suitable for the DC microgrids powered by the RESs. The proposed converter has an interleaved structure in input side, causing reduction in the input current ripple and current stresses of the components. Combining the BIT with SC cells in the MV stage, a high-voltage gain and a low voltage stress on the semiconductors are obtained. Two diode-capacitor pairs of the MV stage play the roles of passive lossless clamps to absorb the energy stored in the leakage inductances of the BIT and to limit the voltage stresses on the switches. The operating modes, steady-state analysis in continuous conduction mode (CCM), deign considerations of the magnetic components, simulation and experimental results, and a comparison with the closest exiting topologies in the literature are discussed in the rest of this paper.

II. PROPOSED TOPOLOGY AND OPERATING MODES

The topology of the proposed high step-up DC-DC converter is shown in Fig. 1. It consists of three stages located between input source V_{in} and output load R, which are input interleaved stage, voltage multiplier stage, and output filter stage. In the

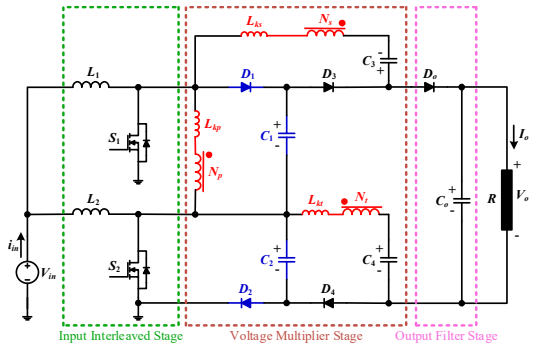

Fig. 1. The proposed interleaved high step-up DC-DC converter.

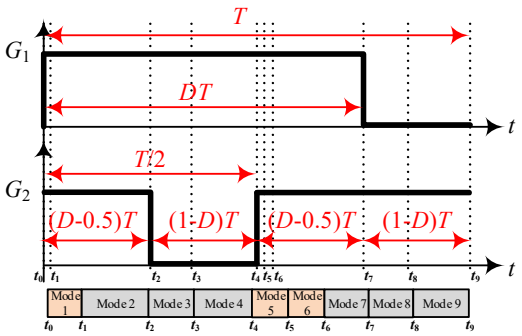

Fig. 2. The gate signals and operating modes of the proposed converter.

input interleaved stage, there are two boost inductors (L_1 and L_2) and two switches (S_1 and S_2); switches S_1 and S_2 are commanded with two gate signals that have the same duty cycle (D) and are 180° out of phase from each other. The voltage multiplier stage is composed of a three-winding BIT, four diodes D_1-D_4, and four capacitors C_1-C_4. Parameters N_p, N_s, and N_t represent the number of turns of the primary, secondary, and tertiary windings of the BIT; also, the primary, secondary, and tertiary leakage inductances of the BIT are denoted by L_{kp}, L_{ks}, and L_{kt}, respectively. In addition to contributing to the voltage gain extension, the diode-capacitor pairs (D_1 and C_1) and (D_2 and C_2) play the roles of passive lossless clamps to absorb the energy stored in the leakage inductances and to limit the voltage stress on the switches S_1 and S_2. The output filter stage is formed by the output diode (D_o) and capacitor (C_o). For the converter to operate normally, at least one of switches S_1 and S_2 is required to be ON at any point in time, which is achieved by a duty cycle greater than 0.5 for the switches. The gating signals are illustrated in Fig. 2, leading to 9 operating modes during a switching period (T) in the CCM. Figs. 3(a)-(i) show the equivalent circuits of the proposed converter for all operating modes, which are explained as follows:

Mode 1 (Fig. 3(a)): At $t=t_0$, switch S_1 turns on and switch S_2 and diode D_o retain their ON states from the previous mode that is Mode 9. The current-falling rate of output diode D_o is controlled by the leakage inductances of the BIT, reducing the reverse-recovery problem of D_o. All diodes D_1, D_2, D_3, and D_4 are reverse-biased, and inductors L_1 and L_2 are energized by input voltage V_{in}.

Mode 2 (Fig. 3(b)): This mode begins when output diode D_o turns off at $t=t_1$. Both switches S_1 and S_2 are in ON state, and the boost inductors L_1 and L_2 continue to be energized by V_{in}. The load is supplied by capacitor C_o.

Mode 3 (Fig. 3(c)): As shown in Fig. 3(c), this mode begins when switch S_2 turns off and diodes D_2, D_3, and D_4 turn on. Inductor L_2 is de-energized by the voltage of the primary winding of the BIT plus V_{in}. Capacitors C_3 and C_4 are charged by the secondary and tertiary windings of the BIT, respectively; capacitor C_1 is discharged, and capacitor C_2 is charged by the current of inductor L_2 and the voltage of switch S_2 is clamped to V_{C2}. This mode ends when diode D_2 turns off smoothly under zero-current switching (ZCS) condition; thus, there is no reverse-recovery problem for diode D_2.

Mode 4 (Fig. 3(d)): At $t=t_3$, diode D_2 turns off and the other semiconductors maintain their states from the previous mode; capacitor C_o continues to supply the load, and inductors L_1 and L_2 continue to be energized and de-energized, respectively.

Mode 5 (Fig. 3(e)): At $t=t_4$, switch S_2 turns on. As obvious from Fig. 3(e), capacitors C_1, C_2, and C_o are discharged, while inductors L_1 and L_2 are energized and capacitors C_3 and C_4 are charged. The current of diode D_3 starts to decrease and its falling rate is controlled by the leakage inductances of the BIT, which reduces the reverse-recovery problem of D_3. This mode ends when diode D_3 turns off.

Mode 6 (Fig. 3(f)): At $t=t_5$, diode D_3 turns off and the current of diode D_4 starts to decrease; the BIT's leakage inductances control the current-falling rate of D_4, thus resulting in the reduction of its reverse-recovery problem.

Mode 7 (Fig. 3(g)): This mode is the same as Mode 2.

Mode 8 (Fig. 3(h)): At the beginning of this mode, switch S_1 turns off and its voltage is clamped to V_{C1} through diode D_1; inductor L_1 starts to be de-energized; also, output diode D_o turns on to transfer the energy to the output side, thus charging output capacitor C_o and supplying load R.

Mode 9 (Fig. 3(i)): At t=t_8, the current through capacitor C_1 decreases to zero and diode D_1 turns off naturally with ZCS condition, resulting in no reverse-recovery problem for D_1. This mode continues until the end of switching period T.

III. Converter Steady-State Performance Analysis

To simplify the steady-state analysis of the proposed converter, the leakage inductances of the BIT are ignored; thus, the transitional Modes 1, 5 and, 6 are ignored. Also, the voltages of all the capacitors are supposed to be constant during the whole switching period. Given the above assumptions, Modes 3 and 4 are assumed to be the same and Modes 8 and 9 are the same. Also, the turns-ratio of the BIT is defined as $N=N_s/N_p=N_t/N_p$.

A. Voltage Gain

Applying the volt-second balance principle to boost inductors L_1 and L_2, the voltages on capacitors C_1 and C_2 are obtained as:

$$V_{C_1} = V_{C_2} = \frac{1}{1-D} V_{in} \tag{1}$$

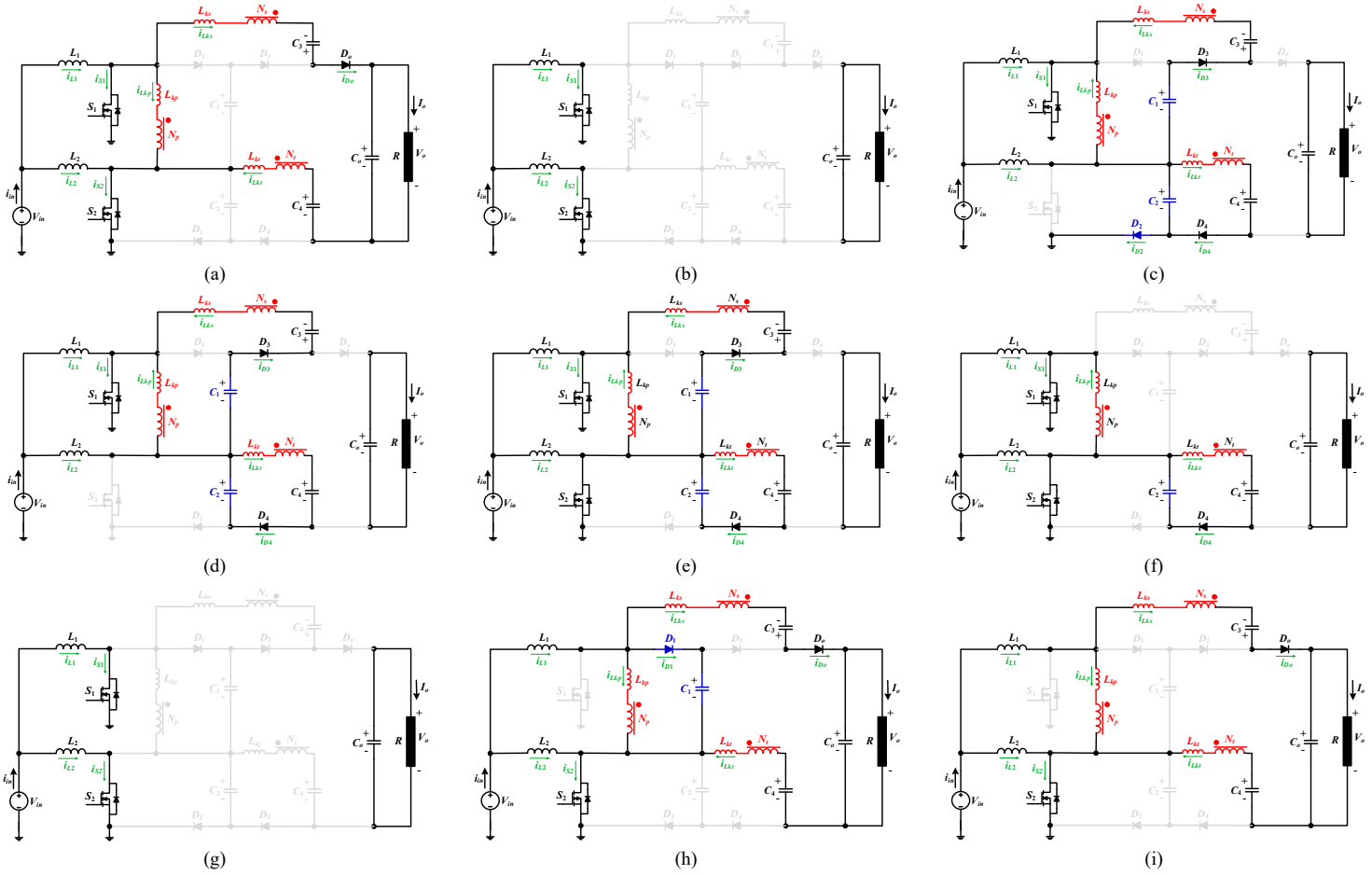

Fig. 3. The operating modes of the proposed converter: (a) Mode 1, (b) Mode 2, (c) Modes 3, (d) Mode 4, (e) Mode 5, (f) Mode 6, (g) Mode 7, (h) Mode 8, (i) Mode 9.

Considering Mode 3 in Fig. 3(c), the voltage on the primary winding of the BIT (V_{Np}) is -V_{C2}; thus, the voltages on capacitors C_3 and C_4 are obtained as:

$$V_{C_3} = -(N+1)V_{N_p} + V_{C_1} = \frac{N+2}{1-D}V_{in}$$
$$V_{C_4} = -(N+1)V_{N_p} = \frac{N+1}{1-D}V_{in} \quad (2)$$

According to the equivalent circuit of the proposed converter in Mode 8, shown in Fig. 3(h), V_{Np}=V_{C1} and the voltage on the output capacitor is extracted as:

$$V_{C_o} = V_o = (2N+1)V_{N_p} + V_{C_3} + V_{C_4} = \frac{4N+4}{1-D}V_{in} \quad (3)$$

From (3), the voltage gain of the proposed converter is obtained as:

$$M = \frac{V_o}{V_{in}} = \frac{4N+4}{1-D} \quad (4)$$

It is concluded from (4) that the voltage gain of the proposed converter can be adjusted by two independent parameters of N and D, which increases the design flexibility of the proposed converter. Fig. 4 shows the voltage gain curves versus the duty cycle for different values of turns-ratio. As obvious, the proposed converter achieves high voltage gains without operating under extremely high duty cycles.

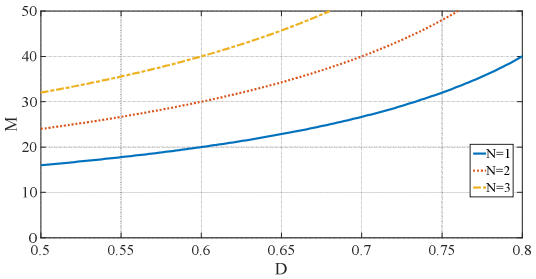

Fig. 4. The voltage gain of the proposed converter.

B. Voltage and Average Current Stresses Analysis

The voltage stresses on the switches and diodes are given by:

$$V_{S_1} = V_{S_2} = V_{D_2} = \frac{1}{4N+4}V_o$$
$$V_{D_1} = \frac{1}{2N+2}V_o; \qquad V_{D_3} = \frac{1}{2}V_o \quad (5)$$
$$V_{D_4} = \frac{N}{2N+2}V_o; \qquad V_{D_o} = \frac{2N+1}{2N+2}V_o$$

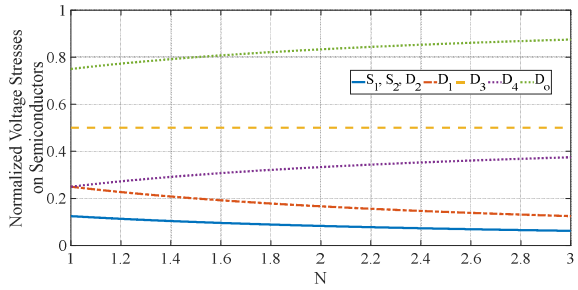

Fig. 5. The normalized voltage stresses of the semiconductors for the proposed converter.

Fig. 5 illustrates the normalized voltage stresses of the semiconductors, which are normalized to the output voltage. As seen, the normalized voltage stresses on the switches are far lower than 1. In other words, the voltage stresses on the switches are far less than the output voltage. Also, the voltages stresses on the diodes are lower than the output voltage, thus enabling the adoption of low-voltage-rated MOSFETs and diodes with low ON-state resistances, which improves the efficiency of the proposed converter.

Ignoring the power losses of the proposed converter, the average input current as well as the average currents of the leakage inductances L_{kp}, L_{ks}, and L_{kt} and boost inductances L_1 and L_2 are ideally calculated as:

$$\begin{aligned} I_{in} &= MI_o = \frac{4N+4}{1-D} I_o \\ I_{L_{kp}} &= I_{L_{ks}} = I_{L_{kt}} = 0 \\ I_{L_1} &= I_{L_1} = \frac{2N+2}{1-D} I_o \end{aligned} \tag{6}$$

The average currents of the semiconductors are obtained as:

$$\begin{aligned} I_{S_1} &= I_{L_1} - I_o = \frac{2N+1+D}{1-D} I_o \\ I_{S_2} &= I_{L_2} = \frac{2N+2}{1-D} I_o \\ I_{D_1} &= I_{D_2} = I_{D_3} = I_{D_4} = I_{D_o} = I_o \end{aligned} \tag{7}$$

IV. Design Considerations of Magnetic Components

A. Boost Inductors Design

Considering maximum x% current ripple, the boost inductances L_1 and L_2 are calculated as:

$$\begin{aligned} \Delta i_{L_{\max}} &= \frac{x}{100} I_{L1} = \frac{x(N+1)}{50(1-D)} I_o \\ L_1 = L_2 = L &\geq \frac{V_{in} D}{\Delta i_{L_{\max}} f_{sw}} \rightarrow L \geq \frac{50D(1-D)V_{in}}{x f_{sw}(N+1) I_o} \end{aligned} \tag{8}$$

B. BIT Design

1) *Limitation of Turns-Ratio*

The duty cycle of the switches is greater than 0.5, leading to the limitation on the BIT's turns-ratio as:

$$D = 1 - \frac{4(N+1)}{M} \geq 0.5 \rightarrow N \leq \frac{M}{8} - 1 \tag{9}$$

2) *Number of Turns of BIT's Windings*

Having the flux density variation (ΔB_{BIT}) and cross-sectional area of the core ($A_{c,\mathrm{BIT}}$) for the BIT, and considering Modes 3 and 4, the numbers of turns for the windings of the BIT are obtained as:

$$\begin{aligned} V_{Np} &= \frac{\Delta \lambda_{BIT}}{\Delta t} = \frac{N \Delta \phi}{t_4 - t_2} = \frac{N_p \Delta B_{BIT} A_{c,BIT}}{(1-D)T} \\ \rightarrow N_p &= \frac{V_{in} D}{(1-D) \Delta B_{BIT} A_{c,BIT} f_{sw}} \\ N_s &= N_t = N \times N_p \end{aligned} \tag{10}$$

V. Simulation and Experimental Results

In order to confirm the performance of the proposed converter, a 400 W converter was simulated in PLECS Blockset; also, an experimental prototype was developed. The specifications of the converter are listed in Table I. The simulation and experimental results for V_{in}=20 V, D=0.6, and N=1 are presented in Figs. 6 and 7, respectively. From (4), the ideal voltage gain is calculated as 20, which gives an output voltage of 400 V that is relatively verified by both the simulation and experiment depicted in Figs. 6(a) and 7(b), respectively. Also, both simulated and experimentally measured voltages of the capacitors C_1-C_4 are close enough to the calculated values from that are as V_{C1}=V_{C2}=50 V, V_{C3}=150 V, V_{C4}=100 V. Figs. 6(b) and 7(c) show the simulated and experimentally measured currents of boost inductors L_1 and L_2 and input current. Currents i_{L1} and i_{L2} are 180° out of phase from each other with the average value of about 10 A, which validates the interleaved behavior of the proposed converter; also, as seen, the input current is continuous with small ripple, which is beneficial for the renewable energy applications in the DC micro grids. Moreover, according to Figs. 6(c) and 7(d), the voltage stress on switches S_1 and S_2 is about 50 V, which is far less than the output voltage of 400 V. In addition, the voltage stresses on the diodes are as V_{D1}= V_{D4}=100 V V_{D2}=50 V, V_{D3}=200 V, and V_{Do}= 300 V.

TABLE I. Converter Specifications

Parameter	Value
Input voltage V_{in}	20 V
Duty cycle D	0.6
Load resistance R	400 Ω
Switching frequency	100 kHz
Inductances L_1 and L_2	270 µH
Leakage inductances L_{kp}, L_{ks}, and L_{kt}	1 µH
Capacitors C_1 and C_2	50 µF
Capacitors C_3, C_4, and C_o	20 µF

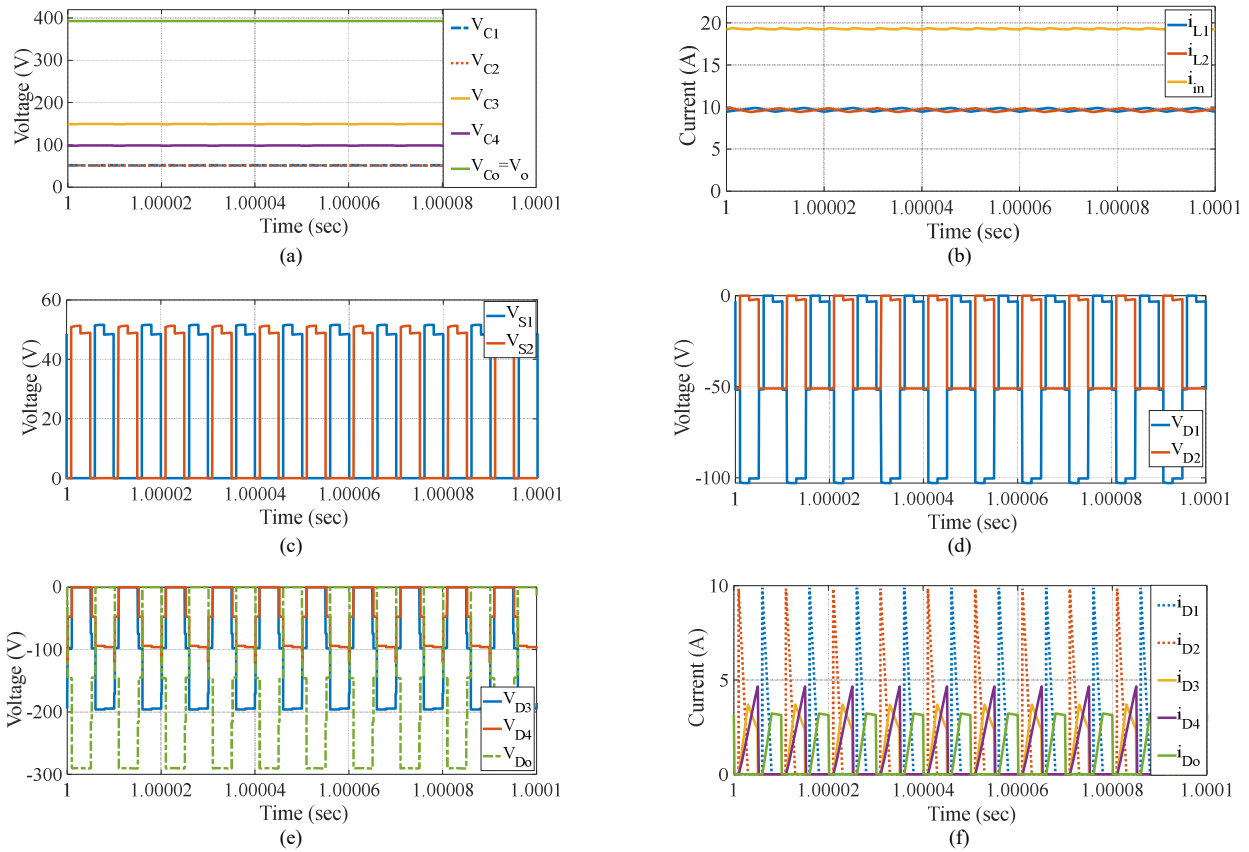

Fig. 6. Simulation results of the proposed converter for V_{in}=20 V, D=0.6, and N=1.

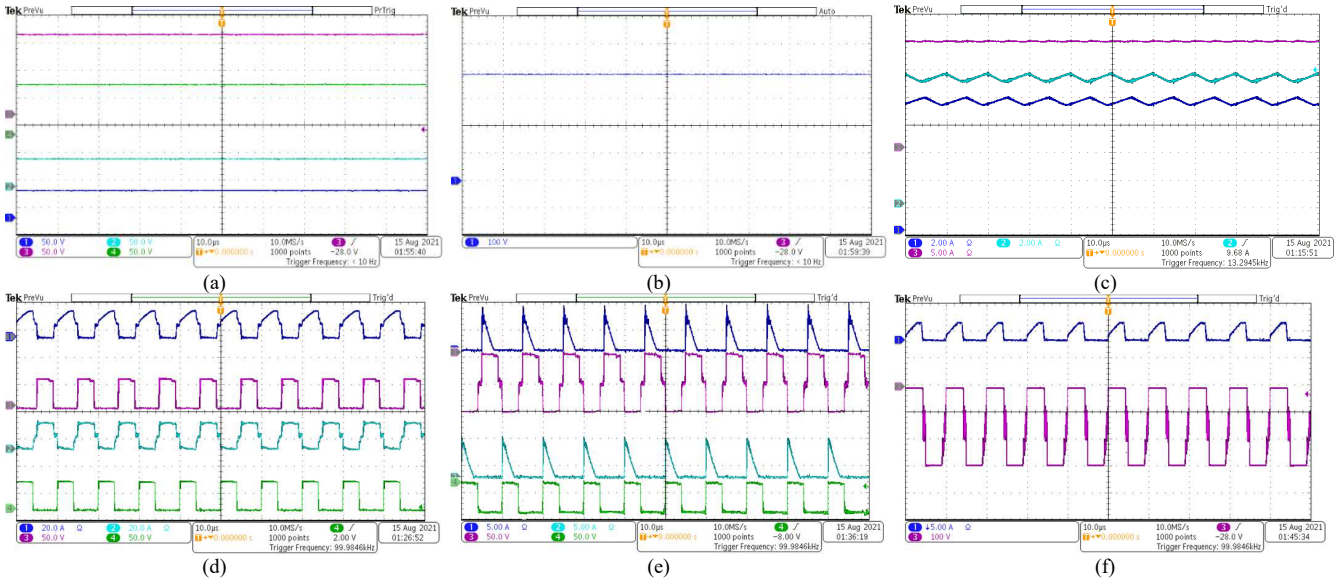

Fig. 7. Experimental results of the proposed converter for V_{in}=20 V, D=0.6, and N=1: (a) voltages of capacitors C_1 (CH1), C_2 (CH2), C_3 (CH3), and C_4 (CH4); (b) output voltage; (c) currents of boost inductances L_1 (CH1) and L_2 (CH2) and input current (CH3); (d) currents of switches S_1 (CH1) and S_2 (CH2) as well as voltages of switches S_1 (CH3) and S_2 (CH4); (e) currents of diodes D_1 (CH1) and D_2 (CH2) as well as voltages of diodes D_1 (CH3) and D_2 (CH4); (f) current of diode D_o (CH1) and voltage of diode D_o (CH3).

Therefore, the simulation and experimental results are consistent with each other and are in good agreement with the theoretical calculations, which verify the performance of the proposed converter.

TABLE II. PERFORMANCE COMPARISON WITH THE CLOSEST EXISTING LITERATURE

Converter	Number of components					Normalized voltage stress on switches	Normalized voltage stress on output diode	Voltage gain
	Switches	Diodes	Capacitors	Windings	Cores			
[17]	2	4	6	6	4	$\frac{1}{2N+D+1}$	$\frac{N+1}{2N+D+1}$	$\frac{2N+D+1}{1-D}$
[18]	4	2	4	4	2	$\frac{1}{2N+4}$	$\frac{N+1}{N+2}$	$\frac{2N+4}{1-D}$
[19]	4	4	5	5	2	$\frac{1}{2N+2}$	1	$\frac{2N+2}{1-D}$
[20]	2	4	3	5	2	$\frac{1}{N+2}$	1	$\frac{N+2}{1-D}$
Proposed	2	5	5	5	2	$\frac{1}{4N+4}$	$\frac{2N+1}{2N+2}$	$\frac{4N+4}{1-D}$

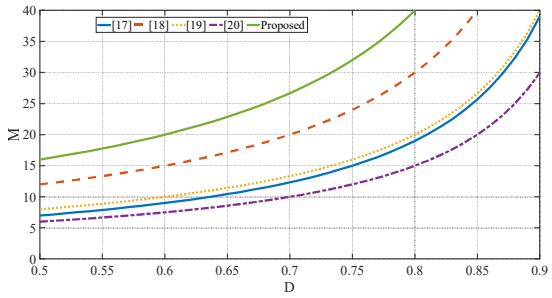

Fig. 8. Voltage gain comparison.

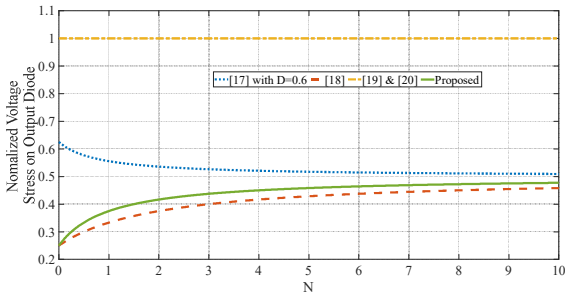

Fig. 9. Comparison of normalized voltage stresses on the switches.

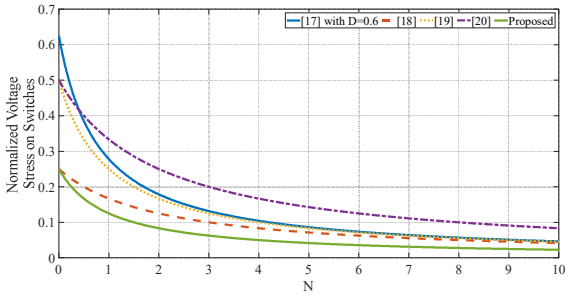

Fig. 10. Comparison of normalized voltage stresses on the output diode.

VI. PERFORMANCE COMPARISON

To verify the superiority of the proposed converter over the closest existing works in the literature, a comparison is carried out in Table II. High-voltage gains are obtained using the BIT and SC cells in all the converters listed in the comparison table. The proposed converter and converters in [18-20] have two magnetic cores, while the converter in [17] has four magnetic cores. There are two MOSFETs in the proposed converter and those in [17, 20], but the converters in [18, 19] have four MOSFETs. Fig. 8 shows the voltage gains of the converters versus the duty cycle for N=1; as obvious, the proposed converter offers the highest voltage gain. Fig. 9 illustrates the normalized voltage stresses on the switches for the converters; as seen, the proposed converter has the lowest voltage stress on the MOSFETs. Regarding the normalized voltage stress on the output diode, as shown in Fig. 10, for the converters in [19, 20], the output diode's normalized voltage stress is equal to 1, which means that the voltage stress across the output diode equals the output voltage; however, for the proposed converter and those in [17, 18], the normalized voltage stress on the output diode is lower than 1 for all values of the BIT's turns-ratio.

VII. CONCLUSIN

In this paper, a high step-up DC-DC converter was proposed, which is based on the interleaved structure with BIT and VMCs. The interleaved feature leads to the reduced input current ripple and low current stresses on the components, and the BIT along with the SC-based VM cells provides the proposed converter with high voltage gain with medium duty cycles. The proposed converter is superior to the closest topologies in the literature. The key features of the proposed converter are high voltage gain, low voltage stresses on the semiconductors, and alleviations of the severe reverse-recovery problem of the diodes. A 400 W converter was simulated and experimentally implemented to verity the performance of the proposed converter

REFERENCES

[1] Y. Hsieh, J. Chen, T. Liang and L. Yang, "A Novel High Step-Up DC–DC Converter for a Microgrid System," in *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1127-1136, April 2011.

[2] R. Rahimi, S. Habibi, P. Shamsi and M. Ferdowsi, "A High Step-Up Z-Source DC-DC Converter for Integration of Photovoltaic Panels into DC Microgrid," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1416-1420, 2021.

[3] R. Rahimi, S. Habibi, P. Shamsi and M. Ferdowsi, "A Dual-Switch Coupled Inductor-Based High Step- Up DC-DC Converter for Photovoltaic-Based Renewable Energy Applications," 2021 IEEE Texas Power and Energy Conference (TPEC), pp. 1-6, 2021.

[4] R. Rahimi, S. Habibi, M. Ferdowsi and P. Shamsi, "A Two-Phase Interleaved High-Voltage Gain DC-DC Converter with Coupled Inductor and Built-in Transformer for Photovoltaic Applications," IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society, pp. 1-6, 2021.

[5] F. L. Tofoli, D. d. C. Pereira, W. Josias de Paula and D. d. S. Oliveira Júnior, "Survey on non-isolated high-voltage step-up dc–dc topologies based on the boost converter, " IET Power Electronics, vol. 8, no. 10, pp. 2044-2057, Sep. 2015.

[6] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg and B. Lehman, "Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications," in *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9143-9178, Dec. 2017.

[7] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli and R. Gules, "Voltage Multiplier Cells Applied to Non-Isolated DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 871-887, March 2008.

[8] R. Rahimi, S. Habibi, M. Ferdowsi and P. Shamsi, "Z-Source-Based High Step-Up DC-DC Converters for Photovoltaic Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, pp. 1-14, 2021.

[9] B. P. Baddipadiga and M. Ferdowsi, "A high-voltage-gain DC–DC converter based on modified Dickson charge pump voltage multiplier," IEEE Trans. Power Electron., vol. 32, no. 10, pp. 7707–7715, Oct. 2017.

[10] R. Rahimi, S. Habibi, P. Shamsi and M. Ferdowsi, "An Interleaved High Step-Up DC-DC Converter Based on Combination of Coupled Inductor and Built-in Transformer for Photovoltaic-Grid Electric Vehicle DC Fast Charging Systems," *2021 IEEE Texas Power and Energy Conference (TPEC)*, pp. 1-6, 2021.

[11] R. Rahimi, S. Habibi, M. Ferdowsi and P. Shamsi, "A Three-Winding Coupled Inductor-Based Interleaved High-Voltage Gain DC–DC Converter for Photovoltaic Systems," in *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 990-1002, 2022.

[12] M. Y. Hassani, M. Maalandish and S. H. Hosseini, "A New Single-Input Multioutput Interleaved High Step-Up DC–DC Converter for Sustainable Energy Applications," in *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1544-1552, Feb. 2021.

[13] S. -W. Seo, J. -H. Ryu, Y. Kim and J. -B. Lee, "Ultra-High Step-Up Interleaved Converter With Low Voltage Stress," in *IEEE Access*, vol. 9, pp. 37167-37178, 2021.

[14] K. R. Kothapalli, M. R. Ramteke, H. M. Suryawanshi, N. K. Reddi and R. B. Kalahasthi, "A Coupled Inductor Based High Step-Up Converter for DC Microgrid Applications," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 6, pp. 4927-4940, June 2021.

[15] K. Zaoskoufis and E. C. Tatakis, "An Improved Boost-Based dc/dc Converter With High-Voltage Step-Up Ratio for DC Microgrids," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 2, pp. 1837-1853, April 2021.

[16] S. Habibi, R. Rahimi, M. Ferdowsi and P. Shamsi, "A Coupled Inductor-Based Dual-Switch High Step-up DC-DC Converter with Common Ground," IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society, pp. 1-6, 2021.

[17] M. F. Guepfrih, G. Waltrich and T. B. Lazzarin, "High Step-Up Dc-Dc Converter Using Built-in Transformer Voltage Multiplier Cell and Dual Boost Concepts," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*.

[18] T. Nouri, N. Vosoughi Kurdkandi and M. Shaneh, "A Novel ZVS High-Step-Up Converter With Built-In Transformer Voltage Multiplier Cell," in *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 12871-12886, Dec. 2020.

[19] W. Li, X. Xiang, C. Li, W. Li and X. He, "Interleaved High Step-Up ZVT Converter With Built-In Transformer Voltage Doubler Cell for Distributed PV Generation System," in *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 300-313, Jan. 2013.

[20] K. Tseng, C. Cheng and C. Chen, "High Step-Up Interleaved Boost Converter for Distributed Generation Using Renewable and Alternative Power Sources," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 2, pp. 713-722, June 2017.

[21] T. Nouri, N. Vosoughi Kurdkandi and O. Husev, "An Improved ZVS High Step-Up Converter Based on Coupled Inductor and Built-In Transformer," in IEEE Transactions on Power Electronics.

[22] G. Ortiz, L. Fässler, J. W. Kolar and O. Apeldoorn, "Flux Balancing of Isolation Transformers and Application of "The Magnetic Ear" for Closed-Loop Volt–Second Compensation," in IEEE Transactions on Power Electronics, vol. 29, no. 8, pp. 4078-4090, Aug. 2014.