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Fixture Design for Parasitic Capacitances of MOSFETs for EMI Applications

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***Abstract*—Due to the fast-switching nature of modern power converters, up to hundreds of MHz of common-mode noise can easily be generated. The characterization of switching components, e.g., Si MOSFETs, is essential for noise reduction. However, limited by the bandwidth of instruments, the voltage-dependent capacitances of high voltage MOSFETs are typically characterized at approximately 1 MHz, which is insufficient for EMI applications. In this paper, the measurement method and the test fixtures are presented. The measurement bandwidth is pushed to 30 MHz and higher, and frequency-dependent capacitances of a MOSFET are observed through measurements.**

***Index Terms*—MOSFET, voltage-dependent capacitances**

I. INTRODUCTION

Switching power converters are widely used in modern electronic devices due to their high efficiency. However, unwanted high-frequency noise is generated by the converters due to their switching nature. Noise can even be observed at thousands of order harmonics of the switching frequency. With the trend toward higher power density, the switching frequencies of converters are pushed higher and can reach dozens of MHz. Severe electromagnetic interference (EMI) issues will be generated with the evolution of power converters.

To estimate the noise produced by a switching converter, reliable measurement and modeling techniques are required. The capacitance-voltage ($C-V$) characteristic is one of the most important parameters of MOSFETs, and the simplified equivalent circuit of a MOSFET is plotted in Fig. 1. Semiconductor device parameter analyzers, e.g., Keysight B1505A, have been developed for such measurements. Nevertheless, the frequency of $C-V$ is limited to 5 MHz, which is insufficient for EMI applications. Vector network analyzers (VNAs) have been applied to extend the frequency range in previous research [1]. Limited by the fixed port impedance, the resolution of the capacitance measurement is insufficient. Additionally, reconfiguration of the measurement setup is required during the $C-V$ test process, as MOSFETs contain three parasitic capacitors.

In this work, considerations in the $C-V$ test are discussed regarding the sensitivity of different impedance characterization methods. In addition, two sets of test fixtures are designed for MOSFETs with a standard 5 × 6 mm footprint. The proposed fixture can greatly reduce the efforts spent on setup configuration. The original contribution of the paper includes the demonstration of frequency-dependent capacitances of Si MOSFETs, which invalidates the modeling method of a commercially available model.

II. $C-V$ MEASUREMENT METHOD AND PRACTICAL CONSIDERATIONS

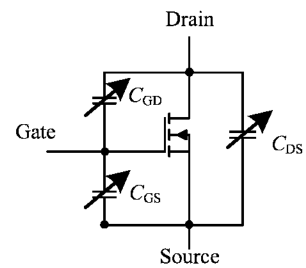

Fig. 1. Simplified circuits of a MOSFET containing three junction capacitances.

As demonstrated in Fig. 1, three parasitic capacitances need to be characterized for a MOSFET. Three different configurations are then required to extract those values separately. The configurations have been standardized and can be easily achieved with commercially available instruments [2]. C_{iss}, C_{rss} and C_{oss} can be measured accordingly with the measurement setups shown in Fig. 2.

Fig. 2(b) shows that the floating current generated by C_{DS} is not detected by the impedance analyzer (IA), as the AC guard provides an alternative current path. It is important to understand that the AC guard is a circuit unique to the autobalancing bridge and that it is connected to the shields of the four-terminal pair connectors. Therefore, C_{rss} can only be measured by an autobalancing bridge IA.

The junction capacitances can be calculated with the measured capacitances through the following equations:

$$C_{GS} = C_{iss} - C_{rss}, \quad (1)$$

$$C_{GD} = C_{rss}, \quad (2)$$

$$C_{DS} = C_{oss} - C_{rss}. \quad (3)$$

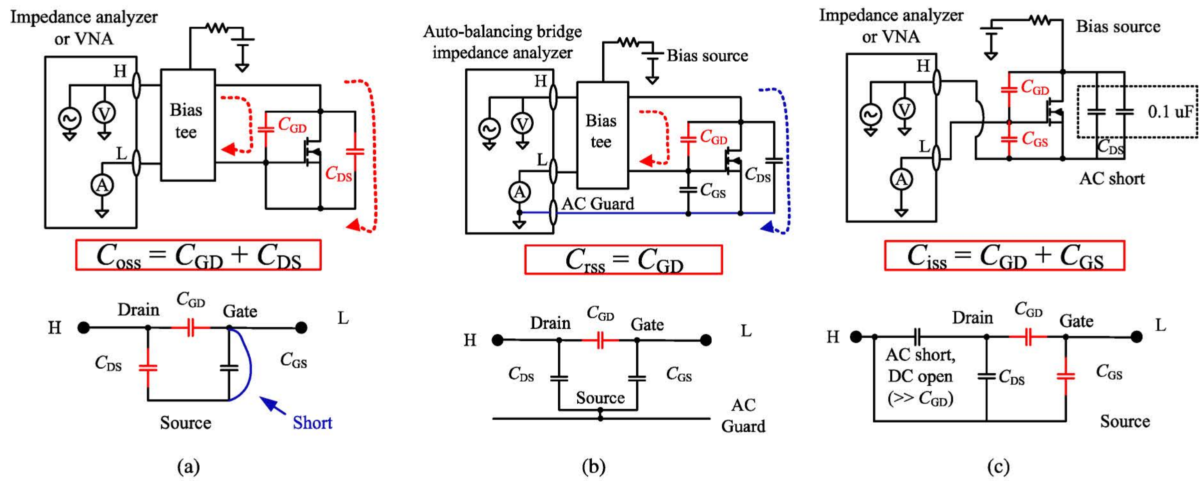

Fig. 2. Configurations and equivalent circuits with an autobalancing bridge impedance analyzer: (a) C_{oss}; (b) C_{rss}; (c)C_{iss}. The autobalancing bridge IA can be replaced by a VNA or an RF I/V IA for C_{iss} and C_{oss} measurements.

The autobalancing bridge IAs bring peculiar advantages in $C-V$ measurements, however, the operation frequency is limited to several MHz, especially when a high bias voltage is expected in the measurement. As an example, the E4990A IA (Keysight) can operate up to 120 MHz, but the bandwidth of its bias fixtures is no more than 2 MHz (model: 16065A and 16065C). RF instruments, e.g., a VNA or an RF IA, are required to extend the measurement to dozens of MHz or even higher frequency ranges. We note that an RF-IV IA enables accurate measurements over a broad range from 1/10 times lower impedance to 10 times higher impedance than the network analyzer method [3].

III. Fixture Design and Measurement Validation

A. Considerations in the Fixture Design

In this section, fixtures for $C-V$ measurements are presented to accommodate different interconnects of the autobalancing bridge IA (Kelvin connection) and the RF-IV IA (coaxial connector).

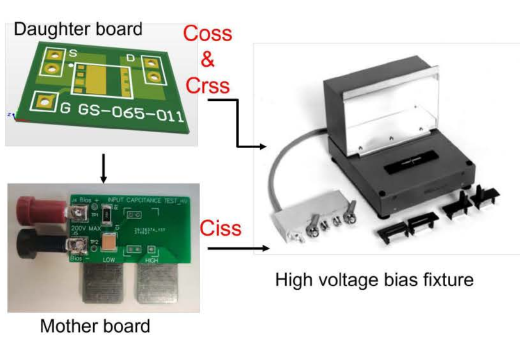

Fig. 3. Fixtures for an autobalancing bridge IA. An external bias tee (Model: Keysight 16065A, ±200 V) is used.

A modular design is applied in the fixture design, as shown in Fig. 3. C_{rss} and C_{oss} can be directly measured with a daughterboard. A motherboard is designed to measure C_{iss}, the bias voltage can be applied through banana connectors, and the daughterboard can be directly installed on the motherboard. Limited by the bias tee, the maximum bias voltage and the maximum frequency are limited to 200 V and 2 MHz, respectively.

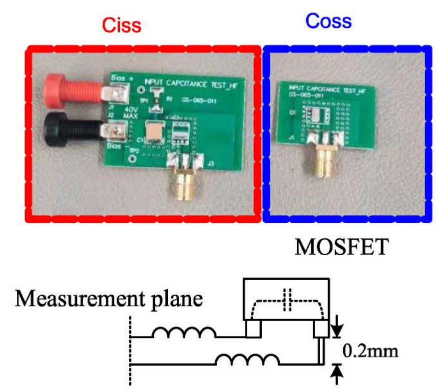

Fig. 4. Fixtures for an RF-IV IA or a VNA. The internal bias tee of the instruments is used.

The operation frequency can be extended to 30 MHz and greater with high-frequency fixtures. It is worth noting that the parasitic inductance should be minimized to extend the operation frequency, and the height between the signal plane and its return plane is configured to be 0.2 mm in this design. The inductance can be further reduced by using a smaller height, but the maximum bias voltage will be compromised.

B. Experimental Verification

To validate the designed test fixtures, a Si MOSFET (model: IPLK70R2K0P7) and a GaN HEMT (High Electron Mobility Transistor) (model: GS-065-11-1-L) is tested with an autobalancing bridge IA at 1 MHz, as illustrated in Fig. 5 and Fig.

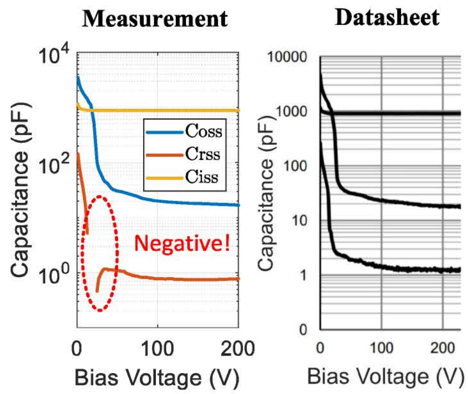

Fig. 5. Parasitic capacitances of the Si MOSFET obtained from the measurement and datasheet.

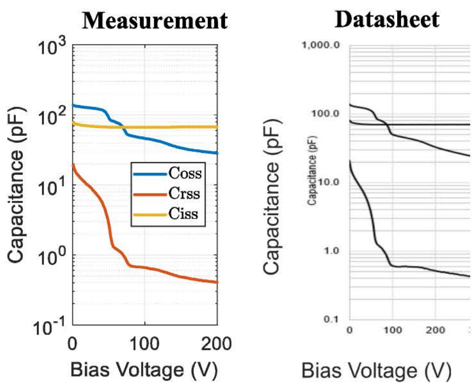

Fig. 6. Parasitic capacitances of the GaN HEMT obtained from the measurement and datasheet.

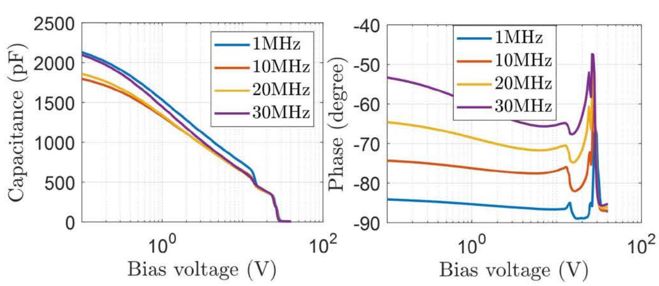

Fig. 7. Measured C_{oss} (IA model: HP4294A, 1 MHz - 1.8 GHz) under different excitation frequencies.

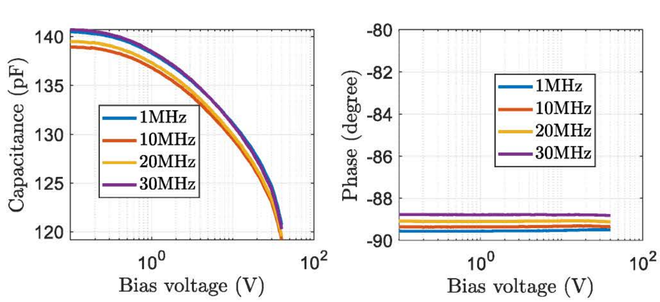

Fig. 8. Measured C_{oss} under different excitation frequencies.

6. The discrepancies between the measured capacitances and those provided by the datasheet are within 3%. However, the C_{rss} of the Si MOSFET exhibit negative value while that of GaN HEMT is positive.

To further validate examine the capacitances, the same transistors are measured by an RF-IV IA, and the measured C_{oss} is demonstrated. The excitation frequency is swept from 1 - 30 MHz, and the bias voltage is configured between 0 - 40 V. The C_{oss} of Si MOSFET is not increasing monotonously with frequency, which indicates the variation is not brought by the parasitic inductance, as shown in Fig. 7. It is worth noting that the phase of the measured capacitance shows a highly unstable phase when the bias voltage is approximately 30 V. As the comparison, the C_{oss} of the GaN HEMT is much more linear, as depicted in Fig. 8.

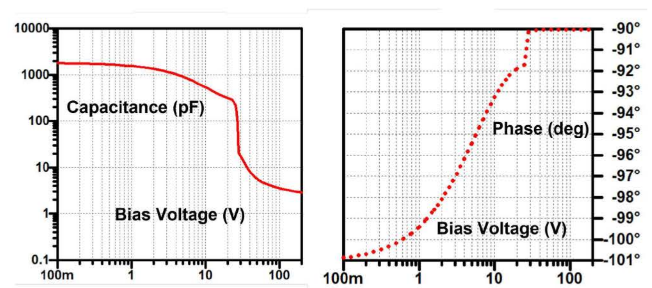

Fig. 9. Simulated C_{oss} of IPLK70R2K0P7. The simulation model is provided by the manufacturer.

Finally, C_{oss} extracted from its SPICE model is illustrated for comparison. The voltage-dependent capacitance is captured by the model; however, the simulated capacitance is frequency-independent. Additionally, the capacitance contains a negative resistance according to its phase information.

IV. Conclusion

The measurement methods and considerations of Si MOSFET s in real practice are discussed in this paper. Two sets of fixtures are designed to facilitate measurements when specialized instruments are not available. The frequency-dependent capacitances of Si MOSFET are captured with the proposed fixture, while the behavior is not shown in the SPICE model. Fundamental modifications are required in the modeling of MOSFETs to enable the next order-of-magnitude improvement for EMC applications.

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