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Insertion Loss Reduction Using Rounded Corners to Mitigate Surface Roughness Effect in PCB Transmission Lines

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***Abstract*—Signal integrity (SI) can be interpreted as a measure of the distortion of the incident pulse, which is attributed to various contributors, e.g., inter-symbol interference (ISI), crosstalk, jitter, etc. The channel insertion loss is generally the most critical concern in SI designs, since it determines the working bandwidth of a high-speed channel, and the bandlimited channels are known as the root cause of ISI. At the tens of Gigabit rates in use today, PCB transmission lines may have appreciable losses, which can be divided into frequency-dependent dielectric loss and conductor loss, and noticeable amount of losses can be generated at high-frequencies due to the skin effect and copper rough surfaces. In order to reduce the additional conductor loss due to the surface roughness, the employment of low-profile copper foils is a common practice in high-speed digital design. However, this existing method is not cost-effective. In this paper, insertion loss reduction using rounded corners are proposed and verified using both 2D and 3D full-wave simulations for the first time. Rounded corners can mitigate the increased insertion loss due to copper surface roughness in PCB transmission lines, and can be applied in high-speed interconnect designs to increase eye margins. The impact of applying rounded corners on far-end crosstalk is also discussed.**

Keywords—conductor loss; channel loss; dielectric loss; far-end crosstalk; insertion loss; rounded corner; surface roughness; transmission line.

I. Introduction

Signal integrity (SI) can be described as simple as the study of incident pulse distortion [1], which can be further attributed to multiple contributors, for instance, inter-symbol interference (ISI) [2], crosstalk [3]-[6], jitter [2], etc. The frequency-dependent insertion loss of a high-speed channel determines the working bandwidth, and a bandlimited channel is unwanted in SI designs since it may cause severe ISI issues and introduce a closed eye at the receiver end [7].

The total channel losses can be divided into dielectric and conductor loss, both of which also demonstrate strong frequency dependency [8][9]. It is known that there is additional conductor loss at high frequencies resulted from the rough copper surfaces [10][11]. At the tens of Gigabit rates in use today, channel loss has already become the bottleneck for high-bandwidth and high-data-rate applications.

In order to reduce the channel loss for high-speed data transition, it is currently a common practice in industries to employ low-loss (or even ultra-low-loss) dielectrics and low-profile copper foils. However, these materials are expensive, making the associated design not cost-effective during the high-volume production.

In this paper, insertion loss reduction using "rounded corners" is proposed and verified using both 2D and 3D full-wave simulations. The real testing coupons are under manufacturing, and the measurement-based validations will be reported in future publications. The rounded corners can reduce the increased conductor loss due to copper surface roughness, and we observed more than 10% improvement in the comparison of total insertion loss at 20 GHz. We expect to see more reduction at higher frequencies according to the trends in the comparisons.

Since the cross-section of a transmission line is changed after applying the rounded corners, the influence on far-end crosstalk (FEXT) is also investigated. It is found that the resulting FEXT may increase by approximately 8% based upon the simulated data, which may necessitate the implementation of FEXT noise mitigation technique described in [3] and [6] in both design and manufacturing phases.

The motivation of introducing rounded corners to PCB transmission lines and various current density distributions are illustrated in Section II. The 3D simulation-based verification is shown in detail in Section III. The impact of applying rounded corners on FEXT is briefly discussed through simulation-based studies in Section IV. Section V concludes the paper.

II. Distribution of Current Density

The high-frequency currents only flow on the "skin" of a conductor, which is known as the skin effect [2], resulting in

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larger AC resistance and conductor loss. Edge effect is another inherent characteristic of eddy current [12]. In order to reveal the impacts of these two effects, several stripline models are constructed in ANSYS Q2D, each of which contains a single-ended signal trace with a different cross-sectional shape, as indicated in Fig. 1(a). All these 2D models adopt the same material properties and smooth coppers, and their characteristic impedance are identical. The complex dielectric constant and geometrical parameters can be found in [13].

Fig. 1(b) compares the distributions of current density in each 2D model, implying that the current tends to be concentrated at the sharp corners due to the skin and edge effects. The maximum current density obtained from the simulations are plotted in Fig. 2, where a noticeable increase in current density is observed when the signal conductor's cross-section switches from rectangle to trapezoid.

The real cross-section of a PCB stripline trace is given in Fig. 3(a), which is mimicked by using the sketch in Fig. 3(b) in the 2D simulation. It is anticipated that the maximum current density is higher than that of the "trapezoid" case in Fig. 1(b), given that the edges in Fig. 3(b) are sharper. The proposed trace cross-sectional shape with rounded corners is demonstrated in Fig. 3(c).

The simulated current density distributions before and after applying the rounded corners are shown in Fig. 4, where it is found evident that rounding the sharp edges can significantly change the current density distribution.

III. Verification of Insertion Loss Reduction

The frequency-dependent per-unit-length (P.U.L.) resistance and inductance values are obtained through the 2D simulations. The comparison of P.U.L. resistance is exhibited in Fig. 5(a), where an approximate 22% reduction can be identified at around 20 GHz.

The conductor loss α_c can be calculated using [12]

$$\alpha_c \approx 0.5R / \sqrt{Z_0} \tag{1}$$

where the characteristic impedance $Z_0 \approx \sqrt{L/C}$. Fig. 5(b) illustrates the improvement in conductor loss after implementing the rounded corners, and the reduction at 20 GHz is about 20%.

The full-wave simulations are performed in ANSYS HFSS, and the Huray surface roughness model [14] is utilized in order to reveal the impact of rounded corners on total insertion loss. In addition to the trace cross-section with rounded corners in Fig. 3(c), one more trace with larger curvatures around the corners is simulated, and the result is included in the comparison in Fig. 6, where the insertion loss reduction at 20 GHz by using the rounded corners in the "rough conductor" cases is pinpointed to be about 11%, and the insertion loss curves may indicate that more reduction in percentage can be expected at higher frequencies. This will be verified through measurement-based studies and reported in future publications.

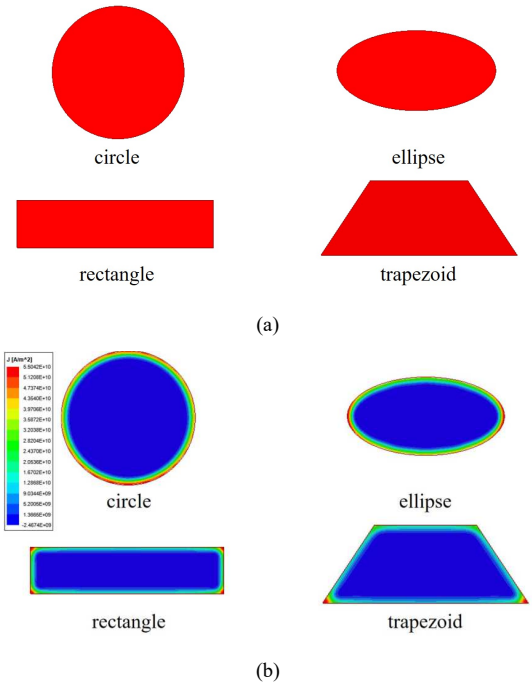


Fig. 1. Stripline signal conductors with various cross-sectional shapes are built in ANSYS Q2D to reveal the distribution of current density due to edge and skin effects: (a) cross-sections of different signal conductors in 2D stripline models, (b) the distributions of current density in each model indicating the current tends to be concentrated at the sharp corners.

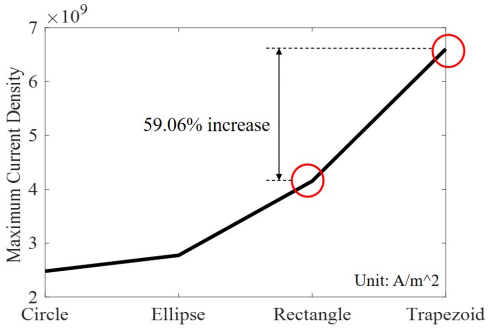


Fig. 2. Comparison of the maximum current density for each shape.

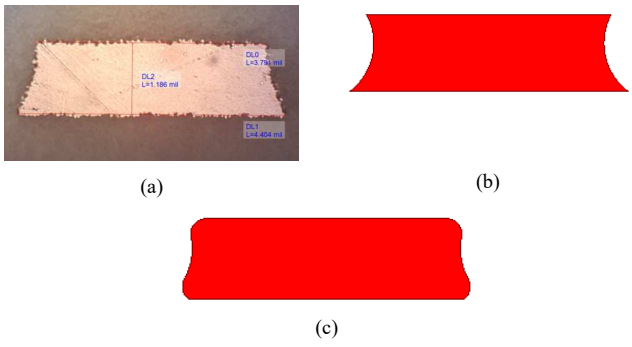


Fig. 3. The cross-section of PCB signal traces: (a) a signal trace of real PCB stripline, (b) 2D cross-section of modeled PCB trace without rounded corners, (c) 2D cross-section of modeled PCB trace with rounded corners.

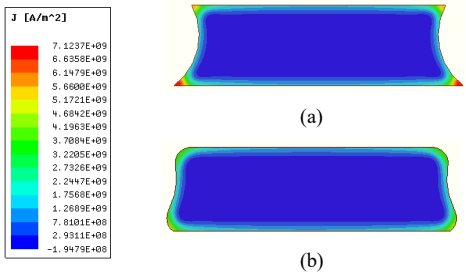


Fig. 4. The simulated current density distributions: (a) baseline case, before applying rounded corners, (b) after applying rounded corners.

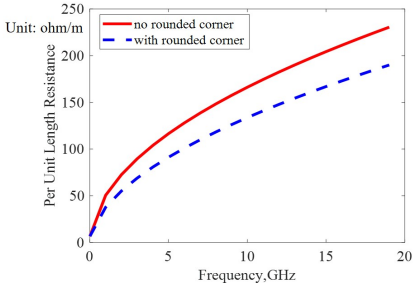


Fig. 5. Comparison of P.U.L. resistance and conductor loss: (a) P.U.L. resistance comparison, (b) conductor loss comparison.

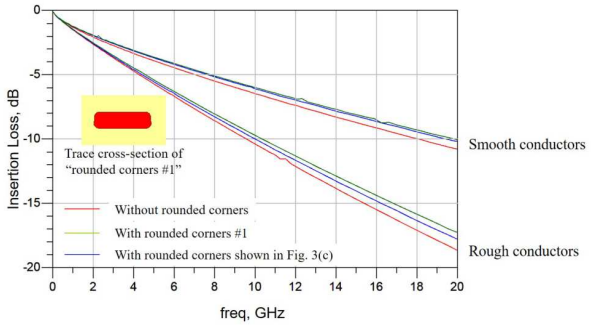
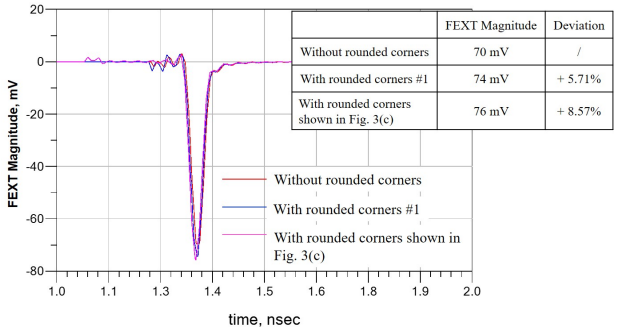


Fig. 6. Comparisons of insertion loss for both "smooth conductor" and "rough conductor" cases.

IV. The Influence on FEXT

The influence of rounded corners on PCB stripline FEXT is examined through 2D simulations, and the results are manifested in Fig. 7. The maximum increase in the time



	FEXT Magnitude	Deviation
Without rounded corners	70 mV	/
With rounded corners #1	74 mV	+ 5.71%
With rounded corners shown in Fig. 3(c)	76 mV	+ 8.57%

Fig. 7. Comparison of FEXT magnitudes in the time domain after implementing the rounded corners.

domain FEXT after applying the rounded corners is 8.57%, which can be readily mitigated using certain FEXT noise cancellation techniques.

V. Conclusion

Insertion loss reduction using rounded corners is proposed and verified through the full-wave simulation-based studies in this paper. About 20% reduction in the conductor loss and approximately 11% decrease in the total insertion loss are identified. The downside of using the rounded corners is the slight increase in FEXT magnitude, which can be overcome by employing the FEXT noise cancelation techniques.

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