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A Methodical Approach for PCB PDN Decoupling Minimizing Overdesign with Genetic Algorithm Optimization

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***Abstract*— An optimization routine is applied for the decoupling capacitor placement on Power Distribution Networks to identify the limit beyond which the placement of additional decaps is no longer effective, thus leading to wasting layout area and components, and to a cost increase. A specific test example from a real design is used together with the required target impedance and frequency band of interest for the PDN design. The effectiveness of the decap placement while selecting different layers of the stack-up, and while moving the upper limit of the PDN design band is analyzed. Such analysis leads to helpful insights based on the progression of the input impedance during the optimization process, and to develop useful guidelines for avoiding over-design of the PDN.**

Keywords—PDN, power integrity, decoupling capacitors, optimization, genetic algorithm, physical limitation.

I. INTRODUCTION

The ever-growing complexity of electronic systems, the current trend toward a larger current demand and toward lower supply voltage levels, calls for a proper design of the Power Distribution Network (PDN) in order to meet the required noise margin at the input power and reference IC pins, and thus ensure the IC functionality [1]. The PDN decoupling at the PCB level usually consists of two primary design bands, the lower band involving the selection of low frequency decoupling capacitors (decaps) in combination with the specific DC/DC converter requirements, and an upper band, from tens or hundreds of kHz up to tens of MHz, where the PDN design relies on the high frequency decaps. This paper focuses on the design of the PCB PDN by applying an optimization routine based on the Genetic Algorithm (GA) for appropriately selecting the decap value [2]-[3]. Optimization algorithms have been reported and applied to the PCB PDN design, similarly to the one used herein [4]-[7]. However, such optimization methodologies may lead to overdesign of the PDN by placing a very large number of decaps when getting close to the physical limit of the PDN inductance. Such limit is dictated by the inductance defined by the loop from the IC power and reference pins, to the decaps, in the case that all available decap locations are loaded by the minimum decap ESL. So, it is very important to critically evaluate the progression of the PDN input impedance to avoid applying many decaps for only an incremental improvement of the input impedance toward the target impedance. This paper addresses this aspect in order to develop relevant insight for PI designers.

II. PRE-LAYOUT PDN DESIGN

A. Physics-Based PDN Modeling

A PDN impedance that is lower than the target impedance is a crucial criterion for the PDN design to maintain the stable voltage level of the supply system. In a multilayer board, the PDN geometry, including the stack-up, IC pin map pattern, as well as the decoupling capacitor keep-in area, placement pattern and number of decaps will have a great impact on the designed PDN impedance.

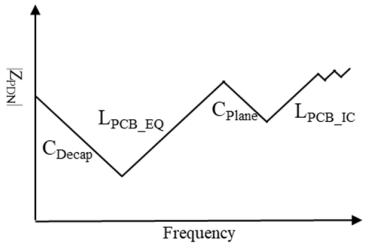
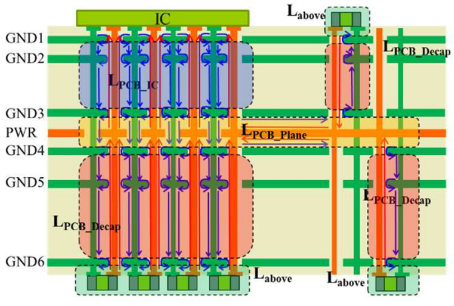


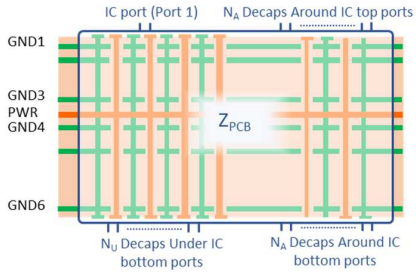
Fig. 1 A typical PDN impedance profile.

A typical trend of the frequency dependent PDN impedance is shown in Fig.1. In the PDN design, the C_{Plane} is related to the power-net area fill shape, thickness of the dielectric substrate and dielectric material property in the power-power and power-power return cavity. The C_{Decap} is the capacitive trend obtained after placing decaps on the PDN, which is followed by the inductive trend as the combination of the parasitic inductance associated to the decap location, the decap ESL, and the inherent inductance L_{PCB_IC} of the power plane connection up to the package. The low frequency portion of the impedance profile in Fig. 1 will become more complex once several decoupling capacitors with different frequency response will be placed right under the IC pins or around the IC on the top or on the bottom layer. At higher frequency, beyond the inductive part due to L_{PCB_IC}, the alternating trend of poles and zeros may be visible due to the distributed resonances associated to the power-net area fill size. This behavior may be hidden in the case that the package and IC PDN modes are included, or when the power plane distributed resonances occur beyond the frequency of interest. The specific inductance contributions that are relevant for an accurate modeling of the PDN system and its impedance optimization are shown in Fig. 2. The L_{PCB_EQ} can be segmented as the sum of L_{PCB_IC}, L_{PCB_Plane}, L_{PCB_Decap}, and L_{above} based on the current loops identified in Fig. 2 and introduced in [8]. The minimum inductance that can be

obtained in the PDN design is the L_{PCB_IC}, and it sets the minimum inductance value of the PDN system, although it is impractical since it takes into account only a partial loop of the complete path from the IC to the decap. For each decap, instead, the loop and its corresponding inductance is comprised of several contributions highlighted in Fig. 2. The current flowing from the decap to the IC pins flows through the direct and return paths involving L_{PCB_IC}, L_{PCB_Plane}, the L_{PCB_decap}, L_{above}, and the ESL. L_{above} is the contribution that takes into account the current loop from the top-most plane (GND1 in Fig. 2) or bottom-most plane (GND6), in the case that decaps are placed on the bottom layer, up to the decap itself. The ESL is the decap inductance due to its specific package size and packaging technology. The overall PDN system shown in Fig. 2 is quite complex since it may involve large plane areas (tens or hundreds of mm), very small dielectric thickness (tens or hundreds of µm), round geometries such as vias, pads, and antipads, decap pads, etc… This makes the 3D modeling quite complex and difficult due to the inevitably large mesh size and simulation time. More appealing approaches can be implemented for a reliable and much quicker modeling ranging from the cavity model method [9]-[11], to the boundary element method [12], among many fully analytical or 2D-based approaches. The modeling method implemented in this paper is the one in [8], [17] based on the self and mutual inductance terms identified in Fig. 2, and whose outcome is a multiport impedance matrix, Z_{PCB}. Its first port corresponds to the IC port as a result of the combination of all power and ground vias connecting the IC power/ground pins to the power plane of interest (PWR in Fig. 2), according to the procedure in [13]; thus, the IC port to which all subsequent calculations of the PDN impedance in this paper refer to is assumed to be at the center of the IC footprint. The other tens (or even hundreds) ports of Z_{PCB} corresponds to the locations where decaps can be added. The decaps can be placed under the IC where appropriate pads are placed at the end of the power/ground IC via pairs. Other locations around the IC are made available by the designers within the keep-in areas set by other layout constraints. Such locations provide the flexibility to place the decaps either on top or on the bottom side. However, all decaps around the IC will be placed on the top or on the bottom layer depending on the location of the PWR layer in the multilayer stack-up, and potential manufacturing constraints. A PWR layer above the midpoint of the stack-up will provide a smaller inductance L_{PCB_Decap} toward the top layer rather than toward the bottom layer, therefore the top layer will be devoted to the placement of the decap around the IC. A PWR layer below the stack-up midpoint leads to place the decaps on the bottom layer.



(a)



(b)

Fig. 2 (a) Physics-based circuit model for inductance modeling. (b) Developed impedance matrix for the PDN optimization based on N_U (number of ports for the placement of decaps Under IC) ports, and N_A (number of ports for the placement of decaps Around the IC) ports on either the top or bottom sides.

B. Optimization Algorithm for Decap Placement

Once the PDN modeling is established, and the PDN impedance for the bare PCB can be readily calculated, the decoupling capacitors need to be placed. The key aspects for placing the decap on the PDN are the decap position, the decap capacitance value, and the decap ESL and package size. The decap position is strictly related to the corresponding inductance, mainly due to L_{PCB_Plane}, that depends on the distance between the decap and the IC [11]. The decap ESL is mainly due to its package, with the package dimensions affecting the decap pads and connection vias. The decap capacitance can be selected to be as large as possible within a given package size; however, more sophisticated design strategies may involve optimization algorithms and machine learning approaches [7],[14]. Since several variables are involved in the PDN design and decap placement, the PDN optimization aimed at minimizing the number of decaps is a challenging task. Currently several methodologies have been developed to identify the best PDN decoupling solution, and some of them rely on optimization algorithms [15]-[16]. One promising optimization methodology is based on the Genetic Algorithm [2]-[3], [6], and it has been shown to be effective while iteratively adding only one decap at each optimization step. While the GA is running, it evaluates the cost function for each combination of decap value and position that is associated to a newly created chromosome. The cost function is evaluated by summing up, in dB and for each frequency point of the logarithmic frequency axes, the distance between the PDN impedance and the target impedance that needs to be reached. Of course only the points for which the input impedance is above the target impedance are considered.

The structure of the impedance matrix Z_{PCB} is shown in Fig. 2b, whose total number of ports is $1+N_U+2\cdot N_A$, as defined in the caption of Fig. 2, and it is handled by the GA optimization process as:

I. The Z_{PCB} matrix is first reduced by removing all ports dedicated to the placement of decaps around the IC (both for the top and bottom connection) in order to make the optimization process more efficient.

II. The GA runs and optimizes the number and types of decaps Under IC, up to a maximum N_U. A fixed population size and number of generations equal to 10 is used; such value is demonstrated to be a good compromise between identification of the best solution and calculation speed.

III. If the Z_{target} is met with a number of decaps less than or equal to N_U, the optimization stops. Otherwise Step IV is applied.

IV. The impedance matrix Z_{PCB} is loaded with the N_U optimized decaps Under IC.

V. The user may select one or more stack-up layer where the PWR net of interest is assigned in order to explore one or more solutions and identify which layer provides the best decap configuration. Thus, depending on the position of the PWR layer above or below the midpoint of the stack-up, the decaps will be placed only on the top or on the bottom side. The unused ports will be removed from Z_{PCB}, that will become a $1+N_A$ ports impedance matrix.

VI. The GA runs and optimizes the number and types of decaps Around the IC, up to a maximum N_A.

C. Evaluation of PDN Decoupling Feasibility

The number of possible decaps under the IC N_U is usually forced by the PWR pins of the IC and the corresponding through hole vias that reach the bottom side of the PCB. Whereas the PI designer may set, at a pre-layout stage, the keep-in areas and the maximum number of the decaps around the IC N_A based on the BOM requirements. Having the total decap N_U+N_A being set, a physical limitation may be derived as the minimum inductance that the PDN may reach. This physical limitation is computed by loading all N_U+N_A decap ports with the minimum ESL available in the decap database, thus assuming the best decoupling configuration. This preliminary calculation is essential, especially concerning the high frequency portion of the target impedance that is inductive above a certain frequency limit. This behavior is primarily dictated by the L_{PCB_IC} in Fig. 2a [17], to which other specific inductive contributions are summed up such as L_{PCB_decap} and L_{plane}. An example is shown in Fig. 3, where the target impedance Z_{target} is defined, and the specific range of interest associated to the specific power net is identified by the lowest and highest target frequencies f_{Low} = 1 MHz and f_{High}= 50 MHz, respectively. Two physical limitations are shown as examples to demonstrate their usefulness at an early design stage. The red dot-dashed curve, Case 1, is always below the Z_{target}, therefore a decoupling solution exists based on a maximum of N_U+N_A decaps. The green dotted line, instead, is associated with Case 2, and it crosses the Z_{target} at around 29 MHz, thus before f_{High}, the desired high-frequency upper bound of the decoupling solution. This indicates that no matter how many decaps will be placed, at most N_U+N_A, the selected PWR layer and the maximum decaps N_U+N_A will never lead to completely satisfying the Z_{target} requirements. Practical examples will be shown in Section III to demonstrate the relevance of such preliminary evaluation of the decoupling feasibility.

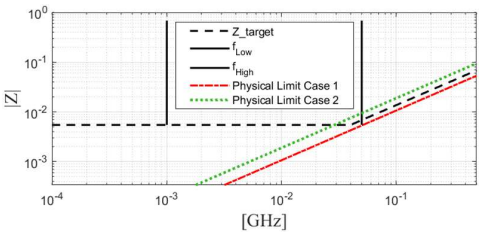


Fig. 3 Explanation of the physical limitation for two different cases whose inductive value is below (Case 1) and above (Case 2) the inductive portion of the target impedance.

III. Application Examples

This Section applies the procedure described in Section II to a specific PCB in order to demonstrate the effectiveness of the proposed modeling and optimization methodology, and to define useful guidelines for PI designers to be applied at an early PDN design. The specific example is taken from a production PCB design whose PDN impedance calculation based on [8], [17] led to a multiport Z_{PCB} with 105 ports (1 IC port, and N_U+N_A for decaps). The decaps are loaded to the ports analytically in Matlab.

A. Description of Test Cases

The power net area fill is of square shape of 1.8"× 1.8" size and it is shown in Fig. 4a. The low frequency PDN design is completed and consists of 18 low-frequency large-value decaps, typically greater than 100 µF, identified by the black rectangles in the figure. The blue dots correspond to the GND pads on the top and bottom layers connecting the vias to the IC pads, whereas the red dots identify the N_U = 44 PWR pads where decaps under the IC can be placed (the available under IC decap locations are marked by a black line) The two yellow rectangles identify the keep-in areas where the decaps around the IC can be placed. The two areas on the left and on the bottom right side of the IC are divided into 24 and 6 sub-areas, respectively, where a maximum of 2 decaps for each sub-area can be placed. Thus, a total of N_A = 60 decaps are available to the optimization routine. The stack-up is shown in Fig. 4b, where three possible layers dedicated to host the PWR net are identified and marked in red, V06, V09, and V12. Only a single layer is used for the PDN power net area fill though. The IC is placed on the top layer. A typical decap database is considered in this study whose capacitance, ESL and ESR values are reported in Table I for the decaps under the IC (d_A-d_L) and around IC (d_A-d_N) locations.

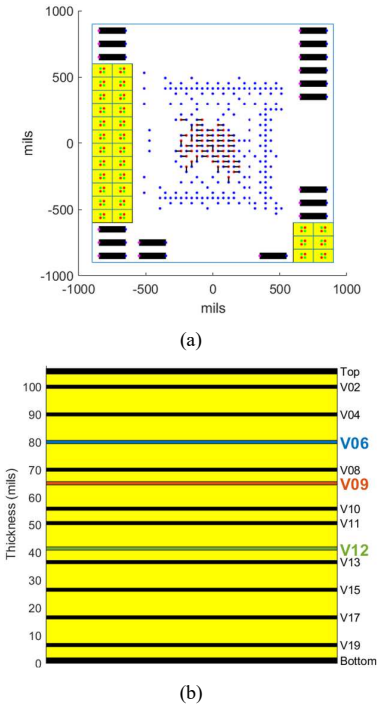


Fig. 4 (a) Overview of the power net are fill (blue outline) and of the decap locations around the IC (yellow areas) and under the IC (small black lines). Units: mils (b) Stack-up indicating three possible layer locations for the PDN power-net area fill.

TABLE I. DATABASE OF DECAPS UNDER AND AROUND THE IC

Decap Name[a]	ESL	ESR	C	Package
d_A	0.4 nH	60 mΩ	10 nF	0402
d_B	0.4 nH	43 mΩ	22 nF	0402
d_C	0.4 nH	38 mΩ	47 nF	0402
d_D	0.4 nH	28mΩ	100 nF	0402
d_E	0.4 nH	20 mΩ	220 nF	0402
d_F	0.4 nH	16 mΩ	470 nF	0402
d_G	0.4 nH	12 mΩ	1 µF	0402
d_H	0.4 nH	9 mΩ	2.2 µF	0402
d_I	0.4 nH	7 mΩ	4.7 µF	0402
d_J	0.4 nH	5 mΩ	10 µF	0402
d_K	0.4 nH	4 mΩ	22 µF	0402
d_L	0.4 nH	3 mΩ	47 µF	0603
d_M	0.4 nH	2 mΩ	100 µF	0603
d_N	0.4 nH	1 mΩ	220 µF	0805

[a] Decaps d_M and d_N are used only for the locations around the IC

The target impedance is constant and equal to 5.5 mΩ up to 40 MHz; beyond this point an inductive trend is usually specified by the IC vendor or by PI designer experience based on the corresponding voltage fluctuation allowed on the PWR rail. This inductive trends corresponds to an inductance of 21.75 pH. The physical limitations for the possible location of the power net area fill in the stack-up are evaluated and are shown in Fig. 5. The minimum inductance value that can be reached is 21.3 pH, 24.62 pH, and 31.08 pH for the power net area fill located on layer V06, V09, or V12, respectively. The range of interest for the PDN design starts from f_{Low} = 100 kHz (not shown in the figure). However, a proper decoupling is achieved by adding the low frequency decaps shown in Fig. 4a. The upper limit f_{High}, instead, is varied to demonstrate the usefulness of the proposed pre-layout analysis to identify a proper PDN decoupling solution in order to avoid an inordinate number of small-value decoupling capacitors at the high-frequency range limit for incrementally approaching the PDN target impedance. The f_{High} is assumed to be 20 MHz, 30 MHz, and 40 MHz, with the latter value corresponding to the knee frequency of the target impedance.

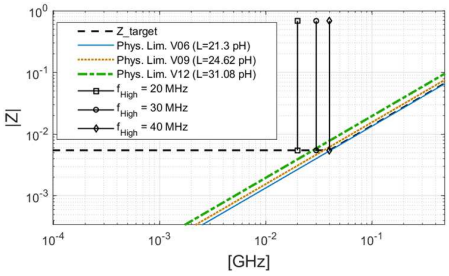
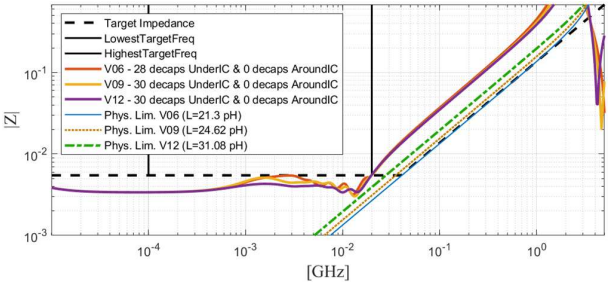


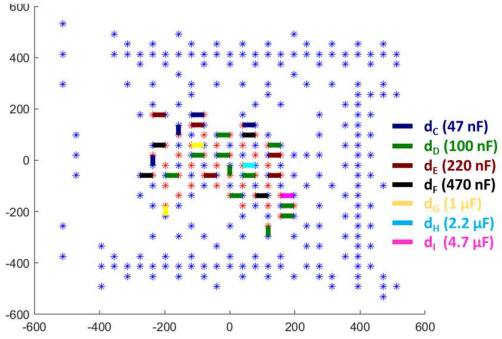
Fig. 5 Physical limitation for the three considered cases of the PWR layer assigned to V06, V09, or V12.

B. Optimization Results

The optimization process is run for the three cases with the power net area fill on different layers (V06, V09, or V12), and for three different upper limits of the target impedance. The first simulation is run based on f_{High} = 20 MHz. The results are shown in Fig. 6a. The target impedance in the frequency range of 100 kHz to f_{High} = 20 MHz is met by placing only decaps under the IC for the three PWR layer cases, thus those decaps that are effective the most due to their smaller L_{PCB_Decap}, compared to the decaps around the IC. The PDN at V06 is successfully decoupled by using a slightly smaller number of decaps, 28 compared to the 30 to be used for both V09 or V12. An example of the decap placement is shown in Fig. 6b for the case of V06. While the GA is running, it adds a decap at each iteration, thus it is possible to catch the PDN impedance progression during the optimization process, as shown in Fig. 6c for the V06 case. It is clear how the first larger value decaps are very effective at the lower frequencies, and they bring down the PDN input impedance with only a few decaps, as opposed to the incremental effectiveness of the numerous small-value decaps at the higher frequencies. This will be more apparent for the following cases where the f_{High} is moved to 30 MHz and then to 40 MHz, and the decoupling solution given in Table II.



(a)



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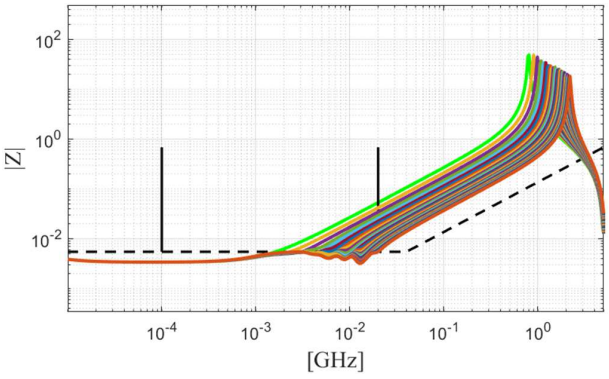

(c)

Fig. 6 (a) Optimization results for the cases of the power net area fill on V06, V09, or V12 when f_{High} is set to 20 MHz. (blue-GND, red-PWR vias) (b) Optimized decaps under the IC for the V06 case (Units: mils). (c) Progression of the V06 PDN optimization as decaps are added: the advantage of the small-valued decaps added toward the end of the optimization for improving the PDN impedance toward f_{High} is marginal compared to the large-valued decaps more effective at lower frequencies.

The optimization results for the case of f_{High} = 30 MHz are summarized in Fig. 7. In this case the physical limitation for V12 falls within the optimization band, as shown in Fig. 5, since the V12 minimum achievable inductance crosses the Z_{target} = 5.5 mΩ at 27.9 MHz, thus before the f_{High}. The PDN power net area fill located on layer V12 is unfeasible, thus the optimization is run only for the power net area fill on layer V06 or V09. This time the placement of the decaps only under

the IC is insufficient for meeting the target impedance requirements. Therefore, all 44 locations under the IC are first filled, and the corresponding decaps are optimized; then 6 decaps and 14 decaps around the IC are also added during the optimization process for the V06 and V09 PDN cases, respectively.

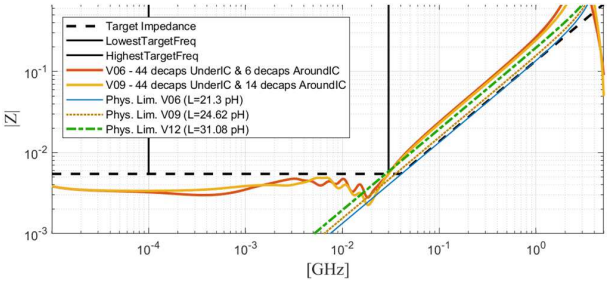

Fig. 7 (a) Optimization results for the cases of V06 or V09 when f_{High} is set to 30 MHz.

The last case is based on f_{High} = 40 MHz. For this case the V09 PDN design is unfeasible, since the physical limitation curve crosses the Z_{target} at 35.8 MHz, thus the GA optimization provides a viable solution only for the V06 case at the cost of additional decaps around the IC. The target impedance is met with 44 decaps under the IC and 21 around the IC as shown in Fig. 8. If the optimization is forced to run also for the V09 case, thus bypassing the physical limitation check, all 60 locations around the IC would have been filled, with a very limited incremental improvement in the V09 PDN impedance as the PDN impedances approaches the target impedance.

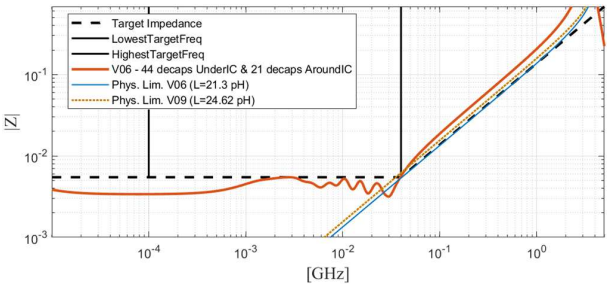

Fig. 8 (a) Optimization results for the case of V06 when f_{High} = 40 MHz.

A complete summary of all optimized cases is given in Table II where the details of all placed decaps are specified. The resonant frequency of each decap is given by the series inductance of L_{PCB_decap}, L_{above}, and the ESL with the decoupling capacitor value. As seen in Table II while f_{High} increases, the most used decap has a smaller value, thus a high resonant frequency, to be able to bring down the PDN input impedance at higher frequency. For the designs based on f_{High} = 20 MHz all three cases of PDN layer area fill location (V06, V09, or V12) can meet the required Z_{target}, and this is accomplished by placing only some decaps under the IC (28, 30, and 30, respectively). However, when moving f_{High} to 30 MHz, all 44 locations under the IC will be filled up and some decaps around the IC are required to meet the Z_{target}, i.e., 6 and 14 decaps for the V06 or V09 cases, respectively. The number of decaps around the IC further increases when f_{High} = 40 MHz to 21 for the V06 case, and all locations would be filled for the V09 or V12 cases without achieving the PDN impedance completely below the Z_{target}. A detailed comparison is shown in Fig. 9 where the three PDN designs for V06 are compared. The inductive behavior of the V06 PDN input impedance beyond f_{High} is shown for the three PDN designs; the values obtained are 58.6 pH, 37.7 pH, and 29.6 pH, for the 20 MHz, 30 MHz, and 40 MHz cases, respectively. Basically, the inductive improvement of Z_{in} becomes more and more incremental when f_{High} is increasing, at a relevant cost in terms of number of decaps, moving from 28 decaps under the IC for the case of f_{High}=20 MHz, to 44+6 decaps when f_{High}=30 MHz, and 44+21 decaps for the last case of f_{High}=40 MHz. From the inset in Fig. 9 the improvement of the impedance bandwidth from 20 MHz to 40 MHz is highlighted. However, this is achieved at a cost of 37 additional decaps of small value (mainly 22 nF and 47 nF), thus more than twice the decaps initially optimized for f_{High}=20MHz. In these specific examples the ESL is constant and equal to 0.4 nH for all decaps, independently on their package; if different packages and corresponding ESL are involved in the design, the optimization results would certainly be different. However, the conclusions drawn in terms of number of necessary decaps and their marginal impact toward the f_{High} would be the same obtained by the examples shown herein. Moreover, the optimization process can be readily applied when multiple power rails need to be designed as long as the specific keep-in areas for decaps Around the IC are defined by the designer. The locations of decaps Under IC, instead, are inherently assigned by the package footprint for the multiple rails. The shown optimization can also be used when the Z_{target} is defined as a mutual impedance in the case that the goal is to reduce the noise on the overall PDN area.

TABLE II. OPTIMIZED PDN DECOUPLING SOLUTIONS AT DIFFERENT f_{High} : #DECAPS UNDER IC (AROUND IC)

Decap Name[a]	V06 20 MHz	V09 20 MHz	V12 20 MHz	V06 30 MHz	V09 30 MHz	V06 40 MHz
d_A (10 nF)	0	0	0	0 (0)	0 (0)	0 (0)
d_B (22 nF)	0	0	0	4 (0)	0 (0)	12(19)
d_C (47 nF)	4	3	0	20(5)	25(13)	13 (2)
d_D (100 nF)	11	14	15	8 (0)	7 (0)	7 (0)
d_E (220 nF)	5	5	6	4 (0)	5 (0)	4 (0)
d_F (470 nF)	4	3	3	4 (0)	2 (0)	4 (0)
d_G (1 µF)	2	2	2	2 (0)	2 (0)	2 (0)
d_H (2.2 µF)	1	2	2	1 (0)	2 (0)	1 (0)
d_I (4.7 µF)	1	1	1	1 (0)	1 (0)	1 (0)
d_J (10 µF)	0	0	1	0 (0)	0 (1)	0 (0)
d_K (22 µF)	0	0	0	0 (0)	0 (0)	0 (0)
d_L (47 µF)	0	0	0	0 (1)	0 (0)	0 (0)
d_M (100 µF)				(0)	(0)	(0)
d_N (220 µF)				(0)	(0)	(0)
Total	28	30	30	44 (6)	44(14)	44(21)

[a] Decaps d_M and d_N are used only for the locations around the IC

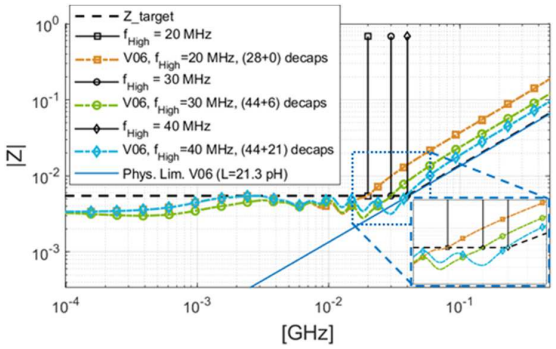

Fig. 9 Comparison among the three optimized V06 PDNs based on the three f_{High} values.

CONCLUSIONS

A careful analysis for the PDN design based on the optimization of decap type and position is carried out aimed at defining practical design guidelines for avoiding PDN overdesign. This is especially relevant for a design involving a new IC, where the on-die and on-package capacitance may be unknown, and also at an early stage of a pre-layout design when transient current information is not available. So, the proposed methodology helps the PI designer to understand the marginal impact of additional decaps placed to move up the effective frequency of the input impedance, even beyond the value of f_{High} initially set. Once the IC design is defined the transient current and its spectrum may be somehow available, such that the corresponding PDN transient noise can be evaluated based on the PDN impedance, and the benefit of the additional decaps can be quantified. Then the PDN layout can be adjusted by accordingly refining the number of necessary decaps. The possibility to calculate the transient noise helps also to relax the constant (resistive) portion of the Z_{target}. The analysis is based on a real test case where the selection of the most appropriate stack-up layer for locating the PWR net is also considered. Further, a parametric analysis is performed to investigate the impact of the high-frequency bound of the target impedance specification f_{High}, in terms of the required number of decoupling capacitors necessary to meet the Z_{target} up to f_{High}. The results shown suggests that a careful look should be given to the required f_{High}, and its relationship to the frequency point where the resistive portion of Z_{target} meets the physical limitation inductance curve. When they are too close, although the PDN design may still be feasible, it is achieved at a high cost in terms of number of decaps using many decaps of low capacitance value. Avoiding the use of numerous small-valued decaps that provide only incremental improvement in the region where the resistive portion of the target impedance approaches the inductive physical limitation curve, may be achieved by increasing the corresponding BOM in terms of layout area and components, or the f_{High} may be accordingly decreased. This may be done while taking into account also the impact of the package PDN, and significant on-chip capacitance, since, after being combined with the PCB PDN, the Z_{target} requirements toward a lower f_{High} might be relaxed. To this aim, even though an accurate model is not made available by the IC vendor, a rudimentary R-L-C PDN package model may be sufficient for setting Z_{target} constraints. The R and L elements should take into account the PCB to package connection mainly based on known geometries, and any on-package and the on-chip decoupling capacitance, may be derived according to typical IC current demand using a broad design maxim, e.g. 10-100 nF/A of DC current. Further research is currently on-going to demonstrate the impact of the package PDN and on-chip capacitance on the optimized decoupling solutions. Future work will also be carried out to make the proposed methodical approach more valuable and of practical use by:

- Running a parametric variation of the resistive portion of the Z_{target} to understand the sensitivity of the overall decoupling solution in terms of number of caps, physical inductance limitation with added number of potential decap sites, and f_{High}.
- Quantifying the marginal improvement of additional decaps toward f_{High} by evaluating the PDN transient voltage noise in order to avoid overdesign in the region where the resistive portion of the target impedance intersects the physical inductance limitation, although difficulties may arise in knowing the time-domain current profile to use.

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