

Missouri University of Science and Technology Scholars' Mine

Electrical and Computer Engineering Faculty Research & Creative Works

**Electrical and Computer Engineering** 

01 Jan 2022

# A Practical Simulation Flow for Singing Capacitor based Acoustic Noise Analysis

Xin Yan

Songping Wu

Mingfeng Xue

Chi Kin Benjamin Leung

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele\_comeng\_facwork/4687

Follow this and additional works at: https://scholarsmine.mst.edu/ele\_comeng\_facwork

Part of the Electrical and Computer Engineering Commons

### **Recommended Citation**

X. Yan et al., "A Practical Simulation Flow for Singing Capacitor based Acoustic Noise Analysis," *2022 IEEE International Symposium on Electromagnetic Compatibility and Signal/Power Integrity, EMCSI 2022*, pp. 29 - 33, Institute of Electrical and Electronics Engineers, Jan 2022. The definitive version is available at https://doi.org/10.1109/EMCSI39492.2022.9889341

This Article - Conference proceedings is brought to you for free and open access by Scholars' Mine. It has been accepted for inclusion in Electrical and Computer Engineering Faculty Research & Creative Works by an authorized administrator of Scholars' Mine. This work is protected by U. S. Copyright Law. Unauthorized use including reproduction for redistribution requires the permission of the copyright holder. For more information, please contact scholarsmine@mst.edu.

## A Practical Simulation Flow for Singing Capacitor Based Acoustic Noise Analysis

Xin Yan\*1, Songping Wu<sup>#2</sup>, Mingfeng Xue<sup>#3</sup>, Chi Kin Benjamin Leung<sup>#4</sup>, Daryl Beetner\*5, Jianmin Zhang<sup>#6</sup>

\*EMC Laboratory,

Missouri University of Science and Technology

Rolla, MO, USA

<sup>5</sup>daryl@mst.edu

#Google Inc.

Mountain View, CA, USA <sup>6</sup>jianmin@google.com

Abstract-Multilayer ceramic capacitors (MLCCs) are widely used in modern electronics. Due to the piezoelectric effect of the ceramic material, however, MLCCs subjected to electrical noise may vibrate and generate acoustic noise, as 'singing'. Acoustic noise can be annoying for users, especially within mobile devices, so it becomes important to perform acoustic noise analysis before a product is released. In this paper, a practical simulation flow for singing capacitor based acoustic noise is presented. The simulation flow and analysis method are developed on Ansys Sherlock and Mechanical. In Ansys Sherlock, local library and Approved Vendor List (AVL) files were used to build the model efficiently. After the PCB and all parts were set correctly, the model was imported to Ansys Mechanical for further modal analysis and harmonic analysis. Using the proposed simulation flow the simulation model could be easily created, and the inherent vibration properties and frequency response of the structure could be estimated.

#### Keywords—Simulation flow, Ansys, modal analysis, harmonic analysis

#### I. INTRODUCTION

The acoustic noise generated from electronic devices can be disturbing to users. One of the major sources of acoustic noise is multilayer ceramic capacitors (MLCCs). MLCCs are made of many alternating layers of metallic electrodes and dielectric ceramic. MLCCs are available in a wide range of capacitance values with a compact size. They are useful in part because the equivalent series inductance (ESL) of MLCCs is smaller than other types of capacitors. As a result, MLCCs are widely used on consumer PCBs, and applied as decoupling capacitors on Power Distribution Networks (PDNs), as shown in Fig. 1. Many studies have addressed the power integrity issues associated with MLCCs [1]-[3]. Power integrity issues, however, are not the only issue of concern. When an electrical signal is applied to the MLCCs, the MLCCs could vibrate and generate acoustic noise through the piezoelectric effect, which is described as 'singing' [4][5]. This acoustic noise issue could be critical if the product is close to ear, for instance when used in wireless earbuds.

Some studies have previously addressed the acoustic noise from MLCCs. The correlation between the acoustic noise and vibration in MLCCs was studied in [6] and the mechanism of acoustic noise was explained. Another study demonstrated that acoustic noise can be measured by analyzing the board vibration instead of directly measuring the MLCCs, as the size and weight



Fig. 1. Use of MLCCs. (a) PCB PDN geometry. (b) MLCCs on a graphic card.

of MLCCs are too small to generate noticeable noise [7]. A simulation methodology to provide design guideline for MLCC placement and PCB fixation to decrease board vibration was proposed in [7]. In [8], a statistical simulation methodology for PCB intrinsic vibration properties was proposed, and the thickness, mass density, and Young's modulus of each board layer were identified as the key parameters. A test methodology was developed using laser Doppler vibrometer to accurately identify primary vibration MLCC sources on PCBs in [9]. By calculating the coherence value between the electrical signal during product operation and MLCC vibration characteristics, it was shown that problematic MLCCs could be identified in [10]. Besides PCB vibration analysis, measuring the acoustic noise in the chamber is also an efficient and direct way to analyze the acoustic noise from the product.

While a simulation analysis can be useful for estimating board vibration behavior at the early design stage, setting up the simulation is a time consuming task due to the massive number of parts on a single board. Although the weight of most parts is



Fig. 2. Overview of the simulation flow.

small, the total weight of all parts is not negligible, especially in a small device where the weight of the parts is comparable with the weight of the PCB. In order to get an accurate simulation result, all parts need to be modeled properly. It is therefore necessary to optimize the simulation flow for acoustic noise analysis.

In this paper, a practical simulation flow for acoustic noise analysis is proposed. The simulation flow was developed on Ansys Sherlock and Mechanical [11]. The simulation method is based on PCB vibration behavior analysis, including modal and harmonic analysis. The proposed simulation flow is demonstrated in detail in Section II. In Section III, simulation analysis of an earbud based on the simulation flow is presented. Lastly, a summary of the study is given in Section IV.

#### II. PROPOSED SIMULATION FLOW

#### A. Overview

The proposed simulation flow is shown in Fig. 2. The input files for the simulation include a board file, bill of materials (BOM) file, and a component library exported from Ansys Sherlock. The board file is imported to Ansys Sherlock directly and contains the basic information about the PCB and associated parts. The BOM file is imported to MATLAB and data processing is done afterwards. A mapping file between an internal part number and vendor part number is created in MATLAB and can be imported to Ansys Sherlock as an Approved Vendor List (AVL) file. In addition, a local library is created for the parts that are not included in the Ansys Sherlock library. After the PCB information and all part properties are updated and set properly, the Ansys Sherlock model is finished and can be transferred to the Ansys Mechanical model. Modal and harmonic analysis can then be conducted with the mechanical model.

#### B. Simulation Model Setup in Ansys Sherlock

Ansys Sherlock is a reliability physics-based engineering simulation software that provides fast and accurate life predictions for electronic hardware at the part, board and system levels in the early design stages [11]. The board (CAD) file can



Fig. 3. An example of an Approved Vendor List file.

be easily imported and transferred to Finite Element Analysis (FEA) files for Ansys Mechanical. For acoustic noise analysis, Ansys Sherlock provides an efficient way to build the simulation model.

The material density, volume and Young's modulus of the PCB and components are critical to the accuracy of the mechanical simulation [8]. Typically, the PCB and part parameters imported from a board file design are not accurate, especially for the parts. The size, weight, and material for the parts are based on the CAD file or are guessed if there is no reference, so manual checks and updates are required. The materials and properties of PCB layers can be easily edited, but it may take few days to finish building the part models as there could be hundreds of parts on a single board. The part properties could be updated from Ansys Sherlock parts library directly, however, the part name on the board has to match with the vendor's name in the library. It is not typically efficient to build and update part models manually for each board.

For these reasons, we propose to use an AVL file and local library in the simulation flow. The AVL file is used to match the internal part number with vendor part number. After importing the AVL file, the parts could be updated from Sherlock library without modifying the internal part number. Mapping information is needed to generate the AVL file, which can usually be found in the BOM file. An example of an AVL file is shown in Fig. 3. In AVL file, internal part numbers, part descriptions and vendor information are included. The AVL file considers the fact that each part could have several vendors. When the part is updated from the library, the software will search for a model from all possible vendors provided in the AVL file, and the first possible model will be applied.

The Ansys Sherlock library provides a large number of part models, however there may still be some parts that do not have models. A local library is built for these parts. The local library is particularly useful for different versions of one product, as many of the parts could be the same. When the MATLAB script generates the AVL file, it also lists all parts which do not have a model by searching the Sherlock library. The parameters of an IC in the local library are shown in Fig. 4. Most of the parameters are from the vendor datasheet, and the rest are based

ID		
	Package Name: 🧐	BGA-168
Package	Package Mount: 🥝	SMT
Electrical	Package Units: 🥝	MM
Thermal	Package Length: 🥝	2.658
Dia	Package Width: 🥹	2.658
Flag	Package Thickness: 🥝	0.64
Ball	Overmold Thickness: 📀	0.3375
User	Laminate Thickness: 🥝	0.1125
	Corner Shape: 🥹	SQUARE
	Corner Radius: 🥝	0
	Corner Face: 0	ТОР_ВОТТОМ
	Material: 🥝	LAMINATE-BGA
	Overmold Material: 🥝	OVERMOLD-BGA
	Junction Res (C/W): 🥝	
	Weight (gram): 🥝	0.1
		(2)
		(a)
	Die Units: 🥝	MM
Package	Die Length: 🥹	1 329
Electrical	Die Width: 🥑	1.329
Thermal	Die Thickness: 🥑	0.185
Pad	Die Material: 💡	
11 12		SLICON
Die	Process Node: 0	350NM PLANAR
Die Flag	Process Node: 🧿	350NM PLANAR
Flag	Process Node: 9	350NM PLANAR V (b)
Flag	Process Node: •	(b)
Die Flag	Process Node: • Ball Pattern: •	(b)
Die Flag	Process Node: • Ball Pattern: • Ball Count: •	SSONM PLANAR
ID Flag ID Package Electrical Thermal	Process Node:  Ball Pattern:  Ball Court:  Ball Units:  Ball Units:	SOUND PLANAR
ID Flag ID Package Electrical Thermal Pad	Process Node: • Ball Pattern: • Ball Count: • Ball Units: • Ball Units: •	JLCON         350NM PLANAR         •           (b)         •         •           FULL         •         •           36         •         •           0.4         •         •
ID Flag Package Electrical Thermal Pad Die	Process Node: • Ball Pattern: • Ball Count: • Ball Units: • Ball Diamete: • Ball Diamete: •	JLCON         350NM PLANAR         •           (b)         •         •           FULL         •         •           36         •         •           0.4         •         •           0.27         •         •
ID Flag ID Package Electrical Thermal Pad Die Flag	Process Node: • Ball Pattern: • Ball Count: • Ball Units: • Ball Diameter: • Ball Diameter: • Ball Diameter: •	JLCON         350NM PLANAR         •           (b)         •         •           FULL         •         •           36         •         •           0.4         •         •           0.27         •         •           0.216         •         •
Die Flag	Process Node: • Ball Pattern: • Ball Count: • Ball Units: • Ball Diameter: • Ball Diameter: • Ball Package Diameter: •	JLCON         350NM PLANAR         •           (b)         •         •           FULL         •         •           36         •         •           0.4         •         •           0.27         •         •           0.216         •         •
Die Flag	Process Node: • Ball Pattern: • Ball Count: • Ball Units: • Ball Diameter: • Ball Diameter: • Ball Package Diameter: • Ball Pad Diameter: • Ball Pad Diameter: •	JLCON         350NM PLANAR         •           (b)         •         •           FULL         •         •           36         •         •           MM         •         •           0.4         •         •           0.27         •         •           0.216         •         •           0.19         •         •
Die Flag	Process Node: • Ball Pattern: • Ball Count: • Ball Diate: • Ball Diameter: • Ball Danmeter: • Ball Package Diameter: • Ball Pad Diameter: • Ball Pad Diameter: • Ball Height: •	JLCON         350NM PLANAR         •           (b)         •         •           FULL         •         •           36         •         •           MM         •         •           0.4         •         •           0.27         •         •           0.216         •         •           0.19         •         •
Die Flag	Process Node: • Ball Pattern: • Ball Count: • Ball Unit: • Ball Pitch: • Ball Pitch: • Ball Package Diameter: •	JLICON         Image: Solid state
Die Flag	Process Node: • Ball Pattern: • Ball Count: • Ball Units: • Ball Pich: • Ball Package Diameter: • Ball Chan Width: • Ball Material: •	JLICON         Image: Solid state
Die Flag	Process Node: • Ball Patterr: • Ball Court: • Ball Units: • Ball Pich: • Ball Package Diameter: • Ball Perimeter Rows: • Ball Perimeter Cols: •	JLICON       350NM PLANAR       (b)       FULL       36       MM       0.4       0.27       0.216       0.216       0.216       0.19       635N37PB       6       6
Die Flag	Process Node: • Ball Pattern: • Ball Count: • Ball Units: • Ball Pich: • Ball Package Diameter: • Ball Pall Material: • Ball Perimeter Rows: • Ball Perimeter Cols: •	JLICON       350NM PLANAR       (b)       FULL       36       MM       0.4       0.27       0.216       0.216       0.216       0.216       0.19       63SN37PB       6       6

Fig. 4. An IC model built in the local library. (a) Package information. (b) Die information. (c) Solder ball information.

on recommendations and built-in guidelines, including the die size and the solder ball material.

It only takes a few hours to finish the parts modeling using the proposed AVL file and local library, instead of few days for each board using the conventional approach. The simulation analysis for acoustic noise is more practical and can be easily applied early in the design process.

#### C. Simulation Model Setup in Ansys Mechanical

After the parameters of the PCB and all of the parts are updated, the model is exported to Ansys Mechanical. It is worth noting that all parts are modeled as rectangular blocks for simplicity. As a result, complex mechanical structures may need to be imported to Ansys Mechanical directly. In practice, the PCB is usually fixed to a housing or other structure at several positions, so fixed supports should be added in the model. The fixed supports are also the boundary conditions for modal analysis. After finishing the simulation model in Ansys



Fig. 5. Ansys Mechanical model.

Mechanical, the PCB vibration properties and the impact of the MLCCs on acoustic noise can be studied.

#### **III. SIMUALTION ANALYSIS EXAMPLE**

#### A. DUT Introduction and Simulation Setup

The acoustic noise from an earbud was analyzed using the proposed simulation flow. The PCB in the DUT had 8 layers and 150 parts in total. There were 55 unique parts, and 32 unique part models had been built in the local library. Based on the proposed method, it took only 5 hours to build the Sherlock model. The orientations of some parts had to be corrected before exporting to the FEA mechanical model.

The mechanical model is shown in Fig. 5. On the PCB there is a spring finger which cannot be presented and modeled accurately in Ansys Sherlock. The 3D .step file of the spring finger was therefore imported to Ansys Mechanical directly. As the spring finger is not a rigid structure, additional natural frequencies of the structure are expected. Since the PCB was fixed to the housing at 4 different positions, 4 fixed supports were added on the side surface at similar positions within the simulation model.

#### B. Modal Analysis and Harmonic Analysis

The natural frequencies of the first eight modes found through modal analysis are shown in Table I. The model shapes of the first two modes are shown in Fig. 6. The first natural frequency is 5980.6 Hz, which is related to the spring finger, as shown by the large deformation area located only at the tip of the spring finger in the first modal shape. The second natural frequency is about 8045.4Hz, which is related to the vibration of the PCB. The modal analysis can be used to estimate the inherit vibration properties of the whole structure. The modal shape results can similarly be used to find the locations where the board is most sensitive to external vibrational forces.

Based on the modal analysis, the harmonic response of the structure can be analyzed using the mode superposition method. Since the MLCC is the source of the PCB variation, the external force is added at the MLCC in the simulation model, as shown in Fig. 7. The total deformation of the structure under the external force is simulated as shown in Fig. 8. The total deformation is defined as the maximum deformation for the whole structure (include PCB and all components) at different frequencies, which can be considered as the frequency response of the DUT. The simulation frequency is from 100 Hz to 20 kHz





Fig. 6. Modal shapes. (a) Mode 1. (b) Mode 2.

TABLE I.MODAL FREQUENCY OF THE PCB

Mode	Frequency [Hz]
1	5980.6
2	8045.4
3	11187
4	12488
5	13885
6	20305
7	28162
8	29516

and the amplitude is plotted in decibels. The structure tends to vibrate most under the action of external forces at resonant frequencies. The resonant frequencies match with the natural frequencies as expected.

The inherent vibration properties and the frequency response of the structure can be estimated from the modal analysis and harmonic analysis results. This information is useful for engineers trying to understand how acoustic noise may be induced by MLCCs. For this DUT, the model setup time (build from the existing library) and the computational resources required are given in Table II. It shows that the simulation analysis for acoustic noise is practical and can be easily applied in the early stages of design.

#### IV. CONCLUSION

A practical simulation flow for singing-capacitor-based acoustic noise was presented in this paper. The simulation modeling and analysis were developed using Ansys Sherlock and Mechanical. Use of an AVL file and local library was proposed to speed up the development of the simulation models. Modal analysis and harmonic analysis can be used to estimate



Fig. 7. External force is added on the MLCC as shown with the red arrow.



Fig. 8. Total deformation of the structure.

TABLE II. RESOURCE CONSUMPTION

Model setup time	About 5 hours
Simulation time	About 1 hour
CPU cores	4
Memory Usage	About 30 GB

the inherent vibration properties and the frequency response of the structure. An example of simulation analysis was given to demonstrate the proposed method. The vibration properties of the spring finger and the PCB were simulated successfully, and the frequency response of the whole structure was estimated. The proposed simulation flow makes simulation analysis of acoustic noise practical and effective.

#### REFERENCES

- [1] F. de Paulis, R. Cecchetti, C. Olivieri and M. Buecker, "Genetic Algorithm PDN Optimization based on Minimum Number of Decoupling Capacitors Applied to Arbitrary Target Impedance," 2020 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI), 2020, pp. 428-433.
- [2] L. Zhang, Z. Zhang, C. Huang, H. Deng, H. Lin, B. Tseng, J. Drewniak, and C. Hwang, "Decoupling Capacitor Selection Algorithm for PDN Based on Deep Reinforcement Learning," 2019 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+SIPI), 2019, pp. 616-620.
- [3] B. Zhao, S. Liang, S. Connor, M. Cocchini, B. Achkir, A. Ruehli, B. Archambeault, J. Fan and J. Drewniak, "Decoupling capacitor power ground via layout analysis for multi-layered PCB PDNs," in *IEEE Electromagnetic Compatibility Magazine*, vol. 9, no. 3, pp. 84-94, 3rd Quarter 2020.

- [4] J.D. Prymak, "Piezoelectric effects ceramic chip capacitors (singing capacitors)." Arrow Asian Times, 2006.
- [5] [Online]. Available: https://product.tdk.com/system/files/contents/faq/ca pacitors-0031/singing\_capacitors\_piezoelectric\_effect.pdf
- [6] B.H. Ko, S.G. Jeong, Y.G. Ahn, K.S. Park, N.C. Park, and Y.P. Park, "Analysis of the correlation between acoustic noise and vibration generated by a multi-layer ceramic capacitor," *Microsyst. Technol.*, vol. 20, no. 8-9, pp.1671-1677, Aug. 2014.
- [7] Y. Sun, J. Zhang, Z. Yang, C. Hwang and S. Wu, "Simulation Investigation on Acoustic Noise Caused by "Singing" Capacitors on Mobile Devices," 2019 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+SIPI), 2019, pp. 406-410.
- [8] Y. Sun, S. Wu, J. Zhang, C. Hwang and Z. Yang, "Simulation Methodologies for Acoustic Noise Induced by Multilayer Ceramic Capacitors of Power Distribution Network in Mobile Systems," in *IEEE*

Transactions on Electromagnetic Compatibility, vol. 63, no. 2, pp. 589-597, April 2021.

- [9] Y. Sun, J. Zhang, Z. Yang, C. Hwang and S. Wu, "Measurement Investigation on Acoustic Noise Caused by "Singing" Capacitors on Mobile Devices," 2019 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+SIPI), 2019, pp. 505-510.
- [10] Y. Sun, S. Wu, J. Zhang, C. Hwang and Z. Yang, "Measurement Methodologies for Acoustic Noise Induced by Multilayer Ceramic Capacitors of Power Distribution Network in Mobile Systems," in *IEEE Transactions on Electromagnetic Compatibility*, vol. 62, no. 4, pp. 1515-1523, Aug. 2020.
- [11] [Online]. Available: https://www.ansys.com/products/structures