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Junho Joo

Soumya Singh

P. K. Seema

Chulsoon Hwang
Missouri University of Science and Technology, hwangc@mst.edu

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/4685

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Analysis of Switching Voltage Regulator Noise Coupling to a High-Speed Signal

Junho Joo[#1], Soumya Singh[*2], Seema PK[*3], Chulsoon Hwang [#4], Bhyrav Mutnury[**5], and James Drewniak[#6]

[#]*EMC Laboratory,* Missouri University of Science and Technology, Rolla, Mo, USA
[1]jooju, [4]hwangc, [6]drewniak@mst.edu
[*]*Dell, Enterprise Product Group, Bagmane Parin, Bagmane Tech Park, Bangalore, KA, India*
[**]*Dell, Enterprise Product Group, One Dell Way, MS RR5-31, Round Rock, TX, USA*

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***Abstract*— In this paper, a real-world signal and power integrity problem due to the switching noise of buck converter IC coupling to a high-speed signal line in a server system is studied. The rapid switching field effect transistors (FETs) of the voltage regulator module (VRM) are the main source of the performance degradation on the nearby signal lines. A simplified mock-up simulation setup is proposed based on the actual board design to investigate the coupling mechanism of the VRM noise. The mechanism of the switching noise coupling is explained with the phenomenon of capacitive and inductive coupling. Based on this finding, the solutions will be identified as decreasing the inductive coupling by optimizing the board layout.**

Keywords— voltage regulator module noise coupling; switching FETs; capacitive coupling; inductive coupling; board layout

I. INTRODUCTION

In server systems we use multiphase buck converters to provide stabilized power to CPU, RAM and other devices [1]. However, unwanted high-frequency noise can be generated by the switching nature of voltage regulator modules (VRMs). The upper/lower side field effect transistors (FETs) of VRMs in each phase are switched on and off alternately resulting in the ringing voltages at the transition edges of voltage and current due to the package and interconnection parasitics [2]. The frequency of power noise can be as high as few hundreds of MHz that can be coupled to other devices easily.

In recent studies, the switching power noise coupling is reproduced by extracting S-parameters using full-wave simulation [3-5]. The S_{21} of VRM power vias to signal vias is usually extracted to describe the coupling problems. Typically, many vias are arranged on the VRM power shape, the via-to-via coupling was the main source of the signal degradation in [4]. In addition, the power noise coupling between horizontal power shape and penetrating vias was studied and validated with measurement [5]. However, the coupling mechanism of power switching noise to the transmission line is still opaque.

In actual design, engineers take extra care of signal VIAs since they are vulnerable to noise coupling. As a result, the signal VIAs are located far away from the noisy VRM, but traces are still routed around the noisy power shapes to meet the small form factor of PCB. Therefore, the VRM noise coupling to traces in electrically small condition may be created in the server systems. In order to mitigate the power noise coupling, a rigorous investigation of VRM noise coupling to the nearby transmission line is required.

In this paper, VRM noise coupling to high-speed traces is studied. The simplified mock-up test case is proposed based on the actual board design for server systems. The noise generated by the switching nature of VRM is reproduced with reduced order macro-model for buck converter consisting of linear RLC component. In the circuit simulator, power noise is injected to the extracted S-parameter of mock-up test setup and then coupled voltage on the transmission line is analyzed. The coupled voltages are described by near-end crosstalk (NEXT) and far-end crosstalk (FEXT) based on the inductive and capacitive coupling.

II. POWER SWITCHING NOISE ISSUE IN SERVER SYSTEM

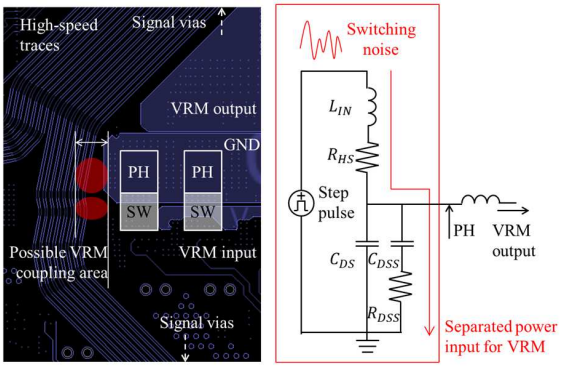


Fig. 1. (a) board layout of server system (b) equivalent circuit model of VRM generating switching noise

To better understand the power noise coupling in electronic devices, the VRM switching noise is introduced here briefly. Fig. 1(a) shows the board design of the server system with the multiphase VRM and high-speed traces. The SW and PH denote the FET switches and phase nodes, respectively. Since the traces are passing by the switches of VRM, the switching noise can be easily coupled. The equivalent circuit model of VRM generating the high-frequency switching noise is shown in Fig. 1(b). This circuit can reproduce the switching noise during the turn-on transition of high-side MOSFET. L_{IN} and R_{HS} denote that input parasitic inductance and turn-on resistance of high-side

MOSFET, respectively. Since the low-side FET is turned off during the turn-on period, it can be replaced by the combination of capacitors and resistors that describe the body diode C_{DS} and package parasitic R_{DSS} and C_{DSS}. The parameters extraction and fitting method is illustrated in Fig. 2.

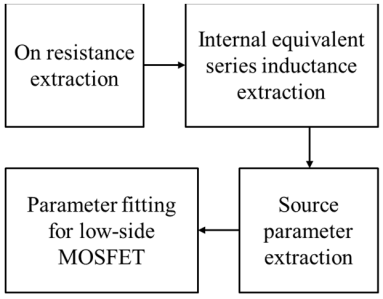


Fig. 2. Parameter fitting flow for equivalent circuit model

For the on resistances of both high- and low-side MOSFETs can be found from tis datasheet. Since the noise is generated due to the resonance of RLC circuit, the input inductance L_{in} can be extracted from its ringing frequency. The ringing frequency can be calculated by adding an additional external inductance between voltage source and L_{in}. With the two different external inductances, the L_{in} can be solved by eliminating total capacitance by comparing two different ringing frequencies. Once the internal inductance is determined, the rise time of buck converter can be extracted from the voltage waveform of turn-on transition of switching node. Finally, the total capacitances of low-side MOSFET can be fine-tuned with fixed on resistance, internal inductance and rise time of voltage source. With the equivalent circuit model, switching noise with hundreds of MHz of ringing frequency can be generated. To investigate the coupling mechanism of VRM noise to traces, the S-parameter extraction with full-wave simulation can be performed. However, the simulation with the entire board in the server system consumes tremendous resources makes this method unattractive.

A. Proposed Mock-up Test Case

To overcome the inefficiency of full-wave simulation, a simplified setup is proposed by clipping the board area around the SW node in Fig. 1(a). The simplified mock-up test case is proposed in high-frequency structure simulator (HFSS) as shown in Fig. 3. The test case consists of 4 layers as PWR-GND-GND-PWR, and ports for input voltage and equivalent buck model are assigned between power (PWR) and ground (GND) planes on the bottom layer. The power shapes and GND planes on each layer are connected by through hole vias (THVs). For the simplicity of simulation, dielectric heights of all layers are fixed as 0.5 mm and thickness of conductor is 0.035 mm. On the top layer, 8.7 mm long microstrip line with 50Ω termination on each edge is placed 1 mm away from the power shape. At first, to understand the noise coupling path surface current distribution and field generation simulations are performed.

The main current path created by input voltage will be focused on the below layers with VRM input port. However, due to the vias arranged on the PWR and GND shapes, the current can leak on the bottom surface of the top layer and the top surface of the second layer. Especially in this layer stackup, the surface current tends to return through the antipads for VRM vias. The vector of leakage current of y-direction on the PWR and GND layers is shown in Fig. 4. Among the current vectors on the surfaces, the current vector nearby the microstrip is highlighted in blue and red arrows. Since the microstrip is placed along with the PWR shape, the current in the y-direction can inject the noise on the trace inductively. Among the highlighted arrows, the blue arrows have opposite directions compared to the current vector on the entire board. Due to this opposite behavior of surface current, the opposite directions H-fields can be created around the one edge of PWR shape.

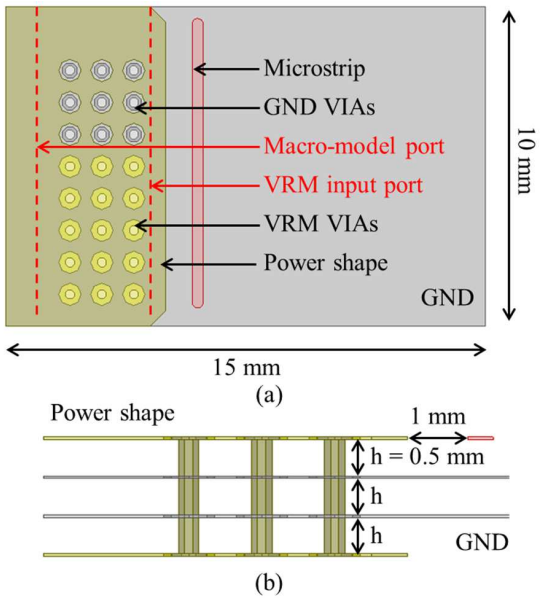


Fig. 3. Proposed mock-up test case with microstrip line. (a) top view (b) cross-sectional view

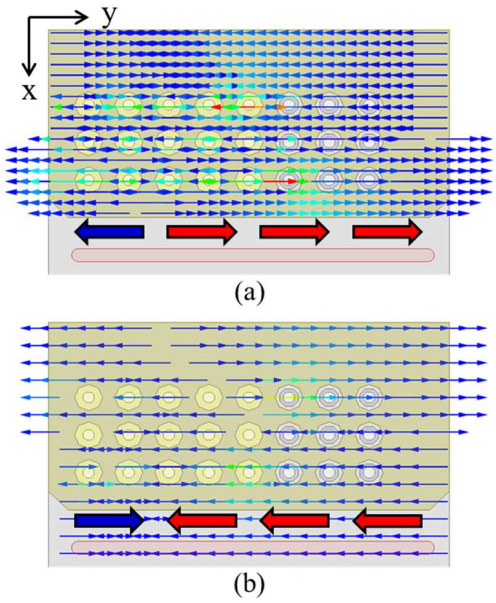
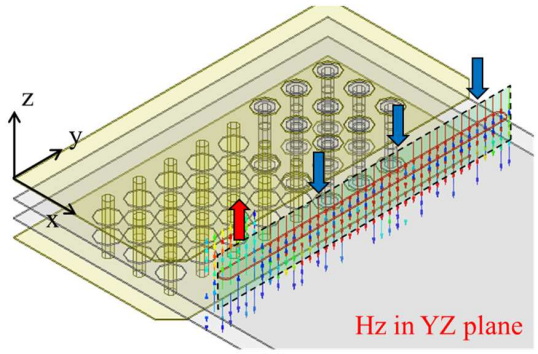
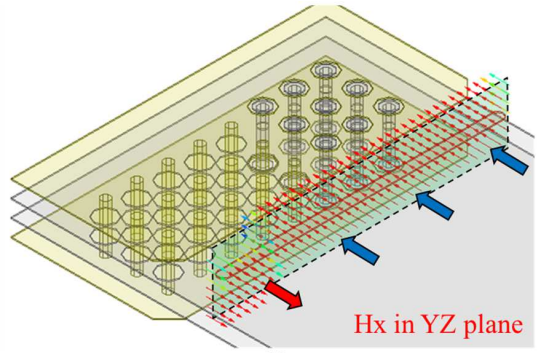


Fig. 4. Simulated surface current distribution. (a) bottom surface of top layer (b) top surface of second layer



(a)



(b)

Fig. 5. Simulated H-fields distributions. (a) Hz in YZ plane (b) Hx in YZ plane

To visualize the inductive coupling in mock-up test case, the H-fields around microstrip line are plotted as shown in Fig. 5. Hx and Hz-fields that can inject the current to the microstrip in full-wave simulation show the opposite direction on the left-hand side of VRM vias. In this case, the mutual inductance created by the surface current can induce noise current onto a quiet trace within close enough proximity. Based on the simulation results, the antipads of power vias on GND layer and PWR vias on power shape can generate return surface current resulting in VRM shape related inductive coupling to the traces.

B. Analysis of Coupled Voltages

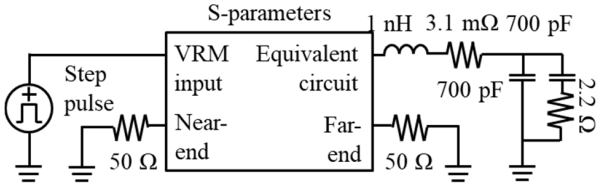
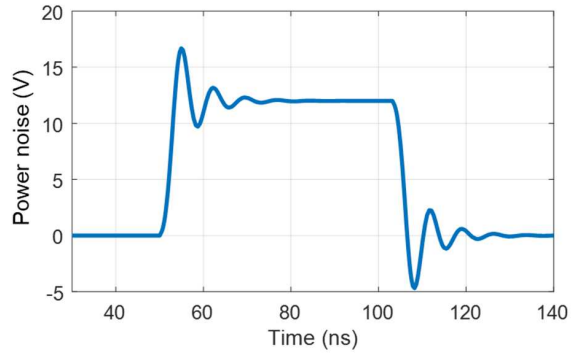
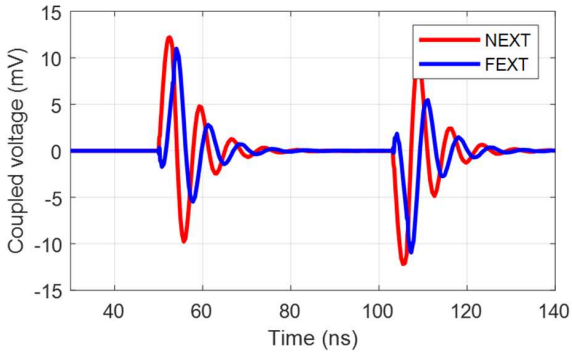


Fig. 6. Transient simulation setup.

The VRM noise coupling to transmission line is simulated using the circuit simulator of ANSYS with the setup shown in Fig. 6. The switching noise behavior model in Fig. 1(b) is connected to the S-parameters extracted from a simplified mock-up test case. A 12 V step input with 3.1 ns of rising time and 50 ns of pulse width is applied. The simulated power noise and coupled voltages on the microstrip line are shown in Fig. 7. The 160 MHz switching noise is generated on the VRM power shape, and it is dissipated by the RLC circuits. In the meantime, the noise voltage that correlated with the power noise is obtained on each 50Ω termination. The wavelength of switching noise and trace length are 900 mm and 8.7 mm, respectively. Since the wavelength is greater than trace length, it is under the electrically small condition. Even though the 3D simulation setup was in the electrically small condition, the coupled noise voltages on each termination has variations in both phase and magnitude. Those variations can be described by the inductive and capacitive coupling as follows [6]:



(a)



(b)

Fig. 7. Transient voltage waveforms. (a) switching noise on PWR shape (b) coupled noise voltage on near- and far-end

$$V_{NE}(t) = l\frac{R_{NE}}{R_{NE}+R_{FE}}l_{21}\frac{di_1}{dt} + l\frac{R_{NE}R_{FE}}{R_{NE}+R_{FE}}c_{21}\frac{dv_1}{dt}$$
$$V_{FE}(t) = -l\frac{R_{NE}}{R_{NE}+R_{FE}}l_{21}\frac{di_1}{dt} + l\frac{R_{NE}R_{FE}}{R_{NE}+R_{FE}}c_{21}\frac{dv_1}{dt} \quad (1)$$

$V_{NE}(t)$ and $V_{FE}(t)$ describe the NEXT and FEXT, respectively where l_{21}, c_{21} are the mutual inductance and capacitance per unit length, l is the length of the trace, and i_1, v_1 are the current and voltage on the VRM power distribution network (PDN). R_{NE} and R_{FE} denote the terminations of near- and far-end of the victim microstrip line. In the voltage expressions, di/dt and dv/dt denote the inductive and capacitive coupling. Since the inductive coupling has opposite polarity in the FEXT, the phase and magnitude variation can be created. To double confirm the inductive/capacitive coupling and validity of the mock-up test case, the different equations extracting each coupling are compared.

$$\frac{V_{NE}(t) - V_{FE}(t)}{2} = V_{NE}(t) - V_{open-load}(t) \quad (2)$$

$$\frac{V_{NE}(t) + V_{FE}(t)}{2} = V_{open-load}(t) \quad (3)$$

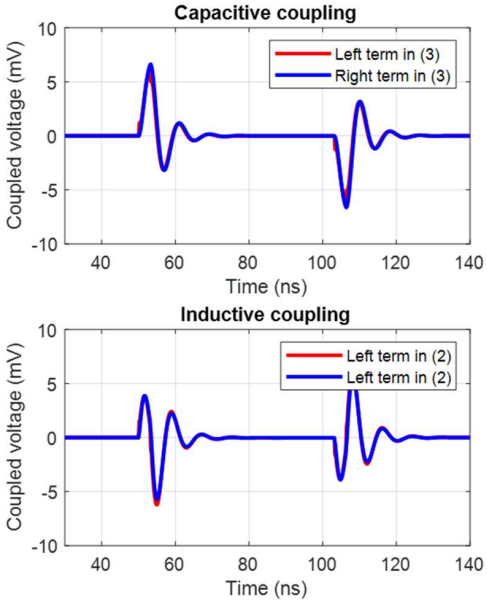


Fig. 8. Comparison of analytical expressions.

In both (2) and (3), the left terms describe inductive and capacitive coupling based on the known equation (1), and the right terms denote the inductive and capacitive coupling extracted from the revised 3D model to double confirm the validity of the mock-up test case. In (2), the left term can be calculated by using the NEXT and FEXT shown in Fig. 7(b). By subtracting the FEXT from NEXT, the coupled voltage due to the inductive coupling can be extracted based on the known equation (1). To obtain $V_{open-load}(t)$ in (2), the full wave simulation model is revised. By removing the macro-model port in Fig. 3(a) to eliminate the inductive coupling source, the coupled voltage due to the capacitive coupling can be simulated. Thus, the right term in (2) denotes the coupled voltage caused by inductive coupling. For the capacitive coupling extraction, the same method is applied in (3). The comparison results are shown in Fig. 8. A good agreement between the known analytical expression (1) and mock-up test case supports that the VRM noise coupling to the transmission line could be described by the NEXT and FEXT based on inductive/capacitive coupling.

III. S/H Ratio Comparisons

For the analysis of VRM to trace noise coupling in the server platform design, the coupled voltage depending on the *S/H* ratio is simulated. The *S/H* ratio is usually used to describe the coupled voltage depending on the function of geometry where *S* and *H* are the trace-to-trace distance and dielectric height, respectively. As the VRM noise coupling to trace can be described by near- and far-end crosstalk, the *S/H* ratio comparison between power shape and trace is applicable. In this case, the single-ended crosstalk coefficient separated by distance *S* is as follows [7]:

$$C = \frac{k}{1 + (S/H)^2} \quad (4)$$

where k is a proportionality constant which is related to other parameters such as signal rise time, transfer function, permeability, etc. Thus, the coupled voltage on the victim trace must be the same when the value of k and *S/H* ratio are maintained. In two coupled line case, the coupling coefficient *C* is dominated by the inductive coupling, and it has a negative value since inductive coupling injects the opposite polarity of the coupled voltage on the far-end side. By comparing the coupled voltages with different *S/H* ratios for various *H*, the VRM noise coupling to the transmission line depending on the PCB design can be discussed. For the comparison of coupled voltage, 2.3, 5, and 9 mil of dielectric heights are applied to the mock-up test case and the total thickness is fixed to 64 mil. After extractions of S-parameters with different geometries, the transient setup in Fig. 6 with a sinusoidal voltage source and a 1Ω resistor is applied to VRM input and equivalent circuit ports for the simplicity of analysis. The frequency of sinusoidal source is 160 MHz which is identical with the noise frequency in Fig. 7.

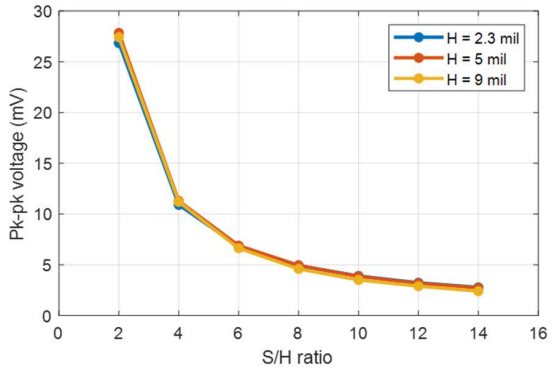


Fig. 9. Coupled voltage depending on S/H ratio.

The coupled voltage comparison results are shown in Fig. 9. Even though the distance between power shape and traces is different, the same amount of voltage is coupled when *S/H* ratios are the same. All simulation setups show the large voltage drop when distance increased from 2H to 4H, and begins to saturate after 8H. Typically, power-related signal integrity design guidelines recommend routing traces at least 8H away from the noisy VRM shapes. The above simulation results using the mock-up test case clearly show that the VRM noise coupling to the transmission line can be dramatically reduced by following the design rules. In addition, it is confirmed that the noise coupling from VRM to trace can be described by the crosstalk based on the inductive/capacitive coupling.

IV. Conclusion

In this paper, the VRM noise coupling to the microstrip is studied. A simplified mock-up test case is proposed based on the actual board design. On the surface of PWR and GND planes, the leakage current generates the H-fields on the one edge of the microstrip. Due to the H-fields, the inductive coupling is created resulting in the magnitude/phase variations of coupled voltage

on the microstrip in the electrically small condition. Each coupling mechanism is extracted based on the analytic expressions. To further validate the voltage coupling, the coupled voltage depending on the *S/H* ratio is simulated. With the simulation results, it is validated that the VRM noise coupling to the transmission line can be described by inductive/capacitive coupling.

REFERENCES

[1] A. I. Pressman, "Switching Power Supply Design", 2nd Edition, McGraw-Hill, 1998, pp. 413 – 426.

[2] K. W. Kam, D. Pommerenke, C.-W. Lam and R. Steinfeld, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis," *in Proc. IEEE Int. Symp. Electromagn. Compat.*, Detroit, MI, USA, 2008, pp. 1-7.

[3] Y. Wu, Z. Ji, J. Wang and W. Ma, "Noise Coupling Analysis for High Speed Differential Trace Crossing Switching Voltage Regulator Area," *in Proc. IEEE Int. Symp. Electromagn. Compat. and Asis-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC)*, Singapole, 2018, pp. 12-17.

[4] G. Ouyang, X. Ye, and T.-T. Nguyen, "Switching Voltage Regulator Noise Coupling to Signal Lines in a Server System," *in Proc. IEEE Int. Symp. Electromagn. Compat.*, Jul. 2010, pp. 72–78.

[5] H. Lin, B.C. Tseng, J. Yen, "Effect of Power Noise Coupling between Power Via and Signal Via and its Relationship with Distance," *in Proc. IEEE Int. Symp. Electromagn. Compat.*, 2016.

[6] C. R. Paul, Introduction to Electromagnetic Compatibility, 2nd ed., New York, NY, USA: Wiley-Interscience, 2006.

[7] V. Ungvichian and M. B. Kopp, "Crosstalk in Coupled Microstrip Lines due to Substrate Permittivity and S/H Ratios," *in Proc IEEE Southcon*, 1993, pp. 301-304.