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An Interleaved High Step-Up DC-DC Converter with Coupled Inductor and Built-in Transformer for Renewable Energy Applications

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***Abstract*—This paper introduces an interleaved high step-up DC-DC converter with high voltage gain, low voltage stresses on the switches, low current stresses on the components, and continuous input current with low ripple, all of which are beneficial for the renewable energy (RE) applications. The proposed converter is based on the integration of three voltage-boosting (VB) methods: coupled inductor (CI), built-in transformer (BIT), and switched-capacitor (SC) cells. The energies of the leakage inductances of the CIs and BIT are absorbed and recirculated to the output side, which further extends the voltage gain. In addition, the current-falling rates of the diodes are controlled by the leakage inductances, which leads to the reduced reverse-recovery losses of the diodes. The operating stages, steady-state analysis, and a comparison with similar existing topologies are presented in this paper. Furthermore, the performance of the proposed converter is verified through the experimental results of a 200-W prototype with an output voltage of 400 V and a voltage gain of 30.**

***Keywords*—High step-up DC-DC converter, high voltage gain, coupled inductor, built-in transformer, switched-capacitor, photovoltaic, fuel cell, renewable energy.**

I. INTRODUCTION

Due to the reduction of the fossil fuels and importance of the environmental protection, the adoption of the renewable energy (RE) resources, such as solar photovoltaic (PV) panels and fuel cells (FCs), has recently increased rapidly. However, the output voltage of the RE resources is relatively low; accordingly, they need a high step-up DC–DC converter to lift their low voltages that is about 10-50 V to a high voltage that is about 380-400 V [1, 2]. The conventional DC-DC boost converter can achieve a high voltage gain with a very high duty cycle close to 1, which leads to the problems that are high voltage and current stresses on the switch and output diode, severe reverse-recovery problem of the output diode, large current ripple of the input boost inductor, and high voltage ripple of the output capacitor [3, 4]. To overcome these issues, many high step-up DC-DC converters have been introduced that can achieve high voltage gains under low or medium duty cycles using the voltage-boosting (VB) methods [5]. The first VB method is cascading conventional DC-DC boost-based converters. Adopting the switched-capacitor (SC)/switched-inductor (SL) cells is the second VB method [6-8], which is based on charging the capacitors/inductors in parallel and discharging them in series during a switching period. The first and second VB methods have low efficiency with increased cost and complexity due to the utilization of many components. Another major problem with the high step-up DC-DC SC-based converters is that they suffer from high inrush/transient currents due the presence of the capacitors [9]. These problems can be overcome by the third VB method that is based on the integration of the coupled inductor (CI) and/or built-in transformer (BIT) with the SC cells. Using the CI and BIT, the degrees of freedom for the converter design increase because the voltage gain can be adjusted by their turns-ratios in addition to the duty cycle of the switch(es) [10]. The high-efficiency DC-DC converters in [11-15] are based on the integration of the CI, BIT, and SC cells in interleaved structures, which can reach high voltage gains without extremely high duty cycles and with reduced voltage stresses on the switches. Additionally, due to the interleaved structure, the input current ripple and currents stresses of the components are low for the converters in [11-15]. Moreover, the leakage inductances of the CI and BIT lead to the reduced reverse-recovery losses of the diodes.

In this paper, a high step-up DC-DC converter is proposed, which is based on integrating two CIs and one BIT with SC cells. Also, the proposed converter has an interleaved structure resulting in the low current stresses on the components and reduced input current ripple. The voltage gain of the proposed converter is adjusted by three parameters that are the turns-ratio of the CIs, turns-ratio of the BIT, and duty cycle of the switches. Due to the existence of the leakage inductances of the CIs and BIT, all diodes turn off under the zero-current switching (ZCS) conditions; accordingly, the revere-recovery problem of the diodes is alleviated. In addition, the voltage stresses on the switches are far less than the output voltage, leading to the selection of the MOSFETs with low voltage ratings and low ON-state resistances, which contributes to the reduced power losses and improved power efficiency of the proposed converter. The circuit diagram of the proposed converter, operating stages, steady-state analysis, comparative study, experimental results, and conclusion are presented in the following sections.

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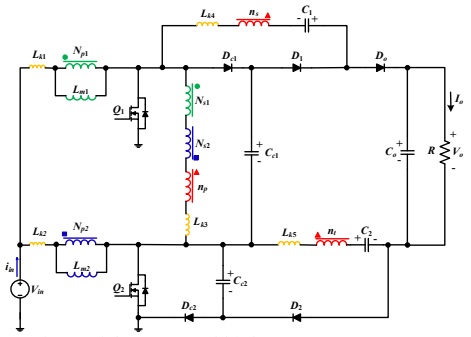

Fig. 1. The topology of the proposed high step-up DC-DC converter.

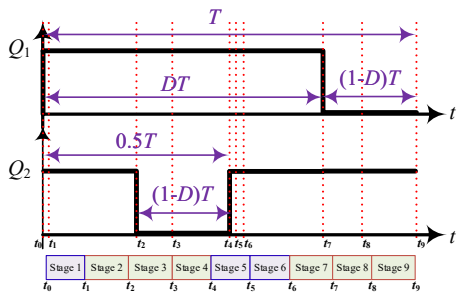

Fig. 2. The switching pattern of the proposed DC-DC converter.

I. Topology and Operating Stages of Proposed Converter

Fig. 1 illustrates the topology of the proposed high step-up DC-DC converter, which has an interleaved structure with two CIs and one BIT—both of which are combined with the SC cells to extend the voltage gain. Parameters L_{k1}, L_{k2}, L_{k3}, L_{k4}, and L_{k5} represent the leakage inductances of the CIs and BIT; L_{m1} and L_{m2} represent the magnetizing inductances of the CIs (CI1 and CI2) and act as the boost inductors. There are two switches (Q_1 and Q_2), five diodes (D_{c1}, D_{c2}, D_1, D_2, D_o), and five capacitors (C_{c1}, C_{c2}, C_1, C_2, C_o). The input RE resource and output load are represented by V_{in} and R, respectively. The diode-capacitor pairs D_{c1}-C_{c1} and D_{c2}-C_{c2} act as the passive lossless clamps to absorb the energy stored in the leakage inductances and limit the voltage stresses on the switches; also, they contribute to the further extension of the voltage gain. For the proposed converter to operate normally in the continuous conduction mode (CCM), switches Q_1 and Q_2 operate at 180º out of phase from each other with a duty cycle greater than 0.5. The switching pattern of the proposed converter is depicted in Fig. 2; as seen, there are 9 operating stages, and Figs. 3(a)-(i) show the equivalent circuits of the proposed converter for all operating stages as described below.

Stage 1 (Fig. 3(a), $t_0 \le t \le t_1$): This operating stage starts when switch Q_1 turns on at $t=t_0$ and ends when output diode D_o turns off naturally under ZCS condition at $t=t_1$. This stage is transitional with a very short duration.

Stage 2 (Fig. 3(b), $t_1 \le t \le t_2$): When output diode D_o turns off at $t=t_1$, Stage 2 begins and the primary windings of both CIs are still energized by the input voltage source, while the load is supplied by output capacitor.

Stage 3 (Fig. 3(c), $t_2 \le t \le t_3$): This stage begins at $t=t_2$ in which switch Q_2 turns off and diodes D_1, D_2, and D_{c2} are forward-biased. In this stage, the clamp capacitor C_{c2} is charged and its voltage is equal to the voltage across switch Q_2. At the beginning of this stage, the primary winding of CI2 starts to be de-energized and its secondary winding transfers the energy indirectly to capacitors C_1 and C_2 to charge them.

Stage 4 (Fig. 3(d), $t_3 \le t \le t_4$): At $t=t_3$, Stage 4 starts when clamp diode D_{c2} turns off smoothly under the ZCS condition. During this stage, the primary windings of CI1 and CI2 continue to be energized and de-energized, respectively.

Stage 5 (Fig. 3(e), $t_4 \le t \le t_5$): At $t=t_4$, switch Q_2 turns on and Stage 5 starts. This stage is a very short transitional stage and ends when diode D_1 turns off at $t=t_5$.

Stage 6 (Fig. 3(f), $t_5 \le t \le t_6$): Like Stage 5, Stage 6 is transitional with a very short duration, starting at $t=t_5$ and ending when diode D_2 turns off at $t=t_6$.

Stage 7 (Fig. 3(g), $t_6 \le t \le t_7$): This stage is the same as Stage 2, during which both switches are ON and all diodes are OFF.

Stage 8 (Fig. 3(h), $t_7 \le t \le t_8$): At $t=t_7$, switch Q_1 turns off and its voltage is limited to the voltage of clamp capacitor C_{c1}. CI1 starts to be de-energized, and the output diode turns on to transfer the energy to the output side.

Stage 9 (Fig. 3(i), $t_8 \le t \le t_9$): At $t=t_8$, Stage 9 starts when clamp diode D_{c1} turns off smoothly with the ZCS condition. This operating stage continues until switch Q_1 turns on again at $t=t_9$.

II. Steady-State Analysis of Proposed Converter

To simplify the steady-state analysis of the proposed converter, the leakage inductances of the CIs and BIT are ignored; accordingly, the transitional operating Stages 1, 5 and, 6 are ignored. Also, the capacitors' voltages are supposed to be constant during the whole switching cycle (T). Moreover, the turns-ratios of the CIs and BIT are defined as $N=N_{s1}/N_{p1}=N_{s2}/N_{p2}$ and $n=n_s/n_p=n_t/n_p$, respectively.

A. Voltages of Capacitors and Voltage Gain

Applying the volt-second balance principle to the magnetizing inductances L_{m1} and L_{m2}, the capacitors' voltages are obtained as:

$$V_{C_{c1}} = V_{C_{c2}} = \frac{1}{1-D} V_{in} \tag{1}$$

$$V_{C_1} = \frac{2+n(1+N)}{1-D} V_{in} \tag{2}$$

$$V_{C_2} = \frac{1+n(1+N)}{1-D} V_{in} \tag{3}$$

$$V_o = \frac{4+4n(1+N)}{1-D} V_{in} \tag{4}$$

The voltage gain is extracted as in (5); as obvious, the voltage gain is adjusted by three independent parameters of N, n, and D, which increases the design flexibility of the proposed converter. Also, due to the connection of the secondary windings of the CIs in series with the primary winding of the BIT, the voltage gain is proportional to the product of the turns-ratios of the CIs and BIT, thus leading to the ultra-high voltage gains

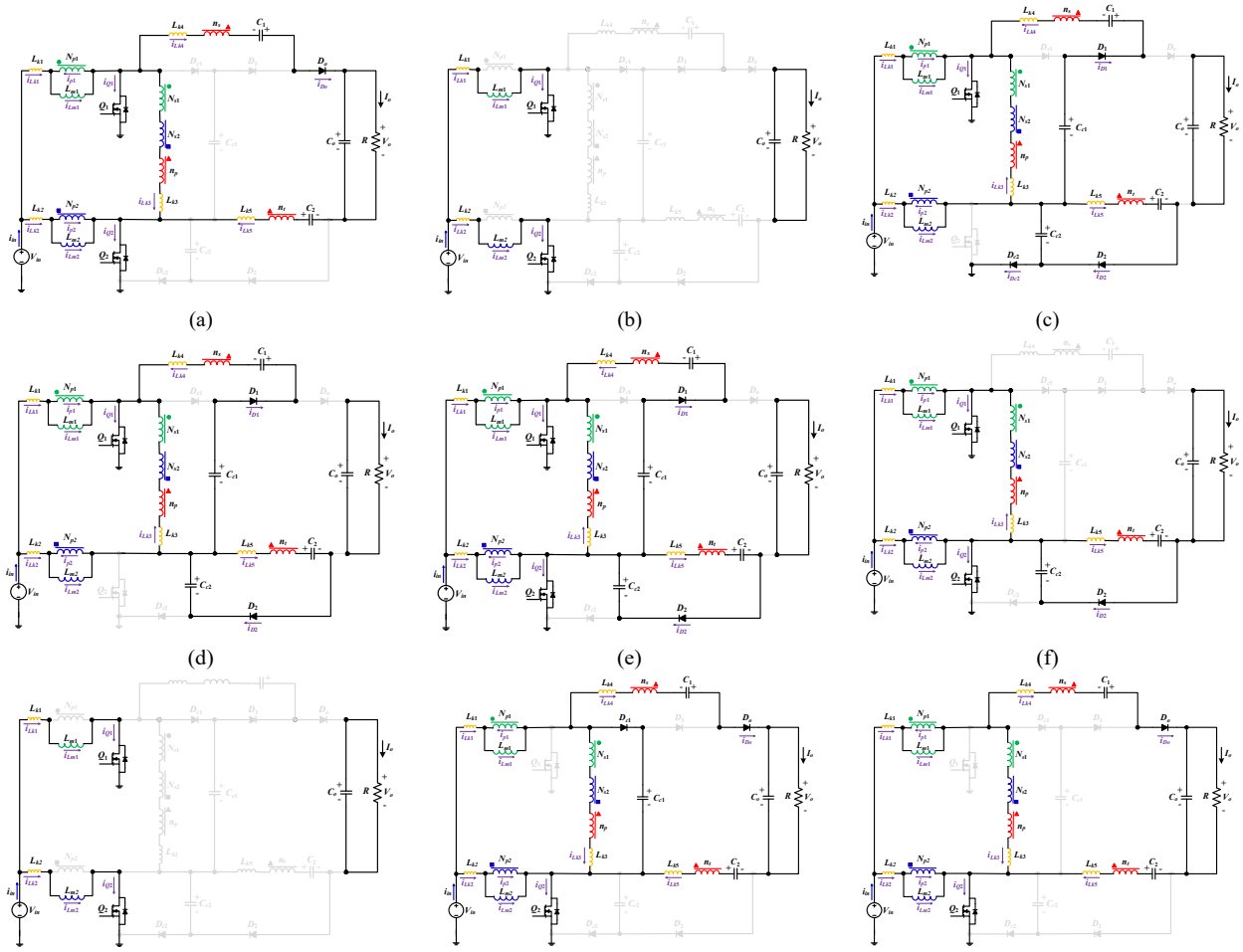

Fig. 3. The operating stages of the proposed converter: (a) Stage 1, (b) Stage 2, (c) Stage 3, (d) Stage 4, (e) Stage 5, (f) Stage 6, (g) Stage 7, (h) Stage 8, (i) Stage 9.

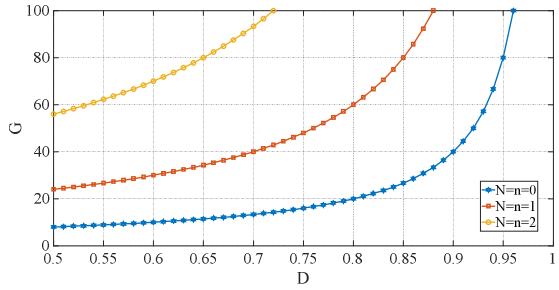

Fig. 4. The voltage gain versus the duty cycle for various values of the turns-ratios of the CIs and BIT.

under the medium duty cycles, as can be seen from Fig. 4.

$$G = \frac{V_o}{V_{in}} = \frac{4 + 4n(1+N)}{1-D} \tag{5}$$

B. Voltage and Average Current Stresses Analysis

The voltage stresses on the switches and diodes are given by (6)-(10). As seen, the voltage stresses on the switches are far less than the output voltage; also, the voltage stresses on the diodes are lower than the output voltage, thus enabling the adoption of low-voltage-rated semiconductors, which leads to the improved efficiency of the converter.

$$V_{Q_1} = V_{Q_2} = V_{D_{c2}} = \frac{1}{1-D} V_{in} \tag{6}$$

$$V_{D_{c1}} = \frac{2}{1-D} V_{in} \tag{7}$$

$$V_{D_1} = \frac{2 + 2n(1+N)}{1-D} V_{in} \tag{8}$$

$$V_{D_2} = \frac{2n(1+N)}{1-D} V_{in} \tag{9}$$

$$V_{D_o} = \frac{2 + 4n(1+N)}{1-D} V_{in} \tag{10}$$

The average input current, average magnetizing currents of the CIs, and average currents of the leakage inductances are

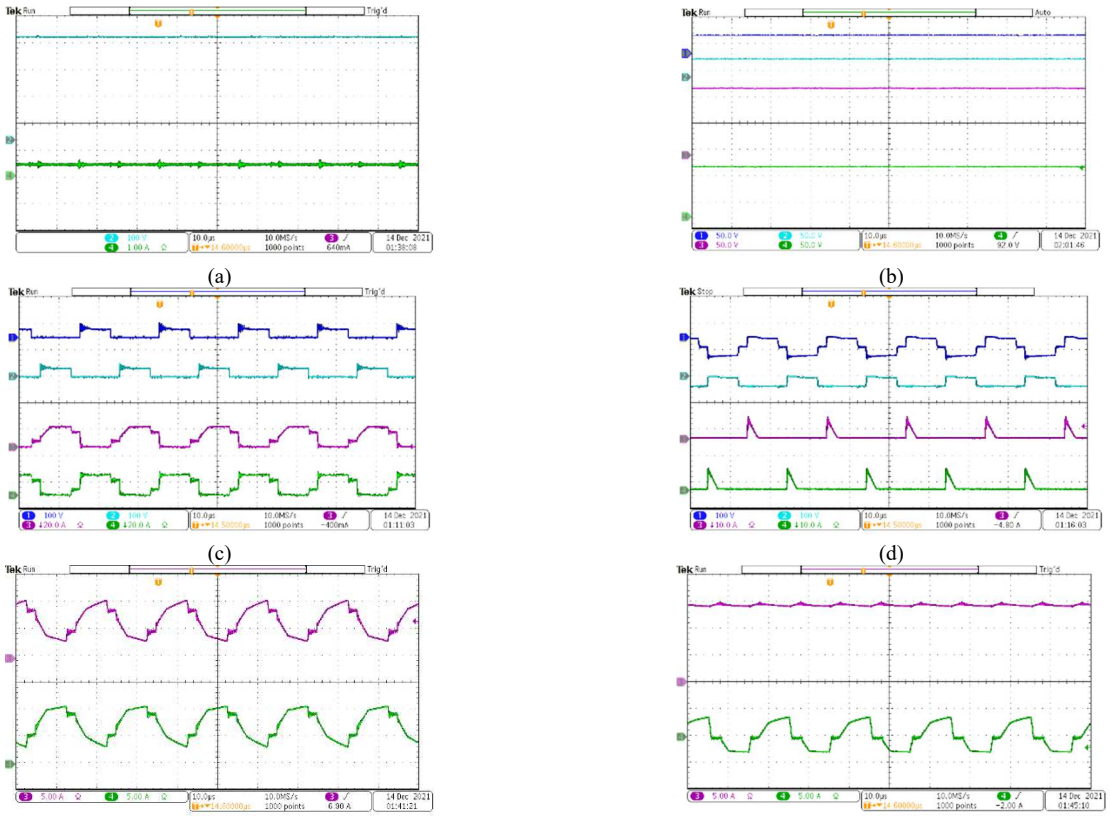

Fig. 5. Experimental results of the proposed converter for V_{in}=13.33 V, D=0.6, and R=800 Ω: (a) output voltage (CH2) and output current (CH4); (b) voltages of capacitors C_{c1} (CH1), C_{c2} (CH2), C_1 (CH3), and C_2 (CH4); (c) voltages of switches Q_1 (CH1) and Q_2 (CH2) as well as currents of switches Q_1 (CH3) and Q_2 (CH4); (d) voltages of diodes D_{c1} (CH1) and D_{c2} (CH2) as well as currents of diodes D_{c1} (CH3) and D_{c2} (CH4); (e) currents of leakage inductances L_{k1} (CH3) and L_{k2} (CH4); (f) input current (CH3) and current of leakage inductances L_{k3} (CH4).

calculated from (11)-(13). Also, the average currents of the semiconductors are obtained from (14)-(16).

$$I_{in} = GI_o = \frac{4+4n(1+N)}{1-D} I_o \tag{11}$$

$$I_{Lm1} = I_{Lm2} = I_{L_{k1}} = I_{L_{k2}} = \frac{1}{2} I_{in} = \frac{2+2n(1+N)}{1-D} I_o \tag{12}$$

$$I_{L_{k3}} = I_{L_{k4}} = I_{L_{k5}} = 0 \tag{13}$$

$$I_{D_{c1}} = I_{D_{c2}} = I_{D_1} = I_{D_2} = I_o \tag{14}$$

$$I_{Q_1} = I_{Lm1} - I_o = \frac{1+2n(1+N)}{1-D} I_o \tag{15}$$

$$I_{Q_2} = \frac{2+2n(1+N)}{1-D} I_o \tag{16}$$

III. Experimental Results

In order to confirm the theoretical analysis of the proposed converter, a 200-W prototype was developed. The critical parameters of the fabricated prototype are listed in Table I.

TABLE I. Critical Parameters of Fabricated Prototype

Parameter	Value
Input voltage V_{in}	13.33 V
Duty cycle D	0.6
Output power	200 W
Switching frequency	50 kHz
Magnetizing inductances L_{m1} and L_{m2}	80 μH
Leakage inductances L_{k1}, L_{k2}, L_{k4}, and L_{k5}	1 μH
Leakage inductances L_{k3}	3 μH
Turns-ratios N and n	1
Capacitors C_{c1} and C_{c2}	50 μF
Capacitors C_1, C_2, and C_o	20 μF

TABLE II. PERFORMANCE COMPARISON

Topology	Total number of magnetic windings of CIs and BIT	Voltage gain (M)	Normalized voltage stress of switches (V_S/V_o)	Maximum normalized voltage stress of diodes (V_D/V_o)
Ref. [11]	7	$\frac{2(N+n+1)}{1-D}$	$\frac{1}{2(N+n+1)}$	$\frac{2n+1}{2(N+n+1)}$
Ref. [12]	6	$\frac{2(N+n+2)}{1-D}$	$\frac{1}{2(N+n+2)}$	$\frac{n+1}{N+n+2}$
Ref. [13]	7	$\frac{2(n+1)+N}{1-D}$	$\frac{1}{2(n+1)+N}$	$\frac{N+2n+1}{2(n+1)+N}$
Ref. [14]	6	$\frac{2(2N+n+2)}{1-D}$	$\frac{1}{2(2N+n+2)}$	$\frac{N+n+1}{2N+n+2}$
Ref. [15]	7	$\frac{2(N+2n+2)}{1-D}$	$\frac{1}{2(N+2n+2)}$	$\frac{N+2n+1}{N+2n+2}$
Proposed converter	7	$\frac{4+4n(N+1)}{1-D}$	$\frac{1}{4+4n(N+1)}$	$\frac{1+2n(N+1)}{2+2n(N+1)}$

Figs. 5(a)-(f) illustrates the experimental results for V_{in}=13.33 V, D=0.6, and N=n=1. From (5), the theoretically calculated voltage gain is 20, which gives an output voltage of 400 V, which is relatively verified by the experimental waveform shown in Fig. 5(a). Also, as shown in Fig. 5(b), the measured voltages of the capacitors are close enough to the theoretically calculated values that are V_{Cc1}=V_{Cc2}=33.33 V, V_{C1}=133.33 V, and V_{C2}=100 V. Other experimental results are in agreement with the theoretical analyses. According to Fig. 5(a), the voltage stress on MOSFETs Q_1 and Q_2 is about 33.33 V, which is far less than the output voltage, thus reducing the switching and conduction losses. Fig. 5(d) shows the voltages and currents of clamp diodes D_{c1} and D_{c2}; as seen, the clamp diodes turn off smoothly under the ZCS condition, thus alleviating their revere-recovery losses. The currents of leakage inductances L_{k1}, L_{k2}, and L_{k3} and input current are shown in Figs. 5(e) and (f). As obvious from Fig. 5(e), there is a 180º phase shift between the currents of L_{k1} and L_{k2}, thus verifying the interleaved operation between two phases of the proposed converter. In addition, the input current ripple is small as seen from Fig. 5(f).

IV. COMPARITIVE STUDY

To demonstrate the merits of the proposed converter, an extensive comparison is made with the similar topologies in [11-15], which is summarized in Table II. All converters are based on the integration of both CI and BIT with SC cells. The converters in [12] and [14] have 6 magnetic windings, while the propose converters and others have 7 magnetic windings. The comparison results of the voltage gain, normalized—based on V_o—voltage stress across the MOSFETs, and maximum normalized voltage stress of the diodes are shown in Figs (5), (6), and (7), respectively. To have a fair comparison of the VB capability of the converters, N=n=1 is selected for all converters in Fig. 5. As seen, the proposed converter has the highest voltage gain. Moreover, according to Fig. 6, the proposed converter has the lowest voltage stress on the MOSFETs. Furthermore, as shown in Fig. 7, the maximum normalized voltage stress of the diodes is lower 1 for all converters; that is, the diodes' voltage stresses are lower than high output voltage in all converters, thus reducing their power losses. Therefore, it

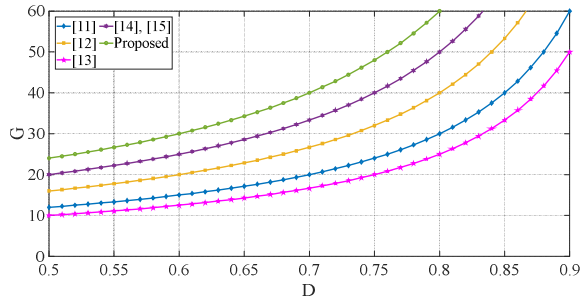

Fig. 5. Comparison of voltage gains for N=n=1.

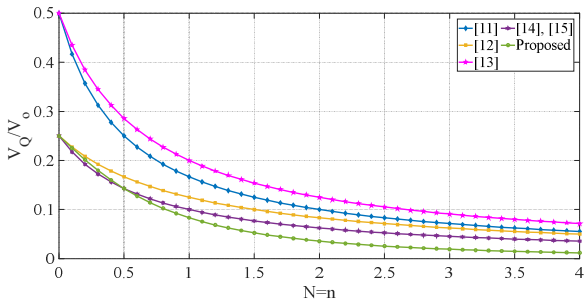

Fig. 6. Comparison of normalized voltage stresses on the switches.

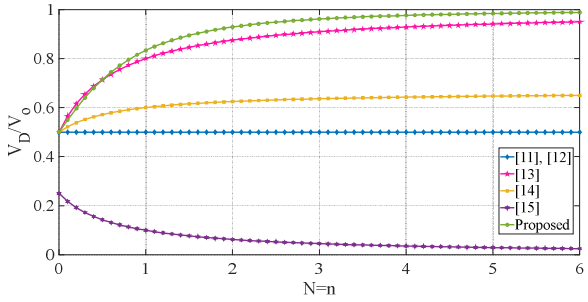

Fig. 7. Comparison of normalized voltage stresses on the output diode.

can be concluded that due to the high voltage gain with medium duty cycle and low voltage stresses on the semiconductors, the proposed converter can be considered as a promising candidate for RE applications.

V. Conclusion

A new high step-up DC-DC converter was proposed in this paper, which is suitable for RE applications. Due to the combination of two CIs and one BIT with SC cells, the proposed converter can provide a high voltage gain under a medium duty cycle. The voltage stresses on the switches are low, leading to the adoption of low-voltage-rated MOSFETs with low ON-state resistance, which improves the efficiency of the converter. Due to the existence of the leakage inductances of the CIs and BIT, the reverse-recovery problem of the diodes is alleviated. The input current is continuous with a low ripple, thus increasing the lifetime of the input RE resource. There are three degrees of freedom (duty cycle of the MOSFETs and turns-ratios of the CIs and BIT), increasing the design flexibility of the proposed converter. The operating states and steady-state analysis of the proposed converter were discussed in detail. Moreover, the theoretical analysis and feasibility of the proposed converters were verified through the experimental results from a 200-W (13.33 V to 400 V) laboratory prototype.

References

[1] J. Ding, S. Zhao, S. Gao and H. Yin, "A Single-Switch High Step-Up DC–DC Converter Based on Three-Winding Coupled Inductor and Pump Capacitor Unit," in *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 3053-3061, 2022.

[2] Z. Wang, Z. Zheng and C. Li, "A High-Step-Up Low-Ripple and High-Efficiency DC-DC Converter for Fuel-Cell Vehicles," in IEEE Transactions on Power Electronics, vol. 37, no. 3, pp. 3555-3569, 2022.

[3] J. Zhao and D. Chen, "Switched-Capacitor High Voltage Gain Z-Source Converter With Common Ground and Reduced Passive Component," in IEEE Access, vol. 9, pp. 21395-21407, 2021.

[4] S. Sadaf, M. S. Bhaskar, M. Meraj, A. Iqbal and N. Al-Emadi, "Transformer-Less Boost Converter With Reduced Voltage Stress for High Voltage Step-Up Applications," in IEEE Transactions on Industrial Electronics, vol. 69, no. 2, pp. 1498-1508, 2022.

[5] R. Rahimi, S. Habibi, M. Ferdowsi and P. Shamsi, "A Three-Winding Coupled Inductor-Based Interleaved High-Voltage Gain DC–DC Converter for Photovoltaic Systems," in IEEE Transactions on Power Electronics, vol. 37, no. 1, pp. 990-1002, 2022.

[6] Y. Tang, T. Wang and D. Fu, "Multicell Switched-Inductor/Switched-Capacitor Combined Active-Network Converters," in IEEE Transactions on Power Electronics, vol. 30, no. 4, pp. 2063-2072, 2015.

[7] V. A. K. Prabhala, P. Fajri, V. S. P. Gouribhatla, B. P. Baddipadiga and M. Ferdowsi, "A DC–DC Converter With High Voltage Gain and Two Input Boost Stages," in IEEE Transactions on Power Electronics, vol. 31, no. 6, pp. 4206-4215, 2016.

[8] B. P. Baddipadiga and M. Ferdowsi, "A high-voltage-gain dc-dc converter based on modified dickson charge pump voltage multiplier," in IEEE Transactions on Power Electronics, vol. 32, no. 10, pp. 7707-7715, 2017.

[9] A. Singh, A. Kumar, X. Pan, S. K. Singh, X. Xiong and N. K. S. Naidu, "Quasi-Impedance-Source-Network-Based Nonisolated High-Step-Up DC–DC Converter," in IEEE Transactions on Industry Applications, vol. 57, no. 6, pp. 6405-6416, 2021.

[10] R. Rahimi, S. Habibi, M. Ferdowsi and P. Shamsi, "An Interleaved Quadratic High Step-Up DC-DC Converter With Coupled Inductor," in IEEE Open Journal of Power Electronics, vol. 2, pp. 647-658, 2021.

[11] T. Nouri, N. Nouri and N. Vosoughi, "A Novel High Step-Up High Efficiency Interleaved DC–DC Converter With Coupled Inductor and Built-In Transformer for Renewable Energy Systems," in IEEE Transactions on Industrial Electronics, vol. 67, no. 8, pp. 6505-6516, 2020.

[12] R. Rahimi, S. Habibi, P. Shamsi and M. Ferdowsi, "An Interleaved High Step-Up DC-DC Converter Based on Combination of Coupled Inductor and Built-in Transformer for Photovoltaic-Grid Electric Vehicle DC Fast Charging Systems," 2021 IEEE Texas Power and Energy Conference (TPEC), pp. 1-6, 2021.

[13] T. Nouri, N. Vosoughi, S. H. Hosseini, E. Babaei and M. Sabahi, "An Interleaved High Step-Up Converter With Coupled Inductor and Built-In Transformer Voltage Multiplier Cell Techniques," in IEEE Transactions on Industrial Electronics, vol. 66, no. 3, pp. 1894-1905, 2019.

[14] R. Rahimi, S. Habibi, M. Ferdowsi and P. Shamsi, "A Two-Phase Interleaved High-Voltage Gain DC-DC Converter with Coupled Inductor and Built-in Transformer for Photovoltaic Applications," IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society, pp. 1-6, 2021.

[15] R. Rahimi, S. Habibi, M. Ferdowsi and P. Shamsi, "An Interleaved High Step-Up DC-DC Converter Based on Integration of Coupled Inductor and Built-in-Transformer With Switched-Capacitor Cells for Renewable Energy Applications," in IEEE Access, vol. 10, pp. 34-45, 2022.