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A High Step-Up DC-DC Converter Using a Three Winding Coupled Inductor for Photovoltaic to Grid Applications

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***Abstract*— A dual-switch high step-up DC-DC converter topology is proposed in this paper. The proposed topology uses two power switches, a three-winding coupled inductor (TWCI), and voltage multiplier cells to provide a high voltage gain. Furthermore, the voltage stresses on power semiconductor switches are low, resulting in lower switching and conduction losses. Moreover, the common electrical ground is preserved in this topology, making it a suitable candidate for photovoltaic (PV) to grid systems. The operating modes and steady state analysis of the proposed converter are presented, and a comparative study is carried out to demonstrate advantages of the proposed topology over the existing topologies. Finally, the simulation results of the proposed topology are presented using PLECS software along with the experimental results for a 200 W, 30 V to 400 V laboratory setup.**

Keywords*— *High Step-up, DC-DC, PV to Grid

I. INTRODUCTION

Because of the energy crisis and the need to reduce CO2 emissions caused by the combustion of fossil fuels for energy generation, the expansion of renewable resources is unavoidable [1], [2]. Among the renewable resources, photovoltaic (PV) systems have seen the most growth in terms of both research and installation . Due to the low voltage of the PV panels (20 V to 40 V), a high voltage conversion ratio is required to connect a PV panel to the DC bus of an inverter or a DC microgrid [3]–[6]. Traditionally, boost converters are used to lift the PV panel voltage to an appropriate level. But, due to the issues such as the high voltage stress on the power switch and reverse recovery of the output diode, the conventional boost converter efficiency is low in these applications [6]. To overcome the well-known limitations of the conventional boost converter in high voltage gain applications, high step-up converters are used to provide high voltage gain and high efficiency . Various voltage boosting techniques (VBT) have been adopted in the literature to increase the voltage gain of a converter, such as switched capacitor (SC), switched inductor, and magnetically coupled devices [7]. Combinations of different VBTs are also used to further increase the voltage gain [8], [9]. Converters using only SC cells to increase the voltage gain suffer from high number of switches and capacitors, beside the high transitional currents of capacitors, which increases power loss of a converter and may generate electromagnetic interference (EMI) in system [10].

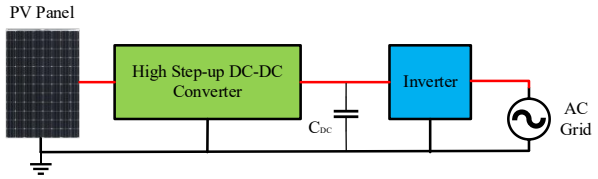

Fig. 1. Simplified schematic of a transformer less grid-tied PV system.

Utilizing SC cells with coupled inductors (CIs) in a converter helps to overcome the aforementioned issues, and it provides one more degree of freedom (CI's turns ratio) in the converter design [11]. Different combinations of the SC cells with CIs or built in transformers are presented in the literature, These converters are able to provide high voltage conversion ratio and keep the voltage stress on the power switches low [12], [13].

In this paper, a high step-up DC-DC converter is proposed based on the combination of diode-capacitor voltage multiplier cells and a three-winding coupled inductor (TWCI). The proposed topology has a large voltage gain, low voltage stress on power switches, flexibility in design, and common electrical ground. The proposed converter is a suitable candidate for PV to grid applications. In these systems, preserving the common electrical ground is critical to reduce the leakage current. A

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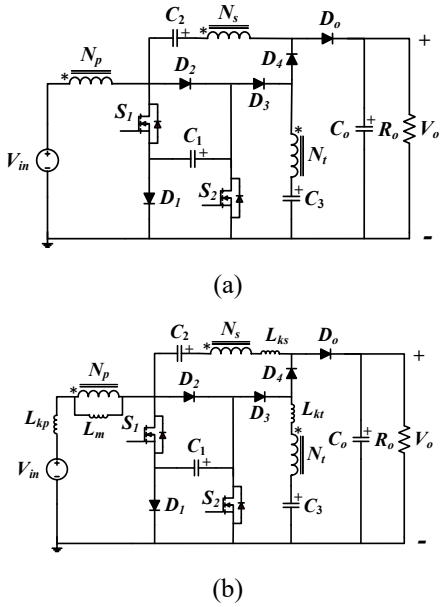


Fig. 2. The proposed topology, (a) circuit configuration, (b) equivalent circuit.

simplified schematic of PV to grid system is shown in Fig. 1.

The rest of this paper is organized as follows. The proposed topology is introduced in Section II. The operating modes of the proposed converter are presented in Section III. The steady-state analysis is carried out in Section IV. A comparative study is demonstrated in Section V. The simulation and experimental results are in Section VI, and the paper is concluded in Section VII.

II. Proposed Topology

The circuit configuration of the proposed topology is shown in Fig. 2 (a). The proposed topology has two power switches (S_1 and S_2), five diodes ($D_1 - D_4$ and D_o), four capacitors ($C_1 - C_4$), and a TWCI. The number of turns for the primary, secondary, and tertiary windings of the TWCI is denoted by N_p, N_s, and N_t, respectively. The coupling reference of the TWCI is shown by "*" at each winding. By replacing the TWCI with a three-winding transformer, the equivalent circuit of the proposed topology is shown in Fig. 2 (b). Each winding of the TWCI is replaced with a transformer winding with series leakage inductances (L_{kp}, L_{ks}, and L_{kt}), and a parallel magnetizing inductance (L_m) is used with the primary winding.

III. Operating Modes

The proposed topology has four operating modes. Using the equivalent circuit shown in Fig. 2 (b), the operating modes are explained. The ideal key waveforms of the proposed converter including, the gate-source signals, current of the power switches, current of the TWCI, and current of the diodes are presented in Fig. 3. The operating modes of the proposed topology are shown in Fig. 4 (a)-(d). The proposed topology has two dominant modes – Mode II and Mode IV. Mode II and Mode IV represent the circuit configuration of the converter when both switches are on (DT) and off ($(1\text{-}D)T$), respectively. Mode I is a transitional mode prior to Mode II, and Mode III is a transition mode prior

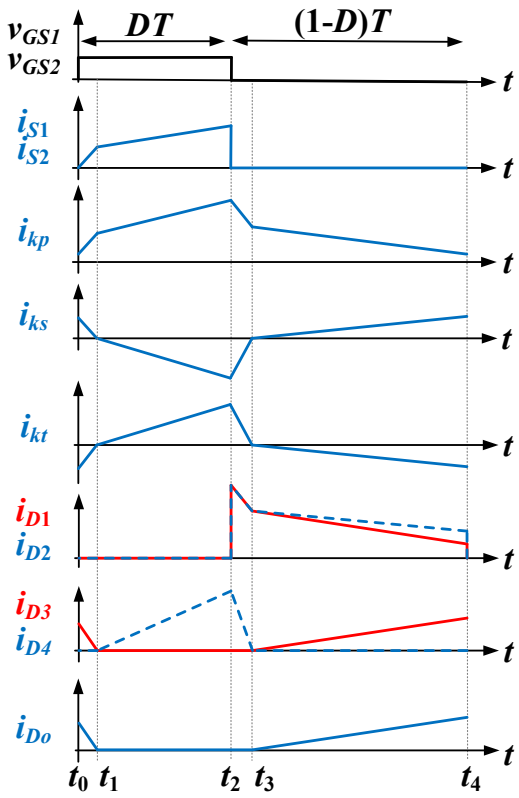


Fig. 3. Ideal key waveforms of the proposed topology.

to Mode IV. Each of the modes are explained in the following paragraphs, and to simplify the analysis, the turns ratio of the secondary to primary winding is assumed to be equal to the turns ratio of the tertiary to primary winding ($N_s/N_p = N_t/N_p = N$).

Mode I ($t_0 < t < t_1$): At the beginning of this mode, S_1 and S_2 turn on simultaneously. The magnetizing and primary leakage inductances current start to increase, meanwhile, the secondary and tertiary inductances current begin to decrease to reach zero. During this mode, D_o and D_3 are on, and other diodes are off. Diode D_o provides a current path from the input source to the output capacitor, and D_3 provides a path for C_3 to charge. The voltage equations of this mode are shown by (1).

$$\begin{cases} V_{L_m} + V_{L_{kp}} = V_{in} + V_{c_1} \\ NV_{L_m} + V_{L_{ks}} = V_{c_2} - V_{c_1} - V_o \\ NV_{L_m} + V_{L_{kt}} = -V_{c_3} \end{cases} \quad (1)$$

Mode II ($t_1 < t < t_2$): When the currents in the secondary and tertiary inductances reach zero, they flow in the opposite direction. Therefore, D_3 and D_o turn off, and D_4 turns on to provide a path for i_{Lks} and i_{Lkt}. S_1 and S_2 are still on in this mode and the output capacitor provides power to the load. The circuit stays in this mode until the power switches turn off with the gate signal. The voltage equations of this mode are shown by (2).

$$\begin{cases} V_{L_m} + V_{L_{kp}} = V_{in} + V_{c_1} \\ 2NV_{L_m} + V_{L_{ks}} + V_{L_{kt}} = V_{c_2} - V_{c_1} - V_{c_3} \end{cases} \quad (2)$$

Mode III ($t_2 < t < t_3$): At the beginning of this mode, S_1 and S_2 turn off with gate signal. Diodes D_1 and D_2 turn on to provide

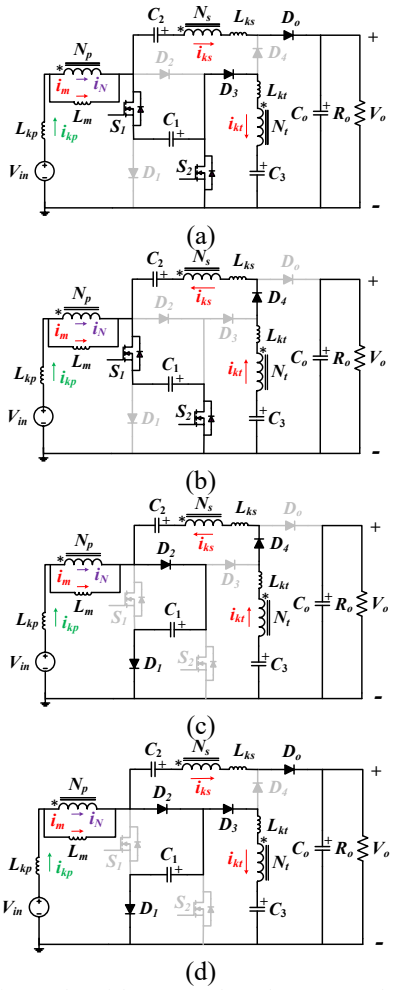


Fig. 4: Operating modes of the proposed topology, (a) Mode I, (b) Mode II, (c) Mode III, (d) Mode IV.

a current path for i_{Lkp} *and* i_{Lks}, and D_4 stays on until the current in the secondary and tertiary windings reach zero. In this mode, D_1, D_2, and C_1 generate a clamp circuit to capture the leakage inductance energy and prevent destructive spikes on the power switches. Voltage equations of this mode are shown by (3).

$$\begin{cases} V_{L_m} + V_{L_{kp}} = V_{in} - V_{c_1} \\ 2NV_{L_m} + V_{L_{ks}} + V_{L_{kt}} = V_{c_1} + V_{c_2} - V_{c_3} \end{cases} \quad (3)$$

Mode IV ($t_3 < t < t_4$): When the i_{Lkp} *and* i_{Lks} reach zero, they change direction, therefore, D_4 turns off and D_3 and D_o turn on. The power switches are off in this mode, and the circuit stays in this mode until the switches turn on again. Voltage equations of this mode are labeled by (4).

$$\begin{cases} V_{L_m} + V_{L_{kp}} = V_{in} - V_{c_1} \\ NV_{L_m} + V_{L_{ks}} = V_{c_2} + V_{c_1} - V_o \\ NV_{L_m} + V_{L_{kt}} = V_{c_1} - V_{c_3} \end{cases} \quad (4)$$

IV. Steady State Analysis

To carry out the steady-state analysis, it is assumed that all capacitors are large enough and their voltages are constant during a switching cycle, the parasitic elements are ignored except for the leakage inductances, and the converter operates in the continuous conduction mode (CCM). Among the four operating modes shown in Fig.4, Mode I and III are transitional modes and their duration are negligible compared to Mode II and IV durations. By applying the volt-second balance principle to the voltages of the magnetizing inductance, the voltage on the capacitors are found in (5). Using (5), the voltage gain of the converter is achieved in (6). It is obvious that the volage gain of the converter is dependent on the TWCI turns ratio and duty cycle of the converter, which provides two degrees of freedom for a designer. The voltage gain of the converter versus the duty cycle is plotted for different values of the TWCI turns ratio in Fig. 5 (a). As it can be seen from Fig. 5 (a), very high voltage gains such as 30 can be achieved in low duty cycles for this converter.

The voltage stress on the semiconductor devices is calculated using the voltage of the capacitors. The voltage stress on the power switches is presented in (7), and as it can be seen from the normalized voltage stress plots in Fig. 5 (b), the voltage stress on the power switches is less than one seventh of the output voltage for the TWCI turns ratio higher than one. This is one of the important features of the proposed converter that can generated a very high voltage at the output and keep the voltage stress on the power switches low. Following the same procedure, the voltage stress of the diodes is calculated in (8).

To calculate the current stress on the semiconductor components, the average current passing through the switches and diodes are calculated. By considering that the average

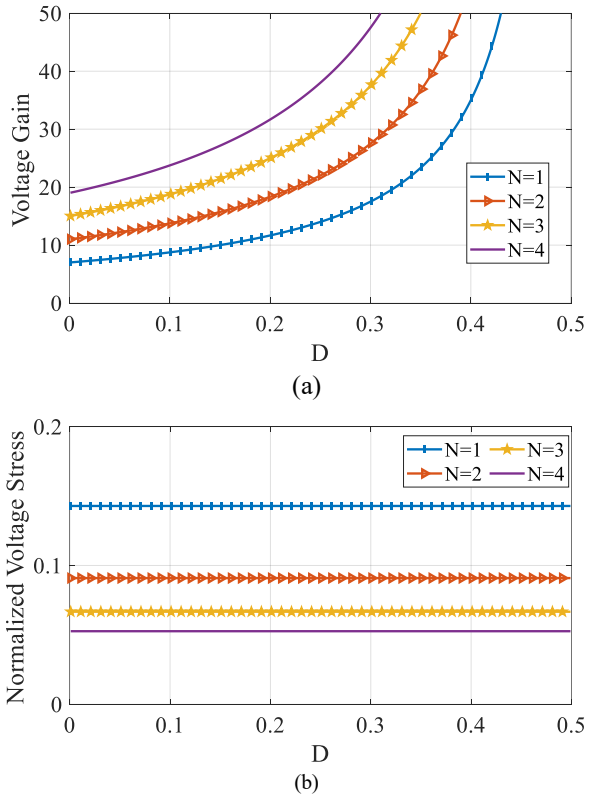


Fig. 5. The voltage gain and normalized voltage stress of the proposed converter for different values of the TWCI turns ratio, (a) voltage gain, (b) normalized voltage stress.

TABLE I. SIMULATION PARAMETERS

Converter	Number of components					Voltage gain ($\frac{V_o}{V_{in}}$)	Voltage stress of power switch ($\frac{V_s}{V_o}$)	Common ground
	S	C	D	L	CI/NW			
[11]	2	4	5	0	1/2	$\frac{3+2N}{1-2D}$	$\frac{1}{3+2N}$	No
[14]	1	6	5	0	1/3	$\frac{2+N(2-D)}{1-2D}$	$\frac{1}{2+2N-ND}$	Yes
[15]	1	7	5	3	0	$\frac{2+D}{1-2D}$	$\frac{1}{2+D}$	No
[16]	1	5	4	1	1/2	$\frac{2+N+ND}{1-2D}$	$\frac{1}{2+N+ND}$	Yes
[17]	2	4	5	0	1/3	$\frac{3+4N}{1-2D}$	$\frac{1}{3+4N}$	No
Proposed	2	4	5	0	1/3	$\frac{3+4N}{1-2D}$	$\frac{1}{3+4N}$	Yes

current of the capacitors is zero at a switching cycle, the average current of the switches is found (9), and the average current of the diodes are presented in (10).

$$\begin{cases} V_{c_1} = \frac{V_{in}}{1-2D} \\ V_{c_2} = \frac{2(1-DN+2N)}{1-2D} V_{in} \\ V_{c_3} = \frac{1+2ND}{1-2D} V_{in} \end{cases} \quad (5)$$

$$\left\{ \frac{V_o}{V_{in}} = \frac{3+4N}{1-2D} \right. \quad (6)$$

$$V_{s_1} = V_{s_2} = \frac{V_o}{3+4N} \quad (7)$$

$$\begin{cases} V_{D_1} = V_{D_2} = \frac{V_o}{3+4N} \\ V_{D_3} = \frac{1+2N}{3+4N} V_o \\ V_{D_4} = \frac{2+4N}{3+4N} V_o \\ V_{D_o} = \frac{2+2N}{3+4N} V_o \end{cases} \quad (8)$$

$$I_{S_1} = I_{S_2} = \frac{1+2N+D}{1-2D} I_o \quad (9)$$

$$\begin{cases} I_{D_1} = \frac{1+2N+D}{1-2D} I_o \\ I_{D_2} = \frac{2+2N-D}{1-2D} I_o \\ I_{D_3} = I_{D_4} = I_{D_o} = I_o \end{cases} \quad (10)$$

V. COMPARISON

The proposed topology is compared with the existing topologies with similar voltage gain relationships. The comparison study includes the number of components, voltage gain, voltage stress on power switches, and the common electrical ground as listed in TABLE I. Converters voltage gain and the normalized voltage stress on the power switch (V_s/V_o) are plotted in Fig. 6 (a) and (b), respectively. As it can be seen from Fig. 6 (a) and (b), the proposed topology has higher voltage gain than converters presented in [11], [14]–[16], and also less normalized voltage stress than these converters. Except for the higher voltage gain and less voltage stress on the power switch, the proposed converter has one magnetic core, but the converters in [15], [16] use more than one magnetic core. The proposed converter and the converter in [17] have similar voltage gain and voltage stress on the power switch, and also the number of the components are same in these converters. The superiority of the proposed converter over the converter in [17] is preserving the common electrical ground between the input and output. As mentioned before, this feature is critical in some of the renewable applications. Similar to [17], converters in [11] and [15] also have a floating load. Based on the TABLE I and Fig.

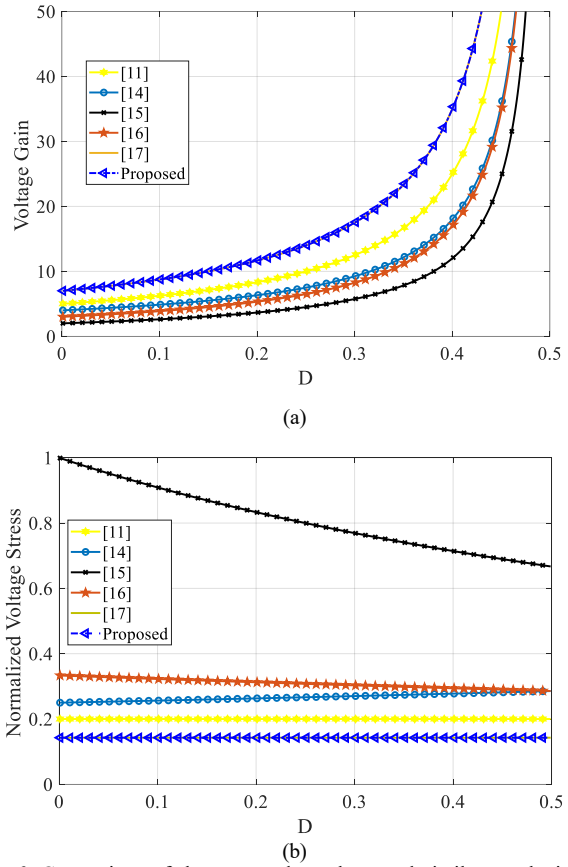


Fig. 6. Comparison of the proposed topology and similar topologies, (a) voltage gain, (b) normalized voltage stress on the power switches.

6, it can be concluded that the proposed converter is superior to the existing converters in the literature.

VI. RESULTS

To validate the proposed converters steady-state analysis and its functionality, a simulation models and experimental setup are developed. The simulation and experimental results are explained in the following subsections.

A. Simulation Results

To validate the steady-state analysis, a simulation model is developed in PLECS Standalone software. The simulation model is for a 30 V to 400 V converter and the output load is set to 800 Ω. The list of simulation parameters is presented in

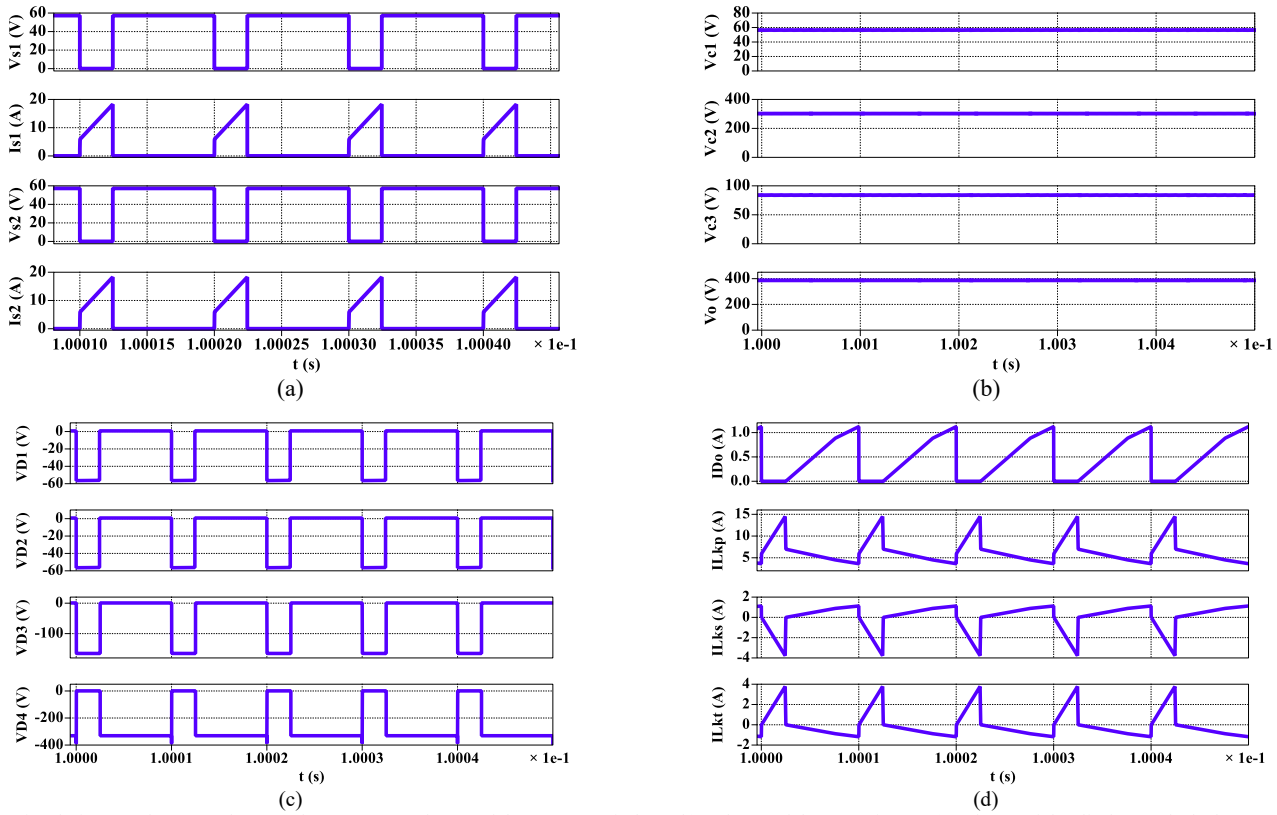


Fig. 7. Simulation results, (a) voltage and current waveforms of the power switches, (b) voltage of the capacitors, (c) voltage of the diodes, and (d) the output diode and TWCI current waveforms.

TABLE II. SIMULATION PARAMETERS

Input voltage (V_{in})	30 V
Output voltage (V_o)	400 V
Power (P_o)	200 W
TWCI turns ratio (N)	1
Duty cycle (D)	0.24

TABLE II. Based on the steady-state analysis, the voltage of the power switches is 57 V, and as it can be seen from Fig. 7 (a), the power switches voltage is very close to 57 V. Similarly, the voltage of the capacitors in Fig. 7 (b) are 56.4 V, 302.2V, 84 V, and 387 V for C_1, C_2, C_3, and C_o, respectively. The capacitor voltage values are consistent with the steady-state analysis. In Fig. 7 (c), the voltage of the diodes are shown. As it be seen from Fig. 7 (c), voltages on D_1, D_2, D_3, and D_4 are 57 V, 57 V, 165 V, and 331 V, respectively. These voltage values are in good agreement with the steady-state analysis. The current of the output diode and each winding of the TWCI is shown in Fig. 7 (d). These simulation results validate the steady-state analysis in Section IV and shows the functionality of the proposed converter. These results verify that the proposed converter is able to provide a high gain such as 13.3 from a 30 V input source and keep the voltage stress on the power switches low.

B. Experimental Results

To verify the steady-state analysis and simulation results, A 200 W, 30 V to 400 V setup is designed and implemented in the laboratory. The components of the experimental setup such as the input source, load, and proposed converter are shown in Fig .8. In the experimental setup, the input source is connected to a DC power supply and the converter out is connected to a resistive load. The experimental setup parameters are similar to the simulation model presented in TABLE II.

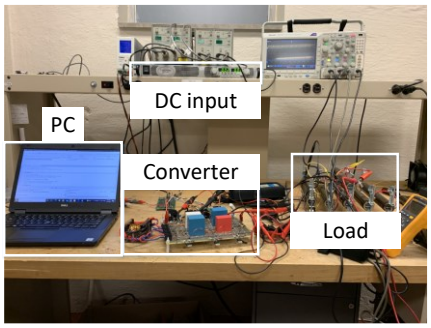
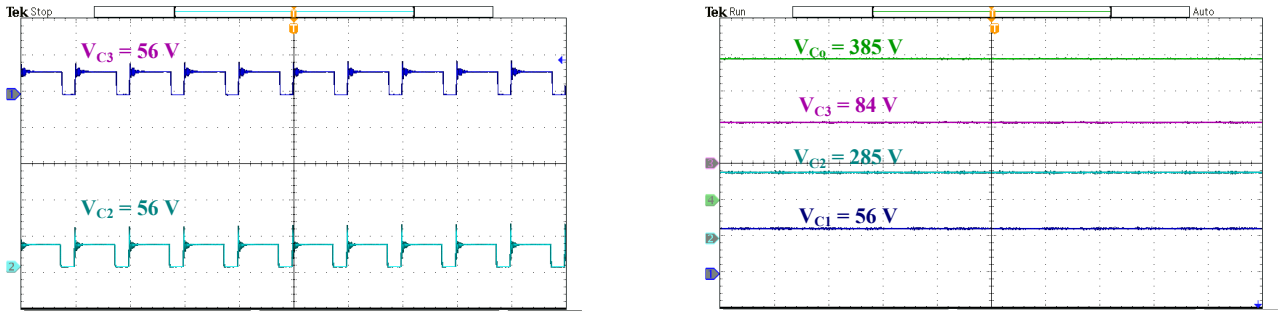


Fig. 8. The experimental setup.

The experimental results are shown in Fig. 9. In this setup, the input voltage is 30 V, and the duty cycle of the power switches is 0.24. Fig. 9 (a) shows the voltage of the power switches, and as it can be seen from it, the voltage on the power switches is approximately 56 V, which is very close to the simulation results. Also, the voltage overshoot for the turn off instances of the power switches is very low, meaning the clamp circuit in the circuit absorbs the leakage inductance energy. In Fig. 9 (b), the voltages of the capacitors and the approximate



(a) (b)

Fig.9. Experimental results, (a) voltage of the power switches, (b) Voltage of the capacitors.

value of the voltages seen from the measurement device are shown. The capacitors voltage is in a good agreement with the simulation results and steady-state analysis.

VII. Conclusion

In this paper, a high step-up DC-DC converter based on the combination of a three-winding coupled inductor and diode capacitor cells are proposed. The proposed topology provides a very high voltage gain in a low duty cycle. Moreover, the proposed topology has a common electrical ground between the input and output terminal, which is critical requirement for part of the renewable applications. Furthermore, the voltage stress of the power switches in this converter are low, resulting in the selection of low $R_{DS(ON)}$ MOSFETs. Using low $R_{DS(ON)}$ MOSFETs leads to a lower conduction loss in the power switches along with a lower switching loss due to the low voltage stress on the power switch, which consequently high efficiency is achieved. The operation principle and steady-state analysis are presented for the proposed converter, and a performance comparison between the proposed converter and similar topologies is provided to justify the superiority of the proposed converters over the existing similar topologies. Finally, simulation model and experimental setup are used to validate the analysis of the proposed topology.

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