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RESEARCH ARTICLE

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Fast impedance prediction for power distribution network using deep learning

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Abstract

Modeling and simulating a power distribution network (PDN) for printed circuit boards with irregular board shapes and multi-layer stackup is computationally inefficient using full-wave simulations. This paper presents a new concept of using deep learning for PDN impedance prediction. A boundary element method (BEM) is applied to efficiently calculate the impedance for arbitrary board shape and stackup. Then over one million boards with different shapes, stackup, integrated circuits (IC) location, and decap placement are randomly generated to train a deep neural network (DNN). The trained DNN can predict the impedance accurately for new board configurations that have not been used for training. The consumed time using the trained DNN is only 0.1 s, which is over 100 times faster than the BEM method and 10 000 times faster than full-wave simulations.

KEYWORDS

boundary element method, deep learning, deep neural network, impedance, power distribution network

1 | INTRODUCTION

Accurate and fast modeling for multi-layer printed circuit boards (PCBs) is of critical importance to the design and performance evaluation of the power distribution network (PDN). Different methodologies have been proposed to model PDN structure and compute impedance.[1–5] The cavity model method[1,2] is an efficient approach to calculate PDN impedance, but it is limited to rectangular board shapes. The plane-pair partial element equivalent circuit (PEEC) method[3] can address irregular board shapes but requires solving a 2D mesh circuit and is, therefore, computationally intensive. There are also some boundary integral methods[4,5] that only require 1D integration but are still not efficient enough in some applications. For example, in the pre-layout stage, a substantial amount of computations are needed to optimize design parameters.

In recent years, the success of deep learning for complex and non-linear problems like computer vision,[6] natural language processing,[7] and strategy games[8] has also impacted many other fields. There has been some research[9–12] in applying machine learning in PDN modeling and optimization. However, most of these works do not have a well-trained and generalized machine learning model for PDN impedance prediction at the PCB level. In the work of Schierholz et al.,[9] an artificial neural network has been adopted to predict target impedance violations for PDN by considering the variations of IC location, decap placement, and target impedance. However, their task is just a simple

[Corrections added on 9 November 2021, after first online publication: Figures 10(c) and 11(c) have been corrected in this version.]

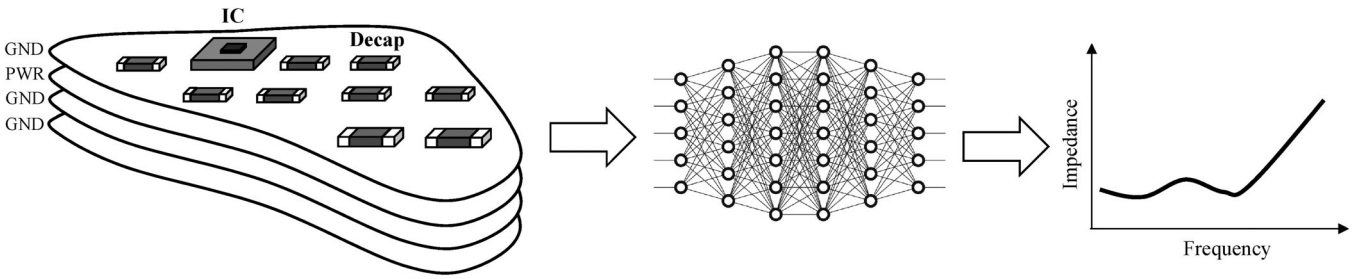

FIGURE 1 A deep neural network (DNN) can be trained to predict the power distribution network impedance for different design parameters, including board shape, stackup, IC location, and decap placement

classification problem to judge if the target impedance will be violated or not. It cannot provide quantitative and insightful details about the actual impedance curve. Moreover, the variation of board shape and stackup is not considered, which makes the trained deep neural network (DNN) hard to generalize.

In this paper, deep learning will be utilized to predict the impedance curve for any board shape, stackup, IC location, and decap placement, as illustrated in Figure 1. A DNN can be trained by using a considerable number of boards with different configuration parameters. Compared to the traditional ways of calculating PDN impedance,[1–5] the trained DNN can be much faster while retaining a tolerable accuracy. Therefore, it can be a particularly powerful and efficient tool for PDN impedance evaluation at the design stage.

The remaining sections are organized as follows. In Section 2, the impedance calculation method for arbitrary board shape and stackup is briefly introduced, and the data generation process is elaborated. Section 3 shows the detailed DNN structure and the training process. Section 4 demonstrates the testing result for the trained DNN. Finally, conclusions are drawn in Section 5.

2 | TRAINING DATA GENERATION

2.1 | Impedance calculation

To ensure the good performance of a DNN, abundant board data with different configurations need to be generated for training. Hence, developing an efficient method to calculate the impedance for arbitrary board shape and stackup is crucial to the feasibility of the deep learning algorithm. Consequently, a boundary element method (BEM)[5,13] that can handle arbitrarily-shaped parallel planes is applied to calculate the quasi-static inductances between vertical vias. In this BEM method, only the boundary needs to be discretized into a proper number of segments for 1D integration. Afterward, an equivalent circuit can be formed by the inductances and parallel-plate capacitances for multi-layer PDN structures. Instead of using commercial tools, the well-known node voltage method is applied to obtain the Z-parameters of the network looking into the IC and decap ports.[13] The Z-parameters of decaps can be further connected to the decap ports to obtain the total impedance looking into the IC.

Figure 2 demonstrates a test example[13] to verify the BEM method by comparing it with an HFSS full-wave simulation.[14] Figure 2A describes the PCB shape. There are six ports formed by six pairs of power and ground vias. Port 6 is the observation port, and ports 1–5 are connected to decaps of 330, 47, 10, 10, and 2.2 μF, respectively, in Table 1. Table 1 lists 10 different decap types represented by number 1–10 that will be used throughout this paper. Figure 2B shows the stackup of this test board. Figure 2C plots the results of the BEM method and the HFSS simulation. The observation frequency is from 0.01 to 20 MHz. The perfect agreement in Figure 2C strongly corroborates the accuracy and reliability of the BEM method. The BEM method, however, only consumes about 5 s, while the HFSS simulation spends over 5 min.

2.2 | Data generation

To mimic different possible board shapes in real PCB designs, an algorithm[15] was adopted to generate random 2D shapes. First, the maximum board size is specified as 200 mm × 200 mm. Then, the algorithm generates several

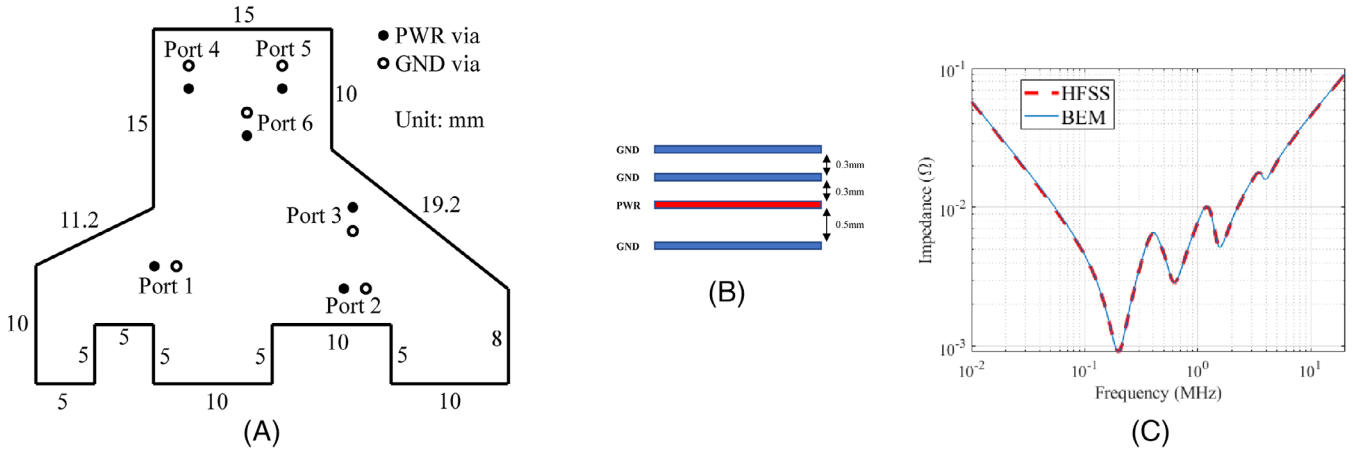

FIGURE 2 An irregular-shape power plane is used to verify the boundary element method (BEM) algorithm.[13] (A) Board shape and port distribution. The separation distance between each pair of power and ground vias is 2 mm. (B) Stackup. (C) Impedance comparison between BEM and HFSS simulation

TABLE 1 Decap parameters

Decap number	Capacitance (μF)	ESL (nH)	ESR (mΩ)
1	0.1	0.19	34.7
2	0.47	0.18	18.3
3	1	0.22	15.2
4	2.2	0.20	7.2
5	4.7	0.28	7.1
6	10	0.26	5.2
7	22	0.27	4.0
8	47	0.15	2.9
9	220	0.41	1.9
10	330	0.46	1.2

Abbreviations: ESL, equivalent series inductance; ESR, equivalent series resistance.

random points (8 points are used in this paper) within the constrained board area. The generated points are sorted along one rotational direction and connected smoothly to form a closed contour. Figure 3 shows two randomly generated 2D shapes using the method.

For machine learning applications, input parameters need to be encoded into matrices. In this paper, a 2D matrix is used to represent the board shape. Figure 4 illustrates an example of encoding and approximating a randomly generated board shape into a matrix of 16 × 16. The same dimension will be used for the remainder of this paper. For the impedance calculation using the BEM method throughout this paper, the accurate board shapes illustrated in Figure 4A are utilized. We assume that each unit cell in the 16 × 16 board matrix can only contain either one IC port or one decap port. Moreover, each decap port is assumed to be horizontally oriented (along *x*-direction), and the distance between the power and ground vias is 2 mm. For simplification purposes, the IC port is also represented by a pair of power and ground vias that are 2 mm apart and horizontally oriented (along *x*-direction). The discrete decap locations approximate possible continuous decap locations in real designs. The reason for choosing 16 × 16 as the resolution is a tradeoff between the problem complexity and the approximation accuracy. A larger matrix dimension can better approximate continuous locations, but a more complex neural network structure, more training data, and a longer training time is required.

To consider the variations of IC location and decap placement, different possible combinations are generated randomly inside the PCB area. The number of decaps is a random value from 1 to 19, and they are randomly distributed on the top and bottom layers. The IC port is also randomly located on the top layer. Each decap port is connected to a

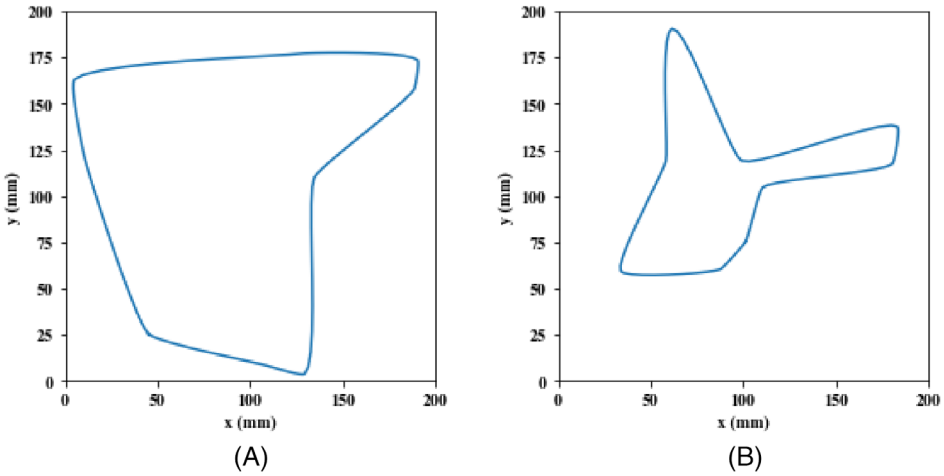

FIGURE 3 Two examples of randomly generated shapes. The maximum board size is 200 mm × 200 mm

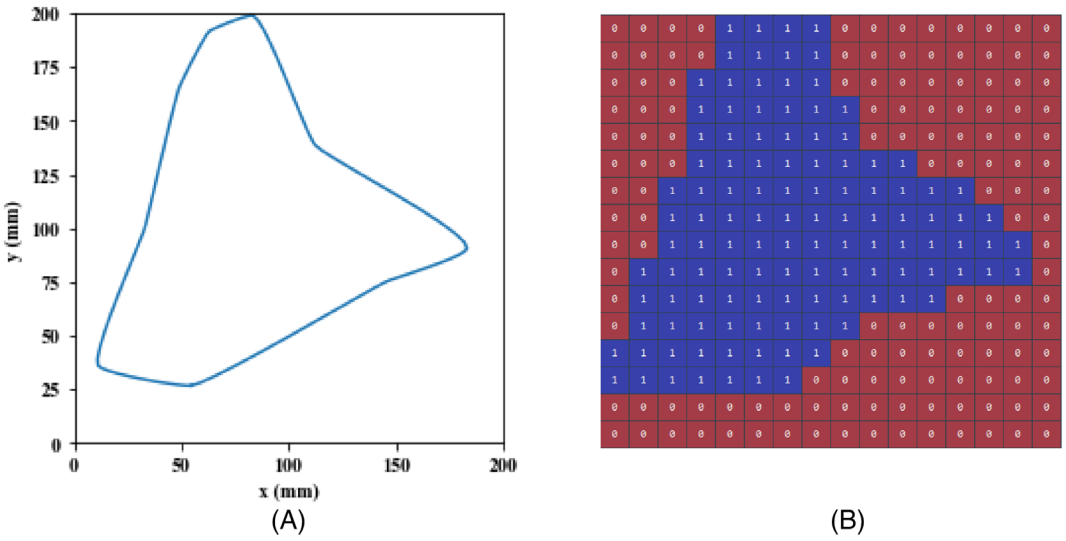

FIGURE 4 (A) An example of a randomly generated board shape. (B) The matrix representation of the board shape using a matrix of 16 × 16

decap randomly chosen from Table 1 and denoted by a number from 1 to 10. Figure 5A shows an example with random IC and decap distributions. Three 16 × 16 matrices are used to describe the board shape, IC location, top decap placement, and bottom decap placement. The first matrix, as shown in Figure 5B, defines the board shape and IC location using 1 and 2, respectively. The second and the third matrix represent the top and the bottom decap placement, respectively, as shown in Figure 5C,D. These three matrices are cascaded into a 3 × 16 × 16 matrix that will be used as the first input matrix of the DNN.

Another parameter to be included is the PCB stackup. A random stackup can be simply generated with a random thickness from 1 to 10 mm and a random number of layers from 4 to 9. The power layer is randomly located among the generated layers but cannot be located on the top layer or the bottom layer. The minimum distance between two adjacent layers is specified as 0.1 mm. Figure 6 shows two examples of randomly generated stackup, including the layer type and the dielectric thickness. In this paper, the relative permittivity of the PCB dielectric material is defined as 4.4.

Similarly, the stackup information needs to be encoded into a matrix. Since using a 2D matrix is unnecessary, a 1D matrix of 1 × 17 is used instead. Since the maximum number of layers is 9, the first 9 elements of the 1 × 17 matrix define the layer type, in which 1 means ground layer, 2 means power layer, and 0 means empty (number 0 only appears

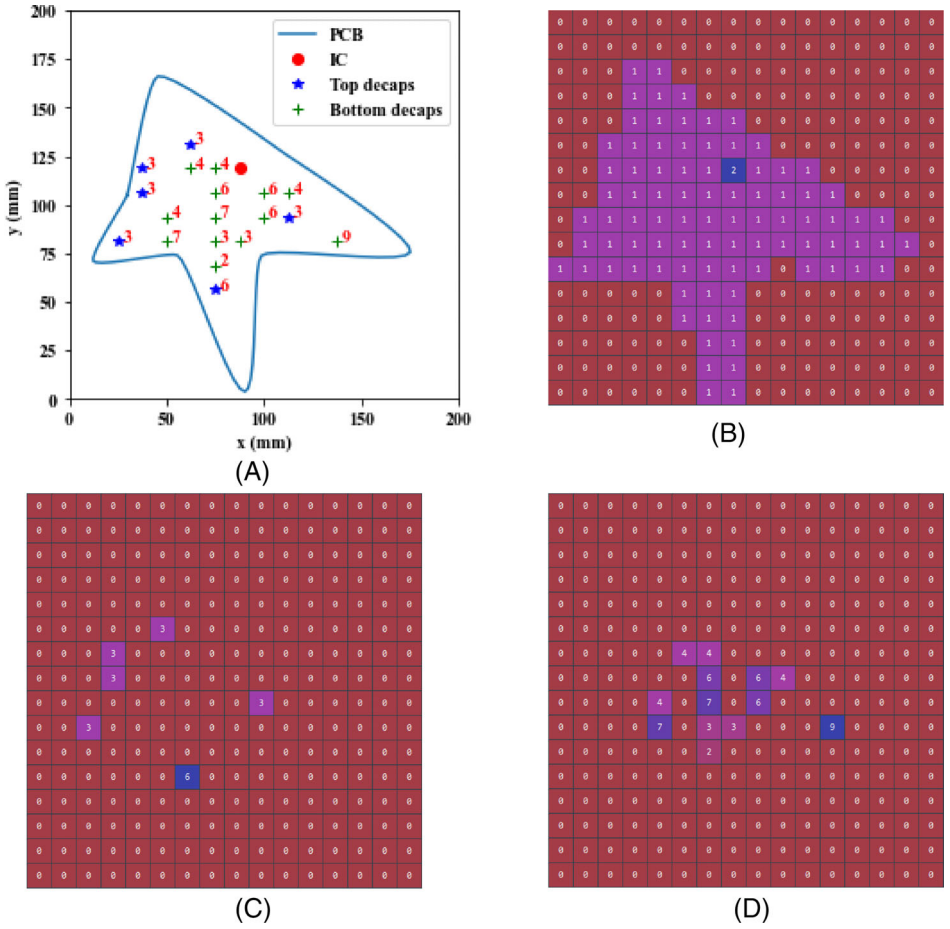

FIGURE 5 (A) An example of randomly generated board shape, IC location, and decap locations on the top and bottom side. The numbers represent the placed decaps corresponding to Table 1. (B) The matrix representation of the board shape and the IC location using a matrix of 16 × 16; number 1 represents the board shape, and number 2 represents the IC location. (C) The matrix representation of the top decaps using a matrix of 16 × 16. (D) The matrix representation of the bottom decaps using a matrix of 16 × 16

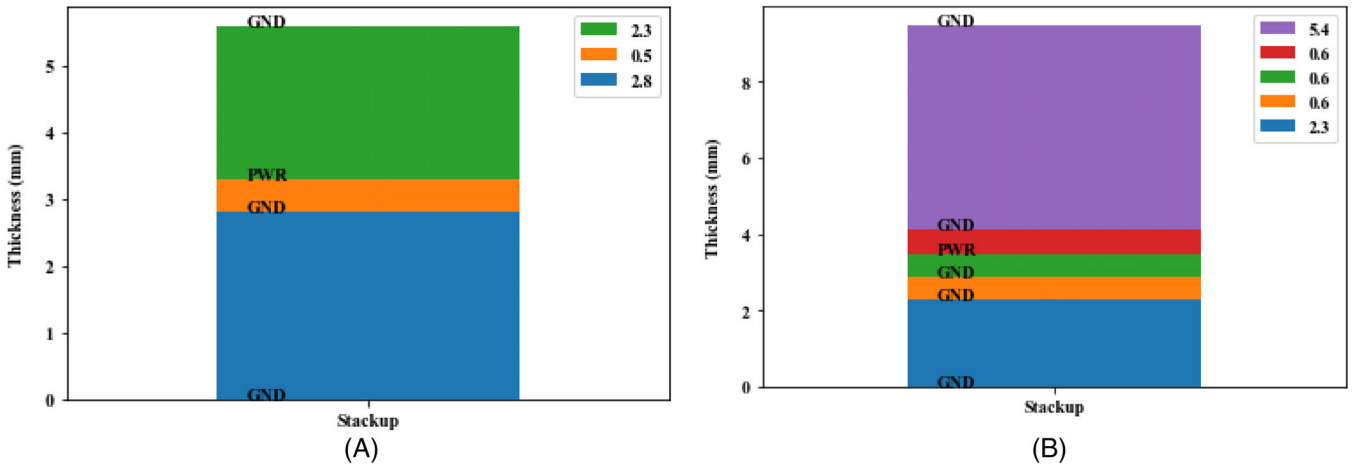

FIGURE 6 Two examples of randomly generated stackup. (A) Four layers. (B) Six layers

when the number of layers is less than 9). The last 8 elements of the 1 × 17 matrix represent the dielectric thickness in millimeters, in which 0 also means empty. This stackup matrix will be the second input matrix of the DNN. Figure 7 shows the matrix form for the two stackup examples in Figure 6.

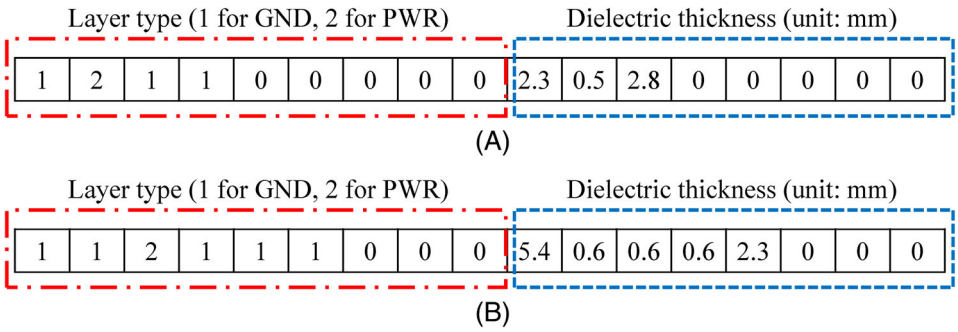

FIGURE 7 (A) The matrix representation of the stackup as shown in Figure 6A using a 1D matrix of 1 × 17. (B) The matrix representation of the stackup as shown in Figure 6B using a 1D matrix of 1 × 17

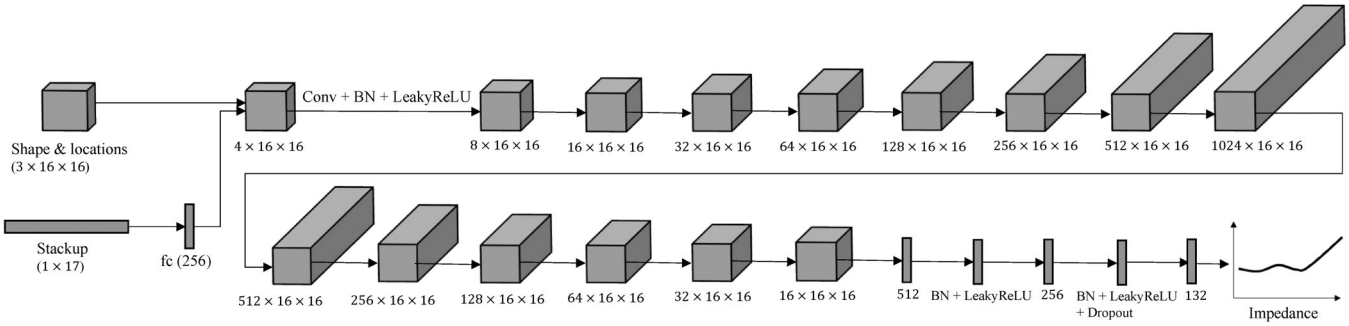

FIGURE 8 The detailed structure of the convolutional neural network (CNN)

3 | DNN TRAINING

As introduced earlier, there are two input matrices for the DNN—the first 3 × 16 × 16 matrix defines the board shape, IC location, and decap placement, and the second 1 × 17 matrix defines the stackup information. These two matrices have different dimensions. In this paper, a fully connected (FC) layer[16] is used to convert the 1 × 17 matrix to a 1 × 256 matrix first, which is further reshaped to a 16 × 16 matrix and cascaded with the 3 × 16 × 16 matrix. Thus, a 4 × 16 × 16 matrix is formed and then followed by a series of convolutional layers. The reason for combining the 1 × 17 matrix with the 3 × 16 × 16 matrix at the beginning of the neural network is to learn the influence of the stackup better with a deep structure of convolutional layers. The structure of the convolutional layers was further tuned and optimized until both the training and testing loss converged to low values, as will be introduced later, which indicates appropriate convolutional neural network (CNN) complexity for suppressing underfitting and overfitting effects. The detailed structure of the CNN[6] is depicted in Figure 8.

Starting from the 4 × 16 × 16 matrix, 14 convolutional layers are connected in series. In each convolutional layer, the kernel size is 3, the padding size is 1, and the stride is 1. In addition, each convolutional layer is followed by a batch normalization (BN) layer[17] and a Leaky ReLU activation layer.[18] After the convolutional layers, several FC layers are utilized to reduce the matrix size to 132, which is the size of the output impedance matrix that corresponds to the number of frequency points in the output impedance curve. A dropout layer[19] is applied between the last two FC layers to prevent overfitting.

By adopting the method of generating random board configurations, 13 000 PCBs with different IC locations, decap locations, and stackups were randomly generated. For each of these PCBs, the maximum number of decap locations was 19, and the BEM and the node voltage method were applied to calculate the Z-parameters. These Z-parameters were used repeatedly to connect with different decap combinations. For each PCB, 100 different decap placement scenarios, with different decap number (0–19) and different decap values (1–10), were randomly created, for a total number of 1.3 million groups of data. The entire data generation process took about 1 week. For each case, the decibel (dB) values of the impedance were used as the DNN output. The frequency range is from 10 kHz to 20 MHz.

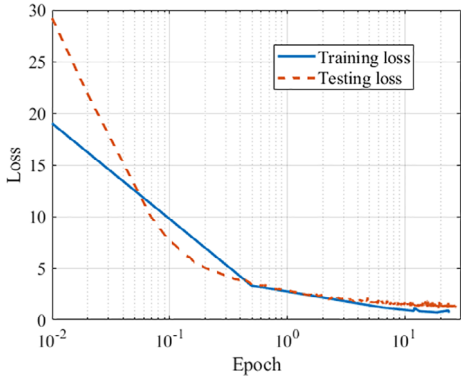

FIGURE 9 The convergence of the training loss and testing loss during the training process

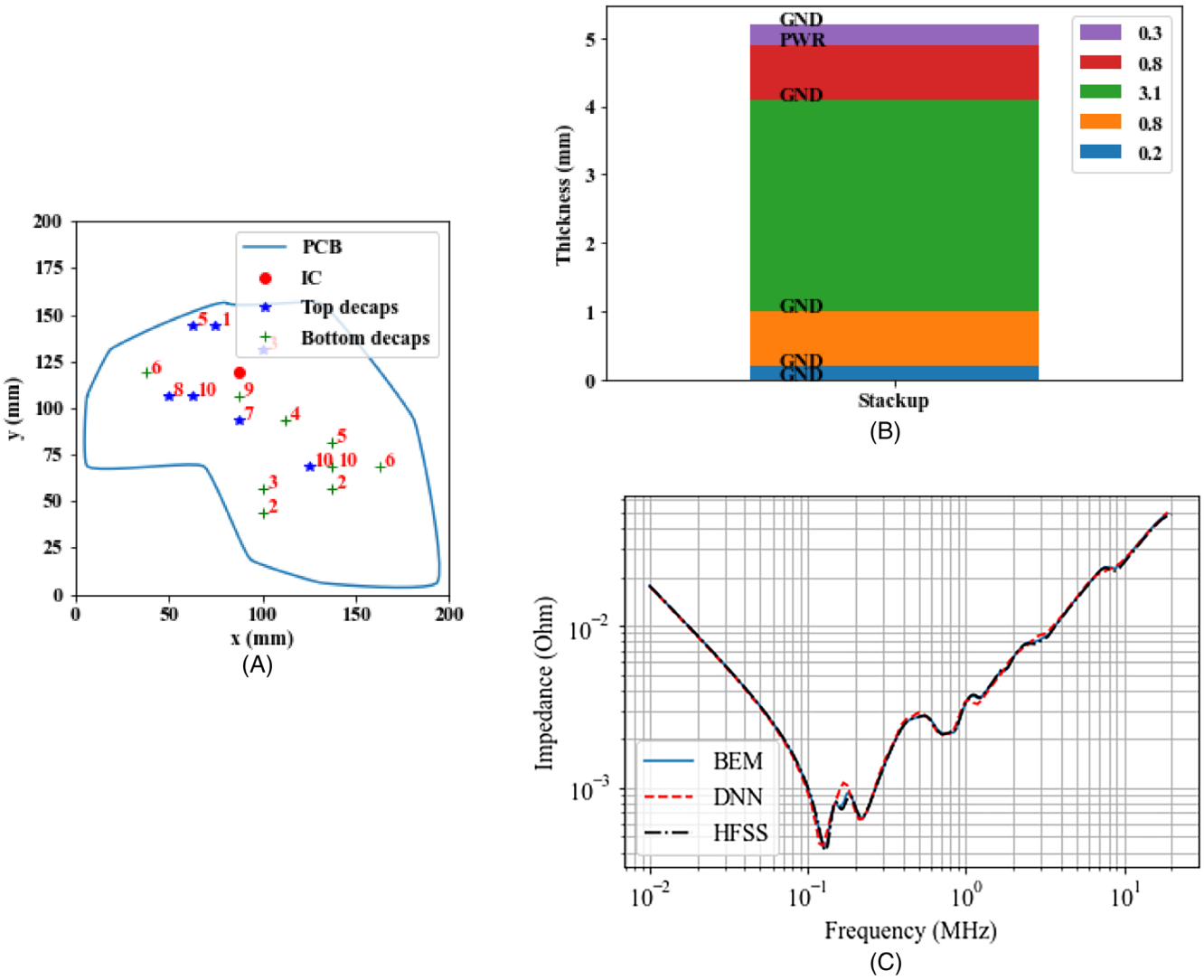

FIGURE 10 The first randomly selected test case. (A) Printed circuit board shape, IC location, and decap placement. (B) Stackup. (C) Comparison between the predicted impedance by the trained deep neural network and the calculated impedance by the boundary element method

Among all the generated data, 10 000 groups of data were used as a testing set, with the remaining used for training. The batch size was 128. The learning rate was 0.0001, and the Adam optimizer was utilized. The loss function was defined as the root mean square error (RMSE). One NVIDIA Tesla K80 GPU was used to accelerate the training. The

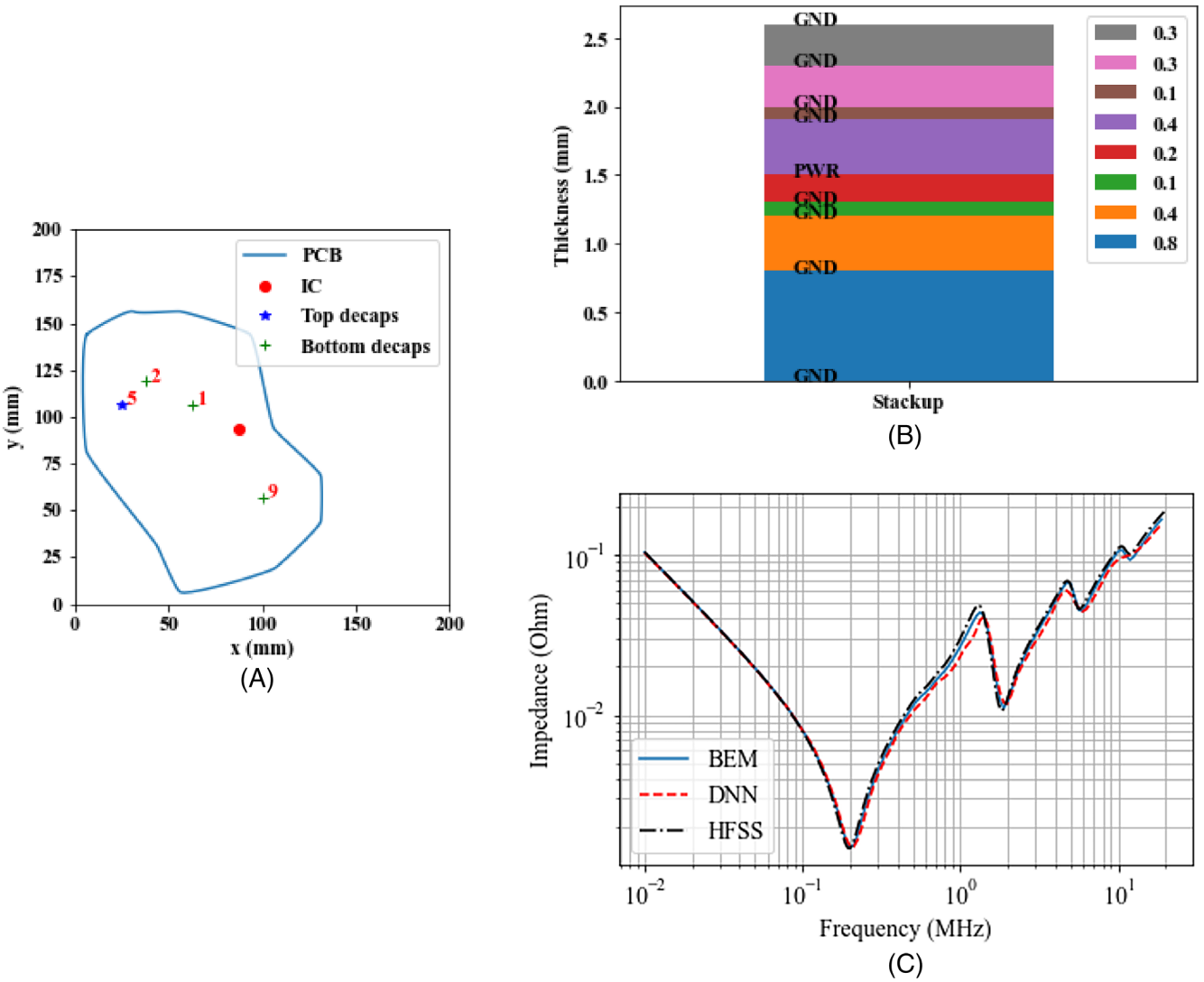

FIGURE 11 The second randomly selected test case. (A) Printed circuit board shape, IC location, and decap placement. (B) Stackup. (C) Comparison between the predicted impedance by the trained deep neural network and the calculated impedance by the boundary element method

TABLE 2 Time comparison

Methods	Case 1	Case 2
Full-wave simulation	35 min	40 min
Boundary element method	10 s	30 s
Deep neural network	0.1 s	0.1 s

training and the testing loss are plotted in Figure 9. After 20 epochs, which took about 80 hours, both the training and testing loss converged stably to a low value close to 1, which indicates that the RMSE for the testing cases is only approximately 1 dB.

4 | DNN TESTING

The trained DNN has a low testing loss as seen from Figure 9. To further validate how the trained DNN behaves in predicting the impedance curve, two test cases are randomly selected from the testing dataset. The validation results of

these two cases are shown in Figures 10 and 11. The impedance curves predicted by the trained DNN have a good agreement with the calculated curves by the BEM method as well as HFSS simulation results. Using full-wave commercial products to simulate the impedance for similar structures requires more than 30 min. The BEM method reduces the computation time for these two cases to 10 and 30 s, respectively. The trained DNN, however, only needs 0.1 s for both cases on a normal CPU, which is hundreds of times faster than the BEM method and tens of thousands of times faster than full-wave simulations. The detailed time comparison is listed in Table 2.

5 | CONCLUSIONS

In this paper, a novel concept of using deep learning to predict PDN impedance while considering the variations of board shape, stackup, IC location, and decap placement is proposed. A BEM and the well-known node voltage method are adopted to quickly calculate the PDN impedance for arbitrary board shapes and stackup, which allows the algorithm to generate 1.3 million groups of training data with different board shapes, stackup, IC location, and decap placement. A CNN is constructed and trained with the produced data. The trained CNN can predict the impedance accurately for the testing cases, with an RMSE of around 1 dB only. But the trained CNN has a much faster prediction speed than both full-wave simulations and the BEM method, using only 0.1 s.

This paper demonstrates the feasibility of using CNN for the high-dimensional problem of PDN impedance prediction. The number of possible combinations for the input parameters by considering the variations of board shape, stackup, IC location, and decap placement is an extremely large number that is hard to quantify. Only the number of decap combinations is 10^{20} in total, which is already a huge number, without considering the variations of board shape, stackup, IC location, and decap locations. Nevertheless, the CNN is still capable of handling such a complex scenario and achieving a decent generalization performance after being trained with abundant data and time. This deep learning approach can be a powerful tool for the application scenarios where a super-fast PDN impedance estimation is demanded, for example, at the design optimization stage. Assuming 10 000 iterations are needed for PDN design optimization (the detailed optimization method is not within the scope of this paper) to achieve a target impedance, using the BEM method will take more than 20 h. However, using the trained CNN will only consume 20 min.

Since this paper assumes the decaps to be distributed among discrete locations, more work can be done in the future to consider continuous decap locations and the effect of different decap sizes and rotation angles. In addition, the variation of IC pin configurations can also be taken into account.

ACKNOWLEDGMENTS

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are openly available in GitHub at https://github.com/lingzhang0319/PDN-Impedance-Prediction-Using-Deep-Learning/tree/master.

REFERENCES

1. Kim J, Ren L, Fan J. Physics-based inductance extraction for via arrays in parallel planes for power distribution network design. *IEEE Trans Microw Theory Tech*. 2010;58(9):2434-2447.
2. Kim J, Shringarpure K, Fan J, Kim J, Drewniak JL. Equivalent circuit model for power bus design in multi-layer PCBs with via arrays. *IEEE Microw Wirel Compon Lett*. 2011;21(2):62-64.
3. Wei L, Li L, Shringarpure K, et al. Plane-pair PEEC model for power distribution networks with sub-meshing techniques. *IEEE Trans Microw Theory Tech*. 2016;64(3):733-741.
4. Zhang Y, Feng G, Fan J. A novel impedance definition of a parallel plate pair for an intrinsic via circuit model. *IEEE Trans Microw Theory Tech*. 2010;58(12):3780-3789.
5. Friedrich M, Leone M. Boundary-element method for the calculation of port inductances in parallel-plane structures. *IEEE Trans Electromagn Compat*. 2014;56(6):1439-1447.
6. Krizhevsky A, Sutskever I, Hinton GE. Imagenet classification with deep convolutional neural networks. *Commun ACM*. 2017;60(6):84-90.
7. Young T, Hazarika D, Poria S, Cambria E. Recent trends in deep learning based natural language processing. *IEEE Comput intelligenCe Mag*. 2018;13(3):55-75.

8. Silver D, Schrittwieser J, Simonyan K, et al. Mastering the game of go without human knowledge. *Nature*. 2017;550(7676):354-359.
9. Schierholz CM, Scharff K, Schuster C. Evaluation of neural networks to predict target impedance violations of power delivery networks. Paper presented at: 2019 IEEE 28th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS) 2019: 1–3.
10. Sourav S, Roy A, Cao Y, Pandey S. Machine learning framework for power delivery network modelling. Paper presented at: 2020 IEEE International Symposium on Electromagnetic Compatibility Signal/Power Integrity (EMCSI) 2020: 10–15.
11. Park H, Park J, Kim S, et al. Deep reinforcement learning-based optimal decoupling capacitor design method for silicon interposer-based 2.5-D/3-D ICs. *IEEE Trans Compon Packag Manuf Technol*. 2020;10(3):467-478.
12. Cecchetti R, Paulis DF, Olivieri C, Orlandi A, Buecker M. Effective PCB decoupling optimization by combining an iterative genetic algorithm and machine learning. *Electronics*. 2020;9(8):1243.
13. Zhang L, Juang J, Kiguradze Z, Pu, S. Jin, S. Wu, Z. Yang, and Chulsoon Hwang, Efficient DC and AC impedance calculation for arbitrary-shape and multi-layer PDN using boundary integration. Paper presented at: IEEE Transactions on Electromagnetic Compatibility; to be submitted 2021.
14. Ansys. https://www.ansys.com/products/electronics/ansys-hfss.
15. https://stackoverflow.com/questions/50731785/create-random-shape-contour-using-matplotlib.
16. Basha SS, Dubey SR, Pulabaigari V, Mukherjee S. Impact of fully connected layers on performance of convolutional neural networks for image classification. *Neurocomputing*. 2020;378:112-119.
17. Ioffe S, Szegedy C. Batch normalization: accelerating deep network training by reducing internal covariate shift. Paper presented at: International Conference on Machine Learning arXiv Preprint arXiv:1502.03167 2015.
18. Xu B, Wang N, Chen T, Li M. Empirical evaluation of rectified activations in convolutional network. arXiv Preprint arXiv:1505.00853 2015.
19. Srivastava N, Hinton G, Krizhevsky A, Sutskever I, Salakhutdinov R. Dropout: a simple way to prevent neural networks from overfitting. *J Mach Learn Res*. 2014;15(1):1929-1958.

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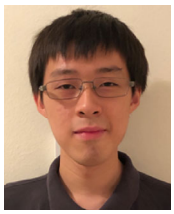

Jack Juang is an MS Degree student with the EMC Laboratory at Missouri University of Science and Technology (S&T). He received his BS degree in Electrical Engineering from S&T in 2020. His research interests include power distribution network modeling and optimization. He has been involved in projects relating to the optimization of decoupling capacitor placement and RF susceptibility of smart devices.

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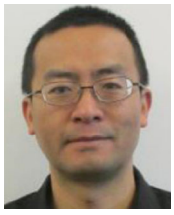

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