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Transient Response of ESD Protection Devices for a High-Speed I/O Interface

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***Abstract*—System-efficient electrostatic discharge (ESD) design (SEED) models of a diode and transient voltage suppressor (TVS) were developed to study their transient response in a high-speed input/output interface. Previously reported SEED models were improved to strengthen their convergence stability and facilitate accurate predictions over a wide range of conditions. These improvements were required to accurately capture the race conditions between the TVS and ON-chip diode, where the diode's turn ON may prevent turn ON of the TVS. Simulations and measurements were performed to demonstrate the impact of the ESD pulse's rise time on race conditions. During a race, results showed the worst-case quasi-static diode current could be twice as high for long rise-time pulses than for short rise-times where the TVS does not turn ON, and ON-chip diode current may be larger at low test voltages than at high test voltages where the TVS does turn ON. Adding a small passive impedance between the external TVS and the ON-chip diode helps the TVS turn ON and reduce the current through the ON-chip diode by more than 50%. Similarly, lengthening the trace between the TVS and diode could reduce ON-chip diode current by up to a factor of two.**

***Index Terms*—Electromagnetic immunity, electrostatic discharge (ESD), integrated circuit (IC), system efficient ESD design (SEED), system-level ESD, transient-voltage suppression.**

I. Introduction

With the increasing speed of digital communication channels, the input/output (I/O) interface is at higher risk to electrostatic discharge (ESD) due to the thinner gate oxide of the I/O drivers and other FET characteristics. For a 35 nm complementary metal oxide semiconductor technology, the gate oxide film can be as thin as 1.2 nm, making it susceptible to damage from relatively small gate-to-source or gate-to-drain voltages. As logic gates shrink, there is increasing pressure to shrink the size of I/O cells, which means that the energy transferred during an ESD event can easily cause thermal damage to the ON-die drivers and associated ESD protection [1].

Although the I/O pin is designed with ON-chip diode protection, the protection may not be sufficient to guarantee robust ESD design due to its limited capability for energy dissipation [2]. An external transient voltage suppressor (TVS) device can clamp the peak voltage seen by an IC during an ESD event and can significantly reduce the current into the I/O pin [3]–[5].

There is a common misconception that meeting component-level immunity standards [6] will ensure system-level immunity [7]. Component-level ESD tests use human body model ESD pulses with long rise times of up to tens of nanoseconds [8], which may be insufficient to guarantee passing the IEC system-level test [7]. The IEC-61000-4-2 standard, for example, specifies use of the human metal model, which has a much faster initial rise time and a higher peak. ESD events in real systems, which may be modified through coupling and parasitics between the location of the ESD event to the point where it encounters the IC and TVS, may differ substantially from the standard pulses [10].

SEED simulation provides a methodology for ensuring the system's robustness against ESD events. The TVS device characteristics alone do not ensure it will turn ON when placed on the printed circuit board (PCB) along with the IC. Test structures including the external TVS and the ON-chip ESD protection were used to investigate race conditions in [11] and [12], to understand when the TVS would and would not protect the IC and the influence of passive components and the ESD pulse rise time on TVS performance. Results showed that an extra inductance between the TVS and ON-chip diode, and the associated rapid voltage change at the TVS during a fast transient event, is important for helping the external TVS turn ON to protect the IC.

The external TVS and ON-chip ESD protection diode were modeled in [11] and [12] using the simulation framework shown in Fig. 1 [13], [14]. This framework can accurately model the quasi-static IV characteristics and the transient behavior of the ESD protection device. The framework includes both a passive linear network and a nonlinear modeling block to account for conductivity modulation and snapback delay. The simulation model used in [11] was preliminary and used to predict the transient behavior of a protection device for an ideal TLP source, however, the convergence stability of the model and

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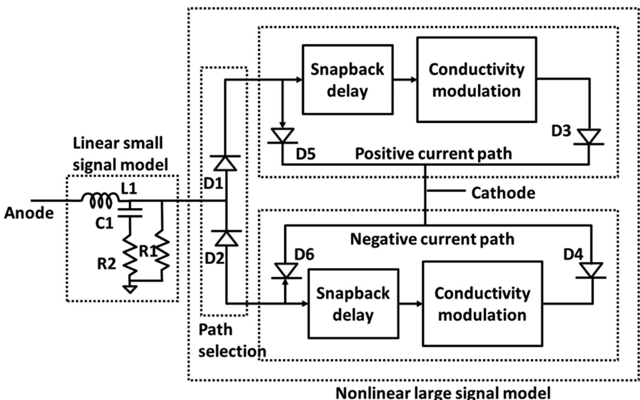

Fig. 1. SEED model framework for TVS devices.

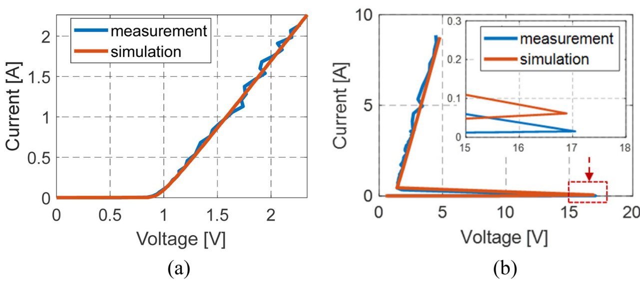

Fig. 2. Quasi-static IV characteristic for the ON-chip diode and the external TVS device. (a) IV curve for on-chip diode. (b) IV curve for external TVS.

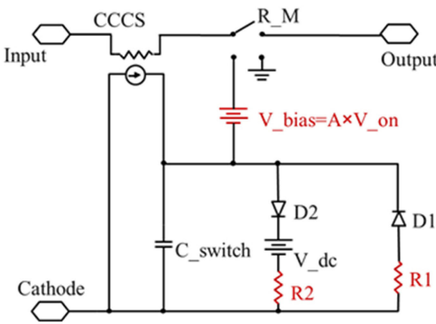

Fig. 3. Conductivity modulation model.

accuracy need to be improved if the model is to be implemented in a complex system with multiple ESD protection devices. This model will be improved in the following article using a better-defined switch for the conductivity modulation and the snapback delay module. Improvements were also made to the overall measurement methodology.

The TVS model will be developed in Section II and validated against TLP measurements. In Section III, the model will be incorporated into a larger model of an I/O port, including a TVS device and ON-chip diode, to evaluate the impact of the TLP rise time and the use of passive impedances between the TVS and the ON-chip diode on the TVS performance. In Section IV, the effects of including a filter between the TVS and I/O pin and the location of the TVS are investigated through simulation.

II. SEED Simulations

Ensuring an IC does not fail during a race condition, where the ON-chip diode turns ON and prevents the TVS from turning ON and protecting the diode, is an important part of evaluating the quality of an ESD protection strategy. To predict race conditions and to understand the effects of passive impedances between the external TVS and the ON-chip diode and the effects of ESD pulse rise time, it is essential to model the TVS device transient response accurately. Several improvements to the TVS and diode models from [11] are implemented and tested in the following Section II-A silicon-based ESD protection device (NExperia PUSB3FR4) for ultrahigh-speed interfaces was used as the external TVS protection and a unidirectional silicon-based ESD protection device (NExperia PESD5V0L1USF) was used to represent the ON-chip protection diode inside the IC. Circuit simulations were performed using the advanced design system SPICE simulator.

A. SEED Model Improvements

Improvements were made to the portions of the device model responsible for conductivity modulation, snapback delay, and its quasi-static IV device behavior.

1) Quasi-Static IV: For a nonsnapback diode, the quasi-static IV characteristics can be represented using a modified PN junction model with diodes D3 and D4, as shown in Fig. 1. For the external TVS, the snapback behavior needs to be accurately modeled to show the threshold voltage above which the TVS starts to turn ON. Small errors in the turn-ON threshold for either the diode or TVS were found to substantially change the simulation result during a race condition. Fine tuning the model to accurately capture the IV curve at the turn-ON point is crucial to achieve accurate results. The quasi-static IV for the ON-chip diode and the external TVS after fine tuning of the model are shown in Fig. 2.

2) Conductivity Modulation: The conductivity modulation model predicts the "overshoot" in the TVS or diode voltage beyond the voltage predicted by the quasi-static IV curves and the inductance associated with the small signal model. Conductivity modulation results from limitations in the rate of change of carrier concentrations in the device. Overshoot also occurs from parasitic inductance, which is accounted for separately in the small-signal model block. The model of conductivity modulation in [11] used only the components shown in black in Fig. 3. This circuit allows for a delay in the turn-ON behavior of the diode but causes a relatively fast transition between the case where the diode is "OFF" and not conducting to the case where it is "ON". The sudden change in state can cause stability issues in the simulation.

The resistors R1 and R2 were added to the model, as shown in Fig. 3, to avoid nonconvergence that sometimes occurs when using this model along with another nonlinear device (e.g., a TVS and diode together). The bias voltage was added to allow for better tuning of the variable resistance of the voltage-controlled switch and allows a smooth transition of the diode from an "OFF" to an "ON" state where its behavior is dominated by its quasi-static characteristics. The switch resistance transition behavior

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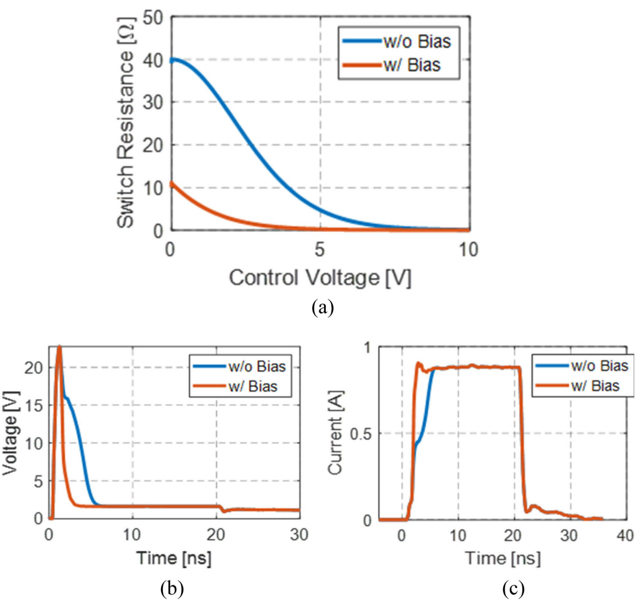

Fig. 4. Impact of the bias voltage on the ON-chip diode conductivity modulation model. (a) Switch resistance as a function of control voltage with/without a bias voltage. (b) Transient voltage waveform. (c) Transient current waveform.

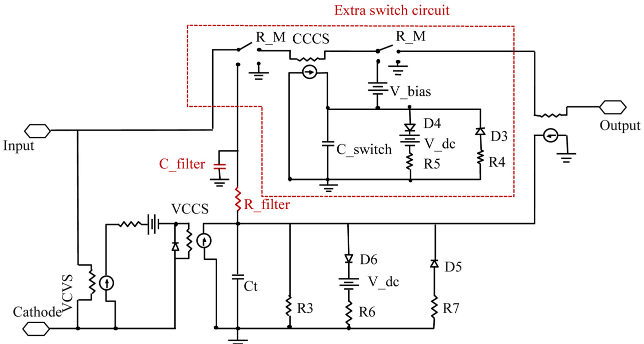

Fig. 5. Snapback delay model. The added components are highlighted in red.

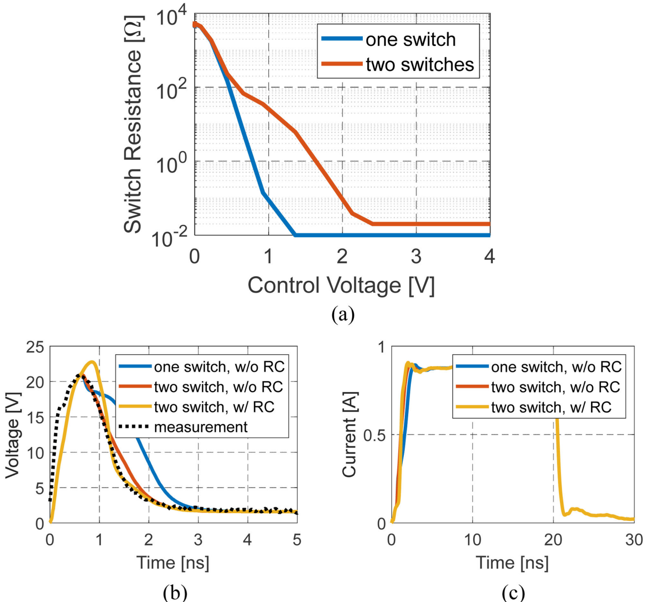

Fig. 6. Effect of adding additional voltage-controlled switch and *RC* circuit to snapback delay model for the external TVS; The TLP voltage was 60 V. (a) Switch resistance as a function of control voltage with/without added voltage-controlled switch. (b) Transient voltage waveform. (c) Transient current waveform.

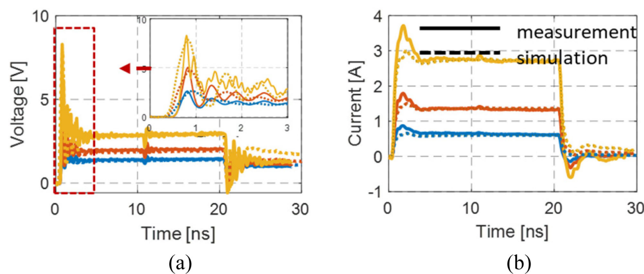

Fig. 7. Transient waveforms for the ON-chip diode for different applied TLP voltage levels. The color indicates the TLP voltage: blue: 19 V, orange: 42 V, yellow: 84 V. (a) Transient voltage waveform. (b) Transient current waveform.

before and after adding the additional components is shown in Fig. 4(a). The corresponding transient response of the ON-chip diode during a TLP event is shown in Fig. 4(b) and (c).

3) Snapback Delay: A similar methodology was used to improve the snapback delay model, as shown in Fig. 5. An additional voltage-controlled switch and a *RC* integration circuit was added to further expand the ability to tune the turn ON time and resistance of the switch. The change in the switch resistance with the control voltage is shown in Fig. 6(a). The effect of the additional switch and the *RC* circuit on the transient waveforms are shown in Fig. 6(b) and (c). While the comparison of the time-domain voltage over time is slightly worse with the *RC* circuit than without in this case, we found this circuit was required to maintain the accuracy and stability of simulations when pairing a TVS and a diode together.

B. Transient Response of TVS and Diode

The transient current and voltage waveforms for the TVS (NExperia PUSB3FR4) and ON-chip diodes (NExperia PESD5V0L1USF) are shown in Figs. 7 and 8 when reacting to TLP pulses of different magnitudes. A TLP was used as an excitation source because of its good repeatability and because of the ease of changing its rise time using low pass filters. The ON-chip diode turns ON for each of the waveforms in Fig. 7, as they are above its 0.7 V turn-ON voltage. The external TVS does not turn ON until the TLP source voltage is above 28 V. The simulation models do a reasonably good job of predicting both the transient and steady-state voltage and current levels for the ON-chip diode and the external TVS.

III. In-System Transient Response

Once good models of the TVS and ON-chip diode were created, these models were used to investigate the interaction between the devices when used together in a system, the impact of adding passive impedances between them, and the impact of the pulse rise time.

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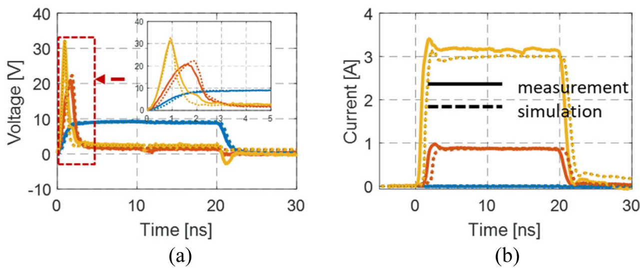

Fig. 8. Transient waveforms for the external TVS for different applied TLP voltage levels. The color indicates the TLP voltage: blue: 9 V, orange: 28 V, yellow: 93 V. The TVS does not turn for less than a 28 V TLP voltage. (a) Transient voltage waveform. (b) Transient current waveform.

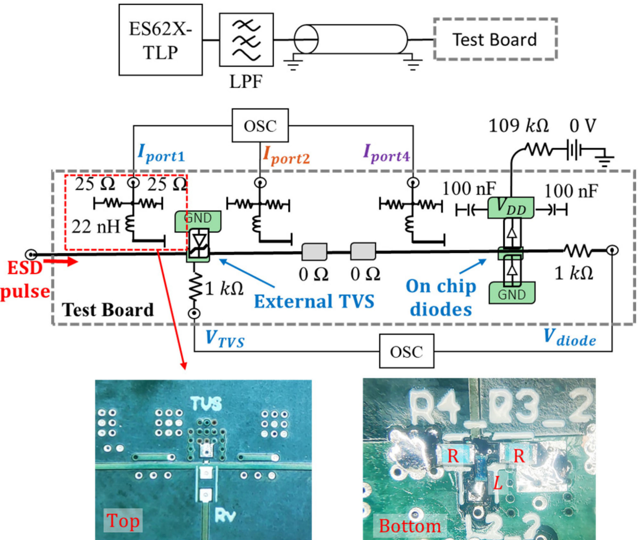

Fig. 9. Test board allows for device current and voltage measurements.

A. Measurement Setup

A test board was built that simulates a typical I/O configuration consisting of an ON-chip diode and an external TVS, as shown in Fig. 9. The board allows for measurement of the voltage and the current associated with each device. Two 1-kΩ resistors (R_V) connected at the location of the TVS and the ON-chip diode serve as a 21:1 probes of the voltage at each device. Current was measured using inductive probes integrated into the PCB, which have been used in previous studies [11]. Current probes were placed just before and after the TVS (I_{port1} and I_{port2}, respectively), so the TVS current could be determined from the difference in currents measured by the two probes. Another current probe (I_{port4}) was placed just before the ON-chip diode to capture the current to the ON-chip diode.

The PCB layout was improved over [11] by reducing the length of the inductive probes from 4 mm to 2.5 mm to better capture high-frequency components, and by "shielding" the probe components from the TVS and trace by placing them on the other side of the board (see Fig. 9). The induced voltage measured by the loop probe was converted to current using the reconstruction process discussed in [11]. In [11], only the transfer impedance from the input port to the probe output was used in the reconstruction. Here, the full S-parameter matrix was used, as including the reflection coefficient further improves the accuracy. In this case, the transfer impedance of the probe is given by

$$Z_T = \frac{Z_0 * S_{21}}{1 - S_{11}} = \frac{50 * S_{21}}{1 - S_{11}}. \tag{1}$$

The accuracy of the probe was demonstrated by comparing the reconstructed current with a direct measurement of current at a matched termination at the end of the board. The difference between the current found using the integrated loop probe and the current found at the matched termination was less than 5% for a 20 ns TLP pulse.

The current probes were characterized using a Keysight E5071C Vector Network Analyzer. An 8 GHz Tektronix DPO 70804 digital oscilloscope was used to measure the voltage at the current probes and for the ON-chip diode measurement. A 2 GHz Rohde and Schwarz RTO2022 oscilloscope was used to measure the voltage at the TVS. The current probe measurements required an oscilloscope with at least a 4 GHz bandwidth to achieve a good current reconstruction for a current pulse with a fast rising edge.

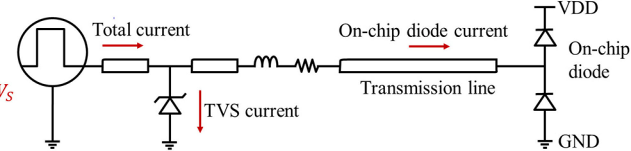

Fig. 10. Circuit diagram for the test board and TLP source. The added resistance and inductance were varied among experiments.

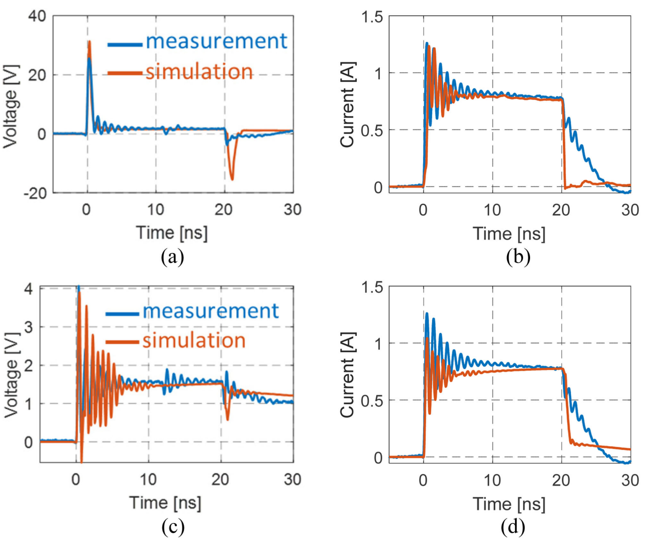

Fig. 11. Transient waveforms for the external TVS and the ON-chip diode when a 45 V TLP was applied to the test board in Fig. 9. (a) Voltage at external TVS. (b) Current through external TVS. (c) Voltage at on-chip diode. (d) Current through on-chip diode.

B. Circuit Simulation

Fig. 10 shows a simplified circuit diagram for the test board. The resistor and inductor shown in the figure represent passive components, which could be added between the TVS and ON-chip diode. These could be installed at the pad locations in

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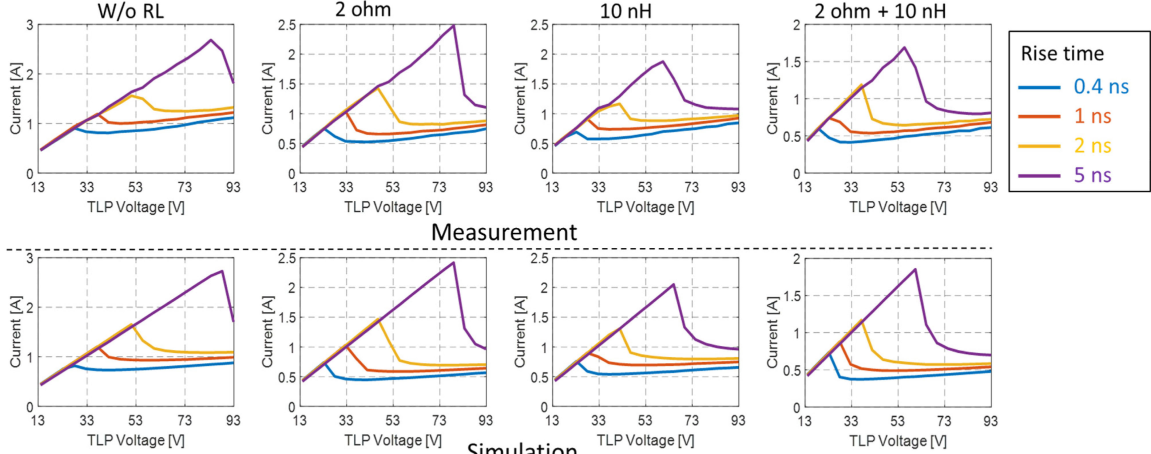

Fig. 12. Quasi-static current through the ON-chip diode as a function of rise time and TLP voltage. Rise time varies from 0.4 ns to 5 ns. The current was measured using the current probe at I_{port4} shown in Fig. 9.

the middle of the test-board trace, as shown in Fig. 9. When no inductor or capacitor was used, these pads were "shorted" with 0-ohm resistors. It is worthwhile to note that the microstrip trace between the TVS and the ON-chip diode must be modeled, as a lossy transmission line. This transmission line impacts both the level and delay of the reflections between the devices and is critical for accurate SEED model results.

Example waveforms are shown in Fig. 11 for a 45 V TLP. The simulation accuracy is improved using the revised SEED model compared to the results in [11], especially for the first 0–5 ns when the transient response is dominated by the conductivity modulation and snapback delay model. The quasi-static current matches the measurements within 5%. Similar performance was observed at other TLP levels.

C. *Impact of TLP Rise Time*

The peak voltage on the trace is positively correlated with the derivative of current as a result of the parasitic inductance of the devices. The rise time of the ESD pulses will, thus, play a significant role in the transient response of the system and the turn-ON behavior of the TVS. Ultimately, the designer wants to limit the current flowing into the ON-chip diode.

Fig. 12 shows the ON-chip diode quasi-static current at different TLP voltage levels and different TLP pulse rise times. The measured data were obtained by increasing the TLP voltage from 13 V to 93 V in 5 V steps. The quasi-static current through the ON-chip diode current starts to drop when the TVS turns ON. The point where the TVS turns ON is highly dependent on the TLP pulse rise time since the voltage across the ON-chip diode inductance goes up with the rise time. For example, in the case where there are no components between the external TVS and the ON-chip diode, the TVS turns ON with a 28 V TLP voltage with a pulse rise time of 0.4 ns, but does not turn ON until the TLP voltage exceeds 83 V for a pulse rise time of 5 ns. For the slower pulse rise time the ON-chip diode current can reach as high as 2.6 A, which may damage the IC. For the faster pulse the current is limited to 1 A. Fig. 13 shows examples of the transient waveforms for different excitation rise times at the same TLP

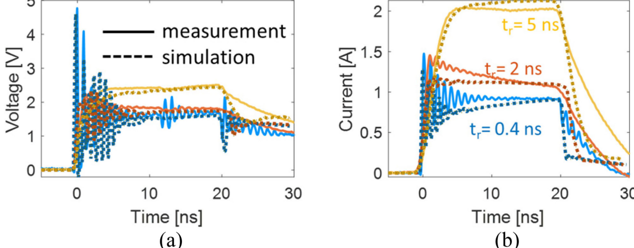

Fig. 13. Transient voltage and current for the ON-chip diode when applying 65 V TLPs with different rise times (no passive components added). (a) Voltage at the on-chip diode. (b) Current through the on-chip diode.

voltage level for the case when there are no components placed between the external TVS and the ON-chip diode. A low pass filter between the TLP source and the board was used to vary the rise time from 0.4 ns to 5 ns while the TLP voltage level remained at 65 V. The TVS turns ON for rise times less than 5 ns and does not turn ON for the 5 ns rise-time pulse. The ON-chip diode current is much higher for the slow-rise time pulse than for the other cases. The simulation accurately predicts the measured results.

D. *Impact of Components Between the TVS and on-Chip Diode*

Series resistance or inductance between the TVS and ON-chip diode contributes to the development of voltage at the external TVS and will, thus, help ensure an earlier turn ON of the TVS. Figs. 12 and 14 show the impact of placing different values of resistance or inductance between the TVS and diode. The component values were selected to be comparable to the parasitic inductance or resistance of a signal line or comparable to the inductance of a common-mode choke widely used for USB 3.0 I/O interfaces. Results show the impact of the components both as a function of the TLP voltage and of the TLP rise time.

As expected, adding resistance or inductance allows the external TVS to turn ON for a lower TLP voltage, thus reducing the worst-case current flowing to the ON-chip diode.

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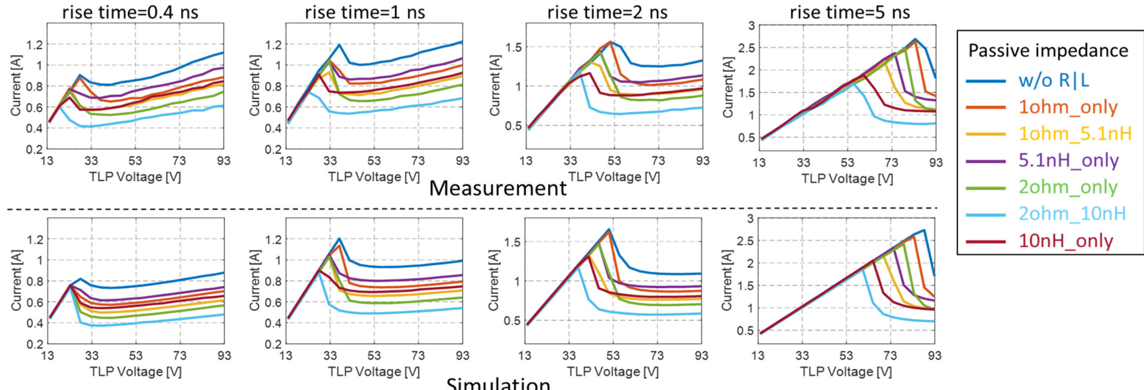

Fig. 14. Quasi-static current through the ON-chip diode when different passive impedances were placed between the external TVS and the ON-chip diode. The current was measured using the current probe at I_{port4} shown in Fig. 9.

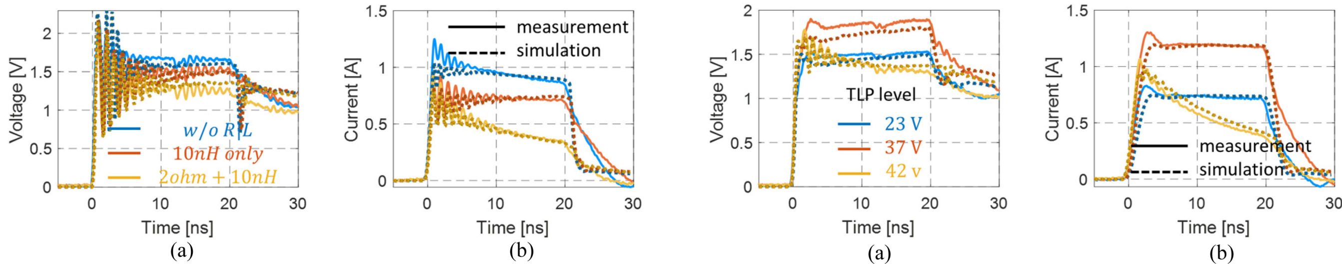

Fig. 15. Transient waveform for the ON-chip diode with different passive impedances between the external TVS and the ON-chip diode. The TLP voltage was 45 V. (a) Voltage at on-chip diode. (b) Current through on-chip diode.

Fig. 16. Transient waveform for the ON-chip diode at different TLP voltages. (a) Voltage at the on-chip diode. (b) Current through the on-chip diode.

these components also resulted in lower diode currents even at voltages where they are not required to turn ON the TVS. For example, for the 5 nS rise-time, the turn-ON voltage was reduced from 83 V with no components to 53 V when a 2 ohm resistor and 10 nH inductor were added between the TVS and diode. An example of transient waveform is shown in Fig. 15 when the TLP rise time was 0.4 ns. The current through the ON-chip diode was reduced by 50% when a 2 ohm resistor and 10 nH inductor were added between the TVS and diode. Depending on the rise time, the worst-case diode current was reduced by 60–70% by adding both resistance and inductance. The current for TLP voltages above the point where the TVS is firmly turned ON (e.g., above 50 V for a 1 ns rise time) were reduced by 50–60%.

Figs. 12 and 14 show that the ON-chip diode current increases with the TLP voltage until the external TVS turns ON. At that point, the diode current quickly drops for a higher TLP voltage before slowly rising again. Fig. 16 shows a case where the ON-chip diode quasi-static current is the same for both a 23 V and 42 V TLP, and is higher for a 37 V TLP. The fact that higher diode currents may be seen for lower TLP voltages is worth noting, as it means that passing the highest TLP voltage test does not guarantee that failures will not occur at lower levels.

IV. Discussion

Accurately measuring the on-board current and voltage waveforms during rapidly changing transients is challenging. The modified PCB design improves the measurement accuracy of the integrated loop probes, especially for the first 0–5 ns of the ESD pulse. To improve results, we provided an electric field shield between the trace and the probe, used a shorter coupling stub trace, and placed all other probe components on the bottom side of the board to reduce the direct coupling from the trace to other portions of the probe circuitry. Results were also improved by using a more accurate calibration process than in [11], which used only the transfer impedance of the probe. Here, the full two-port S-parameter matrix between the trace and the probe was used in the deconvolution process to determine trace current. These modifications to the measurement process were required to get a good match between measurements and simulations.

The simulation model presented in [11] is able to determine the TLP voltage and ON-chip diode current when the external TVS starts to turn ON, but there are noticeable discrepancies between the measured and simulated transient waveforms, especially for the first 0–5 ns of the ESD pulse. These discrepancies are due to the insufficient accuracy of the SEED model. The modeling framework was improved here using additional switching components to allow finer tuning of the model, and to prevent instability issues during simulations. A smooth turn-ON transition is particularly important when there are substantial interactions between the TVS and diode through reflections along the trace transmission line. Very small errors in the model could lead to large errors in the simulation of the system, which includes both the TVS and diode. The simulated transient waveforms match

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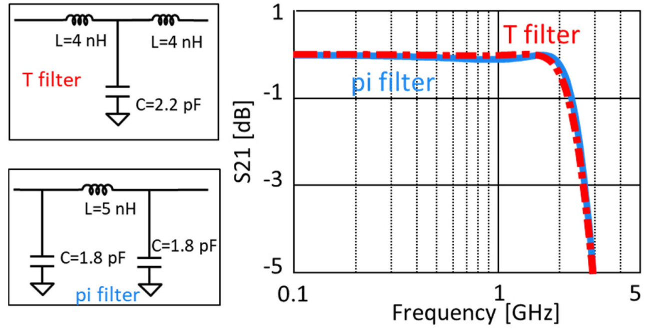

Fig. 17. T filter and pi filter circuit and their frequency response.

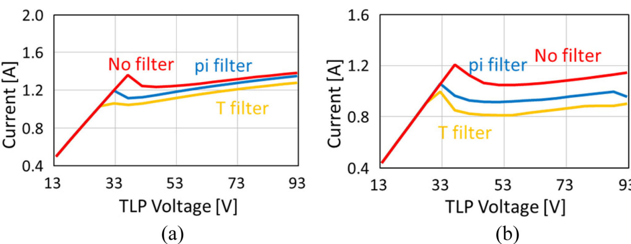

Fig. 18. Peak current and quasi-static current through the ON-chip diode as a function of TLP voltage and the filter configuration placed between the external TVS and the ON-chip diode. (a) Impacts on the peak current. (b) Impacts on the quasi-static current.

the measured diode and TVS voltage and currents within 10%. The TLP voltage level and the diode current when the external TVS starts to turn-ON matches the measurements within 20%.

Added resistance or inductance can significantly improve the turn ON of the TVS and decrease the worst-case current seen by the ON-chip diode. While even a 2-ohm resistance can have a substantial impact on performance, signal integrity issues should be carefully considered before adding any impedances between the devices.

Filtering of the signal on the USB line can also have an impact on TVS turn ON. To demonstrate, two low pass filters with different topologies but same frequency response were placed between the external TVS and the ON-chip diode. Fig. 17 shows the frequency response of the filters. The peak current and quasi-static current versus the TLP input voltage are compared in simulation for the different filters in Fig. 18. Similar to adding other impedances between the TVS and diode, the external TVS turns ON at a lower voltage level when adding the filters since the inductance of the filter increases the peak voltage at the TVS. The worst-case current through the ON-chip diode is reduced by 20% using the T filter. Although the pi filter has a similar frequency response as the T filter, it reduces the peak current by less (10%) than the T filter because of its lower overall inductance and lower input impedance at low frequencies.

The location of the TVS relative to the IC has been reported to have a strong impact on the TVS behavior [16]. To test this possibility, the distance between the TVS and the ON-chip diode was studied in simulation. The diode peak current and quasi-static current versus the TLP voltage is compared in Fig. 19 for distances of 2.5, 4.5, and 6.5 cm. The closer the TVS to the ON-chip diode, the higher the TLP voltage before the TVS

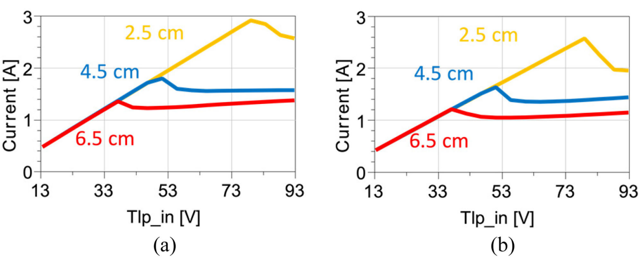

Fig. 19. Peak current and quasi-static current through the ON-chip diode as a function of the distance between the TVS and diode and the TLP voltage. (a) Peak current. (b) Quasi-static current.

turns ON. When the TVS is placed 2.5 cm away from the ON chip diode, the external TVS does not turn ON until the TLP voltage exceeds 76 V. When the TVS is placed 2.5 cm away the worst case diode current is roughly twice as high as at 6.5 cm. The current peak reaches 2.9 A, which indicates a higher risk of damage to the IC.

V. Conclusion

The transient response of an external TVS and ON-chip diode placed together in a configuration typical of a high-speed signal I/O interface was studied through measurements and simulation. The SEED models of the TVS and diode were improved by smoothing the transition of the device from "OFF" to "ON" at the end of the conductivity modulation or the start of snapback in order to obtain stable simulations. Improvements to the test board to limit transient coupling to the ON-board current probe and improvements to the calibration process were made to enhance the accuracy of transient voltage and current measurements. The SEED models presented here accurately predicted the current and voltage associated with an external TVS and an ON-chip diode for a wide range of TLP voltages and rise times, and when adding passive components between the two devices.

Careful selection of the TVS protection device is critical for ESD design. Adding components to provide an additional impedance between the external TVS and the ON-chip diode can significantly improve the ability of the TVS to protect the IC. The modeling process outlined here can help the design engineer to intelligently select protection devices and other components to maximize protection against a range of transient events while also ensuring the signal integrity of the design. Models may also be used to predict what conditions (e.g., rise-times and voltages) may cause the worst-case current at the diode so that testing and protection schemes may be adjusted accordingly.

Results demonstrate the importance of a thorough simulation strategy as the ON-chip diode may be stressed more at a lower test voltage than a higher test voltage when a race condition between the TVS and ON-chip diode occurs. For example, in one case shown here the ON-chip diode current was 2.5 times higher at a lower test voltage than the highest voltage under test. These race conditions become more important for slow rise time events that may be seen in-practice but are not part of standard test protocols.

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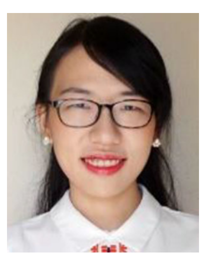

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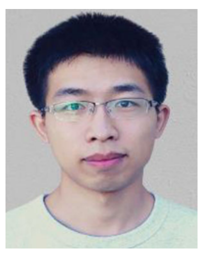

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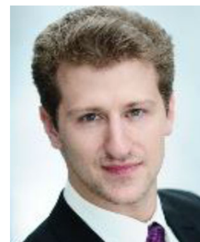

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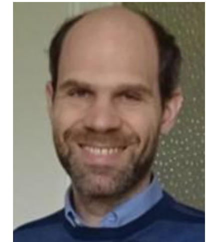

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