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Electrical Parameters Extraction of CMOS Floating-Gate Inverters

Extracción de parámetros eléctricos de inversores CMOS de compuerta flotante

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Abstract

This work provides an accurate methodology for extracting the floating-gate gain factor of CMOS floating-gate inverters with a clock-driven switch for accessing temporarilly to the floating-gate. With the methodology proposed in this paper, the factor and other parasitic capacitances coupled to the floating-gate can be easily extracted in a mismatch-free approach. This parameter plays an important role in modern analog and mixed-signal CMOS circuits, since it limits the circuit performance. Theoretical and measured values using two test cells, fabricated in a standard double poly double metal CMOS AMI-ABN process with 1.2 m design rules, were compared. The extracted parameters can be incorporated into floating-gate PS pice macromodels for obtaining accurate electrical simulation.

Keywords: FG-inverter, neuMOS, floating-gate.

Resumen

En este trabajo se brinda una metodología precisa para la extracción del factor de ganancia de la compuerta flotante en inversores CMOS, que constan de un interruptor para acceder temporalmente a la compuerta flotante. Con la metodología propuesta, el factor y otras capacitancias parásitas acopladas a la compuerta flotante pueden ser extraídas. Estos parámetros son de mucha importancia, ya que juegan un papel importante en el desempeño de circuitos analógicos y de señal mixta. La comparación entre cálculos teóricos y simulaciones es hecha utilizando dos celdas de prueba fabricadas de tecnología AMI ABN de 1.2 m, a través de la organización MOSIS. Los parámetros extraídos pueden ser incorporados a macromodelos en PSpice para obtener simulaciones más precisas.

Descriptores: *inversor de compuerta flotante, NeuMOS, compuerta flotante.*

Introduction

The CMOS floating-gate inverters with multiple inputs have become a useful circuit block in modern analog and mixed-signal circuit design. A CMOS floating-gate inverter is a typical CMOS inverter with two or more input capacitances coupled to the floating gate (FG), which is common to both N and P channel enhancement MOSFET transistors which are connected in the drain mode. The potential induced in the FG can be controlled as a weighted linear sum, in voltage-mode, of all input signals. The potential of the FG establishes the on-off state of the CMOS inverter (Shibata *et al*., 1992-1993).

Discharging of the FG is commonly required but also, for many applications, it is desirable to pre-charge the FG to a given bias voltage. Discharging and pre-charging the FG can be achieved by using an analog switch that connects temporally the FG to an externally applied potential (V_{RES}). By using an external voltage V_{RES} = 0V, the FG can be discharged and the typical UV erasing technique can be avoided (figure 1). This concept has been introduced first in (Kotani *et al.*, 1995-1998) and was named as clocked-controlled NeuMOS inverter, but it will be referred as clocked-controlled FG-CMOS inverter.

The FG gain factor determines the maximum input contribution to the FG potential. For *n* capacitive inputs it is expressed as:

$$\frac{\sum_{i=1}^{n} C_i}{C_T} \qquad (1)$$

Where C_T is the total capacitance including parasitic capacitances. The physical characterization of the FG gain factor , also known as the capacitive coupling coefficient, and the parasitic capacitances coupled to the FG, is a fundamental step in the design of high performance FG-CMOS based circuits, since the device behavior strongly depends on these values. The strategy followed in this work consists in comparing some features of the transient behavior in the "reset" and "evaluation" periods. One advantage of this approach is that the extraction of the above mentioned parameters can be done to the FG inverter without the use of a "dummy cell" (Mondragón *et al*., 2000), resulting in an accurate mismatch-free technique, and whose evaluation will be demonstrated by comparing theoretical and measured results in the next sections.

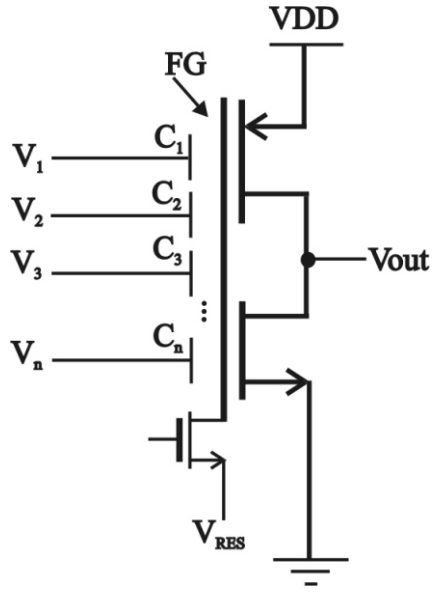


Figure 1. Electrical Diagram of a Clocked-Controlled FG-CMOS Inverter

Clock-controlled FG-CMOS inverter

Electrical charge and potential in the FG using an ideal analog switch

The electrical equivalent circuit for the FG inverter showing the control and relevant parasitic capacitances is shown in figure 2.

According to figure 1, the total charge stored in the FG, Q_{FG} is given by:

$$Q_{FG} \quad C_{FSN}(V_{RES} \quad V_{SN}) \quad C_{FBN}(V_{RES} \quad V_{BN}) \quad C_{FDN}$$
$$(V_{RRES} \quad V_{DN} \quad C_{FSP}(V_{RES} \quad V_{SP}) \quad C_{FBP}(V_{RES} \quad V_{BP})$$
$$C_{FDP}(V_{RES} \quad V_{DP}) \quad C_{OXN}(V_{RES} \quad {}_{SN} \quad V_{BN}) \quad C_{OXP}$$
$$(V_{RES} \quad {}_{SP} \quad V_{BP}) \quad C_{poly}(V_{RES} \quad V_x) \quad \sum_{i\ 1}^{n} C_i(V_{RES} \quad V_i) \tag{2}$$

where C_i, is the capacitance between the FG and the input node i, V_i is the ith input voltage, V_{DN}, V_{DP}, V_{SN}, V_{SP} and V_{BN}, V_{BP} are the drain, source and substrate voltages for the NMOS and PMOS transistors, respectively. From now on, the right side subscripts N and P will denote NMOS and PMOS, respectively. C_{FDN}, C_{FDP} and C_{FSN}, C_{FSP} are the overlap capacitances between the FG and the drain or source, respectively. C_{FBN} and C_{FBP} are the overlap capacitances between the FG and the bulk along the edge of the channel, C_{OXN} and C_{OXP} are the gate oxide capacitances, C_{DEPN} and C_{DEPP} in figure 2, are the depletion layer capacitances, which can be neglected after the channel begins to form under the floating gate (Shibata *et al*., 1993). Potentials $_{SN}$ and $_{SP}$ represent the surface potential of the silicon substrate. C_{poly} is the parasitic capacitance between the FG (polysilicon back-plate) and the below substrate layer tied to a V_x potential. In this case, for a P- substrate $V_x = GND$. Potential V_{RES} is the voltage transferred to the FG through the switch. All voltages in (2) are relative to substrate.

It is assumed that no charge injection and no charge leakage occur during device operation. Then, from the charge conservation law on the FG, (2) can be simplified and rearranged to obtain an expression for the potential on the FG, V_{FG}, when the initial net charge is zero, this is given by:

$$V_{FG}(\quad 1) \quad \frac{1}{C_T} \sum_{i\ 1}^{N} C_i V_i(\quad 1) \quad V_i(\ ) \quad C_{FPD}$$
$$[V_{DP}(\quad 1) \quad V_{DP}(\ )] \quad C_{FDN}[V_{DN}(\quad 1) \quad V_{DN}(\ )] \quad +$$
$$V_{RES}(\ ) \tag{3}$$

where the potentials at the reset period are represented by ( ), this is, when the reset switch is closed, and the potentials at the evaluation period represented by (+1), when the switch is open. In (3), $V_i(\ +1)$ represents the ith input voltage during the evaluation period, and $V_i(\ )$ is the ith input voltage applied during the reset period. The remaining potentials terms, coupled to the FG do not contribute with charge in both

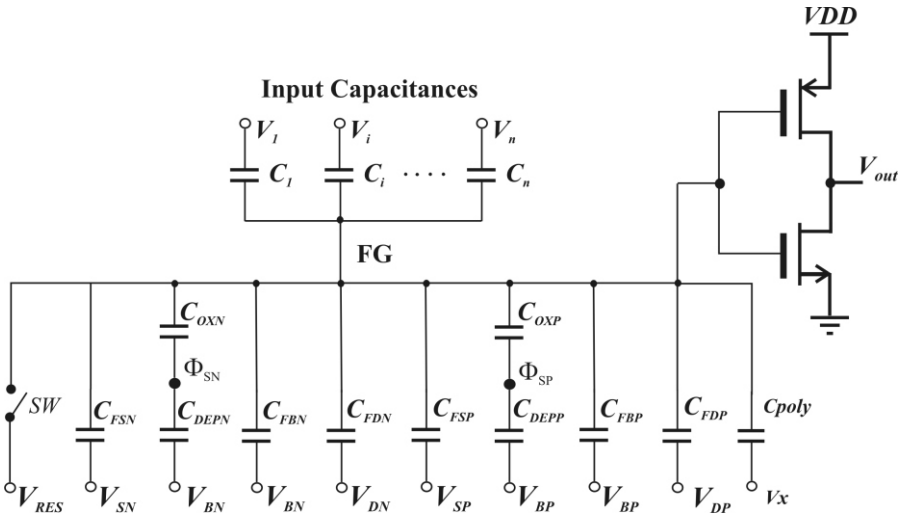


Figure 2. Electrical equivalent circuit for a FG-CMOS inverter with an ideal analog switch (SW)

periods, but their associated capacitances contribute to form C_T, which is defined as the sum of all capacitances coupled to the FG as follows.

$$C_T \sum_{i=1}^{n} C_i \quad C_{FSN} \quad C_{FBN} \quad C_{FDN} \quad C_{FSP} \quad C_{FBP} \quad C_{FDP}$$

$$C_{OXN} \quad C_{OXP} \qquad (4)$$

Potential in the FG using a real analog switch

For practical implementations, a single N-channel MOSFET can be used instead of the *SW* element as shown in figure 2. In figure 3, an equivalent circuit for the FG inverter using a real switch is introduced.

If the access switch transistor (SW) is ni cut off region, a simplest electrical equivalent circuit for the FG potential can be obtained (Ramírez *et al*., 2004), figure 4, where all the inputs are tied together and form a single input capacitor C_{IN}, $C_{IN} = C_1+\ldots+C_i+\ldots+C_n$. Capacitance C_{OUT} represents the sum of C_{FDP} and C_{FDN}. The C_{pi} capacitor is the *i*th parasitic capacitance that couples the FG to a DC voltage V_{DCi}.

Here, the ideal diode element models the N^+/P parasitic drain-bulk junction, associated to the access switch transistor (SW) in cut off and R_{leak} is an approximation to the non-linear leakage resistance of this junction.

The input V_{IN} voltage contribution to the FG potential can be obtained through the solution of a simplified circuit (figure 5a).

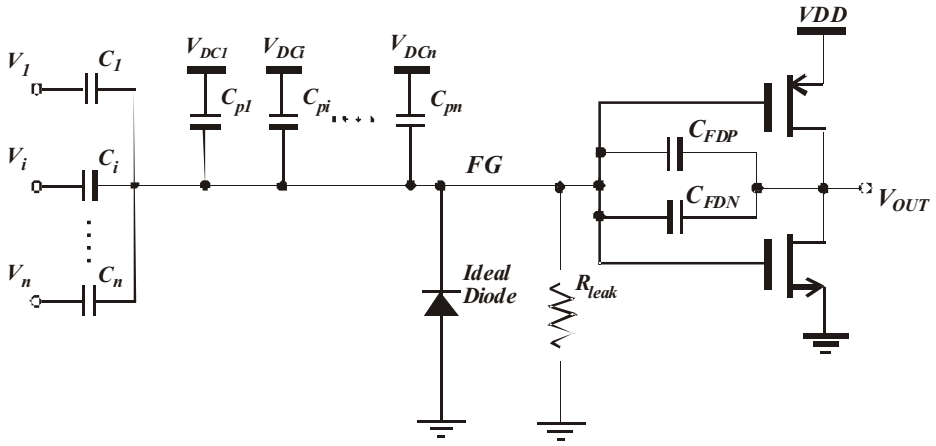


Figure 3. Equivalent circuit for a multiple-input FG-CMOS inverter using a N-channel MOSFET as a real analog switch

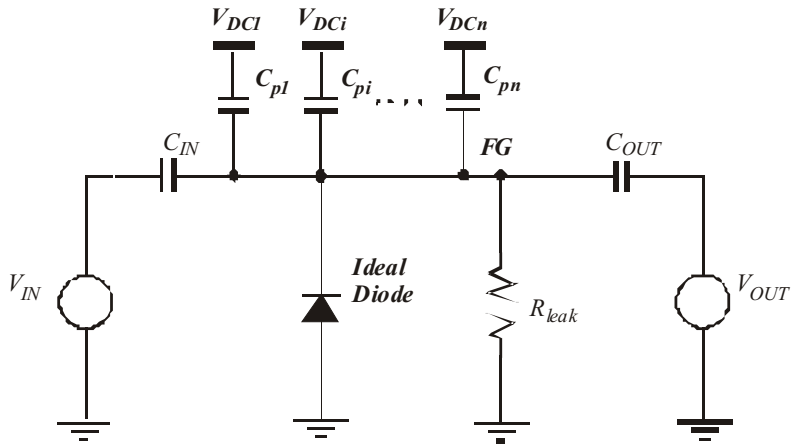


Figure 4. Equivalent circuit of a multiple-input FG-CMOS inverter using an N-channel MOSFET as a real analog switch, operating in the evaluation period

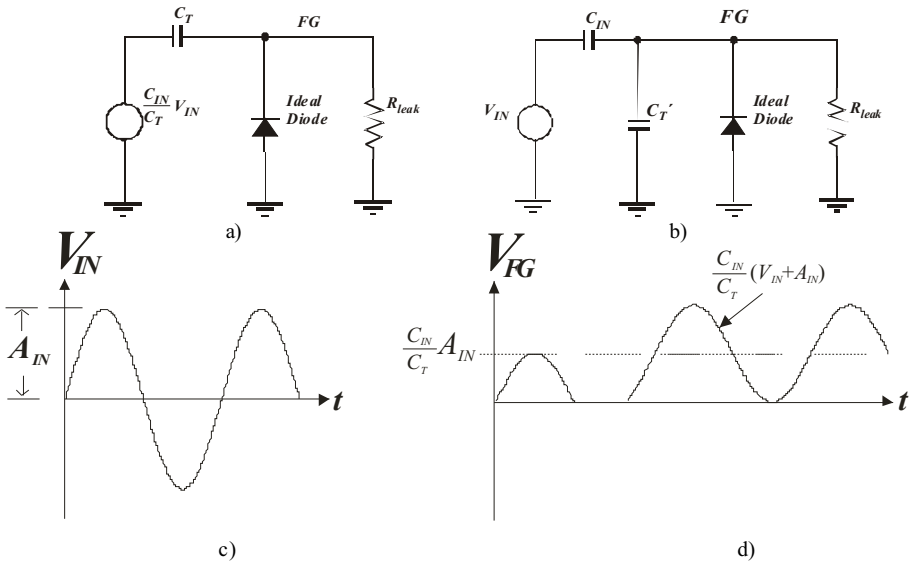


Figure 5. (a) Simplified circuit. (b) Thevenin reduction. (c) Periodical input. (d) V_{IN} contribution to the FG potential, V_{FG}

where the capacitance C_T' is defined as $C_T' = C_T - C_{IN}$. By conducting a Thevenin reduction to the circuit, the clamping circuit in figure 5b is obtained. For any periodical and continuous voltage signal applied to the circuit, $V_{IN} = A_{IN} f_1(t+nT)$ with amplitude A_{IN} and period T, such that $T << R_{leak}C_T$, figure 5c, the FG potential due only to this input-signal, figure 5d, will be given by:

$$V_{FG}|_{input} \quad \frac{C_{IN}}{C_T} V_{IN} \quad \frac{C_{IN}}{C_T} A_{IN}. \tag{5}$$

The same analysis holds for the corresponding contribution on the FG potential as a function of a periodical output signal $V_{OUT} = A_{OUT} f_2(t+nT)$, coupled to the FG through C_{OUT}, as follows:

$$V_{FG}|_{output} \quad \frac{C_{OUT}}{C_T} V_{OUT} \quad \frac{C_{OUT}}{C_T} A_{OUT}. \tag{6}$$

For the DC contribution, the following analytical time-domain expression for the FG potential is obtained:

$$V_{FG}(t)|_{DC,VRES} \quad \sum_{i=1}^{n} \frac{C_{pi} V_{DCi}}{C_T} \quad V_{RES} \; e^{(-t/R_{leak}C_T)}. \tag{7}$$

The global expression that models the FG potential will be obtained by summing equations (5), (6) and (7), this is:

$$V_{FG} \quad V_{FG}|_{VIN} \quad V_{FG}|_{VOUT} \quad V_{FG}|_{DC,VRES} \tag{8}$$

During the evaluation period, the terms associated to DC potentials coupled to the FG, vanish for $t >> R_{leak}C_T$. This means that the induced DC-charge on the FG at circuit startup and the reset-charge due to V_{RES}, will be swept out during the evaluation period, after several circuit-time constants $R_{leak}C_T$. Therefore, in steady-state, the FG potential will be:

$$V_{FG} \quad \frac{C_{IN}}{C_{TOT}} V_{IN} \quad \frac{C_{OUT}}{C_{TOT}} V_{OUT} \quad \frac{C_{IN}}{C_{TOT}} A_{IN} \quad \frac{C_{OUT}}{C_{TOT}} A_{OUT} \tag{9}$$

By deriving equation (9) with respect to time, the following expression is obtained

$$\frac{dV_{FG}}{dt} \quad \frac{dV_{IN}}{dt} \quad _{par} \frac{dV_{OUT}}{dt}, \tag{10}$$

where, $=C_{IN}/C_T$ is the FG gain factor and $_{par} = C_{OUT}/C_T$ would correspond to a parasitic FG gain factor due to the feedback of the FGMOS inverter's output voltage on the FG.

In reset mode, applying a direct signal to the FG, i.e. a sawtooth, the slope of the inverter transfer characteristic associated to the circuit shown in figure 6a, is given by:

$$A_{VR} \quad \frac{dV_{OUT}}{dt} \frac{dt}{dV_{FG}}. \tag{11}$$

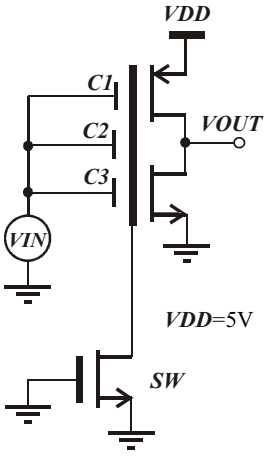
In a similar way, as illustrated in figure 7a, the slope of the transfer characteristic, when the circuit operates in the evaluation period, is given by

$$A_{VE} \quad \frac{dV_{OUT}}{dt} \frac{dt}{dV_{IN}} \tag{12}$$

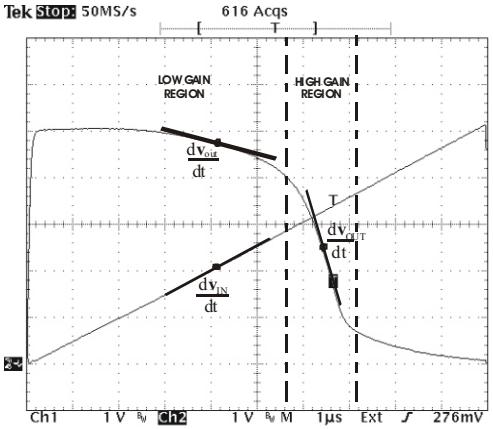
Now substituting (11) and (12) in (10), the following relation is obtained:

$$\frac{A_{VE}}{A_{VR}} \quad {}_{par} A_{VE} \tag{13}$$

Where, the slopes A_{VE} and A_{VR} can be easily measured in order to extract the parameters and $_{par}$.

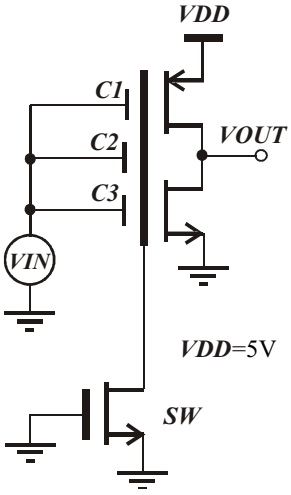


a)

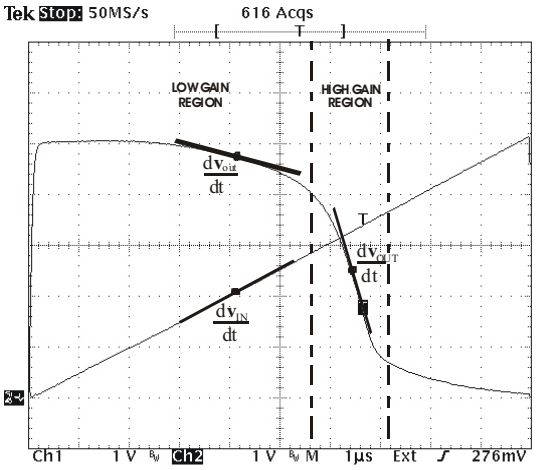


b)

Figure 6. Measurement in the reset period. (a) Applying a saw-tooth voltage signal (V_{IN}) directly to the FG terminal by using the access switch. (b) Graph of the inverter's output transient response



a)



b)

Figure 7. Measurement in the evaluation period (SW in cut off). (a) Applying a saw-tooth voltage signal (V_{IN}) to all input capacitors. (b) Graph of the inverter's output transient response

Extraction methodology

The basic idea that supports the extraction methodology consists in comparing the inverter transient response obtained in the reset period with that obtained during the evaluation period. The extraction methodology is presented next as a sequence of six steps:

Step 1. A measurement during the reset period of A_{VR} is taken around a fixed point in V_{IN} which corresponds to a low-gain slope of the output characteristic (V_{OUT}), (figure 6b).

Step 2. A measurement during the evaluation period of A_{VE} is taken around the same point of step 1, (figure 7b).

Step 3. Parameter is calculated using (13). The second term of the right side of this equation is negligible in the low-gain region due to $_{par}<$ and since A_{VE} is small, then, approaches to

$$\frac{A_{VE}|_{Step\,2}}{A_{VR}|_{Step1}} \tag{14}$$

Step 4. A measurement during the reset period of A_{VR} is taken at a fixed point V_{IN} near the switching-point of the inverter, which corresponds to a high-gain slope of the output characteristic, (figure 6 b).

Step 5. A measurement in the evaluation period of A_{VE} is taken at the same point of step 4, see figure 7b.

Step 6. From (13), $_{par}$ is calculated using the values obtained in the steps 3, 4 and 5, by using

$$_{par} \quad \frac{1}{A_{VR}|_{Step4}} \quad \frac{|_{Step\,3}}{A_{VE}|_{Step\,5}}. \tag{15}$$

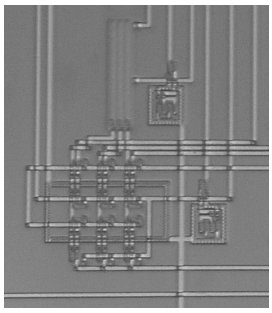
Experimental results

Two test cells were fabricated using a double-poly, double-metal CMOS process with 1.2 m design rules, available through MOSIS services (run: T2AH-BJ and T48S-AM). The microphotograph of each test cell is shown in figure 8. The first test cell corresponds to the circuit introduced in figure 6a. The schematic diagram for the second test cell is not shown, but is a six-input FG-CMOS inverter.

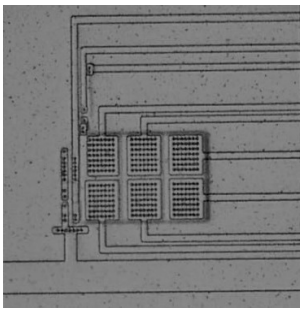
The test cells were measured using the described methodology presented in section 3. The small-signal slopes were computed by using a linear-fit approximation from data points obtained by means of a digital oscilloscope. Table 1, shows the theoretical and extracted values for and $_{par}$, using a 100 kHz saw-tooth signal

Table 1. Test cells electrical characteristics and theoretical and measured floating-gate gain factors

Test Cell	Num. Inputs	Input capacitance	Transistor Aspect Ratio	Measured		Theoretical	
					$_{par}$		$_{par}$
1	3	0.256 pF	P=27 m/1.2 m, N=9 m/1.2 m	0.837	6.71 10^{-3}	0.85	7.55 10^{-3}
2	6	0.35 pF	P=16.8 m/3 m N=6 m/3 m	0.923	-	0.926	-



Test-cell Num.1



Test-cell Num.2

Figure 8. Microphotograph of the fabricated cells

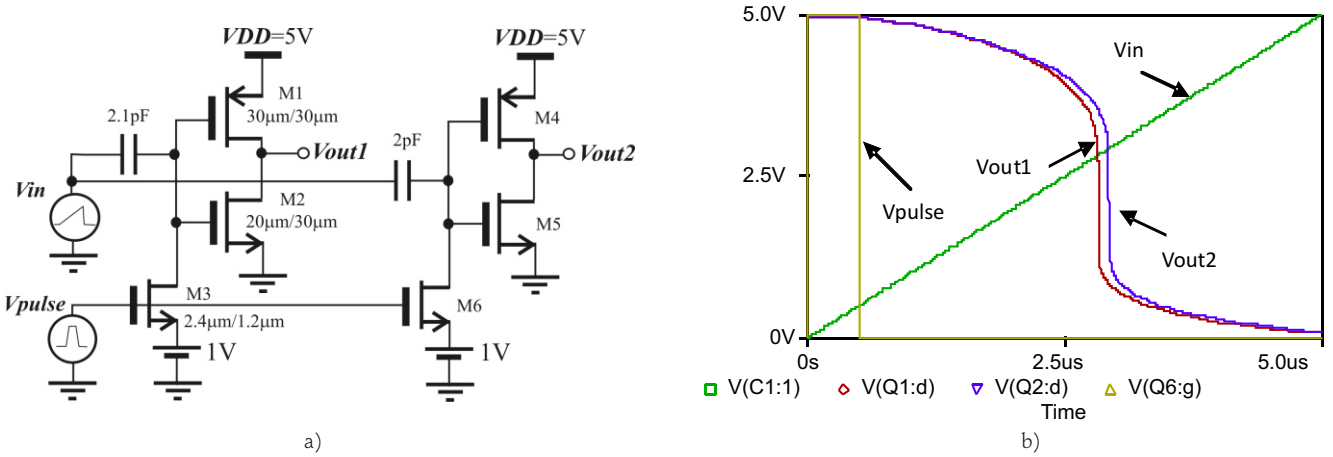


Figure 9. A simulation example, a) Two similar CMOS FG Inverters M1=M4, M2=M5 and M3=M6 with a slight difference at the input capacitance, b) The inverters simulation response using Transient Analysis on PSpice

with 5V peak-to-peak and a 2.5V offset. The period of this signal (T=10 s) is smaller than the intrinsic circuit-time constant which normally is in the order of seconds.

Discussion

Although the theoretical capacitance values can be calculated using the process parameters given by the foundry, the physical differences of the input capacitances can lead to an important deviation of factor and thus affecting significantly the circuit operating point.
As an example, two identical CMOS inverters were simulated through PSpice, one of them with an input capacitance deviation of 5% (figure 9a).

The inverters outputs are shown in figure 9b. The switching operating point (Jacob *et al*., 1998) of the inverters as shown, is shifted near by 60mV with respect the input voltage V*in* , this condition is undesirable for many analog and mixed signal applications since the recent low-voltage trends requires high accuracy. The methodology presented in this work focuses on CMOS floating-gate circuits with a clock-driven switch at the FG, and represents a good choice when the factor must be determined experimentally for high accuracy requirements.

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