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Scalable and CMOS-Compatible Catalyst Assisted Chemical Etch

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Scalable and CMOS-Compatible Catalyst Assisted Chemical Etch

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Dedicated to my parents, Rayudu & Satyavati.

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Abstract

Scalable and CMOS-Compatible Catalyst Assisted Chemical Etch

Akhila Mallavarapu, Ph.D.
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The ability to reliably and repeatably control the geometry of high aspect ratio silicon nanostructures over large areas is essential for a variety of applications in electronics, energy, point-of-use healthcare and sensing. For about five decades, Moore's Law consistently delivered computing devices with improved performance, lower power consumption and enhanced functionality, transitioning from 2D scaling to 3D device geometries. However, this transition to 3D has led to unique challenges in deep etching of nanoscale geometries by plasma etch, which limits creation of small and deep features. Metal Assisted Chemical Etching (MACE or MacEtch), an electroless catalyst-based wet etch discovered in 2000, has superior etch anisotropy and sidewall profile and can improve fabrication of high aspect ratio nanostructures. However, MACE literature has not demonstrated wafer-scale etch uniformity, lacks compatibility with CMOS fabrication due to the use of Au as a catalyst, and has limited exploration of complex geometries. Solving these challenges enables a MACE process that can be deployed broadly for a wide variety of CMOS and non-CMOS devices that require precise, high throughput, high yield nanofabrication.

This thesis has demonstrated scalable solutions to address MACE challenges, with a focus on adoption in high volume nanomanufacturing. To that end, first, wafer-scale reliable and repeatable fabrication of high aspect ratio silicon nanostructures is presented, based on integrating nanoimprint lithography, metal assisted chemical etching, and spectroscopic scatterometry. Next, a precise experimental technique to study the onset of Si-NW collapse is discussed. This approach resulted in unprecedented ultrahigh aspect ratio Si-NWs for oversized wires separated by sub-50nm gaps. A new nanostructure collapse avoidance methodology was developed using these results. Further, with respect to CMOS-compatibility of the MACE process, a replacement for gold was explored. For the first time, a Ruthenium MACE process that is comparable in quality to Au MACE is reported here. This result is significant because Ruthenium is not only CMOS-compatible but has also already been introduced in the semiconductor fab as an interconnect material. Finally, this research has explored complicated geometries that are specific to CMOS devices such as FinFETs and DRAM cells, and provided MACE-based process flow details to further demonstrate the potential of this technology for next-generation nanodevices.

The results in this thesis thus remove a significant barrier to adoption of MACE for scalable fabrication of ultrahigh aspect ratio semiconductor nanostructures, and provide new directions of research for creation of 3D semiconductor nanodevices.

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Chapter 1: Introduction and Overview

Novel nanomaterials and nanofabrication technologies can create unique capabilities to address unmet social needs. However, deploying such nanomaterials requires considerable resources and innovation to scale to viable products. This requires innovation at the interface of nanoscale materials, device designs and scalable fabrication techniques. The devices that benefit from such innovation can change the world - the transistor[1], for instance, is the building block of the electronics industry, and is arguably one of the most important technologies of the modern era. Other such transformational technologies include liquid crystal displays[2], magnetic storage[3], and more recently organic light emitting diodes[4] and human genome sequencing[5] devices.

The semiconductor industry ecosystem, which makes billions of transistors every day, has fast-tracked progress in a plethora of other fields such as biotech, augmented reality, AI, optics, MEMS and quantum computing. With increased miniaturization to make faster, denser, better devices comes a host of new engineering challenges in precision nanofabrication and process integration, resulting in a slower pace of progress, and higher cost of manufacturing. Moore's law[6–8], a scaling trend that described the rate of progress in making smaller and faster computing devices, was enabled by shrinking transistor sizes in 2D. As this 2D shrink has hit fundamental barriers over the last 5 years[7], innovative device architectures have further improved device performance by moving from 2D to 3D. The shift to 3D has brought into focus three key limitations of nanoscale pattern transfer using plasma etch – the industry standard – in current 3D nanofabrication:

(1) Poor nanoscale cross-section shape retention for tall or deep structures

(2) Erosion of hard masks during plasma etch.

(3) Poor structural stability of high aspect ratio 3D nanostructures.

Metal Assisted Chemical Etch (MACE or MacEtch), discovered in 2000, is a catalyst-based silicon etch that surpasses the resolution and aspect ratios of plasma etch and does not use hard masks. Further, MACE can control the porosity of etched structures, a property that can be used to create novel device flows. The remarkable taper-free, anisotropic and high selectivity etch results obtained using MACE have been demonstrated in research labs but have not transitioned to industry fabs. A critical reason is due to the use of gold as the MACE catalyst. Gold is not CMOS compatible and cannot be used in a semiconductor fab, severely limiting the ability to make devices at scale with MACE. This thesis aims to address the question, **"How can we develop an industry-compatible MACE process to create atomically precise high aspect ratio structures that enables next generation 3D electronic, optic, and biotech devices?"**

To scale MACE to a high throughput, high yield process, many challenges need to be solved, both in the MACE process as well as its integration into device fabrication. These process-related challenges include wafer-scale etch non-uniformity, nanoscale feature collapse, lack of CMOS-compatibility and process excursions such as catalyst wandering, porosity control, and stability of structures during the MACE process. Solving these challenges requires innovation in materials, process development and metrology.

This work addresses some of these challenges, and shows the promise of MACE as a next generation atomically precise fabrication technology. We build upon existing literature to create a definitive pathway towards industrial implementation and societal deployment of MACE to enable next generation nano-devices.

1.1. MOTIVATION

Silicon nanostructures, due to their quasi one-dimensional nature, possess several unique electronic, mechanical and optical characteristics. This, coupled with silicon's wide-spread use in the semiconductor industry makes it an ideal material for commercial applications. The ability to reliably and repeatably control the geometry of high aspect ratio silicon nanostructures over large areas is essential for a variety of devices, including tall silicon fins for high performance computing devices [9], deep etched silicon nanopillars or holes for memory devices [10,11] and inter-connects [12], sensors [13], batteries [14], capacitors [15,16], solar cells [17], nanoscale deterministic lateral displacement arrays for exosome and antibody separation [18] and zone plates [19,20] among others, as shown in **Figure 1.1**. Each application requires optimized designs of nanoscale geometry with tunable parameters ranging from placement and periodicity of nanostructures to variation of cross-sections and sizes. The nanopatterns are defined by lithography and transferred into the desired substrates by etch.

Etching has historically been characterized as wet and dry etch. Wet etching is a chemical etch process that selectively removes one material without affecting the other. It is isotropic in nature, and thus creates an undercut in the desired features. In etching of silicon to fabricate transistors, wet etching was used for the microscale devices, but due to its isotropic nature, has since been replaced by dry etching processes for creating nanoscale structures. Dry etching uses a plasma and has both chemical and physical component that can be used to tune the etch selectivity and anisotropy.

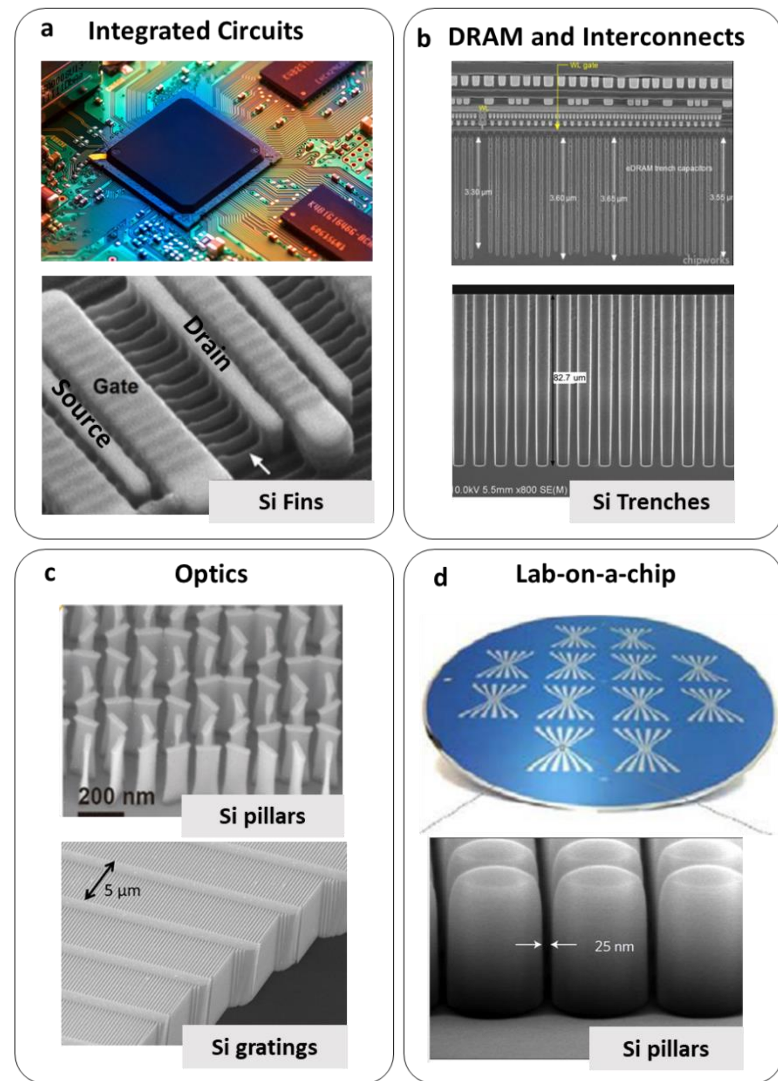

Figure 1.1: Exemplar applications that require precise nanopatterning and high aspect ratio Si etch. (a) Si fins for FinFETs [21], (b) Si trenches for DRAM and Through-Si-Via interconnects[22], (c) Si pillars for metalens[23] and gratings for X-ray optics[24], and (d) Nanopillar arrays for biological particle separation [18]

Plasma etching[25] processes are used in the semiconductor industry for anisotropic etching of highly controlled arbitrary nanopatterns in a variety of materials and substrates. However, they require expensive vacuum equipment and for 3D high aspect ratio structures, cannot retain cross-section shape easily. They suffer from etch challenges such as Aspect Ratio Dependent Etching (ARDE) and etch taper. For high aspect ratio silicon

etching in particular, various plasma etch defects can occur that affect fidelity of the nanostructures, depicted in **Figure 1.2**. Etch taper in logic and memory device structures is shown in **Figure 1.3**.

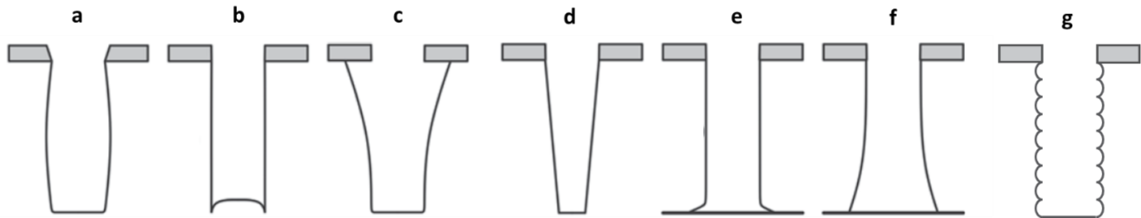

Figure 1.2: Loss of feature fidelity with high aspect ratio plasma etching. (a) bowing, (b) micro-trenching, (c) undercutting, (d) taper, (e) notching, (f) overcutting, (g) scalloping in Bosch etch, Adapted from Donnelly *et al.* and Wu *et al.*[25,26]

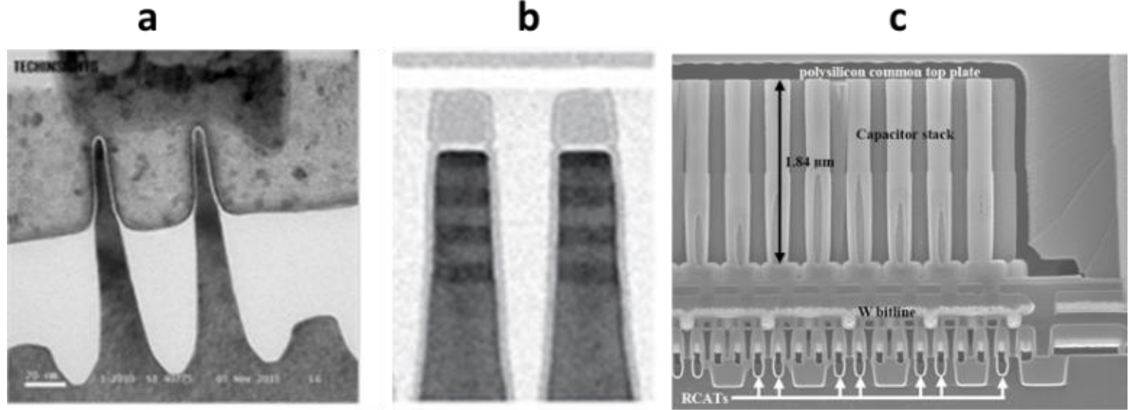

Figure 1.3: Etch taper in nanostructures made by plasma etch in industry. (a)finFETs in 16nm node TSMC chips (Source: TechInsights[27]), (b) nanosheet FETs in 5nm node IBM chips[28], (c) DRAM capacitors in 90nm node Samsung chips[29]

For semiconductor etching in particular, another method of pattern transfer into silicon was discovered in 2000, called Metal Assisted Chemical Etching (MACE or MacEtch)[30,31]. It is a metal catalyzed electroless chemical etch process that has been used to fabricate high aspect ratio features in silicon. The resulting structures can be optimized to have aspect ratios of >500:1 with no etch taper and no sidewall damage, and have been used to make zone plates and through-silicon-vias as shown in the **Figure 1.4**. Black

silicon, made by MACE without lithography, shows the capability of MACE to produce ultrahigh AR (>5000:1) nanostructures.

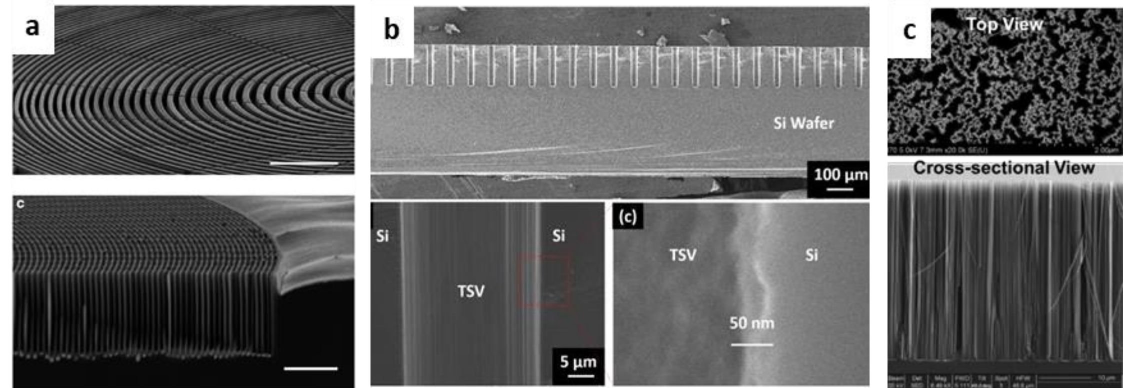

Figure 1.4: High aspect ratio nanostructures made with MACE for (a) zone plates[20] (AR>120:1), (b) TSVs[32] (AR> 5:1), (c) black silicon[33] (AR>5000:1)

As an example of applications enabled by MACE (that cannot be realized with plasma etch), sharp diamond-shaped cross-section silicon nanowires were demonstrated with MACE without loss of feature fidelity at high aspect ratios. Metal-Oxide-Semiconductor (MOS) capacitors made with these diamond shaped silicon nanowires show a 90% higher specific capacitance than NWs with circular cross section of same pitch, and highest specific capacitance per area of NWs in literature.[15]

A review of MACE literature and its mechanisms is explained in the next section.

1.2. BACKGROUND ON METAL ASSISTED CHEMICAL ETCH (MACE)

The development of electrochemistry of silicon and the formation of porous silicon laid the groundwork for the subsequent discovery of the catalytic effects of certain metals in the etching of silicon. Early electrochemical studies on silicon focused on anodic oxidation, electropolishing and chemical etching. Porous silicon films were reported during chemical etch with HF/HNO_3 without any applied bias, called “stain etching”, with pore formation due to localized dissolution of silicon.[34] Formation of porous silicon using stain etching requires a much simpler setup than electrochemical etching, but porous silicon made by stain etching does not exhibit photoluminescence unlike electrochemically etched porous silicon. In 1997, Dimova-Malinovska *et al.*[35] demonstrated the preparation of luminescent porous silicon by aluminum assisted chemical etching. However, the aluminum dissolves in the HF and HNO_3 based etchant solution. In 2000, porous silicon films with higher luminescence than Al-assisted ones were created using Pt, Au and Au/Pd films.[36] These metals did not dissolve in the etchant solution, and ultimately formed the basis for silicon nano-structuring using metal assisted chemical etching.

MACE is a catalyst based etching method that can be used to etch semiconducting materials locally in the presence of a catalyst. The chemicals used for MACE depend on the semiconducting substrate to be etched. **Figure 1.5** shows examples in literature for MACE of semiconductors such as Si, Ge, Si_xGe_{1-x}, GaN, InP, GaAs, InAs, etc., with MACE of silicon showing the desired high aspect ratio nanoscale features with no etch taper and no porosity.

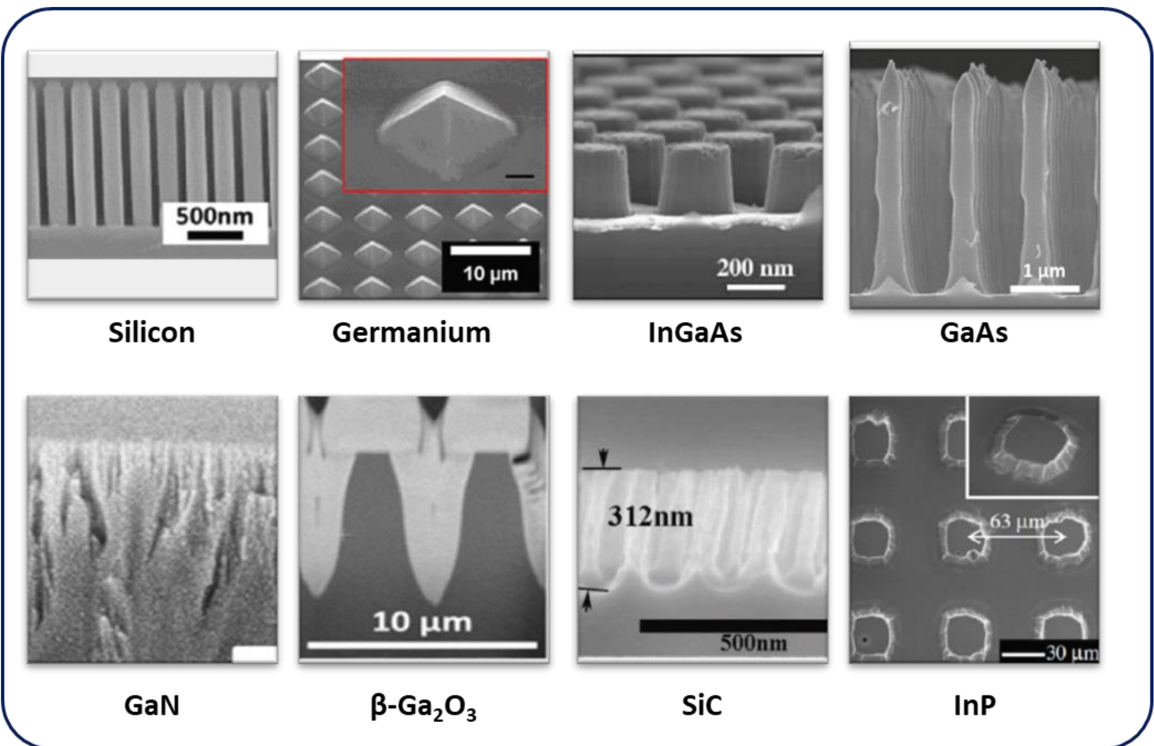

Figure 1.5: Semiconductor materials etched by MACE: silicon[37], germanium[38], indium gallium arsenide[39], gallium arsenide[40], gallium nitride[41], gallium oxide[42], silicon carbide[43], indium phosphide[44]

For MACE of silicon, a silicon wafer with a catalyst patterned on it is immersed in a solution containing an etchant such as HF and an oxidant such as H_2O_2. The mechanism for the MACE process has been investigated and reviewed in literature, and remains an area of active research.[31,45,46] The most widely accepted mechanism describes a local redox reaction at the location of the catalyst: it involves reduction of the oxidant in the presence of a catalyst, thereby creating positively charged holes h+. These holes are then injected through the catalyst metal to the metal-semiconductor interface thereby oxidizing the silicon underneath the metal. The oxidized silicon is dissolved by the fluoride component of the etchant that diffuses from the sides of and through the catalyst, and the soluble products diffuse away. For MACE of silicon with HF and H_2O_2, this redox reaction can

also produce hydrogen gas. The variable n=2 to 4 is determined by the ratio of oxidant to HF which determines the etch regime [31]:

$$Si + \frac{n}{2} H_2O_2 + 6HF \xrightarrow{Catalyst} H_2SiF_6 + nH_2O + \frac{4-n}{2} H_2 \uparrow$$

The catalyst material can be Ag, Au, Pd, Pt, Cu, TiN, graphene etc., with the materials having a strong effect on the morphology of the silicon nanostructures produced by MACE. **Figure 1.6** shows desired non-porous vertical nanostructures for MACE of Si with gold as a catalyst, with other catalyst materials showing porosity, sidewall roughness and/or etch taper.

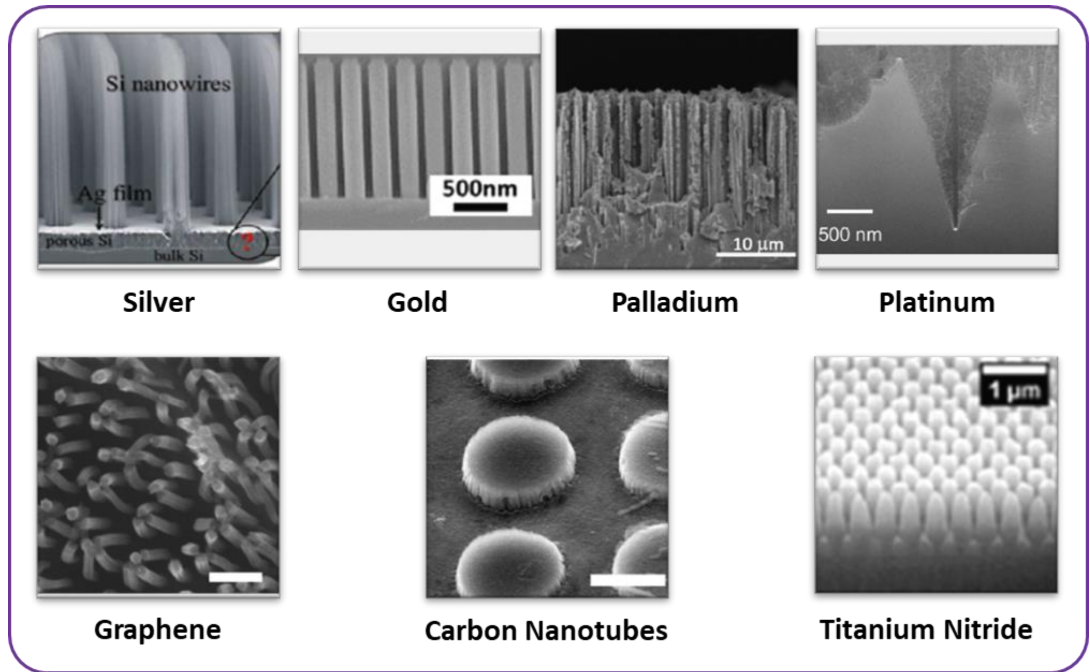

Figure 1.6: Catalyst materials used in literature for silicon nano- and micro-scale etch using MACE: Ag[47], Au[37], Pd[48], Pt[49], Graphene[50], CNT[51], TiN[52]

Various catalyst patterning methods have been used to create silicon nanostructures with nano- and micro-scale geometries. Initially, metal catalysts in the form of thin films, nanoparticles and metal salts in the MACE etchant were used to etch into silicon. Ordered

silicon nanostructures were subsequently created with MACE using catalyst patterning by lithography, shown in **Figure 1.7**.

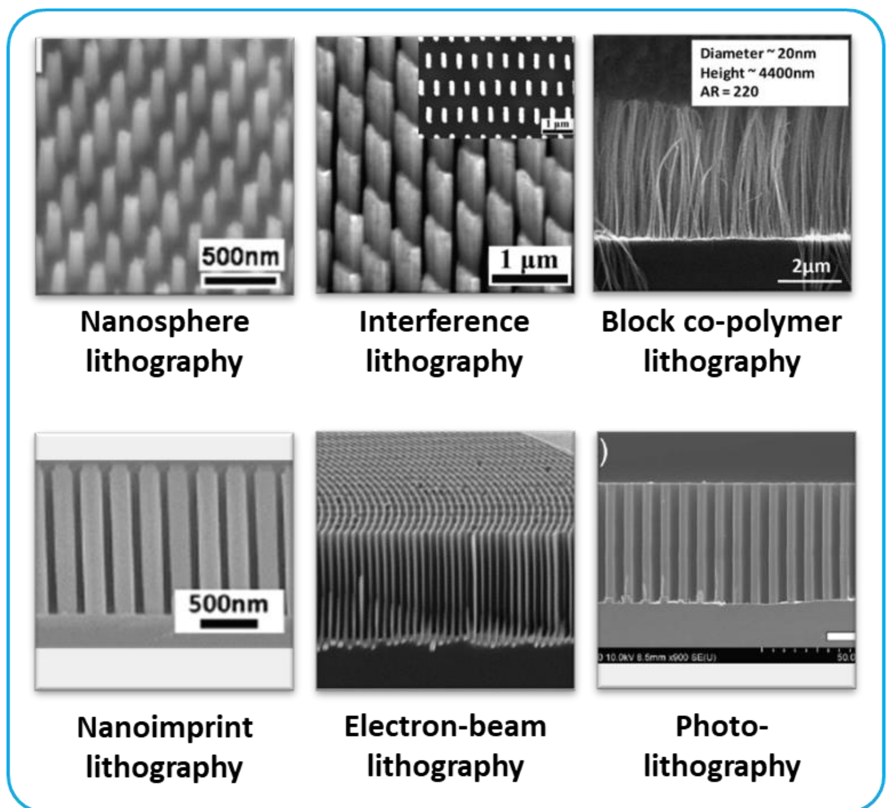

Figure 1.7: Lithography techniques used to pattern gold catalyst for MACE: nanosphere[53], interference[54], BCP[55], NIL[37], e-beam[20], photolithography[56]

Certain catalyst patterns are more prone to defectivity during MACE, with isolated nanoscale catalysts showing process excursions such as wandering from the desired anisotropic path during MACE. Such lateral motion has been reduced by catalyst pattern placement and geometry optimization, and through use of electric fields, magnetic fields and/or by using porous catalysts to anchor the catalysts during the etch. (**Figure 1.8**)

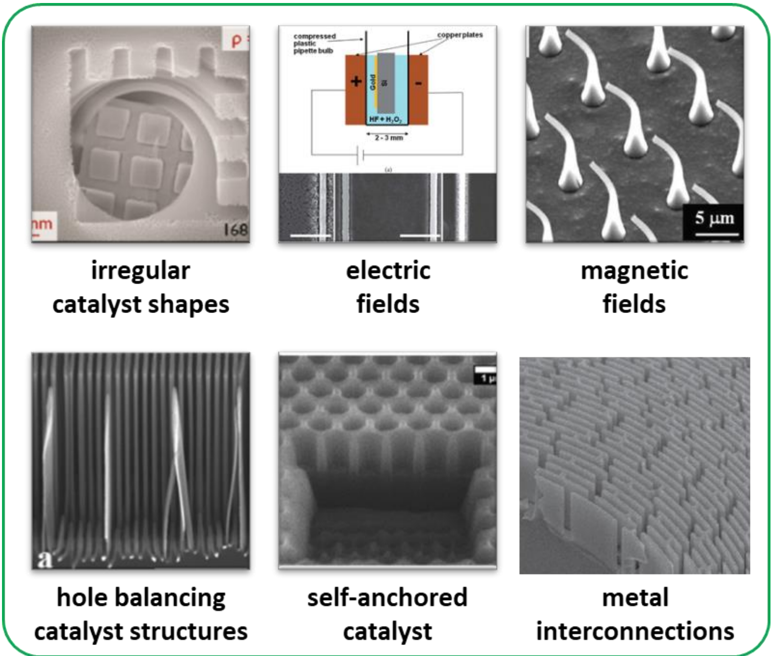

Figure 1.8: Catalyst motion control during MACE with gold as a catalyst, using: catalyst shape design[57], and control of isolated catalyst wandering using electric fields[58], magnetic fields[59], electronic hole (h+) balancing structures[60], self-anchored porous catalysts[61], metal interconnections[20]

Apart from creating high aspect ratio nanostructures in single-crystal silicon, MACE can also be used to tune the morphology of the nanostructures. The substrate doping and crystallinity also determine MACE results, with poly-crystalline and amorphous silicon etched by MACE showing increased sidewall roughness and taper. The morphologies of silicon nanostructures such as the orientation and/or porosity along the length of the nanowires can be controlled using varying etchant concentrations, electric fields, and/or dopant concentrations, shown in **Figure 1.9**.

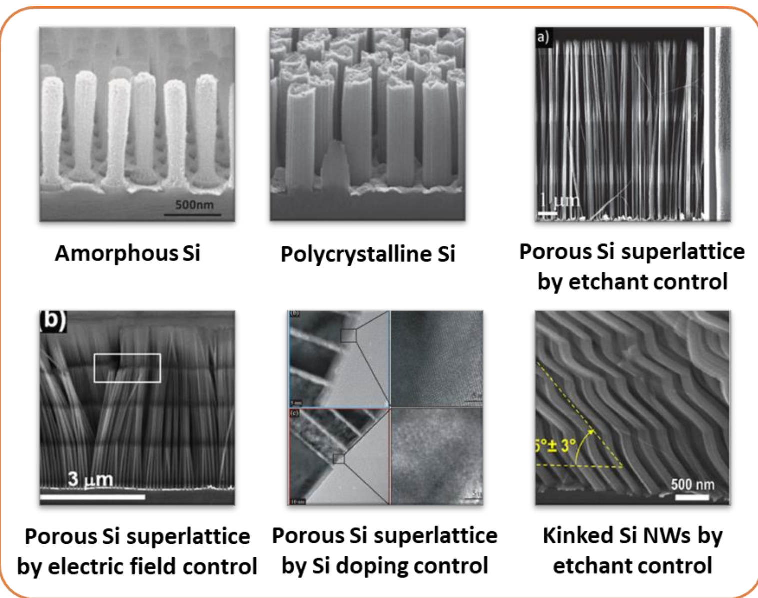

Figure 1.9: Silicon nanostructure morphology control during MACE: Amorphous and poly-crystalline microwires[62], silicon porosity control using etchant concentrations[63], electric field[64], and substrate doping concentration[65], kinked nanowire shape control using etchant concentrations[66]

Thus, MACE of silicon with gold as a catalyst can create precise silicon nanostructures with sizes ranging from sub-10nm to hundreds of microns with smooth sidewalls, no taper and ultra-high aspect ratios, surpassing limitations of plasma etch.

Further information on MACE can be found in several review articles[30,31,45,46,67,68] in literature.

1.3. THESIS LAYOUT

Despite its many advantages, MACE is perhaps not yet widely adopted due to process-related challenges, including:

(1) Large area etch uniformity and characterization

(2) Nanoscale feature collapse

(3) CMOS-compatibility

(4) MACE-based device designs and process integration

This work is divided into 6 chapters, and demonstrates scalable solutions that can enable adoption of MACE as an additional tool in the 3D nanofabrication toolbox. This Introduction chapter provided a motivation for this study as well as a brief overview and history of the MACE process.

Chapter 2 demonstrates wafer-scale high yield fabrication and characterization of vertical silicon nanowire arrays. The process is based on integrating nanoimprint lithography and metal assisted chemical etching (MACE) with gold as the catalyst. Nanowire array uniformity and defectivity is characterized using imaging spectroscopic scatterometry, which allows for extraction of geometric features of nanowires across the wafer, revealing a high degree of large-scale uniformity.

Chapter 3 describes experimental and theoretical insights into nanowire collapse behavior. Precise experimental prediction of onset of silicon nanowire collapse is performed by controlling NW diameter and analog etch depth variations in silicon nanowires fabricated with nanoimprint lithography and MACE. This approach has resulted in unexpectedly tall Si-NWs for oversized wires separated by sub-50nm gaps, as compared to known collapse theory. This discrepancy between known theory and experimental

results was eliminated when gold-resist caps (a feature of our MACE process) on top of these nanowires were removed. The known theory was then modified to include electrostatic repulsion to address this discrepancy.

Chapter 4 reports a Ruthenium MACE process that is porosity-free, taper-free, HAR and is comparable in quality to Au MACE. New parameters are introduced to reduce catalytic activity – including decreased Ru surface area and plasma modification – to achieve this result. This work provides powerful process variables to control undesirable porosity during MACE, and can be extended to non-Si semiconductors as well. Ruthenium is particularly desirable as it is not only CMOS-compatible but has also been introduced in the fab as an interconnect material. The results presented here remove a significant barrier to adoption of MACE for scalable fabrication of 3D semiconductor devices, sensors, and biodevices that can benefit from production in CMOS foundries.

Chapter 5 demonstrates the versatility of MACE for fabrication of arbitrary geometries and material stacks needed in logic devices. This chapter broadens the capabilities of MACE beyond circular nanowires to arbitrary nanopatterns and establishes a pathway for MACE-specific Design for Manufacturing. Further, the capabilities of MACE in creating nanostructure superlattices by controlling silicon porosity during etch is explored.

The final chapter, *Chapter 6* summarizes this work, describes other applications for MACE in sensors, optics and bio-tech devices, and outlines future process and materials development work needed to enable the transition of MACE from lab to fab.

Chapter 2: Wafer-scale Gold Assisted Chemical Etching of Silicon

A scalable fabrication technique for silicon nanowires based on integrating nanoimprint lithography, metal assisted chemical etching (MACE), and spectroscopic scatterometry is presented in this chapter†. The resulting wafer-scale process has demonstrated reliable and repeatable fabrication of high aspect ratio silicon nanostructures, and can provide cost-effective fabrication to enable applications in electronics, energy, point-of-use healthcare and sensing. Traditional pattern transfer using plasma etching suffers from etch taper and loss of feature fidelity at high aspect ratios, unlike MACE. However, MACE has largely been demonstrated in the literature over small areas, with scarce information on full wafer etching, critical dimension control, and etch depth uniformity.

In this chapter, a 100mm wafer high yield process to fabricate silicon nanowires is described. A large-area characterization of the process has been developed using imaging spectroscopic scatterometry. This scatterometry technique provides full wafer data on critical dimension control and etch depth uniformity. This work shows the promise of MACE as a next generation etch technology.

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† The work in this chapter overlaps with the following article[69] (in review) –
A. Mallavarapu, B. Gawlik, M. Grigas, M. Castaneda, O. Abed, M. Watts, S.V. Sreenivasan. "Water-Scale Fabrication and Hyperspectral Characterization of Silicon Nanowire Arrays made by Metal Assisted Chemical Etching." *in Review*, 2020.
Akhila Mallavarapu designed and performed the experiments, characterized and analyzed the data, and wrote the final paper.

2.1. MOTIVATION

The ability to reliably and repeatably control the geometry of high aspect ratio silicon nanostructures over large areas is essential for a variety of applications in electronics[9,10], optics[19,70], energy (batteries, solar cells, thermo-electrics)[14,17,71], sensors[13] and nanoparticle filtration[18]. Silicon nanostructures can be fabricated using both (1) bottom up approaches such as chemical vapor deposition (CVD), Vapor-Liquid-Solid (VLS) growth, or hydrothermal growth [72,73] and (2) top down approaches involving lithography and etch. Bottom-up approaches are typically used to fabricate periodic structures with circular cross-sections, such as silicon nanowires, and lack long-range order. They cannot be used to create arbitrary structures with varying dimension scales, and thus limit the nanostructure designs.

Top-down processes can precisely define and control the nanoscale feature geometric parameters (size, shape, aspect ratio, duty cycle, high fill-factors and placement) over large areas. Catalyst patterning with imprint lithography[74] is chosen for this work as it is able to create highly controlled arbitrary complexity patterns and nanoshapes with high fill-factors, and has a low cost structure, critical to cost-sensitive applications in silicon nanofabrication.

The patterns defined by lithography are then transferred into the desired substrates by etch. Plasma etching suffers from challenges such as plasma induced sidewall damage, Aspect Ratio Dependent Etching (ARDE) and sidewall etch taper. Another method of transferring patterns into semiconductors such as silicon, is by Metal Assisted Chemical Etching (MACE) [30,31]. MACE can maintain silicon nanostructure critical dimensions with high fidelity for ultrahigh aspect ratio features. Features with sizes ranging from sub-10nm to hundreds of microns with smooth sidewalls, no sidewall taper and very high aspect ratios

can be made with MACE [15]. **Table 2.1** describes typical methods of patterning and MACE reported in literature.

Table 2.1. Si etch by MACE processes reported in literature

<table>
<tr><th>MACE feature sizes</th><th>Lithography</th><th>Catalyst patterning</th><th>MACE area</th><th>Metrology</th><th>Large-area data on etch uniformity</th><th>Ref.</th></tr>
<tr><td>Microscale (> 5µm)</td><td>Photo-lithography (§)</td><td>Metal break (ψ)</td><td>Wafer-scale</td><td rowspan="7">SEM (small area)</td><td>Yes</td><td>32,75</td></tr>
<tr><td rowspan="7">Nanoscale (< 200nm)</td><td>NA</td><td>Nano-particles</td><td>Wafer-scale</td><td>No</td><td>33,76</td></tr>
<tr><td>Electron-beam (§)</td><td>Lift-off</td><td>Small area</td><td>NA</td><td>20</td></tr>
<tr><td>Laser interference</td><td>Lift-off</td><td>Small area</td><td>No</td><td>77</td></tr>
<tr><td>Block co-polymer</td><td>Lift-off</td><td>Small area</td><td>No</td><td>78</td></tr>
<tr><td>Colloidal</td><td>Lift-off</td><td>Wafer-scale</td><td>Yes</td><td>53,79–81</td></tr>
<tr><td>AAO</td><td>Metal break (ψ)</td><td>Small area</td><td>No</td><td>55</td></tr>
<tr><td>Nanoimprint (§)</td><td>Metal break (ψ)</td><td>Wafer-scale</td><td>SEM & Scatterometry (α)</td><td>Yes (wafer-scale)</td><td>This work</td></tr>
<tr><td colspan="7">(§) Can be readily extended to arbitrary geometries and nanostructure designs
(ψ) Does not suffer from yield issues, metal redeposition and high defectivity unlike lift-off
(α) Non-destructive high-throughput wafer-scale optical metrology for extraction of Si nanostructure geometries</td></tr>
</table>

Despite its many advantages, MACE is perhaps not yet widely adopted due to issues in fabrication of reliable, repeatable and high yield nanostructures over full wafers. Research in MACE has not demonstrated precise etch depth control and wafer scale uniformity for nanoscale arbitrary patterns. Large area wafer scale uniform etch with photolithography and MACE has been demonstrated in the micron-scale using Au as a catalyst [32,75]. However, wafer-scale MACE for nanoscale features has largely involved patterning-free formation of black silicon with metal nanoparticles [76,82,83]. Intentionally

designed and patterned complicated silicon nanostructures have only been demonstrated on small areas, with scarce information on large-area etch depth uniformity. Most characterization techniques rely on Scanning Electron Microscopy (SEM), which is an inherently small area metrology method.

Scalable silicon nanofabrication enabled by Nanoimprint lithography, MACE, and Scatterometric metrology (NIMS) is described in this chapter. The process is demonstrated through fabrication of Si nanopillar arrays on a 100mm wafer using nanoimprint lithography and MACE. Pattern uniformity and defectivity is characterized using imaging spectroscopic scatterometry with hyperspectral imaging as a large area metrology technique [84], in conjunction with local scanning electron microscope images.

2.2. METHODS

MACE uses a patterned catalyst that sinks into the silicon substrate as the etch progresses, leaving behind un-patterned areas as the etched structures. Gold (Au) is the most commonly used catalyst in MACE literature, and has the best process window for porosity-free silicon etch, compared to other catalysts reported in literature such as Ag, Pt, Pd [45]. Diffusion of gold into silicon causes deep-level defects in silicon which prevents its use in CMOS applications. But this occurs only at temperatures >200^0C [85]. MACE, as a low- to room-temperature process, along with complete removal of gold post-etch, can potentially avoid this. Additionally, for non-CMOS applications, gold can be used as a catalyst.

Figure 2.1 shows results of a typical MACE process on a relatively large area of 4 mm^2, with the gold catalyst patterned using nanoimprint lithography. The imprint template consisted of 1mm x 1mm nanowire arrays having circular pillars with a diameter of 120nm and pitch of 200nm distributed across the wafer.

The silicon nanowires are made on a 4-inch diameter p-type (100) Si wafer with a resistivity of 1-10 ohm-cm purchased from UniversityWafer, Inc. Circular resist pillars are imprinted on the silicon wafer using Jet and Flash Imprint Lithography (J-FIL)[74]. The residual resist layer of 10-15nm is removed (descumed) by an oxygen plasma on a Trion Oracle etcher, using the recipe – 15mT pressure, 65W power, 5sccm O_2, 70sccm Ar. Gold catalyst and Titanium adhesion layer are deposited on the patterned wafers using electron beam evaporation at a pressure of 5E-6 torr, with 10nm thick gold at a deposition rate of 0.4 A/s, and 2nm thick titanium at a deposition rate of 0.2A/s. The patterned wafer is immersed in a MACE solution comprising of 12.5M HF and 1M H_2O_2 for 30s. The etch is quenched in a beaker of water, and subsequently rinsed with water and dried with an air gun supplying clean dry air (CDA).

SEMs show the yield of the process, with nanowires having widely varying etch depths and collapsed pillars.

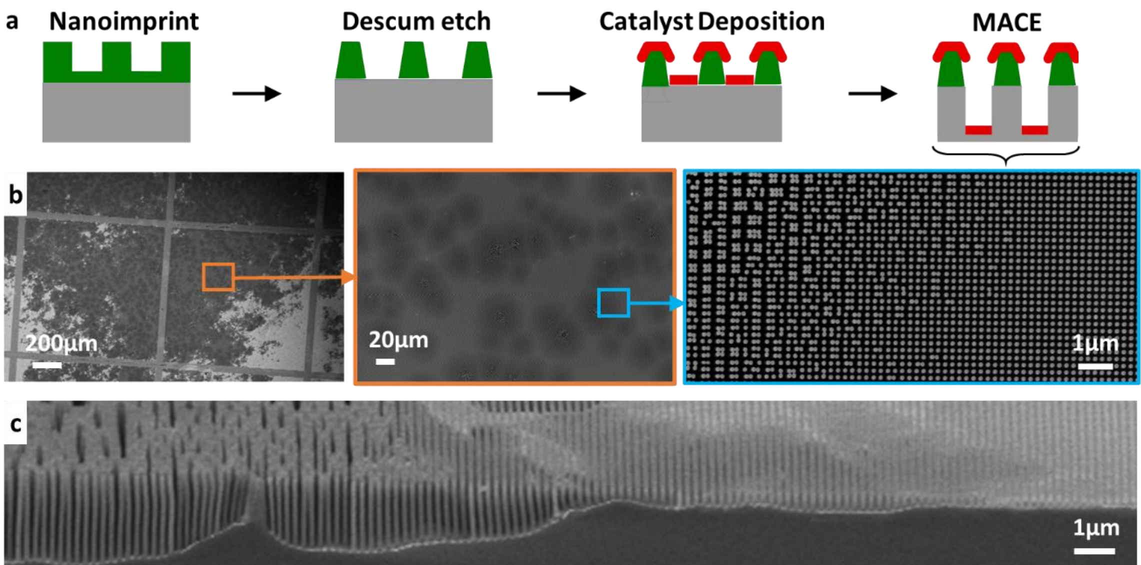


Figure 2.1: Preliminary MACE results show etch non-uniformity. (a) Process flow for making silicon nanowires using nanoimprint lithography and MACE, (b) Progressively zoomed in SEMs of top-down views of silicon nanowire arrays showing regions of collapse and etch failure, (c) Cross-section SEM showing a region of very-high non-uniformity of MACE. The samples are etched in a MACE solution of 12.5M HF and 1M H_2O_2 for 30s.

Reliable patterning of the gold catalyst is challenging, particularly for nanoscale geometries – low volatility of Au etch products prevents reliable plasma etch, and Au wet etch has >1 micron resolution due to its isotropic nature [86,87]. Lift-off, the most common process used for Au patterning, uses an undercut resist profile to create a metal break in the gold film deposited directionally using electron-beam lithography. This process is not ideal for manufacturing, as redeposition during lift-off causes yield issues [88]. Creating a metal break with imprint lithography faces further challenges, as methods to create an undercut profile in other patterning methods cannot easily be translated to nanoimprint lithography. Imprint, while having incredible resolution at low cost, needs a residual layer

break through etch which complicates the metal break process, as described in the next sections.

2.2.1. MACE without a metal break layer – non-uniform etch

MACE uses a patterned catalyst that sinks into the silicon substrate as the etch progresses, leaving behind un-patterned areas as the etched structures. The catalyst patterning process typically includes a lift-off step, which has low yield for large areas due to redeposition of lifted-off material. Lift-off can be eliminated in the MACE process flow, as only the metal directly in contact with silicon acts as a catalyst. Thus, ensuring a metal-break when depositing gold after lithography is sufficient for MACE. This can be done by creating an undercut in a typical lift-off layer, which we call a metal-break layer.

SEMs in Figure 2.1 show nanowires made with MACE having widely varying etch depths and collapsed pillars. The primary reasons for non-uniform MACE results are:

(1) Challenges of patterning gold (especially with nanoimprint lithography): Creating a metal break with imprint lithography is challenging due to the low height of imprint resist (60-70nm), and the loss of resist shape (rounding off tops of the resist pillars due to physical component of plasma etch) during the removal of resist residual resist layer with an Ar/O_2 plasma descum step prior to gold deposition.

(2) Variations in imprint resist residual layer thickness (RLT): Variations in resist RLT can result from uncalibrated inkjet dispense of resist, particle contamination on wafers, pattern density variations, and poor surface roughness of starting substrates. Such variations exacerbate the issues with Au patterning, as shown in **Figure 2.2**. An RLT variation of 15nm ± 5nm was achieved by developing a cleanroom protocol for avoiding particle contamination, and using double side polished 4-inch Si wafers and inkjet calibration.

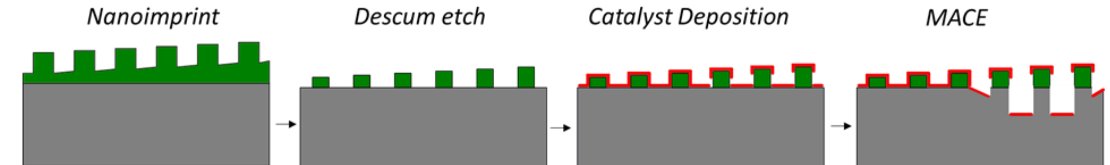


Figure 2.2: Effects of varying residual layer thickness on gold patterning and non-uniform MACE. Causes of such residual layer thickness include imprint defects such as particle contamination, change in pattern density and solid-phase and liquid-phase defects during UV curing of resist.[89,90]

Such large variability in etch cause high yield losses and prevents use of optical metrology techniques such as spectroscopic scatterometry. Improving the etch uniformity area to greater than the resolution of the optical metrology technique – ~ 5-100 microns – can enable high-throughput geometric and defect characterization. Forming a reliable metal-break across the wafer improves etch uniformity. The thickness of the gold film plays a critical role in the creation of metal break, as shown in **Figure 2.3**.

Reducing the gold thickness, and/or eliminating a 2nm adhesion layer, results in a discontinuous film of gold, with individual gold grains acting as isolated catalysts that result in random “nano-whiskers” that are created along with the desired lithographed pattern. Increasing the gold thickness to remove grain boundaries makes the film conformal over the imprint resist, causing no metal break, and consequently no MACE. This process is also heavily dependent on the imprint resist sidewall profile, resulting in small areas with good MACE, but does not scale to large areas reliably.

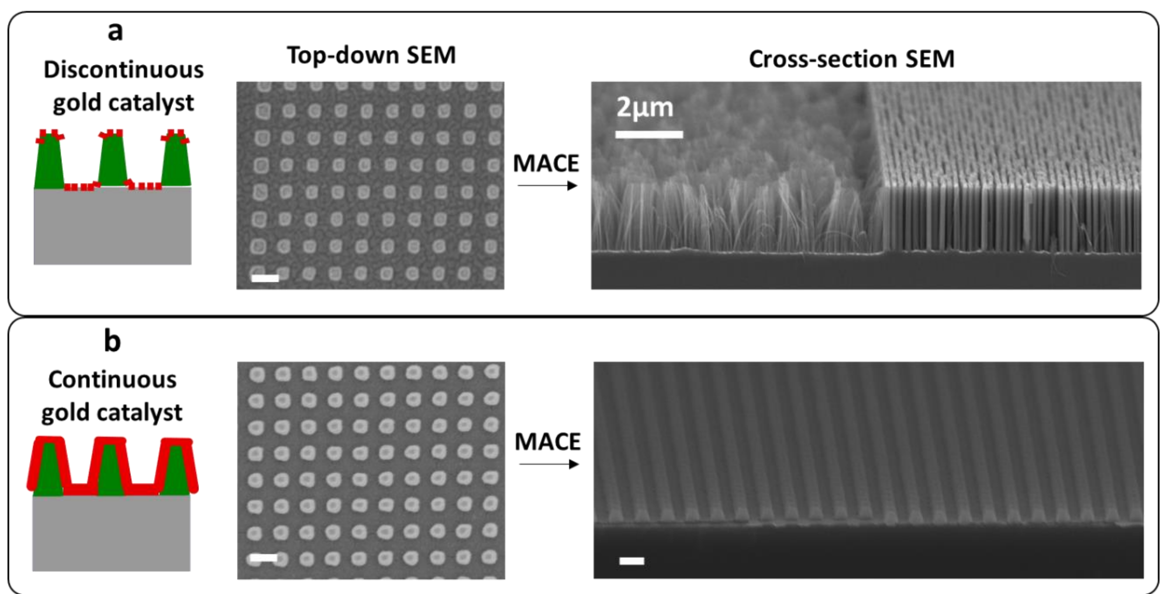


Figure 2.3: Effect of gold morphology on MACE: (a) Discontinuous gold catalyst (5nm thick) showing grain boundaries in the top-down SEM after deposition, and etched silicon nano-whiskers alongside patterned nanowires after MACE. (b) Continuous gold catalyst (20nm thick) showing no etch due to lack of access of etchant for MACE. Scale bars are 200nm.

2.2.3. MACE with a metal break layer – uniform etch

Figure 2.4 shows processes developed in literature for metal patterning with lift-off. Lift-off demonstrated in literature is performed for nanoscale features using a photosensitive lift-off layer that over-develops during photolithography or e-beam lithography, thereby creating an undercut to aid in a metal break prior to liftoff. This is not possible in imprint lithography due to the entire resist being exposed to a blanket UV light for curing of resist. A residual layer thickness is formed in the resist pattern after imprint, which is removed using a short oxygen plasma etch. The short descum etch tends to round-off the resist pillars. An undercut layer needs to be etched using a highly precise and selective plasma etch, and further rounds off the resist pillars.

For MACE, the lift-off step itself can be eliminated, as only the portion of the catalyst in contact with silicon is etched, and the portion separated by the resist is not etched. This allows the process to be free of lift-off related yield losses such as redeposition and incomplete removal of metal, particularly for nanoscale features. A metal break layer can enable uniform etching by creating an undercut using a selective wet etch, using a layer that improves wetting (oxide). Figure 2.4(d) shows the effect of excess undercut.

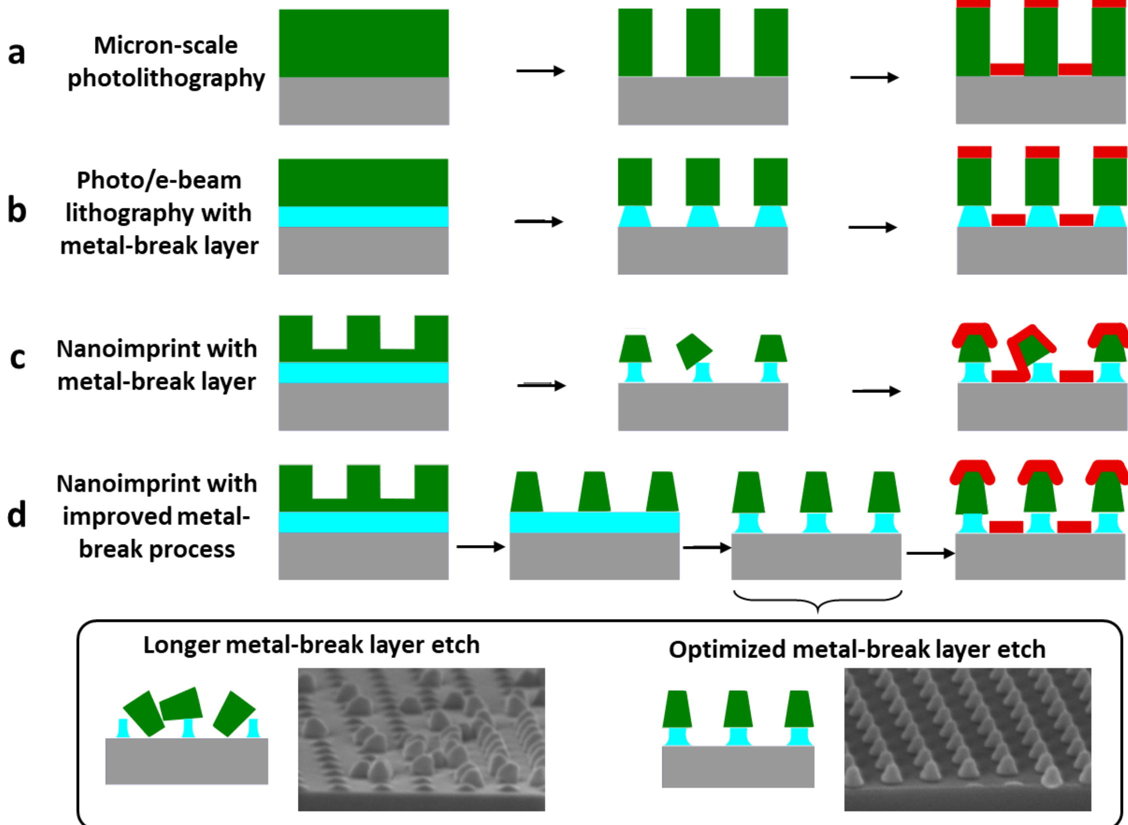


Figure 2.4: Methods of creating a metal-break in gold using (a) photolithography, (b) with a metal-break layer, (c) Nanoimprint lithography with a metal-break layer, and (d) improved undercut process

2.3. Results and Discussion

2.3.1. Wafer-scale Implementation of MACE

An optimized MACE process for wafer-scale fabrication of silicon nanowires is shown in **Figure 2.5**. We add a silicon oxide metal-break layer between the resist and silicon, and create an undercut using a short, diluted silicon oxide etch that is highly selective and does not affect the resist cap. 30nm thick thermal oxide is grown on the wafer followed by imprint lithography and resist descum etch. A short BOE (Buffered Oxide Etch- 6:1) dip is used to isotropically etch the oxide layer and create an undercut prior to catalyst deposition and MACE. This BOE dip prevents further loss of resist features caused by plasma etch of a typical polymer undercut layer. Further, the oxide layer is hydrophilic and etched by HF in the MACE solution, thereby enabling a uniform "starting point" throughout the wafer. This allows the etch to start at the same time in all portions of the wafer and ensures etch depth uniformity. After MACE, gold catalyst is removed using a wet etchant.

The etch uniformity and nanowire geometries are then characterized using imaging spectroscopic scatterometry[89] to extract feature geometries over a 100mm wafer with micron-scale spatial resolution. The extracted features are validated using cross-section SEM images at multiple locations on the wafer. The results of the Nanoimprint lithography, MACE, and Scatterometric metrology (NIMS) process are described below.

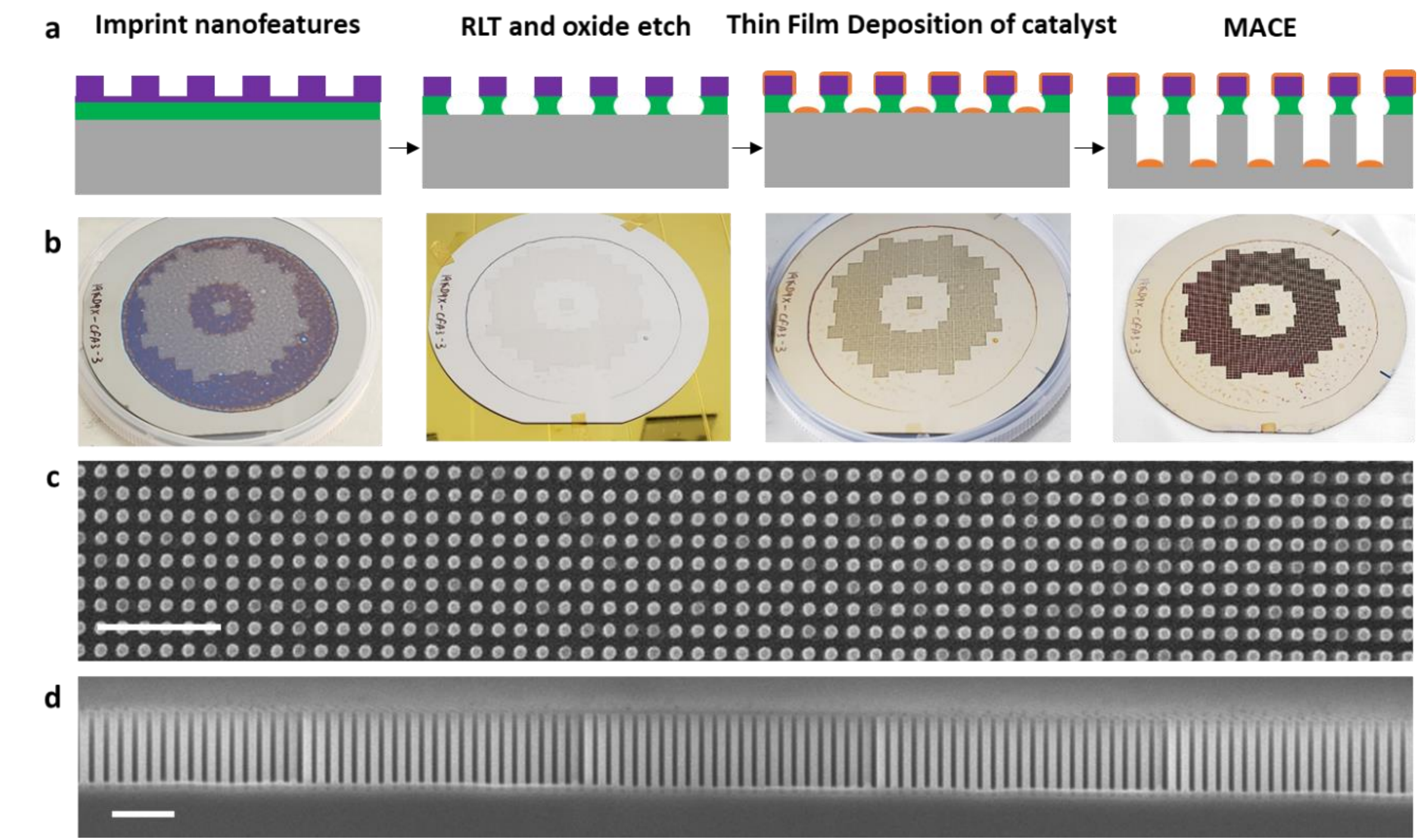


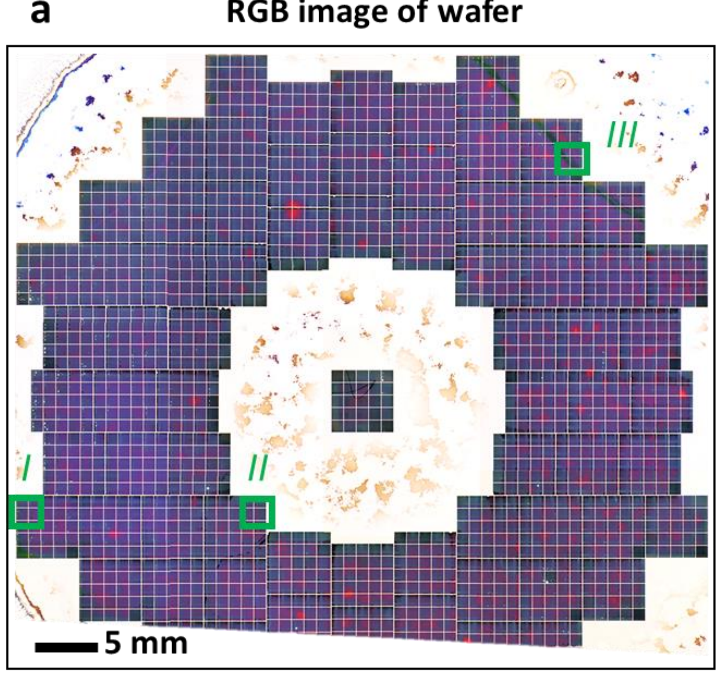
Figure 2.5: Full wafer MACE process showing (a) optimized MACE process, (b) images of a 4-inch wafer after each process step, (c) Top-down and (d) cross-section SEM images of Si NWs made with MACE. The samples are etched in a MACE solution of 12.5M HF and 1M H_2O_2 for 30s. The scale bars are 1μm in length.

2.3.2. NIMS Metrology results – Spectroscopic Scatterometry

Metrology techniques to characterize nanowire geometry – such as diameter and height – using traditional methods such as scanning electron microscopy (SEM), atomic force microscopy (AFM), transmission electron microscopy (TEM), etc. have very low throughput, limited field of view, and are often destructive. Scatterometry [91–93] is an optical metrology technique that, combined with imaging methods, enables a high throughput, non-destructive wafer-scale characterization. Scatterometry measures angle (angular) [94] or wavelength (spectroscopic) [84] resolved reflectance from nanostructure arrays to enable non-destructive geometric characterization when coupled with inverse modeling of the optical behavior of nanostructures. Angular scatterometry is preferred when accurate material optical parameters across a range of wavelengths is not available, or for structures with multilayer films where optical parameters are difficult to estimate. However, angular scatterometry requires more complicated hardware and methods to solve focusing issues related to oblique imaging. The spectroscopic approach is simpler to implement and is as robust as the angle-resolved approach for nanostructures with accurate material data across a range of wavelengths, such as single crystal silicon nanowires used in this work. Thus, silicon nanowires made with MACE are amenable to spectroscopic scatterometry as the MACE process, with gold as a catalyst, creates non-porous single crystal silicon nanowires.

The experimental reflectance spectra are obtained using a wafer scale spectral imaging system (described in Gawlik *et al.* [84]), which is used to measure the specular reflectance spectra at each pixel in the image at wavelengths of 400nm to 550nm, taken at an interval of 10nm, thereby generating an experimental dataset for quantitative analysis. The throughput of spectral imaging for the current range of wavelengths is about 7min per individual field of view (FOV). A full wafer requires 12 measurements of 19mm x 23mm

FOV for reliable image stitching. **Figure 2.6**(a) shows an RGB image of the wafer, which is obtained via image stitching and transformation of the spectral reflectance image, along with cross-section SEMs at three locations on the wafer in Figure 2.6(b). The SEM-based height variation across the wafer is captured by inspecting three different cross-sections across three 1mm x 1mm array of pillars (marked *I, II and III* in Figures 2.6(a) and 2.6(b)). At each of these three locations, 21 SEMs are captured going across 1mm cross-sections at intervals of 50 microns as plotted in *Figure 2.6(b)*. The diameter and height are extracted from the SEMs using ImageJ. This shows a variation of 22% in height in areas I and II, and a variation of 9% in area III. The variation in color in the RGB image qualitatively shows the nanowire height variations. Locations I, II and III were chosen to be at the transition of nanowires from high-density to no patterns as it is well known in MACE that these transition areas show the highest etch non-uniformities.



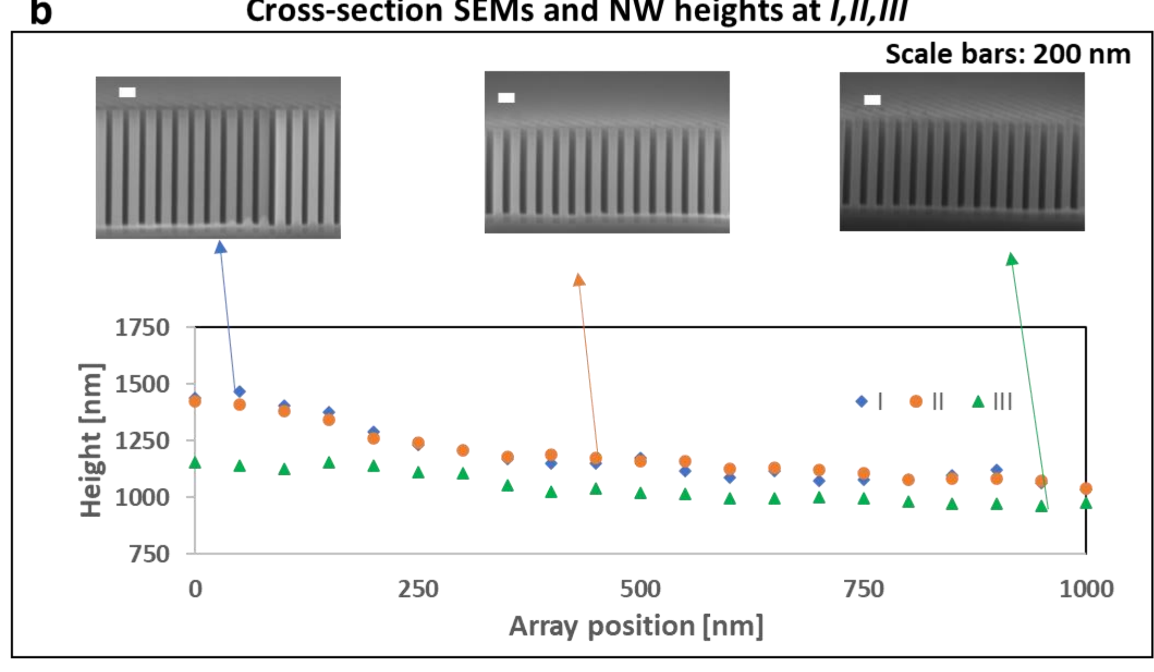


Figure 2.6: Full wafer MACE metrology: (a) RGB image of wafer after MACE and gold removal showing color variation, indicative of variations in Si NW geometry, (b) cross-section SEMs and a plot of NW heights at 3 representative 1mm x 1mm arrays (Locations I, II, III) on the wafer.

2.3.3. NIMS Metrology results – Geometric parameter extraction

The optical behavior of the silicon nanowires is modelled using Lumerical FDTD with diameter and height as the geometric parameters.[89] Sidewall angle is not used in this model as MACE creates nanostructures with no measurable etch taper, which is a significant advantage over plasma etching, particularly for high aspect ratio nanostructures. A library of 3400 simulated spectra was generated for nanowire diameters ranging from 80nm to 160nm in steps of 5nm, and heights ranging from 10nm to 2000nm in steps of 10nm. For each pixel, the experimental reflectance spectrum is compared to every simulated spectrum in the library to find the best match using root-mean-square-error (RMSE) minimization. A mapping of the height and diameter produced by this inverse modelling, with a maximum acceptable RMSE value of 0.25, is shown in **Figure 2.7**(a), which also shows higher NW heights and variability at the pattern transitions. Computing the matching process takes 3 hours.

The results are validated by taking SEM measurements as shown in Figure 2.7(b), and comparing it to the heights determined by imaging scatterometry at specific locations on the wafer. The simulation follows the decreasing trend of heights in the array quite closely, and shows a good match for a good portion of the sample (such as spot A in Figure 2.7(b)). The simulation predicts a lower value than experiments (spot B in Figure 2.7(b)), with poor matching of some of the spectra peaks in spot B. The data in Figure 2.7(b) is representative of other data collected during this research – a good portion of the data has the SEM results matching the scatterometric measurement, with some spots where there is a poor matching.

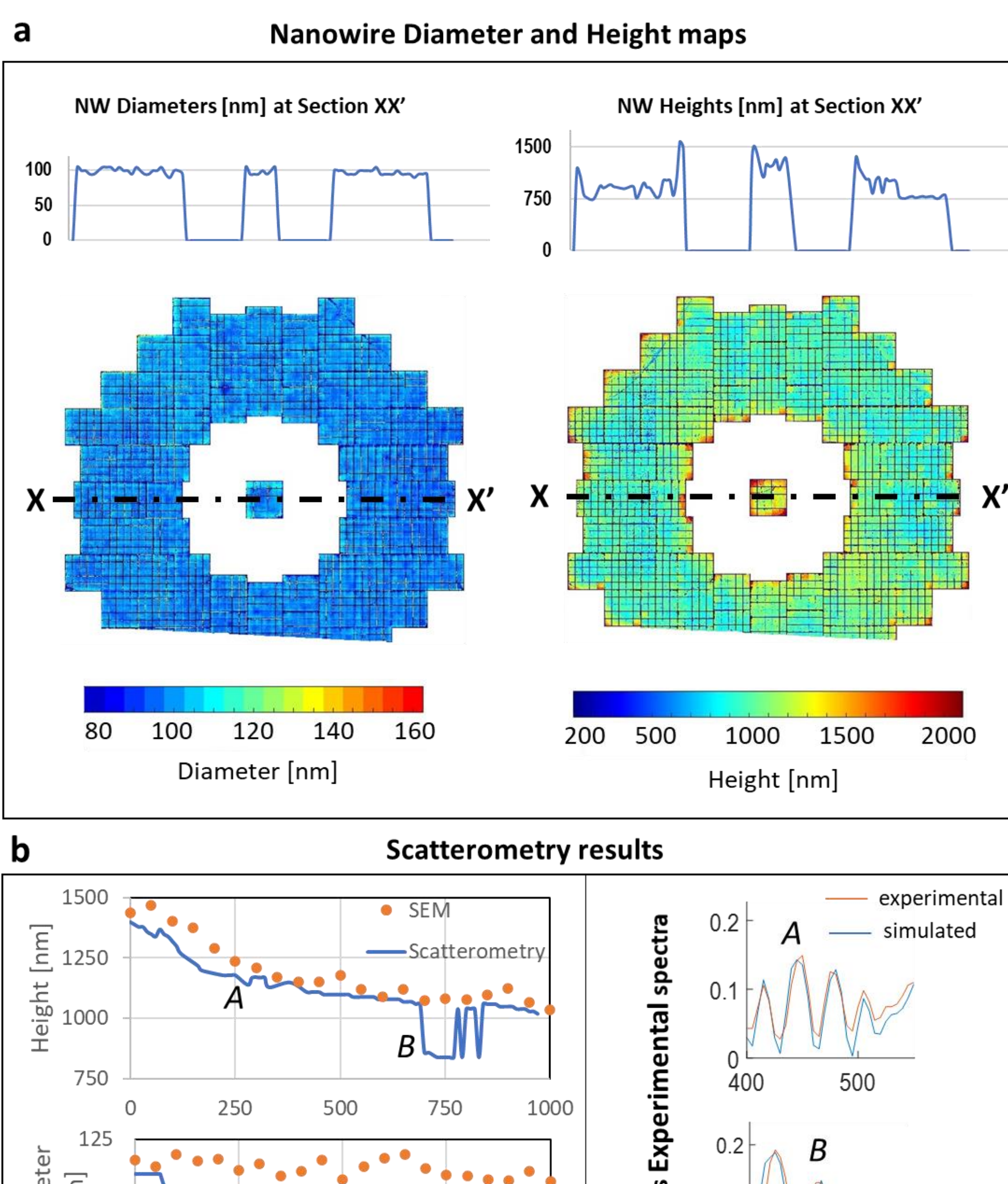


Figure 2.7: Full wafer MACE Scatterometry: (a) Diameter and height maps of NW arrays showing variations in height determined using spectroscopic scatterometry, (b) Results of the nanowire height and diameter at Location II predicted by matching simulated and reflectance spectra, compared to SEM measurements

This poor matching (dip at spot B) could be due to one of many things including (i) insufficient granularity of diameters/heights/wavelengths in the model; (ii) the result of the cross-section SEM measurements being incorrectly offset with respect to the optical pixel; (iii) variability or noise in the illumination system during this spectral scatterometry measurement. Further, in Figure 2.6(b),the predicted diameter and height of the nanowires are both consistently lower than experimental measurements, which may be expected due to the presence of native oxide that has not been incorporated into these models [84]. Again, the low granularity of the simulated geometries could contribute further error.

To address some of the problems discussed in the previous paragraph, we could increase the granularity of height/diameter, but this causes challenges with much higher computational complexity in the inverse search problem [89]. The inverse search problem can be sped up by using efficient data curation and search algorithms and using better computational resources [95]. Increasing granularity in wavelength requires faster data capture in real-time and this requires automation of the experimental setup using a precision X-Y stage, and increasing the speed of wavelength switching to the speed of measurement with future work targeting <30 seconds for the whole wafer. Also, avoiding illumination variability measurement errors can be addressed by adding intensity measurement sensors on the wafer chuck of the metrology systems.

Future research includes improving the etch depth uniformity of MACE further by controlling the etchant concentration and controlling the local silicon wafer temperature, which affects the local etch rates[96]. As an example, local temperature control by wafer chucks with spatially controllable temperatures[97] can allow us to improve etch depth uniformity in future MACE systems. The match between simulated and experimental spectra can be improved with increased granularity of diameter, height and wavelength, inclusion of effects of native oxide in the forward optical model, and avoiding illumination

variability errors. Further, low-sampling angular scatterometry can be combined with high-speed spectroscopic scatterometry to potentially improve the scatterometry measurements for NIMS.

In summary, scalable silicon nanofabrication enabled by Nano-Imprint lithography, MACE, and Scatterometric metrology (NIMS) is described in this chapter. Improvements in the MACE fabrication process to achieve reliable and repeatable wafer-scale fabrication is demonstrated via the production of a 100 mm wafer containing vertical silicon nanowire arrays. These nanowires are subsequently characterized using imaging spectroscopic scatterometry, which allows for extraction of geometric features of the nanowires across the wafer revealing a high degree of large-scale uniformity. This paves the way for large area fabrication and yield characterization for silicon nanostructures, thereby enabling deployment of NIMS for commercial applications. This process is not limited to circular geometries, and can be extended to any desired geometries due to the versatility of nanoimprint lithography. **Figure 2.8** shows exemplar non-circular geometries demonstrated by J-FIL and MACE.

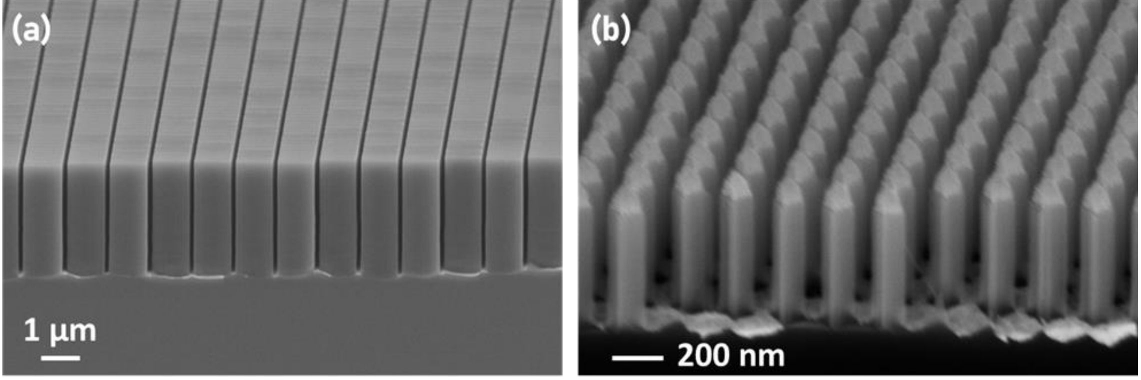


Figure 2.8: Exemplar non-circular geometries fabricated by nanoimprint lithography and Au MACE. (a) rectangular Si fins, (b) diamond-shaped cross-section Si nanowires.

Chapter 3: Insights into Silicon Nanowire Collapse by Analog MACE

Top down patterning along with metal assisted chemical etching (MACE) can enable fabrication of highly controlled wafer-scale silicon nanowires (Si-NWs). Maximizing NW aspect ratio, while avoiding collapse, can enable many important applications. A precise experimental technique has been developed in this chapter‡ to study the onset of Si-NW collapse by creating controlled variation of NW heights using MACE. Micrographs of the resulting structures are processed through a binary feature classification algorithm to precisely detect the onset of nanowire collapse for a range of wire diameters. This experimental approach has resulted in unexpectedly tall Si-NWs for oversized wires separated by sub-50nm gaps. As compared to known theory, a 4.5X increase in maximum aspect ratio was achieved for un-collapsed nanowires with 200nm pitch and 25nm spacing. This discrepancy between known theory and experimental results was eliminated when gold-resist caps (a feature of our MACE process) on top of these nanowires were removed. The incorporation of electrostatic repulsion into known theoretical formulations matches the experimental results.

Thus, this work provides new experimental and theoretical insights into nanowire collapse behavior, and provides a new method of collapse prevention to enable free-standing ultra-high aspect ratio silicon nanostructures.

‡ The work in this chapter was originally published in the following article[98] –
A. Mallavarapu, P. Ajay, S.V. Sreenivasan. "Enabling Ultrahigh-Aspect-Ratio Silicon Nanowires Using Precise Experiments for Detecting Onset of Collapse," *Nano Letters*, vol. 20, no. 11, pp. 7896–7905, Nov. 2020, doi: 10.1021/acs.nanolett.0c02539.
Akhila Mallavarapu designed and performed the experiments, characterized and analyzed the data, and wrote the final paper.

3.1. MOTIVATION

Silicon nanowires (Si NWs) possess several unique electronic, sensory, mechanical and optical characteristics due to their quasi one-dimensional nature and high surface area. Increasing the surface area of the nanowires – both by increasing the aspect ratio and increasing the cross-section perimeter – can enable higher performance transistors,[99,100] memory devices,[10,11] sensors,[13,101–103] capacitors[15,104] and batteries.[105,106] Si NW arrays with vertical sidewalls and precise spacing between NWs can also be used in microfluidics applications such as Nano-DLD arrays to filter sub-50nm biological species such as exosomes and antibodies.[18] However, high aspect ratio silicon nanowires are prone to clustering and collapse[107–109] due to adhesion and capillary forces, which decreases yield and performance in the above applications.

Maximization of surface area of Si NWs while avoiding collapse requires ***precise experimental prediction of onset of collapse***. In this chapter, a method called "Analog MACE" has been developed to intentionally create silicon nanowires with analog etch depth variation. We then use a collapse detection image processing algorithm to determine the etch depth at the onset of collapse in Scanning Electron Microscope (SEM) images of the etched NWs.

3.2. METHODS

MACE is an inexpensive anisotropic electroless chemical etch process that has been used to fabricate high aspect ratio features with sub-20nm resolution in silicon. **Figure 3.1** shows the process flow for a typical MACE process with uniform local etch as seen in the SEMs, where the catalyst is patterned using nanoimprint lithography,[90,110] This process creates highly anisotropic nanofeatures in silicon. Note the presence of gold-resist caps on top of the etched silicon nanowires in Figure 3.1, which are present as the process flow does not require lift-off for catalyst patterning before MACE, thereby improving yield.

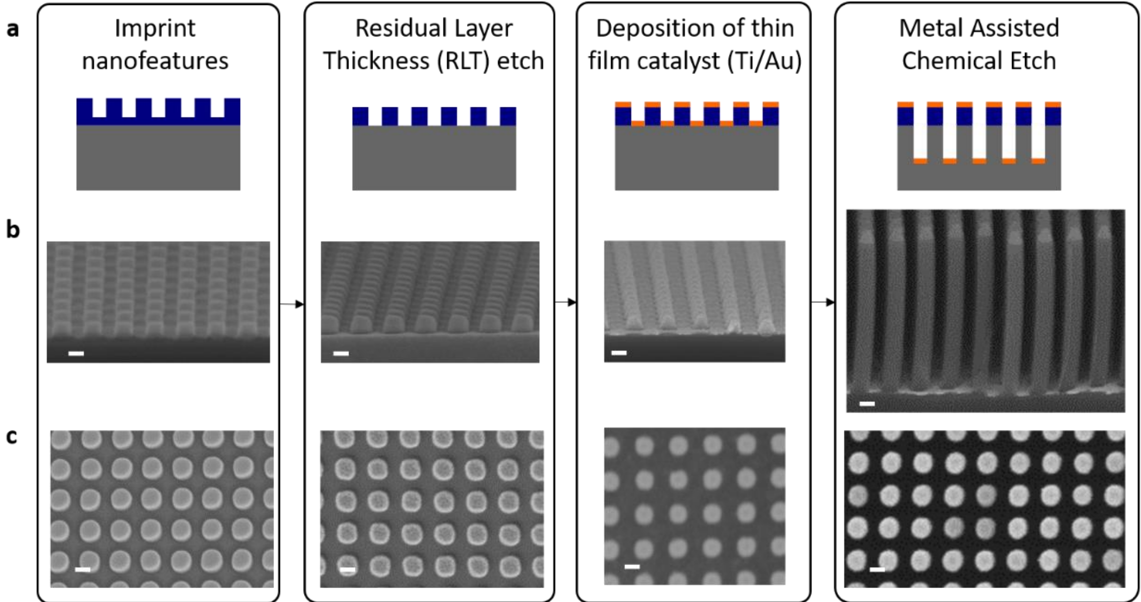


Figure 3.1: Top-down process flow for MACE to create vertically aligned silicon nanowire arrays of 100nm diameter and 200nm pitch. (a) Schematic, (b) Tilted cross-section SEM and (c) Top-down SEM of the process steps. The scale bar in all the SEM images is 100nm.

Intentional variation of the NW heights is achieved using Analog MACE, where the NWs are made with uniformly varying etch depths to determine the height at onset of NW collapse. The resulting SEMs are analyzed for nanowire collapse using Local Binary Pattern defect detection algorithms, and edge detection algorithms are used for consistent

NW diameter and height measurements. This method is used to detect critical collapse heights for SiNWs with diameters ranging from 75-175nm at a pitch of 200nm. The resulting experimental data is then compared to known theoretical collapse models reported in literature.

3.2.1. Analog MACE

Etchant transport to the metal/silicon interface is critical for uniform MACE.[111] Etch uniformity is highly dependent on the method of catalyst patterning and the thickness of the film used. Tuning these parameters can enable intentional analog variation of the etch depth to visualize collapse behavior at the nanoscale.

Gold patterning is typically done in the literature using liftoff.[112] Microscale plasma etching and wet etching of gold[86] were explored, but they led to poor pattern transfer for nanoscale features. Liftoff processes require a break in the gold film after deposition on resist features, where the resist features have an "undercut" profile. Gold on top of the resist features is removed during a wet etch of the resist, leaving behind patterned gold on a silicon wafer. Alternatively, as long as there is a break in the gold film, MACE can occur without a liftoff step. For "overcut" resist features, or for thicker films of gold, if a uniform continuous film is deposited on patterned resist without metal breaks, then MACE will start to occur at pinhole defects and discontinuities in catalyst metal on the wafer. The initiation of such pinholes will further enable etchant transport laterally, causing delayed MACE in the surrounding areas, thereby creating nanowires with an analog variation of heights. **Figure 3.2** shows the difference between MACE for gold deposited on "undercut" features where an oxide underlying layer is used to create an undercut for metal break (also described in Chapter 2), compared to "overcut" features with no underlying layer to create a metal break in the nanoscale pattern. MACE of the two patterns shows the difference in

uniformity of the etch as well as the formation of "pinhole-locations" where the MACE process starts.

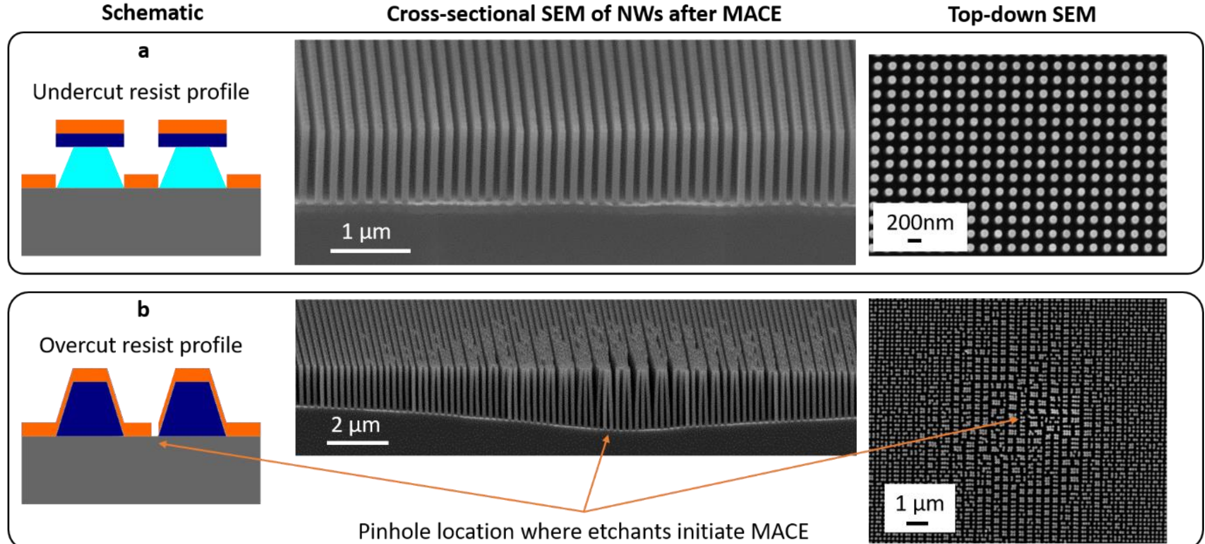


Figure 3.2: Effect of continuous vs discontinuous catalysts on MACE etch variation: (a) Undercut, and (b) Overcut resist profiles and their effect on subsequent MACE to create NWs

The overcut process is used here to locate regions with varying nanowire heights, where the onset of collapse can be visualized as the height at which the tips of two or more nanowires start to touch. **Figure 3.3** shows a 4-inch (100mm) silicon wafer with circular regions showing etch depth variation, which manifest as collapse of tall nanowires. Top-down SEMs show the collapse of nanowires.

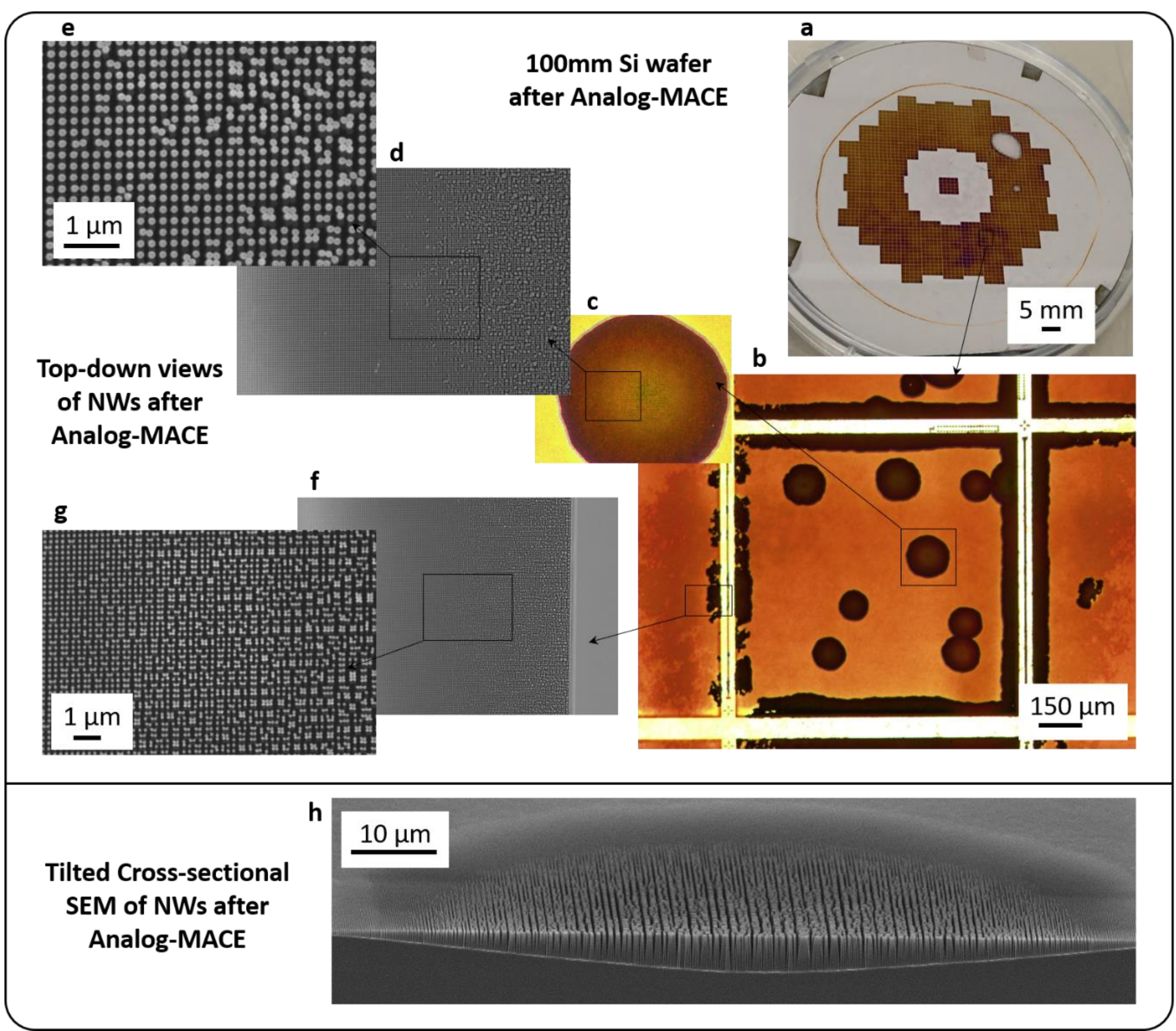


Figure 3.3: Analog etch depth variation in MACE using pinholes in catalyst film, showing progressively magnified insets of silicon nanowire arrays: (a) Optical image of 100mm silicon wafer after Analog MACE in patterned areas, (b, c) Magnified optical images, and (d – g) Top-down SEM images of Si NW arrays. (h) Tilted cross-section SEM image of Si NWs after Analog-MACE, showing variation of NW heights, and collapse for taller NWs.

3.2.2. NW Diameter Control in Catalyst Patterning for MACE

Varying the diameters of these wires can be done by imprint lithography with templates having patterns with different diameters. This is however very expensive due to the cost of making a template with e-beam lithography and the long e-beam write times.

For a given pitch, plasma etching, chemical vapor deposition, or atomic layer deposition can be used to vary the diameters of the resist after imprinting, prior to gold deposition and MACE. **Figure 3.4** shows the process modification from a typical MACE process to change the diameter of the nanowires at a constant pitch.

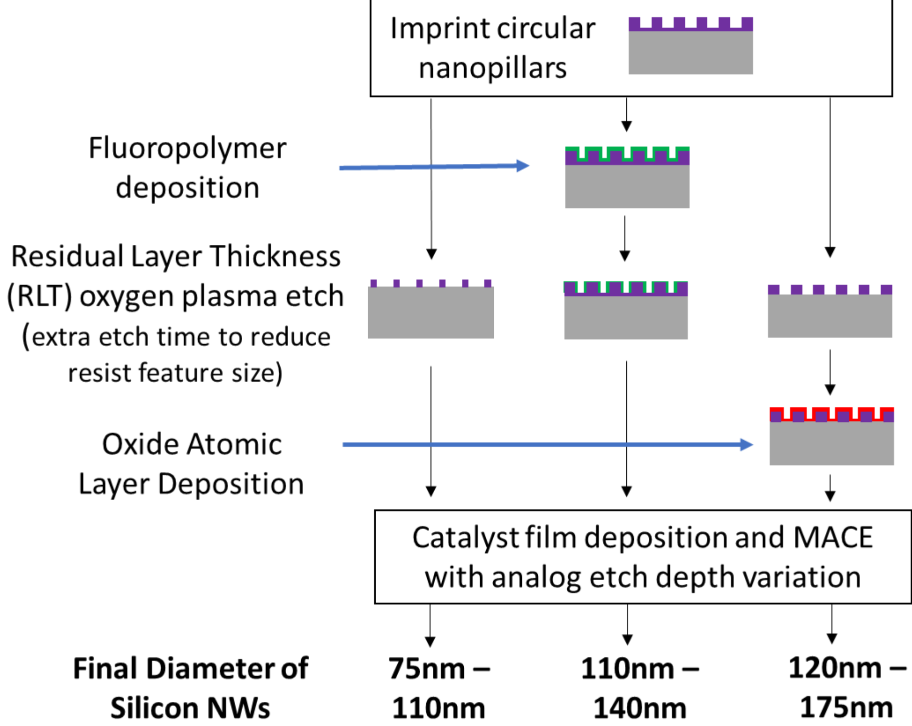


Figure 3.4: Process steps to vary the diameter of imprinted resist pattern to fabricate silicon nanowires with precise diameters ranging from 75-175nm at a constant pitch

NW diameters ranging from 75-110nm are obtained by the standard process shown in Figure 3.1, with an increased residual layer thickness etch time. This is done using an Ar/O_2 plasma etch, with a vertical etch rate of 30nm/min and a lateral etch rate of 5nm/min. Varying the etch times to simultaneously remove the RLT and reduce the diameter allows us to reduce the nanowire diameters. Increasing the etch time to get to diameters below

75nm does not work as the height of the resist pillars is reduced and no pinhole defects or metal break is obtained after gold deposition.

For NW diameters ranging from 110nm – 140nm, a CVD process is used to deposit fluoropolymer on imprinted resist by flowing C_4F_8 gas in a plasma reactor. A thin conformal layer of fluoropolymer is deposited using PlasmaTherm Deep Si RIE tool after imprint, using the recipe – 25mT pressure, 150sccm C_4F_8, 50sccm SF_6, 40sccm Ar, 10V RF Bias, 1600W ICP power for 10s, increasing the diameter of the resist. The residual layer is then removed using oxygen plasma at varying etch times to get circular pillars with diameters ranging from 110nm to 140nm. Diameters greater than 140nm cannot be achieved with this method as the etch time is insufficient to remove the RLT, causing a thin layer of resist to block contact between gold and silicon needed for MACE.

For diameters ranging from 140-175nm, a conformal layer of aluminum oxide is deposited using ALD, after imprint and RLT etch. A conformal coating of aluminum oxide is deposited using Atomic Layer Deposition (ALD) with trimethylaluminum (TMA) and H_2O as precursors in an Argon carrier gas flow, with the substrate held at a temperature of 150^0C. The aluminum oxide thickness is changed by changing the number of ALD cycles, to get the desired pillar thickness. For instance, 30nm of aluminum oxide deposited on a resist pillar of diameter 110nm (after RLT etch) gives a pillar with a diameter of 170nm. Gold deposition and MACE results in silicon nanowires with a diameter of 170nm. The thickness of the wires can be varied by changing the ALD film thickness. The ALD oxide gets etched away during the MACE process. The thickness of the evaporated film is tuned to ensure that the gold film has pinhole defects that cause local etching, to ensure that the density of pinholes is sufficient to prepare cross-sectional SEM samples for characterization.

Gold catalyst and Titanium adhesion layer are deposited on the patterned wafers using electron beam evaporation at a pressure of 5E-6 torr, with gold at a deposition rate of 0.4 A/s, and titanium at a deposition rate of 0.2A/s. For pillars with diameters less than 140nm, 2nm of Ti and 10nm of Au is used. For pillars with diameters greater than 140nm, 2nm of Ti and 7nm of Au is used. The patterned wafer is immersed in a MACE solution comprising of 12.5M HF and 1M H_2O_2 for 30s. The samples are then immersed in a beaker of water, and subsequently rinsed with water and dried with an air gun supplying clean dry air (CDA). The resulting etched silicon nanowires are characterized using tilted cross-section SEMs.

3.2.3. Theoretical Mechanics Models for NW Collapse

Collapse of high aspect ratio nanostructures[113–119] depends on the mechanical properties of the material as well as the forces acting on it. The main modes of failure which may cause collapse nanowires made with MACE are:

(i) buckling due to the weight of the nanowire, and

(ii) surface forces (these are phenomena that keep the features from returning to a vertical position after they have collapsed) including: (a) adhesion to the substrate (ground collapse), and (b) adhesion to neighboring nanowires (lateral collapse), and (c) capillary forces acting on the nanowire when the MACE wet etch solution is drying.

Previous work in literature shows that the collapse height predicted by buckling due to gravity[120,121] is highly overestimated, likely due to other more dominant effects compared to gravity at nanoscale dimensions, along with an increased role of adhesion forces. Roca-Cusachs *et al.*[119] suggest an alternate model using adhesion forces between the nanowire and the ground to explain this phenomenon. For dense arrays of nanowires,

solid-to-solid adhesion forces between wires and capillary forces play a more dominant role than between the wire and substrate.

I. Lateral collapse theory – Glassmaker *et al.*[116]

Glassmaker *et al.* developed a model to estimate the critical height for lateral collapse of nanostructures due to solid-to-solid adhesion forces acting on nanowires, shown in Equation 3.1. In their work, they model lateral collapse of two identical circular wires of height *h*, diameter *d,* separated by a distance *2w*. They assume that the two wires are collapsed at one end, and separated by a spacing of *2w* at the fixed end. The collapsed wires have two regions – a non-contact region of length *L* and a contact region of length *(h-L)*. The wires stay collapsed under an equilibrium condition, where the bending energy of the non-contact portion is balanced by the adhesion energy in the contact portion and the stored elastic energy in the contact region (where elastic deformation of the circular wires occurs). Critical collapse height is determined by energy balance when the non-contact region length is increased by a small amount *dL*. The resulting decrease in bending energy in the non-contact region is equated to the energy required to separate the two surfaces in the contact region by *dL*. For identical nanowires of diameter *d*, spacing 2*w*, elastic modulus *E*, Poisson's ratio *v* and surface energy γ_s, this results in a critical collapse height in Equation 3.1: [116]

$$h_{crit,lateral\ collapse} = \frac{1}{2}\left(\frac{\pi^4 E\, d}{(1-\vartheta^2)\gamma_S}\right)^{1/12}\left(\frac{3Ed^3w^2}{2\gamma_S}\right)^{1/4} \quad (3.1)$$

II. Capillary collapse theory – Chandra and Yang[122]

As MACE is a wet etch process, it is reasonable to consider the effect of capillary forces on the critical aspect ratios. Capillary forces acting on the nanowires occur when the MACE solution is removed after etching and the etching solution dries. Chandra and Yang[122] model the effect of capillary forces on polymer micropillar collapse using

Equation 3.2 by calculating the maximum height at which the capillary force between circular pillars is smaller than the elastic restoring force. For identical nanowires of diameter d, pitch p, elastic modulus E, contact angle θ and surface tension γ_{lv} This results in a critical collapse height in Equation 3.2: [122]

$$h_{crit,capilary\ collapse} = \left(\frac{3Ed^4}{32\sqrt{2}\, cos^2\theta\, \gamma_{lv} f(r)}\right)^{\frac{1}{3}} \tag{3.2a}$$

$$f(r) = \frac{1}{r-k}\left(\sqrt{\frac{2}{k^2-1}} + \sqrt{\frac{1}{2k^2-1}}\right) = ab^r \tag{3.2b}$$

$$r = \frac{1}{k}\left(\frac{\sqrt{2}(k^2-1)^{\frac{-1}{2}} + (2k^2-1)^{\frac{-1}{2}}}{\sqrt{2}(k^2-1)^{\frac{-3}{2}} + 2(2k^2-1)^{\frac{-3}{2}}}\right) + k = \frac{p}{d} \tag{3.2c}$$

The model parameters used are listed in the **Table 3.1**.

Table 3.1: Model parameters for theoretical predictions of Si-NW collapse

Parameter	**Value**
Elastic modulus of Silicon (E)	175 GPa
Density of silicon (ρ)	2390 kg/m^3
Poisson's ratio of silicon (ν)	0.22
Surface energy of silicon (γ_s) [123]	2130 mJ/m^2
Surface tension of water at 25°C (γ_{lv}) [124]	72 mJ/m^2
Silicon/water contact angle after surface treatment with HF [125,126]	60 degrees

3.2.4. Experimental Detection of Onset of NW Collapse

Mechanics models for nanowire collapse described above are compared to experimental results to determine collapse behavior of the wires when their diameter is varied at a given pitch. Silicon nanowires with varying diameters and etch depths are made using nanoimprint lithography, diameter control and Analog-MACE.

Cross-sectional SEM images of the nanowires are taken at a tilt of 70^0 to examine the collapse behavior of the nanowires and to determine the onset of collapse. The diameter and height of pillars is measured using an edge detection algorithm on the resulting micrographs, and the onset of collapse is detected using Local Binary Pattern (LBP) based texture classification. The problem of collapse detection in tilted SEM images is essentially one of detecting the onset of change from a specified grid pattern, to an irregular and/or a different grid pattern. Thus, the determination of collapse requires one to encode the periodic nature of nanopillar grids in some manner, and to detect variations in the periodicity. Defect detection in textiles is a good analog for the problem of collapse detection in nanopillar arrays – both involve images that have repeating unit structures, where a defect might consist simply of subtle variations in periodicity of the repeating units. A variety of textile defect detection algorithms were surveyed,[127–129] and the Local Binary Pattern (LBP) based approach of Tajeripour et al.[128] was identified as ideal for our work as – 1. LBP is a fairly robust classifier of textures, 2. The relatively simple implementation lends itself well to real-time computation. We incorporate scikit-image's rotation-invariant LBP implementation in Python[130] for our analysis. The Graphical User Interface (GUI) for our tool is built around the FAN-tool.[131]

A periodic un-collapsed region in the SEM image is first used to compute a reference feature vector and a detection threshold, which are then applied to the SEM image to detect collapsed regions. Note that the LBP based approach is agnostic to the SEM tilt, and the size, shape, and orientation of the nanowires. Apart from making the detection generally robust, this feature is also critical for the precise detection of the pillar height at the onset of collapse, since LBP can be used to detect collapse in tilted cross-section SEM images where both top-down and lateral data is available simultaneously, instead of separate top-down and cross-section images. **Figure 3.5** shows an exemplar

implementation of the LBP based approach. Note that LBP algorithm only classifies regions of the image as collapsed or uncollapsed. To obtain the *collapse front*, which demarcates the image into a largely collapsed and a largely uncollapsed region, further processing is done. First, at each Y location, the centroid of the collapsed and un-collapsed pixels is computed. If the centroids are closer to each other than a small, pre-specified limit (implying that the collapsed and un-collapsed regions are interspersed uniformly at that Y location, and therefore a boundary cannot be determined), that particular Y value is excluded from the collapse front calculation. The front at a particular Y-coordinate (Y_j) in the image is calculated by dividing the line connecting the centroids of the collapsed and uncollapsed regions in the ratio of the number of pixels in those regions, as follows –

$$X_{collapse-front} = \frac{n_{collapsed\ pixels} * X_{uncollapsed\ centroid} + n_{uncollapsed\ pixels} * X_{collapsed\ centroid}}{n_{uncollapsed\ pixels} + n_{collapsed\ pixels}} \quad (3.3)$$

where, $X_{collapse\text{-}front}$ is the X-coordinate of the collapse-front at Y_j, $n_{uncollapsed\ \mathrm{pixels}}$ is the number of pixels marked un-collapsed by the LBP-based algorithm (at Y_j), $X_{uncollapsed\ centroid}$ is the X-coordinate of the centroid of the pixels marked as collapsed (at Y_j). The overall collapse-front is determined by linearly interpolating $X_{collapse\text{-}front}$ values for all values of Y. This line is plotted in the image in blue, as shown in Figure 3.5.

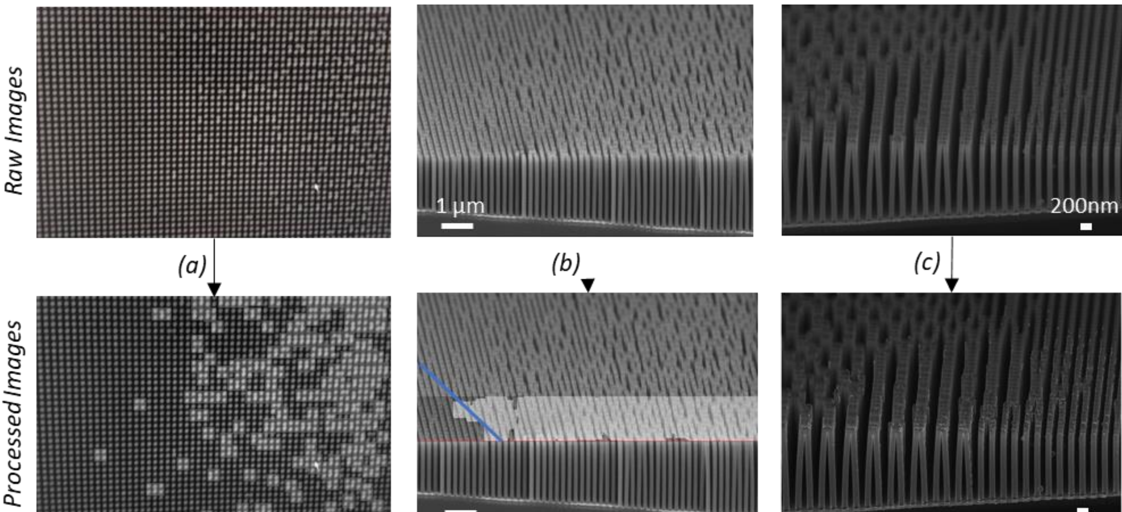


Figure 3.5: Implementation of the modified LBP algorithm for collapse determination in (a) top-down SEM images, (b) tilted-cross-section images: the blue line shows the front for onset of collapse, and (c) edge detection to evaluate diameter of pillars at the onset of collapse

This method of collapse-front determination was validated by comparing the experimental results of critical nanowire height to lateral collapse models for diameter-to-pitch ratios of < 0.5, as Zeniou *et al.*[113] validated lateral collapse theory for SiNWs that are thinner than half of the pitch. We then use the same parameters to determine collapse fronts for all our experiments.

For nanowires made with Process 3 (using oxide atomic layer deposition to tune the diameter) in Figure 3.4, we see irregularities in the un-collapsed portion as well. This is due to etch of diameter-increasing ALD oxide layer surrounding the resist during the MACE process. This causes the resist to move on top of the etched nanowire, as shown in **Figure 3.6.** Training of the LBP algorithm on the known un-collapsed region takes into account these irregularities during collapse prediction. Additionally, for NW diameters 140-175nm, due to the reduced spacing between the wires, the thickness of the gold catalyst film is reduced to 6nm to enable creation of pinholes. This causes some portions of the thinner catalyst to break during MACE, and a tapered (varying diameter) structure gets

etched into the silicon as the broken mesh goes through the MACE process. This is marked at two locations at the foot of the SEMs in Figure 3.6. Images where this type of catalyst tear occurs near the critical collapse region are considered anomalies relative to this collapse study, and are therefore not considered for experimental estimation of collapse onset.

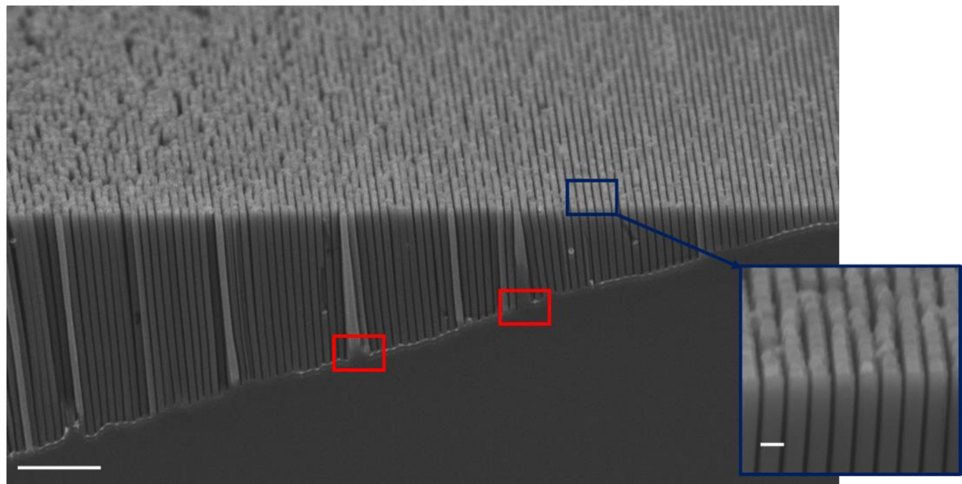


Figure 3.6: Etch depth variation for nanowires with a diameter of 170nm. The tops of the wires (inset) show that the thinner resist has shifted during the etch, but the Si NWs are uncollapsed. The red boxes at the foot of the wires show a break in the catalyst film causing tapered etch. The scale bar of the image is 2 microns, and the inset scale bar is 200nm

3.3. RESULTS AND DISCUSSION

Height and diameter of the collapsed nanowires are measured using an edge detection algorithm, where the diameters are measured at a magnification of 50,000X, and the heights are measured at a magnification of 25,000X. This magnification allows us to visualize the height variation from un-collapsed to heavily collapsed, thereby enabling precise collapse transition height analysis. At these magnifications, the error in measurement of diameter is ±3nm, and of height is ±6nm, based on the image pixel size.

Figure 3.7 shows images corresponding to etch depth variations of nanowires with diameters ranging from 75-175nm at a pitch of 200nm, with the collapse front line shown in blue in the SEM images. The results are plotted alongside theoretical predictions of collapse defined in Equations 3.1 and 3.2. The data shows a good match between adhesion collapse theory[116] and experimental results for nanowires with a diameter < 120nm. However, at larger diameters (smaller spacing), these precise experiments consistently result in higher NW heights and therefore refutes the model predictions. In fact, surprisingly, the trend indicates that at larger diameters (smaller spacing) the collapse height increases significantly, in contrast with existing theoretical models which predict that the height will trend downwards with increase in diameter-to-pitch ratio. The experimental results thus show a marked improvement in un-collapsed surface area of nanowires, compared to theoretical predictions.

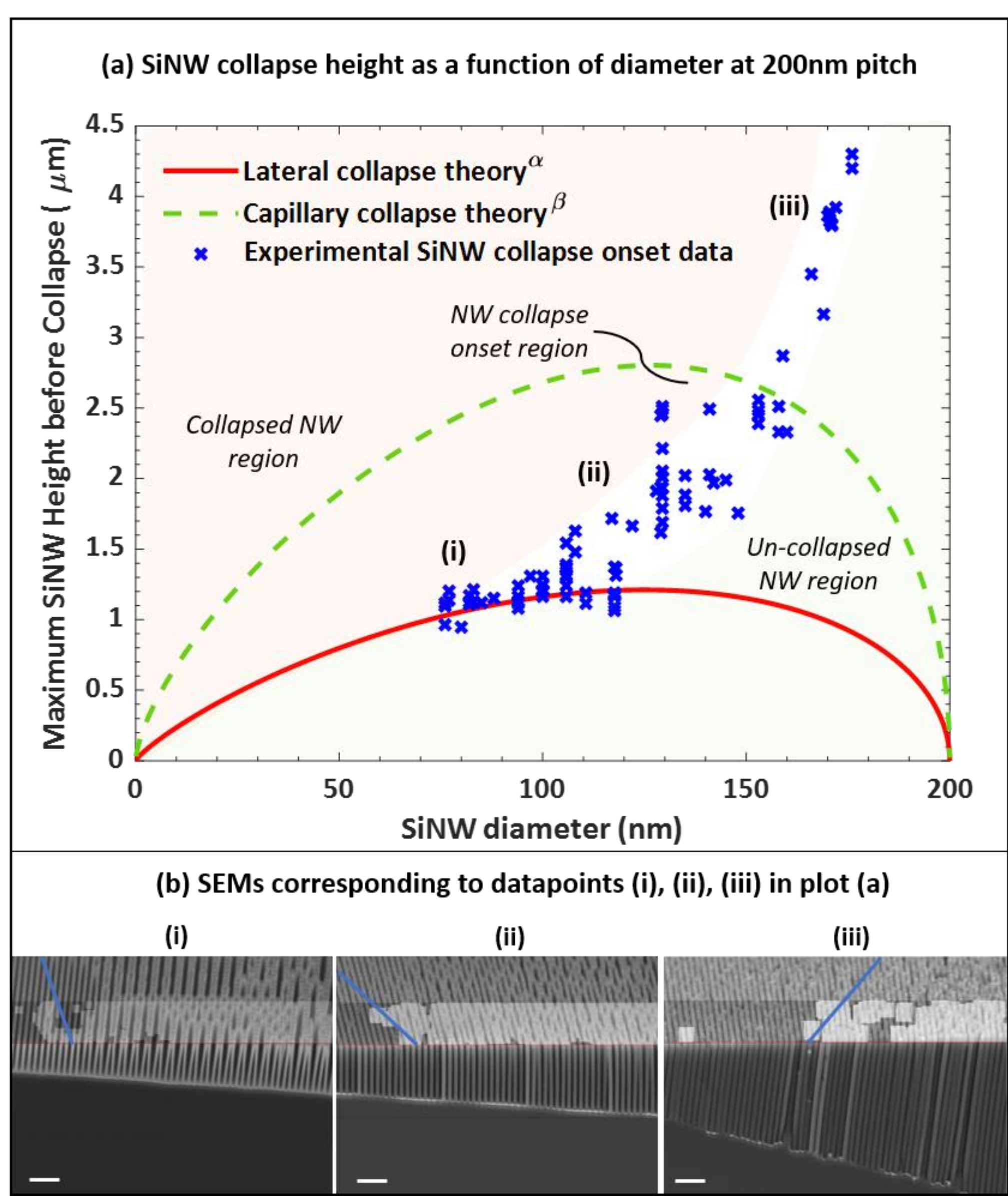


Figure 3.7: Plot of experimental and theoretical critical collapse heights for circular silicon nanowires with diameters varying from 75-175nm at a pitch of 200nm. The theoretical collapse models are adapted from (α) Glassmaker et al.[116] and (β) Chandra and Yang[114]. Tilted cross-section SEMs below the graph show the onset of NW collapse with collapsed regions identified by Local Binary Pattern based image processing. The scale bar of the SEMs is 1 micron.

3.3.1. Cause of Si NW collapse

Table 3.2 compares our experimental results in Figure 3.7 to the lateral collapse model (Theory 1) and the capillary collapse model (Theory 2). For mid-sized wires, the experimental results match lateral collapse theory quite well in the range of ($d/p = 0.375$ to 0.6), similar to observations by other relevant studies[113,132].

Table 3.2: Silicon NW collapse literature – Experiments and Theory

Si NW Array Geometry (d: NW diameter, p: pitch)	Bottom-up patterning combined with MACE	Top-down patterning and RIE	Top-down patterning and MACE
Poor long-range control (Nanoforests)	Ref. [33,78,133] *Collapse cause stated:* Theory 2 (Capillary) *Evidence:* insufficient (*)		
Controlled mid-sized $0.375 < d/p < 0.6$		Ref. [113,132] *Collapse cause stated:* Theory 1 (Lateral) *Evidence:* sufficient (#)	This work (+) *Collapse cause:* Theory 1 *Evidence*: sufficient (§)
Controlled oversized $d/p > 0.6$			This work (+) *Collapse cause*: Unknown Theory 1 extended (ψ)

(+) We used analog etch height control and image processing for collapse detection. Surface properties of silicon right after MACE are chosen carefully to ensure Theory 1 and Theory 2 are accurately implemented.
(*) Reason for stating collapse as due to capillary forces is insufficient, as Ref.[33,78,133] did not carefully study collapse and/or control for NW diameter, height or pitch. Sputtered Au and AgNO3 as MACE catalysts have poor control of lateral dimension, while BCP self-assembly has local order, but does not have long range order.
(#) These two papers used top-down lithography and controlled etch height in their studies, similar to this work. They state that Theory 2 (capillary) is not valid for onset of collapse.
(§) For mid-sized wires, our work confirms the observations of [113,132], that Si NW collapse is due to Theory 1.
(ψ) For oversized wires, our experimental observations do not match the values or trends of both theories, demonstrating the need for new/extended theories. Inclusion of electrostatic charges in the lateral collapse theory helps explain this anomalous behavior

The papers that suggest that the cause of Si-NW collapse is due to capillary forces do not precisely control and vary the NW diameters and heights to conclusively state that the cause is capillary. This is in contrast to literature in polymer nanostructure collapse, which is dominated by capillary collapse likely due to permanent plastic deformation after collapse (due to capillary forces during drying). However plastic deformation is unlikely for small lateral bending of nanowires made of crystalline silicon. Once the drying is completed, the collapsed silicon nanowires will spring back due to the restoring elastic forces unless solid-solid adhesion forces are strong enough to ensure that the nanowires remain collapsed. In this sense, capillary forces can act as an initial source of nanowire collapse in silicon, but adhesion forces determine whether they will stay collapsed.

For over-sized nanowires in the range of $d/p>0.6$, the collapse of MACE nanowires shows anomalous behavior at low wire-to-wire gaps. Conventional collapse theory – the solid-solid adhesion model[116] and the capillary collapse model[114] – predicts that as the gap between NWs becomes close to zero, nanowire collapse height should decrease and become close to zero as well (Figure 3.7). However, our experiments show the opposite trend. Similar anomalous tall nanowires were obtained for plasma-etched silicon nanowires at a 100nm pitch by Khorasaninejad et al.[132] They posit that this is due to increased mechanical stiffness of thicker wires as compared to increased adhesion forces due to reduced spacing. However, lateral collapse models described previously include both these parameters but fail to predict the trend of higher critical collapse heights for smaller gaps and larger diameter nanowires.

The data suggests that there might be additional repulsive forces, not accounted for in the models, for small gaps between the wires, that cause the observed anomalous high critical heights. Based on literature[134], these repulsive forces between nanowires could likely be due to electrostatic effects, arising from charges that are present in the resist-gold

caps of the nanowires, or within the silicon nanowires and nanowire surfaces. In fact, when the gold and imprint resist is removed after Analog MACE using a gold wet etchant and piranha, we observe that critical collapse height drops to values close to the adhesion theory predictions **(Figure 3.8)**.

This observation, along with the fact that the collapse critical heights increase with decreasing gaps, suggests that the deviation of our experimental results from lateral collapse theory for oversized nanowires is likely due to electrostatic repulsion, which itself is correlated to the presence of gold-resist caps. The theoretical model in the next section supports this hypothesis. The fact that the collapse height after gold-resist cap removal does not fully match lateral collapse theory resulting in a marginally higher collapse height is likely due to changes in the surface energy of Si NWs due to the oxidizing nature of the resist cap removal process.

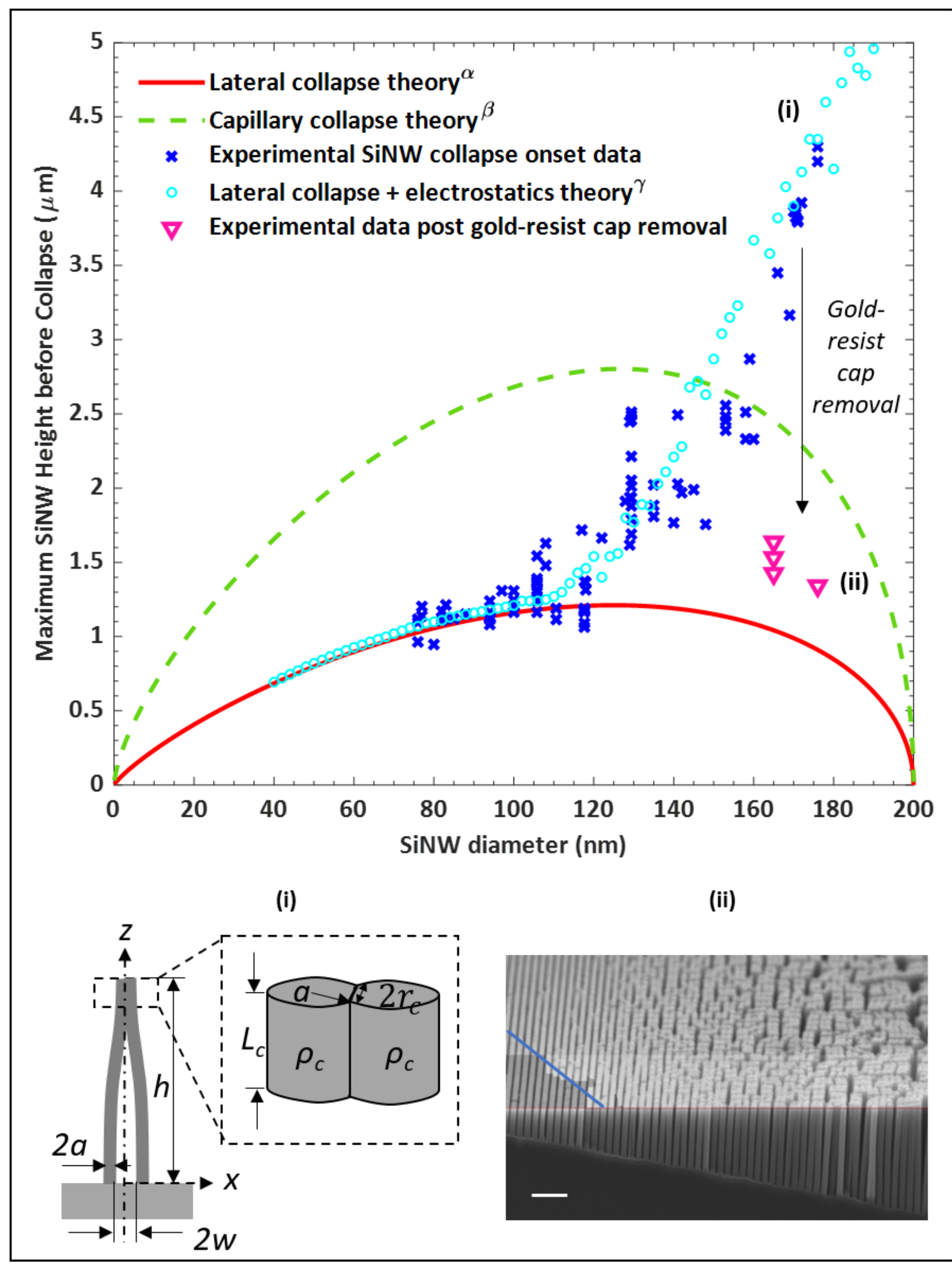


Figure 3.8: Additions to the plot in Figure 3.7, showing a plot with modifications to the lateral collapse theory model to include electrostatic repulsion (γ), and effect of removal of gold-resist caps on oversized NW collapse. (i) Schematic illustration of a pair of collapsed charged nanowires, with variables used for lateral collapse model with electrostatics. (ii) Tilted cross-section SEM of oversized silicon NWs after removal of gold-resist caps, showing collapse onset at shorter heights. The scale bar is 1 micron.

3.3.2. Anomalous Oversized NW Collapse Behavior

As shown in Figure 3.8, the observed trend with oversized nanowire collapse disagrees with the trend predicted by lateral collapse theory (nanowire collapse height increases instead of decreasing with increase in NW diameter). Here, we present a collapse model which includes repulsive electrostatic forces. In this model, we modify the lateral collapse model[116] to include charges near the top of the nanowires. Consider the nanowires shown in Figure 3.8(i), where the nanowires have collapsed and have a contact length of L_c.

The equilibrium contact width, $c_0 = 2r_c$, is derived using Johnson-Kendall-Roberts (JKR) theory of adhesion[135] by Glassmaker et al.[116] for the case of two identical cylinders subject to *no external force:*

$$r_c = \left(\frac{32a^2\gamma_s}{\pi E^*}\right)^{1/3} \tag{3.4}$$

Equation (3.1) is now modified to include the repulsion due to electrostatic force. We assume that the nanowires each carry an average volumetric charge density $\rho_{c,avg}$ that resides near the top of the nanowires (within and up to L_c in the current analysis). This is a reasonable assumption, since the likely source of the charges – the gold-resist caps, are present only at the top of the nanowires, as observed in Figure 3.6. A schematic of the gold-resist caps is shown in Figure 3.1 on nanowires after MACE.

In the lateral collapse model[115,116], the estimation of adhesion energy and elastic deformation of the region of contact between the nanowires requires calculating the contact width. Johnson-Kendall-Roberts (JKR) theory of adhesion[135] is used to predict the equilibrium contact width for two identical cylinders subject to *no external force*. We modify this model to include coulombic repulsion due to electrostatics as an external force P per unit length, leading to an updated JKR model in Equation (3.5)

$$P = \frac{\pi E^* r_c^2}{4a} - \sqrt{2 r_c \pi E^* \gamma_s} \quad (3.5)$$

$$where, P \cong -k_e \frac{(\pi a^2 L_c \rho_{c,avg})(\pi a^2 L_c \rho_{c,avg})}{(2a)^2} * \frac{1}{L_c} \quad (3.6)$$

$$\frac{\partial U_C}{\partial r_c} = 4\gamma_s \quad (3.7)$$

$$\frac{36EIw^2 dL_c}{L_c^4} = (2\gamma_s c_0 - U_C) \quad (3.8)$$

with P as the external force per unit length Lc, contact length r_c, diameter $2a$, $E^* = E/(1-\nu^2)$, elastic modulus E, Poisson's ratio ν, spacing $2w$, surface energy γ_s, and ρ_c as charge density. U_c is the compressive energy at the contact area. Equation (3.5) and (3.6) are solved numerically for r_c, and then substituted into equations (3.7) and (3.8) in Glassmaker et al.[116] to derive the collapse height. Note that the charges present within the fixed contact length L_c do not perform any work as the contact length is advanced. Hence, equation (3.8) remains unchanged. The expression for P is approximate, and is adequate to capture the trend seen in our experiments. A more accurate analysis of electrostatic repulsion could be done, if needed, by solving the drift-diffusion equations for the two interacting nanowires with gold-resist caps. **Figure 3.9** shows a plot of the collapse height for various values of nanowire charge density ($\rho_{c,avg}$). While the plot does show signs of following the anomalous trend, beyond certain charge densities and diameter values (for instance, beyond points A and B in Figure 3.9), the repulsive coulombic force is strong enough that the nanowires never collapse. However, even at these high values of charge density and diameter, we do see some nanowire collapse. This is likely due to stochastic variation between nanowires in the charge density held.

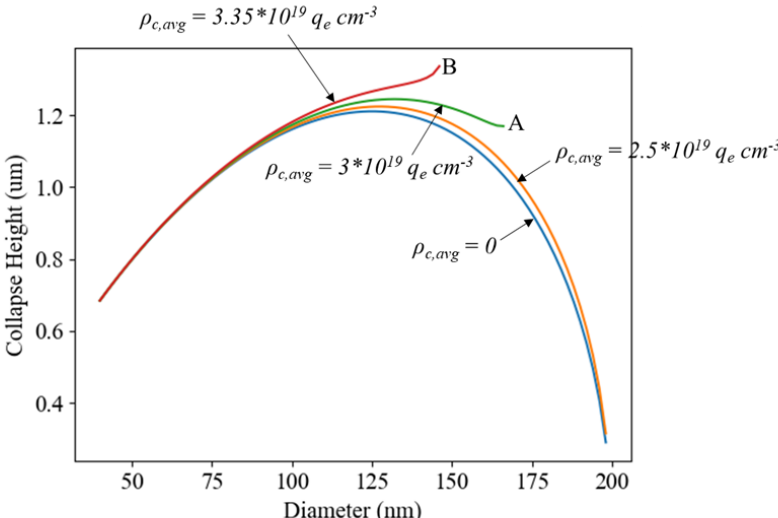


Figure 3.9: Plot of nanowire collapse height for various values of NW charge density ($\rho_{c,avg}$). q_e is the elementary charge. A fixed, small contact length of L_c = 20nm is assumed here. For the current model (with a fixed charge density) beyond points A and B, for the green and red curves respectively, the repulsive coulombic force is strong enough that nanowire collapse never happens.

Stochastic variation between charge densities in the oversized nanowires with gold-resist caps is included using a normal distribution. A fixed, small contact length of L_c = 20nm, and a maximum un-collapsed height of 10um is assumed, beyond which the nanowires are assumed to be collapsed by default. Based on this new model, we achieve a plot with the same trends as observed experimentally in Figure 3.8. Thus, the addition of electrostatic repulsion to the lateral collapse theory appears justifiable. We obtain a good fit between our experimental results and our electrostatics-enhanced lateral collapse model for a normally distributed nanowire charge density with mean $\rho_{c,mean} = 6.4*10^{19}\ q_e\ cm^{-3}$ and standard deviation $\rho_{c,SD} = 1.7*10^{19}\ q_e\ cm^{-3}$ where q_e is the elementary charge. The origin of electrostatic charges may be due to the electrochemical nature and flow[136] of the etchant during MACE. The retention of such charges after MACE may be due to a native oxide shell around the wire. For instance, silicon nanowires with permanent static charges were reported in the literature using oxide-assisted growth and thermal annealing.[137] It is worth

noting that the suggested repulsive forces may not be due to electron-beams during SEM characterization as they have been reported to be attractive in nature.[138] In summary, we have experimentally demonstrated that oversized silicon nanowires made using the MACE process in Figure 3.1 do not collapse for unexpectedly large nanowire heights, and that the reason for this anomalous behavior is due to the presence of gold-resist caps on top of the wires. Further, we have developed collapse theory based on electrostatic repulsion that shows good agreement with the experimental results.

This chapter thus describes a new experimental methodology which enables precisely controlled diameter and analog etch depth variation in silicon nanowires fabricated with nanoimprint lithography and MACE. Precise experimental estimation of onset of collapse in silicon nanowires made by this approach is performed using edge detection and Local Binary Pattern defect detection algorithms. For oversized nanowires with diameters > 120nm at a fixed pitch of 200nm, the experimental results and trends depart from known theoretical models to give unexpectedly tall free-standing nanowires. Removal of gold-resist caps (a feature of our MACE process) on top of these oversized nanowires brings the collapse height back down to known collapse theory. This suggests that this unexpected behavior is likely due to electrostatic repulsion correlated to the presence of gold-resist caps. By including electrostatic repulsion in the lateral collapse theory, the same trends observed experimentally are achieved. In summary, this work presents two important contributions: (1) a process to achieve ultra-high aspect ratio un-collapsed silicon nanowires that enables ~ 4.5X improvement in maximum aspect ratio than predicted by known models, and (2) a modified lateral collapse model that includes an electrostatic repulsion component that matches observed experimental results.

Chapter 4: Ruthenium Assisted Chemical Etch of Silicon

The semiconductor industry's transition to 3D logic and memory devices has revealed the limitations of plasma etching in reliable creation of vertical high aspect ratio (HAR) nanostructures. Metal Assisted Chemical Etching (MACE) can create ultra-HAR, taper-free nanostructures in silicon, but the catalyst used for reliable MACE – gold – is not CMOS-compatible and therefore cannot be used in the semiconductor industry. In this chapter[§], CMOS-compatible alternatives to gold are explored.

For the first time, a Ruthenium MACE process that is porosity-free, taper-free, HAR and is comparable in quality to Au MACE is reported here. New process variables – catalyst plasma treatment and Ru surface area – are used to achieve this result. Ruthenium is particularly desirable as it is not only CMOS-compatible but has also been introduced in the fab as an interconnect material. The results presented here remove a significant barrier to adoption of MACE for scalable fabrication of 3D semiconductor devices, sensors, and biodevices that can benefit from production in CMOS foundries.[139]

[§] The work in this chapter overlaps with the following article[139] –
A. Mallavarapu, P. Ajay, C. Barrera, S.V. Sreenivasan. "Ruthenium Assisted Chemical Etching of Silicon – Enabling CMOS-Compatible 3D Semiconductor Device Nanofabrication", *Accepted, ACS Applied Materials and Interfaces,* 2020.
Akhila Mallavarapu designed and performed the experiments, characterized and analyzed the data, and wrote the final paper.

4.1. MOTIVATION

Gold is the catalyst of choice in MACE literature due to its ability to robustly create non-porous, high aspect ratio, vertical silicon nanostructures[20,30,31]. However Au is not CMOS-compatible and cannot be used in semiconductor fabs as it is known to cause undesirable deep-level defects in silicon circuits[140]. Developing a CMOS-compatible catalyst could allow the use of MACE to create ultrahigh aspect ratio 3D device structures such as silicon fins for finFETs[141] and trenches for DRAM capacitors[142], thereby potentially enabling higher performance and higher density logic and memory devices.

A CMOS-compatible MACE process that can be deployed in a semiconductor foundry also enables cost-effective scaling for a wide variety of non-CMOS devices that require precise, high throughput, high yield nanofabrication. Services like MOSIS[143,144] offer prototyping, development and high volume manufacturing of nanodevices at semiconductor fabrication facilities such as Global Foundries and TSMC. Silicon photonic integrated circuits[145], atomic force microscopes-on-a-chip[146,147], optical clocks[148], silicon nanobiosensors[149], and nanoscale deterministic lateral displacement (nanoDLD) devices for biological particle separation[18] have all been demonstrated in CMOS fabs. Thus, devices that need high aspect ratio silicon nanofeatures such as nanoDLD arrays[18], X-ray[20,24] and visible wavelength[70] optical components, nanowire sensors[103], etc. suffer from plasma induced sidewall damage and etch taper as they use semiconductor-compatible plasma etching.

MACE has superior etch anisotropy and sidewall profile, and can improve performance of these devices, but the use of gold prohibits its process integration in manufacturing of these devices. To unlock this potential of MACE for CMOS fabrication facilities, this chapter demonstrates MACE with CMOS-compatible materials and processes, with etch results comparable to those achieved by gold.

4.2. METHODS

The main criteria for a material to act as an effective catalyst for MACE of silicon, based on the mechanisms for MACE[31] are as follows:

(i) Does not react with or dissolve in the MACE etchant. Hydrofluoric acid (HF), one of the main components of the MACE etchant, is a highly reactive chemical and limits the number of materials that can be used as catalysts.

(ii) Catalyzes reduction of oxidant components in the MACE etchant (such as H_2O_2)

(iii) Locally injects holes into the silicon substrate at the catalyst locations

(iv) Sinks into etched silicon features to enable continuous etch

Au, Ag, Pt, and Pd have been explored as MACE catalysts in literature[31,45,68,150], with Au showing the desired characteristics – i.e. porosity-free, taper-free, high aspect ratio nanostructures over large areas. Unlike Au, Ag MACE suffers from poor catalyst stability in the etchant solution, causing Ag dissolution and redeposition.[45,68,151] Pt and Pd MACE in literature show formation of undesirable, extraneous silicon porosity during MACE[48,49]. CMOS-compatible MACE catalysts that are described in the literature (such as TiN[52], Graphene[50], W[152]) have not produced silicon nanostructures comparable to those made by gold.

Ruthenium is a promising alternative for MACE as it already used in semiconductor fabs as a barrier metal for interconnects[153,154], and is listed in IRDS roadmaps as the next metal for future generation metal interconnects in logic devices, and as a metal electrode for DRAM capacitors[155–157]. Thus, there is a semiconductor ecosystem already in place for Ruthenium thin film deposition with high yield and low defectivity, and patterning and etch of sub-20nm features in Ru. This research in Ru-based MACE aims to leverage this existing Ru ecosystem in the semiconductor industry.

Ru is a promising catalyst for MACE, as it does not dissolve in HF or H_2O_2, and Ru nanoparticles have demonstrated MACE of Si[158] and electrocatalytic behavior for hydrogen evolution reactions[159]. As MACE also produces hydrogen as one of the reaction products and the MACE catalyst acts as a local electrode[111,160], nanopatterned Ru was tested as a MACE catalyst. **Figure 4.1** shows the nanofabrication process flow for Ru MACE.

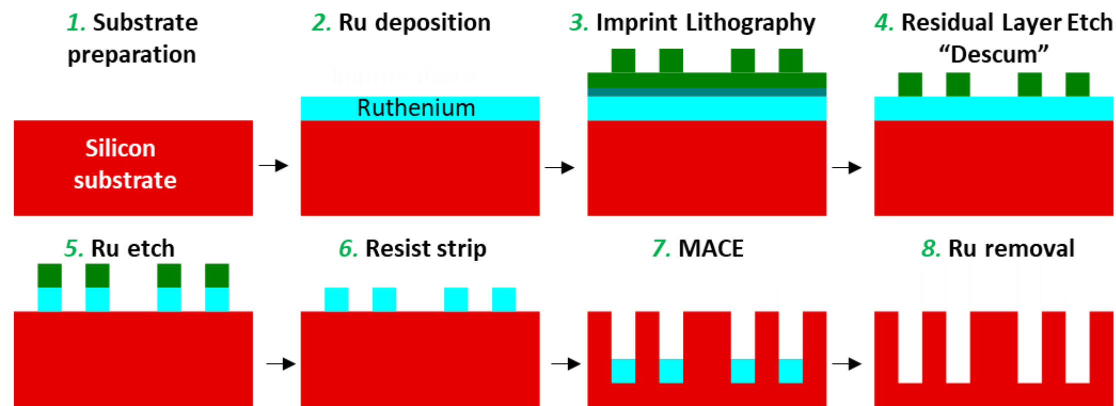


Figure 4.1: Process flow of patterning and MACE with Ruthenium

Thin films of Ruthenium for MACE were patterned using Jet and Flash Nanoimprint lithography (J-FIL)[90] over 100 mm wafers. An Ar/O_2 plasma was used in the descum etch step to remove resist residual layer thickness (RLT) prior to Ru etch. In this work, Ru is etched using a diluted wet etchant from Transene Inc.[161], resulting in isotropically etched Ru mesh pattern. As the Ru catalyst film is ~5nm thick, and the nominal pattern size is ~100nm, isotropic etching of Ru provides a feasible path to explore Ru-MACE. Plasma etch of Ru is well-known and used in the semiconductor industry for making Ru nanopatterns[156]. While plasma etch of Ru would be the ideal choice in the long-run, wet etch of Ru was chosen here as this research did not have access to a plasma etcher for Ru etch. Following Ru wet etch, the imprint resist was removed in a piranha solution.

MACE was performed by immersing the patterned sample in a solution comprising of HF and H_2O_2.

The MACE mechanism suggests that an open circuit local redox reaction occurs at the site of the catalyst, with cathodic and anodic reactions proposed by Li and Bohn[36], Huang *et al.*[31] and Chartier *et al.*[162], where *n* depends on the oxidation state of silicon.

(i) cathodic reaction: $H_2O_2 + 2H^+ \xrightarrow{catalyst} 2H_2O + 2h^+$

(ii) anodic reaction: $Si + 6HF + nh^+ \rightarrow H_2SiF_6 + nH^+ + \frac{4-n}{2}H_2 \uparrow$

The above mechanism was described for catalysts such as Au, Ag, Pt and Pd, and may equally apply for Ru. Therefore, Ru catalyzes the reduction of H_2O_2 and injects the resulting electronic holes into silicon, thereby changing the oxidation state of silicon. HF selectively etches this silicon, and Ru sinks into the etched region to continue the local redox reaction, thereby producing silicon nanostructures in areas without Ru. The characteristics of the resulting silicon nanostructures are highly dependent on the balance of reaction rates, charge transfer, etchant mass transfer and movement of the catalyst. **Figure 4.2** shows a schematic of rates of hole generation (cathode reaction rate R_C), charge transfer (hole injection rate R_i and hole diffusion rate R_D) and hole-oxidized silicon etch rate (anode reaction rate R_A) which depend on the etchant mass transport to the location of hole-oxidized silicon. For optimized Au MACE, the balance of these reactions enables creation of robust porosity-free, taper-free, high aspect ratio silicon nanostructures.

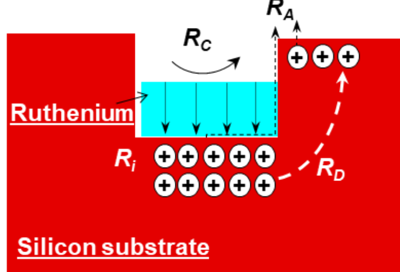


Figure 4.2: Ru MACE reaction rates, showing rates R_C: cathodic reaction, R_i: hole injection, R_D: hole diffusion and R_A: anodic reaction.

Figure 4.3 shows initial evidence that Ru causes silicon etch by MACE. The Ru MACE etch regime depends on the native silicon oxide layer – highly porous silicon layer is formed when the native oxide is removed by HF prior to Ru deposition in the process flow in Figure 4.1. The presence of the native oxide layer results in lower porosity etch to produce porous silicon nanowires with a porous silicon layer underneath. A possible reason for this might be the effect of the Ru/Si interface contact. The rate of injection of holes is lower at the beginning of Ru MACE due to the presence of the native oxide layer. This reduces the amount of silicon oxidized at the beginning of the etch and allows HF to etch locally before the injected holes diffuse to non-catalyst areas. The mesh then sinks into the substrate, creating larger access for HF, and better balance of the rates of HF transport and hole diffusion. Better ohmic contact in Figure 4.3(c) may cause much higher rates of injection of holes into the substrate than the HF etch rates of oxidized silicon, resulting in diffusion of holes to areas outside the local vicinity of the catalyst, causing bulk porous Si formation. A native oxide between Ru and Si may delay the injection of holes till after MACE starts to occur.

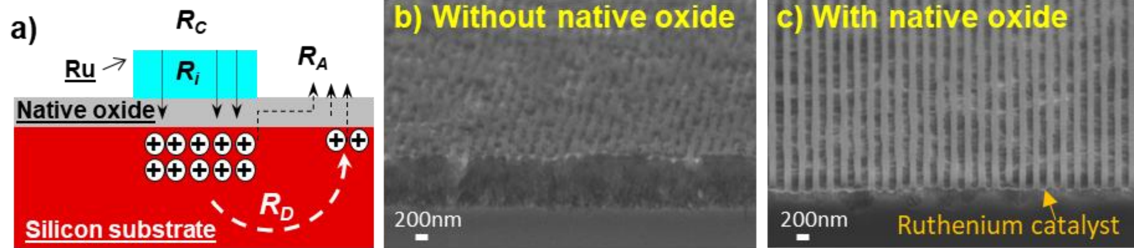


Figure 4.3: Effect of native oxide layer on Si porosity. (a) MACE schematic; Tilted cross-section SEM images of porous silicon nanowires made using MACE where the native oxide layer was (b) removed, (c) not removed, prior to Ru deposition for Ru MACE.

However, these preliminary Ru MACE results show high extraneous porosity, compared to Au MACE. The sub-sections below describe process modifications to reduce

porosity of the silicon nanostructures created by Ru-MACE, based on experimental results reported in literature for Au MACE. Porosity in silicon made by Au MACE can occur due to high substrate doping concentrations, high H_2O_2 in etchant concentration[63], etc., suggesting that excess holes created and injected into silicon during Au MACE can result in extraneous porosity. Reduction in porosity due to Au MACE has been demonstrated by reducing H_2O_2 in the etchant concentration[63] and reducing the etch temperature[163].

4.2.1. Effect of Etchant Concentrations and Temperature

For Au MACE, the etchant concentration plays an important role in the amount of porosity created, with lower H_2O_2 and higher HF concentrations resulting in non-porous etch.[63] To understand the effect of etchant concentration on Ru MACE, samples with nanopatterned Ru on silicon were exposed to different concentrations of HF and H_2O_2. Here, the molar concentration ratio of H_2O_2 is defined as[57,67,162,164]

$$\rho[H_2O_2] = \frac{H_2O_2\,[M]}{HF\,[M] + H_2O_2\,[M]}$$

Low concentrations of HF and high H_2O_2 caused delamination of the film, leaving behind pitted areas corresponding to the Ru patterns, likely due to highly porous or electropolishing regime for high H_2O_2 with Ru. For high HF and low H_2O_2, Ru MACE created highly porous silicon, with local areas showing porous silicon nanowires with a porous silicon underlayer. The effect of changing the MACE concentrations on Ru is, however, not strong enough to reduce the porosity to morphologies similar to Au MACE, as shown in **Figure 4.4**.

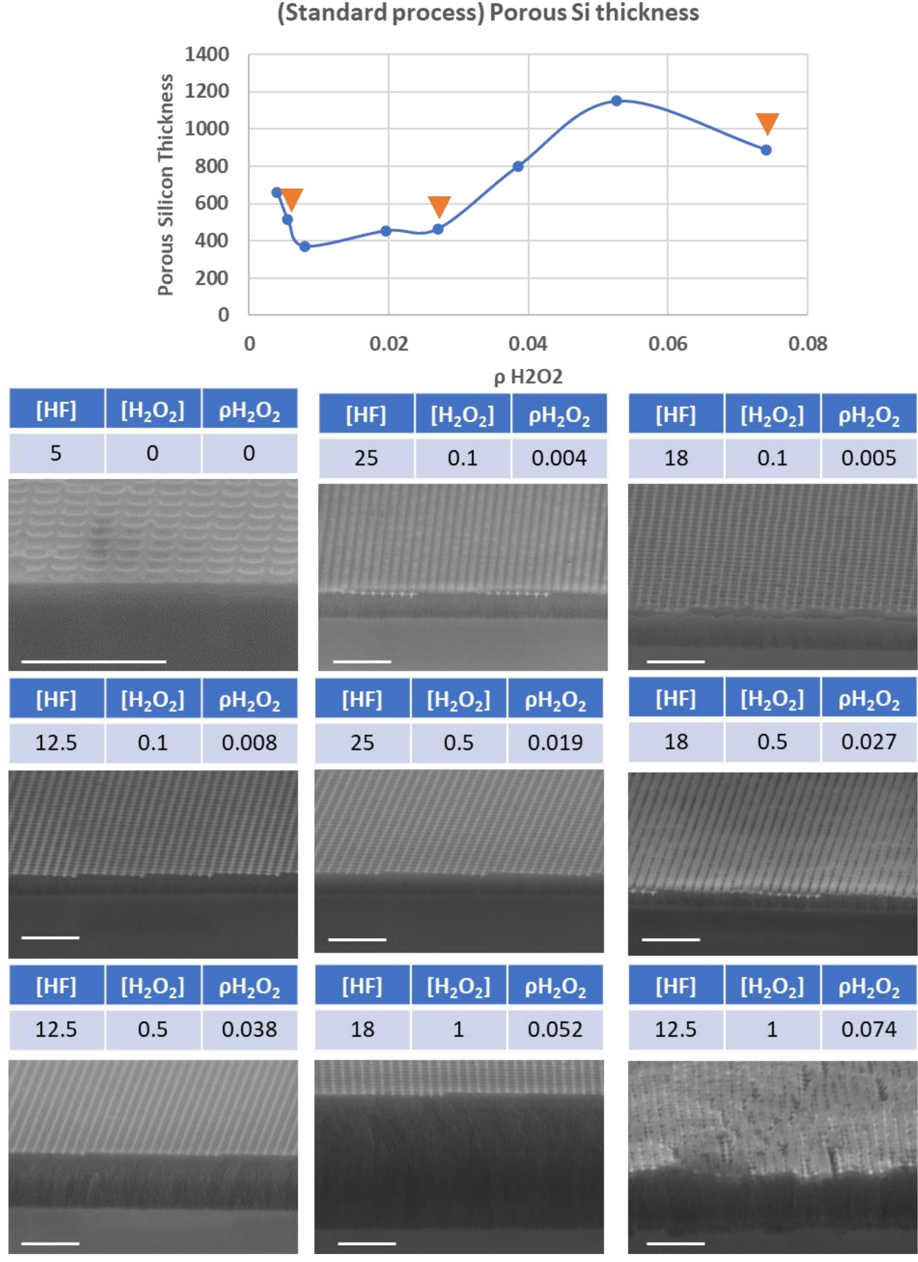


Figure 4.4: Effect of etchant concentration on standard Ru MACE, where all samples are etched for 60s. The plot shows the thickness of porous silicon formed after Ru MACE, and the triangles mark etchant concentrations that show short porous silicon nanowires along with porous silicon. Tilted cross-section SEMs of porous silicon for various etchant concentrations show that Ru MACE creates porosity in silicon. All scale bars are 1µm in length.

Additionally, etch stalling was observed when the etch time was increased – causing an increase in porosity as opposed to increase in porous nanowire height. It is worth noting that some etching occurs for etchants without H_2O_2, possibly due to the oxidizing nature of trace amounts of dissolved oxygen in the HF etchant, which is similar to prior work by Sadakane et al.[158] Other methods of porosity reduction based on Au MACE literature such as reducing the etch temperature also did not show a significant reduction in silicon porosity for Ru MACE (**Figure 4.5**).

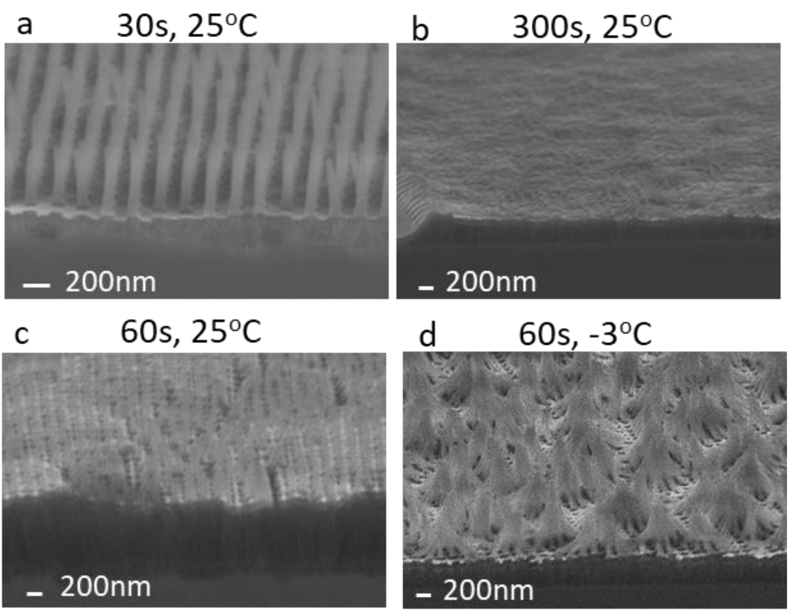


Figure 4.5: Effect of etch time and temperature on Ru MACE quality. All samples are etched in 12.5M HF and 1M H_2O_2

These results point towards the extremely high catalytic activity of Ru compared to Au for MACE, to the extent that the hole generation rates likely overwhelm the capacity of temperature and etchant concentration knobs to attenuate the reaction.

4.2.2. Effect of Silicon Substrate Doping

Ru MACE creates porous silicon layers in the un-patterned regions, as well as on the back of the etched samples – visually seen as colorful areas on the front and back of the samples. Use of electric fields and low temperatures during MACE was tested, but did not reduce porosity of etched NWs appreciably. The cause of this porous silicon can be because of: (i) excess holes diffusing to non-patterned areas from the patterned Ru, or (ii) Dissolution and redeposition of Ru during the MACE process. Additionally, the wafer doping (p-type) can be a cause of porosity. To test these hypotheses, Ru was etched on wafers with different doping type and concentrations. (**Figure 4.6**).

The lack of porosity on the back of the n-type samples, as well as the shape of the porous silicon-induced color on the back of the coupons shows that porosity is due to diffusion of excess holes from the Ru/Si interface, and not from Ru dissolution and redeposition during etch. The average etch rates show dependence on the substrate doping, but all NWs show porosity.

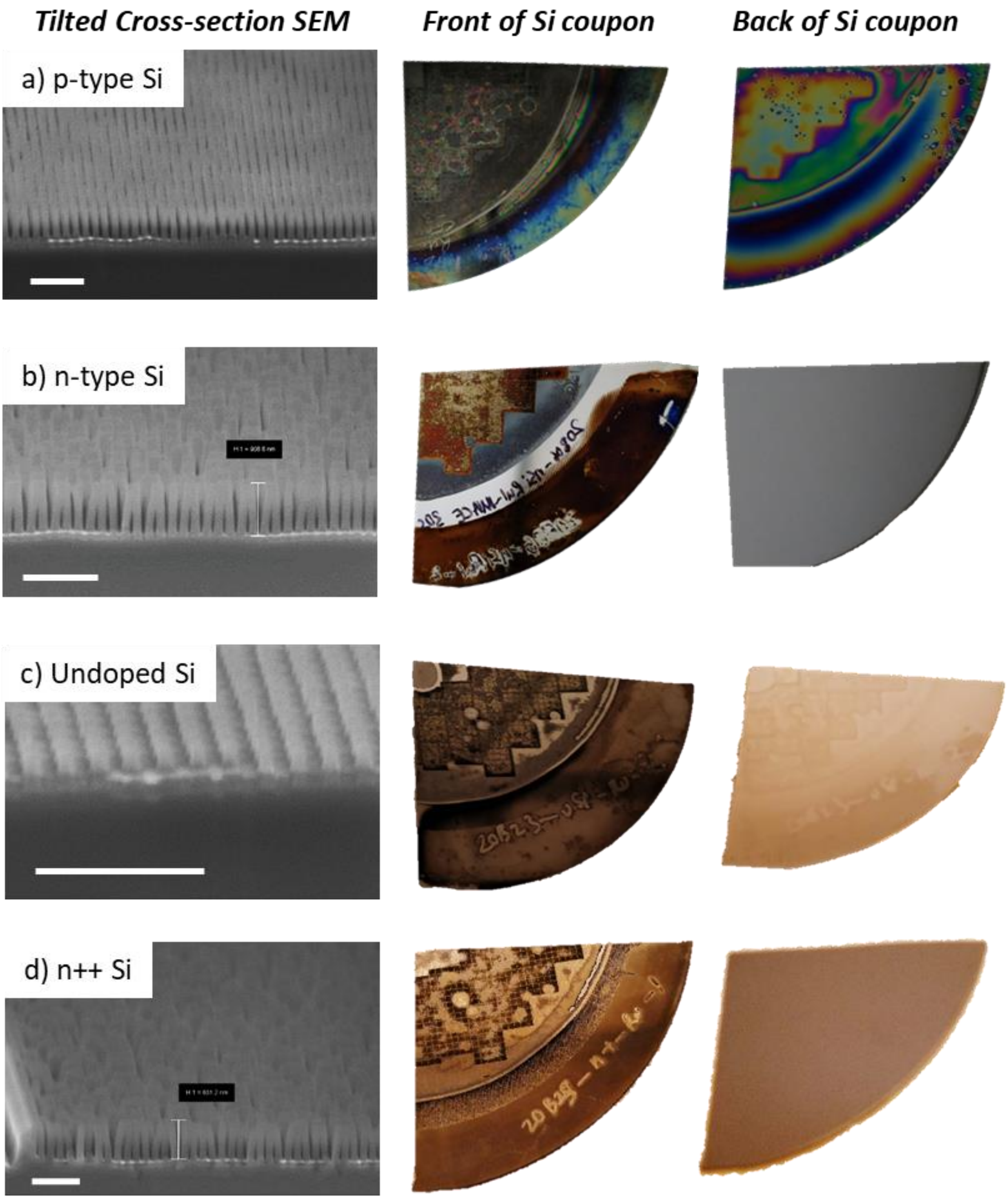


Figure 4.6: Effect of silicon wafer doping on MACE with Ru. All samples are etched for 60s in 12.5M HF and 1M H_2O_2. All scale bars are 1µm in length.

4.2.3. Effect of Ruthenium Surface Area

As discussed above, nanopatterned ruthenium across the entire surface of the silicon samples causes high concentrations of H_2O_2 to get reduced, which results in higher concentrations of holes generated. Reducing the area of Ru could lower hole generation,

and thereby improve the balance between hole transfer into silicon and etchant mass transport. To test this hypothesis, Ru mini-meshes are created using three difference process schemes, resulting in meshes with significant reduction in the Ru surface exposed to H_2O_2 across the wafer.

(A) Photolithography: Removal of Ru in photolithography defined areas after full wafer patterning resulting in 10µm x 10µm Ru mini-mesh areas (**Figure 4.7**)

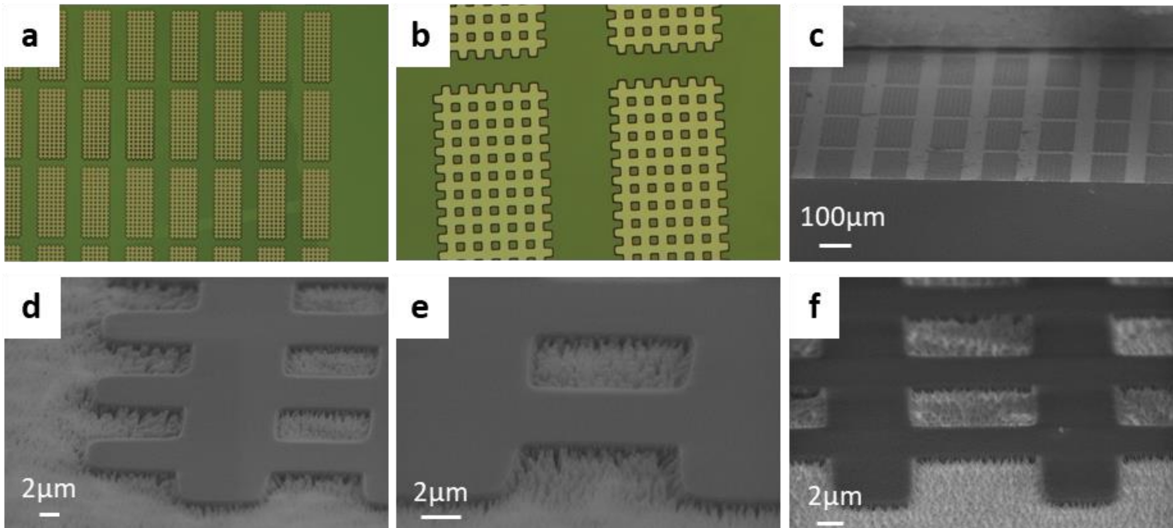


Figure 4.7: Ru mini-mesh patterning using photolithography and MACE (the green areas have Ru nanopatterns): (a, b) optical images, (c) SEM images of Ru mini-mesh, (d, e) Ru MACE for 180s, (f) Ru MACE for 300s

(B) Small-area template for imprint: Replica of imprint template made with photolithography-defined 100um x 100um regions of pattern etched into template (**Figure 4.8**)

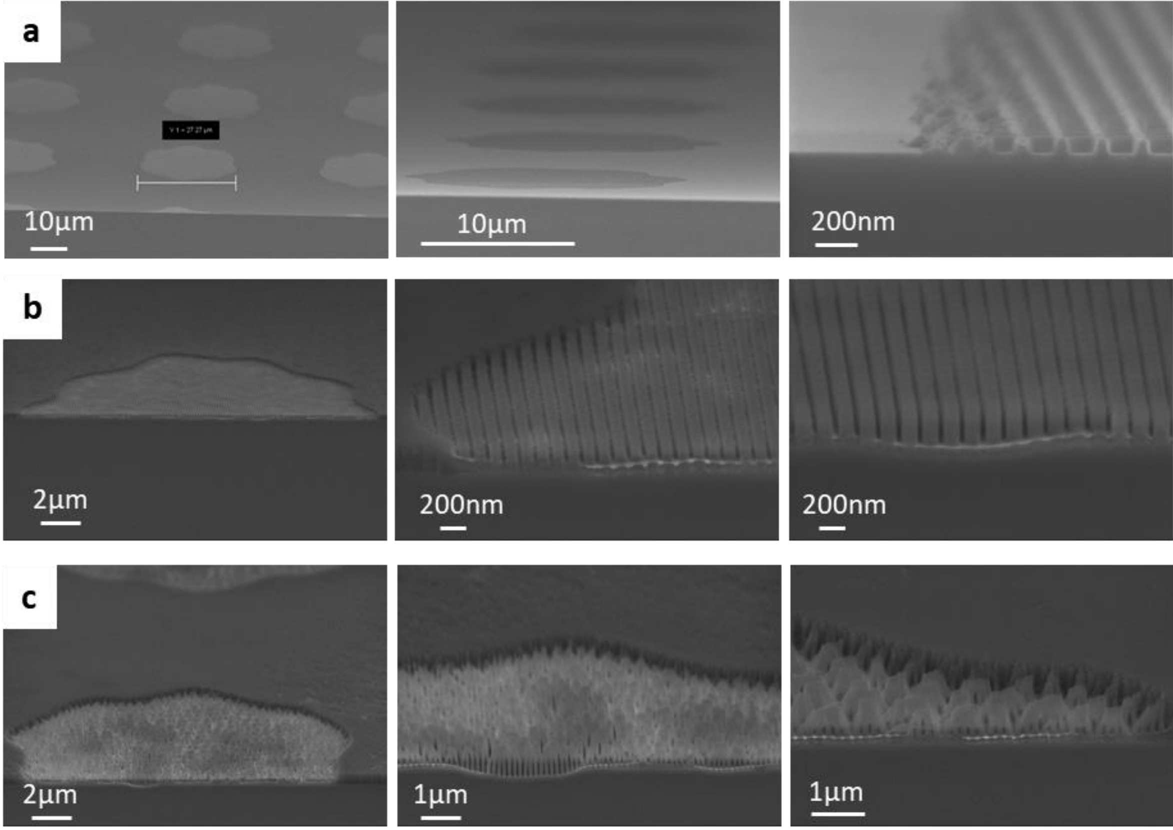


Figure 4.8: Ru mini-mesh patterning using imprint lithography with small area nanopatterns on template, and MACE: (a) Imprinted Resist, (b) Ru MACE for 60s, (c) Ru MACE for 180s

The Ru MACE results for mini-meshes made by photolithography or small area imprint templates are comparable to the baseline wafer-scale meshes. Both these methods create porous Si NWs reliably, but do not show the tall non-porous pillars seen occasionally at pattern edges. Also, increasing the etch time increases the porosity, and does not have as significant an effect on the etch depth. The porous nanopillars collapse at short heights due to reduced stiffness with increased porosity.

(C) Modified imprint with sparse inkjet drops:

Inkjet of sparse imprint drops during J-FIL process is used to prevent full wafer patterning using a modified version of the J-FIL process[74]. In the J-FIL process, an inkjet is used to dispense resist drops on the substrate, and a patterned template is used to transfer

nanopatterns to the resist. In the standard J-FIL process, the density of resist drops is tuned to facilitate merging of drops during imprint to create a contiguous patterned area and uniform residual resist layer thickness (RLT) across the 100mm wafer. For making Ru mini-meshes, the density of resist drops is intentionally lowered to prevent merging of inkjet drops. Modified J-FIL process and resulting resist patterns are shown in **Figure 4.9**.

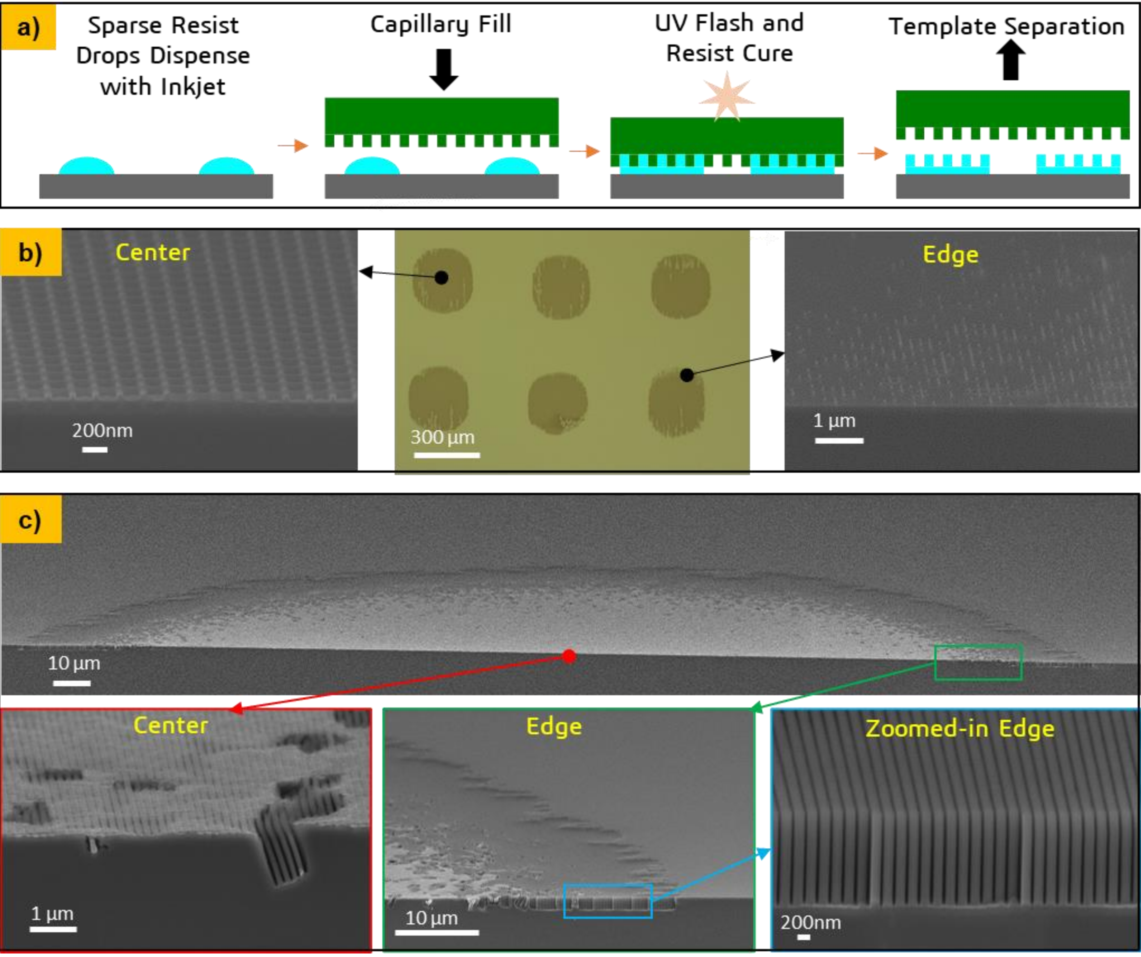


Figure 4.9: Ru mini-mesh patterning using modified Jet and Flash imprint lithography with sparse inkjet drops, and MACE. (a) Modified J-FIL process flow. (b) Tilted cross-section SEM and top-down optical microscope images of resist pattern after sparse drops imprint. (c) MACE of Ru mini-mesh patterns showing tilted cross-section SEMs of a mini-mesh after MACE, where annular regions of mini-mesh patterns show tall non-porous Si NWs, and short porous wires in the center of the mini-meshes. Samples are etched for 20s in 12.5M HF and 1M H_2O_2.

These sparse resist drops result in isolated areas of patterned Ru – resulting in Ru mini-meshes with significant reduction in the Ru surface exposed to H_2O_2 across the wafer. MACE with Ru mini-meshes resulted in short porous nanowires in the middle of the drops, but it resulted in high-quality non-porous high aspect ratio silicon nanowires in the annular regions (Figure 4.9(c)).

This unexpected result was the first time Ru-MACE resulted in patterned nanostructures comparable to Au-MACE. Unpatterned areas outside the mini-meshes had thin porous silicon layers. Repeating experiments of Figure 4.9 on multiple wafers and multiple days show repeatable good annular regions with good Ru MACE results. This is not observed in experiments with Ru patterning using standard J-FIL. The modified J-FIL process has a larger variation in resist residual layer thickness (RLT), with thicker RLT in annular regions compared to thinner regions at the center of the mini-mesh. We hypothesize that the reason for the better annular region etch may be caused by (i) lower exposure to argon/oxygen plasma etch during descum due to thicker RLT at annular regions or (ii) fewer holes (h+) in annular region due to removal of hole-injecting Ru in areas outside the mini-mesh.

Hypothesis (i) was tested first by creating an experiment which has analog variation of argon/oxygen plasma exposure time of the Ru film. This was done by imprinting on a wafer with a particle – resulting in areas closest to the particle to have the largest RLT – thus Ru would have lowest Ar/O_2 plasma exposure, and therefore should have best Ru MACE results closest to the particle. This is what we observe in **Figure 4.10**, and therefore hypothesis (i) is confirmed.

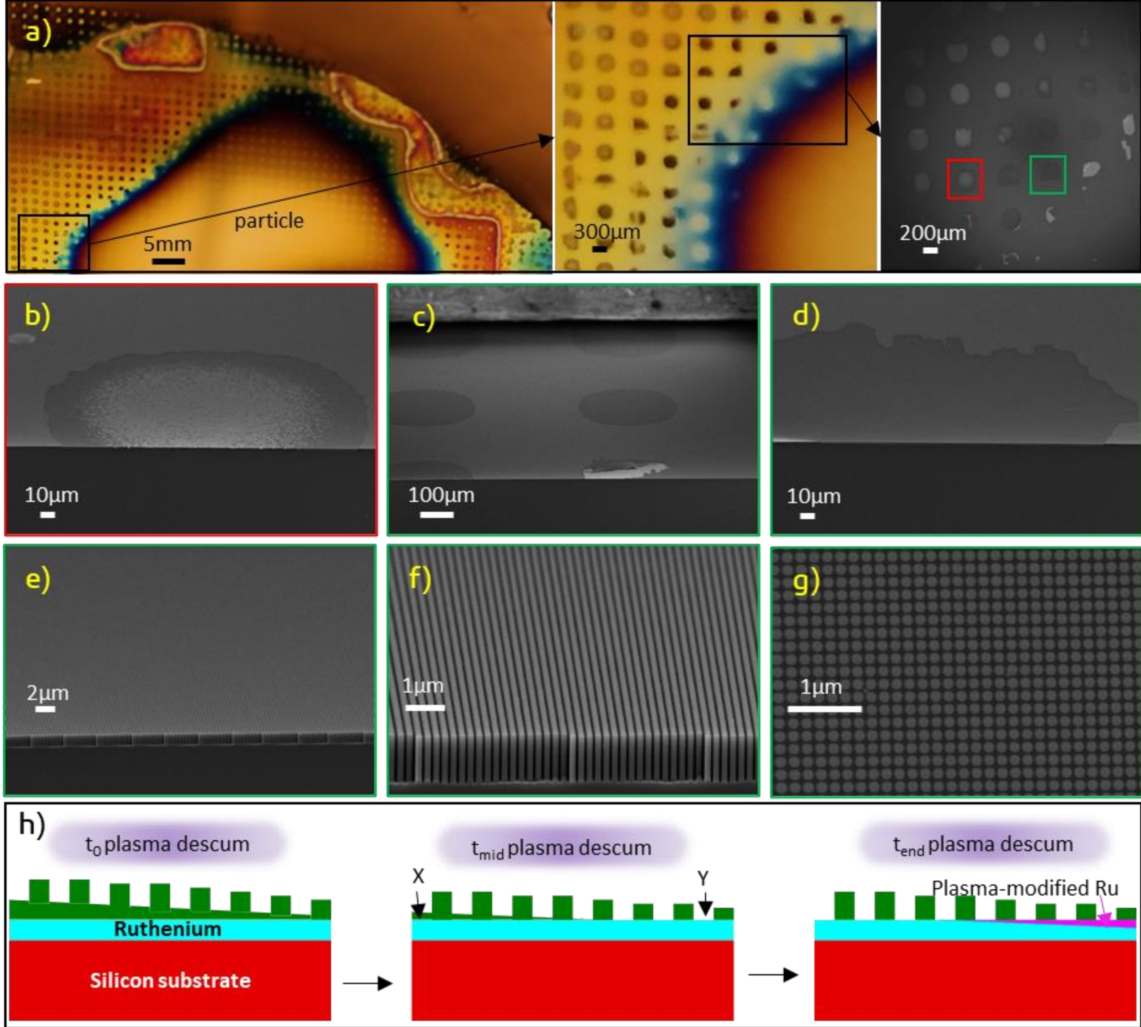


Figure 4.10: Effect of residual layer thickness (higher near particles), and thereby exposure of Ru to oxygen/argon plasma, on Ru MACE: (a) Progressively zoomed in top-down images of sample after Ru MACE, (b) Tilted cross-section SEM of Si NWs in annular region at locations away from particle (marked in red in (a)), (c-f) tilted cross-section SEMs of Si NWs in Ru mini-meshes closer to particle, (g) top-down SEM of Si NWs. (h) Schematic showing longer exposure of Ru in low RLT areas (Y) due to argon/oxygen plasma descum (Step 4 in Figure 2) as opposed to areas with high RLT (X).

4.2.4. Effect of plasma on Ru catalytic activity

To further explore the effects of exposure of the Ru film to Ar/O_2 plasma during the descum step, we try multiple descum etch times (**Figure 4.11**). Increasing the oxygen plasma time results in poor etch. However, the descum step is essential for patterning, and reducing the time too much can result in no patterning of Ru. As it is a timed plasma etch, additional time is typically added (over-etch factor) to ensure that the residual layer thickness is removed across the entire wafer resulting in Ru underneath the RLT being exposed to Ar/O_2 plasma for further pattern transfer.

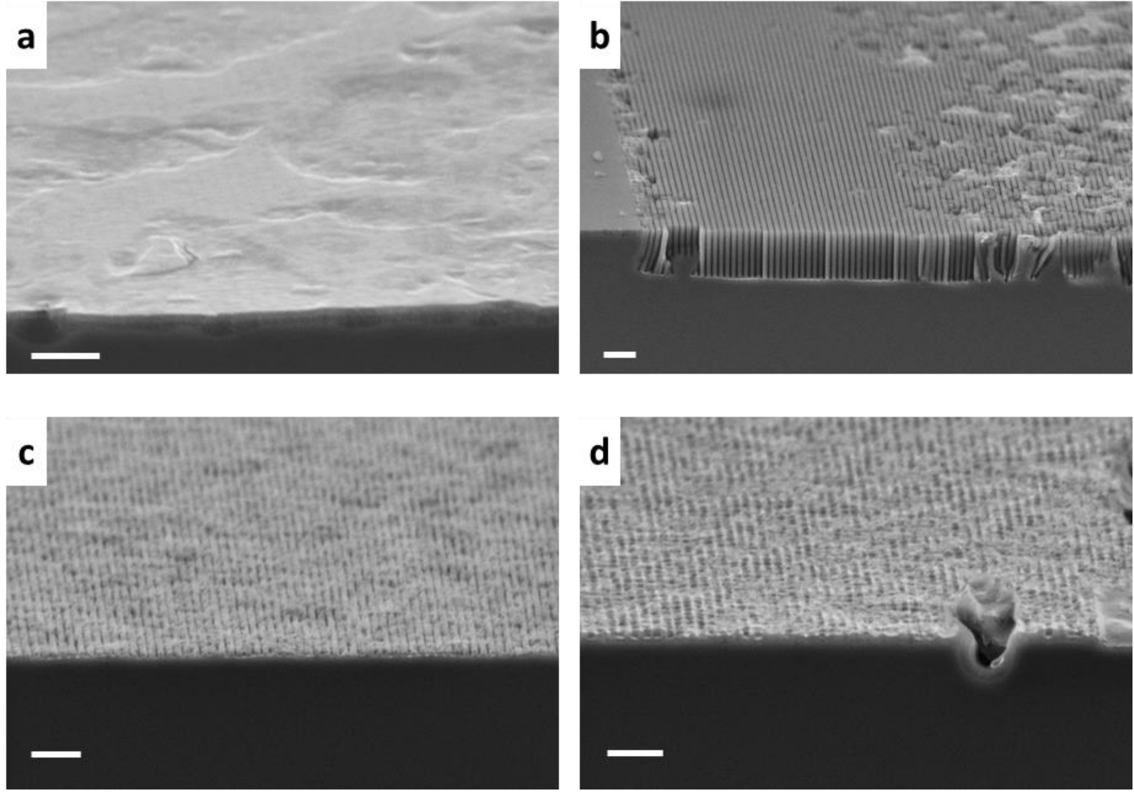


Figure 4.11: Effect of Ar/O_2 descum times on Ru patterning and MACE: (a) 5s, (b) 10s, (c) 20s, (d) 30s. Samples are etched for 20s in 12.5M HF and 1M H2O2. Scale bars are 1 micron in length.

As Ru is deposited using sputter coating in an Ar plasma, the main reason for poor MACE when Ru is exposed to the Ar/O_2 descum recipe is likely due to the oxygen

component of the plasma. This is tested by modifying the descum recipe to contain only argon (for an ion milling-type of resist etch, which may suffer from redeposition), an argon/hydrogen plasma, and an argon/CF_4 plasma. We see a marked dependence of Ru mini-mesh MACE results on the plasma chemistry used **(Figure 4.12)**, with non-oxygen chemistries showing non-porous high aspect ratio SiNWs at both the center and annular regions.

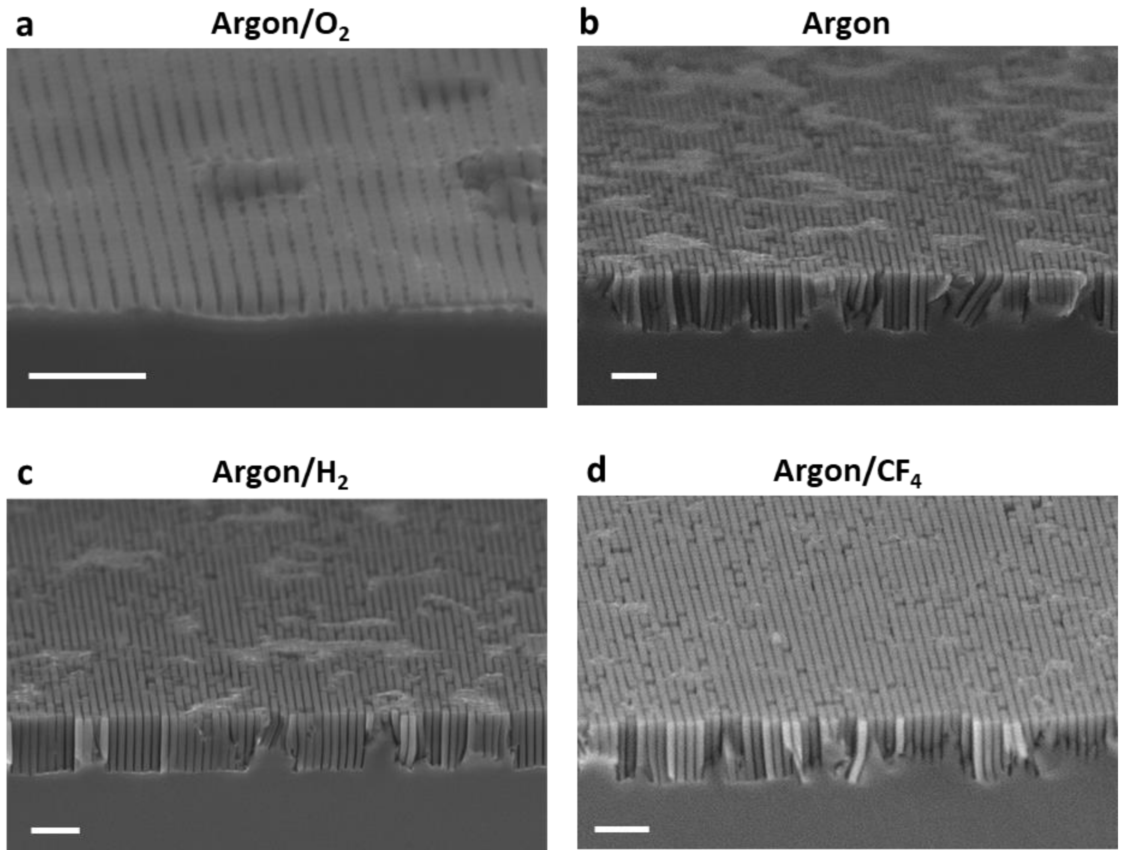


Figure 4.12: Effect of various descum plasma chemistries on Ru mini-mesh MACE. (a) Ar/O_2 plasma descum, (b) Ar plasma descum, (c) Ar/H_2 plasma descum, (d) Ar/CF_4 plasma descum. The descum time is 10s for all shown data points. All samples are etched for 20s in 12.5M HF and 1M H_2O_2. Scale bars are 1 micron in length.

However, the Ru MACE is good in patches surrounded by defects at the mini-mesh centers. This defectivity is highest for Ar plasma, is slightly lower for Ar/H_2 and least for

Ar/CF_4. This is likely due to reduction of the catalytic activity of Ru, as compared to Ar/O_2 plasma, for hole generation. The effect of plasma activation on catalyst behavior has been recently examined by Gao et al.[165] for electrocatalytic reduction of CO_2 using copper nanoparticles, with highest activity achieved for copper nanoparticles treated with O_2 plasma as opposed to untreated, H_2 plasma treated and Ar plasma treated Cu. They found that the plasma chemistry and plasma etch time can be tuned to achieve high catalytic activity and hydrocarbon/alcohol selectivity. This observation can be used to explore *reducing* Ru catalytic activity for MACE, to reduce excess hole generation to eliminate silicon porosity. For Ru MACE, based on the results in Figure 4.12, the catalytic activity is the least for Ru exposed to Ar/CF_4 plasma during descum for 10s.

Increasing the Ar/CF_4 descum time to 30s shows the best Ru MACE results – similar to that obtained by gold – as shown in **Figure 4.13**. Areas outside the mini-meshes have thin porous silicon regions. Increasing the descum time further results in removal of all the imprint resist, resulting in no Ru patterning.

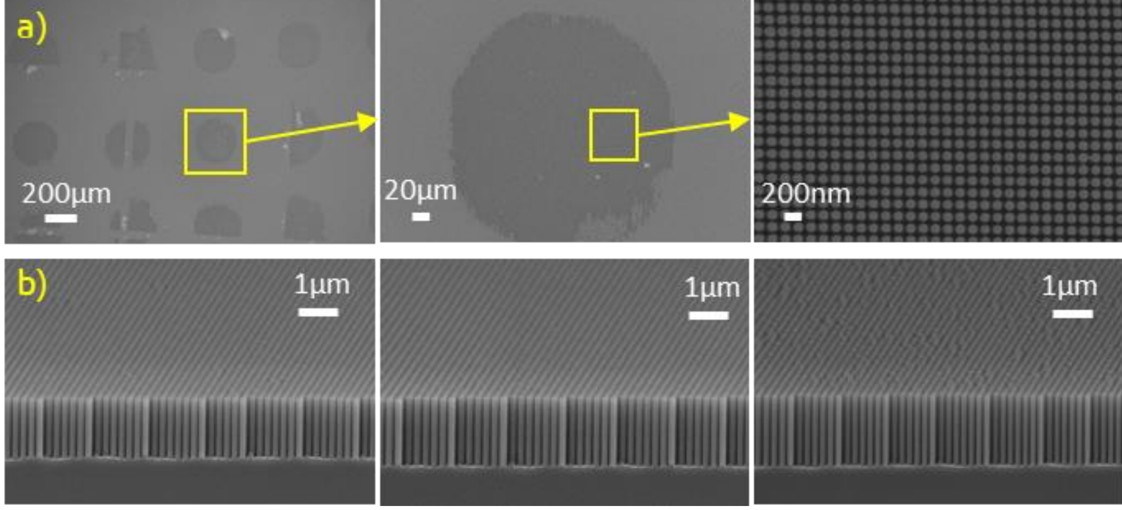


Figure 4.13: Desired MACE results with Ru mini-mesh are obtained using a long (30s) Ar/CF_4 plasma for descum etch (a) Top-down SEM images with progressively higher magnifications showing defect free silicon nanowires, (b) tilted cross-section SEMs at different locations in the mini-meshes showing uniform defect-free Ru MACE

Thus, this Ar/CF_4 descum time of 30s results in all mini-mesh areas having non-porous high aspect ratio defect-free silicon nanowires. Additionally, highly porous silicon is obtained when the Ar/CF_4 descum is used for a process where native oxide is removed before Ru patterning in the Ru MACE process flow. Further, wafer-scale Ru MACE with Ar/CF_4 plasma creates porous SiNWs, demonstrating the importance of both reducing the Ru surface area, as well as using plasma modification of catalytic activity, to achieve desired MACE. With these parameters, porosity-free and taper-free Si NWs are obtained for a range of etchant concentrations, as shown in **Figure 4.14**.

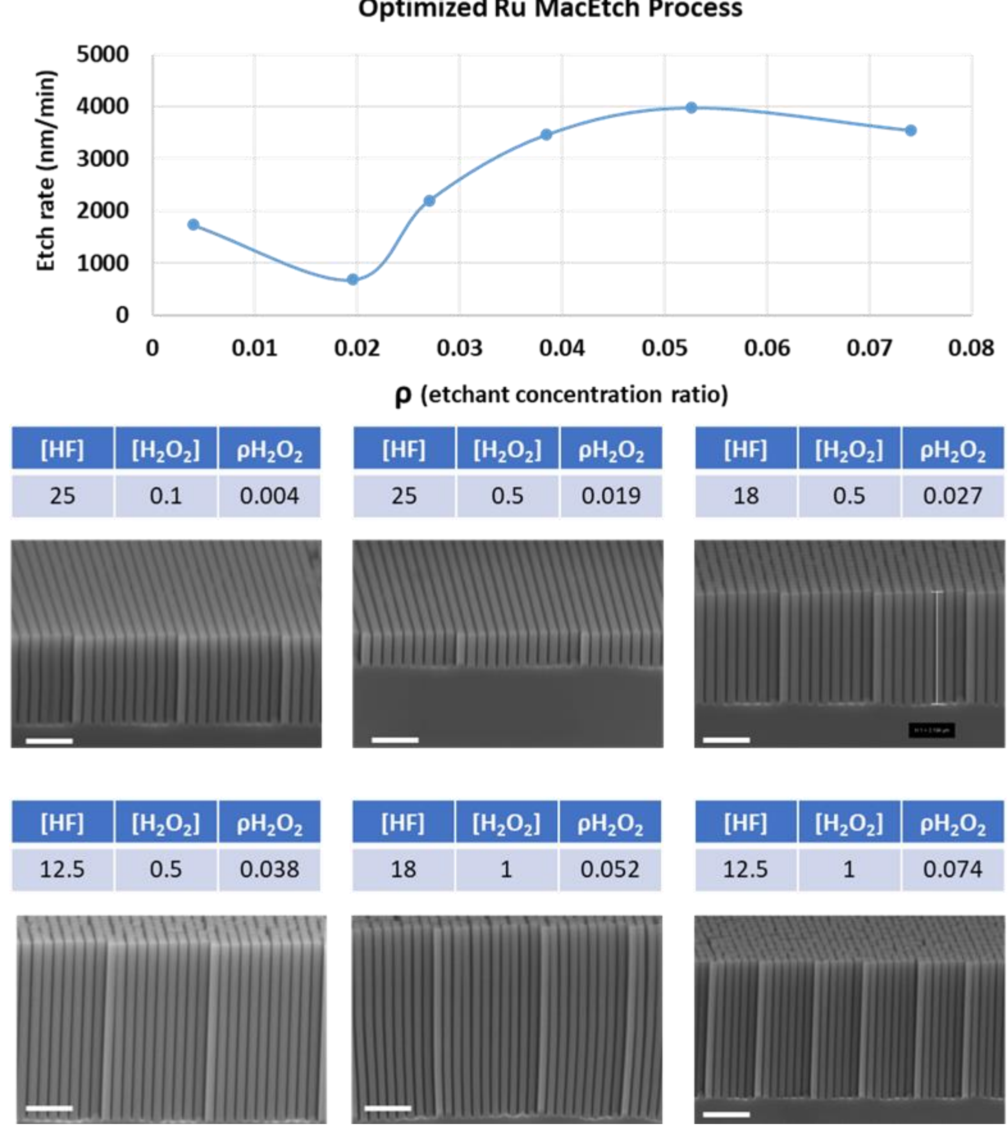


Figure 4.14: Effect of etchant concentration on optimized Ru MACE (using mini-meshes and Ar/CF_4 descum), where all samples are etched for 60s. All scale bars are 1μm in length.

Future research could focus on exploring the effects of plasma chemistry, gas flow rate, power, time etc. to increase the area of Ru mini-meshes to wafer-scale while retaining porosity-free MACE. **Figure 4.15** shows a comparison between the standard Ru MACE process (that uses Ar/O_2 descum and standard J-FIL) and our new optimized Ru MACE process (that uses Ar/CF_4 descum and modified mini-mesh J-FIL) for a range of etchant

concentrations. The optimized Ru MACE process achieves etch rates> 4000nm/min and aspect ratios > 40.

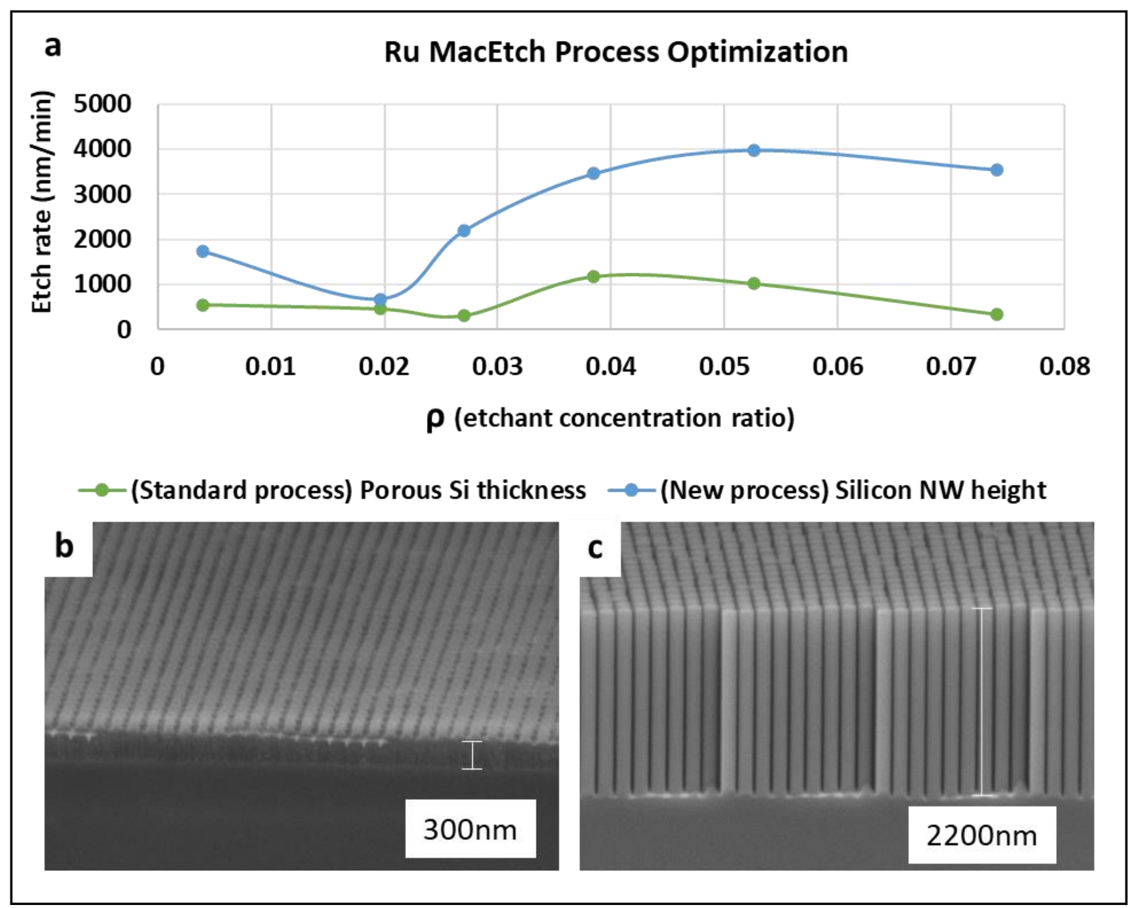


Figure 4.15: Effect of etchant concentration on standard and optimized Ru MACE. (a) plot of etch rate vs etchant concentration ratio ($[H_2O_2]/([HF] + [H_2O_2])$). (b) Exemplar tilted cross-section SEM showing porous silicon layers and porous silicon NWs after standard Ru MACE at ρ=0.028. (c) Exemplar tilted cross-section SEM showing high aspect ratio Si NWs after optimized Ru MACE with mini-meshes and Ar/CF_4 descum at ρ=0.028. Samples are etched for 60s.

4.3. RESULTS AND DISCUSSION

In this chapter, a CMOS-compatible MACE process is demonstrated for creating porosity-free, taper-free, high aspect ratio silicon nanostructures over large areas using Ruthenium Assisted Chemical Etching. To achieve this result, we had to significantly reduce porosity in Ru MACE, and the strategy used to do so involved reducing the catalytic activity of Ru in the MACE cathodic reaction. The resulting optimal Ru MACE process is comprised of the following features:

(i) **Mini-meshes**: Local Ru mini-meshes were used, instead of full coverage of the silicon wafer with patterned Ru, to reduce the area of Ru participating in the cathodic reaction. Standard Ru MACE without mini-meshes has a surface coverage of 1, i.e. the entire silicon wafer is covered by patterned Ru – these samples show porous silicon after etch. Mini-meshes with a spatial density of 0.192 (diameter of 256µm and a pitch of 585µm) show high aspect ratio Si NW etch.

(ii) **Ar/CF_4 plasma**: The plasma chemistry and etch time during the resist descum step plays a critical role in Ru catalytic activity, with enhanced Ru catalytic activity for A/O_2 plasma, and reduced activity for Ar/CF_4 plasma. Exposure of Ru to a long (30s) Ar/CF_4 plasma during resist etch resulted in improved Ru MACE thereby creating non-porous, high aspect ratio anisotropic silicon etch with characteristics comparable to Au MACE.

Table 4.1 shows a comparison of SiNWs made by Au MACE with those made by Ru MACE for selected process modifications described in this work, with respect to characteristics such as porosity, sidewall taper and aspect ratios over large areas. The characteristics (listed in column 1 of this table) have been qualitatively chosen to enable comparison of Ru MACE processes to Au MACE as a benchmark. As can be seen in the

final column, Ru MACE results that are comparable to Au MACE were obtained using the two process features discussed above. The characteristics (listed in column 1 of this table) have been qualitatively chosen to enable comparison of Ru MACE processes to Au MACE as a benchmark. While Ru MACE results in this paper are comparable to Au, further research needed in (i) non-mini-mesh large area Ru patterns, and (ii) elimination of porosity in unpatterned regions, to achieve results fully equivalent to Au.

Table 4.1: Comparison of Au MACE and selected stages of Ru MACE process

	Gold	Preliminary Ru	Ru testing	Optimized Ru
all scale bars are 1 micron				
Process	$\rho[H_2O_2]=0.074$, 30s @ Room T Au MACE[98]	$\rho[H_2O_2]=0.074$, 60s @ -3C Std. Ru MACE	$\rho[H_2O_2]=0.074$, 30s @ Room T Std. Ru MACE	$\rho[H_2O_2]=0.074$, 20s @ Room T Optim. Ru MACE
Porosity in SiNWs	none	high	mid	low (some porosity at the top)
Porosity below SiNWs	none	high	mid	none
Unpatterned region porosity	none	high	mid	low
NW sidewall angle	90 (vertical)	<90 degrees, early collapse	90 (vertical), early collapse	90 (vertical)
Aspect ratio	Ultrahigh possible	Low – highly porous SiNWs etch away	Low – highly porous SiNWs etch away	Ultrahigh possible
Areas with good etch	>50x50 sq. mm	-	-	>5x5 sq. mm

A key challenge in the broad MACE literature outside of Au MACE on low doped silicon appears to be the management of undesirable, extraneous porosity. Much of the literature involving either non-Au catalysts or non-silicon semiconducting substrate materials have shown results that are far inferior to the benchmark results using Au MACE on silicon.[30,31] This work demonstrates a new method of MACE porosity reduction research

includes plasma modification of catalysts. Research on using plasma pretreatment to modify catalytic behavior is in its infancy, and is mainly focused on *increasing* catalytic activity for industrial chemical reactions, such as CO_2 reduction using copper catalysts[165,166]. For instance, Gao *et al.*[165] suggest that O_2 plasma oxidation leads to stabilization of subsurface oxygen species in Cu nanoparticles to improve catalytic performance for CO_2 reduction. However, DFT simulations of this mechanism by other groups show that subsurface oxygen alone does not change Cu catalytic activity.[167,168] While the mechanisms are under debate, Bergmann *et al.*[169] conclude that catalytic function can be tuned by plasma pretreatment. Our work extends the validity of such plasma pretreatments to Ru MACE.

Based on this prior literature, a few hypotheses regarding the observed reduction in the catalytic activity of Ar/CF_4 plasma-treated Ru are presented–

Hypothesis 1: Ru is known to be a p-type metal: the concentration of holes equals that of electrons in Ru, and conduction involves both holes and electrons with higher mobility holes giving rise to the observed p-type behavior.[170–172] This could partly explain the high catalytic activity of Ru in MACE, as it likely transports holes generated during the reduction step at the top surface, towards the silicon surface during MACE more effectively compared to n-type metals (such as Au). The lower catalytic activity of Ar/CF_4 plasma pretreated Ru may be due to one or more components of the CF_4 plasma acting as a dopant that reduces the hole transportation rate for Ru.

Hypothesis 2: A core-shell structure of Ru and RuO_2 is a highly effective catalyst, at least for CO oxidation.[173] It is possible that in an oxygen plasma, such a core-shell structure forms in Ru, and increases the catalytic activity of Ru for MACE as well.

Hypothesis 3: Defect engineering is a known method of changing the conduction behavior, band gap, surface adsorption behavior and electrocatalytic behavior of electrocatalysts such

as metals, metal oxides and 2D materials [174–176]. Such defects can be created by plasma treatment.[177] It is possible that this works in conjunction with a doping-based electronic mechanism (Hypothesis 1). This would explain the limited but noticeable effect of Ar and H_2, which likely only act through this defect-based physical mechanism. For CF_4 plasmas, both a dopant-based electronic mechanism and a defect-based mechanism could together act to curtail the activity of Ru. Induced defects could also affect the Si/Ru band bending (which are important in MACE mechanisms[46,178]), induce internal stresses or lead to local suppression of electric fields.

More experimental and theoretical work is required to develop an understanding of the effect of plasma chemistries on catalytic behavior, especially in the context of *reducing* catalytic activity for Ru MACE.

Chapter 5: Enabling Enhanced 3D CMOS Device Performance and Scaling using MACE

An exemplar application in 3D CMOS logic devices is used as a motivation to demonstrate the versatility of this process and the promise of MACE as a next generation etch technology. The 3D geometries of transistors used in the semiconductor industry have challenges such as the stability of the structures coupled with the lithography and etch related fabrication challenges, which leads to significant challenges in scaling below 10nm half-pitch structures. High aspect ratio structures that can enable tall fins and/or increased number of stacked nanosheets and nanowires can improve the performance of logic devices and enable scaling for many future nodes, for instance, by decreasing the number of fins required per transistor.

The previous chapters lay a foundation for translation of MACE from a lab-scale etch method to industry-grade semiconductor fabs by demonstrating solutions to MACE process challenges using circular cross-section silicon nanowire arrays. This chapter[**] broadens the capabilities of MACE beyond circular nanowires to arbitrary nanopatterns and establishes a pathway for MACE-specific Design for Manufacturing. Further, the capabilities of MACE in creating nanostructure superlattices by controlling silicon porosity during etch is explored.

[**] The work in this chapter partly overlaps with the following article[139] –
A. Mallavarapu, P. Ajay, C. Barrera, S.V. Sreenivasan. "Ruthenium Assisted Chemical Etching of Silicon – Enabling CMOS-Compatible 3D Semiconductor Device Nanofabrication", *Accepted, ACS Applied Materials and Interfaces*, 2020.
Akhila Mallavarapu designed and performed the experiments, characterized and analyzed the data, and wrote the final paper.

5.1. MOTIVATION

For about five decades, Moore's Law consistently delivered computing devices with improved performance, lower power consumption and enhanced functionality, enabled by primarily by innovations in lithographic scaling, along with complementary developments in etch, deposition, materials development, and process integration.[7] This 2D scaling trend has however slowed in recent years due to major challenges in sub-10nm manufacturing technologies. These scaling challenges coincide with a relentless demand for enhanced performance in logic and memory, creating a need for breakthroughs that are outside the normal trends in semiconductor manufacturing.

In recent years, 2D scaling has been overcome, to some extent, by 3D device geometries. For instance, as feature sizes reduced from 10 microns in 1950s to 10nm today, the transistor geometry changed from 2D planar FETs to 3D finFETs to retain transistor performance while reducing its footprint. However, this has led to unique challenges in deep etching of nanoscale geometries, exposing basic limits of plasma etching such as etch taper, sidewall damage, and aspect ratio dependent etching, which limits creation of small and deep features. **Figure 5.1** shows cross-sectional SEM images of fins used for transistors today, showing a marked etch taper.

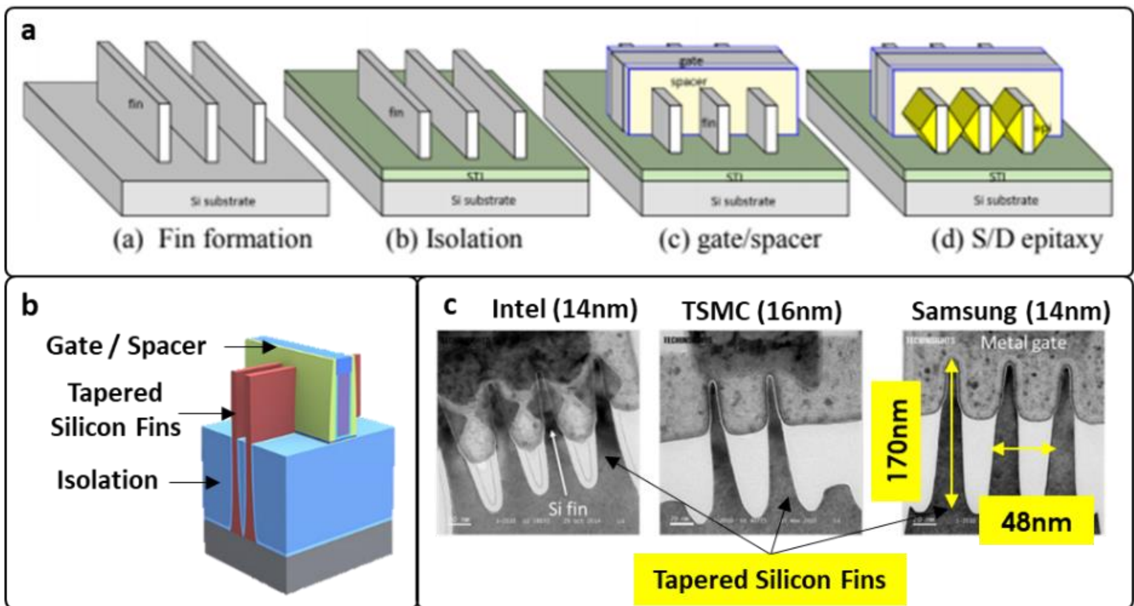


Figure 5.1: Silicon fin etch taper in FinFETs (a) FinFET fabrication process flow,[141] (b) FinFET schematic showing tapered silicon fins (Source: Lam Research[179]), (c) Cross-section SEM images of FinFETs in 14nm-16nm technology nodes showing tapered silicon fins made by plasma etch (Source: TechInsights[27])

The etch taper angle creates further challenges as it limits the maximum height of the fin at a certain fin width. To increase the height of the fin, the width of the fin has to be increased, which reduces the transistor packing density. Due to this limitation, high performance transistors use multiple fins as opposed to increasing the height of a fin to increase the transistor surface area. MACE does not suffer from the same limitations as plasma etch and can enable taller fins, thereby improving the performance of chips and decreasing transistor footprint. **Figure 5.2** shows an exemplar I/O transistor in Apple A9 processor that requires 14 fins. MACE with taller fins can enable a significant reduction in transistor footprint as fewer taller fins have the same surface area as many short fins.

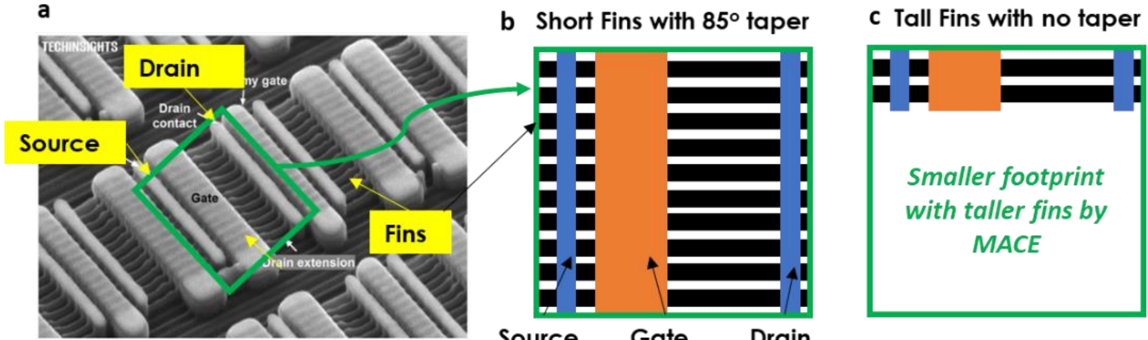


Figure 5.2: Elimination of etch taper can enable large area savings and increased transistor packing. (a) Top-down SEM image of TSMC 16nm finFET I/O Transistors in Apple A9 Processor (Source: TechInsights[27]), (b) Top-down schematic of fin arrangement for plasma-etched short, tapered fins, (c) Fewer taller fins made by MACE enable smaller footprint transistors

The process of making tall, thin silicon fins with minimal sidewall damage, no collapse and no etch taper has been challenging as the dimensions reduced to sub-20nm. For sub-10nm nodes, new 3D transistor architectures such as nanosheet FETs, nanowire FETs, and complementary FETs are being explored. These devices also require high aspect ratio plasma etch.

Nanosheet FETs (**Figure 5.3**) have horizontally stacked gate-all-around structures that can be a good replacement of FinFETs at the 5nm technology node and beyond. They enable versatile designs and show higher performance and electrostatics than FinFETs for the same footprint. Greater number of nanosheet layers can further improve the performance of the transistors. Nanosheet FETs are made by etching fins that have alternating layers of Si/SiGe ("nanostructure superlattices") and subsequently removing the SiGe layers, resulting in suspended nanosheets. Nanosheet FETs have better electrostatics than finFETs due to their gate-all-around configuration as opposed to finFET's trigate structure. Similar to the height limitations of fins discussed in the previous section, the critical height of the alternating layers of semiconductor in the nanosheet fins limits the number of layers that can be etched. This limitation is not present in the MACE process.

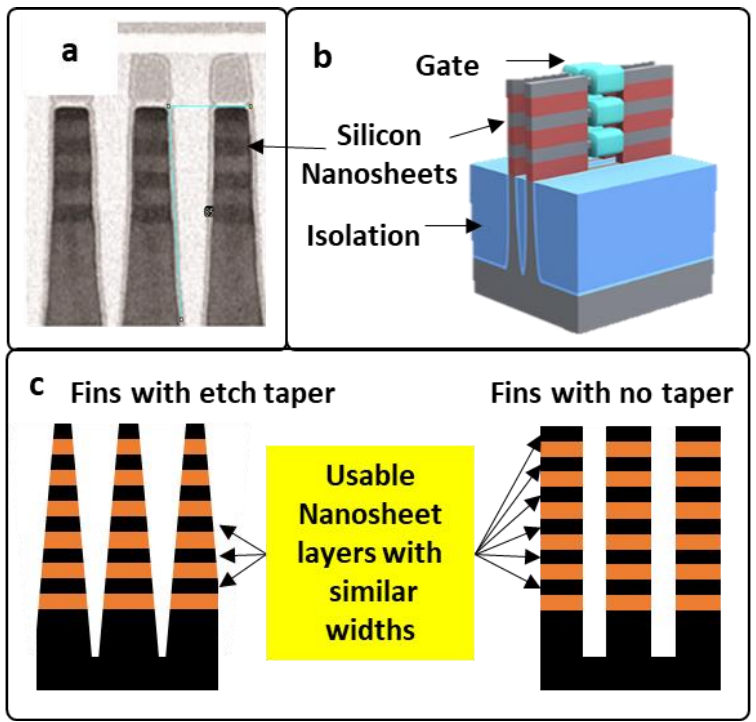


Figure 5.3: Nanosheet FETs: (a) SEM of 5nm nanosheet fins[28], (b) Schematic of nanosheet FETs (Source: Lam Research[179]), (c) Effect of etch taper angle on maximum possible nanosheet layers

Complementary FETs[180] are multi-tier transistors that have been proposed as a method to further increase scaling by stacking transistors on top of each other. This requires ultra-high aspect ratio fins whose lengths depend on the number of stacked transistors, as shown in the schematics in **Figure 5.4**. Extrapolating from Ref. [181], it can be estimated that 200nm tall fins of 10nm width are required for a 2-stacked CFET – which is beyond the limits of plasma etch due to etch taper limitations, but can be made by MACE.

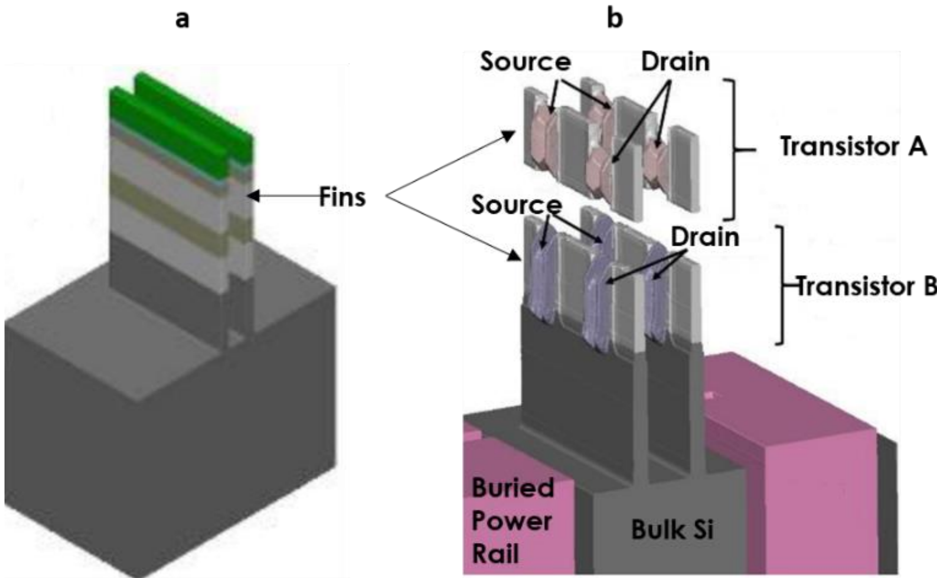


Figure 5.4: Complementary FETs with 2 stacked transistors (A and B): (a) Schematic of vertical Si/SiGe fins required for CFET fabrication, (b) Schematic of CFET with 2 stacked transistors. Reproduced from Vincent *et al.*[181]

Such stacked transistor architectures can also enable high density stacked SRAM devices to increase on-chip memory. SRAM stores memory using 6 transistors per bit and occupies ~70% of computing chips. Stacking these transistors, or stacking multiple SRAM cells can dramatically improve on-chip memory or reduce footprint to enable ultra-fast computing applications in CPUs and GPUs.

Apart from transistors, other devices that require ultrahigh aspect ratio etch include DRAM[29,142] and 3D NAND Flash. DRAM cells comprise of 1 transistor and 1 capacitor, and use stack or trench capacitors to increase capacitance per cell without compromising on device footprint. However, this method has limitations of high aspect ratio etch of holes for trench capacitors, and feature stability for stack capacitors. Also, decreasing feature sizes affect the reliability of planar and recessed channel or fin-based DRAM transistors. **Figure 5.5** shows a schematic of DRAM cells and high aspect ratio trench capacitors.

Increasing the aspect ratio of trench capacitors can enable scaling of DRAM cells while maintaining the minimum capacitance required.

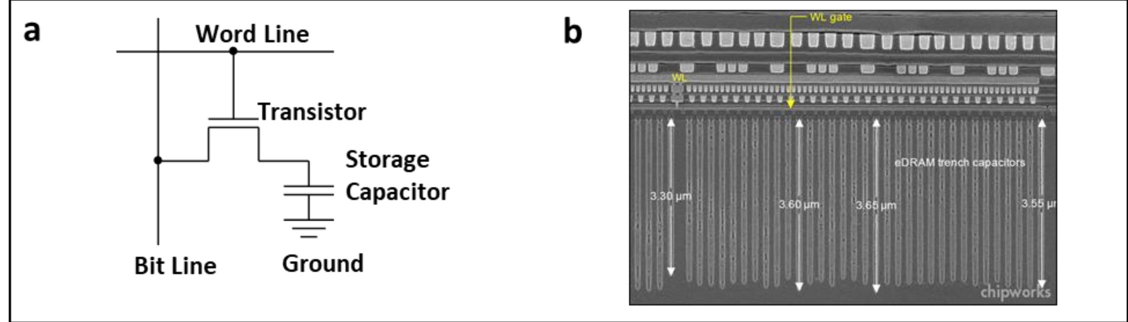


Figure 5.5: DRAM with trench capacitors. (a) Schematic of 1T-1C DRAM bit-cell, (b) Cross-section SEM of a DRAM device with trench capacitors (Source: Chipworks[182])

Thus, the ability to fabricate ultra-high aspect ratio silicon nanostructures and silicon superlattice nanostructures with no etch taper can enable future generation high performance computing devices at smaller footprints, and MACE has the ability to achieve these requirements. This chapter broadens the capabilities of MACE beyond circular nanowires described in the previous chapters, to arbitrary nanopatterns, thereby establishing a pathway for MACE-specific Design for Manufacturing. Further, the capabilities of MACE in creating nanostructure superlattices by controlling silicon porosity during etch is explored.

5.2. METHODS

High-aspect ratio rectangular silicon fins made by plasma etch are used in transistor fabrication as shown in Figure 5.1(a). Due to the nature of plasma etching, the fin sidewalls are tapered creating a trapezoidal prism structure as opposed to a rectangular cuboid. This taper limits the ability to shrink the fin width and fin pitch while maintaining or increasing fin height. For instance, FinFETs in the "14nm" technology node have a taper angle of ~85°, and a physical Half Pitch (HP) of 24nm and pitch of 48nm. Using this ratio of technology node to physical half pitch, the maximum fin height possible for different taper angles is plotted in **Figure 5.6**, where the critical height is calculated by $\text{Maximum fin height} = 0.5 * \text{HP} * \tan(\text{TaperAngle})$. 100nm of the fin height is used for Shallow Trench Isolation (STI) and is thus not a part of the active finFETs.

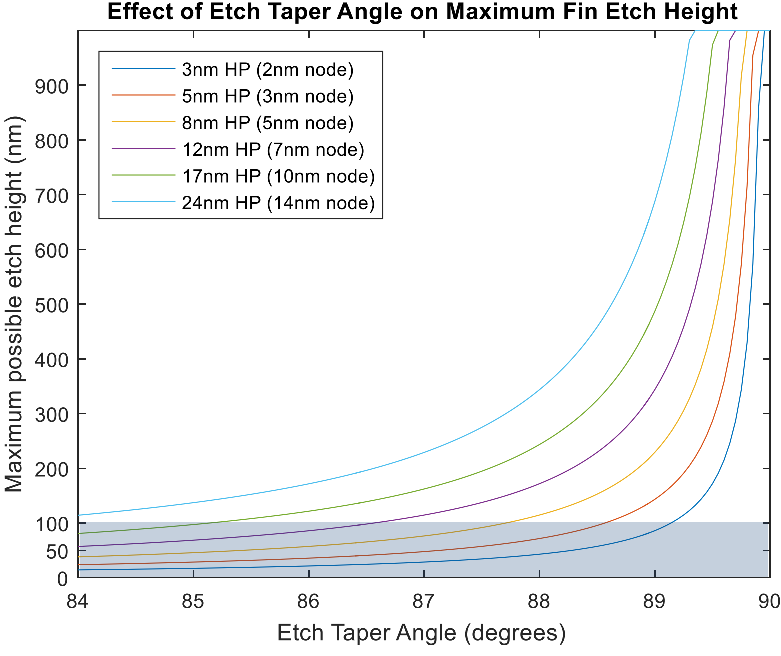


Figure 5.6: Effect of etch taper angle on maximum achievable fin height for different technology nodes. No etch taper (90° taper angle) allows for fins with arbitrarily tall heights.

This plot thus shows the scaling potential of a vertical taper-free etch like MACE to increase aspect ratios of fins. Fabrication of rectangular fins by CMOS-compatible Ru MACE, as well as methods of ultra-high aspect ratio fin collapse management are described below.

5.2.1. Silicon nanofins by MACE

Optimized CMOS-compatible Ru mini-mesh MACE described in Chapter 4 can be extended to application-specific geometries such as rectangular nanofins for transistors. This is demonstrated for rectangular cross-sections pillars, where, similar to results obtained for circular nanopillars, mini-meshes and catalyst plasma modification are required to achieve desired non-porous silicon etch with Ru MACE. The effect of Ru surface coverage is critical, as shown in **Figure 5.7**. [139]

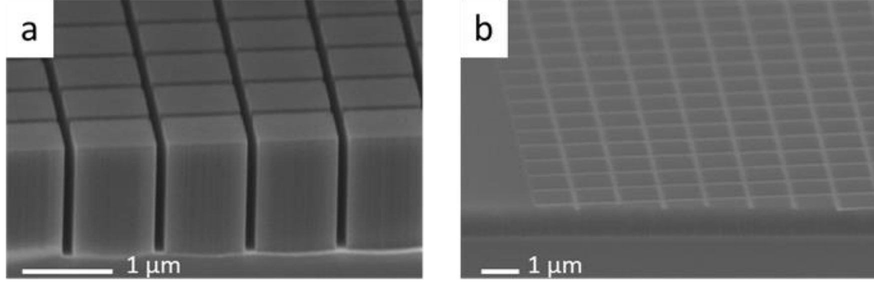


Figure 5.7: Effect of mini-mesh spatial density of Ru MACE etch quality for Ar/CF_4 descum and 20s MacEtch with 12.5M HF and 1M H_2O_2. (a) spatial density of 0.192, (b) spatial density of 0.264. Standard Ru patterns have a spatial density of 1, i.e. the entire silicon surface is covered by patterned Ru.

For Ru MACE on samples processed with Ar/CF_4 descum, increase in Ru surface coverage (or mini-mesh spatial density) causes porosity in features etched. Standard Ru MACE without mini-meshes has a surface coverage of 1, i.e. the entire silicon wafer is covered by patterned Ru – these samples show porous silicon after etch. Mini-meshes with a spatial density of 0.192 (diameter of 256µm and a pitch of 585µm) show

high aspect ratio nanostructure etch, while those with a spatial density of 0.264 (diameter of 256μm and a pitch of 507μm) show porous silicon. The pitch is varied by changing the inkjet drop pattern during Jet and Flash Imprint Lithography.

Regular arrays of silicon fins with different rectangular cross-sections are etched to determine the effect of fin geometries on Ru MACE etch rates. A high level of etch uniformity across fin geometries is obtained, as shown in **Figure 5.8**.

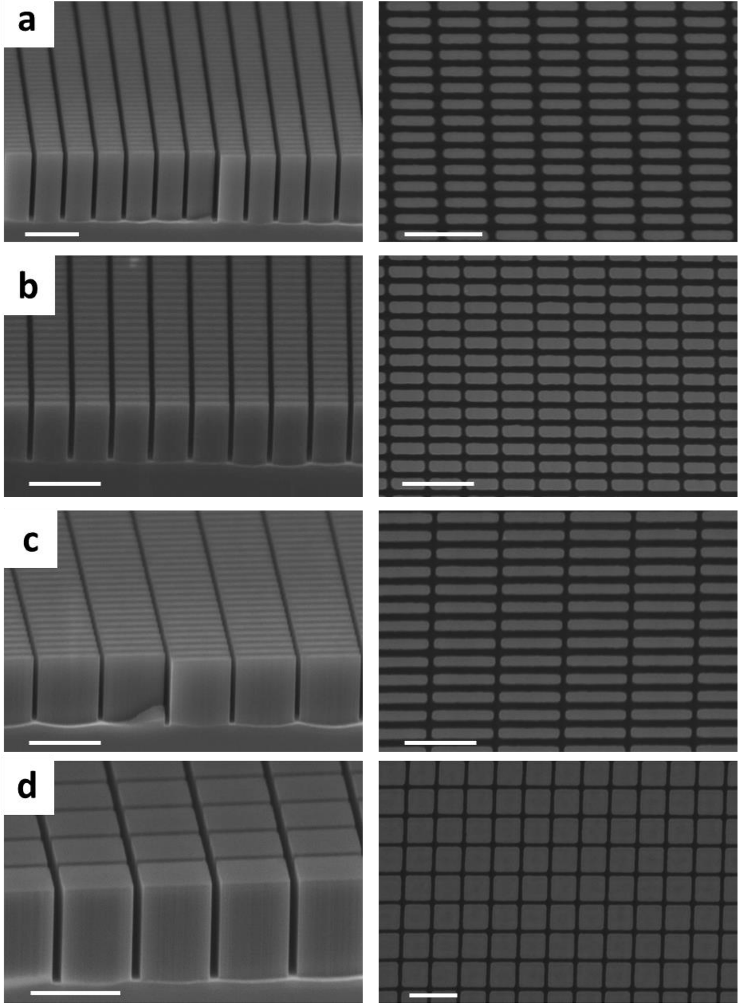


Figure 5.8: Ruthenium MACE for fabrication of silicon rectangular pillar arrays with different geometries. All samples are etched using optimized Ru MACE (Ar/CF_4 descum and 20s MacEtch with 12.5M HF and 1M H_2O_2.) All scale bars are 1μm in length.

While Ru MACE can enable ultra-high aspect ratio fins for transistors, a major limitation to scaling to smaller fin widths is their structural instability. For FinFETs made with bulk silicon, a major portion of their length is utilized for shallow trench isolation (STI). Assuming the minimum height required for STI is 100nm, only fins of width 10nm and above can be used. Further, the active portion of the fins are much shorter than the initial fin height. **Figure 5.9** shows the maximum achievable fin heights for a given half pitch using the lateral collapse models described in Glassmaker *et al.*[116], with the structural parameters for rectangular fins. This is calculated by equating the bending energy of the fin due to collapse with the surface energy required to separate the fins.

$$h_{cr_lengthwise} = (\frac{18EI_x w^2}{\gamma_{sv}\, b})^{1/4} \quad (6.1a)$$

$$h_{cr_widthwise} = (\frac{18EI_y w^2}{\gamma_{sv}\, a})^{1/4} \quad (6.1b)$$

where E is the elastic modulus of the fin, I is the moment of inertia about the bending axis, w is the deflection of the fin, i.e. half the distance between the collapsing fins, γ_{sv} is the surface energy of the fin material, and a and b are the lengths of the fin perpendicular to the direction of collapse. For nanosheet layers comprising Si and SiGe, the new critical height depends on the modified elastic modulus of the multilayer stacked fins. Considering the thickness of each nanosheet to be 5nm, and the lower region of the fin that is covered by STI to be Si, the new elastic modulus can be calculated by the "slab" model using the inverse rule of mixtures in composites literature. For a volume fraction of Si ~ 75%-95%, the resulting effective elastic modulus is ~ 100-150GPa, and the critical heights for nanosheet fins are similar to those of finFET fins.

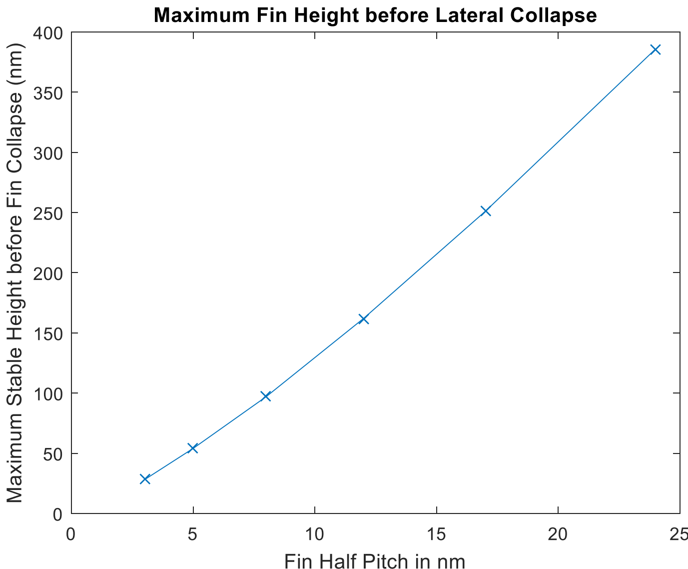


Figure 5.9: Maximum height of a fin with no taper before lateral collapse along the length of the fin (50nm in this case), as a function of the fin half-pitch (or fin width)

Methods of improving the structural stability of fins beyond the heights in Figure 5.9 include:

(1) use of repelling "caps" described in Chapter 3

Chapter 3 demonstrated circular nanowires that had much taller critical collapse heights than predicted by known theoretical collapse models due to "repelling caps". An electrostatics model was added to known lateral collapse models to account for this anomalous behavior. However, the electrostatics models used in Chapter 3 do not translate to rectangular geometries, as a critical component of the model for circular nanowires – local deformation of circular cross-section NWs at the contact location – is not present for rectangular fins. Further experimental and theoretical work for non-circular silicon nanostructures is required to determine the use of repelling caps for arbitrary geometries.

(2) use of stabilizing structures to avoid fin collapse

An alternate process flow for fin fabrication that avoids collapse is by using connecting links, as described in Chang and Sakdinawat[20], between fins to stabilize the fins during etch. After further processing of the device – including deposition of material between the fins - the stabilizing structures can be removed. For instance, fins connected on both ends

create rectangular holes that would not collapse. MACE of holes, however, require isolated catalyst features which tend to wander during MACE and cause defects, as described in the next section.

5.2.2. Silicon nanoholes by MACE

During the MACE process, isolated metal catalysts may wander and create non-vertical undesired etch paths. Discontinuous catalyst features tend to wander during the MACE process and cause defects. Hildreth *et al.*[57] utilized this property to make 3D spiral microscale structures with gold as a catalyst, and calculated the effect of the catalyst stiffness and geometric constraints on its motion. MACE of rectangular holes with isolated rectangular catalysts wander due to van der Waals forces on the catalyst as well as stochastic variations in forces applied due to local etchant concentration or etch rate variations. **Figure 5.10** shows the effects of catalyst material and geometry on catalyst wandering behavior, with lower wandering for ruthenium compared to gold catalyst materials and larger catalyst sizes. Catalyst wandering with gold is larger than ruthenium, likely due to lower bending and torsional stiffness of Au, shown below.

	Young's modulus	Shear modulus
Gold	76-81 GPa	26-30 GPa
Ruthenium	424-450 GPa	168-182 GPa

As shown in Figure 5.10, wandering of isolated catalyst structures causes poor MACE of holes. Catalyst wandering can be reduced by modifying the etchant concentrations and optimizing the recipe, however, as the size of holes to be etched is reduced, catalyst wandering increases (Figure 5.10(c)). Kim *et al.*[164] demonstrate etch of 200nm-400nm diameter holes with Au MACE, but observe etch stalling and low etch rates for smaller 100nm geometries.

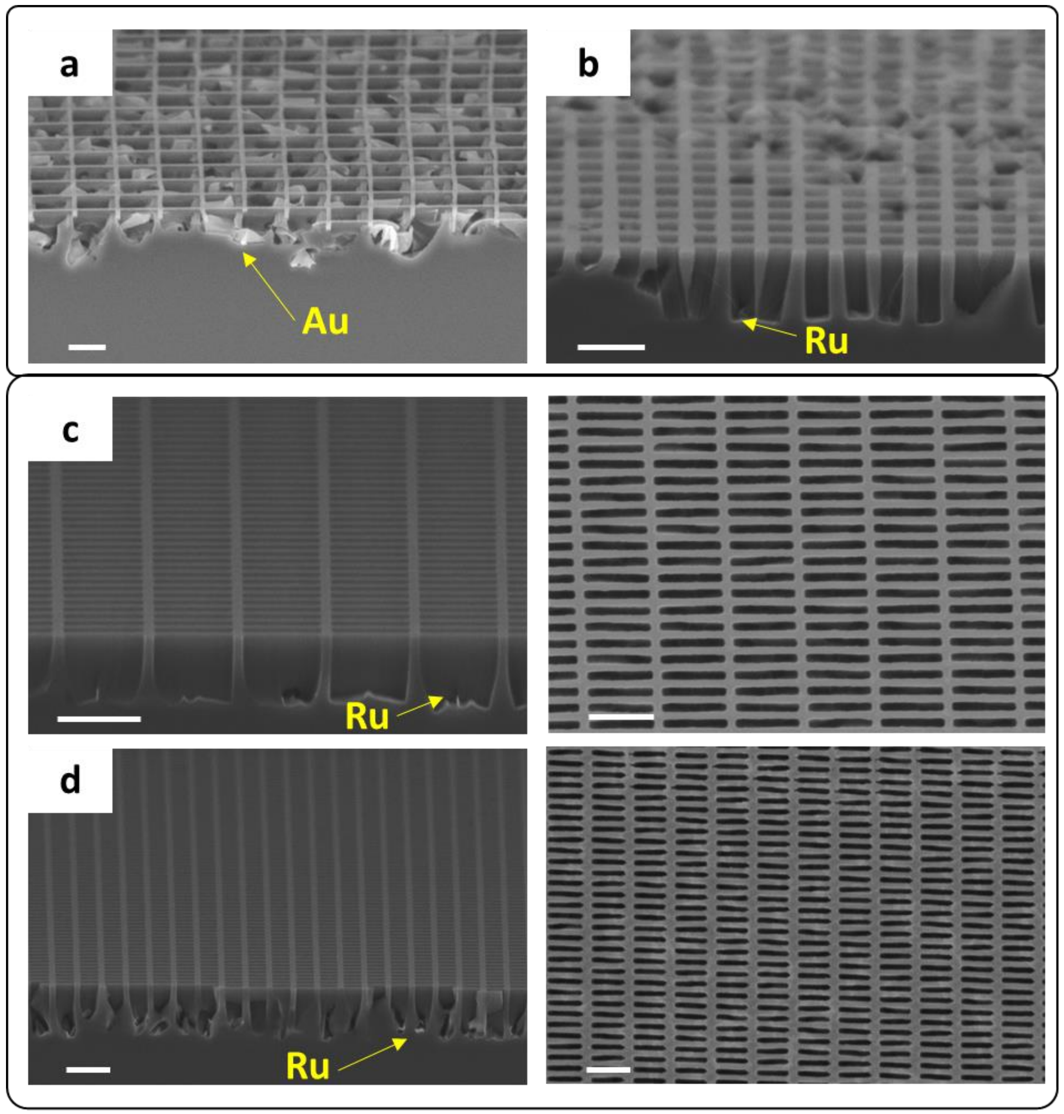


Figure 5.10: Effect of catalyst material and geometry on wandering of holes during MACE, (a-b) Au and Ru MACE of rectangular holes, (c-d) Effect of catalyst geometry on wandering for Ru MACE of rectangular holes

For CMOS applications such as ultrahigh aspect ratio DRAM capacitors, the typical cell size is <50nm. An alternate approach to making deep holes for DRAM is presented here, which combines the atomic precision of feature dimension and overlay of lithography, vertical etch of MACE, and atomic layer deposition. Fabrication of fins with

defined DRAM-cell-like geometries is followed by ALD to fill desired gaps, thereby enabling deep holes. (**Figure 5.11**)

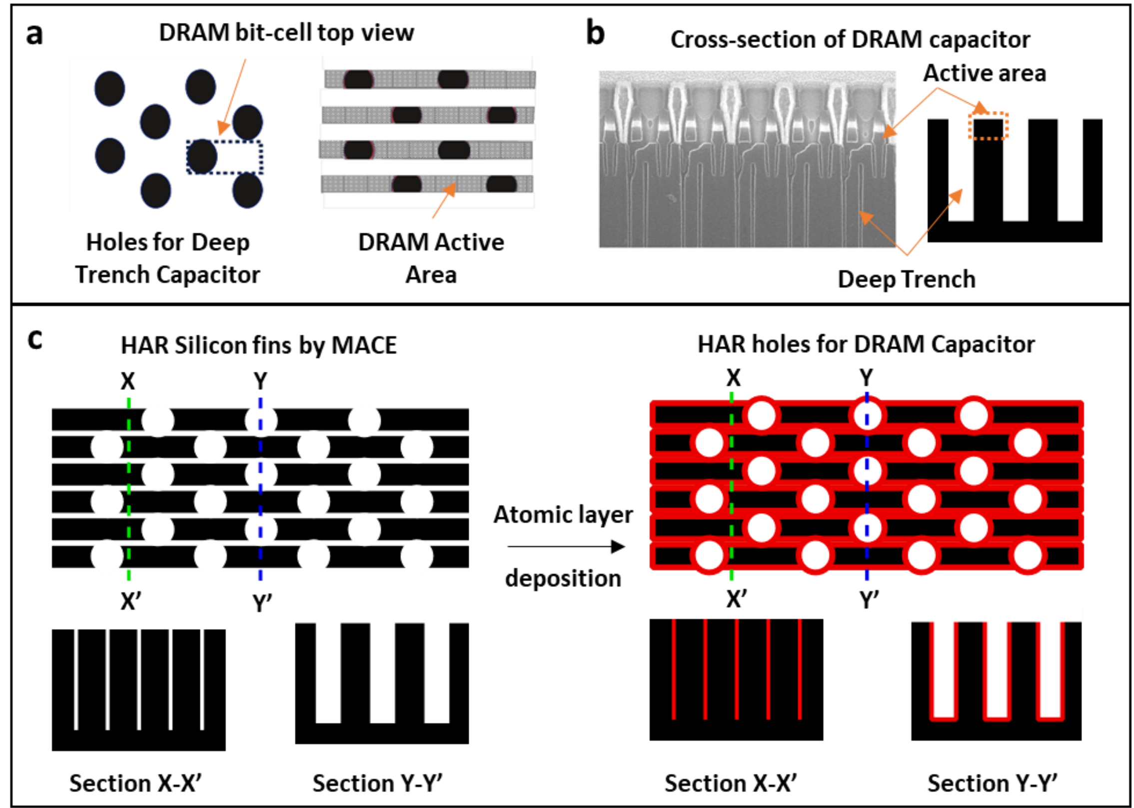


Figure 5.11: High aspect ratio holes for DRAM deep trench capacitors using MACE + ALD. (a, b) DRAM cells design and SEM showing capacitor placement. Reproduced from Tran *et al.*[183] (c) MACE + ALD process flow showing fin geometries made by MACE and high aspect ratio holes made by filling designed gaps with ALD.

The MACE+ALD methodology of fabricating fins with precise geometries and placement, combined with conformal material deposition, can enable new design rules for 3D device design with arbitrary geometries. Additionally, design specifications do not need to be constrained to regular periodic geometries shown above. For instance, typical transistor architectures have fins of multiple dimensions and/or spacing determined by the desired circuit design. Arbitrary varying geometric patterns with rectangular fins are etched

to confirm etch uniformity and independence of etch rates from aspect ratios for Ru MACE. **Figure 5.12** confirms etch uniformity for fin-like geometries beyond regular arrays for Ru MACE, thereby providing freedom of MACE geometry design in applications in logic, memory, optic and photonic devices.[139]

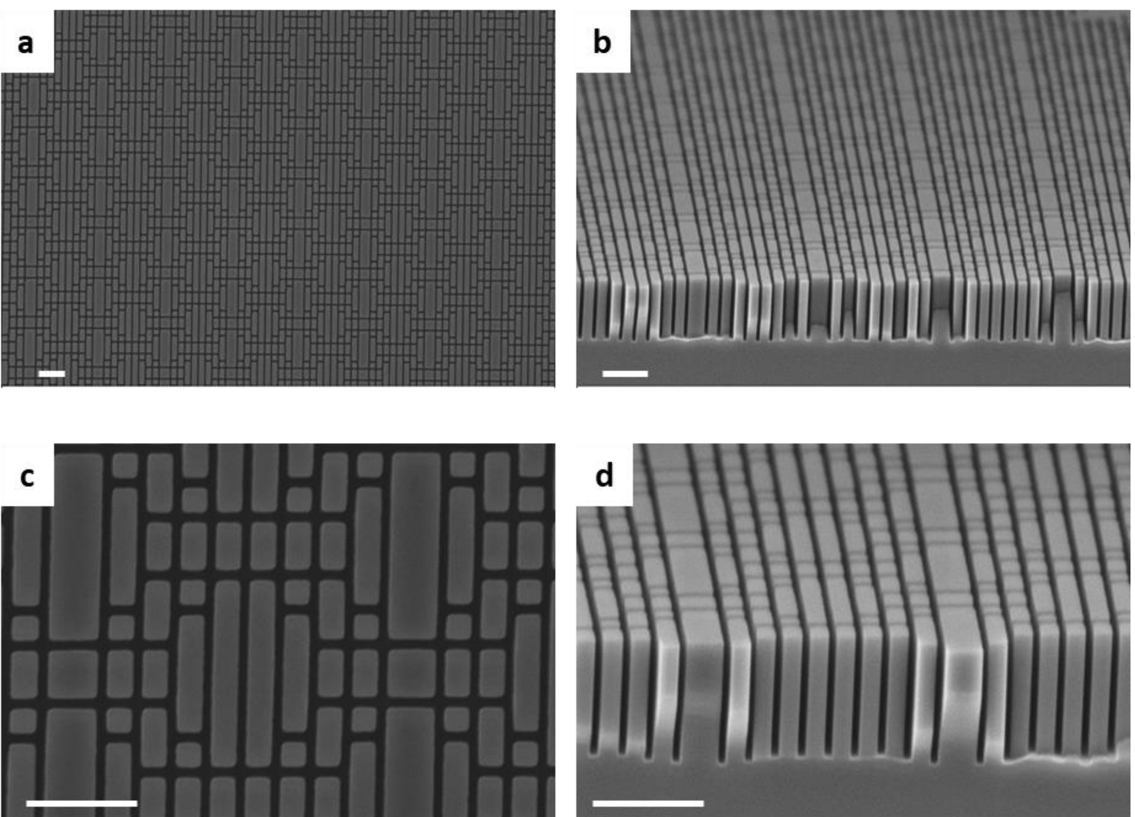


Figure 5.12: Ruthenium MACE for fabrication of silicon rectangular pillars with different geometries (a-d) tilted cross-section SEMs and top-down SEMs at different magnifications. All scale bars are 1 μm in length.

The porosity in features after optimized etch is characterized using TEM and EDS mapping (**Figure 5.13**), which shows ~15nm thick sidewall porosity at the top of the features, and no porosity at the bottom of the features.[139] HRTEM and EDS show that the porous silicon at the top of the features is oxidized, and the oxidized porous silicon is amorphous while the rest of the silicon fins are crystalline. The cause of this porosity may

be due to diffusion of holes from the Ru/Si interface to the tops and sidewalls of the nanofins, as well as prolonged exposure of the top parts of the fins in the etching solution[163].

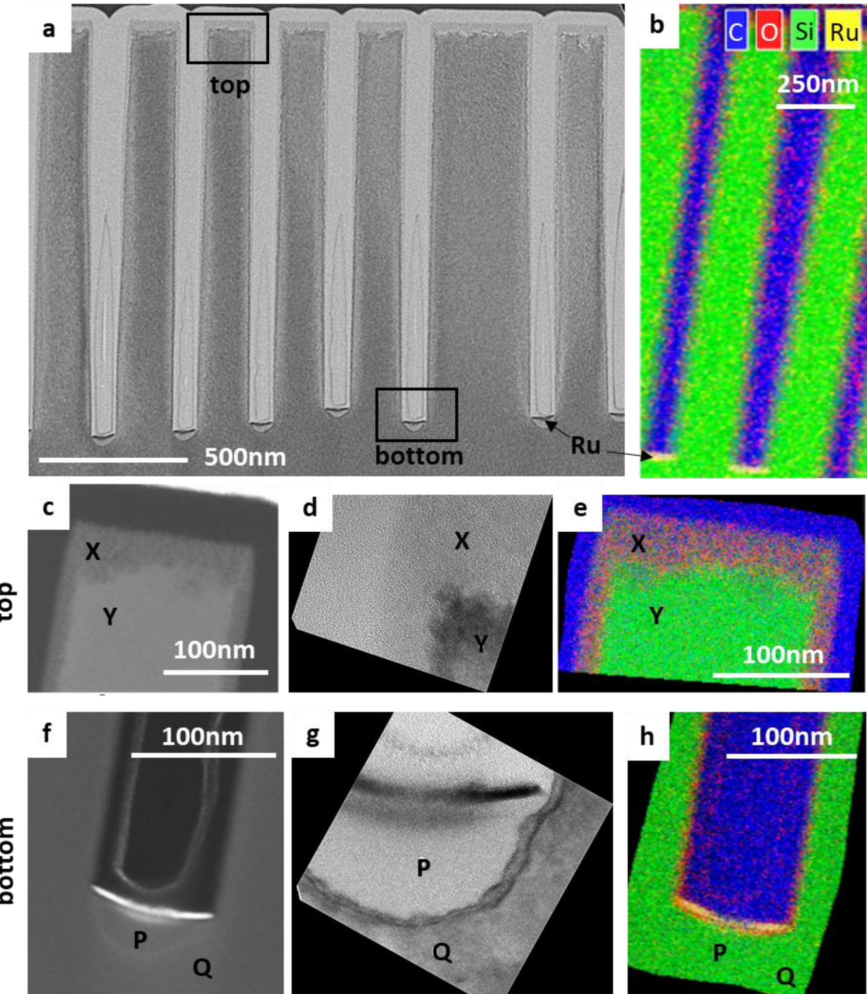


Figure 5.13: High resolution TEM and EDS mapping of silicon fins shown in Figure 5.12. (a) TEM, (b) EDS mapping of silicon fins along the fin length. Top portion of the fins shown by (c) cross-section SEM, (d) HRTEM, and (e) EDS mapping shows ~15nm sidewall porosity and oxidation (X) as opposed to the rest of the silicon fins (Y). Bottom portion of the fins the shown by (f) cross-section SEM, (g) HRTEM, (h) EDS mapping shows Ru catalyst and etch front. The etch front (P) shows amorphous silicon, and the surrounding silicon (Q) is crystalline.

The images also show the MACE front below the Ru catalyst at the bottom of the fins – amorphous Si is observed at the etch front locally underneath the silicon. It should be noted that the amorphous silicon is not oxidized, thereby suggesting that the mechanism of the anodic Si dissolution reaction proceeds by direct dissolution of silicon, as opposed to via silicon oxide formation followed by dissolution.[31] The silicon underneath the etch front in likely amorphous as opposed to porous crystalline Si, as no clusters of crystalline structures are seen in the HR-TEM, unlike other work on TEMs of MACE porous Si NWs[163].

5.2.3. Silicon superlattice nanostructures by MACE

Transistor and memory architectures with ultra-high aspect ratio nanostructures can thus be made using CMOS-compatible MACE. As described in the motivation section, silicon fins are used in FinFETs, while fins made of alternating Si/SiGe are used for nanosheet FETs and complementary FETs. Si/SiGe layers deposited using epitaxial growth are plasma etched to create tapered fins for nanosheet FETs and CFETs. MACE can create fins without etch taper, and MACE of SiGe[184] and Si/Ge[185] superlattices has been demonstrated in literature for sub-20nm nanowires. Alternatively, such superlattices can be made with bulk silicon by utilizing morphology control during MACE. The morphology of silicon nanostructures includes the porosity, pore size, pore orientation, and any variations in porosity along the length of the nanostructures. MACE can be used to tune the porosity as the catalyst etches into the silicon by taking advantage of the electrochemical nature of the etch. Silicon superlattice etching uses the catalyst to etch silicon while simultaneously creating a superlattice with alternating layers where one of the layers is porous. Similar to selective removal of SiGe layers in Si/SiGe superlattice fins

in nanosheet FET fabrication, porous silicon layers can be selectively removed in non-porous Si/porous Si superlattice fins made MACE.

The alternating layers can be formed by electric field parameter modulation, etching through layers with alternating doping characteristics, or by alternating the MACE etchant concentrations. Higher current density, higher doping concentration, and higher oxidant-to-HF ratios respectively increase silicon porosity. Weisse *et al.*[186] and Chiappini *et al.*[63] demonstrated alternating porous silicon superlattice nanostructures using electric fields and etchant concentration modulations, as shown in **Figure 5.14.** Electric fields, however, do not produce non-porous layers, and result in superlattices with layers having alternating porosities. Alternating etchant concentrations can produce non-porous/porous layers, but is a timed etch and requires constant change of etchants, reducing yield and throughput.

Studies have demonstrated the effects of silicon substrate doping concentration on resulting porosity after MACE, with heavily doped wafers producing highly porous silicon, and lightly doped wafers producing non-porous silicon nanostructures[63,163,187]. Multilayers with varying doping concentrations separated by Ge barrier layers have also demonstrated doping level-dependent porosity[65]. The Ge barrier layers are used to prevent dopant diffusion, but result in increased cost of deposition and loss of throughput due to switching of gases during epitaxial growth of the films. This section builds on previous literature and demonstrates a process for making porous silicon superlattices with sharp non-porous/porous silicon interfaces in nanostructures without the use of barrier layers between differently doped films.

Silicon Superlattice Etch

a
Alternating Current Densities *j*

b
Alternating Etchant Concentrations

c
Alternating Si Doping Layers

Etchant Conc. A

Etchant Conc. B

Etchant Conc. A

Etchant Conc. B

High Aspect Ratio Nanostructures with Silicon superlattices having alternating porosities

a. Electric Fields

Porosity-modulated Si nanowires

Weisse et al. (2013)

b. Etchant Conc.

Chiappini et al. (2013)

c. Si doping

Layer A porous film

Vertical sidewalls across interface

Layer B no porosity

200 nm

This work

Figure 5.14: Methods of forming porous silicon superlattice fins using silicon superlattice etch (with Au MACE) with porosity modulation by (a) electric fields[186], (b) etchant concentrations[63], (c) substrate doping layers, showing sharp porous-to-non-porous layer transition for epitaxially growth silicon on bulk silicon.

MACE can etch into silicon while simultaneously changing the morphology depending on tailorable material properties such as doping concentration and dopant type of deposited alternating layers. The method employed for deposition of the alternating layers or "superlattice" depends on commercial availability, cost, throughput, growth rate, thermal budget, number of layers and thicknesses of layers. Polycrystalline silicon layers can also be used, but they may not have reliable vertical MACE due to grain boundaries, and they tend to reduce the size of the structures being etched.[62] Epitaxial (epi) growth of silicon produces crystalline silicon films using Chemical Vapor Deposition (CVD), a process whereby a thin solid film is synthesized from the gaseous phase by a chemical reaction.

Temperature, pressure, gas flow rates, substrate preparation, surface treatment and oxidation prevention are the main parameters that determine the epi superlattice quality and crystallinity. The partial pressure of the gas used for doping, such as B_2H_6 or PH_3, determines the doping concentration in the epi layer. A low total pressure during growth allows for better junctions due to decreased contamination from gases of the previous layer – however, this is not a concern when growing alternating epitaxial silicon films of the same doping type and different doping concentrations.

When epitaxial layers with alternate high and low doping concentrations are deposited at sub-micron thickness per layer, the concentration gradient across the interface of the two layers is shallow due to limitations of the deposition process at high deposition rates, as well as due to diffusion of dopants across the interface. This gives a non-abrupt change of doping across the thickness of the stack, such as a shallow gradient across the interface. MACE of epitaxial layers of differently doped silicon is demonstrated in **Figure 5.15** to create porous/non-porous layers of silicon nanostructures, where the porous layer results from highly B-doped epitaxial silicon with a doping of 1E18 cm^{-3}, and the non-

porous layer results from B-doping of 1E15 cm^{-3}. The epitaxial silicon wafers are obtained from Lawrence Semiconductor Research Lab (LSRL).

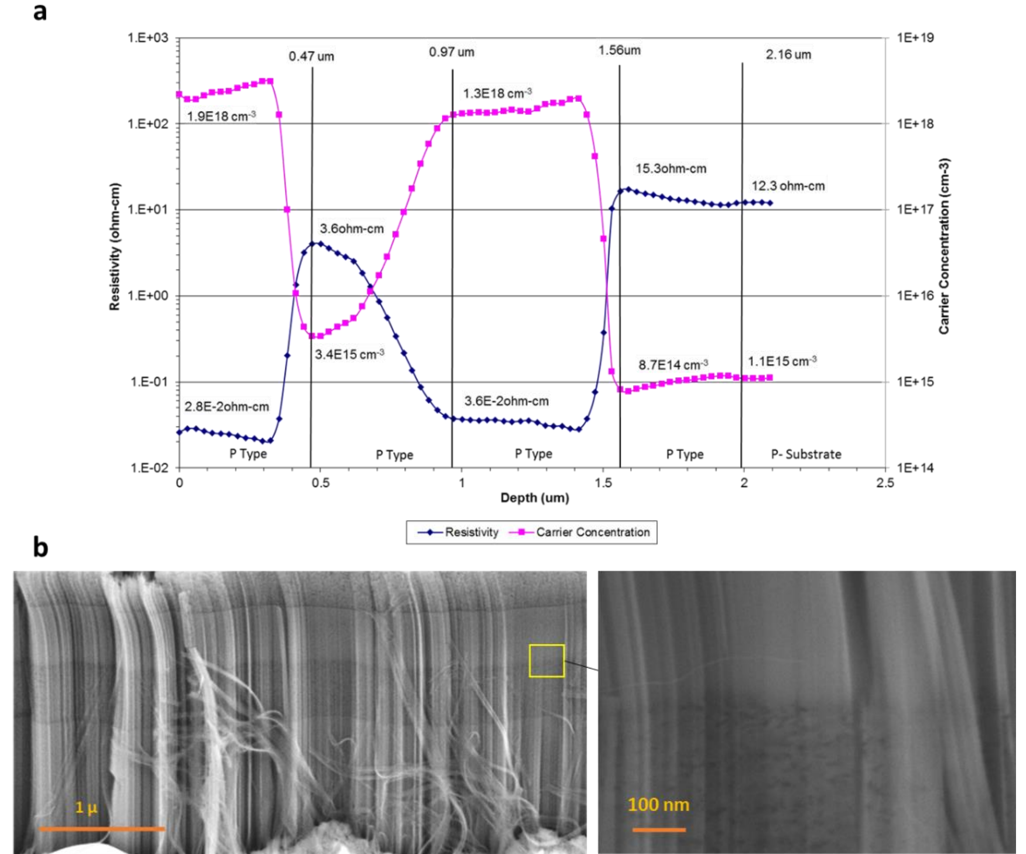


Figure 5.15: Silicon superlattice etch with epitaxial Si layers of alternating doping concentrations. (a) Doping concentration profiles for custom epitaxial wafers from Lawrence Semiconductor Research Laboratory (LSRL) with P++/P doped alternating epitaxial silicon layers, showing shallow (>100nm thick) transitions between high doping (~1E18 cm^{-3}) and low doping (~1E15 cm^{-3}), (b) Cross-section SEM of porous/non-porous interface made by MACE of differently doped epitaxial silicon layers.

With MACE of multilayer epitaxial layers, the etch is tuned to ensure that the morphology changes from porous to non-porous at a specific doping concentration, thereby changing the shallow doping concentration gradient into an abrupt step function of porous/non-porous interfaces. As MACE progresses through the epitaxial layers, the

catalyst mesh etches the silicon stack to reveal high aspect ratio nanostructures with tuned porosity.

Thus, MACE can enable fabrication of ultra-high aspect ratio silicon nanostructures as well as nanostructures with porous silicon superlattices. Methods of preventing process excursions such as nanostructure collapse and catalyst wandering due to isolated features in the catalyst and nanostructure design are described. These methods can be incorporated into application-specific design algorithms to create a MACE-based design for manufacturing framework.

5.3. RESULTS AND DISCUSSION

This chapter uses CMOS device fabrication requirements to demonstrate the potential of MACE as a next-generation etch technology. The main advantages of MACE – creating silicon nanostructures with no etch taper, ultrahigh resolution and aspect ratios – enable fabrication of next-generation 3D finFETs, nanosheet FETs and stacked transistor and memory architectures. Adoption of MACE as an alternative to plasma etch requires that the MACE process satisfy the following requirements (R1 – R7):

R1. Wafer-scale etch uniformity, high yield and high throughput

R2. CMOS-compatible materials and processes

R3. Prevention of nanostructure collapse

R4. Anisotropic etch of silicon for arbitrary design-specific geometries

R5. Prevention of catalyst wandering

R6. MACE porosity control and elimination of undesired porosity

R7. Integration of MACE in typical transistor fabrication process flows

The previous chapters demonstrate solutions to satisfy the above process requirements such as wafer-scale etch uniformity (R1), CMOS-compatible ruthenium catalysts (R2), insights into nanowire collapse (R3) and elimination of undesired porosity (R6).

This chapter extends this work in the context of transistor fabrication for anisotropic etching of design-specific geometries (R4) with Ru MACE, such as arrays of rectangular fins, holes and arbitrary geometries. For hole geometries where catalysts tend to wander during MACE, insights into the effects of catalyst material, geometry and MACE etchant concentration on wandering behavior is provided. Exemplar "maze-like" arbitrary geometries that can avoid both collapse and wandering are demonstrated. Future work can explore MACE process and geometry optimization for elimination of catalyst wandering (R5). Such optimization can be integrated with device design rules to generate device-

specific MACE-optimized catalyst designs. For transistors such as nanosheet FETs and stacked complementary FETs, fins comprising of alternating layers of material are required (R6). Precise porosity control during MACE can enable creation of superlattice nanostructures, as demonstrated in Figure 5.12 with Au MACE. Thus, MACE can act as a "drop-in" alternative to plasma etch for fabrication of finFETs and nanosheet FETs. Integration schemes for exemplar finFETs is shown in **Figure 5.16**, where linked fins are etched with MACE to prevent fin collapse and catalyst wandering, thereby providing a new direction for transistor design with ultra-high aspect ratio fins.

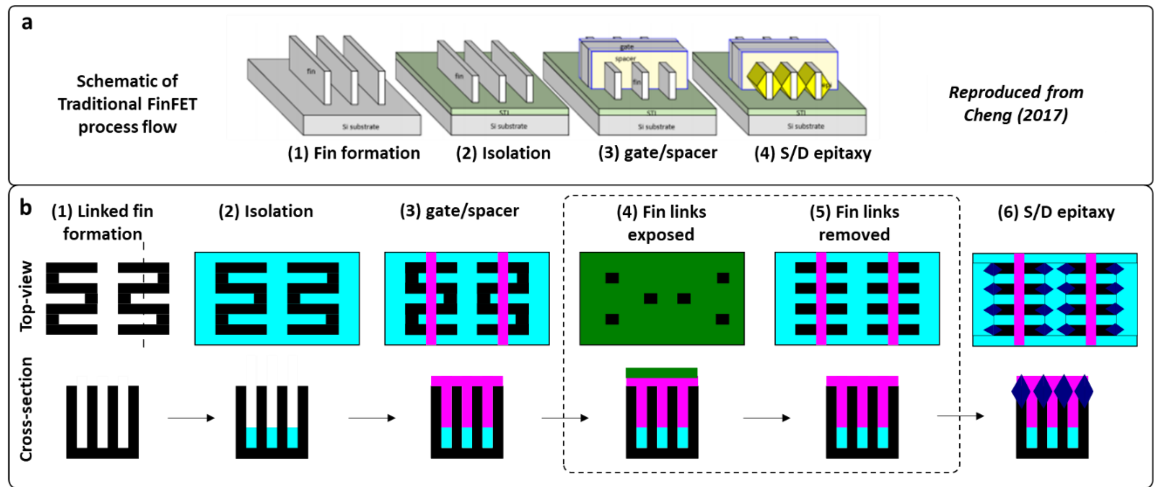


Figure 5.16: (a) Schematic of traditional finFET fabrication flow showing the essential processes[141]. (b) Modified finFET process flow where linked fins are formed to enable collapse-free ultrahigh aspect ratio fins. Steps (4-5) are added to the traditional finFET flow to remove fin links.

Metal Assisted Chemical Etch has been demonstrated as a wafer-scale, high yield, CMOS-compatible process for fabrication of arbitrary ultra-high aspect ratio semiconductor nanostructures that can be used to enable next generation 3D nanodevices.

Chapter 6: Conclusions and Future Work

6.1. Conclusions

The main objective of this thesis was to answer the question, “How can we develop an industry-compatible MACE process to create atomically precise high aspect ratio structures that enables next generation 3D electronic, optic, and biotech devices?” To this end, the following challenges in MACE were identified and resolved:

<u>Wafer-scale fabrication and characterization of silicon nanostructures</u> *(Chapter 2)*

This chapter builds upon small-area demonstrations of MACE in literature, and develops a reliable, repeatable wafer-scale Au MACE process for fabrication of vertical silicon nanowires. The etch uniformity, yield and defectivity is characterized using large-area high-throughput metrology with imaging spectroscopic scatterometry and optical modeling. This scalable silicon nanofabrication by Nanoimprint lithography, MACE, and Scatterometric metrology (“NIMS”) enables deployment of MACE for applications in 3D nanodevices.

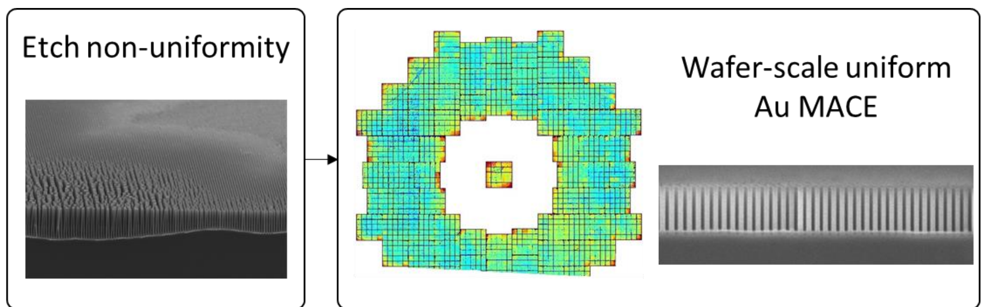


Figure 6.1: Wafer-scale Au MACE results from Chapter 2

<u>Collapse prevention to achieve ultra-high aspect ratio silicon nanostructures</u> *(Chapter 3)*

New experimental and theoretical insights into silicon nanowire collapse behavior are presented, enabled by a precise experimental technique (“Analog MACE”) to study the onset of nanowire collapse by creating controlled variation of NW heights. This

experimental approach resulted in unexpectedly tall Si-NWs for oversized wires separated by sub-50nm gaps, which was then understood to be due to the presence of "electrostatically repelling caps" on the nanowires. Thus, this work provides a new method of collapse prevention to enable free-standing ultra-high aspect ratio silicon nanostructures.

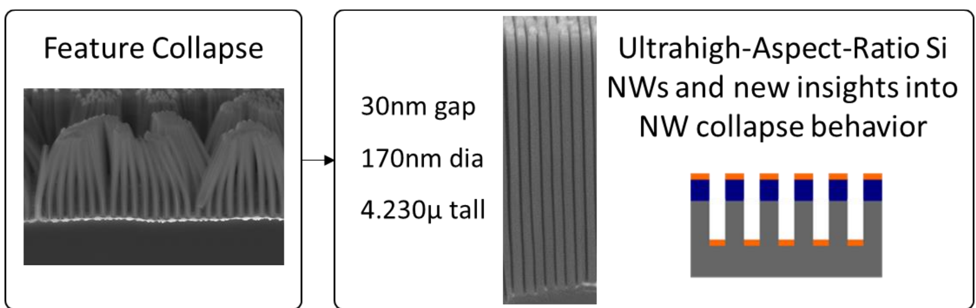


Figure 6.2: Ultrahigh-Aspect-Ratio SiNWs with gold-resist caps by Au MACE from Chapter 3

CMOS-compatible Ruthenium MACE *(Chapter 4)*

Ru MACE process is demonstrated with results comparable to Au MACE, thereby enabling CMOS-compatible MACE of silicon. Ru MACE can leverage the ecosystem already in place in the semiconductor industry for integration of Ru in CMOS devices, and can result in a "drop-in" MACE process in CMOS fabs. New parameters to reduce catalytic activity are introduced – including reduced Ru surface area and plasma modification – to achieve this result. This work provides powerful process variables to control undesirable porosity during MACE. Thus, this work removes a significant barrier to adoption of MACE by the semiconductor industry to enable high volume manufacturing of 3D CMOS nanodevices as well as non-CMOS devices requiring deep silicon etching in CMOS foundries.

Exemplar geometries, material stacks, and processes to demonstrate MACE for CMOS devices *(Chapter 5)*

This chapter extended the MACE process in the context of transistor fabrication for anisotropic etching of design-specific geometries with Ru MACE, such as arrays of rectangular fins, holes and arbitrary geometries. Future work will explore MACE process and geometry optimization for elimination of catalyst wandering. Such optimization can be integrated with device design rules to generate device-specific MACE-optimized catalyst designs, thereby providing a new direction for transistor design with ultra-high aspect ratio fins.

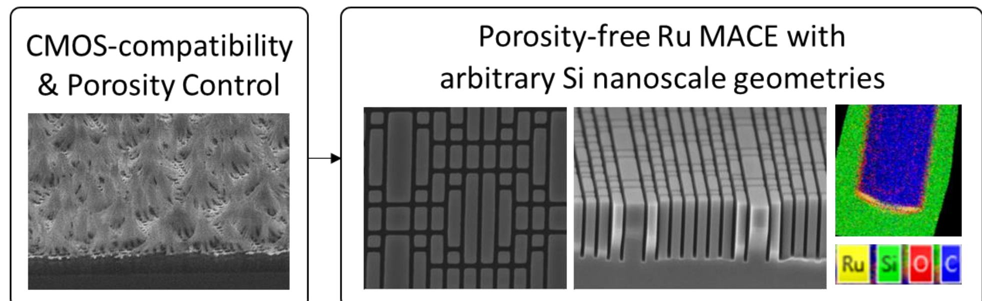


Figure 6.3: CMOS-compatible Ru MACE for arbitrary Si nanostructures from Chapters 4 and 5

In summary, this work demonstrates the promise of MACE as a next-generation etch technology to create ultra-high aspect ratio vertical semiconductor nanostructures, that do not suffer from etch issues caused by the industry standard plasma etch. This aids its translation from lab to fab for industry deployment, thereby enabling applications in next generation 3D electronic, optic, and biotech devices.

6.2. FUTURE WORK

The main requirements for a nanofabrication etch technology are (i) reliable wafer-scale processing, (ii) large area yield characterization, (iii) prevention of process excursions such as nanostructure collapse, and (iv) CMOS-compatibility. This thesis extends known MACE literature and provides solutions to these requirements, thereby creating a new platform to enable fabrication of ultra-high aspect ratio vertical semiconductor nanostructures which do not suffer from etch issues caused by the industry standard plasma etch. Future work broadly comprises of extending the solutions described in this thesis to arbitrary geometries and semiconductor material stacks, developing wafer-scale reliable processes and metrology, and using MACE to enable new design architectures for applications in high performance computing devices [9], memory devices [10,11] inter-connects [12], sensors [13], batteries [14], capacitors [15,16], solar cells [17], nanoscale deterministic lateral displacement arrays for exosome and antibody separation [18] and zone plates [19,20] among others. (Figure 1.1)

6.2.1. Extension of Collapse-avoidance methods to arbitrary geometries

The experimental method of detecting collapse onset in Chapter 3 can be extended to other geometries such as fins and non-circular cross-section arrays. The theoretical models presented here can be extended to more complex geometries based on application-specific nanostructure design constraints – such as to prevent collapse in high aspect ratio silicon fins for transistors and silicon nanowires for DLD arrays. Additionally, further improvements in critical collapse height can be explored using multiple strategies to minimize adhesion between nanostructures, maximizing electrostatic repulsion, etc. This work thus provides a new method of avoiding collapse in high aspect ratio silicon

nanostructures, beyond well-known methods like critical point drying, supercritical drying and use of low surface tension liquids.

Further, the method presented in Chapter 3 of increasing critical collapse heights may also be applied for plasma-etched nanowires with repelling "caps" created by the etch masks. Anomalous tall silicon nanowires obtained for by Khorasaninejad *et al.*[132] had been plasma-etched with an aluminum metal hard mask, and their collapse results were presented without removal of the aluminum mask. This suggests that removal of the aluminum masks for closely spaced silicon nanowires may cause the wires to collapse at lower heights as predicted by traditional collapse models. The effects of plasma etch *vs* MACE, the repelling "caps" and the source and variability of the charges on the "caps" can be explored in future research.

6.2.2. Wafer-scale Ruthenium MACE

The wafer-scale NIMS process and yield characterization in Chapter 1 can be extended to arbitrary design-specific geometries, and can be performed with ruthenium as a catalyst using porosity reduction methods described in Chapter 4. Further studies on the effects of various plasma treatments and their effect on Ru catalytic behavior can be explored to enable wafer-scale Ru MACE. Further, collapse-avoidance caps can be used to create wafer-scale ultra-high aspect ratio silicon nanostructures using Ru MACE as a path towards fabrication of CMOS logic and memory devices.

6.2.3. Catalyst removal after MACE: Ru Atomic Layer Etch

Additionally, to ensure that Ruthenium MACE can be used as a "drop-in" alternative to plasma etch for high aspect ratio silicon nanostructure etch, Ru patterning with plasma etch and its effect on Ru MACE needs to be explored. Ruthenium catalyst patterning with plasma etch typically uses an O_2/Cl_2 plasma, which may affect its catalytic activity for

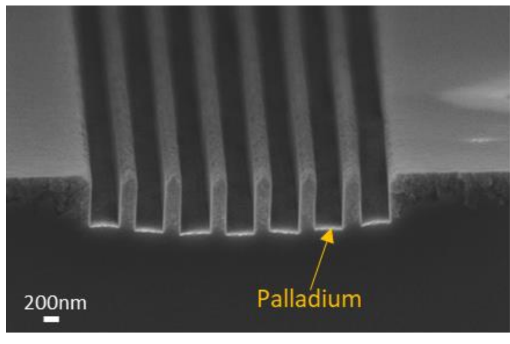
MACE, based on results presented in this chapter. The effects of Ru plasma etch chemistries, as well as the use of separate plasma modification steps on Ru MACE results can be examined. Ru ALE using Vacuum UV for oxidation[188] instead of plasma may have more desirable effects on the catalytic activity compared to plasma, and can be explored as a plasma-free alternative to Ru patterning. Removal of Ru after MACE also requires oxidizing plasmas which may create excess undesired oxidation of silicon nanostructures. Atomic Layer Etch (ALE) of Ru can be explored as an alternate method of removing Ru after MACE without affecting the MACE processed Si nanostructures.

6.2.4. Porosity reduction in MACE of non-silicon semiconductors

Future research could include exploring semiconducting substrate materials other than silicon such as Ge, InGaAs, InP, GaN, SiGe, SiC, etc., whose MACE results in literature also show undesirable, extraneous porosity.[30] The process features discussed in Chapter 4, such as mini-meshes and optimization of plasma treatment may enable much improved MACE processes in some of these semiconducting substrate materials.

6.2.5. Porosity reduction in MACE with other catalysts (Pt and Pd)

Most MACE literature on Pd and Pt shows highly porous silicon features, and further research is needed to explore reduction of porosity. Additionally, Pd and Pt are difficult to pattern with plasma etch due to poor volatility of etch products. Imprint lithography and metal lift-off were used to demonstrate creation of porous silicon nanostructures with Palladium and Platinum catalysts (**Figure 6.1**). The MACE etchant concentrations were optimized to decrease the porosity. Higher porosity for Pt MACE is expected due to higher catalytic activity of Pt compared to Pd. Further reduction of porosity may be explored using methods described in Chapter 4 for Ru MACE, such as mini-meshes and plasma modification of catalytic activity.



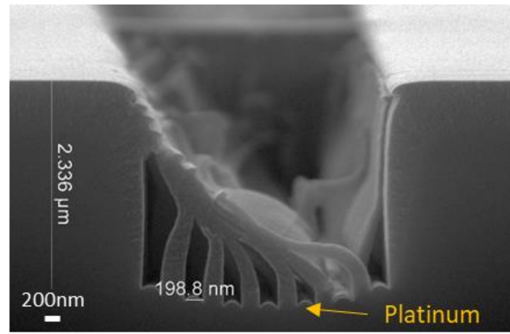


Figure 6.4: Porous silicon nanostructures made by MACE with Pd and Pt (a) Palladium as a catalyst and 6.1M HF and 0.38M H_2O_2, (b) Platinum as a catalyst and 7.4M HF and 0.5M H_2O_2. All samples are etched for 60s.

Another method of porosity reduction was described by Romano *et al.*,[189] where a good control of porosity was using vapor etchants as opposed to liquid etchants to eliminate porosity using Pt/$PtSi_x$ as a catalyst. Pt was patterned using lift-off, and a platinum silicide layer is formed for stable vapor MACE. Unlike Ru, high fidelity etch of nanoscale features of Pt and Pd is not available, but promising directions in ALE exist. Removal of Pt and $PtSi_x$ after MACE requires development of new metal etch processes. Future work in porosity reduction for MACE can include use of (i) plasma modification of catalytic activity, (ii) catalyst surface area reduction, (iii) etchant concentration optimization, and (iv) use of vapor etchants, apart from other known methods such as electric fields and temperature. Thus, this work demonstrates new directions to enable ultra-high aspect ratio etch of desired semiconductor materials with desired catalyst materials.

In summary, there is an unmet need for a reliable anisotropic etch process for fabrication of ultrahigh aspect ratio collapse-free semiconductor nanostructures for a variety of applications in electronics, memory, biotech, MEMS and optics. This work provides solutions for scalable and CMOS-compatible MACE that can be deployed in a semiconductor foundry, thereby enabling cost-effective scaling for a wide variety of CMOS and non-CMOS devices that require precise, high throughput, high yield nanofabrication.

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