10.2478/v10170-010-0020-9

Archives of Control Sciences
Volume 20(LVI), 2010
No. 3, *pages 317–339*

Feedback control of three-Level PWM rectifier: Application to the stabilization of DC Voltages of five-level NPC active power filter

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One of the most important drawbacks of the three phases five-level NPC (Neutral Point Clamped) Active Power Filter (APF) is the neutral point balance. As the consequence, the capacitors voltages of the input DC bus of the APF are not equal which constitutes the major limitation for the use of this power converter. In order to stabilize these DC voltages, it is proposed in this paper to study the cascade constituted by three phases three-level PWM rectifier-clamping bridge filter-five-level NPC APF. In the first part, the authors present a topology of five-level NPC Voltage Source Inverter (VSI), and then, they propose a model of this converter and its PWM control strategy. In the second part, the modeling and control of three-level PWM current rectifier is presented. In the third part, to remedy to instability problem of the input capacitors DC voltages of the APF, the authors propose feedback control of the three-level PWM rectifier followed by clamping bridge filter. After that, the sliding mode regulator used to control the active filter is developed. The obtained results are full of promise to use this topology of APF in high voltage and high power applications.

Key words: active power filter, NPC multilevel inverter, feedback control, PWM current rectifier, clamping bridge filter

1. Introduction

The increasing use of control systems based on power electronics in industry involves more and more disturbance problems in the level of the electrical power supply networks [1]. Thus, one remarks a regular increase in currents harmonic distortion and unbalance rates, as well as an important consumption of the reactive power. These harmonic currents yield voltage harmonics and unbalances via impedance of power supply network, which infects the sinusoidal waveform of the electrical power supply voltage. Obviously, these disturbances cause negative consequences on electrical equip-

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Received 10.05.2010.

ment, such as strong heating, sudden stopping of the revolving machines or even the total destruction of the equipment.

Several solutions for reducing harmonic current in electrical power supply networks were proposed. Those which satisfy more the industrial constraints are the active compensators such as shunt active filter, series active filter and combined shunt-series active filters.

In fact, the main role of active filtering is to constantly control the harmonic distortion in an active way by the compensation of the harmonics [2-3]. European standards CEI 61000-3-4 and CEI 61000-3-6 define low, medium and high voltage power supply networks harmonic currents limits [4].

Research on the shunt active filters implied different works concerning harmonics identification methods such as Fourier transform method [5], the method of synchronous reference frame (d-q) [6], and control strategies such as sliding mode regulators, artificial neural networks and fuzzy logic controllers [7-9]. The structures of the filters also knew an evolution, from two-level converters [10-11] to multilevel converters [12-14]. In high power applications, this latter is more adequate, compared to the conventional two-level structure, simply because of the low harmonic distortion rate of source voltage and current, low switching frequency besides no need to use transformer [15-17]. Various topologies are developed such as flying capacitor multilevel converters, diode clamped multilevel converters, NPC multilevel converters, and H bridge multilevel converters. Research works concerning the use of the three-level voltage source filters in medium voltage power supply applications are developed [17-18].

The unbalance of the different DC voltage sources of the multi-level (NPC) active power filters constitutes the major limitation for the use of these power converters.

The objective of this paper is to stabilize the input DC voltages of five-level NPC APF. For this purpose, a feedback control of three-level PWM rectifier followed by clamping bridge filter is used. This APF is applied for the enhancement of 4kV (ph-ph) network power quality by compensation of harmonic currents produced by an induction motor speed variator (Fig. 1). This variator consists in cascaded thyristor bridge rectifier-clamping bridge filter-three-level PWM NPC VSI-vector controlled induction motor.

The 8.2kV DC bus of the APF contains four series capacitors. It is fed via a PWM controlled three-level current rectifier fed by the same power supply network.

First part is dedicated to the presentation of the mean values model of the three phases five-level NPC VSI with its four carriers triangulo-sinusoidal PWM control strategy. In the second part, the modeling and control of three-level PWM current rectifier is presented. After that the control strategy of the input DC voltages of multilevel NPC APF is presented. The five-level shunt APF is controlled using a sliding mode regulator. At the end, simulation results are presented.

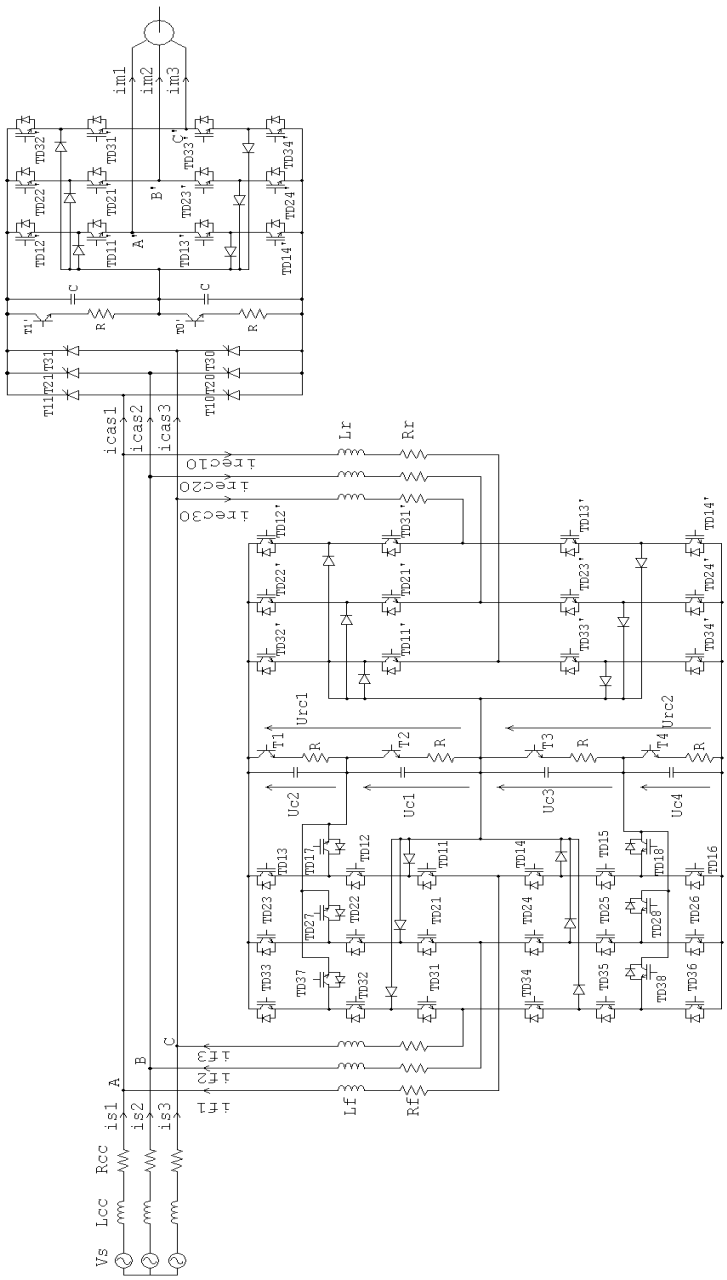

Figure 1. Synoptic diagram of application of shunt APF on power supply fed cascaded thyristor bridge rectifier-clamping bridge filter-three level VSI-induction motor.

2. Modeling of five-level NPC voltage source inverter

2.1. Knowledge model of five-level NPC VSI

The three phases five-level NPC VSI is constituted by three legs and four DC voltage sources. Every leg has eight bi-directional switches, six in series and two in parallel, and two diodes to get the zero voltage for V_{KM} (V_{KM} is the voltage of the phase K relatively to the middle point M and $K = A, B, C$) (Fig. 2). Every switch is composed by a transistor and a diode in anti-parallel. This inverter is fed by a battery of voltage E [19].

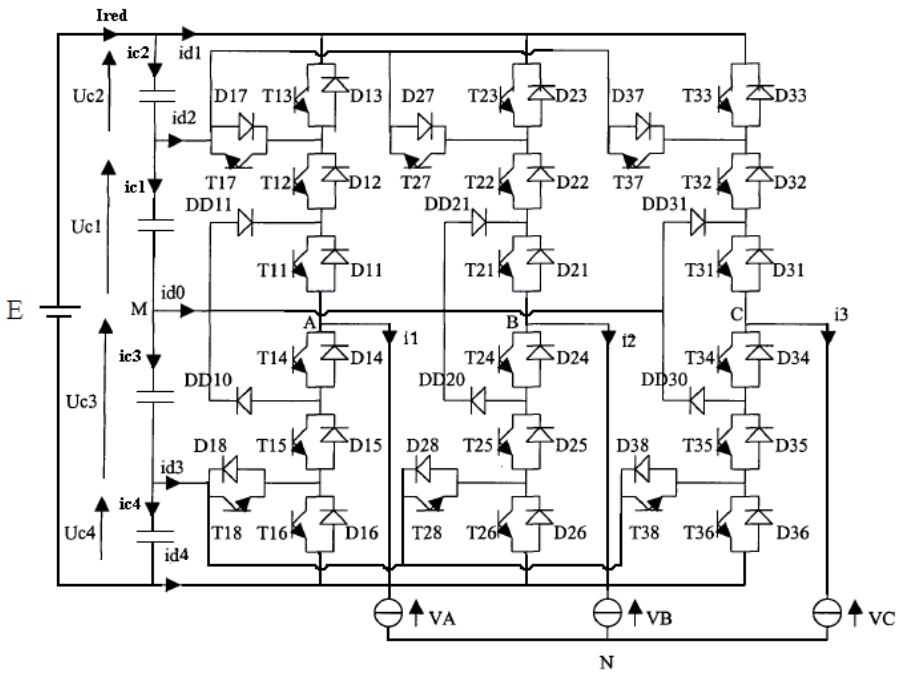

Figure 2. Five-level NPC voltage source inverter.

The switch connection function F_{ks} indicates the opened or closed state of the switch T_{ks}:

$$F_{ks} = \begin{cases} 1 & \text{if} \quad T_{ks} \quad \text{close} \\ 0 & \text{if} \quad T_{ks} \quad \text{open.} \end{cases} \tag{1}$$

We define a half leg connection function F^b_{Km} as:

$$\begin{cases} F^b_{K1} = F_{K1}F_{K2}F_{K3} \\ F^b_{K0} = F_{K4}F_{K5}F_{K6} \end{cases} \tag{2}$$

where $m = 1$ refers to the lower half leg and $m = 0$ to the upper half leg.

For a leg K, several complementary control laws are possible for the five-level NPC VSI. The optimal control law of this inverter is:

$$\begin{cases} B_{k5} = \bar{B}_{k1} \\ B_{k4} = \bar{B}_{k2} \\ B_{k6} = \bar{B}_{k3} \\ B_{k7} = B_{k1}B_{k2}\bar{B}_{k3} \\ B_{k8} = B_{k4}B_{k5}\bar{B}_{k6} \end{cases} \tag{3}$$

where B_{ks} represents the gate control of the switch T_{ks}; $k = 1,2,3$ and $s = 1 \ldots 8$.

Tab. 1 represents the excitation table of switches of a leg of the converter.

The output voltages relatively to the middle point M of the inverter, using the connection functions, are given as follows:

$$\begin{bmatrix} V_{AM} \\ V_{BM} \\ V_{CM} \end{bmatrix} = \begin{bmatrix} F_{17} + F_{11}^b \\ F_{27} + F_{21}^b \\ F_{37} + F_{31}^b \end{bmatrix} U_{c1} + \begin{bmatrix} F_{11}^b \\ F_{21}^b \\ F_{31}^b \end{bmatrix} U_{c2} - \begin{bmatrix} F_{18} + F_{10}^b \\ F_{28} + F_{20}^b \\ F_{38} + F_{30}^b \end{bmatrix} U_{c3} - \begin{bmatrix} F_{10}^b \\ F_{20}^b \\ F_{30}^b \end{bmatrix} U_{c4}. \tag{4}$$

The output voltages relatively to the point N and the input currents i_{d1}, i_{d2}, i_{d3}, i_{d4}, i_{d0} of the inverter using the connection functions and load currents i_1, i_2 and i_3 are given as follows:

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \left\{ \begin{bmatrix} F_{17} + F_{11}^b \\ F_{27} + F_{21}^b \\ F_{37} + F_{31}^b \end{bmatrix} U_{c1} + \begin{bmatrix} F_{11}^b \\ F_{21}^b \\ F_{31}^b \end{bmatrix} Uc_2 - \begin{bmatrix} F_{18} + F_{10}^b \\ F_{28} + F_{20}^b \\ F_{38} + F_{30}^b \end{bmatrix} U_{c3} - \begin{bmatrix} F_{10}^b \\ F_{20}^b \\ F_{30}^b \end{bmatrix} U_{c4} \right\}, \tag{5}$$

$$\begin{cases} i_{d1} = F_{11}^b i_1 + F_{21}^b i_2 + F_{31}^b i_3 \\ i_{d2} = F_{17} i_1 + F_{27} i_2 + F_{37} i_3 \\ i_{d3} = F_{18} i_1 + F_{28} i_2 + F_{38} i_3 \\ i_{d4} = F_{10}^b i_1 + F_{20}^b i_2 + F_{30}^b i_3 \\ i_{d0} = i_1 + i_2 + i_3 - i_{d1} - i_{d2} - i_{d3} - i_{d4} \quad . \end{cases} \tag{6}$$

Equation (7) defines the capacitors currents i_{c1}, i_{c2}, i_{c3} and i_{c4} of the five-level inverter using the input currents i_{d1}, i_{d2}, i_{d3}, i_{d4}, i_{d0} and battery current I_{red} .

Table 2. Excitation table of a leg K of five-level NPC VSI

B_{k1}	B_{k2}	B_{k3}	V_{kM}
1	1	1	$U_{c1}+U_{c2}$
1	1	0	U_{c1}
1	0	0	0
0	0	1	$-U_{c3}$
0	0	0	$-U_{c3}-U_{c4}$

$$\begin{cases} i_{c1} = C_1 \dfrac{dU_{c1}}{dt} = I_{red} - i_{d1} - i_{d2} \\ i_{c2} = C_2 \dfrac{dU_{c2}}{dt} = I_{red} - i_{d1} \\ i_{c3} = C_3 \dfrac{dU_{c3}}{dt} = I_{red} - i_{d1} - i_{d2} - i_{d0} \\ i_{c4} = C_4 \dfrac{dU_{c4}}{dt} = I_{red} - i_{d1} - i_{d2} - i_{d3} - i_{d0}. \end{cases} \tag{7}$$

2.2. Control model

The model established above is discontinuous. It is used to simulate and to validate control algorithms. To adapt this model in order to use it to drive the inverter, we define the generating functions. The generating connection function F_{ksg} is a continuous function which represents average value of connection function F_{ks} on a modulation period T_m supposed very small:

$$F_{ksg} = \left[\frac{1}{T_m} \int_{nT_m}^{(n+1)T_m} F_{ks}(t)\,dt \right] \in [0,1] \quad \text{with} \quad n \in N \quad \text{and} \quad T_m \to 0. \tag{8}$$

The control model of three phases five-level NPC VSI, deduced from the system (8) and by supposing capacitors voltages equal to U_c, is given by the following equation where $\langle V_A \rangle$, $\langle V_B \rangle$ and $\langle V_C \rangle$ represent the mean value of the instantaneous ones.

$$\begin{bmatrix} \langle V_A \rangle \\ \langle V_B \rangle \\ \langle V_C \rangle \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} (F_{11}^{bT})_g - (F_{10}^{bT})_g \\ (F_{21}^{bT})_g - (F_{20}^{bT})_g \\ (F_{31}^{bT})_g - (F_{30}^{bT})_g \end{bmatrix} U_c \tag{9}$$

with

$$\begin{matrix} (F_{i1}^{bT})_g = (F_{i7})_g + 2(F_{i1}^{b})_g \\ (F_{i0}^{bT})_g = (F_{i8})_g + 2(F_{i0}^{b})_g \end{matrix} \quad i = 1,2 \text{ and } 3. \tag{10}$$

2.3. PWM strategy of the five-level NPC VSI

Two-level carrier-based PWM techniques have been extended to multilevel inverters using several triangular carrier signals and one reference signal per phase. For N-level inverter, (N - 1) carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy are contiguous. The reference, or modulation, wave form has peak-to-peak amplitude A_m and frequency f_m, and its centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals (Fig. 3). If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched-on; and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched-off. In multilevel inverters, the amplitude modulation index, m_a, and the frequency ratio, m_f, are defined as [20-22]:

$$\begin{cases} m_a = \dfrac{A_m}{A_c}, \\ \\ m_f = \dfrac{f_c}{f_m}. \end{cases} \tag{11}$$

The different input DC voltages of the inverter are fed by a battery E (Fig. 2). Fig. 4 shows the simple output voltage V_A of the five-level NPC VSI controlled by the PWM strategy for $m_f = 9$ and $m_a = 0.8$. Fig. 5 displays the voltages across input capacitors. It can be noted that these capacitors voltages are unbalanced.

3. Modeling and control of three-level PWM current rectifier

The advantages of three-level PWM current rectifier topology (Fig. 6) are well known and have been applied in medium voltage and high power applications in the last years [20].

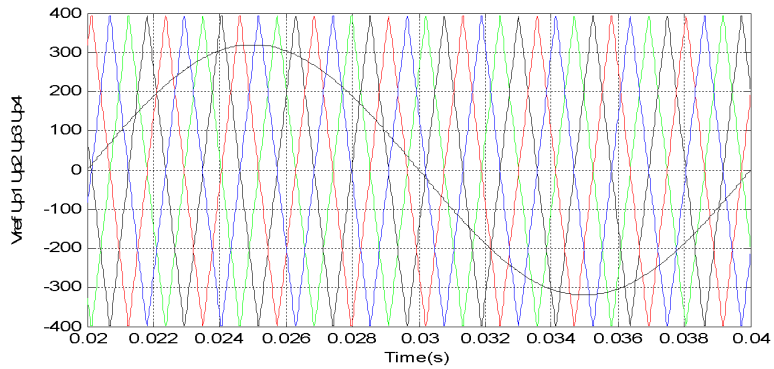

Figure 3. Triangulo-sinusoidal strategy with four bipolar carriers ($m_f = 9$, $m_a = 0.8$).

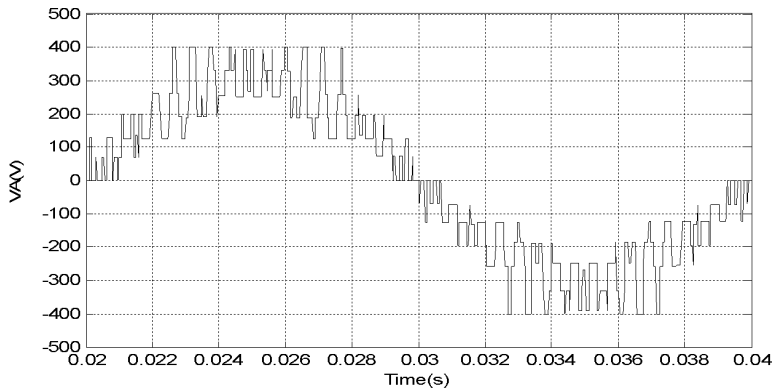

Figure 4. Simple output voltage V_A ($m_f = 9$, $m_a = 0.8$).

3.1. Modeling of three-level PWM current rectifier

The reversibility of the three-level VSI allows it to work as current rectifier. The input voltages of three-level PWM rectifier are defined as follows:

$$\begin{bmatrix} V_{AR} \\ V_{BR} \\ V_{CR} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \left(\begin{bmatrix} F_{11}^b \\ F_{21}^b \\ F_{31}^b \end{bmatrix} U_{rc1} - \begin{bmatrix} F_{10}^b \\ F_{20}^b \\ F_{30}^b \end{bmatrix} U_{rc2} \right). \tag{12}$$

The rectifier output currents are given as follows:

$$\begin{cases} i_{rec1} = F_{11}^b i_{rec10} + F_{21}^b i_{rec20} + F_{31}^b i_{rec30} \\ i_{rec2} = F_{10}^b i_{rec10} + F_{20}^b i_{rec20} + F_{30}^b i_{rec30} \end{cases} \tag{13}$$

with $i_{rec0} = -(i_{rec1} + i_{rec2})$.

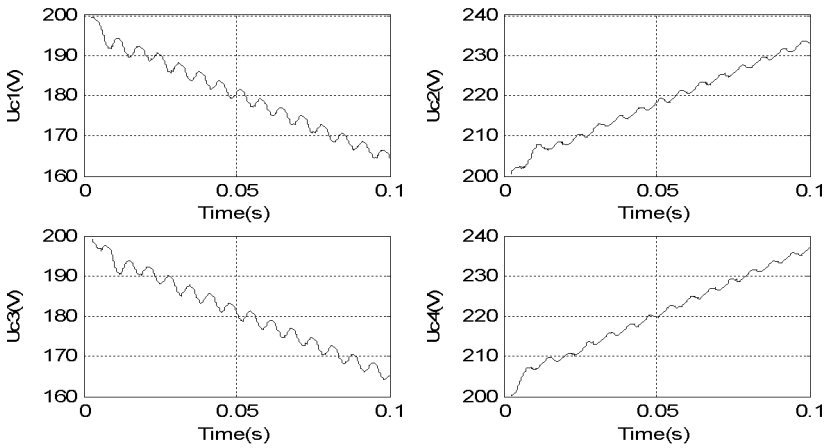

Figure 5. Inverter input capacitors voltages.

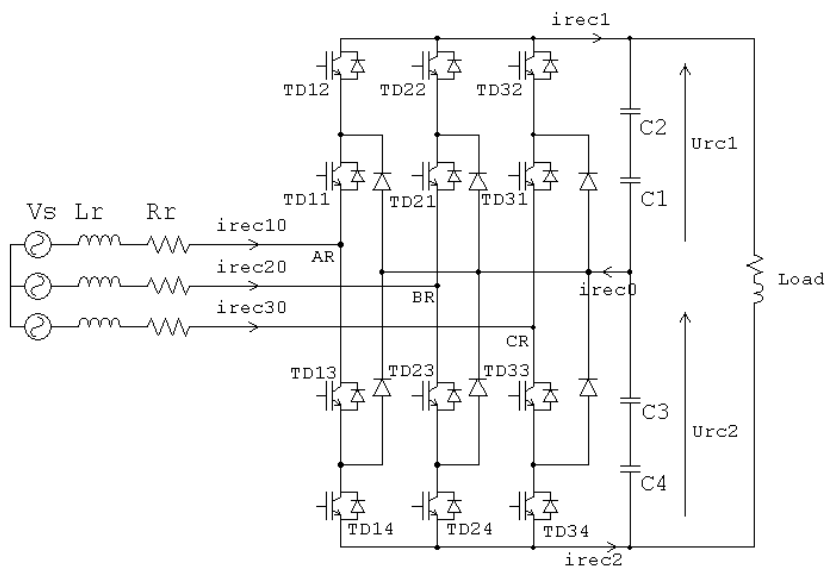

Figure 6. Three-level PWM current rectifier topology.

3.2. Double band hysteresis current control

The basic principle of the double band hysteresis current control is based on the classical hysteresis control applied to conventional two-level inverters. Two hysteresis bands (Upper and Lower Commutation Bands) around the reference current are defined. The hysteresis bands are actually superimposed but to differentiate them, they will be

named as upper and lower band. The hysteresis algorithm is given by equation (15) and Fig. 7.

$$\varepsilon_i = i_{reci0} - i_{reci0ref} \tag{14}$$

ε_i is the difference between reference current $i_{reci0ref}$ and source current i_{reci0}:

$$\begin{cases} [(\varepsilon_i \geqslant \Delta h) \ \& \ (\varepsilon_i \leqslant 2\Delta h)] \text{ or} \\ [(\varepsilon_i \leqslant -\Delta h) \ \& \ (\varepsilon_i \geqslant -2\Delta h)] & \Rightarrow B_{i1} = 1,\ B_{i2} = 0 \\ (\varepsilon_i > 2\Delta h) & \Rightarrow B_{i1} = 0,\ B_{i2} = 0 \\ (\varepsilon_i < -2\Delta h) & \Rightarrow B_{i1} = 1,\ B_{i2} = 1 \end{cases} \tag{15}$$

Δh is hysteresis band width.

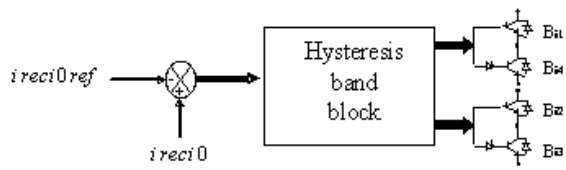

Figure 7. Principle of the hysteresis control.

4. Control strategy of the input DC voltages of multilevel NPC APF

In this part, one proposes to remedy to the problem of the instability of the output DC voltages of PWM rectifier, by using a clamping bridge filter and feedback control of the output DC voltage of PWM multilevel rectifier [21-24].

4.1. Modeling and control of clamping bridge

The clamping bridge cell is a simple circuit constituted by a transistor and a resistor in series connected in parallel with a capacitor as shown in Fig. 8. The transistors are controlled in order to maintain the equality of the different voltages [25-26].

In this part, the model of the intermediate filter with clamping bridge is defined by the following equation:

$$C_i \frac{dU_{ci}}{dt} = I_{redi} + i_{r(i+1)} + i_{c(i+1)} - i_{di} - i_{ri} \tag{16}$$

with $i_{ri} = T_i \frac{U_{ci}}{R_i}$.

The transistor is controlled using the following algorithm:

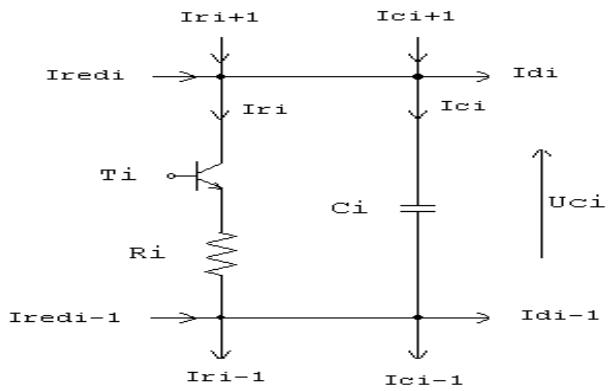

Figure 8. Clamping bridge cell.

$$\begin{cases} \varepsilon_i = U_{ci} - U_{cref} \\ \text{if } \varepsilon_i > d_r \text{ and } T_i = 1 & \Rightarrow ir_1 = T_i = \frac{U_{ci}}{R_i} \\ \text{if } \varepsilon_i < -d_r \text{ and } T_1 = 0 & \Rightarrow ir_1 = 0 \end{cases} \tag{17}$$

where d_r is hysteresis band widh.

4.2. Multi DC bus link voltage controller

In this part, one proposes to enslave the output DC voltage of three-level PWM current rectifier using a PI-based feedback control. The synoptic diagram of three-level PWM current rectifier control is shown in Fig. 9 [21]. The transfer functions $G_I(s)$ and $G_V(s)$ are expressed as follows:

$$G_I(s) = \frac{\dfrac{1}{R_r}}{1 + \dfrac{L_r}{R_r}s}, \tag{18}$$

$$G_V(s) = \frac{1}{Cs}. \tag{19}$$

The modeling of this loop is based on the instantaneous power conservation principle with no loss hypothesis. This loop imposes the root mean square (rms) value of network current [27-28].

Input and output powers are:

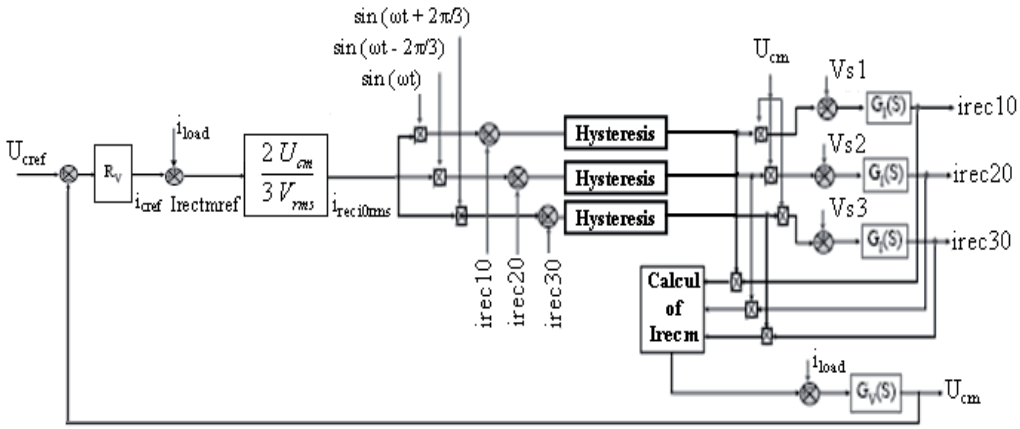

Figure 9. Synoptic diagram of three-level PWM current rectifier control.

$$\begin{cases} P_{in} = \sum_{i=1}^{3} \left(V_{si} i_{reci0} - R_r i_{reci0}^2 - \dfrac{L_r}{2} \dfrac{d i_{reci0}^2}{dt} \right), \\ P_{out} = \sum_{i=1}^{2} (U_{rci} i_{reci}) = 2 U_{cm} (i_c + i_{load}) \quad . \end{cases} \tag{20}$$

Different quantities I_{rectm}, i_{load}, i_c are defined as follows:

$$\begin{cases} I_{rectm} = \dfrac{I_{red1} - I_{red2}}{2} \\ i_{load} = \dfrac{i_{d1} - i_{d2}}{2} \\ i_c = I_{rectm} - i_{load}. \end{cases} \tag{21}$$

Using of the power conservation principle and neglecting of joules loss in the resistor R_r, and considering a sinusoidal supply network current in phase with corresponding voltage V_{si}, it can be written:

$$3 V_{si} i_{reci0} = 2 U_{cm} (i_c + i_{load}). \tag{22}$$

5. Active power filter control

A voltage source of 4 kV (ph-ph) and a frequency $f_s = 50$Hz is considered. It feeds cascaded thyristor bridge rectifier-clamping bridge filter-three-level NPC VSI-induction motor which represents the induction motor speed variator illustrated in Fig. 10. This

load produces a distorted current of 54.44% THD which is above the tolerated THD limit standard. This current with its spectral analysis are presented in Fig. 11. Three-level VSI input DC voltages U_{red1} and U_{red2} are depicted in Fig. 12.

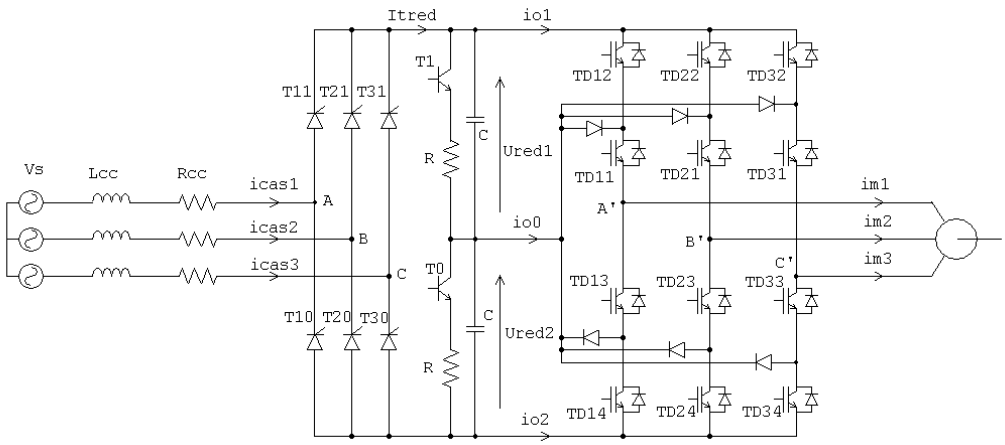

Figure 10. Induction motor speed variator .

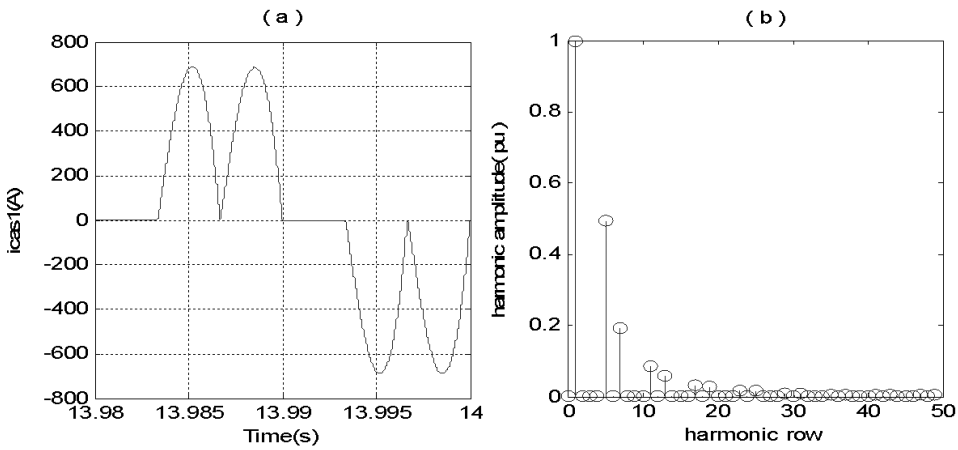

Figure 11. Current drawn by the induction motor speed variator THD=54.44%.

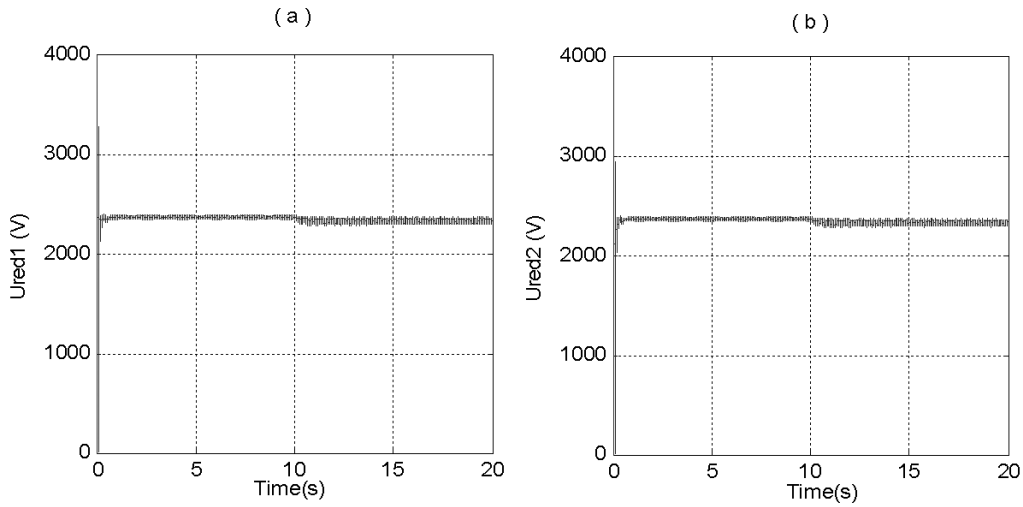

Figure 12. Three-level VSI input DC voltages.

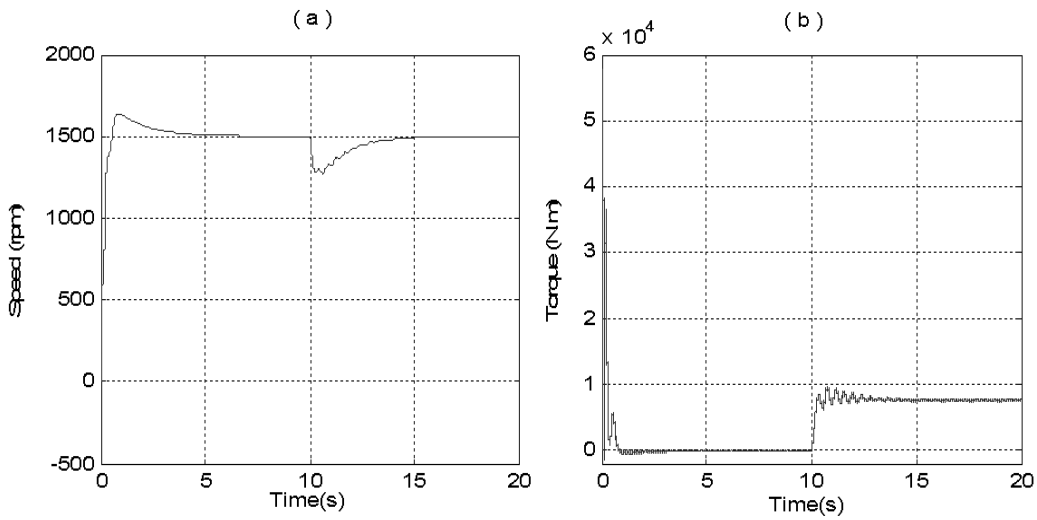

Figure 13. Induction motor mechanical features.

Torque and speed features of this motor are presented in Fig. 13. At $t = 10$sec, rated torque ($T_n = 7.6$kNm) is applied. It is noticed that the speed turns back to its reference (1500 rpm) after a slight decrease.

Active power filter is controlled using sliding mode regulator. It consists in pulling state trajectory of controlled variable towards the sliding surface and makes its evolution with a certain dynamic till the equilibrium point. Sliding mode regulators design considers systematically stability issues and desired performances. Implementation of this method is done basically in three steps. First, made the choice of sliding surface, then satisfy the convergence condition and calculate the control law [7-9], [29-30].

The model of active filter associated to supply network is presented by equation (23). We would control active filter current. For that, we choose the sliding surface (S_s) as indicated in equation (24).

$$V_{frefK} - V_K = R_f i_{fK} + L_f \frac{di_{fK}}{dt} \tag{23}$$

with $V_K = V_{SK} - R_{cc} i_{SK} - L_{cc} \frac{di_{SK}}{dt}$; $K = 1, 2$ and 3,

$$S_s = i_{frefK} - i_{fK} \tag{24}$$

where i_{frefK} is the harmonic current reference and i_{fK} the active filter current of phase K. Its derivative is:

$$\dot{S}_s = \dot{i}_{frefK} - \dot{i}_{fK}. \tag{25}$$

By substituting (25) in (23) and by considering the sliding mode condition $\dot{S}_s = 0$, one obtains the equivalent control law.

$$V_{fref.eq} = R_f i_{fK} + L_f \frac{di_{frefK}}{dt} + V_K. \tag{26}$$

Condition $S_s \cdot \dot{S}_s < 0$ assures the attraction of the trajectory toward the sliding surface. To verify this condition, it's sufficient to choose:

$$V_{fref.att} = k \frac{S_s}{|S_s| + \lambda} \tag{27}$$

where k is the amplification coefficient and λ is the damping coefficient.

Finally, one gets the following control law.

$$V_{fref} = V_{fref.eq} + V_{fref.att} = R_f i_{fK} + L_f \frac{di_{frefK}}{dt} + V_K + k \frac{S_s}{|S_s| + \lambda}. \tag{28}$$

As shown in Fig. 1, the input DC bus of NPC five-level shunt APF is fed by a three-level PWM current rectifier followed by clamping bridge filter. This rectifier is fed by the same power supply network feeding the speed variator. The application of the feedback control on the rectifier allows getting a stable total output DC voltage around its reference. Balancing capacitors voltages is guaranteed by the clamping bridges.

Fig. 14 illustrates the output DC voltages U_{rc1} and U_{rc2} of three-level PWM rectifier. This voltages is maintained around its 4.1kV reference voltage before and after application of clamping bridges at $t = 13$s.

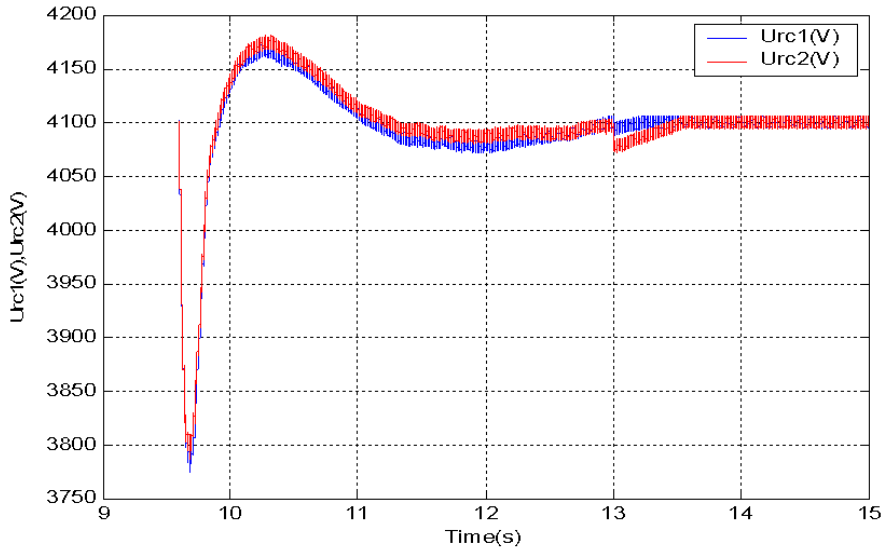

Figure 14. Output DC voltage of three-level PWM rectifier before and after application of clamping bridges.

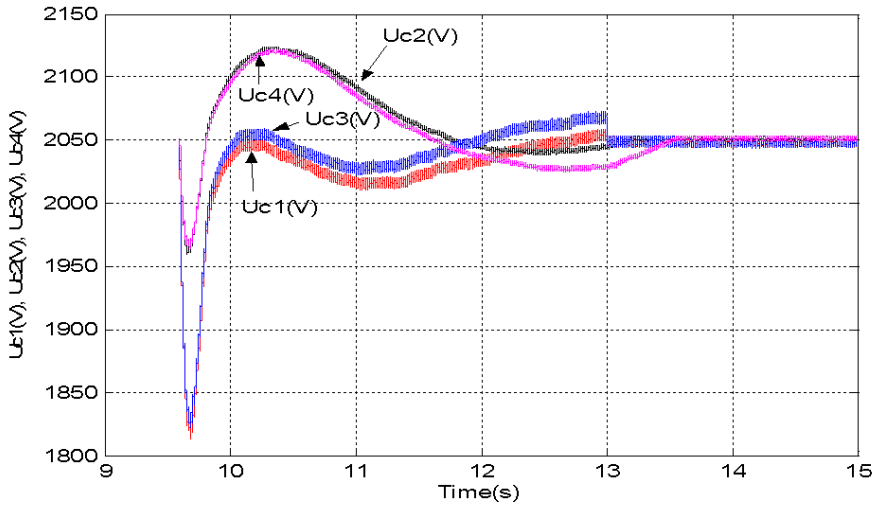

Figure 15. DC bus capacitors voltages before and after application of clamping bridges.

Fig. 15 shows DC bus capacitors voltages before and after application of clamping bridges. Before $t = 13$s, these voltages diverge, but the total voltage remains constant. Application of clamping bridges allows getting stable capacitors voltages around there reference.

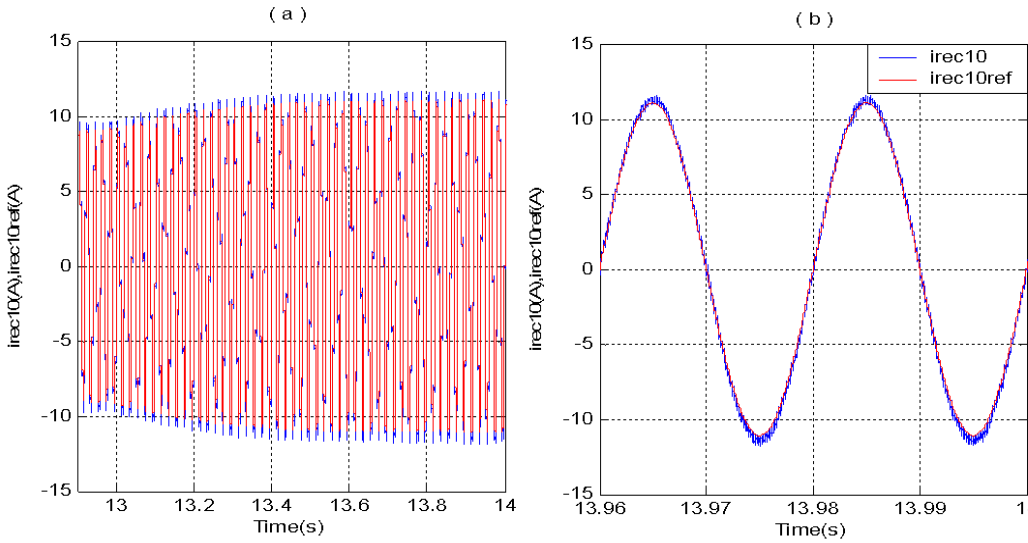

Figure 16. PWM rectifier current irec10 and its reference $i_{rec10ref}$.

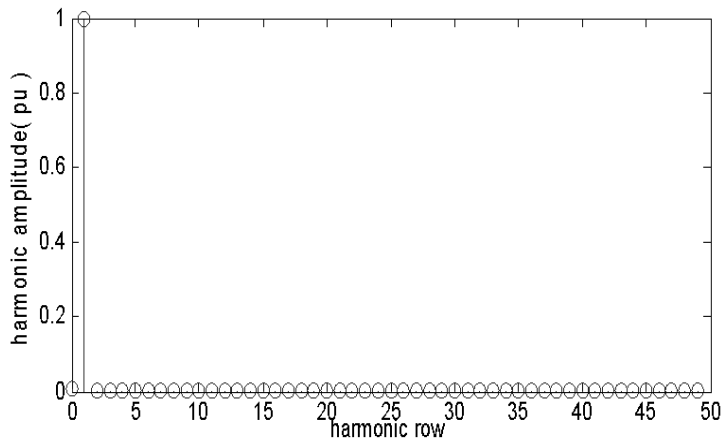

Figure 17. Spectral analysis of PWM rectifier current i_{rec10} (THD=1.3%).

Fig. 16.a presents first phase PWM three-level rectifier current i_{rec10} and its reference current $i_{rec10ref}$ before and after application of clamping bridge. Part of the power is dissipated in resistances of clamping bridges, which justifies the increase in the amplitude of the current. 0.1A band hysteresis controlled three-level rectifier allows maintaining rectifier current i_{rec10} around its sinusoidal reference $i_{rec10ref}$ as shown in Fig. 16.b. Fig. 17 displays spectral analysis of this current with 1.3% total harmonic distortion.

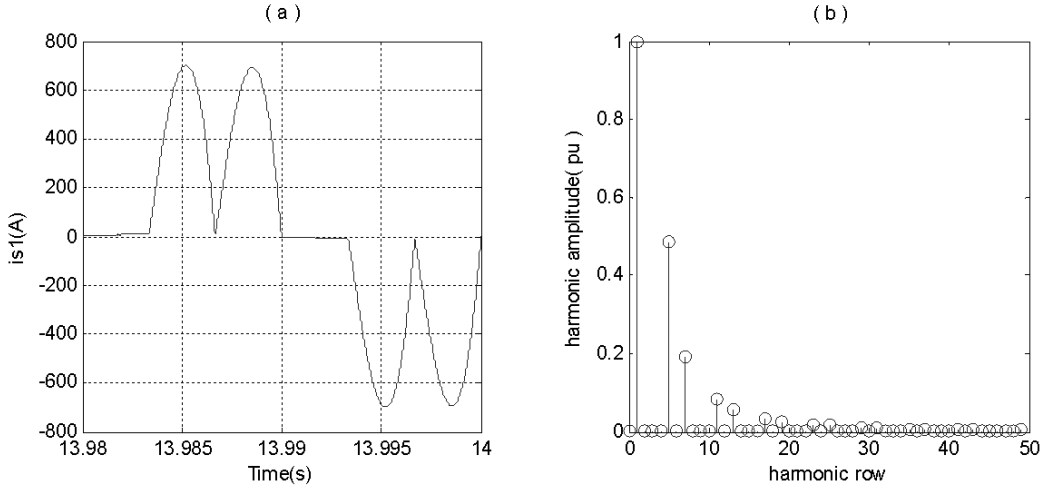

Figure 18. Main source current before harmonic current compensation (THD=53.41%).

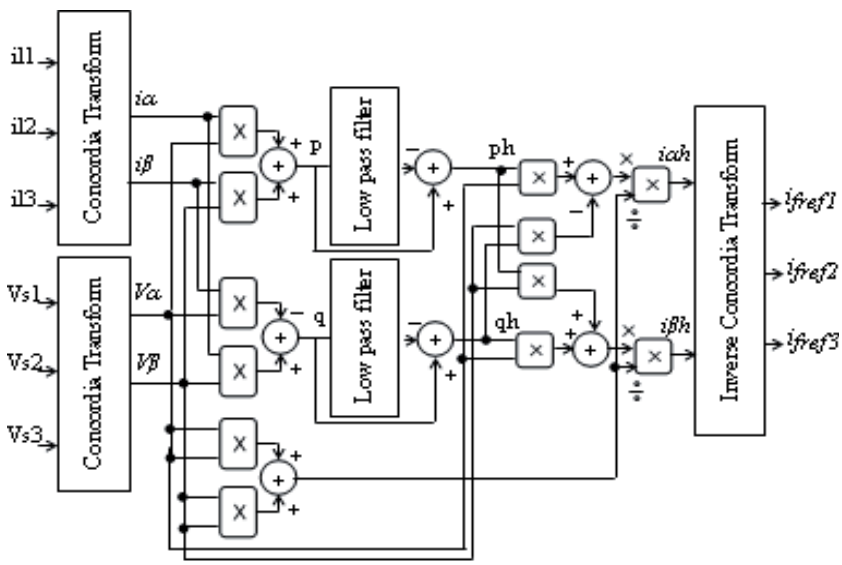

Figure 19. Instantaneous real and imaginary powers harmonic current identification algorithm.

Fig. 18 illustrates source current i_{s1} which is the sum of current drawn by speed variator i_{cas1} and first phase rectifier current i_{rec10} before harmonic current compensation. This current presents a 53.41% total harmonic distortion.

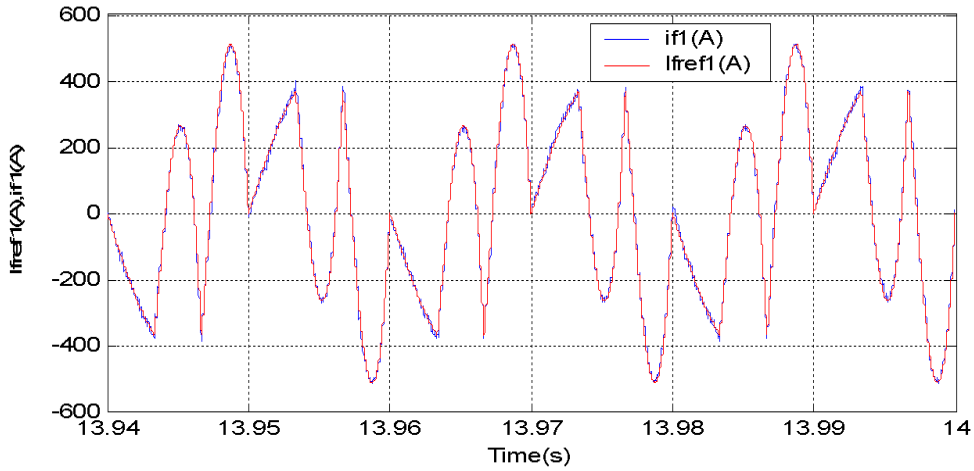

Figure 20. Reference harmonic current Ifref1 and filter output current i_{f1}.

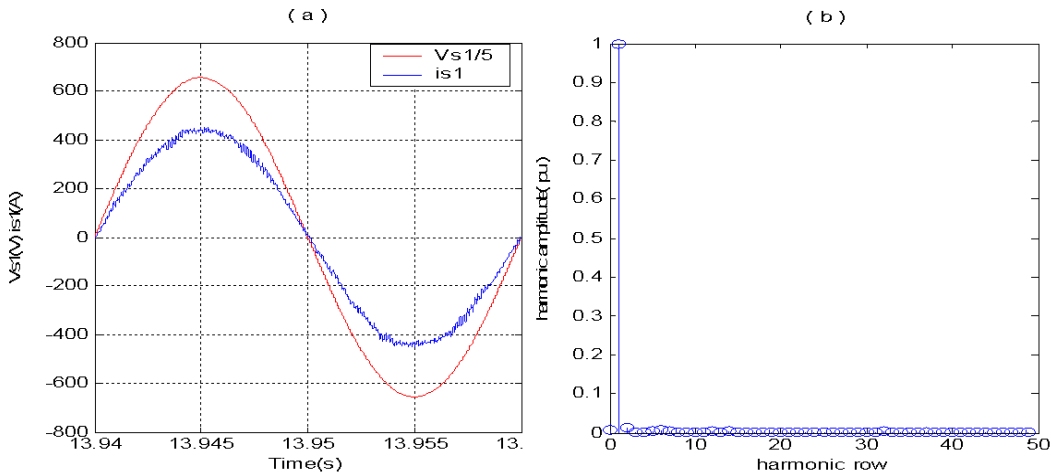

Figure 21. Main source voltage $V_{s1}/5$ and current i_{s1} with its spectral analysis (THD=2.44%).

Instantaneous real and imaginary powers method is used to identify reference harmonic currents. Its algorithm is presented in Fig. 19.

Reference identified harmonic current I_{fref1} and output filter current i_{f1} are almost superimposed as presented in Fig. 20.

Fig. 21.a presents main source voltage V_{s1} and current i_{s1} after harmonic current compensation. Spectral analysis is presented in Fig. 21.b. It is shown that source current is almost sinusoidal with THD less than 3% and unity power factor.

Simulation parameters

Main source:
$V_{ph-ph} = 4\text{kV}$, $R_{cc} = 0.0001\Omega$, $L_{cc} = 0.0009\text{H}$.

Induction motor:
$P_n = 1.2\text{MW}$, $\Omega_n = 1500\text{rpm}$, $T_n = 7.6\text{kNm}$, $V_{IM(ph-ph)} = 2300\text{V}$, $J = 46\text{kgm}^2$,
$R_s = 0.0406\Omega$, $R_r = 0.0308\Omega$, $L_r = 0.0591\text{H}$, $L_s = 0.0591\text{H}$, $M = 0.0581\text{H}$.

Active filter:
$R_f = 0.01\Omega$, $L_f = 0.002\text{H}$, $f_c = 6\text{kHz}$.

Clamping bridge of five-level APF:
$U_{cref} = 2050\text{V}$, $C = 0.05\text{F}$, $R = 5\Omega$.

Clamping bridge of three-level VSI:
$U_{crefi} = 2350\text{V}$, $C = 0.005\text{F}$, $R = 5\Omega$.

Three-level PWM rectifier:
$U_{crefr} = 4.1\text{kV}$, $L_r = 0.1\text{H}$, $R_r = 0.001\Omega$, $\varepsilon_k = 0.1\text{A}$.

6. Conclusion

In this paper, one studies the problem of unbalanced input capacitors DC voltages of five-level NPC shunt active power filter supplied by three-level PWM rectifier.

The modeling of the five-level NPC inverter shows that it is equivalent to four two-level inverters in series. The study of the instability problem of the input DC voltages of this converter shows that its different input voltages are not stables, which implies a bad harmonic current compensation.

To solve this instability problem, one proposes to use a clamping bridge filter to improve input DC voltages balance. In spite of this solution, the output voltages of three-level rectifier are not constant. To remedy to this problem, one proposes the feedback control of its output voltages. The application of the proposed feedback control algorithm to the rectifier shows a good voltage tracking.

Feedback control algorithm of the rectifier associated with clamping bridge filter makes stable the input DC voltages of five-level APF. Stable DC bus supply of sliding

mode controlled five-level NPC shunt APF allows getting low-harmonic content network currents with THD less than 3% and unity power factor.

The obtained results show that the proposed solution allows using this topology to compensate the harmonic current and reactive power in high power utilities.

References

[1] V.E. WAGNER: Effects of harmonics on equipment. *IEEE Trans. Power, Delivery*, **8** (1993), 672-680.

[2] C. HOCHGRAF, R. LASSETER, D. DIVAN and T.A LIPO: Comparison of multilevel inverters for static var compensation. *Conf. Rec. IEEE-IAS Annu. Meeting*, **3** (1995), 2557-2564.

[3] G. CHOE and M. PARK: A new injection method for ac harmonic elimination by active power filter. *IEEE Trans. on Industry Applications*, **35**(1), (1988), 141-147.

[4] S.M. DIGA, D. RUSINARU and A.C. GRIGORESCU: Aspects concernant la limitation des effets de la circulation des harmoniques dans les reseaux de distribution. *Annals of the University of Craiova, Electrical Engineering*, series, No. 30, (2006), 282-287, (in French).

[5] J.H. CHOI, G.W. PARK and S.B. DEWAN: Standby power supply with active power filter ability using digital controller. *Proc. IEEE APEC'95*, (1995), 783-789.

[6] S. BHATTACHARYA, D.M. DIVAN and B.B. BANERJEE: Active filter solutions for utility interface. *Proc. IEEE ISIE*, (1995), 1-11.

[7] S. SAETIEO, R. DEVARAJ and D.A. TORREY: The design, implementation of a three-phase active power filter based on sliding mode control. *IEEE Trans. Ind. Appl.*, **31** (1995), 993-1000.

[8] L. BOR-REN, H. ZONG-LIANG, T. SHUH-CHUAN and L. MU-SHAN: Shunt active filter with sliding mode control. *Proc. IEEE TENCON'OI*, **2** (2001), 884-889.

[9] T. ABDELKRIM and E.M. BERKOUK: Commande non linéaire par mode de glissement d'un filtre actif parallèle à sept niveaux. *Conférence Internationale Francophone d'Automatique CIFA*, Romania, (2008), (in French).

[10] O. ENGIN, K. MURAT and O. SULE: A novel control method for active power filter under non-ideal mains voltage. *Proc. IEEE CCA*, **2** (2003), 931-936.

[11] N. MENDALEK and K. AI-HADDAD: Modeling and nonlinear control of shunt active power filter in the synchronous reference frame. *Proc. Harmonics and Quality of Power*, **1** (2000), 30-35.

[12] R. GUPTA, A. GHOSH and A. JOSHI: Control of 3-level shunt active power filter using harmonic selective controller. *Proc. IEEE Power India Conference*, (2006).

[13] V. ABURTO, M. SCHNEIDER, L. MORAN and F. DIXON: An active power filter implemented with a three-level NPC voltage-source inverter. *IEEE PESC'97 Record*, **2** (1997), 1121-1126.

[14] B.R. LIN, H.K. CHIANG and C.H. HUANG: Three-phase three-level active power filter with a clamped capacitor topology. *IEE Proc.-Electr. Power Appl.*, **153**(4), (2006), 513-522.

[15] A. NABAE, I. TAKAHASHI and H. AKAGI: A new neutral-point-clamped PWM inverter. *IEEE Tran. On Ind. Appl.*, **IA-17**(5), (1981), 518-523.

[16] J.S. LAI and F.Z. PENG: Multilevel converters. A new breed of power converters. *IEEE Tran. On Ind. Appl.*, **32**(3), (1996), 509-517.

[17] V.F. CORASANITI, M.B. BARBIERI, P.L. ARNERA and M.I. VALLA: Comparison of active filters topologies in medium voltage distribution power systems. *Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century*, IEEE, (2008), 1-8.

[18] M. RASTOGI, P.W. HAMMOND and S.R. SIMMS: Multi-level active filter for medium voltage applications. *Int. Conf. on Power Electronics and Drives Systems*, **2** (2005), 1508-1513

[19] R.W. MENZIES, P. STEIMER and J.K. STEINKE: Five-level GTO inverters for large induction motor drives. *IEEE Trans. Ind. Applicat.*, **30** (1994), 938-944.

[20] J. RODRIGUEZ, D. RODRIGUEZ, C. SILVA and E. WIECHMANN: A simple neutral point control for three-level PWM rectifiers. *EPE*, Lausanne, (1999).

[21] F. BOUCHAFAA, E.M. BERKOUK and M.S. BOUCHERIT: Feedback control of DC link voltage of the back-to-back PWM multilevel converter. *J. of Electrical Engineering*, **58**(6), (2007), 318-325.

[22] F. BOUCHAFAA, E.M. BERKOUK and M.S. BOUCHERIT: Modelling and control of a power electronic cascade for the multi DC bus supply. *The Int. J. for Computation and Mathematics in Electrical and Electronic Engineering*, **27**(5), (2008), 1128-1143.

[23] N. HOR, J. JUNG and K. NAM: A fast dynamic DC link power-balancing scheme for PWM converter-inverter. *IEEE Trans. on Industrial Electronics*, **8**(4), (2001).

[24] F.Z. PENG and J.S. LAI: Dynamic performances and control of a static VAR generator using cascade multilevel inverters. *IEEE Trans. on Industry Applications*, **33**(3), (1997).

[25] R. GUEDOUANI, B. FIALA, E.M. BERKOUK and M.S. BOUCHERIT: Control of capacitor voltage of three phase five-level NPC voltage source inverter. Application to inductor motor drive. *Int. Aegean Conf. on Electrical Machines and Power Electronics*, Turkey, (2007), 794-799.

[26] N. CELANOVIC and D. BOROYEVICH: A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters. *IEEE Trans. on Power Electronics*, **15**(2), (2000), 242-250.

[27] S. SRIKANTHAN, M.K. MISHRA, B.K. KUMAR and K.S. BHASKAR: Capacitor voltage balancing in neutral clamped inverters for DSTATCOM application. *Int. Conf. on Power Engineering, Energy and Electrical Drives*, (2009), 558-563.

[28] R. STRZELECKI, C. BENYESEK and J. RUSINSKI: Analysis of DC link capacitor voltage balance in multilevel active power filters. *EPE*, Gratz, (2001).

[29] J.J. SLOTINE and W. LI: Applied nonlinear control. Englewood Cliffs, NJ: Prentice-Hall, UK, 1991, ISBN: 0-13-040890-5.

[30] V.I. UTKIN: Sliding mode control design principles and application to electric drives. *IEEE Trans. on Elect.*, **40** (1993), 23-36.