# Si-based 1.3 μm InAs/GaAs QD Lasers

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***Abstract*—The effects of implementing Ge and Si buffer layers on the performance of Si-based InAs/GaAs quantum dot lasers have been investigated in this paper. The laser performance has been improved significantly by utilising group-IV buffer layers.**

***Keywords—InAs/GaAs quantum dots, Molecular Beam Epitaxy, Semiconductor Lasers, Silicon Photonics***

## I. INTRODUCTION

Si photonic integrated circuits (PICs) are a frontrunner in developing a faster, cheaper, but more ubiquitous data transmission method which meets the high-demanding data traffic nowadays. However, the development of the Si light source is far behind other components and has long been considered the "holy grail" of Si photonics [1-4]. Although a great process has been made to grow high-performance InAs/GaAs quantum dot (QD) lasers on Si substrates [2], lasers with lower threshold current density and energy consumption but better performances at high temperatures are still desirable. To further improve the performance of Si-based InAs/GaAs QD lasers, we have been exploiting the usage of group-IV buffer layers, such as Ge and Si buffer layers grown on Si substrates to improve GaAs buffer layers grown on it, and hence improve InAs/GaAs QD laser performance.

## II. SAMPLE GROWTH AND CHARACTERISTICS

In this work, a twin-MBE system is utilised for the material growth, which consists of a group IV and an III-V growth chamber for the epitaxy of group IV and III-V materials, respectively. An ultra-high vacuum transfer chamber is used to connect both chambers, avoiding potential contamination during the wafer transfer process.

### *A. The Effects of Si buffer layers*

200 nm Si buffer layer was first grown on the deoxidised on-axis Si (001) substrate with a random miscut angle of 0.15°± 0.1° toward [110] orientation. This Si buffer consisted of a 100 nm Si layer annealed at 900 °C followed by 5 periods of 20 nm Si layers annealed at 1200 °C. In the subsequent GaAs growth, a three-step growth method was employed, and a 250 nm GaAs nucleation layer was first grown at a low temperature (LT) of 350 °C on the Si buffer. Then another 250 nm GaAs layer was deposited at a mid-temperature (MT) of 420 °C, followed by a 500 nm GaAs layer grown at a high temperature (HT) of 580 °C to complete the GaAs buffer growth.

To study the effects of the Si buffer layer, the GaAs buffer layers grown on Si substrates with different thicknesses have been grown with and without the Si buffer layer. The surface morphologies are shown in Fig. 1. For deoxidised Si substrate, randomly distributed Si steps without a clear step order appear on the surface [5]. During the growth of GaAs on the deoxidised Si substrate, antiphase boundary (APB) nucleation resembles the underneath Si *S* steps and has a random distribution, making APBs hard to annihilate with each other thoroughly during the intersection, as shown in Fig. 1(a) – (c). As a result, the APBs penetrate through the whole structure and severely degrade the crystal quality. By contrast, the parallel Si *S* steps formed during the Si surface reconstruction help redistribute APB nucleation. Consequently, the APBs that nucleate on parallel Si *S* steps form ordered arrays, as shown in Fig. 1 (d) and (e) [5]. The complete annihilation of APBs is enabled when APB propagation planes are reconfigured to higher index planes during the MT and HT GaAs growth, as shown in Fig. 1 (f).

The temperature-dependent LI measurement of the InAs/GaAs QD laser grown on the APB-free GaAs/Si (001) platform under pulsed operation is presented in Fig. 2 (a). The room temperature threshold current density is measured as low as 83.3 $Acm^{-2}$. Lasing up to 120 °C under pulsed operation is also achieved. The characteristic temperature $T_0$ is calculated as 55 K between 20 °C and 90 °C, and it decreases to 28 K from 100 °C to 120 °C as a result of carrier escape at higher temperatures, as shown in Fig. 2 (b). This poor $T_0$ is due to the undoped QD active region used. By implementing p-type modulation doping in the active region, the holes will be compensated, which contributes to the population inversion and enhances the temperature performance of the InAs/GaAs QD laser.

### *B. The Effects of Ge buffer layers*

30 nm Ge layer was first deposited on Si substrates at 250 °C. Then substrate temperature increased to 500 °C, and another 180 nm Ge layer was grown, followed by continuous *in situ* annealing for 30 min at 850°C. Finally, the substrate temperature was decreased to 600°C, and another 60 nm Ge cap layer was grown on the top to smooth the surface. The effects of Sb and B doping were also studied. We have demonstrated a high-quality 270 nm thick intrinsic Ge with a TDD of ~$6 \times 10^8$ $cm^{-2}$. A further reduction of threading dislocation density (TDD) for this thin Ge buffer layer is possible through Sb doping [6].

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Based on the Ge/Si virtual substrate (VS), the standard InAs/GaAs QD laser structure has been grown, consisting of 7-layer QDs. Fig. 3 (a) and (b) illustrate cross-sectional TEM images of TD propagation in III-V buffer layers directly grown on Si substrate and Ge/Si VS, respectively. A high density of TDs is generated at the GaAs/Si interface and Ge/Si interface due to a large lattice mismatch between materials. As shown in Fig. 3 (a), most defects generated at the GaAs/Si interface are confined within the first ~150 nm of the GaAs region. However, the TDs propagate freely upward before meeting the first DFL with a high-density value of ~$10^9$ $cm^{-2}$. In contrast, the TDs generated at the Ge/Si interface have a significantly lower density in the thin Ge layer, as shown in Fig. 3 (b). A final TDD of $4 \times 10^6$ $cm^{-2}$ is obtained after the four sets of DFLs, as indicated in the ECCI image of the GaAs surface shown in Fig. 3 (c).

The InAs/GaAs QD laser grown on Ge/Si VS has been tested at a range of operating temperatures, as illustrated in Fig. 4. The maximum operating temperature of 130 °C under pulsed operation has been achieved for the InAs/GaAs QD laser grown on Ge/Si VS. However, 130 °C is the upper limit of our temperature controller. Since no thermal rollover is noticed when the laser operates at 130 °C, it suggests this device can work at even higher working temperatures. The characteristic temperature $T_0$ is calculated as 153.4 K between 16 °C and 36 °C, and it decreases to 48.4 K from 36 °C to 130 °C as a result of carrier escape at higher temperatures, as shown in Fig. 4 (b).

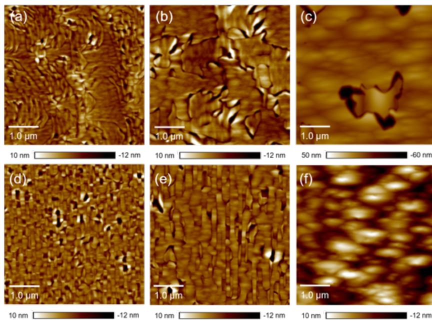


Fig. 1 5 × 5 μm² AFM images showing the surface morphology of (a) 250 nm, (b) 500 nm and (c) 1000 nm GaAs monolithically grown on deoxidised Si substrate. 5 × 5 μm² AFM image showing the surface morphology of (d) 250 nm, (e) 500 nm and (f) 1000 nm GaAs monolithically grown on Si buffer layer.

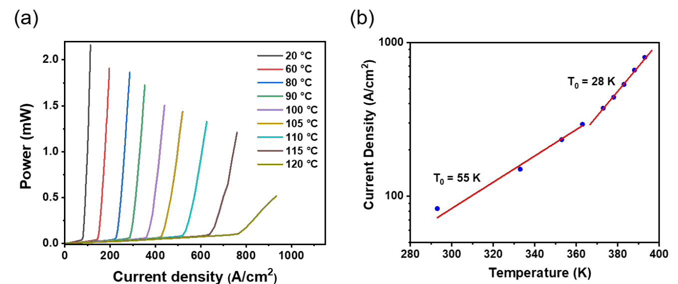


Fig. 2 (a) Temperature-dependent LI curve of InAs/GaAs QD grown on APB-free GaAs/Si (001) platform. (b) Corresponding characteristic temperature $T_0$.

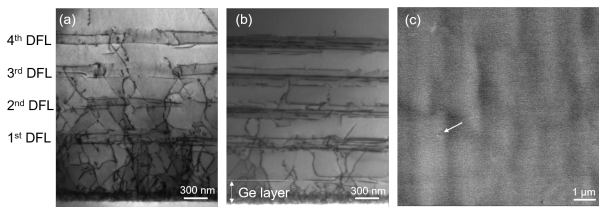


Fig. II Cross-sectional bright-field TEM results of (a) GaAs buffer layer grown on Si substrate and (b) GaAs buffer layer grown on Ge/Si VS. Both (a) and (b) have the same total thickness and consist of 4-set defect filter layers. (c) ECCI image showing TDD level for GaAs buffer layer grown on Ge/Si VS after 4th DFL. Arrow indicates a single threading dislocation observed on the surface.

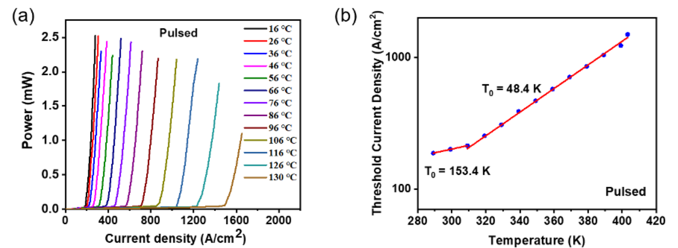


Fig.4 (a) Light output power against injection current density at various temperatures under pulsed operation. (b) Characteristic temperature measured under pulsed mode from 289 K to 409 K.

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