A Low Power, Low THD Current Driver with Discrete Common-Mode Feedback for EIT Applications

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***Abstract*—A low THD sinusoidal current driver for electrical impedance tomography (EIT) applications is proposed and analyzed in this paper. A discrete common-mode feedback method is proposed to increase the accuracy of the output current amplitude and output impedance. The current driver is designed in 65 nm technology under 3.3 V supply with a chip area of 0.0843 mm^2. The maximum output current amplitude is 1.2 mA. In simulations the current driver achieves an average THD of 0.098% at 1 mA output current amplitude and 500 kHz output current frequency. The simulated output impedance is higher than 4 MΩ at a load impedance lower than 3.5 kΩ. The current consumption of the circuit is 1.47 mA and provides a current efficiency of 81.6%.**

Keywords—Current driver, common-mode feedback, EIT.

I. Introduction

Electrical impedance tomography (EIT) is regarded as a promising technology for many clinical applications, including lung monitoring, cancer detection and hand gesture recognition [1]-[5]. A small alternating current (AC)is applied typically 1 to 5 mA rms to a domain (body) with a pair of electrodes. The resulting voltages are measured with another pair of the electrodes. This is repeated with a number of different set of electrodes on the domain to produce a set of independent measurement to produce an image. The phase shift and amplitude variation of the measured voltages, the real and imaginary parts of the tissue impedance can be calculated from the volage measurements.

For accurate impedance measurements using a low total-harmonic-distortion (THD) current driver with a high output impedance is required. A low THD current can provide accurate phase and amplitude measurements of the developed voltages. In addition, a high output impedance can guarantee a constant sinusoidal current amplitude delivered to loads that could vary from a few tens of Ohm to a few kilo-ohms.

Over the years, a large variety of current drivers have been proposed [2], [6]-[8]. Conventionally, current drivers can be classified into open-loop and closed-loop. Open-loop current drivers [6] have high output impedance and high power efficiency, but with limited THD performance and loosely defined transconductance. Closed-loop current drivers [7], [8] have good THD performance and well-defined transconductance due to feedback. However, they suffer from much higher power consumption and design complexity. A low power, low THD current driver based on current feedback instrumentation amplifier has been proposed in [2]; its schematic is shown in Fig. 1. Although the structure can provide a good trade-off between THD and power consumption, it has limited output impedance. In addition, since the impedance of pseudo-resistors have a large mismatch as high as 20% [9], the differential signal in positive and negative outputs cannot be cancelled effectively. As a result, there could be large oscillations at the output node depending on the load conditions. It also introduces extra noise and inaccuracy on the output current amplitude.

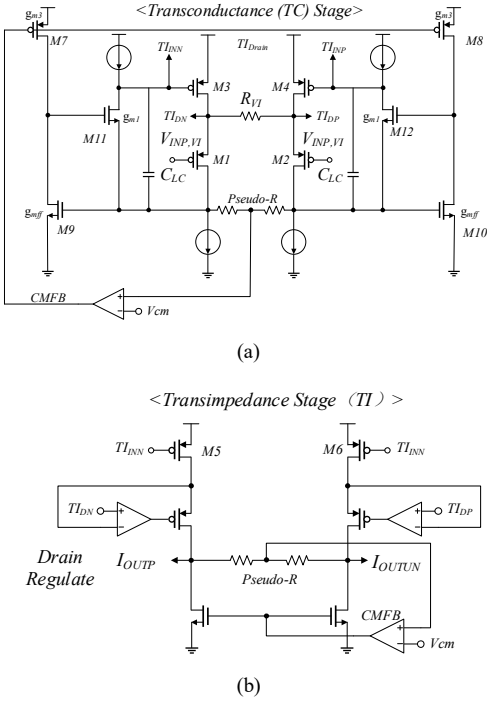

Fig. 1. Current driver proposed in [2]: (a) transconductance stage, (b) transimpedance stage.

This paper presents a new current driver shown in Fig. 2 with discrete common-mode feedback to decrease the oscillations at the output node without compromising the THD and power consumption. The output impedance has also been increased by adding cascode transistors. The paper is organized as follows. Section II describes the working principle of the proposed current driver. Section III presents simulation results. Section IV concludes the paper.

II. Circuit Overview

A. Operating Principle

As shown in Fig. 2, the proposed current driver has a transconductance (TC) stages for V to I conversion, and a

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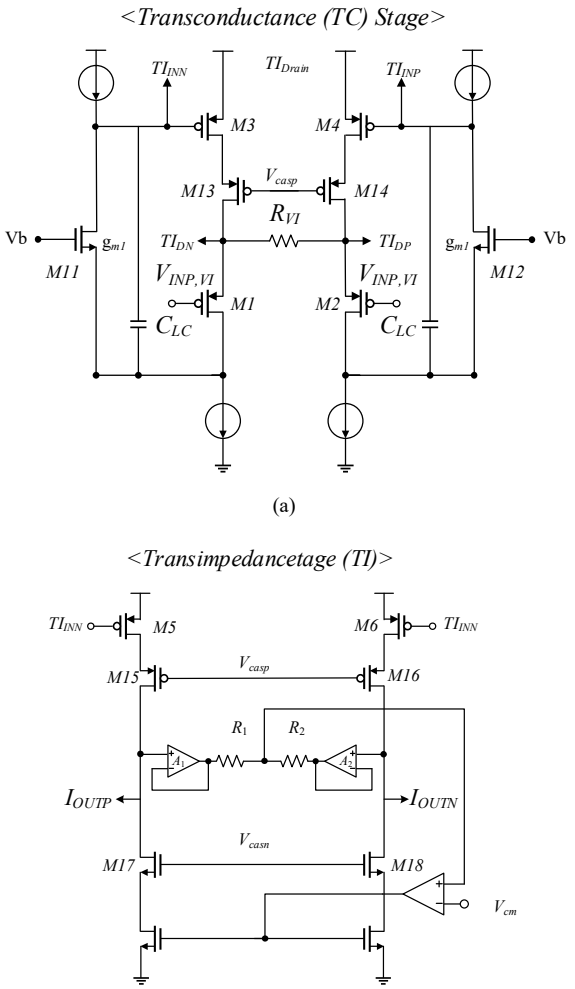


Fig. 2. Proposed current driver with discrete common mode feedback; (a) transconductance stage (b) transimpedance stage.

transimpedance (TI) stage for current amplification, similar to the working principle of classic current feedback IA. The input transistors, M1 and M2, of the TC stage act as source followers. The auxiliary amplifiers formed by M11and M12 at the TC stage increase the strength of local feedback of the source follower. As a result, the input differential signal is copied at each side of the resistor R_{VI}. This resistor converts voltage signals into current. Then, the current is copied to the TI stage by current mirrors, M3 and M5, M4 and M6. Transistors M7 and M8 in the TI stage work as a current mirror and force all the differential current signal to the output load. The output current amplitude is defined by $(V_{in}/R_{VI}) \times K$, where K is the aspect ratio between M3/M5 and M4/M6. Since the resistance of R_{VI} is a constant value, the voltage to current conversion will have very good linearity as long as the differential input signal is smaller than $2 \times R_{VI} \times I_{bias}$. By making the size of M5 and M6 much larger than the size of M3 and M4, this current driver can achieve a very good tradeoff between THD and power consumption.

B. Proposed Current Driver

As discussed in Section I, the current driver in [2] suffers from two drawbacks: 1) large DC voltage ripple at the output nodes due to the mismatch between the two pseudo resistors in common-mode feedback loop and, 2) limited output

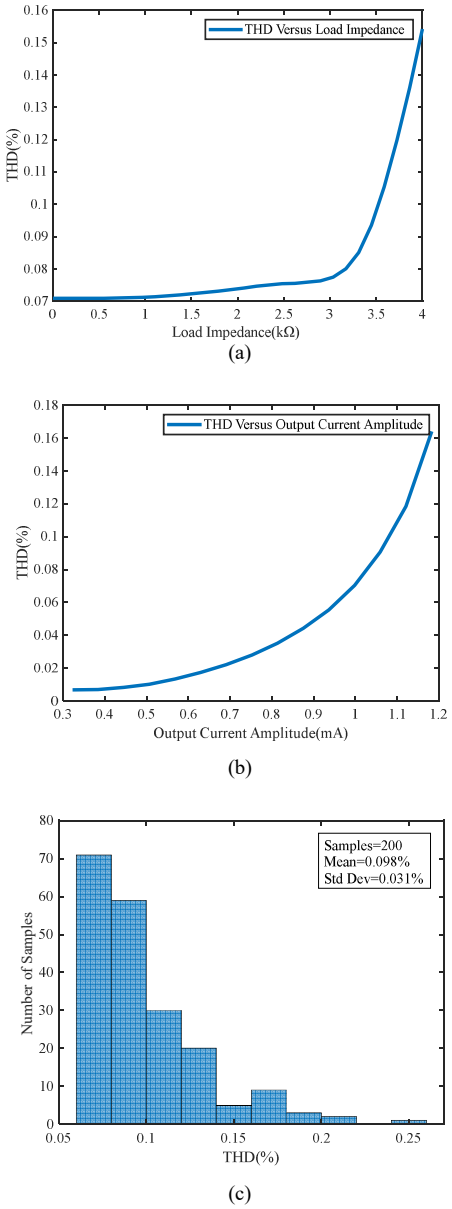
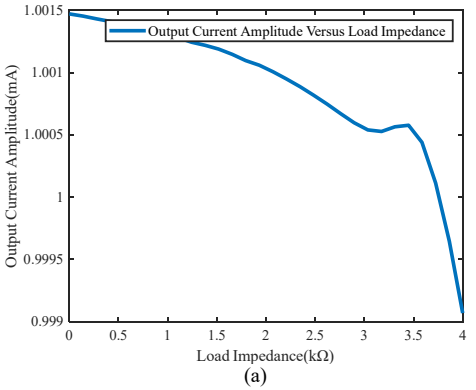
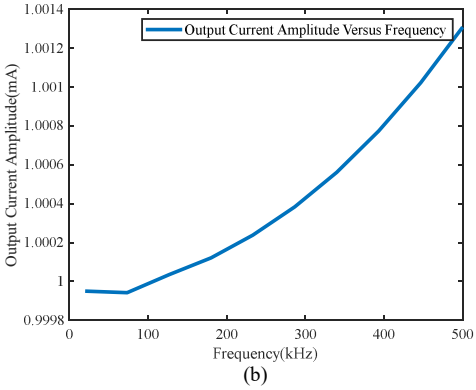


Fig. 3. (a) THD versus load impedance varying from 1 Ω to 4 kΩ at output current frequency of 500 kHz and amplitude of 1 mA. (b) THD versus output current amplitude varying from 0.3 mA to 1.2 mA at frequency of 500 kHz and load impedance of 1 kΩ. (c) Monte-Carlo simulation results of THD at 500 kHz, 1 mA output current frequency and load impedance of 1 kΩ.

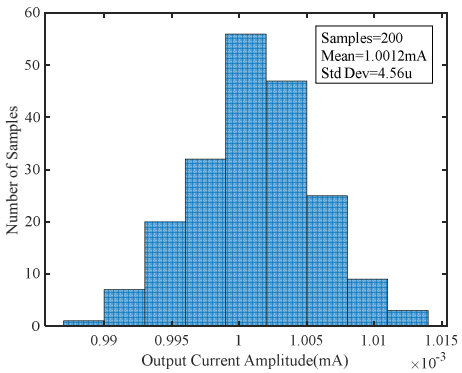
impedance. These drawbacks cause inaccuracy in the output current amplitude and thus decrease the measurement accuracy. Moreover, the gain-boosting circuits formed by M7, M8, M9 and M10 at the transconductance stage increase the design complexity due to extra transistors and extra common-mode feedback loop. The current driver proposed in this paper removes the gain-boosting stage to decrease the design complexity since the intrinsic gain of input pair M1, M2 and the auxiliary transistor M11, M12 is large enough. The output impedance has also been increased by adding cascode transistors M13, M14, M17 and M18 at both the TC and TI stages. As a result, the auxiliary amplifier for drain regulating in Fig. 1 can also be removed (resulting from the copied source voltages of M13/M15 and M14/M16), which further decreases the design complexity. Also, the linear



(a)



(b)



(c)

Fig. 4. (a) Output current amplitude versus load impedance varying from 1 Ω to 4 kΩ at output current frequency of 500 kHz. (b) Output current amplitude versus frequency at 1 kΩ load impedance. (c) Monte-Carlo simulation results of output current amplitude at load impedance of 1 kΩ and frequency of 500 kHz.

range is increased because of the copied source voltage. A discrete common-mode feedback method is proposed to decrease the output DC ripple. In conventional common-mode feedback, the two feedback transistors are connected to the two output nodes. Since the output impedance should be large enough to drive different load impedances (varying from few hundreds to few kilo-Ohm), the resistors for common-mode feedback are implemented by pseudo-resistors due to limited chip area. Since pseudo-resistors have large mismatch, the differential signal of the negative and positive outputs cannot be cancelled effectively, resulting in large DC ripple at the output nodes and an inaccuracy in the output current amplitude. As shown in Fig. 2, the pseudo-resistors have been replaced by two unit-gain buffers A_1, A_2 and two resistors R_1, R_2 to solve this issue. The unit gain buffer can be designed with the basic 5 transistor operational

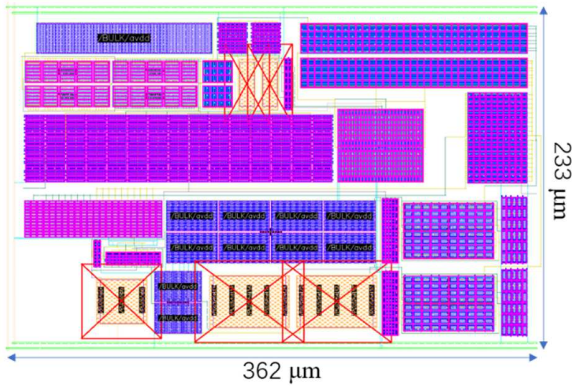


Fig. 5. Layout of proposed current driver.

amplifier with minimum power consumption and without increasing the design complexity. Since the common-mode feedback is achieved by the copied differential signals of unit gain buffers and there is no low-impedance node between the feedback resistors and output nodes, we call it *discrete common-mode feedback*. There are three benefits of this design. Firstly, the input of common-mode feedback loop is the gate of the buffer, which is considered to be high impedance node and would not affect the output impedance. Secondly, since the common-mode feedback transistors and output nodes of the current driver are separated by two unity gain buffers and would no longer affect the output impedance, the pseudo resistors can be replaced by normal resistors R_1 and R_2 with much smaller resistance (100 kΩ in this design) with higher matching, resulting in a much better differential signal cancellation, and thus, less ripple at the output node. Thirdly, the unit gain buffer itself can act like a low-pass-filter because of its limited bandwidth, which further reduces the differential signal. Consequently, this structure can provide accurate output current amplitude resulting from stable DC output node voltage and high output impedance.

III. Simulation Results

The proposed current driver has been designed in TSMC 65 nm CMOS technology with a 3.3 V power supply and maximum output current of 1 mA. The total current consumption is 1.47 mA. All results were simulated at a current frequency of 500 kHz and a load impedance of 1 kΩ.

A. Total Harmonic Distortion

Total harmonic distortion (THD) is one of the most important specifications to evaluate the performance of a current driver. Since THD is sensitive to the load conditions and transistor mismatch, different simulations are presented in Fig. 3 to provide a comprehensive performance evaluation. Fig. 3. (a) shows the THD with load impedance varying from 1 Ω to 4 kΩ at 1 mA and 500 kHz output current. According to the figure, the simulated THD is lower than 0.1% when the load impedance is smaller than 3.5 kΩ. It is suggested that THD will have a large increase when output impedance is higher than 3.5 kΩ due to the limited voltage compliance. THD variation as a function of the output current amplitude is shown in Fig. 3(b). The THD increases as output current increases but the THD is still lower than 0.2% when the output current reaches at 1.2 mA. Monte-Carlo simulation results with 1 kΩ load impedance and output current amplitude of

TABLE I. COMPARISON OF CURRENT DRIVERS

Parameter	[2]	[8]	[10]	[11]	This work
CMOS Process	65 nm	350 nm	350 nm	180 nm	65 nm
Supply Voltage	0.5 V	±2.5 V	±2.5 V	1.5 V	3.3 V
Max Output Current	1 μA_{p-p}	1.8 mA_{p-p}	500 μA_{p-p}	350 μA_{p-p}	1.2 mA_{p-p}
Output Impedance	N/A	>1 MΩ @ 3 MHz	160 kΩ @ 90 kHz	>100 kΩ @ 1 MHz	>4 MΩ @ 500 kHz
THD	0.088% @ 1 μA_{p-p}	0.4% @ 1 mA_{p-p}	0.79% @ 500 μA_{p-p}	<1% @ 250 μA_{p-p}	<0.1% @ 1 mA_{p-p}
Current efficiency	11.4%	60%	50%	26.2%	81.6%
Power consumption	4.38 µW	15 mW	5 mW	2 mW	4.85 mW

1 mA is shown in Fig. 3(c) to analyse the impact of transistor mismatch. A mean value of 0.098% and standard deviation of 0.031% is obtained from the simulation results.

B. Output Current Amplitude

The output current amplitude of this current driver is defined by V_{pp}/R_{VI}, where V_{pp} is the peak-to-peak value of input voltage. The accuracy of the output current amplitude determines the accuracy of the measured load impedance. It is affected by process mismatch, limited output impedance bandwidth of current driver and other factors. Fig. 4 shows the simulation results of the output current amplitude. In Fig. 4(a) the impedance is around 4 MΩ when the load impedance is smaller than 3 kΩ. The output impedance drops more rapidly when the load impedance is larger than 3 kΩ as a result of the limited voltage compliance. As shown in Fig. 4(b), the impact of frequency variation on the output current amplitude is very limited and can be ignored. Fig. 4(c) shows the Monte-Carlo simulation results of the output current amplitude at the frequency of 500 kHz and (ideal) amplitude of 1 mA. A mean output current amplitude of 1.0012 mA and standard deviation of 4.56 µA is obtained.

C. Layout and Post-Layout Simulation Results

The layout of the current driver is shown in Fig. 5. The total chip area is 0.0843 mm^2. The simulation results show an average THD of 0.0954% and an output current amplitude of 0.969 mA. The variation of the output current amplitude between schematic simulation results and post-layout simulation results is caused by parasitic resistors, which increase the value of R_{VI}. The current efficiency of this current driver is 81.6%. The current efficiency is calculated by the maximum output current amplitude over total current consumption.

IV. Conclusion

This paper has proposed a low power, low THD current driver with discrete common-mode feedback designed in TSMC 65 nm CMOS technology with 3.3 V power supply. It has a maximum output current amplitude of 1.2 mA. According to the simulations shown in Section III, the current driver achieves an average THD of below 0.1% at 1 mA output current amplitude. Table I provides a comparison with other work. The proposed current driver achieves the best trade-off between THD performance, output impedance and current efficiency.

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