ABSTRACT

Title of Dissertation:	ULTRA-THIN ON-CHIP ALD LIPON AS SOLID-STATE ELECTROLYTE FOR HIGH ENERGY AND HIGH FREQUENCY CAPACITOR APPLICATIONS
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Liquid electrolytes dominate the supercapacitor market due to their high ionic conductivity leading to high energy and power density metrics. However, with the increase in demand for portable and implantable consumer electronics, all solid-state supercapacitor systems with high safety are an attractive option from both application perspectives and their similar charge storage mechanism. For solid state ionic capacitors, there remains significant room for innovation to increase the ionic conductivity and capacitor architecture to enhance the performance of these devices. Nano-structuring along with advanced manufacturing techniques such as atomic layer deposition (ALD) are powerful tools to augment the performance metrics of these all-solid-state capacitors that can compete with state-of-the-art liquid electrolyte-based supercapacitors. This dissertation has two primary objectives; 1) Study the behavior of polymorphs of ALD LiPON as

a capacitor material and 2) Enhance the performance metrics using advanced materials and 3D nanostructuring for improved energy storage and high-frequency applications.

In this work, ALD LiPON-based solid state capacitors are fabricated with a gold current collector to study the behavior of the solid electrolyte. LiPON shows a dual energy storage behavior, in low frequency (<10 kHz), LiPON shows an ionic behavior with electric double layer type energy storage, beyond this frequency, LiPON shows an electrostatic behavior with a dielectric constant of 14. The capacitor stack's thin film structure and dual frequency behavior allow for extended frequency operation of these capacitors (100 Hz to 2000 MHz). Next, LiPON's energy storage metrics are enhanced by pseudocapacitive energy storage behavior and increased surface area using ALD oxy-TiN. Finally, new fabrication techniques and ALD recipes are developed and optimized for integration into 3D templates. For fabrication of these capacitors, the material's chemistry is analyzed, and ALD techniques are developed for deposition of electrode/electrolyte materials and current collectors into the 3D nanostructures. The intermixing during the ALD processes is studied to understand the behavior and reliability of these thin films. This work highlights LiPON characteristics as a capacitor material for high-energy and high-frequency applications. Though incomplete, we discuss progress towards the development of all ALD solid-state 3D supercapacitors that can compete against state-of-the-art capacitors available in the market.

ULTRA-THIN ON-CHIP ALD LIPON CAPACITORS FOR HIGH ENERGY AND HIGH FREQUENCY APPLICATIONS

by

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Dedication

To my parents, sister, and grandmom.

Acknowledgements

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Chapter 1: Introduction

1.1 Motivation

The move towards miniaturization of electronics and efficient storage of energy is one of the major target for the academic as well as the industrial community of the 21st century. With an increase in usage for emerging technologies such as electric vehicles, biomedical devices, autonomous sensors, and portable electronic devices, the need for efficient electronic circuit have also increased.[1,2] This growing demand for miniaturization of electronic circuit not only apply to integrated chips but also needs passive technologies which can cater the needs of the superfast transient current response and high energy storage with minimum losses.[3,4] Capacitors are once such passives which are used in every electronic circuit and has a variety of applications such as power conditioning, noise filtering, signal coupling and decoupling, and energy storage.[5,6] Supercapacitors in particular are a class of capacitors which have high energy density and are used for energy storage and power condition application. However, a major concern with supercapacitor technology is safety due to the flammability and reactivity of their organic solvents.[7,8] Also, most of these capacitors with liquid electrolyte either work on DC or limited to low frequency response (<1000 Hz). This limits their application into the wearable and implantable electronics where safety and fast response is of prime concern. All solid state ionic capacitors are viable solution for energy storage based on their safety advantage over liquid electrolytes. Another advantage of solid state ionic capacitor is their high temperature and voltage

stability along with high power density.[9,10] Beyond their physical and chemical properties, the easy of manufacturing and packaging with growing demand of miniaturization makes them a perfect candidate for next generation supercapacitor devices.

1.2 What are Capacitors?

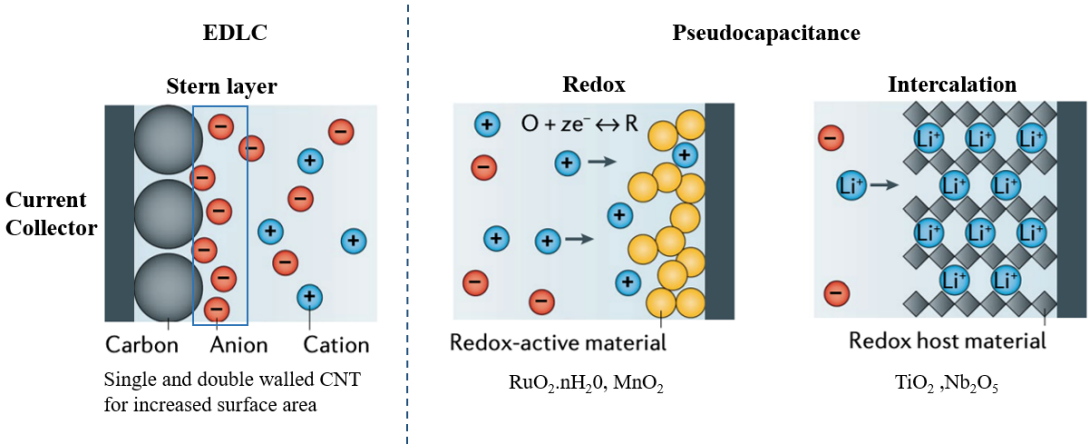

Figure 1: Supercapacitors based on charge storage, EDLC and Pseudocapacitance11

Capacitors are devices that consist of two or more parallel plates separated by an electronically insulating material called the dielectric/electrolyte. Generally, they store energy through in two ways. First, and most common, is through charge separation between two metal plates in an electric field. Second is through electrochemical surface reactions or intercalaction.[11–13] Supercapacitors are devices that have a higher capacitance than the conventional capacitors and are used for applications that require higher energy. Supercapacitors can be divided into two categories based on charge storage mechanisms; electric double-layer capacitors (EDLC) and pseudocapcitors (Figure 1). The EDLC stores charge at an electrode-

electrolyte interface through the adsorption of ions. An electrical double layer is formed at the interface when a voltage bias is applied across an EDLC. The double-layer consists of a stern and diffuse layer. The thickness of these layers depends on the ionic concentration and is on the order of 5-10Å. Charge separation in the stern and diffuse layer leads to a high electric field due to its low thickness and thus energy stored in an EDLC is higher than conventional capacitors. Pseudocapacitors involve fast faradaic reactions and intercalation of ions into an electrode material. This faradaic reaction stores charge in the form of chemical energy, and hence they have a higher capacitance and higher energy densities.

1.2.1 Thin Film Solid State Ionic Capacitors

One of the major advantages of solid state electrolyte is their inherent safety and stability and thus allowing their use in applications such as implantable and wearable electronics. However, a huge challenge preventing their application for next generation energy storage devices is due to their low ionic conductivity and high interfacial impedance. Thin-film processing presents one method to alleviate this concern, where thin layers (<100 nm) do not require high ionic conductivity comparable to the liquid electrolyte (1 mS/cm) and reduce interfacial impedance.[14–17] Another advantage associated with thin film capacitors is their low parasitic inductance and resistance thus allowing for enhanced frequency operation of these capacitors.[18] In spite of thin film configuration, the energy density of the planar solid state ionic

capacitor configuration remains a huge challenge and limits its use to applications with limited energy metrics.

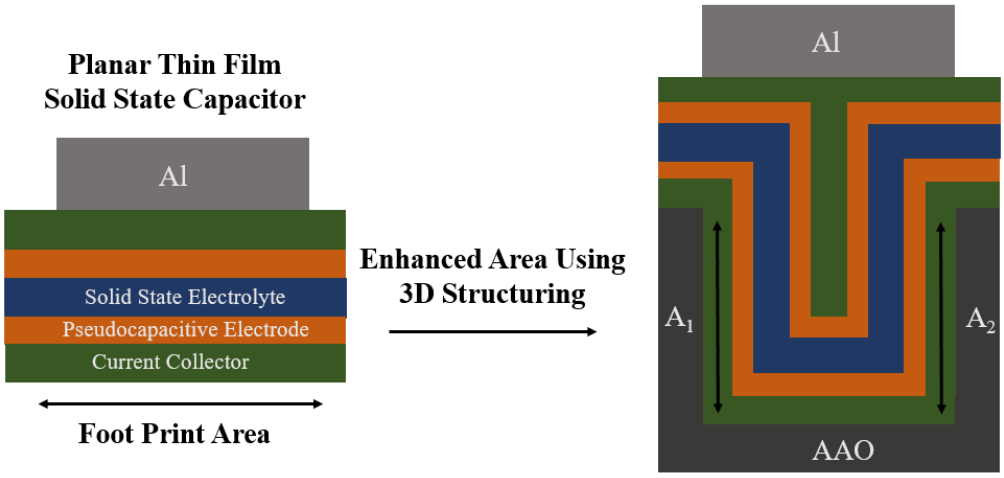

Figure 2: 3D structuring to enhance energy and power density metrics

To enhance the energy and power density of these thin film capacitors, one way is to the change the architecture as shown in Figure 2. The 3D structuring enhances the effective area although the footprint area remains constant. The areal enhancement can be quantitatively defined by the area enhancement factor (AEF = A/A_f), which represents the ratio of the internal surface area, A, to the footprint area, A_f, of the substrate. However, the standard manufacturing techniques such as sputtering might face conformality problems in 3D architecture.[19] Thus, to enhance the performance of these capacitors it not only requires thin films but advanced manufacturing techniques to enable deposition of these thin films.

1.3 Literature Survey: Solid State Electrolyte

1.3.1 Polymer Electrolyte

Solid-state electrolytes can mainly be classified into polymer electrolytes and inorganic electrolytes. Polymer-based electrolytes are further classified into three basic types, (1) gel-based, (2) solid-state, and (3) polyelectrolyte. A diagram of each can be found in Figure 3 (a-c). Solid-state polymer electrolytes, Figure 3 (a), consist of a polymer and salt mixture, with their ionic conductivity based on the transport of ions inside the polymer matrices while the polyelectrolytes (Figure 3 (c)) have charged polymer chains which are responsible for their ionic conductivity. In contrast, gel polymer electrolytes (Figure 3 (b)) contains a solvent with conducting salt inside the polymer host. Ion transport takes place inside the solvent and hence they have higher ionic conductivity than solid polymer electrolytes. Since gel electrolytes have superior ionic conductivity and high flexibility, they are the most common supercapacitor electrolytes.[20–24]

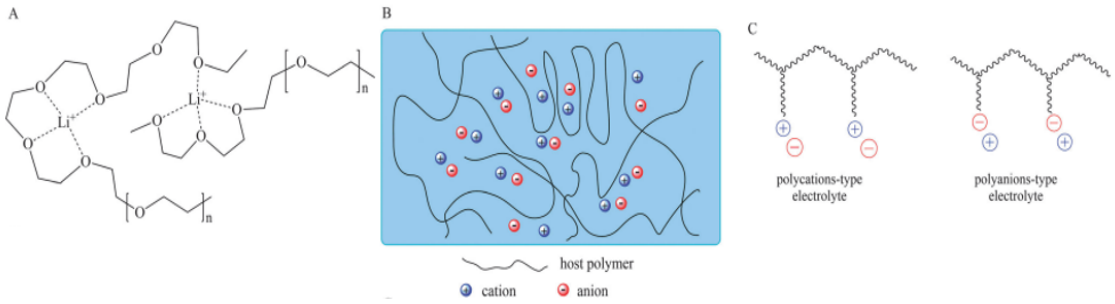

Figure 3:P Schematic diagrams of (a) a dry solid polymer electrolyte (b) gel polymer electrolyte, and (c) a polyelectrolyte[22]

Table 1 shows gel electrolyte supercapacitors with high energy and power density, but a significant drawback of these electrolytes is poor mechanical strength, leading to short circuits and safety issues. Gel polymer electrolytes cannot be operated in a wide temperature range as solvents dry up at extreme temperatures. Also,

miniaturization remains a major issue in gel polymer electrolytes as it is hard to make devices down to nanoscale thickness with high conformality and rigidity. Thus, with safety being a primary concern, polymer gel electrolytes are not suitable for supercapacitor applications which demand high-temperature stability (>70°C) along with high mechanical strength at low thicknesses (<100nm). [25,26]

Table 1: Gel polymer electrolyte used in supercapacitors

Electrolyte	**Capacitance**	**Energy Density**	**Power Density**
PVA/KOH/K_3[Fe(CN)$_6$][27]	430.95 F/g	57.84 Wh/kg	59.84 kW/kg
PVA/H_2SO_4/P-benzenedio][28]	474.29 F/g	10 Wh/kg	1000 W/kg
PVA/H_3PO_4/H_2O[29]	108 F/cm^3	7.5 Wh/cm^3	2.9 W/cm^3
CMC/Na_2SO_4[30]	92 F/g	41 Wh/kg	1276 W/kg
PVA/ $LiClO_4$[31]	145 F/g	41 Wh/kg	2.1 kW/kg
PVA/LiCl[32]	0.52 F/cm^3	0.234 mWh/cm^3	0.133 W/cm^3
PVA/KOH[33]	4.28 F/cm^3	1.21 mWh/cm^3	13.29 W/cm^3
PMMA/$LiClO_4$[34]	270 F/g	9.8 Wh/kg	0.85 kW/kg
PVP/ Na_2SO_4[35]	N/A	24.8 Wh/kg	120 W/kg
PAAK/KCl[36]	72.6 F/g	32.7 Wh/kg	N/A

1.3.2 Inorganic Solid State Electrolyte

Inorganic electrolytes consist of ceramic and oxide materials. A significant advantage of inorganic electrolytes is their high thermal stability, high mechanical strength, and a higher electrochemical stability window. Their ionic conductivities very widely but are generally considered to be lower than liquid and polymer counterparts. Their high rigidity compared to solid state polymer electrolytes, makes them an excellent material for thin film supercapacitor applications. Unlike polymer gel electrolytes, they don't suffer from problems related to solvent drying and hence reduce packaging cost.[21,25] Table 2 shows some state-of-the-art inorganic electrolytes with their respective ionic conductivities. These inorganic electrolytes have shown excellent characteristics in battery performance, but their application in capacitors has yet to be studied intensively.

Table 2: Inorganic SSE and their ionic conductivity

Solid Electrolyte	**Ionic Conductivity (S/cm)**
Perovskite[37–39]	10^{-4}-10^{-3}
NASICON[40–42]	10^{-4}-10^{-3}
Garnet[43–46]	10^{-6}-10^{-3}
Amorphous Li_2S-P_2S_5[47,48]	10^{-4}-10^{-2}
Thio-LiSiCON[49–51]	10^{-2}
LiPON[52–56]	10^{-8}-10^{-5}
Hydride[57,58]	10^{-7}-10^{-2}

Halide[59]	10^{-8}-10^{-3}

Table 3 shows a brief survey of inorganic SSE for capacitor applications. NASICON-type SE ($Li_{1.4}Al_{0.4}Ti_{1.6}(PO_4)_3$)) (LATP), which have a high ionic conductivity (10^{-4} S/cm) was sandwiched between two nanostructured electrodes which incorporate single-wall carbon nanotubes mixed with LATP.[60] LATP shows EDLC behavior, and the highest capacitance measured was 11 mF/cm^3 at 0.01Hz. However, a major drawback is that the capacitance reduces drastically with an increase in frequency. At less than100Hz, the material loses its electric double layer behavior and acts as an electrostatic capacitor with high impedance.

Table 3: Inorganic SSE for supercapacitors

Electrolyte	**Electrode**	**Capacitance**	**Voltage**	**Comments**
NASICON:LATP[61]	Au with Carbon coating	0.13 F/cm^2	0.8 V	Porous/dense/porous using carbon to enhance capacitance
NASICON:LATP[60]	LATP with CNTs	11 mF/cm^3	0.5 V	Porous dense porous to enhance surface area at the interface
Li_2S-P_2S_5[62]	Carbon paper with MWCNTs	8.7 mF/cm^2	0.5 V	Electrolyte formed using heat treatment

$0.4LiClO_4$-$0.6Al_2O_3$[25]	$LiMn_{1.5}Ni_{0.45}Mg_{0.05}O_4$, Mn_2O_3,MnO	29 F/g	2 V	High temperature stability :150 C
Graphene Oxide[63]	Reduced graphene oxide	3 mF/cm^2	1 V	Water trapped inside the graphene oxide serves as ion conductor
LiPON[64]	Platinum	50 uF/cm^2	3 V	High cycling stability, high voltage window
LiPON[65]	Cobalt/Cobalt oxide	15 F/cm^3	2 V	High temperature stability 90C

In another work, LATP shows a capacitance of 50 uF/cm^2 with gold as the current collector, but the capacitance shows a limited voltage stability window of 0.8V, limiting the capacity and hence energy density.[61] Li_2S-P_2S_5 , a ceramic, has been investigated as an electrolyte.[62] The electrolyte is prepared by heat treatment of Li_2S and P_2S_5, and the resulting mixture has an ionic conductivity of 1 mS/cm. The electrolyte shows an EDLC behavior with a high capacitance of 8.7 mF/cm^2. Also, the capacitor showed a small electrochemical voltage stability window of 0.5V.

Finally, initial studies have investigated lithium phosphorous oxynitride (LiPON) as SSE for supercapacitors. In one study, 140 nm of LiPON was sputtered using Li_3PO_4-Li_2O as the target on platinum electrodes. A high capacitance of 50 uF/cm^2 was achieved and showed an excellent voltage stability window of up to 3V

between platinum electrodes.[64] In another study, 20 nm of LiPON was sputtered using a Li_3PO_4 target in a nitrogen atmosphere. The resulting LiPON was sandwiched between Cobalt/Cobalt oxide electrodes and showed a high capacitance and high energy density. The paper also reports the flexibility of LiPON and exhibits stability at high temperature (90°C).[65] Though sputtered LiPON shows high voltage stability, high-temperature stability, and mechanical stability, a major problem is low energy and power density compared to liquid electrolytes. Also, sputtering possesses conformality problems limiting the growth of SSE into 3D architectures.

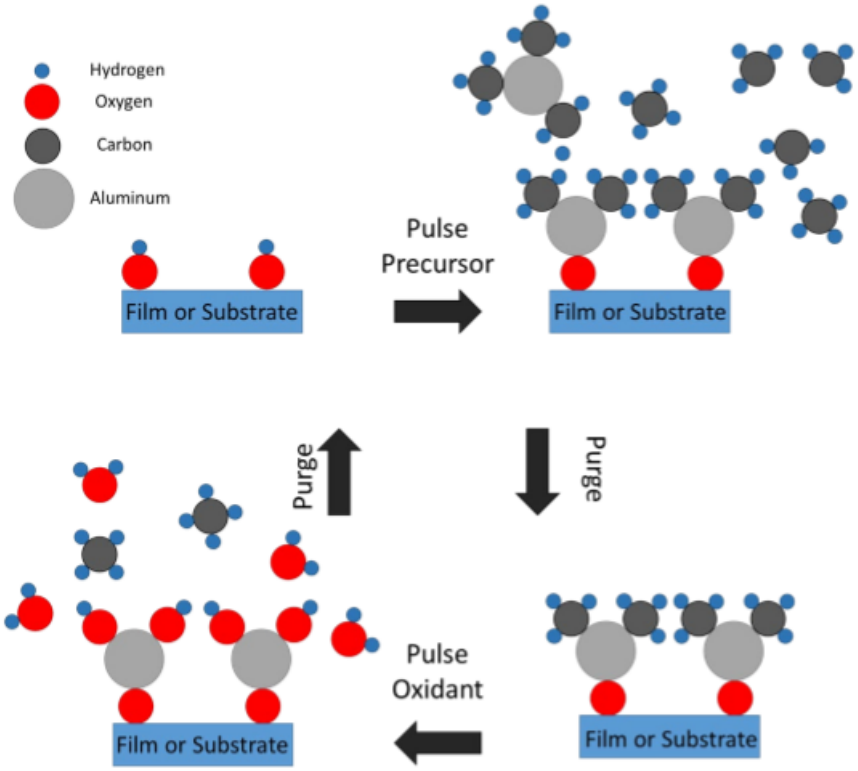

Figure 4: Reaction Scheme of ALD Aluminum Oxide process

In contrast, atomic layer deposition (ALD) is a technique that allows deposition of thin film materials from vapor phase. It consists of sequential alternating pulses of gaseous chemical precursors that reacts with the substrate. Each individual gas-surface

reactions make up only part of the materials synthesis. During each reaction, the precursor is allowed to fully react with the substrate surface through a self-limiting process that leaves no more than one monolayer at the surface. Thus, ALD offers precise control of thickness and composition of the material. Along with confirmability and uniformity on 3D surfaces, the remarkable selectivity and superior scalability make it an excellent choice for synthesizing SSE for supercapacitor applications.[66] One of the most common ALD process is the thermal growth of aluminum oxide using trimethyl aluminum (TMA) and water and the process is shown in Figure 4. The reaction on a substrate with OH termination is described below.[67]

$$-OH^{*} + Al(CH_3)_{3(g)} \rightarrow -O-Al(CH_3)_2^{*} + CH_{4(g)}$$

$$-O-Al(CH_3)_3^{*} + H_2O_{(g)} \rightarrow -O-Al-OH^{*} + CH_{4(g)}$$

1.4 Atomic Layer Deposition of LiPON

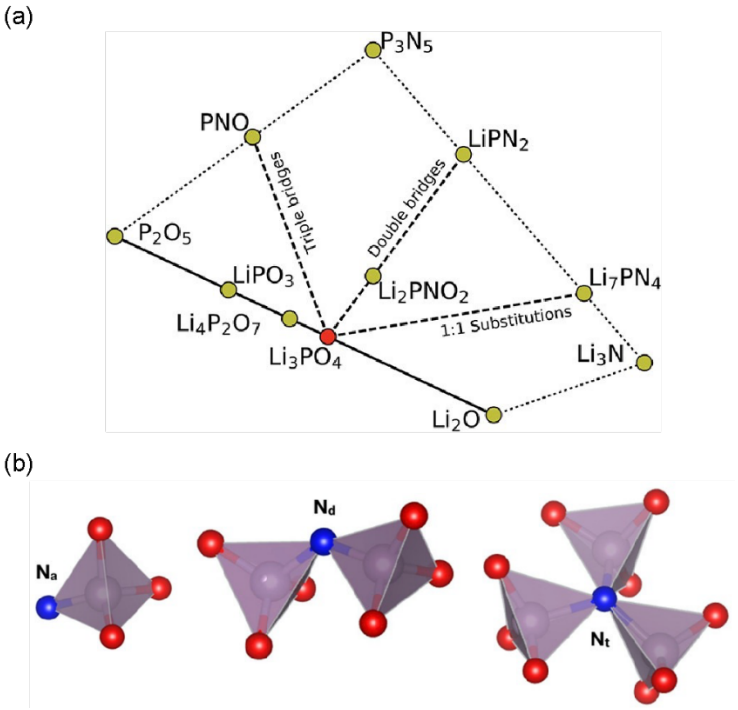

Figure 5: (a) Phase diagram showing LiPON compositions in the LixPOyNz space. (b) Possible N binding environments in LiPON structures. Na is apical N, Nd is doubly coordinated N, Nt is triply coordinated N. Color code: N (blue), O (red), P (gray). From Lacivita68

LiPON is an inorganic glassy material commonly used as a thin film solid electrolyte in soild-state batteries (SSBs) with a general formula of $Li_xPO_yN_x$. It was first developed at Oak Ridge National Laboratory via sputtering.[52] The LiPON structure is based on Li_3PO_4 metaphosphate chain with nitrogen doping which is either doubly (N_d, P-N=P) or triply (N_t, P-N<P) coordinated. Recent molecular dynamic simulation study from Lacivita et al.[68] suggests nitrogen as singly coordinated or apical nitrogen (N_a, P-N) in the LiPON structure. Due to different nitrogen bridging, many polymorphs of Nitrogen exists as shown in Figure 5 (a). The different nitrogen configurations with phosphate units are shown in Figure 5 (b). The high incorporation of nitrogen into the LiPON film is associated with high ionic conductivity due to decreased electrostatic interactions of the P-O bond and replacement with a covalent P-N bonds.[69,70]

ALD LiPON was first developed at UMD by the Rubloff group. Since, three ALD LiPON recipes have been developed with different precursors combinations and different growth windows.[53–55] Table 4 shows the deposition of ALD LiPON with different precursors and their respective growth per cycle along with the reported ionic conductivity. In this work, we have studied plasma ALD LiPON and thermal ALD LiPON previously developed by our group.

Table 4: ALD parameters for different polymorphs of LiPON

Chemical Formula	ALD temperature (°C)	Precursor	Growth per cycle (GPC) (A)	Ionic Conductivity (S/cm)
$Li_{0.99}PO_{2.55}N_{0.30}$ [53]	250	LiO^{t}Bu, H2O, TMP	0.7-1.05	3×10^{-7}
Li_2PO_2N[54]	300	LiO^{t}Bu, DEPA	0.6-0.9	6.51×10^{-7}
LiPON[55]	300	LiHMD, DEPA	0.7	ND

1.5 Dissertation Overview

In this dissertation, we explore ALD LiPON based solid-state capacitors that can provide high energy density and power density for next-generation applications. Different ALD LiPON polymorphs are investigated with reasonable high ionic conductivity and high-temperature stability for better-performing supercapacitors. Further, the solid electrolyte capacitors are characterized based on their electrochemical

working potential, frequency, and leakage currents to define their application range. Also, the electrochemical stability of solid electrolytes is tested with different electrode materials to expand the energy density of the capacitors using pseudocapacitive behavior. Finally, we investigate and develop ALD recipes, fine tune process parameters and develop etching techniques to fabricate all solid state 3D capacitor.

Chapter 2: Experimental Techniques

2.1 Advanced Nanostructures Laboratory (ANSLab)

ANSLab is one of a kind highly equipped laboratory with state of the art tools for manufacturing, characterizing and testing materials and devices which are air sensitive with a focus of applications related to solid state batteries/supercapacitor and other microelectronic devices. It consists of advanced thin film deposition tools, surface analysis instruments which are coupled using Ar-filled glove box and ultrahigh vacuum chamber. A schematic describing the state of the art tools with their respective position and integration with other equipment is shown in Figure 6. It consists of two ALD reactors, Veeco Fiji F200 which are named as Luigi and Mario respectively. All the thin film depositions done in this thesis mainly for solid electrolyte and capacitor fabrication is done using Luigi. An ultra-high vacuum chamber connects Luigi to the glove box. The glove box is also coupled to the RTTA chamber on the other side which has 8-inch pneumatic gate valves that connects to the evaporation chamber, the Krataos Ultra DLD surface analysis system and the other ALD reactor "Mario". An advantage of this coupled system is that it allows for testing, fabrication along with surface analysis without air exposure. The RTTA system consist of a robotic arm which can transfer 3-inch wafers for fabrication and testing into different tools attached to it. The glove box is mainly used for transferring samples and precursors from atmosphere into the inert atmosphere and storing them. Another key advantage of glove box is that it has the biologic potentiostat for testing and characterizing materials and microelectronics. Along with this, the glove box has a custom-built evaporator attached

for Li, Na and Mg metal evaporation. These coupled systems along with all the fabrication and characterization tool makes ANSLab a highly advanced research facility at UMD.

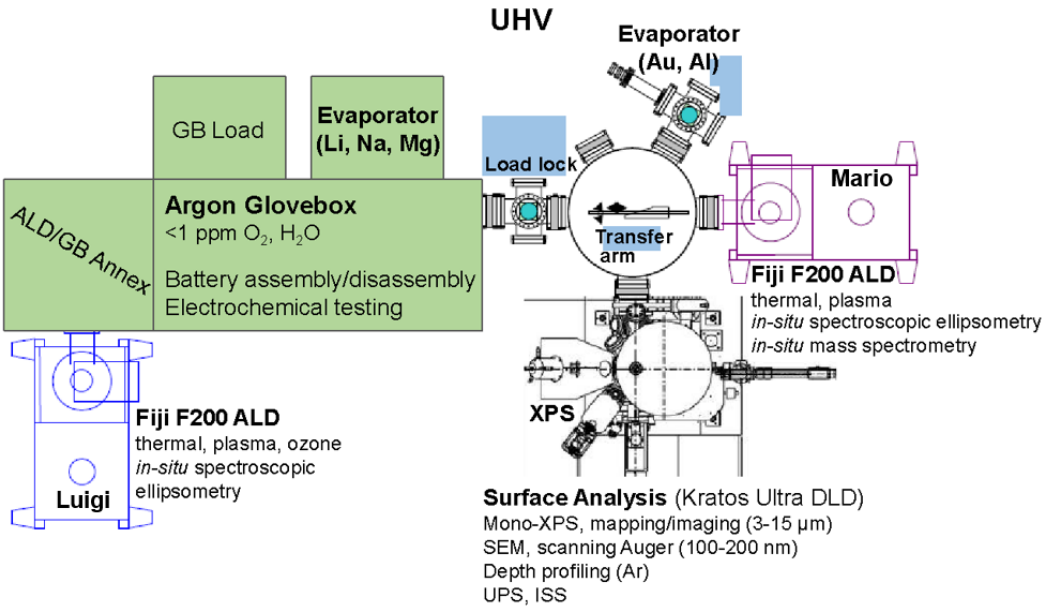

Figure 6: Schematic of ANSLab equipment used to fabricate, characterize, and evaluate materials in this dissertation

2.2 Atomic Layer Deposition

In this dissertation, the primary deposition technique used is ALD which allows for growing thin film coatings with high conformality and ultra-high purity. The ALD process parameters varies with different materials and substrates and is defined in each chapter where the reactor is used for depositions. In this research ALD is used to deposit different polymorphs of LiPON, TiN and TiO_2. The Luigi ALD reactor is used for all the depositions and is shown in Figure 7. An advantage of Luigi is that it has an in-operando spectroscopic ellipsometry that allows for thickness control at angstrom scale. This along with coupled glove box and RTTA tool allows for complete analysis of thin film devices.

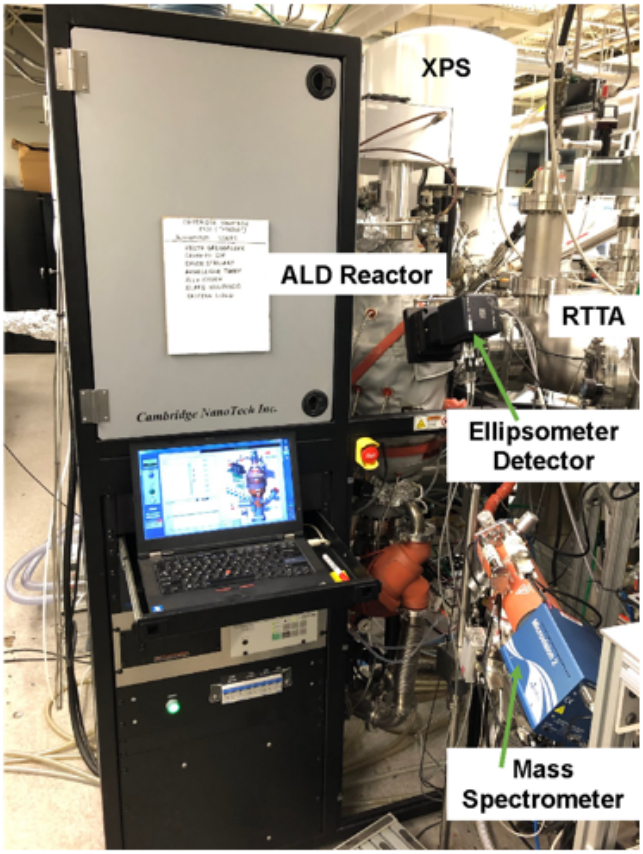

Figure 7: Fiji-F200 ALD Reactor (Mario) in ANSLab. Mario is equipped with in-line mass spectrometry sampling and in-operando spectroscopic ellipsometry. ALD films can be transferred directly to a surface analysis system for XPS through the RTTA UHV transfer chamber

2.3 X-ray Photoelectron Spectroscopy (XPS)

XPS is one of the most used characterization technique used in this thesis to understand and confirm the chemical structure of the solid state electrolyte and electrodes. One of the key elements of XPS is surface sensitivity which makes it the perfect choice for analyzing the chemical composition of thin films deposited using ALD. Another advantage of our XPS tool is its construction into the ANSLab which allows for characterizing pure ALD films without air exposure.

The XPS works on the photoelectric principal which was first proposed by Einstein in 1922.[71] In this technique, X-rays are irradiated on the sample and the analyzed detects the kineteic energy of electrons which are emitted from the top surface. The binding energy of the emitted electron is calculated using conservation of energy equation as shown in equation below.

$$E_{binding} = h\nu - E_{kinetic} + \phi$$

where, $E_{binding}$ is the binding energy of the excited electron, $h\nu$ is the photon energy, $E_{kinetic}$ is the kinetic energy of the excited electron, and φ is the work function of the material. The work function term defines the instrument correction factor and that is different for different working conditions and instruments. The calculated binding energy is then used to analyze the material and their respective oxidation state. This allows for calculating the overall stoichiometry of the thin films along with their bonding structure.

Figure 8 shows the Kratos surface analysis tool that is installed in our lab. Every film was characterized using XPS to analyze their chemical structure to conclude deposition on different substrate material and analyze results. For characterization of ALD films, the films were transferred into the Kratos tool without air exposure. Preventing air exposure is a critical parameter to understand thin films and their interfaces as it allows for accurate material characterization which are air sensitive.

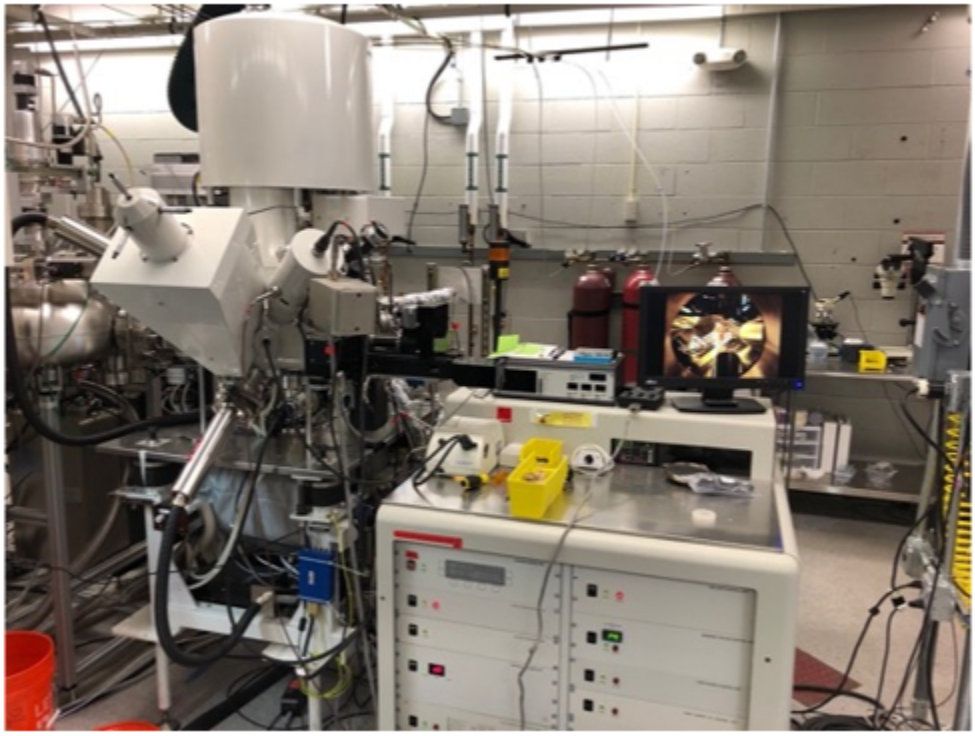

Figure 8: Kratos Ultra DLD surface analysis system in ANSLab used for XPS measurements

2.4 Spectroscopic Ellipsometry

The capacitor fabrication along with process development of each thin film relies on in-operando ellipsometry which is attached to the Luigi tool in ANSlab. Ellipsometry not only allows for thickness measurements but also quantifies process development. The precursor doses and purge time is determined using ellipsometry. It also allows for angstrom level thickness control and thus allows us to deposit thin films with high accuracy and conformality to our specifications.

The ellipsometry analyzed measures the change in polarization of light as it interacts with the surface of the sample. This is correlated to the film thickness using various optical models.[72] The polarization of light is described by the equation below.

$$\tilde{p} = \frac{\tilde{r}_p}{\tilde{r}_s} = \frac{|\tilde{r}_p|}{|\tilde{r}_s|} e^{i(\delta_p - \delta_s)} = \tan tan \Psi \, e^{i\Delta}$$

where r_p *and* r_s are the Frensel reflection coefficients for the p- and s- polarized light, respectively. The amplitude ratio (Ψ) and phase difference (Δ) are measured dynamically across the spectral range (200-2000 nm) throughout the deposition process and are correlated to film thickness through optical models. A J.A. Woollam M-2000D spectroscopic ellipsometer was used for *in-operando* and *ex-situ* measurements of samples in this work.

2.5 Dry Reactive Ion Etch (DRIE)

DRIE technique is used to fabricate planar 2D capacitors or 3D capacitors by etching the top current collector. We used an Oxford Plasmalab System 100 too; which is an inductively Coupled plasma (ICP) reactive ion etcher. Though this tool uses a variety of gas for selective etching. In this work we used Ar ion milling and developed our own recipe. We used the plasma along with various flow of Ar ions at different ICP power. The recipe was developed using spectroscopic and XPS analysis. Timed etches were performed to further quantify the etch rates. Chapter 5 discusses the recipe development process in detail.

2.6 Electrochemical Analysis

This research work is highly dependent on electrochemical analysis for evaluating the performance of materials and solid-state capacitors. A biologic VSP was used in this work to test the capacitors in 2D and 2D configuration. A picture of the

biologic VSP along used for electrochemical analysis is shown in figure 2.4(a). Electrochemical tests include electrochemical impedance spectroscopy (EIS), cyclic voltammetry (CV), and galvanostatic capacitor cycling measurements. Figure 9 (b) shows an image of a LiPON capacitor undergoing electrochemical testing on a custom probe station inside the Ar glovebox. It is critical to evaluate such SSEs in the glovebox to avoid air-exposure for precise determination of electrochemical properties.

(a) (b)

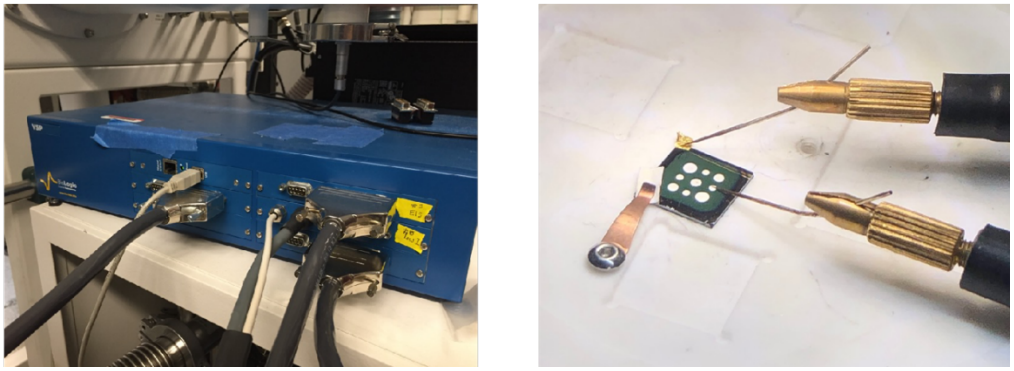

Figure 9: (a) Biologic VSP potentiostat (b) LiPON SSE undergoing electrochemical testing[72]

The first characterization and one of the most important to evaluate thin films is electrochemical impedance spectroscopy (EIS). This technique measures current repose to a sinusoidal low potential AC voltage and calculates the impedance characteristics of the film. The impedance equation is shown below.

$$Z(\omega) = \frac{E}{I} = Z_o \exp exp\ (i\varphi) \ = Z_o(cos\varphi + isin\varphi)$$

where Z is the impedance, ω is the frequency, E is the voltage, I is the current, Z_o is the magnitude, and φ is the phase shift.[73] This data is represented in a Nyquist diagram,

which plots the imaginary part of the impedance vs. the real part of the impedance. An equivalent circuit model is used to fit the Nyquist plot to determine the total resistance, from which ionic conductivity and resistance are determined.

Another important technique to understand capacitors electrochemical behavior is cyclic voltammetry (CV). In this technique, the potential between the electrode systems is changed and the current response is measured. The potential vs current response gives a detailed analysis of oxidation and reduction peaks. This helps in defining the capacitor characteristics along with their respective oxidation and reduction state in a particular capacitor setup. The results are used in this work to report the behavior of our on chip characterization and calculating the capacity of these electrochemical capacitors.

Chapter 3: On-Chip ALD LiPON Solid State Capacitors for High Frequency Application

3.1 Overview

Multi-layer ceramic capacitors have been used for high frequency decoupling application due to a lower overall impedance leading to fast current response. However, high parasitic inductance limits the application of these capacitors in ultra-high frequency domain. Thus, MLCCs are placed close to the IC to improve circuit efficiency and reduce inductance. With next generation applications, the demand for frequency range has further increased which not only requires enhanced capacitor material but improved manufacturing techniques to limit the inductive path. Here, we

demonstrate ALD of two different polymorphs of ultra-thin film lithium phosphorus oxynitride (LiPON) as an inorganic solid-state electrolyte (SSE) for on chip capacitors for decoupling application. Both the LiPON capacitors shows an electric double layer behavior with a capacitance of 15 uF/cm^2 and a low leakage current (<20 nA/cm^2) at 2V. The LiPON shows EDLC behavior up to 10 kHz and beyond this frequency, both the polymorphs show an electrostatic behavior with a high dielectric constant (14). This dual frequency behavior along with low parasitic inductance and on chip integration allows for extended frequency range. Further, integration of these capacitor into 3D nanostructures would enhance the energy density and frequency range beyond state-of-the-art MLCCs.

3.2 Introduction

Capacitors are an indispensable part of electronic circuits, where they are used for a variety of applications, such as, power conditioning, memory, sensors, energy storage, and, more particularly, power spike management.[74–77] The increase in demand for portable and wearable electronics has led to an increased use for capacitor devices for power conditioning applications. In order to improve their power-efficiency, ICs embedded into wearable and portable electronics integrate advanced power management (i.e. voltage to frequency scaling) features requiring very stable (few mV of voltage swing) and fast settling of the DC voltage supply. Ensuring this voltage stability, implies smart design of the power distribution network (PDN). A very common approach is to place a decoupling capacitor at no electrical length from the

load, shorting the inductive path that limits the current flowing from the slow and distant battery.[78,79] During fast current transient on the PDN, resulting from load activity (ex. a wakeup event) the capacitor would be acting as the temporary current supply for few ps~ns, preventing the PDN voltage from swinging. In the AC domain, this would imply a capacitor capable of maintaining a very low PDN impedance (10's of mOhm) over a wide frequency range (DC – 100's of MHz).

The traditional aluminum electrolytic and multi-layer ceramic capacitors (MLCC) have been used for these applications, but a significant problem is their high intrinsic parasitic inductance (i.e. in-operative at fast current transients), bulky volume, rigid shapes, and low energy density.[80–82] Thus, they are incompatible with higher frequency application demands that require miniaturization. In contrast, electric double layer capacitors (EDLCs) match the criterion for both compact size and high energy density. EDLCs consist of two electrodes separated by an electrolyte containing mobile ions and stores energy by adsorption of ions on the surface of electrodes.[12,83] However, due to high impedance and low ionic mobility, EDLCs are limited to low frequency or DC operation.[84] Hence, there is a significant push towards high performing EDLCs which can compete or surpass the current capacitors available in the market for high frequency applications.

A considerable effort has been made to enhance the performance of these EDLCs for high-frequency applications by changing the electrode/electrolyte materials and structures. Most of these studies have report liquid or polymer electrolytes to enhance the frequency operation of these capacitors.[84–89] However, liquid and polymer

electrolytes have low voltage and temperature stability, significantly limiting their application space. Furthermore, liquid electrolytes have leakage issues leading to safety concerns for their application in wearable and implantable electronics. Recent studies have reported the use of all solid state electrolytes for SCs and batteries to reduce the safety issues and increase the application domain.[65,90–92] Solid-state SCs eliminate hazardous electrolyte leakage problems, expand temperature range, voltage windows, and provide structural stability.[55,66,93–95] However, the current solid state solid state EDLCs have a large electrolyte thickness along with moderate ionic conductivity, also limiting their use in high frequency applications.

Lithium phosphorus oxynitride (LiPON) has been extensively studied as a solid-state battery electrolyte. It has a high voltage stability up to 5V vs Li/Li^+ and a high temperature stability up to 300°C.[96–98] These same properties have recently garnered interest from the SC community. Sputtered LiPON has been characterized as a EDLC electrolyte by Sallez *et al*. They reported 140 nm of sputtered LiPON between platinum electrodes and showed a high energy density of 0.04 uWh/cm^2 and a limited cutoff frequency of 1000 Hz.[99] However, to meet the current state of the art application demands the capacitors require an increase in the cutoff frequency. This can be achieved by (1) increasing the ionic conductivity of the SSE, (2) decreasing the thickness of the electrolyte, and/or (3) integration into ultra-high-aspect ratio structures.[85,100] Our group showed this previously integrating ultra-thin Al_2O_3 into porous anodic aluminum templates to drastically expand the areal storage capacity of electrostatic capacitors.[101] More recently, this same structure-based approach was used to report the first 3D solid-state battery.[102]

ALD allows deposition of thin-film materials into high-aspect ratio nano/microstructures with high conformality. It consists of cyclic and sequential alternating pulses of gaseous precursors. Ideally, during each half-reaction, the precursor reacts in a self-limiting process that leaves no more than one monolayer. Typically, however, reactions are less than ideal and have growth rates below a monolayer. Despite this, ALD offers precise control of the thickness and composition of the material through choice of number of deposition cycles and precursors. The first ALD LiPON was a plasma enhanced process (PEALD) involving sequential pulsing of lithium tert-butoxide (LiOtBu), deionized water, trimethyl phosphate (TMP), and N_2 plasma.[53] Since two additional thermal ALD processes have been developed producing different polymorphs of LiPON.[54]

Herein, we report the fabrication and characterization of thin-film ALD LiPON supercapacitors. First, we compare PEALD and thermal ALD LiPON based on their electrochemical stability using cyclic voltammetry and electrochemical impedance spectroscopy. Here, the thermal LiPON shows extended ionic operation up to 10k Hz and cycling stability to 10k cycles. Plasma LiPON shows two states, one in the low-frequency region due to ionic transport, and a high-frequency region above 80k Hz from electrostatic polarization with a high dielectric constant of 13. Finally, we perform impedance simulations of a LiPON capacitor and compare it with MLCCs available in the market. The results demonstrate the suitability of ALD LiPON solid-state electrolytes for wider frequency applications compared to traditional MLCCs.

3.3 Experimental Procedure

3.3.1 Device fabrication

76 mm silicon wafers were oxidized by chemical vapor deposition (Tystar CVD) to create a 500 nm insulating layer of SiO_2. A thin titanium layer (~5 nm) was then deposited on top of the SiO_2 layer by electron beam evaporation (Angstrom NexDep Ebeam evaporator) to act as an adhesion layer for the bottom gold electrode (100 nm), which was also prepared by e-beam evaporation. The wafer was then diced into 1cm ×1cm chips using a dicing saw (Make, model) and cleaned by sonication in baths of acetone, isopropyl alcohol, and H_2O. The chips were then blown dry and heated at 70°C for 12 hours in a convection oven to remove excess water. The diced chips were loaded into a custom-built sample holder (Figure 10 (a)) with shadow mask on top (Figure 10 (b)) and transferred into the ALD reactor for LiPON deposition.

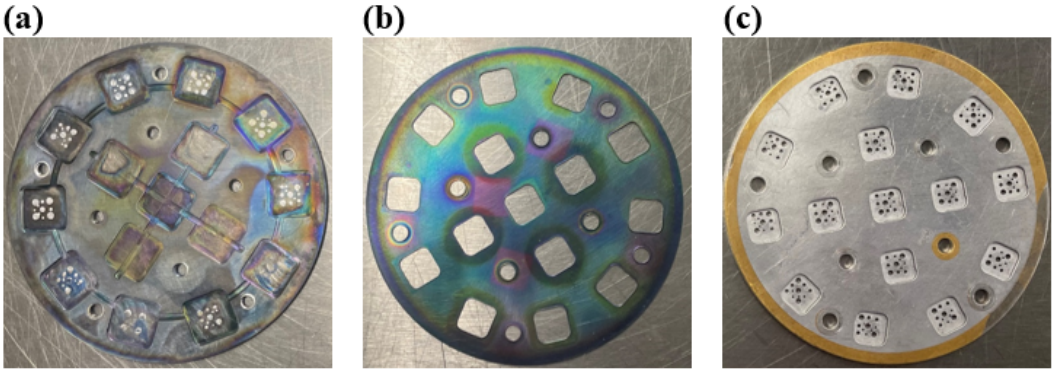

Figure 10: (a) Sample holder (b) Shadow mask for ALD (c) Shadow mask for top contacts

Two ALD (Veeco, Fiji) processes were used to deposit LiPON. First, a thermal process at 350°C (^{t}LiPON) was used. Here, lithium tert-butoxide (LiO^tBu) (Sigma,

97%) and diethyl phosphoramidate (DEPA) (Sigma, 98%), were reacted sequentially. The LiO^{t}Bu was loaded into a stainless-steel bubbler which was heated to 150°C. The DEPA was loaded in a stainless-steel cylinder and maintained at 115°C. The base pressure of the ALD reactor was 1×10^{-6} Torr, and the process pressure was maintained at ~200 mTorr by flow of UHP Argon (Airgas, 99.999%). The reaction was carried out with saturated doses of 20s for LiO^{t}Bu and 2s for DEPA followed by 20s and 10s purges after each dose respectively. Details of this process were published previously.[54]

For a second set, a PEALD LiPON (^{P}LiPON) process was used at 250°C with the same reactor pressure conditions listed above. LiO^{t}Bu (Sigma, 99.7%), deionized H_2O, trimethyl phosphate (TMP) (Sigma, 99.9%), and nitrogen plasma ($^PN_2$) were used as precursors. The LiO^{t}Bu was loaded into a stainless-steel bubbler which was preheated to 150°C. The H_2O and TMP were loaded into stainless-steel vapor-draw cylinders and were used at room temperature and 70°C respectively. Films were deposited using saturated doses of 20 s for the LiO^t Bu, 0.06 s for the H_2O, and 0.4 s for the TMP with 30 s purges after each dose. The $^PN_2$ pulse was carried out for 10s at 40 sccm with a plasma power of 300 W, and a 5s purge step. Details of this process were published previously.[53]

After deposition, the samples were transferred under vacuum to a glove box and a custom-built shadow mask (Figure 10 (c)) was used to limit and vary the size of the top contact. The samples were then transferred in-vacuum to an evaporation chamber. Finally, a thermal evaporation process was done using a custom effusion cell to deposit the top gold electrode (200 nm).

3.3.2 Device Characterization

Surface characterization was conducted using a vacuum coupled Kratos Ultra DLD X-ray photoelectron spectrometer (XPS). The spectra were collected using monochromatic Al Kα radiation at 12kV. Survey spectra were collected using a pass energy of 160 eV in hybrid lens mode with a step size of 1 eV. High-resolution scans were collected at 20 eV using 0.1 eV as the step size. The charge neutralizer was turned on during the data collection using a flood gun with 1A filament current, 1.15 V charge balance, and 1 V filament bias. CasaXPS was used to analyze the data collected from the XPS spectra with a Shirley background. All the spectra were calibrated to C 1s at 284.8 eV.

Scanning electron microscopy (SEM) and focused ion beam (FIB) cross sections were performed using a Tescan GAIA dual SEM/FIB system. FIB cross sections required a two-step cutting and polishing process, using a 30 kV Ga ion beam energy at 500 pA and 50 pA currents for each step, respectively. No protective coating was used on the top surface; the Au top contact provided enough protection for the underlying interfaces.

Electrochemical characterization was performed using a Biologic potentiostat (model) attached to a glove box. Samples were mounted on a custom-made mica glass-ceramic stage with an attached temperature controller for testing.

3.4 Results

3.4.1 Characterization and Metrology of ALD LiPON Processes

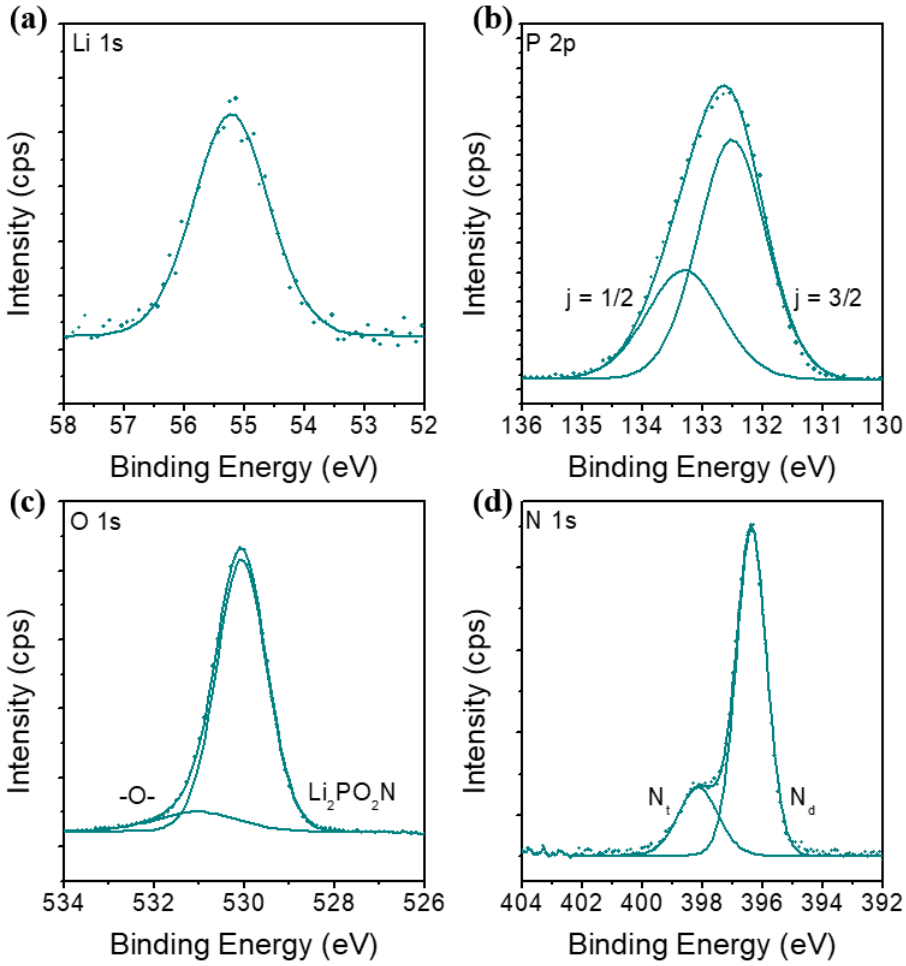

Figure 11: Thermal LiPON XPS spectra high resolution scan (a) Li 1s (b) P 2p (c) O 1s (d) N 1s

To quantify the composition of the different ALD LiPON processes, 50 nm of each was deposited on to Au coated Si chips and were characterized by XPS. The high-resolution spectra's of Li 1s, P 2p, O 1s and N 1s are found in Figure 11 (a-d.). The results show a consistent stoichiometry of Li_2PO_2N as seen in our previously published results. In the high-resolution Li 1s spectra, only one state is identified (Figure 11 (a))

which is also observed in a polyphosphazene chain structure. The P 2p high resolution scan also shows a single phase of phosphorus as seen in Figure 11 (b). In contrast, the O 1s and N 1s high resolution spectra has 2 components. In the O 1s spectra (Figure 11 (c)), the low binding energy peak is associated with the polyphosphazene chain whereas the small peak at high binding energy is associated with surface contamination. The N 1s spectra also contains 2 peaks that are associated with double coordinated and triply coordinated N as shown in Figure 11 (d). However, the ratio of triply coordinated to doubly coordinated is too small. Also the ratio of P:N is one, indicating fully nitrogenated polyphosphazene phase, as published previously.[54,103]

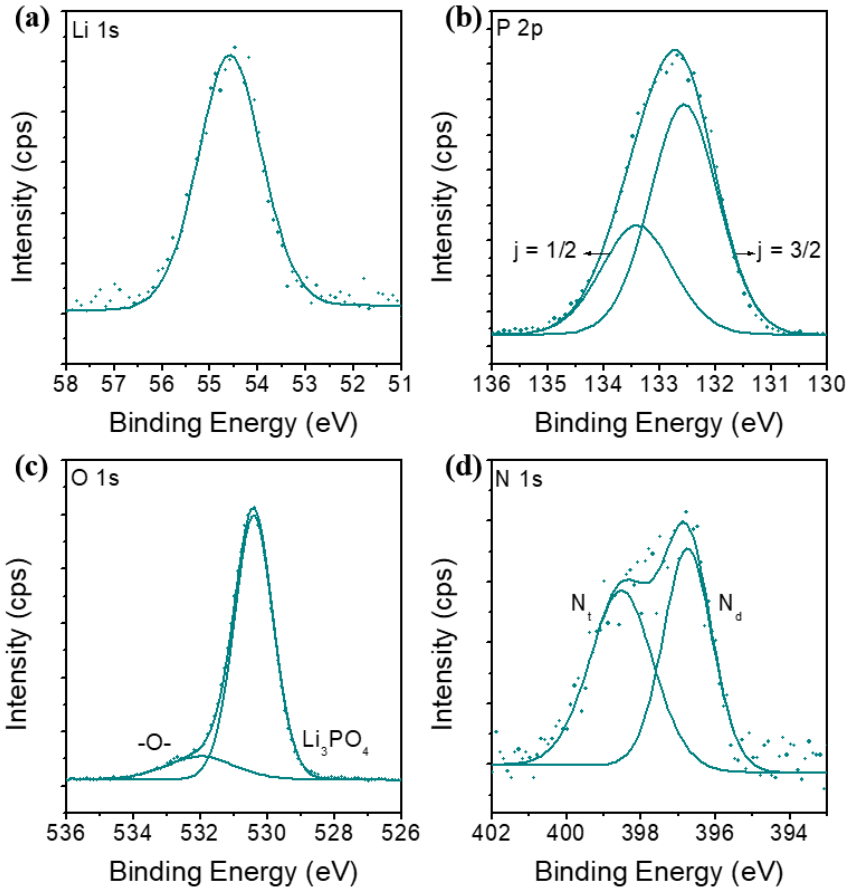

Figure 12: Plasma LiPON XPS spectra high resolution scan (a) Li 1s (b) P 2p (c) O 1s (d) N 1s

The ^{p}LiPON was characterized identically with the high-resolution spectra and is presented in Figure 12 (a-d). The result shows a stoichiometry of $Li_{3.47}PO_{3.43}N_{0.24}$, with a P:N ratio of 0.24. The high-resolution peaks show a similar component as in thermal LiPON structure. However, the film has lower nitrogen content in the plasma LiPON film. This is due to the difference in nitrogen incorporation process. In thermal LiPON DEPA has a preformed P-N bond whereas in plasma LiPON process nitrogen dosing is done using a plasma step as discussed in the experimental section.

Cross-sections were made by FIB to confirm the thickness of the electrolyte. The results are shown in Figure 13Figure 12 (a) and 13(b). Here, ~50 nm ^{t}LiPON and ^{p}LiPON, are respectively witnessed and confirm the electrolyte thickness.

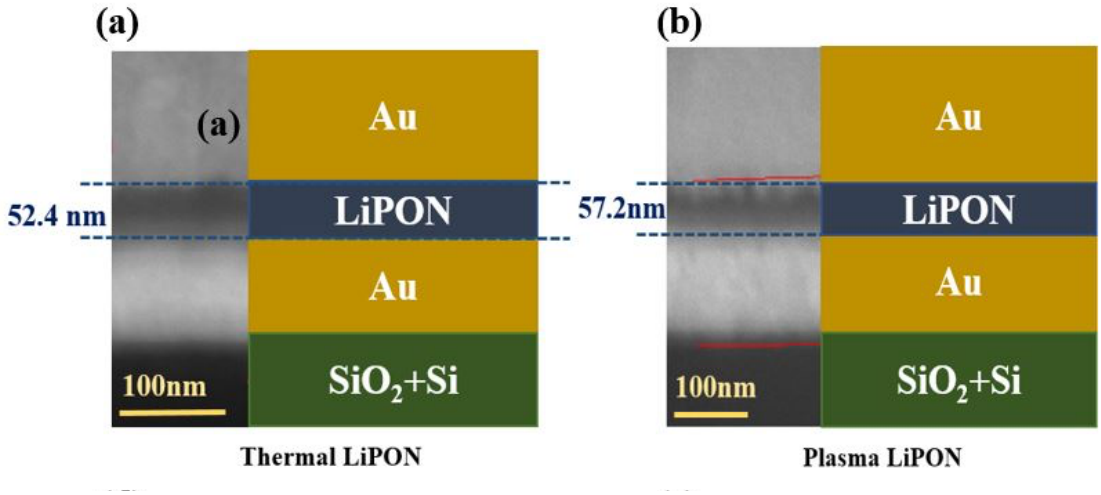

Figure 13: FIB-SEM cross-section of (a) Thermal LiPON (b) Plasma LiPON

3.4.2 Electrochemical Impedance Spectroscopy

The ionic conductivity of the ^{t}LiPON and ^{p}LiPON was quantified using electrochemical impedance spectroscopy (EIS), Figure 14 (a-d). The EIS was

conducted from 0.01 Hz to 100k Hz with a sine amplitude of 10mV. Nyquist plots at room temperature are compared and shown in Figure 14 (a). These data were modeled using two constant phase elements one for the high-mid frequency region (CPE1) and the other for the low-frequency region (CPE2). The resistance and diffusion in the high and mid frequency is modelled using a resistor (Ra) and Warburg diffusion (W), respectively. A diagram of the model is shown in the inset of Figure 14 (a). Here, a semicircular arc in the high-frequency region (>10 kHz) is witnessed followed by a non-vertical line in the intermediate frequency region (10 kHz), and a straight line in the low-frequency region (<10k Hz). The semicircular arc is lithium-ion transport in the solid-state electrolyte. The nonvertical line in the mid frequency range is the impedance caused by non-uniform ion transport from the bulk of the solid-state electrolyte (LiPON) to the Au electrode.[104] Finally, the straight line in the low frequency corresponds to the double-layer capacitance formed at the LiPON/Au interface. The ionic conductivity of the film calculated from the model was 5.42×10^{-7} S/cm for ^{t}LiPON and 6.82×10^{-8} S/cm for ^{p}LiPON film at room temperature and agrees with previous reported results.

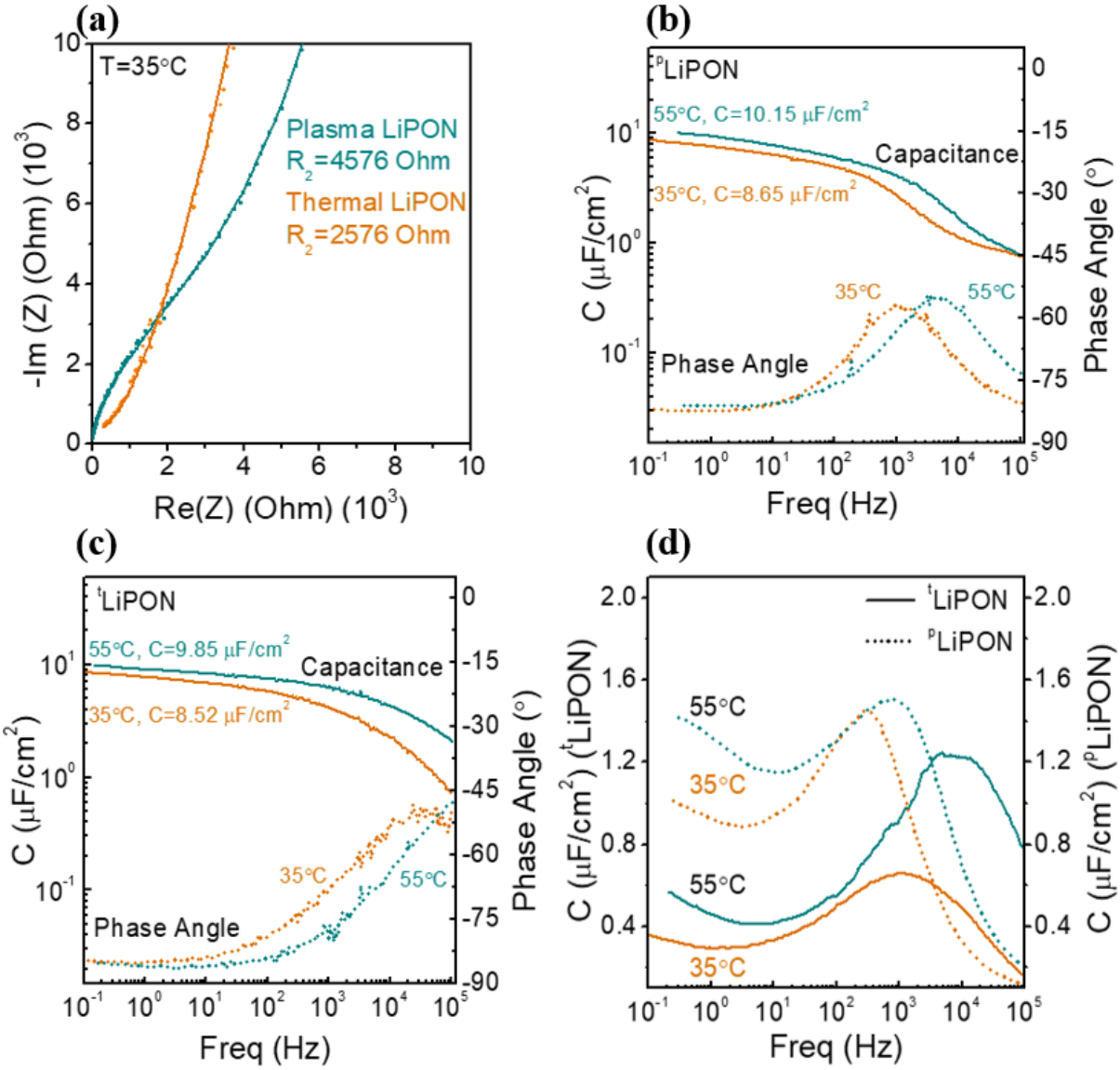

Figure 14: (a) Nyquist plot comparison between tLiPON and pLiPON (b) Capacitance and Phase Angle as a function of frequency (ᵗLiPON) (c) Capacitance and Phase Angle as a function of frequency (ᵖLiPON) (d) Imaginary Capacitance as a function of frequency (thermal)

Frequency dependence of both ᵗLiPON and ᵖLiPON was analyzed to quantify the capacitive characteristics of the electrolytes. The impedance data from the EIS spectra is used to calculate the real capacitance (C') and imaginary capacitance (C'') as

a function of frequency using eq1, eq2 respectively, with the results shown at 35°C and 55°C in Figure 14 (b) and Figure 14 (c).

$$C' = \frac{-Z''(w)}{2\pi f S|Z(w)|^2} \quad eq1$$

$$C'' = \frac{-Z'(w)}{2\pi f S|Z(w)|^2} \quad eq\ 2$$

where $Z'(w)$ and $Z''(w)$ is the real and imaginary part of the impedance $Z(w)$ whereas, f denotes the frequency and S the active area.

For the ^{p}LiPON, the capacitance vs. frequency curve shows two plateaus, the first at low frequency region (<1k Hz) and the second at high frequency region (>10k Hz) as seen in Figure 14 (b) (left axis). In the low-frequency region, a capacitance of 8.65uF/cm^2 at 35°C is measured, decreasing to ~1 uF/cm^2 at high-frequency. At 55°C, the capacitance value increases to 10.15 uF/cm^2 at low frequency, but again decreases to ~1 uF/cm^2 at high frequency. The increase in double layer capacitance in the low frequency region is directly related to the increased ionic conductivity with elevated temperature. The phase angle as a function of frequency is plotted in the same Figure on the right axis. Here, a bell-shaped curve is witnessed. At both, high and low frequency, a phase angle of -82 is seen indicating capacitive behavior. Thus, the low frequency capacitive behavior is attributed to the ionic transport in the solid electrolyte, whereas the high frequency behavior is correlated with electrostatic polarization. Using

equation S2, the dielectric constant calculated from the high-frequency region capacitance is 14.

Figure 14 (c) shows the properties of ^{t}LiPON as a function of frequency and temperature. The capacitance was measured to be 8.95 uF/cm^2 at 35°C, which increases to 15.7 uF/cm^2 at 55°C. The phase angle as function of frequency is plotted on the right axis in Figure 14 (c). The phase does not show a complete bell shape curve as observed in ^{p}LiPON. Similarly, the phase angle at low frequency region is close to -85, implying a double layer behavior of ^{t}LiPON. Since the ^{t}LiPON has an order-of-magnitude higher ionic conductivity, Figure 14 (c) shows all the same characteristics seen for the ^{p}LiPON shifted towards higher frequency, however, the electrostatic behavior of ^{t}LiPON at high frequency is beyond the range of our potentiostat.

The relaxation time constant is a critical factor to determine performance in AC applications and defines the minimum time required to discharge the capacitor and maintain more than 50 percent efficiency. The lower value of τ_0 corresponds to the supercapacitor's better rate capability, which helps to eliminate the high order harmonics and thus protect the electronic circuits. To evaluate the relaxation time, the imaginary capacitance was plotted as a function of frequency at two different temperatures, using equation 2, and is shown in Figure 14 (d). The curve shows a typical bell shape, and the cutoff frequency (f_0) corresponds to the peak of the curve. From Figure 14 (d) (right axis), the cutoff frequency for ^{p}LiPON at 35°C is 200 Hz and increases to 850 Hz at 55°C. Thus, implying a relaxation time constant ($\tau_0=1/f_0$) of 5 ms at 35°C, which decreases to 1.1 ms at 55°C. The cutoff frequency for ^{t}LiPON at

35°C is 1 kHz, increasing to 10 kHz at 55°C (figure 3.5(d) (left axis)). This corresponds to a relaxation time of 1 ms at 35°C and decreases to 0.1 ms at 55°C.

3.2.3 Cyclic Voltammetry Comparison

Cyclic Voltammetry (CV) was conducted from 0-2V at a scan rate ranging from 50 mV/s to 10 V/s. The CV profile for ^{t}LiPON at both low scan rates (0.05V/s to 0.5V/s) and high scan rates (1V/s to 10V/s) is shown in Figure 15 (a,b). The CV exhibits a box shape within 0-2V and a capacitance value of 15uF/cm^2 at 0.05V/s. The box shape is retained up to a scan rate of 10V/s as shown in Figure 15 (b). The capacitance value decreases from 15uF/cm^2 at 50 mV/s to 9 uF/cm^2 at 10 V/s. The capacitance value range and the box shape CVs represent the typical double-layer behavior of ^{t}LiPON electrolyte. The CV also shows an increased current density near both high and low potential. This increase in current density could be associated with Li^+ plating on the gold current collectors. A recent study by Put et al. reports LiPON thermal dissociation and reaction with gold at 1.25-1.5V vs. standard hydrogen electrode[105], suggesting Li alloy formation at the gold/LiPON interface.

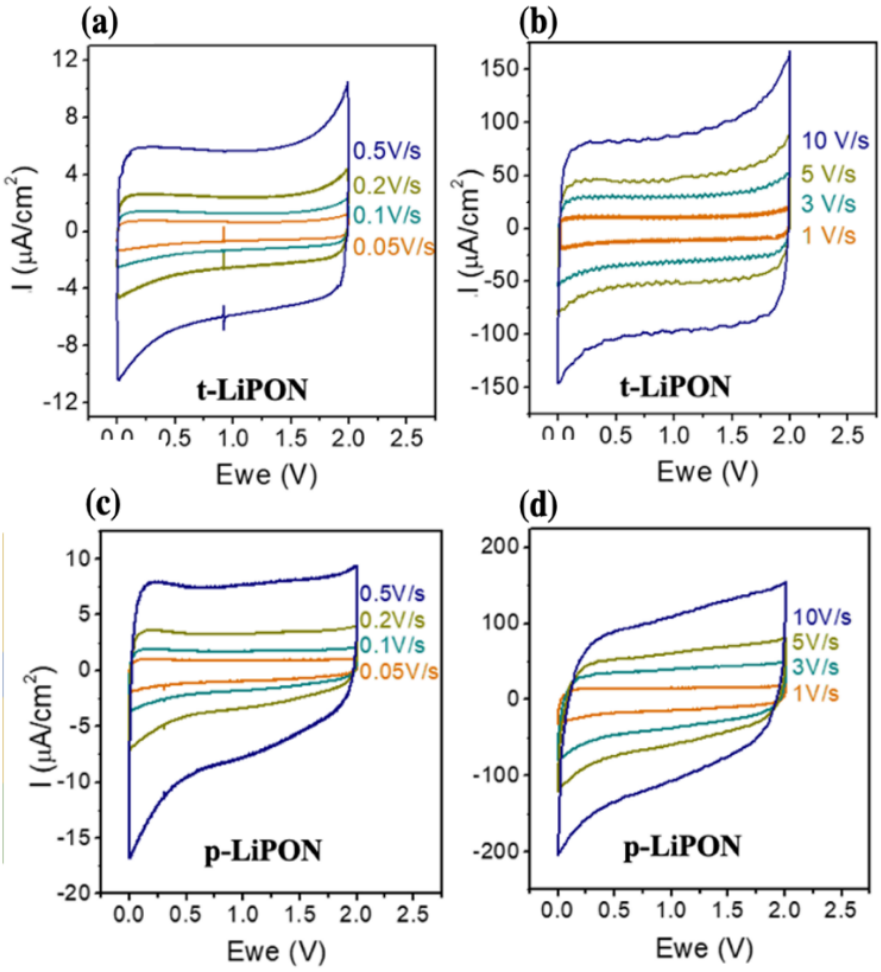

Figure 15: CVs (a) ^{t}LiPON at low scan rate (b) ^{t}LiPON at high scan rate (c) ^{p}LiPON at low scan rate (b) ^{p}LiPON at high scan rate

Similarly, CVs for ^{p}LiPON seen in Figure 15 (c,d), also show a box shape with a slightly higher capacitance value of 18 uF/cm^2 at 0.05 V/s, decreasing to 12.2 uF/cm^2 at 10V/s. As in the thermal case, the high current density observed at low potential decreases with increasing scan rate. This decrease is ascribed to decreased kinetics at high scan rates leading to a decrease in alloy formation. Minor differences in the CVs are related to differences in the ionic conductivities and slight differences in the thicknesses of the devices. Otherwise, these data are in good agreement. The capacitance value and the box shape CVs represent the typical double-layer behavior

of both ^{t}LiPON and ^{p}LiPON electrolyte. The double-layer formed at the Au/LiPON interface is due to Li^{+} migration towards the lower potential gold electrode and vacancies to high potential.[106,107] A box shape is observed at scan rates up to 10V/s, implying the ionic capacity retention of both the electrolytes at high scan rates.

3.4.3 Chronoamperometry

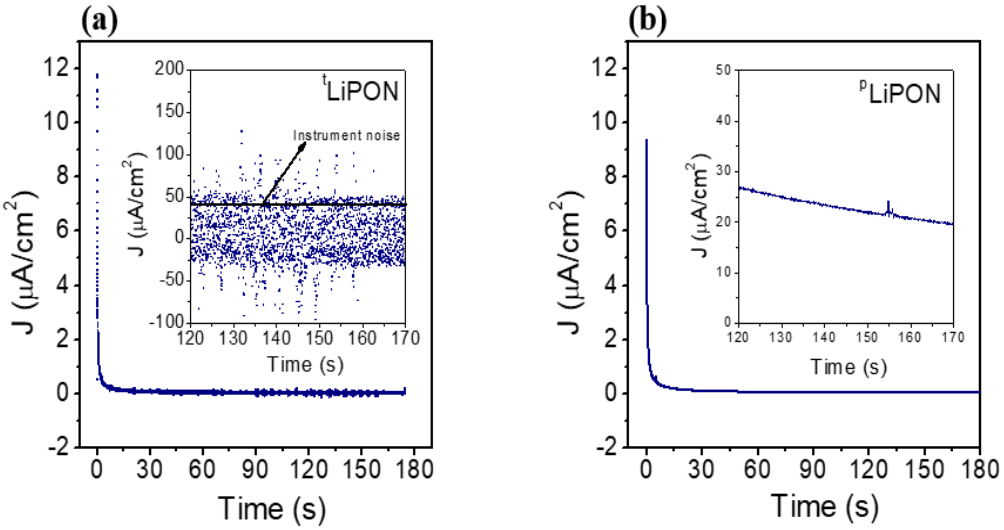

Figure 16: Leakage Current under 2V DC bias (a) Thermal LiPON (b) Plasma LiPON

To quantify the DC leakage current chronoamperometry was conducted and the results are displayed in Figure 16 (a,b). A 2V DC bias was applied across the capacitor and the current as a function of time was measured. The leakage current was then calculated as the average value of the last 10 seconds measured as shown in the inset. The leakage current measured for ^{t}LiPON is ~20 nA/cm^2 and for ^{p}LiPON ~18 nA/cm^2. These results confirm that the increased current density observed in the CVs (Figure

15) at both high and low potential is due to a faradic reaction at the interface and not electronic leakage.

3.2.5 Stability

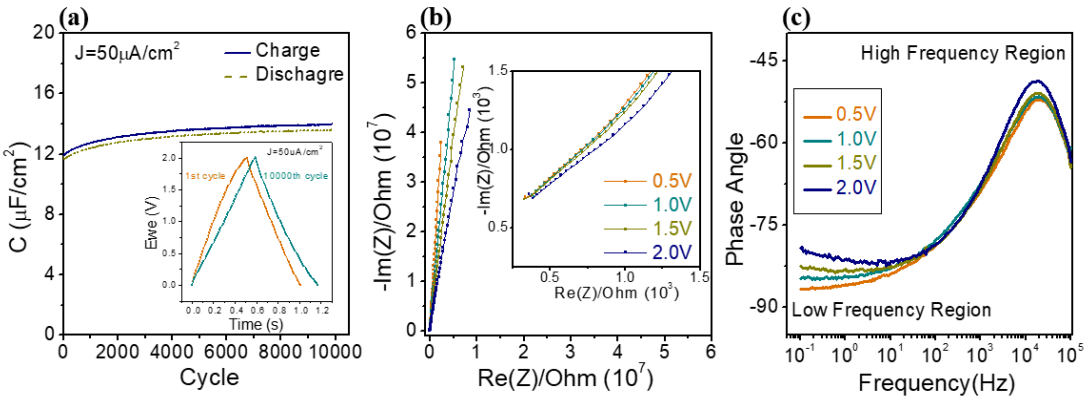

Figure 17: (a) GCD for 10000 cycles (b) Nyquist plot at different applied potential (c) Phase angle as a function of frequency at different applied potential

Galvanostatic charge-discharge (GCD) was conducted at 50 mA/cm^2 from 0-2V for 10k cycles. The capacitance as a function of cycle number was plotted and is shown in Figure 17 (a). The capacitance in the first cycle is 11.95 uF/cm^{2,} and it increases to 13.88 uF/cm^2 after 10000 cycles. The increase in capacitance observed during cycling is due to a faradic reaction at the ^{t}LiPON/Au interface and is also observed during CV cycling from 0-2V. The charge-discharge time for the first and the 10000th GCD cycle is compared and shown in inset of Figure 17 (a). The time to charge the capacitor in the first cycle is 0.5s and it increases to 0.6s in the last cycle. A similar trend was observed for discharge time, where the discharge time increased to 0.6s from 0.5s after 10000 cycles. This increase in charge discharge time is most likely due to degradation of the interface due to Li alloying.

The alloy formation observed during CVs and GCD was further quantified by varying the potential during EIS which was conducted from 0.01 Hz to 100 kHz at a sine amplitude of 10 mV and at potentials ranging from 0.5 to 2V. After each measurement, the capacitor was discharged using a load resistor. The Nyquist plot is shown in Figure 17 (b). The plot can be divided into two main regions, a high-frequency region showing the semicircular arc (inset, Figure 17 (a)) and a low-frequency region showing the double layer behavior. In the high-frequency region, the semicircular arc remains constant for all applied voltages, signifying that the ionic conductivity remains unchanged. A second semicircular region is observed in the low-frequency region for all the applied potentials. The radius of the observed semicircular arc reduces with increased potential signifying an increased impedance. This increase in real impedance corresponds to Li^+ alloying on the gold electrode. The phase angle was plotted as a function of frequency from the impedance data as shown in Figure 17 (c). The high frequency phase angle remains constant, implying that the ionic conductivity is unaltered. At low frequency (<100 Hz), the phase angle shift from -86 to -78 further confirming an alloy reaction.

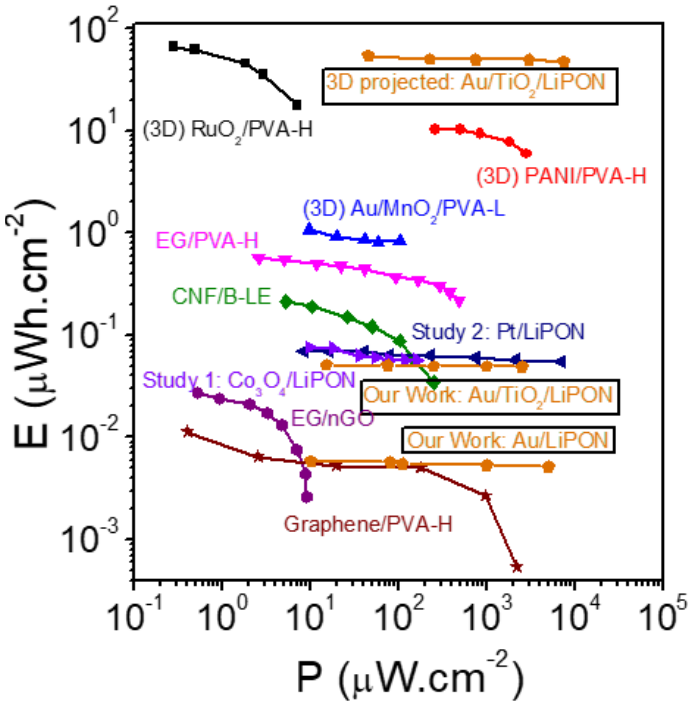

Figure 18: Ragone Plot comparing state of the art solid state supercapacitors

The performance of our ᵗLiPON supercapacitors was analyzed by calculating the energy and power density, with comparison shown in Figure 18. The maximum energy density reported for the symmetric stack is 0.0056 uWh/cm^2 with a power density of 5000 uW/cm^2. The energy density reported is among the top state-of-the-art all solid-state supercapacitors. Some works have reported 3D architecture allowing enhanced energy storage as shown in Figure 18. The performance of our planar work can be enhanced by a factor of 150-250 by deposition into 3D nanostructures [cite]. These results will substantially enhance the energy and power density (figure 3.9(3D projection)) to meet the current energy density demands for portable and wearable electronics.

3.5 Application

Traditionally, MLCCs are used for decoupling applications but due to their higher parasitic inductance they possess a challenge in ultra-high frequency applications. The high parasitic inductance is not only due to their bulky size but their placement on the PCB board adds to the inductance of the system. On the other hand, our LiPON capacitors have low parasitic inductance, this is due to several reasons. First, it allows for on chip integration, thus reducing the wiring length leading to lower overall impedance. Secondly, ALD allows for thin film deposition (<10nm) of electrode system which further reduces the inductance of these capacitors. Finally, integration of these capacitors using ALD into 3D nanopores will further reduce the overall impedance due to the parallel structure of AAO pores. This makes ALD LiPON capacitors an ideal choice for ultra-high frequency applications.

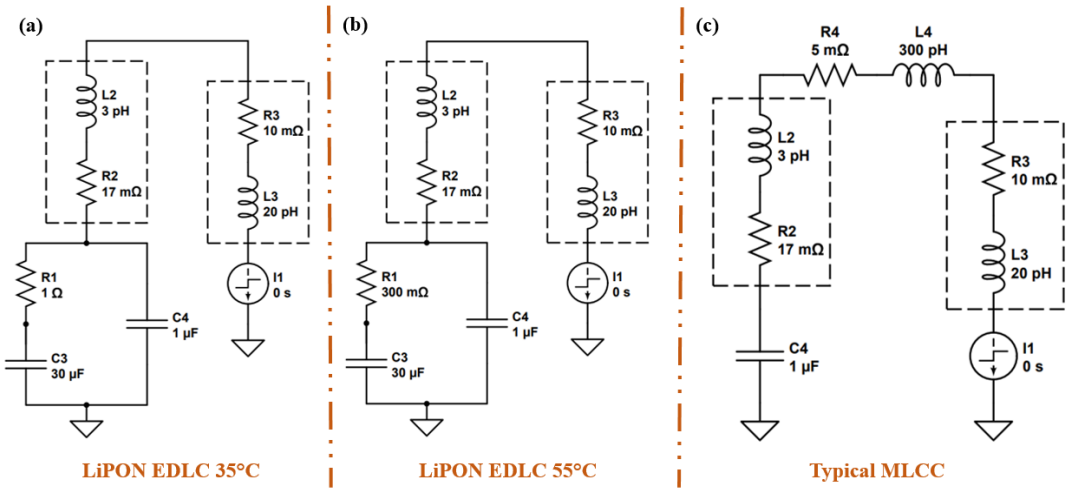

Figure 19: Capacitor impedance circuit with wired connection (a) LiPON EDLC at 35°C (b) LiPON EDLC at 55°C (d) Typical MLCC

Another advantage of ALD LiPON capacitor is its dual frequency behavior. The capacitor shows electrostatic behavior in the high frequency region but also shows a faradaic behavior in the low frequency region. This dual frequency behavior allows for higher energy storage and wider frequency application as compared to MLCCs. However, in the low frequency region the overall impedance of LiPON is high due high ionic resistance. To further understand the advantage of dual frequency behavior of the LiPON capacitor, impedance behavior of the capacitor is modelled in LT spice at 1A step response and compared to a typical MLCC available in the market. The target impedance for decoupling application is 200 mOhm. The circuit used for analysis is shown in Figure 19 (a-c). An optimistic 3D case for LiPON capacitor with thin film and increased ionic conductivity is considered. The 3D on chip integration allows for low parasitic values whereas thin film and improved ionic conductivity adds to reduce the ionic resistance in the low frequency region. Increasing temperature further increases the ionic conductivity as seen in our LiPON MIM structure. Based on these conditions, the 3D LiPON capacitor circuit consist of a high frequency electrostatic capacitor (1 uF) in parallel with a combination of low frequency ionic capacitor (30 uF) in series with ionic resistance as shown in Figure 19 (a,b). The ionic resistance simulated for the optimistic case is assumed to be 1 Ohm at 35°C and 300 mOhm at 55°C. The calculations for ionic resistance are based on an optimistic ionic conductivity of $1\mu S/cm^2$ and thickness of 20 nm of the solid electrolyte. The standard ESR and ESL of the capacitor are 17 mOhm and 3 pH respectively considering on chip integration and thin film electrode structure (10 nm). For the MLCC, standard capacitance is 30 uF, ESR is 2 mOhm and a high ESL of 180 pH. The high ESL is due to the bulky size

of MLCCs. The wire resistance and wire inductance in both the circuits are 10 mOhm and 20 pH respectively. However, MLCC do not have an advantage of on chip integration and thus it adds additional resistance and inductance path compared to on chip LiPON capacitors (Figure 19 (c)). This is accounted in the circuit by adding additional ESR (5 Ohm) and ESL (0.5 nH). The simulated results at 35°C and 55°C are shown in Figure 20. The results shows that the target impedance value for an MLCC is achieved between 50 kHz to 40 MHz (Figure 20, blue curve). For LiPON capacitor at 35°C, the target impedance value is achieved in between 1 MHz to 5000 MHz as shown in Figure 20 (orange curve). At 55°C, the frequency ranges from 50 KHz to 5000 MHz as shown in figure 3.11 (green curve).

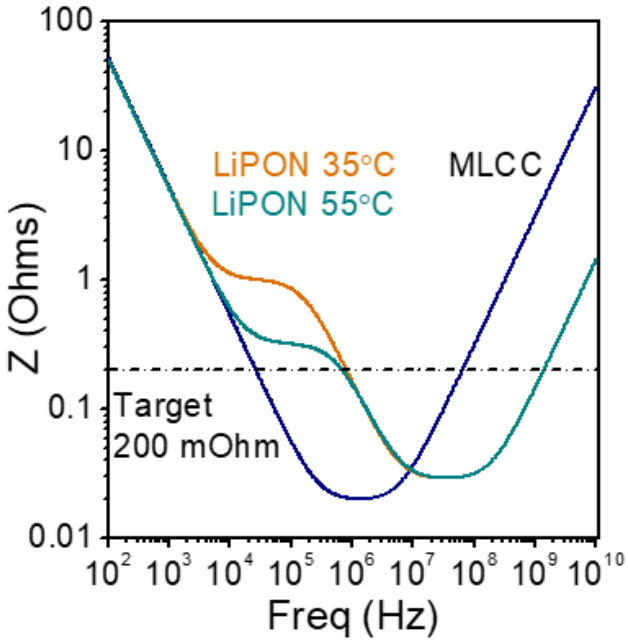

Figure 20: Comparison of impedance spectra of LiPON capacitors with state-of-the-art MLCCs

MLCCs show an excellent behavior at low frequency domain due to lower or negligible series resistance. At high frequency, the impedance increases due to high

parasitic inductance which limits its application to 40 MHz. However, LiPON capacitors shows an extended frequency domain to 1000 MHz at both the temperatures. This is due to the low parasitic inductance and dual frequency behavior (ionic and electrostatic) thereby expanding the frequency range for decoupling application. The LiPON capacitor at 55C shows a wider frequency range as compared to the LiPON at 35C. This is due to higher ionic conductivity and thus shifting the lower frequency cutoff from 1 MHz to 50 KHz. However, to achieve these desired results for EDLCs, the ionic resistance should be decreased in comparison to the 50 nm case studied. This can be achieved by decreasing the solid-state electrolyte thickness from 50 nm to 10-15 nm. Decreasing the thickness leads to lower ion migration path thus leading to fast current response at low frequency. Another way is by increasing the ionic conductivity to 1 uS/cm^2, similar to NASCOIN type solid electrolytes. This can be achieved by modification of the current LiPON structure by adding some additives to increase the ionic conductivity. Increasing temperature also decreases the resistive path for the ions and thus allows them to move freely inside the solid matrix. Also, 3D configuration has been used to decreases the resistive path per unit footprint area. Thus, ALD plays a major role in capacitor fabrication as it allows for both decrease in thickness and deposition into 3D configuration. Further, improving the process parameters to desired values will lead to a new class of capacitors that can cater a wider application window with an advantage of on chip integration.

3.6 Conclusion

In this work, we have successfully demonstrated for the first time ALD inorganic solid-state electrolyte showing ionic capacitance. Two capacitor stacks with polymorphs of ultra-thin ALD LiPON (thermal and plasma) were studied. Their electrochemical characterization confirmed electric double layer behavior. The capacitor stack with ^{p}LiPON clearly shows benefits in two frequency regimes - one below 900 Hz and one above 80 kHz, as can be seen in Figure 1(d). The LiPON electrolyte enhances capacitance below 900 Hz while its electrostatic behavior retains high capacitance at ultra-high-frequency (>80 kHz), in part due to LiPON's high dielectric constant (13). This dual state energy storage behavior opens up a large potential application window for the ^{p}LiPON supercapacitors. A similar behavior was observed for the ^{t}LiPON capacitors, where the ionic behavior was observed up to 10 kHz frequency at 55°C and a low leakage current (<20nA/cm^2). These results highlight the potential advantage of polymorphs of ALD LiPON as a capacitor electrolyte with high temperature stability along with high frequency applications due to ultra-low thicknesses and on chip integration.

Further, improving the ionic conductivity and decreasing the thickness will increase the frequency limit of these capacitors. Fabrication of the LiPON capacitors into 3D nanostructures would reduce the impedance and further enhance the capability of these capacitors into ultra-high frequency to compete or surpass the state-of-the-art MLCCs available in the market. An energy density of 0.005 uWh/cm^2 was measured and a high cyclic stability (>10k cycles) with a significant potential window (2V) was also demonstrated. These results show the stability and process compatibility of ALD LiPON thin films. These advantages of ALD LiPON could be used to grow thin

conformal films into 3D architecture that would increase the energy and power density by a factor of 250. The AAO structure design enhances the capacitance but reduces the overall parasitic inductance and resistance. Thus, the state of art capacitor architecture along with ALD allows for superior performing capacitors. Also, using ALD's process capability with silicon manufacturing gives the electrolyte an edge over the current technology. In future, ALD TiN can be used as current collectors to allow the deposition of full stacks into 3D structures, thus enabling the solid-state inorganic electrolytes to also achieve the high energy demands of the growing electronics market.

Chapter 4: All Solid state ALD LiPON capacitor with TiN and TiO_2 as Electrode Materials

4.1 Introduction

The miniaturization and increased consumption of electronics has led to high demand for energy storage devices. Capacitors and batteries are among the current energy storage technology being widely used. In particular, capacitors are ubiquitous in modern society; used in everything from car components to portable electronics.[1,108,109] Capacitors are used for 1) power conditioning to filter out input signal, 2) memory devices to store information as bits, 3) sensors to detect humidity and pressure, 4) energy storage to deliver energy during power spikes, etc. Due to such wide applications and high demand, the global market for capacitors is predicted to increase by 100 million dollars by end of 2030.[110,111] Generally speaking, capacitors have high power density and long charge-discharge cycle life as compared to a battery.[112] This allows capacitors to be used as an energy storage device in the next generation portable and implantable electronics where there is a demand for energy to be delivered quickly for multiple cycles. However, a major challenge to the current capacitor technology is limited energy density and thus requires multiple devices to increase the overall storage capacity. With next-generation applications requiring less footprint area and higher energy density, there is a need to improve these energy storage devices to achieve higher overall performance. Capacitors, exemplified by supercapacitors, can provide increased energy density along with high power density for these next generation applications.[113]

Chapter 3 results show thermal LiPON as a solid-state electrolyte for EDLCs with superior electrochemical stability and high cutoff frequency. With new generation applications requiring high energy density, we test the thermal LiPON electrolyte with different electrode materials. For this work, TiO_2 is used as an electrode material for Li-ion energy storage as it has shown high energy storage capacity along with high cyclic life.[114–116] Titanium Nitride (TiN) also has oxygen contamination in form of nano dimensional TiOx,[117] we first study TiO_2 and subsequently TiN as an electrode material for our pseudocapcitors. Also, in this work, we study ALD grown electrode materials as ALD offers precise control of thickness and composition of the material. Along with confirmability and uniformity on 3D surfaces, the remarkable selectivity and superior scalability make it an excellent choice for synthesizing electrodes for thin film supercapacitor applications that can be integrated with semiconductor manufacturing.

4.2 ALD TiO_2 and TiN Asymmetric Capacitors

4.2.1 ALD TiO_2 Recipe

Many ALD TiO_2 recipes have been reported in the literature with titanium isopropoxide (TTIP) and tetrakis(dimethylamido)titanium (TDMAT) being the most common precursors.[118–122] Both precursors have two main recipes mainly thermal and plasma. With both these precursors, deionized water and oxygen plasma are used as a co-reactant for the thermal and the plasma ALD process respectively. The standard dose and purge time for each precursor and co-reactant is given in Table 5. The dose and purge time may vary depending on the vapor pressure and the reactor conditions.

Substrate temperature also plays a huge role in deciding the dose and the purge conditions for the precursor and the co-reactant. Many studies have reported different dose and purge time for optimizing the recipes.

Table 5: ALD TiO_2 recipes[123]

	TDMAT Plasma	**TDMAT Thermal**	**TTIP Plasma**	**TTIP Thermal**
Precursor Dose (s)	0.5	1	2	2
Precursor Purge (s)	3	5	6	5
Co-reactant Dose (s)	4	0.15	5	0.15
Co-reactant Purge (s)	2	10	4	20
Substrate Temperature (°C)	270	250	270	250

The selection criteria for TiO_2 recipe in our case was based on ease of ALD process and compatibility with LiPON thin films. Another important criterion was deposition into 3D Nano structures along with process recipe easily tunable for different substrates materials. However, a major problem with plasma enhanced ALD process is conformality into 3D nano structures. Also, integration with chip manufacturing is difficult as the high temperature plasma might destroy or degrade the overall system performance. Thus, thermal TDMAT or thermal TTIP process was considered as the possible recipes for our all-solid-state capacitors but TTIP limits the

potential for large scale uptake due to corrosive nature of by-products. Hence, thermal TDMAT recipe was used in development of our solid-state super capacitors.

The optimized recipe used for TiO_2 deposition is modified for our reactor (Veeco, Fiji) conditions. Tetrakisdimethylammido titanium (TDMA (Ti)) and deionized H_2O were used as precursors. The TDMA (Ti) and water were loaded in stainless steel cylinders and the TDMA (Ti) was heated to 75°C whereas the de-ionized water was kept at room temperature. The base pressure of the ALD reactor was 1×10^{-6} Torr, and the process pressure was maintained at ~200 mTorr by flow of UHP Argon (Airgas, 99.999%). The film was deposited at 250°C with doses of 0.06 s for H_2O and 0.1 s for TDMA(Ti) followed by a 5s purge after each dose.

4.2.2 ALD TiN Recipe

ALD Titanium Nitride (TiN) is deposited using a variety of precursor and co-reactants.[117,124–128] Titanium chloride is most used precursor for TiN. The process involves a binary reaction between titanium chloride and ammonia. However, the titanium chloride precursors are not optimal choice for our case as it requires high temperatures (400°C) for the deposition. The high temperature also makes it incompatible with a lot of semiconductor manufacturing. Also, the byproduct of the reaction is dangerous for the reactor functioning and large-scale production. The chloride contamination due to incomplete reaction might be another issue that could potentially lead to degradation of TiN and LiPON film properties. Thus, in our study we focus on a thermal TiN process involving a simple reaction between tetrakis (dimethylamido) titanium (TDMAT) and ammonia (NH_3) at 250°C with similar reactor conditions as discussed above.

4.2.3 Device fabrication

76 mm silicon wafers were oxidized by chemical vapor deposition (Tystar CVD) to create a 500 nm insulating layer of SiO2. A thin titanium layer (~5 nm) was then deposited on top of the SiO2 layer by electron beam evaporation (Angstrom NexDep Ebeam evaporator) to act as an adhesion layer for the bottom gold electrode (100 nm), which was also prepared by e-beam evaporation. The wafer was then diced into 1cm ×1cm chips using a dicing saw (Make, model) and cleaned by sonication in baths of acetone, isopropyl alcohol, and H_2O. The chips were then blown dry and heated at 70°C for 12 hours in a convection oven to remove excess water. The diced chips were loaded into a custom-built sample holder (Figure 3.1(a)) with shadow mask on top (Figure 3.1(b)) and transferred into the ALD reactor. Recipe discussed in section 4.2.1 and 4.2.2 were then used for TiO_2 and TiN deposition respectively.

After the bottom electrode deposition, thermal LiPON was deposited with similar reactor conditions and recipe as discussed in Section 3.3.1. The samples were then transferred under vacuum to a glove box and a custom-built shadow mask (Figure 10 (c)) was used to limit and vary the size of the top contact. The samples were then transferred in-vacuum to an evaporation chamber. Finally, a thermal evaporation process was done using a custom effusion cell to deposit the top gold electrode (200-400 nm).

4.3 Results: ALD TiO_2 Asymmetric Capacitors

4.3.1 Characterization and Metrology of ALD TiO_2

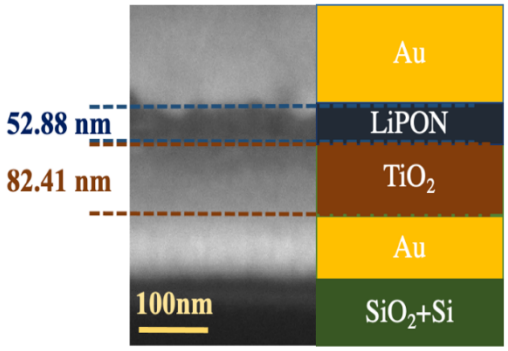

Figure 21: Asymmetric Capacitor Stack (a) FIB-SEM image with cartoon

An asymmetric capacitor stack (Au/TiO2/ᵗLiPON/Au), with an additional pseudocapacitive layer, was fabricated and is shown in Figure 21. 80 nm of TiO_2 was deposited via ALD recipe described above on a gold chip, and a FIB cross-section was done to confirm the thickness. 50nm of LiPON was then deposited on top of TiO_2, and the stack was completed by evaporation of Au using a shadow mask.

Before the fabrication of the complete stack, XPS characterization of TiO_2 thin film was done and the survey and high resolution scan are shown in Figure 22 (a,d). The survey scan shown in Figure 22 (a) clearly shows Ti 2p, O 1s and some carbon contamination into the film. The O 1s high resolution spectra (Figure 22 (b)) shows two different oxygen bonding. The 530.3 eV peak corresponds to TiO_2 whereas the peak at 531.1 corresponds to the reduced TiO_2 due to surface contamination and reaction with carbon. This is also evident in Ti 2p high resolution scan. Figure 22 (c) shows two different oxidation state of Ti, Ti^{4+} and Ti^{3+}. The Ti^{4+} state at 459 eV corresponds to the TiO_2 whereas the Ti^{3+} state at 457.9 corresponds unreacted TDMAT

with some oxygen contamination or surface reactions. The high-resolution carbon 1s peak (Figure 22 (d) shows high amount of adventitious carbon, along with some oxygen and fluorine contamination at 286.3 eV and 289.1 eV respectively. However, 98 percent of film has Ti^{4+} and O^{-2} giving it an even composition throughout.

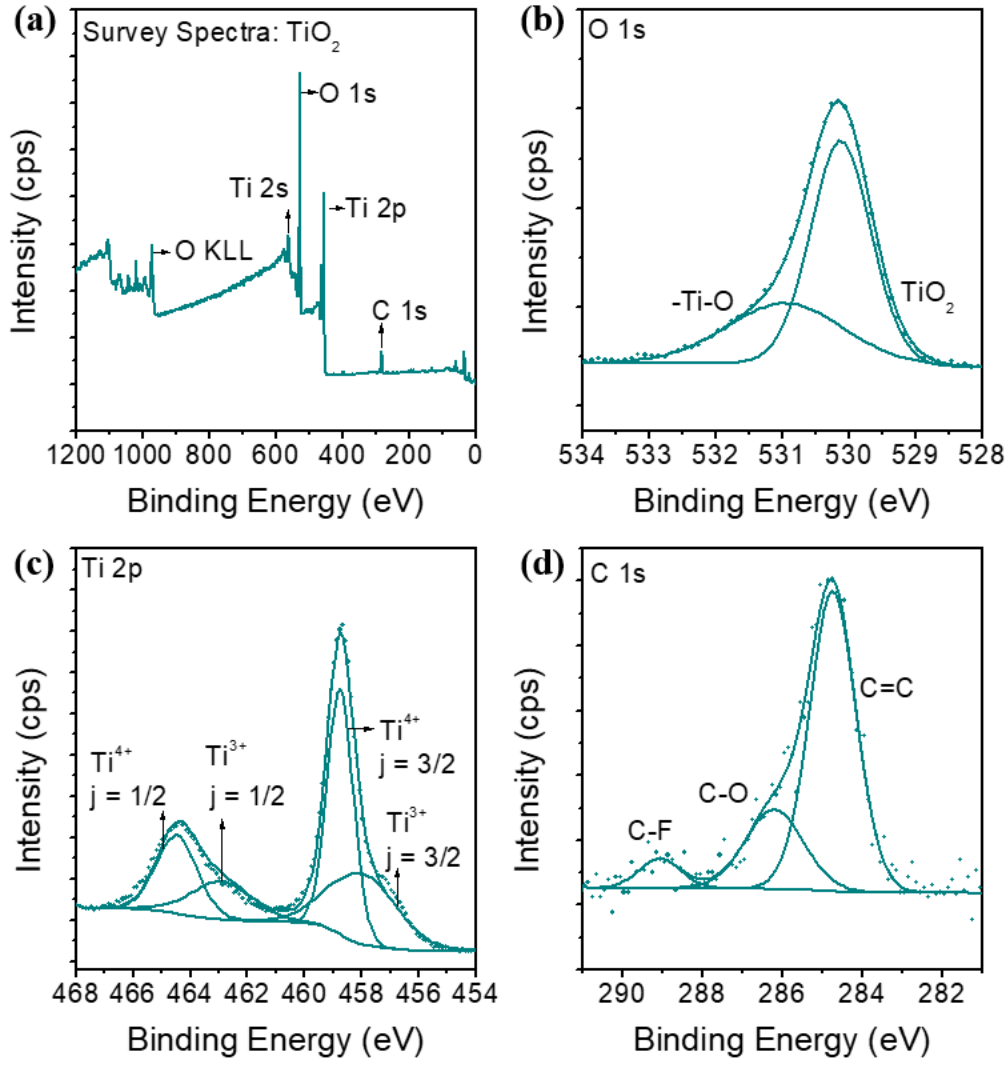

Figure 22: XPS of TiO2 (a) Survey Spectra (b) high resolution O 1s (c) high resolution Ti 2p (d) high resolution C 1s

4.3.2 Electrochemical Characterization

Next, the asymmetric stack was characterized using cyclic voltammetry to understand the lithium-ion insertion into the TiO_2 thin film. CVs were conducted at

0.5V/s from 0-1 V, 0-2 V, 0-3V and 0-4V and the insertion peak was observed in each case. In each voltage window, 5 CV cycles were performed and the first cycle in each voltage window was plotted and is shown in Figure 23. During the first CV from 0-1V (yellow curve), a capacitance of 64 uF/cm^2 was observed, which dropped to 55 uF/cm^2 from 0-2 V. In each subsequent voltage window, the capacitance dropped and at 0-4V (blue curve) the capacitance observed was 17uF/cm^2. In case of 0-1V, a high current density delithiation peak was observed around 1V. During 0-2V (orange curve), the delithiation peak reaches a plateau but a complete peak is not observed. During 0-3V (green curve) and 0-4V, a clear broad delithiation peak is observed at 1V but the intensity of delithiation peak decreases with increased voltage. Also, the delithiation peak shifted towards lower potential with subsequent cycle and in 0-4V the lithiation peak was observed at 0.86V. In all the cases, no clear insertion peak is observed. The high capacitance observed in 0-1 V is ascribed to Li insertion during the ALD deposition of LiPON on the TiO_2. The shift in the delithiation peak suggest a change in interface structure which could be due to some irreversible faradic reaction. The decreased intensity of delithiation peak also concludes towards less/no Li ion insertion into the TiO_2 and hence all the delithiation peaks observed is due to prelithiation of TiO_2 during the deposition process.

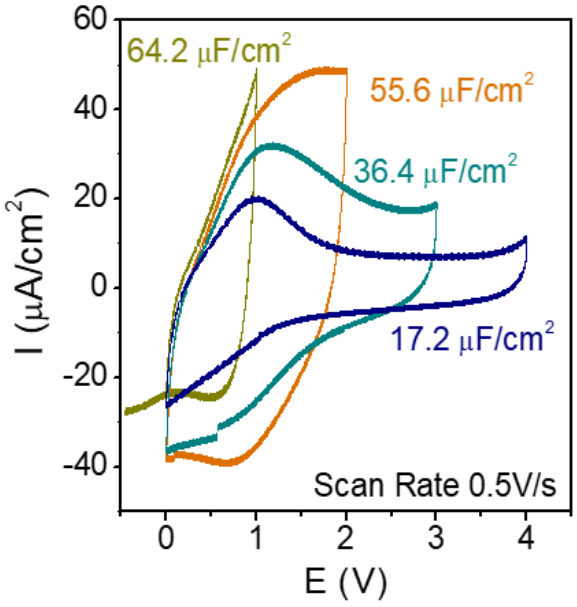

Figure 23: Characterization of asymmetric capacitor (a) CVs 0-1V to 0-4V at 500mV/s

Hence, to further understand the lithiation and delithiation peak and conclude the relaxed state of the capacitor more tests were conducted. First, an open circuit voltage test was performed with the bottom gold current collector as the working electrode. The OCV observed ranged from -1V to -0.5V, implying some pre-lithiation of the TiO_2 electrode. CVs were performed from 0-3V at a scan rate of 500 mV/s for 100 cycles to test the working limits of the capacitor stack. CVs for cycle 1, cycle 20, and cycle 100 are plotted and are shown in Figure 24 (a). In the first cycle, a capacitance of 48 uF/cm^2 was observed, dropping to 17.6 uF/cm^2 after 20 cycles, and at 100 cycles the capacitance reduces to 12.6 uF/cm^2. A broad de-lithiation peak was observed at 1.35V during the first discharge cycle. An incomplete lithiation peak follows this in between 0-0.8V. In the 20th cycle, no clear lithiation peak was observed and a small intensity delithiation peak was seen at 1.05V. During the 100th cycle, the shape of the CV changes to a more box like shape, with a small de-insertion pseudocapacitive peak

at 0.9V. The high capacitance observed during the first cycle is due to a high discharge current due to pre-lithiation of the TiO_2 during the ALD process.

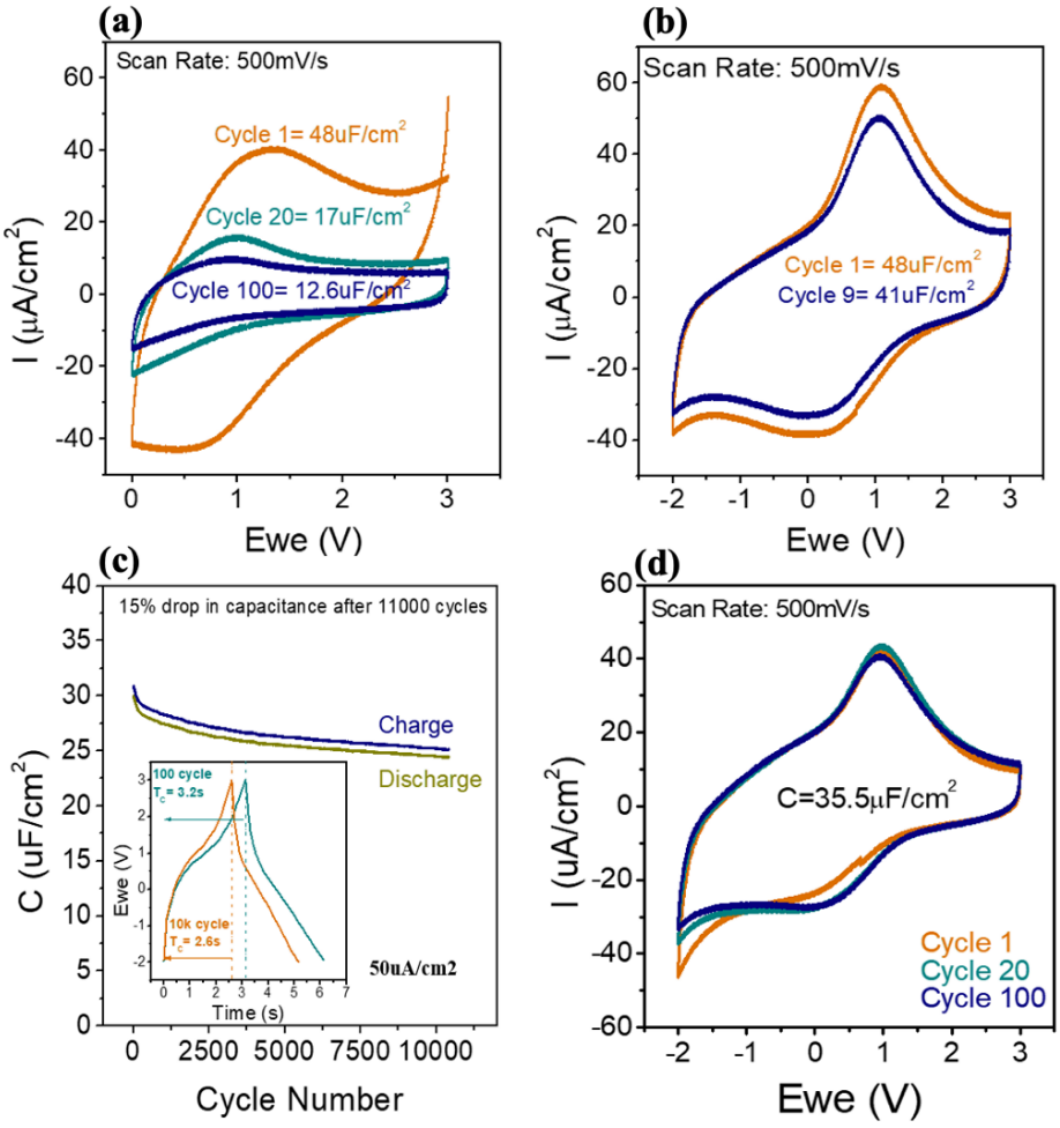

Figure 24: Characterization of asymmetric capacitor (a) CVs 0-3V at 500mV/s (b) CV between -2V to 3V at 500mV/s (c) 10000 charge discharge cycles (d)100 CV cycles post 10k charge discharge cycles

To test the complete lithiation peak and relaxed capacitor behavior, CVs with extended voltage windows ranging from (0V to 3V) to (-2V to 3V) were performed at 0.5 V/s. In between (0-3) V, a decreased capacitance was observed with no clear insertion peak. Following this, CVs were performed from -0.5V to 3V, which increased

insertion of Li ions into TiO_2, leading to increased capacitance. Capacitance increases in subsequent CVs (increased potential window), but no clear insertion peak was observed till –1 V, implying a relaxed state of the capacitor stack was below the applied voltage range. Next, a CV is performed between -2 to 3V, and a broad insertion peak was observed, ranging from -1.75V to 0.5V. When the potential is further increased to 2V, a reduction peak is observed, corresponding to the Li plating at the bottom gold electrode. Capacitance always increases in the extended negative voltage window, implying no discharge state of the capacitor in the current voltage window. Thus, the capacitor works from -2 to 3V in a two-electrode system due to reference Au electrodes and the asymmetric stack structure, leading to different relaxation states of the capacitor at different cycles. The capacitor was then tested between -2 to 3V for nine cycles, as shown in Figure 24 (b). The capacitance decreased from 48 uF/cm^2 to 41 uF/cm^2. An apparent lithiation and dilatation peak was observed which remains constant in all nine cycles. The decrease in capacitance could be due to the irreversible intercalation of Li ions into the bulk TiO_2 [cite].

Further, the stability of the asymmetric capacitor stack and reversibility of Li-ion chemistry into the TiO_2 was studied using galvanostatic charge-discharge cycles. GCD was performed between -2 to 3V at 50 mA/cm^{2,} and the result is reported in Figure 24 (c). The results show an asymptotic decrease in the capacitance from 32 uF/cm2 to 28.5 uF/cm^2 in the first 500 cycles, and then the capacitance decreases by 3 uF/cm^2 over the subsequent 10.5k cycles. The initial drop in the capacitance could be ascribed to irreversible Li-ion intercalation into the bulk TiO_2. Over the entire 11k cycles, only

a drop of 15 percent in capacitance was observed, confirming high Li ions reversibility over an extended period.

GCD was followed by one hundred CV cycles from -2 to 3V at 500mV/s. Figure 24 (d) shows the CV at 1st cycle, 20th cycle and 100th cycle. The CV peaks for all 100 cycles are observed to overlap one another. A delithiation peak at 1V and a broad lithiation peak was observed extending from -1.75V to 0.25V.

Figure 25 (a), shows a comparison between CVs at room temperature and at 60°C. The capacitor was first cycled between -2 to 3V for 10000 cycles at room temperature, followed by a CV at a scan rate of 0.5V/s. Next, the capacitor stack was heated to 60°C, cycled, and then a CV was conducted at similar conditions. The capacitance is observed to increase from 36.6 uF/cm^2 at 25°C to 46 uF/cm^2 at 60°C. It was observed that the lithiation and delithiation peak intensity increases, but the capacitance contribution from the rest of the CV curve remains constant. Since the electric double layer and electrostatic effect are limited by area, the increase in capacitance contribution is only from the pseudocapacitive effect. This is attributed to increased ionic conductivity at high temperatures leading to more intercalation of Li ions into TiO_2.

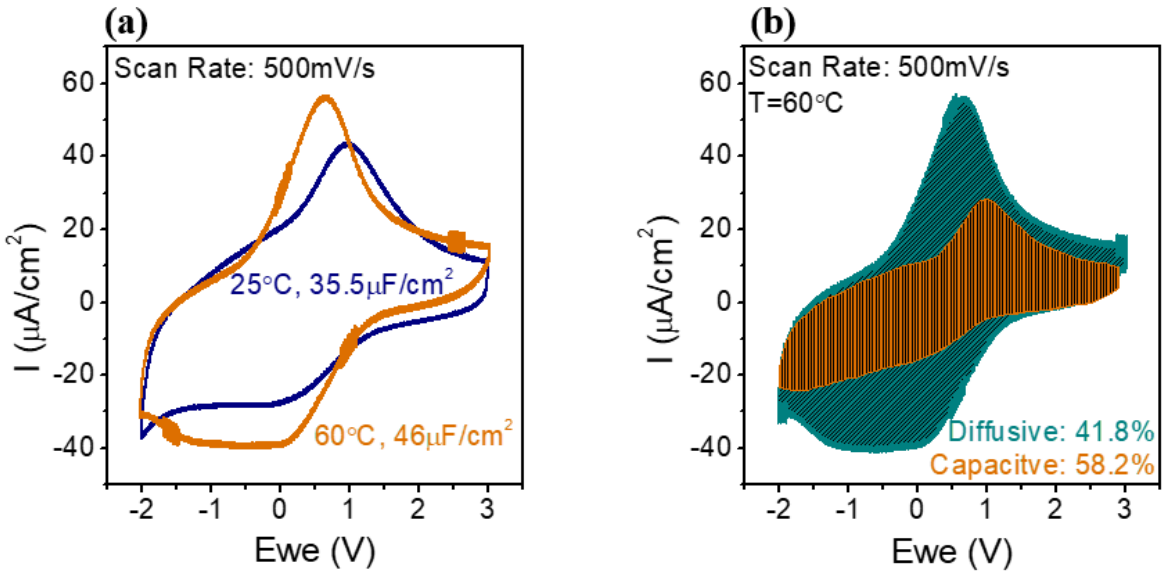

Figure 25: Asymmetric Capacitor (a) CV comparison at 25C and 60C (b) Dunn's analysis at 60C, 500mV/s

4.3.3 Dunn's Analysis

To distinguish bulk intercalation effects from surface capacitive effects CVs at different scan rates were done and are plotted in Figure SX. According to Dunn's analysis the diffusion current (i_d) is proportional to the square root of the scan rate (ν) according to equation (3), and the capacitive current (i_c)is proportional to the scan rate according to the equation (4).[115]

$$i_d = nFAC^*D^{1/2}\,\nu^{1/2}\left(\frac{\alpha nF}{RT}\right)^{\frac{1}{2}}\pi^{\frac{1}{2}}\chi(bt) \quad eq(3)$$

where C* is the surface concentration of the electrode material, R is the transfer coefficient, D is the chemical diffusion coefficient, n is the number of electrons involved in the electrode reaction, A is the surface area of the electrode materials, F is the Faraday constant, T is the temperature, and the function $\chi(bt)$ represents the

normalized current for a totally irreversible system as indicated by the cyclic voltammetry response.[115]

$$i_c = \nu C_d A \qquad eq(4)$$

where C_d is the capacitance

Using the relationships expressed above, the current response at a fixed voltage can be expressed as:

$$i(V) = k_1\nu + k_2\nu^{1/2}$$

where $k_1\nu$ corresponds to the current contribution from surface capacitve effects and $k_2\nu^{1/2}$ from diffusion-controlled intercalation. Thus, by analyzing k_1 and k_2 at a specific potential, we can quantify the fractional contribution due to these effects. Figure 4.6(b) shows the contribution of diffusion and capacitive current at 60°C. A high diffusion contribution of 41% was observed which is ascribed to Li^+ into the TiO_2 electrode. With increases in scan rate, it was observed that the contribution from Li^+ diffusion decreases and the surface capacitive effect increases. This was due to reduced mobility at higher scan rates and thus leading to an increase in the surface capacitive effects.

4.3.4 Performance of TiO_2 Capacitors

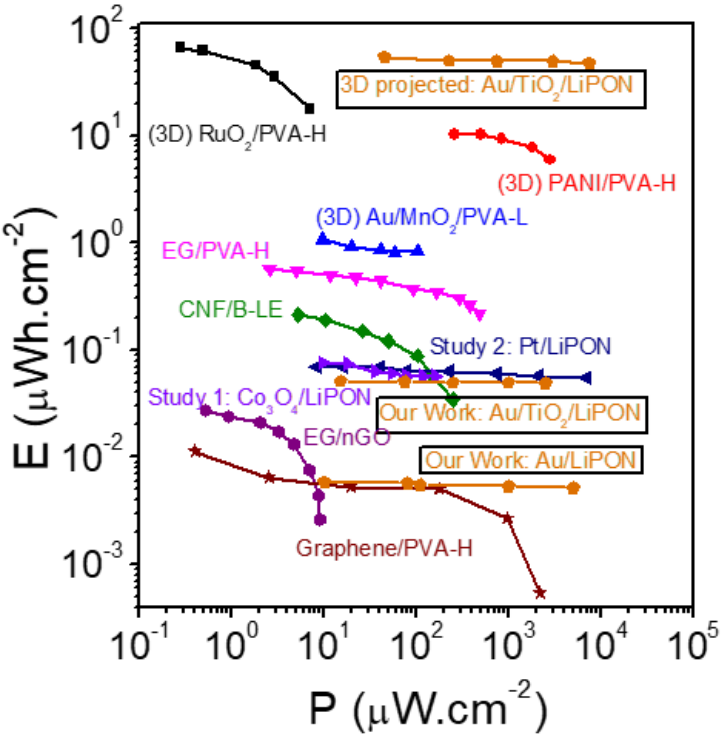

Figure 26: Ragone plot showing a comparison to current state of the art 2D and 3D capacitors

The performance of our t-LiPON supercapacitors was analyzed by calculating the energy and power density. A comparison of the energy and power density is shown in Figure 26. The maximum energy density reported for the symmetric stack is 0.0056 uWh/cm^2 and a power density of 5000 uW/cm^2. The energy density of the stack increased by a factor of 10 when the pseudocapacitive electrode was introduced. The maximum energy density reported at 60°C for the asymmetric stack is 0.0512 uWh/cm^2. The enhanced energy density is a combination of both high capacitance and larger voltage window. The energy density reported is among the top state-of-the-art all solid-state supercapacitors. Some works have reported 3D architecture allowing enhanced energy storage as shown in Figure 26. The performance of our planar work

with pseudocapacitive effects can be enhanced by a factor of 150-250 by deposition into 3D nanostructures.[101] These results will substantially enhance the energy and power density (Figure 26 (3D projection)) to meet the current energy density demands for portable and wearable electronics.

4.4 Results: ALD TiN Asymmetric Capacitors

4.4.1 Characterization and Metrology of ALD TiO_2

In an ideal case, ALD is considered as a self-limiting reaction but not all the reactions are self-limiting. Similarly, ALD TiN doesn't exhibit an ideal ALD behavior. Few studies have reported thermal TiN process with carbon contamination due to an incomplete reaction with ammonia. The ammonia is not able to completely remove the dimethyl amino group in TDMAT, thus allowing for carbon contamination.[117] This leads to a higher resistance of the TiN film due to high porosity attributed to incomplete reactivity. Thus, it makes it difficult to use ALD TiN as a diffusion barrier. However, this is an advantage in our case as the high porosity and surface contamination leads to high accessible area. The oxygen contamination into the TiN layer also leads to a small thin film of pseudocapacitive TiO_2 in TiN. Hence, in this study we explore the surface contamination and porosity of ALD TiN by XPS quantification and then fabricating planar capacitors with TiN as electrode material. Electrochemical analysis is done to understand the increase in the capacitor performance and finally we compare it to MIM capacitors in Chapter 3 and asymmetric TiO_2 capacitors to understand the increase in performance metrics.

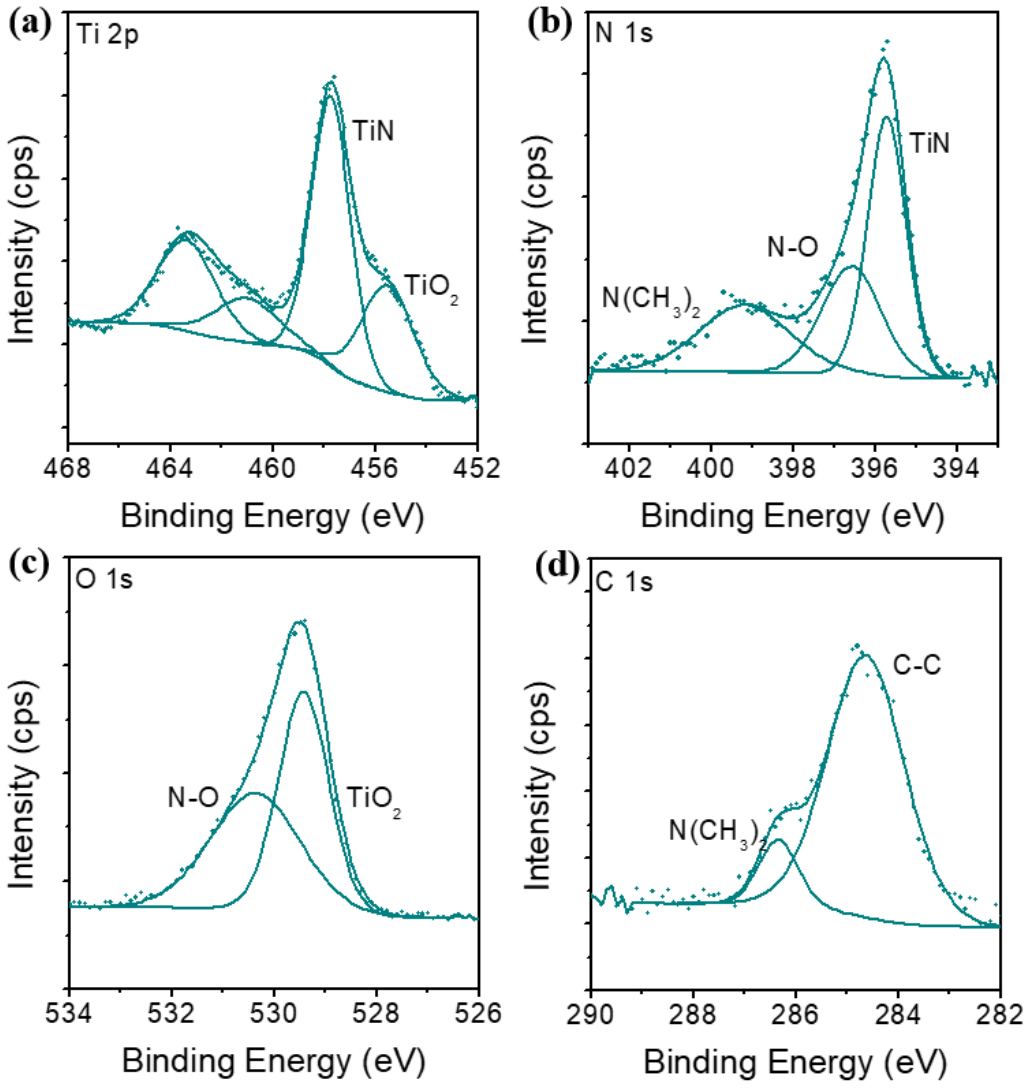

Figure 27: High resolution XPS scan for ALD TiN (a) Ti 2p (b) N 1s (c) O 1s (d) C 1s

First, ALD TiN is deposited on a gold coated Silicon wafer and an XPS quantification is performed. The wafer was air exposed before the XPS quantification. The high resolution Ti 2p, N 1s, O 1s and C 2p are shown in Figure 27 (a,d). The Ti 2p peak shown in Figure 27 (a) clearly shows presence of TiO_2 in the TiN film. The TiO_2 is due to presence of porosity in the TiN film due to the presence of carbon which when air exposed leads to oxygen contamination in the form of TiO_2. The O 1s also confirms the presence of TiO_2 with some side reactions with the nitrogen during the ammonia

purge. The N 1s peak also shows carbon contamination at 399.2 eV. This high binding energy peak corresponds to the unreacted di-methylamino which leads to high porosity films. This is further confirmed in the C 1s peak where the high binding energy peak corresponds to the di-methylamino. These results are in line with the XPS quantification of ALD TiN deposited with similar temperature and precursors. Hence, XPS spectra confirms presence of oxygen contamination and unreacted dimethyl amino group.[124]

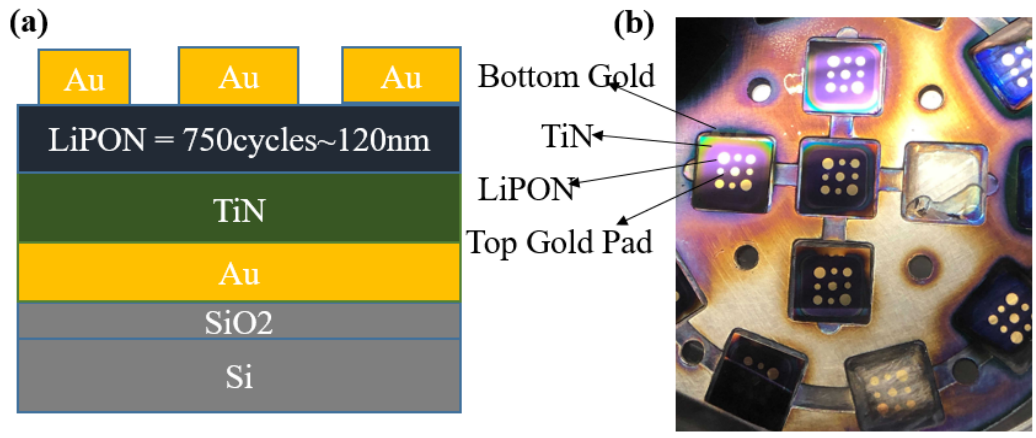

Figure 28: (a) Sketch of the asymmetric stack (b) Picture of the capacitor

To further evaluate the characteristics of ALD TiN as electrode material and the impact of non-ideal ALD behavior, a capacitor stack with a thin layer of TiN between the gold current collector and LiPON is deposited. The sketch of the stack with its FIB cross-section is shown in Figure 28 (a,b). LiPON film was then deposited at 350°C on oxy-TiN, and an XPS was conducted to quantify the film composition. The XPS result confirms the stoichiometry of LiPON film as described previously.

4.4.2 Electrochemical Characterization

Electrochemical analysis was done to understand the characteristics of the LiPON-TiN interface. EIS as a function of temperature was performed, and results were similar to the Au-LiPON-Au stack since TiN is electronically conductive. The ionic conductivity of 5.45 $*10^{-7}$ S/cm was reported at room temperature, and it increases as a function of temperature. A CV study was conducted to understand the interface phenomena and the reversibility at each electrode interface. The test was performed from 0-2V at a scan rate of 1V/s with TiN(bottom gold electrode) as working electrode (WE), followed by top gold as WE, and a CV again followed it with TiN as working electrode. The capacitance achieved with TiN as WE is 115uF/cm^2, whereas with Au as WE is 16uF/cm^2, the CV. The capacitor showed good reversibility when working electrodes were switched and the capacitance remained constant as seen in Figure 29 (a). The high capacitance achieved with TiN as WE is attributed to the high porosity and interface faradaic/intercalation of Li+ ions into the oxy phase of TiN. Post CV, an EIS was conducted to study the electrochemical changes at the interface using the Nyquist plot shown in Figure 29 (b). The arc in the high-frequency region remains constant, suggesting that the ionic conductivity of LiPON is unaltered. The second arc in the low-frequency region is attributed to the interface formed due to a faradic irreversible reaction between Li+ ions and oxy-TiN.

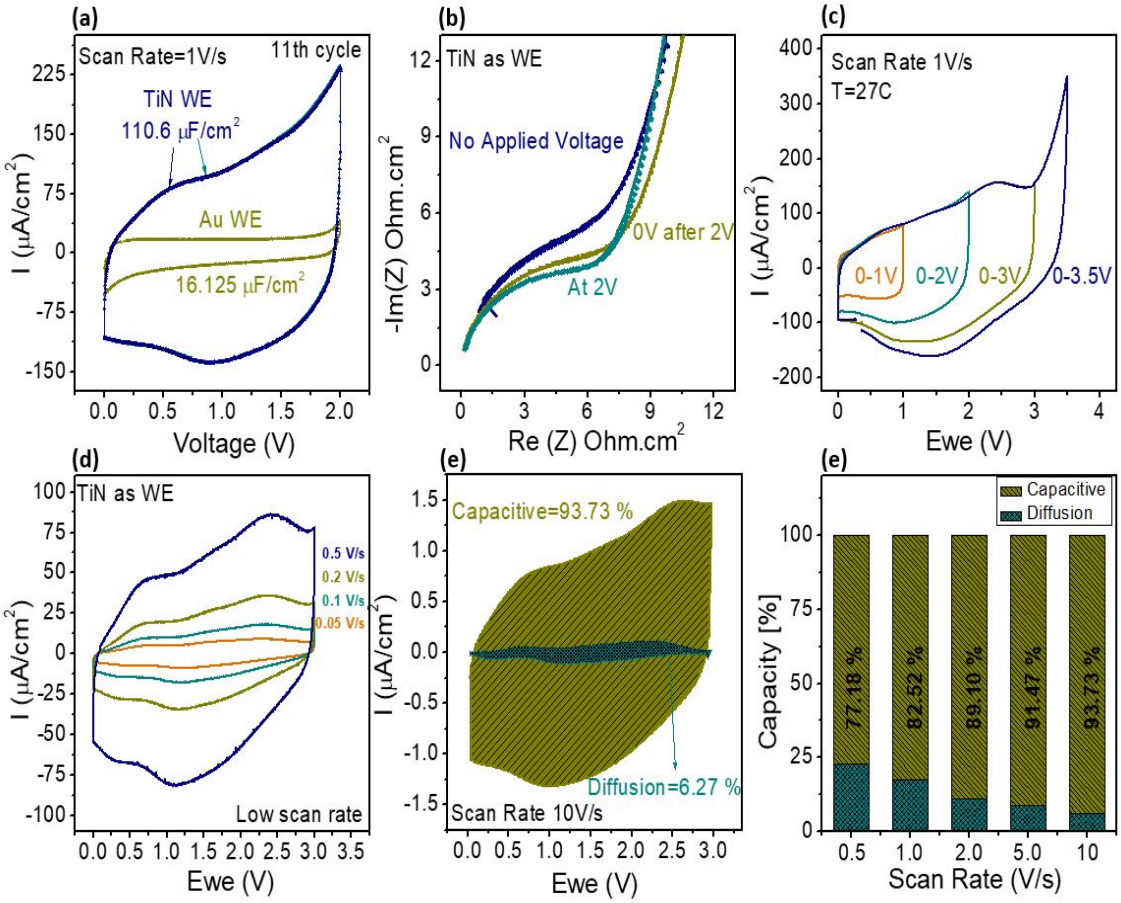

Figure 29: (a) CVs with TiN and Au as WE (b)Nyquist plot before and after applying 2V (c) CVs done at different voltage window (d) CVs at low scan rate with TiN as WE (e) Dunn's analysis at 10V/s (f) Comparison between capacitive and diffusion current at different scan rates

Following this, a cyclic voltammetry study was done to define the working limits of the capacitor stack. The CVs were done at different voltage windows ranging from 1V to 3.5 V at a scan rate of 1 V/s. From Figure 29 (c), it is seen that the capacitor with TiN as a working electrode is stable till 3 V. The increase in current density after 3 V could be associated with the breakdown of LiPON at the TiN interface. The CV between 0-2 V showed a single insertion peak at 1V and a delithiation peak at 0.6 V. When the CV was done between 0-3 V, it clearly showed two peaks in the oxidation and reduction state. These two peaks could be associated with two different phases of

TiOx present in TiN. Cyclic voltammetry between (0-3) V at high and low scan rates were done to further analyze these insertion peaks as a function of scan rates. Figure 29 (d) shows the CV curves at a low scan rate. A high capacitance of 124uF/cm^2 was observed, which dropped to 95 uF/cm^2 at 10 V/s. The insertion peaks could be observed at 10V/s, indicating the retention of pseudocapacitive behavior even at higher scan rates. The CVs at different scan rates were further analyzed using Dunn's analysis, and the results are presented in Figure 29 (e,f). At 0.5 V/s, 22.8 percent diffusion was observed, which dropped to 6.27 percent at 10 V/s. This drop-in diffusion current also explains the drop in capacitance observed at higher scan rates.

4.4.3 Stability of TiN capacitors

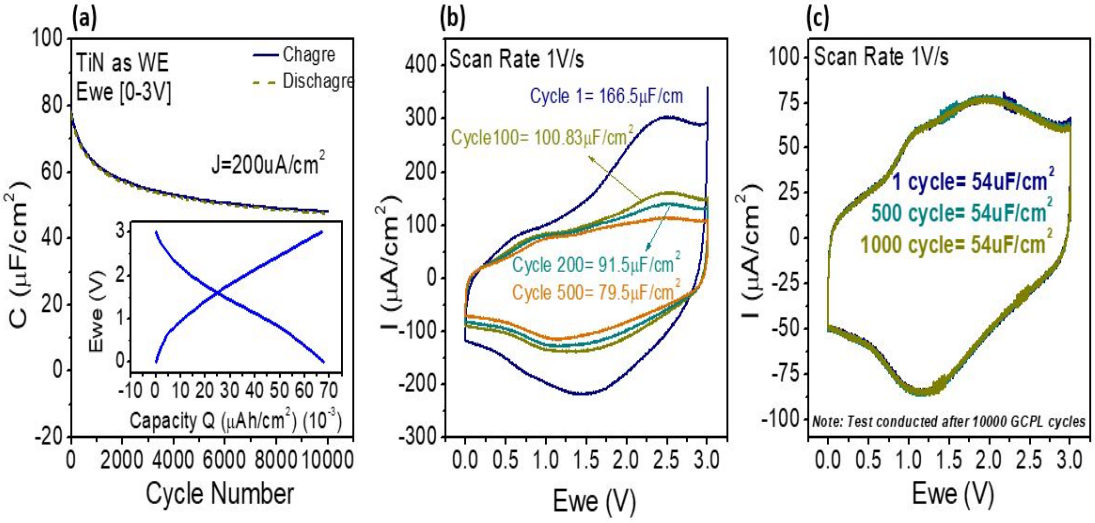

Figure 30: (a) GCD at 200uA/cm2 between (0-3) V (b) 500 CV cycles before GCD (c) 1000 CV cycles after GCD

The stability of the asymmetric capacitor was tested using galvanostatic charge-discharge done for 10000 cycles at different potential windows. Figure 30 (a) shows the capacitor is stable for 10000 cycles. A high capacity of 0.068 uAh/cm^2 is observed

when cycled between 0-3V at 200 uA/cm^2. The decrease in the capacitance observed during the cycling could be due to an irreversible reaction at the interface. CVs before and after the cyclic experiments are compared and presented in Figure 30 (b,c) to understand this decrease in capacitance. Partial merging of the two broad oxidation peaks is observed in CV after cycling. This merging could be ascribed to an irreversible reaction during Li insertion at low potential. Also, a single broad insertion peak is observed after cycling due to the crystallization of one phase of TiOx in TiN. The capacitance remains constant for the 1000 CV cycles after the GCD experiment, implying a stable interface state.

4.4.4 Performance of TiN Capacitors

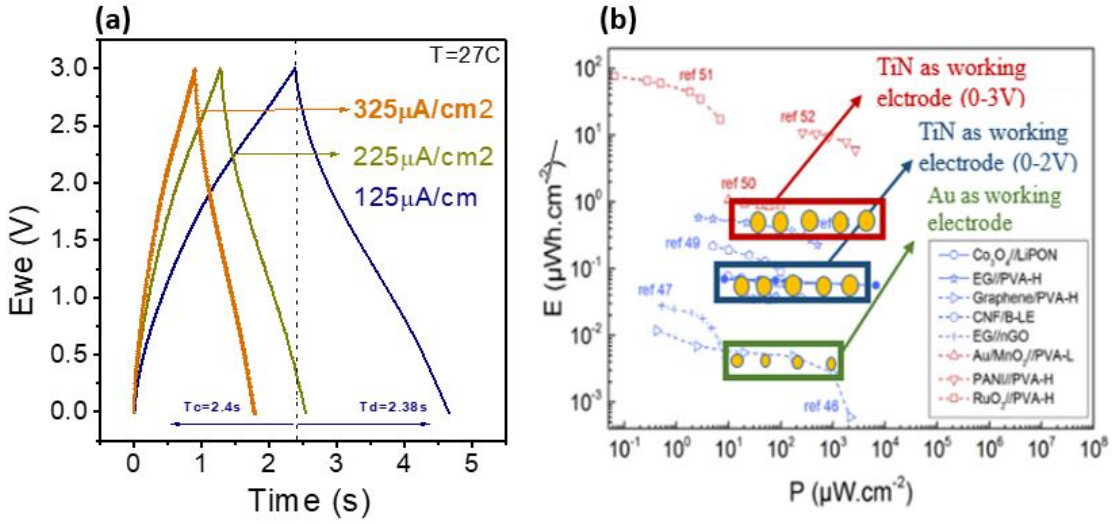

Figure 31: (a) GCD at different current density between (0-3) V (b) Comparison of thermal LiPON with gold and TiN electrodes to state of the art solid state electrolyte

The performance of the capacitors are evaluated by cycling it between 0-2V and 0-3V with both gold and TiN as WE (Figure 31(a)). With gold electrode, the time to charge the capacitor to 2 V at 125 uA/cm^2 is 0.27 s, whereas TiN is 1.22 s. This increase

in charge-discharge time is due to different charge storage mechanisms. The energy density with Au as WE is 0.0055 uWh/cm^2, increasing to 0.07 uWh/cm^2 with TiN as WE. When the capacitor is cycled from 0-3V with TiN as WE, the charge-discharge time increases to 2.4 s. The energy density also increases by order of magnitude to 0.61 uWh/cm^2. The performance of LiPON is summarized in Figure 31 (b) and compared to all solid-state thin-film capacitors. The performance of our capacitors is among the state-of-the-art solid-state 2D capacitor (blue curve) and in range with 3D in-plane configuration (red curve).

4.5 Conclusion

In this work, we have demonstrated ALD LiPON ionic behavior with two different ALD pseudocapacitive electrodes (TiN and TiO_2). Two different stacks of asymmetric capacitors were fabricated and the material property along with capacitor characteristics were studied. The TiO_2 capacitors shows a high voltage window of 5V and a high temperature stability up to 90°C. The CVs with TiO_2 as the working electrode show a clear delithiation and lithiation peak, implying a pseudocapacitive intercalation behavior. The Dunn's analysis further confirms this behavior of TiO_2 with LiPON. When cycled between 0-4V, no clear lithiation peak is observed in CVs. However, when the capacitors were cycled form -2V to 3V, the capacitor clearly shows both lithiation and delithiation implying a relaxed state of capacitor between -2 to 3V. The capacitance calculated from CV between -2 to3V is 35 uF/cm^2 and the capacitor also shows a high stability for 10k cycles. The energy density reported at 60°C is 0.0512 uWh/cm^2. The energy density is 10 times higher than the planar MIM stack. This is due to higher capacitance and larger voltage window as compared to planar MIM structure.

Thus, TiO_2 acts as an excellent pseudocapacitive electrode material with high cyclic stability with LiPON for high energy density supercapacitors

Next, we also demonstrated TiN as a pseudocapacitive electrode with a high capacitance of 120 uF/cm^2. The high capacitance observed in the TiN stack is due to two reasons. 1) TiN has contamination in the form of TiO_2 which leads to surface capacitive effects. 2) TiN ALD reaction involves an incomplete reaction between the two precursors leading to porous films. This is due to the dimethyl amino group which leads to high carbon contamination and thus increases the surface area. The energy density reported it 0.2 uWh/cm^2 and a high voltage stability upto 3V is observed. This energy density is 60 times higher than the planar MIM stack making ALD TiN as an excellent pseudocapacitive material for increasing surface area and thus energy density for all solid state LiPON based capacitors. Further integration of these capacitor stacks into 3D architecture can enhance the energy and power density to compete against state of the art capacitors available in the market.

Chapter 5: Towards Integration with On-wafer 3D Substrates

5.1 Why 3D?

In Chapter 4, LiPON shows excellent pseudo-capacitance with oxy-TiN films, resulting in higher capacitance along with high energy and power density. Despite the attractiveness of SSE, the lower energy density of planar SE capacitors compared to the liquid electrolyte remains a considerable concern. With the ever-increasing demand for energy and power density along with a push towards miniaturization, there is a need for enhanced manufacturing techniques that can allow for high aspect ratio deposition and thus allowing for increased performance of the capacitors. Also, integration with semiconductor manufacturing allows for shortening the interconnection distance thus allowing for lower parasitic losses for the next generation application.

In recent studies, it has been shown that nanoscale 3D structuring provides pathways for high energy storage batteries and capacitors.[101,102,129–132] The increase in the energy and power density is attributed to the significant increase of internal surface area in a given footprint due to 3D architecture. The areal enhancement can be quantitatively defined by the area enhancement factor ($AEF = A/A_f$), which represents the ratio of the internal surface area, A, to the footprint area, A_f, of the substrate. The realization of conformal 3D capacitors is complex and unreasonable with the traditional capacitor manufacturing techniques. However, conformal thin-film processing opens the doorway for 3D energy storage devices, allowing the fabrication of each supercapacitor component over a high aspect ratio template.

Conformal vapor phase processing such as atomic layer deposition (ALD) allows for the fabrication of large surface area/volume devices, which could allow for energy and power densities to compete with conventional liquid electrolyte electrochemical capacitors. ALD coatings have been used for years in industries for improving interface stability of batteries and manufacturing of complementary metal oxide semiconductor (CMOS) devices. Thin film SSBs give rise to desirable properties such as extended cyclability, low self-discharge rates, precise electrode-electrolyte interface control, and improved safety. ALD is an ideal technique for fabricating such devices due to its ability to grow conformal layers over complex 3D architectures. Banerjee et al used ALD to coat TiN-Al_2O_3-TiN into AAO structures to enhance the capacitance 10-100 times. On similar lines, Pearse et al reported fully conformal 3D solid state batteries where all the active material (SnN_x/LiPON/LiV_2O_5) was deposited into silicon trenches using ALD.[102] Recently, Strambini et al. reported an all-ALD capacitor into silicon trenches with Al_2O_3 and $HfAlO_x$ coatings for enhanced energy and power density. These studies conclude the increased performance of capacitors into this 3D architecture using ALD.

However, the traditional silicon trenches have limited area enhancement factor due to their manufacturing process, thereby limiting the performance of these all-ALD capacitors. Anodic Aluminum Oxide (AAO) structures have shown an area enhancement factor of 250-350 which is much higher than the silicon trenches.[133] This architecture enhancement unlocks high performance capacitors. Next, we will study the standard AAO manufacturing process and compare it to the one developed at UMD which will be used for our 3D capacitor manufacturing.

5.2 Anodic Aluminum Oxide UMD

5.2.3 AAO Manufacturing UMD

A schematic of the UMD processes is shown in Figure 32. Starting with an oxidized test wafer, layers of Cu and W are deposited using Ti adhesion layers, as can be seen in Figure 32 (a). The rough Al surface is then electropolished in a perchloric acid and ethanol solution at <5°C. Once polished the wafer is masked and regions for anodization are defined, see Figure 32 (a). The anodization is conducted at 200V in phosphoric acid at <10C and is done in the standard two step fashion, as can be seen in Figure 32 (a) - (d). Pores with diameters from ~200 nm - 450 nm, and with pore lengths varying from <10 µm to >50 µm are produced.[133]

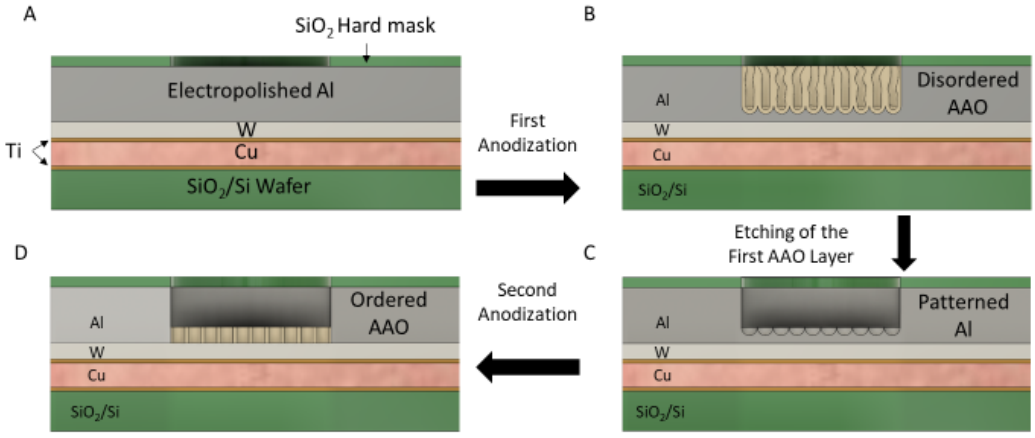

Figure 32: A schematic of the UMD developed 200V Thompson's method process. A stack of materials is deposited by PVD as shown in (A). After which standard photolithography is used to define regions for anodization with a SiO2 hard mask. A first anodization is conducted, as shown in (B), where the initial pore formation is random, but aligns at the bottom of the pores. The disordered AAO is then removed, leaving an ordered pattern of divest in the Al layer, as shown in (C). Finally (D), a second anodization is conducted producing well-ordered pores. Post processing is done to widen the pores and remove the WO_3 plug at the bottom.[133]

5.2.3 AAO Architecture

A template of anodized aluminum oxide is shown in Figure 33. It consists of a hexagonally arranged cells w where each cell is separated by a cell boundary. Each cell structure has a pore within the cell boundary. These pores run perpendicular to the aluminum substrate in the direction of electric field during the anodization process. The separation between the centers of two cell pores is called the inter pore distance as shown in Figure 33. This distance is directly correlated with anodization voltage during the preparation process. The pore diameter denoted by D_p in Figure 33 is dependent on the anodization temperature and additives in the electrolyte during the manufacturing process.[133]

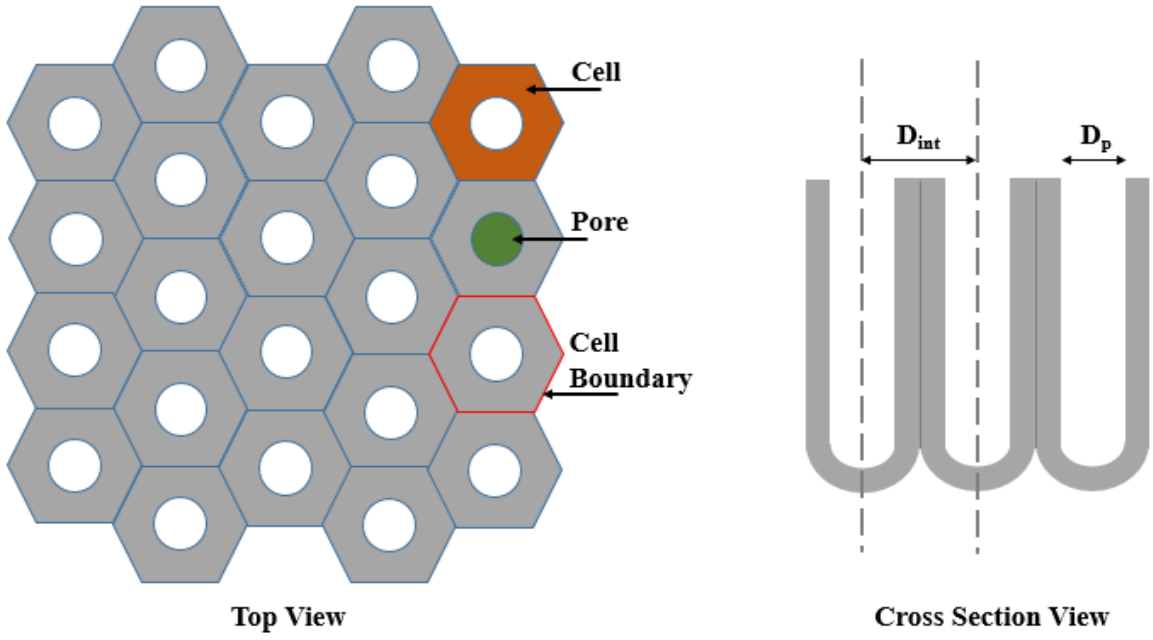

Figure 33: Anodized Aluminum Oxide Schematic[133]

5.3 Process Modification for Full ALD stack development

In order to fabricate the capacitor in 3D AAO substrates, all the capacitor stacks including the current collector should be deposited using ALD. Previously in Chapter 4, asymmetric capacitors with LiPON on top of TiN were fabricated but the top gold contact was evaporated using shadow mask. Hence, an all-ALD planar capacitor was fabricated to study the impact of top TiN on the capacitor stack. Also, ALD involves one precursor molecule interaction with one surface site at a time during the growth process, so it becomes important to have the right nucleation site for the other layers to grow. The order of precursor dose can affect the chemistry and nucleation of the thin film. Thus, to study the growth of top TiN on LiPON, planar symmetric all ALD (Au-TiN-LiPON-TiN-Al) stack was fabricated with the exact same recipe previously used. The full stack cartoon and image are shown in Figure 34. After each layer was deposited, the sample was transferred to the XPS chamber without air exposure to analyze each thin film. The XPS results showed the growth of bottom TiN and then LiPON on top of it. However, the top TiN XPS didn't show any Ti 2p signal or the signal was too low. FIB results also confirmed a missing TiN layer.

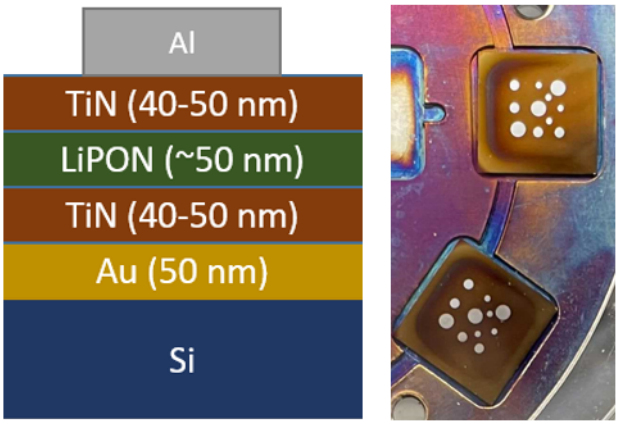

Figure 34: As deposited planar TiN-LiPON-TiN stack cartoon along with original sample

Next, to further confirm the growth of the top TiN, another stack like the one shown in figure 34 was developed but without the bottom TiN (Au-LiPON-TiN). To develop the stack, first thermal LiPON was deposited on a 10*10 mm gold chip using a custom-built shadow mask which was 8*8 mm. An XPS was conducted after the deposition of LiPON to characterize the composition of LiPON. Next, TiN was deposited on LiPON using the exact same recipe. XPS was conducted on the samples to confirm the growth of TiN on LiPON. The XPS was also done on the side of the sample on the gold chip which was covered with shadow mask during the deposition. The XPS analysis is shown and compared in Figure 35 (a,f).

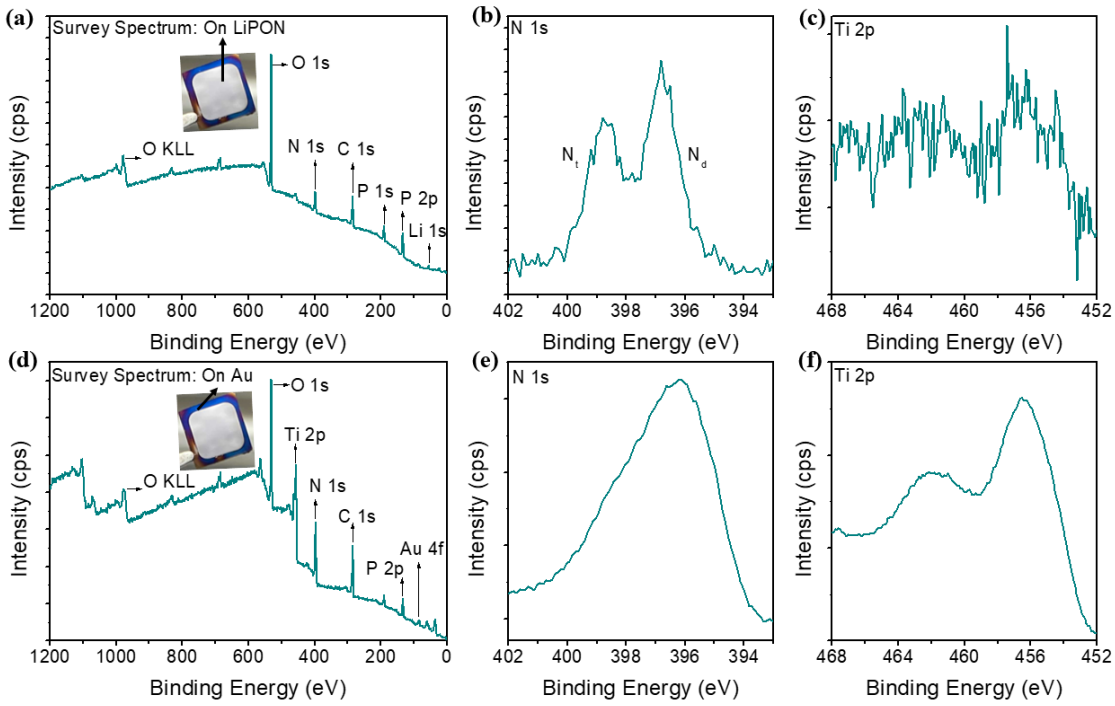

Figure 35: XPS Survey and high resolution scan, "On LiPON": (a) Survey Scan (b) N 1s (c) Ti 2p, "On Au": (d) Survey Scan (e) N 1s (f) Ti 2p

First, the XPS was done on top of LiPON after the complete stack deposition. The survey scan shown in Figure 35 (a) shows all the peaks as seen in LiPON with a lot of carbon contamination. No signs of titanium are seen in the survey scan. Though nitrogen peak is present, but it could be due to the nitrogen in LiPON and not from nitrogen in TiN. This was further confirmed using high resolution XPS scan of N 1s and Ti 2p as shown in Figure 35 (b,c). The Nitrogen peak clearly shows two different nitrogen oxidation states. These two states are like the ones seen in thermal LiPON that is associated with double and triple coordinated N in the LiPON structure. The high-resolution Ti 2p scan shows very low signal. This could be associated with TDMAT pulse on the LiPON leading to some titanium contamination. Next, XPS was conducted on the corners of the sample that was covered with shadow mask as shown in Figure 35 (d, inset). The survey scan showed peaks associated with Au 4f, Ti 2p and some

LiPON. All the peaks implies that there is presence of very thin (<10nm) top TiN and LiPON. The high-resolution scan of N 1s (Figure 35 (e)) shows a broad peak which is associate with N in TiN and some part is associated with LiPON. A clear Ti 2p signal is observed in Figure 35 (f) which confirms the presence of TiN on the corners of the Au chip.

These XPS results demonstrate that the TiN cannot grow on top of the LiPON but grows on gold. This implies the importance of nucleation site and order of precursor doses for growth of thin film using ALD. However, to accomplish the growth of LiPON on TiN we could either end the LiPON precursor differently or start the TiN dose with ammonia rather than TDMAT. This would allow for surface modification thus allowing for TDMAT reaction on LiPON. Another approach is to do a chemical modification of the nucleation sight to remove the nucleation barrier. This can be achieved by adding an OH surface group on LiPON or adding another additional layer to change the surface chemistry for growth of TiN. In our case, since we need a pseudocapacitive layer for increased energy density, we designed the new stack with an additional thin film of TiO_2 on LiPON. The TiO2 deposition starts with a water pulse and purge step which allows for a different nucleating sight. Post TiO_2 deposition, an XPS analysis is conducted which confirms the growth of TiO_2 on LiPON. Next, TiN was deposited using the exact same recipe used previously. An XPS and FIB imaging was done which confirms the growth of TiN with the modified stack.

5.4 Etching: ToF-SIMS

A key step to integration of symmetric capacitor is an etch back step. The top TiN/TiO_2 layer is electronically conductive and thus to isolate each capacitor, an etch

to the LiPON region is needed as shown in Figure 36 (a). It was at this key step that we discovered an intermixed layer is formed between LiPON and TiO_2/TiN. This intermixed layer is roughly ~20 nm, which is the target thickness of the final devices. This intermixed layer has drastic effects on the etch step.

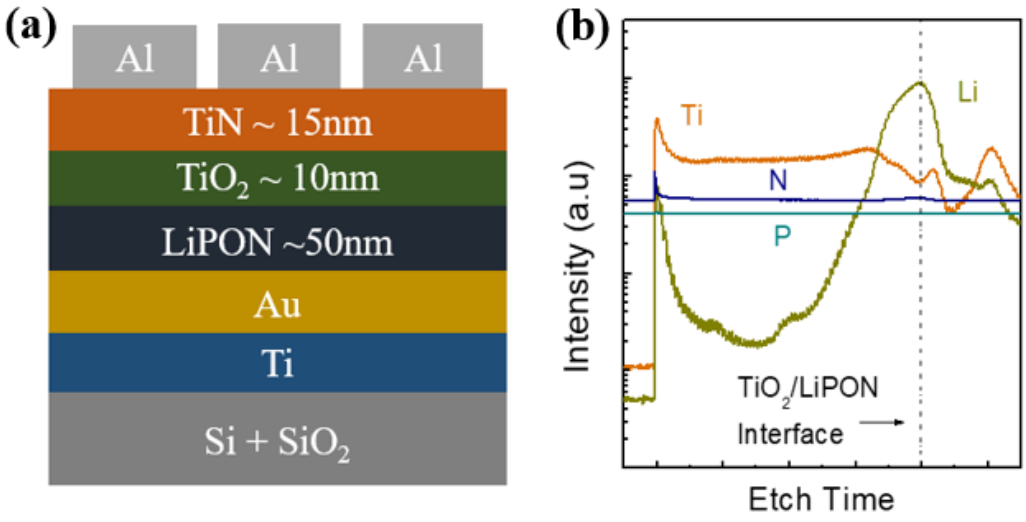

Figure 36: TOF-SIMS etching of top TiO_2 layer

We have pursued two methods of etching the top TiN layer. First, based on prior experience, we have used a coupled Ar-ion milling/time-of-flight secondary ion mass spectroscopy (ToF-SIMS). It was expected that the ToF-SIMS could be used as an etch stop by detecting the increase in the Ti signal. It was discovered, however, that the Ti is intermixing into the LiPON layer and lithium, and phosphorus are intermixing in the TiO_x. The results of one of these experiments can be seen in Figure 36 (b). Here we monitored Li, Ti, P, and N. The Li and P, are observed at the start of the etch, whereas the Ti and Li are observed everywhere during the etch process. Thus, we were unable to stop the etch in the thin LiPON region making ToF-SIMS not an ideal choice for our etch step. However, all the ToF SIMS etch concluded an intermixed region.

Thus, to investigate the diffusion we conducted in situ depth profile experiments in the XPS kratos tool in ANSlab.

5.5 XPS Depth profile

With the SIMS and FIB data both indicating and intermixed layer and XPS study. Both Li and Ti are seen all over the SIMS data during the etch, making the etch stop detection hard. Also, this intermixing could lead to degradation of the device performance. Since the length scale of this diffusion is unknown, hence, studying this interdiffusion becomes an important aspect in going forward. To study this critical phenomenon, a depth profile experiment was designed in our Kratos XPS tool. A stack was made as shown in Figure 36 (a).

The first set of experiments is done to establish the etch rate of both TiO_2 and LiPON using the argon-ion milling in the Kratos tool. In this experiment, an XPS survey scan is conducted after every 120 seconds of etching and repeated till we observe a Si peak in the scan. The first scan is done before the etching and, the Ti 2p peak indicates the presence of top TiO_2. As the etch proceeds, we start seeing the Ti peak reducing, and at 720 seconds into the etch, we start observing P 2p and N 1s peak, indicating the presence of LiPON. Next, the atomic weight percentage of each element is calculated using the area under the survey scan and is plotted in Figure 37. In the first part of the graph, the ratio of Ti 2p to O 1s remains 0.5, indicating TiO_2. The crossover points between the P 2p and Ti 2p, suggests an interface between TiO_2 and LiPON. The rise in the P peak indicates the presence of LiPON. During this LiPON phase, 5-10 percent Ti is observed, indicating the presence of Ti into LiPON. The

Titanium is seen over the entire length scale of LiPON. As we go further into the etch, the Au peak rises, followed by the bottom Ti, and finally reaching Si.

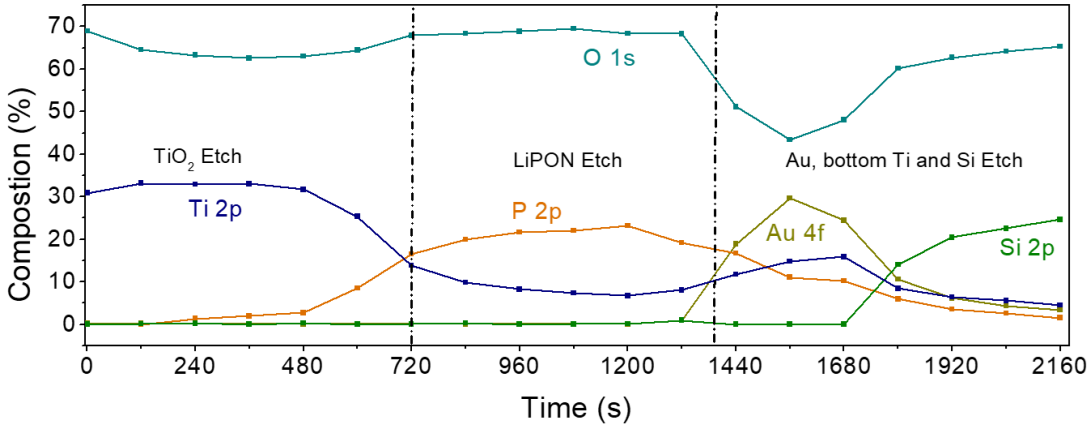

Figure 37: Depth profile to calculate etch rates for TiO2 and LiPON

Another depth profile experiment was done to further understand the length scale of intermixing. The first etch was 400 seconds long and then each subsequent etch was 60 seconds. The survey scan shows P and N peak starts showing up at 700 seconds, wherein we can also see a Ti peak. This intermixed layer is continued till 820 seconds, after which the Ti peak starts dropping down. At the end of the etch we do not see any peaks of Au and Si, which indicates that the etch was stopped in the LiPON region. The atomic weight percentage of Ti 2p, O 1s, and P 2p are calculated from the high-resolution scans and are on plotted as a function of etching time in Figure 38 (a). The composition of Ti remains constant until ~700 seconds and then starts dropping over the next few etches. The crossover of P 2p and Ti 2p at 760 seconds represents the interface. This could also be seen from the composition ratio of Ti 2p/O 1s represented in Figure 38 (b). The ratio remains close to 0.5 until ~700 seconds.

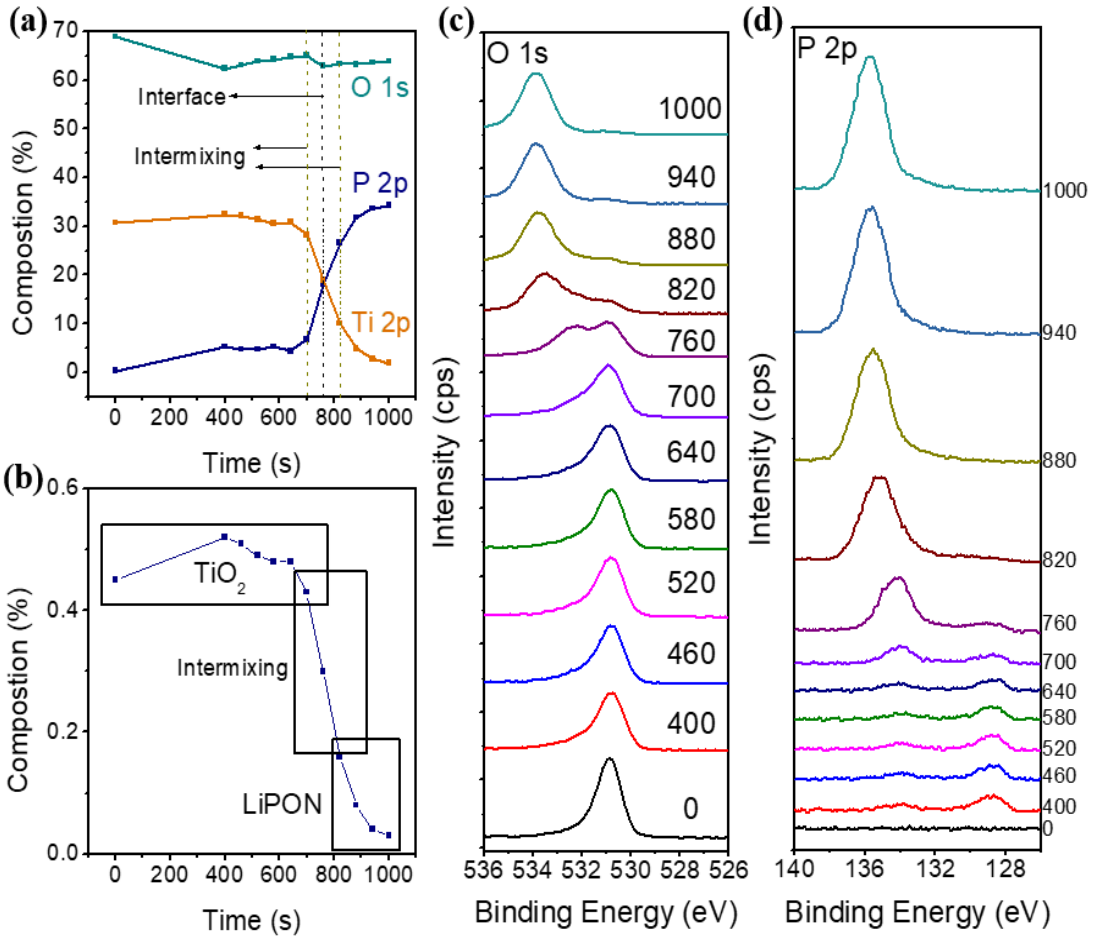

Figure 38: XPS depth profile (a) Composition percentage of Ti, O and P (b) Composition percentage of TiO_2 (c) O 1s high resolution scan (d) P 2p high resolution scan

Comparing the high-resolution O 1s and P 2p peaks, the first part of the etch represents the TiO_2 region Figure 38 (c) shows the O 1s peak having a percentage composition of 65 percent, whereas the P 2p peak represented in Figure 38 (d) has a composition ratio of less than 5 percent. The P 2p peak is at lower binding energy than in LiPON and the composition is less than 5 percent. Also, the O 1s peak is at 529-530 eV binding energy, corresponding to that of oxides.

The next part of the etch, from 700 to 820 seconds, indicates an intermixed layer. From the high-resolution scan of the O 1s peak represented in Figure 38 (c)

middle region, a second O 1s peak at higher binding energy starts to rise, and at 760 seconds into the etch, the peak shifts from lower binding energy corresponding to oxide to higher binding energy as seen in LiPON. Also, the P 1s peak (Figure 38 (d) middle region) is seen at 132.8 eV, and the atomic weight composition increases from 5 percent to 30 percent at 820 seconds. Further into the etch, the lower binding energy O 1s peak starts disappearing, and the P 2p peak at 132.8 eV starts to rise, indicating the LiPON region (Figure 38 (c) top region)). During the etch, the atomic weight composition of O 1s remains constant even though the peak shifts from the oxide phase into the LiPON phase. This could be attributed to the ratio of titanium to oxygen and phosphorus to oxygen is constant.

The conclusion of these experiments is clear. There is an intermixed layer between the TiO_2 layer and the LiPON layer. This layer is approximately ~20 nm thick, which is also the target thickness of the eventual device. This makes in-operando monitoring of the etch difficult. To mitigate this, we have developed an internal process to determine the etch rates of each material using ellipsometry.

5.6 Etch at FABLAB UMD

Due to intermixing of TiO2 and LiPON, the ToF-SIMS data could not be used as an etch stop for symmetrical capacitors. UMD team moved to the etching in the Oxford chlorine etcher in FABLAB. The tool is used in the ion milling mode and after each etch step, wafer mapping using the ellipsometry tool is done to calculate the average thickness. Average thickness as a function of etch time is plotted to calculate the etch rate. The experiment is done on ALD deposited TiN samples (UMD) at 250

C. The sample description with their respective experimental ICP power condition and calculated etch rates is mentioned in Table 6.

Table 6: Ion milling etch at FABLAB UMD, process parameters and etch rate

	ICP Power (W)	**Sample Description**	**Etch rate (nm/min)**
Experiment 1	500	ALD TiN at 250C	0.9294nm/min
Experiment 2	1000	ALD TiN at 250C	3.4695nm/min

At 500 W ICP power, the etch rate is uniform over the entire wafer. The wafer mapping, after first etch and eight minutes into the etch is shown in Figure 39(a,b). The second experiment was done at 1000W ICP power but on a different set of samples. The etch rate at 1000W is higher as compared to 500W. At 1500W, the wafer becomes unstable in the etching tool because of the quick heating of sample, leading to unstable etching condition.

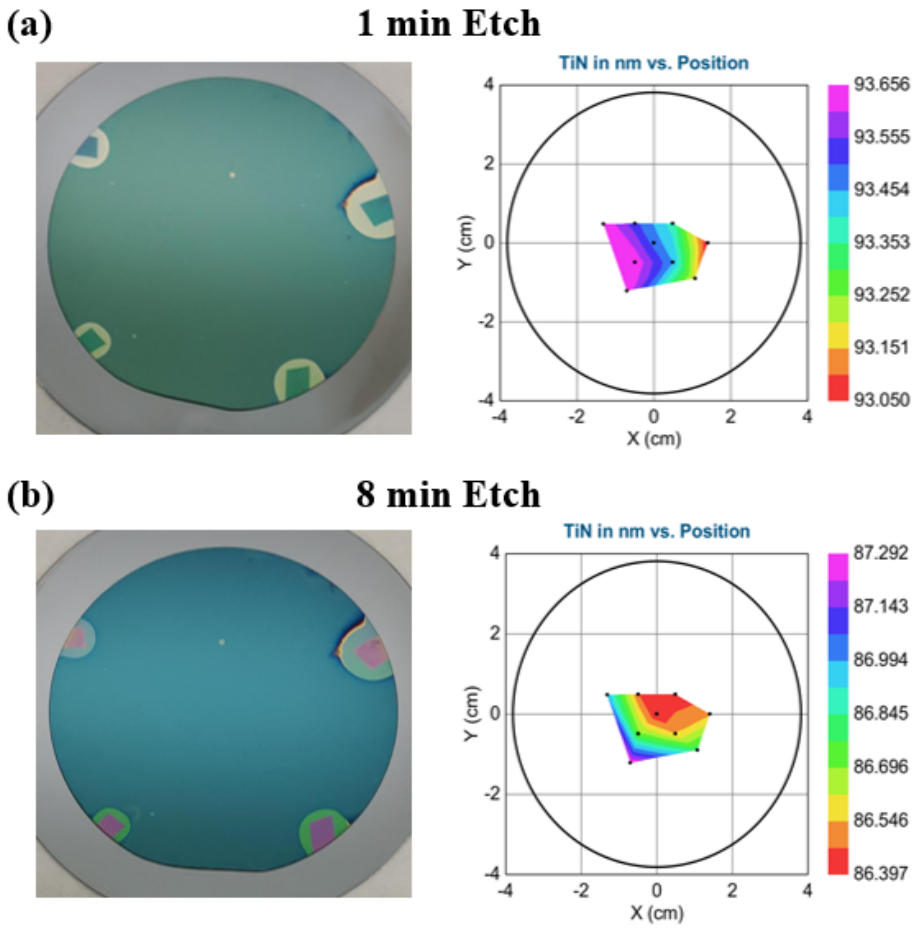

Figure 39: Etch at FABLAB of TiN sample with a picture of original wafer along with wafer mapping (a) 1 minute etch (b) 8 minutes etch

In conclusion, the UMD team has calculated the etch rates at different ICP power for both ALD TiN and TiO_2 samples. The 500W and 1000W etch condition is uniform and stable over the entire etch time. Based on the thickness of the layers, the etch conditions can be changed from 500W to 1000W. For thinner samples (<15-20nm), 500W would lead to precise etching, whereas for faster etching of thick layers (>50nm), 1000W ICP power conditions can be used.

These etch recipe and etch rates were then used for etching a planar sample with TiO_2 and TiN on top of LiPON as shown in Figure 36 (a). The XPS results are shown in Figure 40 (a,d). The Ti 2p, O 1s, Li 1s, and P 2p were chosen as representative of each material and tracked as a function of etch time. Two spectra are shown per element, a control(green) and 5 minutes of etching (blue). The control spectra (no etch) clearly show the presence of TiN with peaks in the Ti spectra at 459.5 eV and 465 eV; notably no Li and very little P are seen. After 5 minutes of etching the Ti peaks decrease to within the noise of the signal. Furthermore, the Li 1s peak begins to show at 56 eV, the O 1s peak shifts to higher energy, and LiPON components Li, O, and P are easily seen, indicating that LiPON has been exposed at the milled surface.

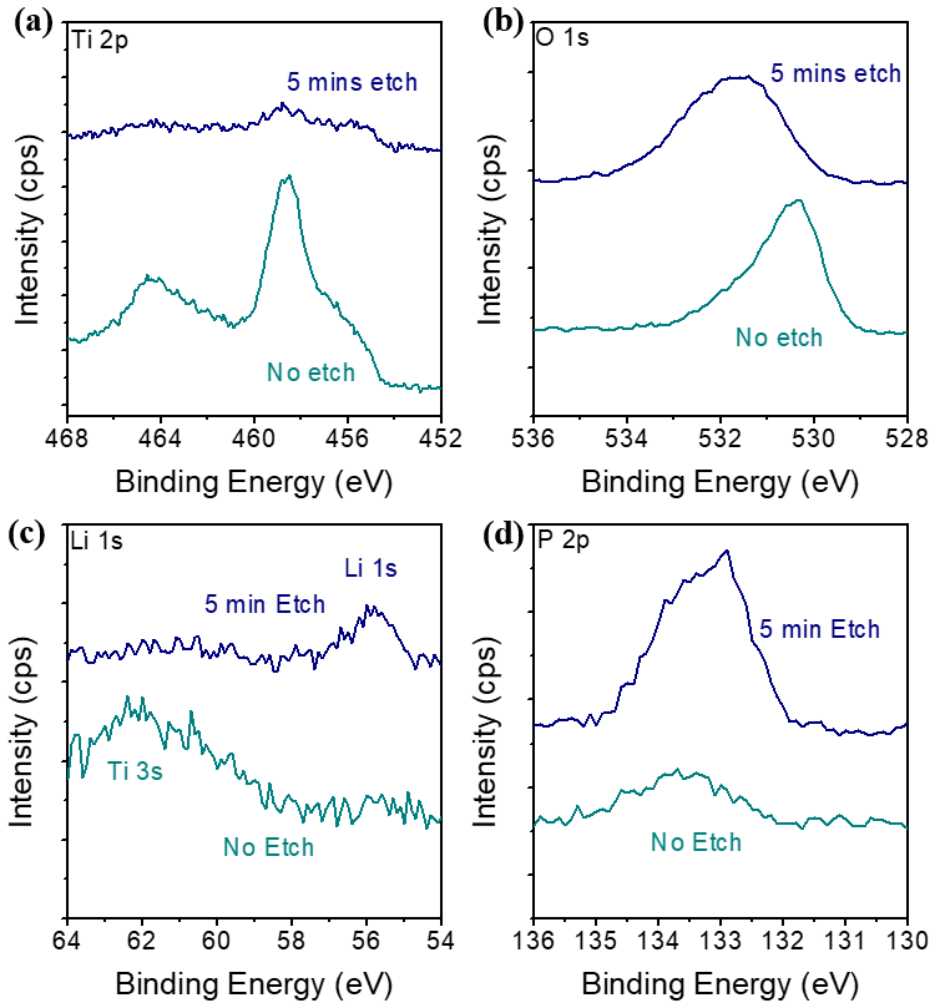

Figure 40: High resolution XPS characterization before etch and after 5 minutes of etch (a) Ti 2p (b) O 1s (c) Li 1s (d) P 2p

The etched samples were then tested in a dot-to-dot configuration, so that any shorting due to conductive surface routes can be eliminated. The electrochemical impedance spectroscopy (EIS) clearly shows a semicircle at high frequency and Warburg tail at low frequency, indicating both ionic activity and electrical isolation. Cyclic voltammetry was conducted while varying which interface was the working electrode. In Figure 41 (a), CVs were conducted from 1-10V/s with TiO_2 as the working electrode. Lithiation/delithation peaks are clearly seen ~1.5V and ~1V respectively.

When Au is used as the working electrode the CVs take on a much more box like shape with some Au/Li alloying present at low potentials Figure 41 (b).

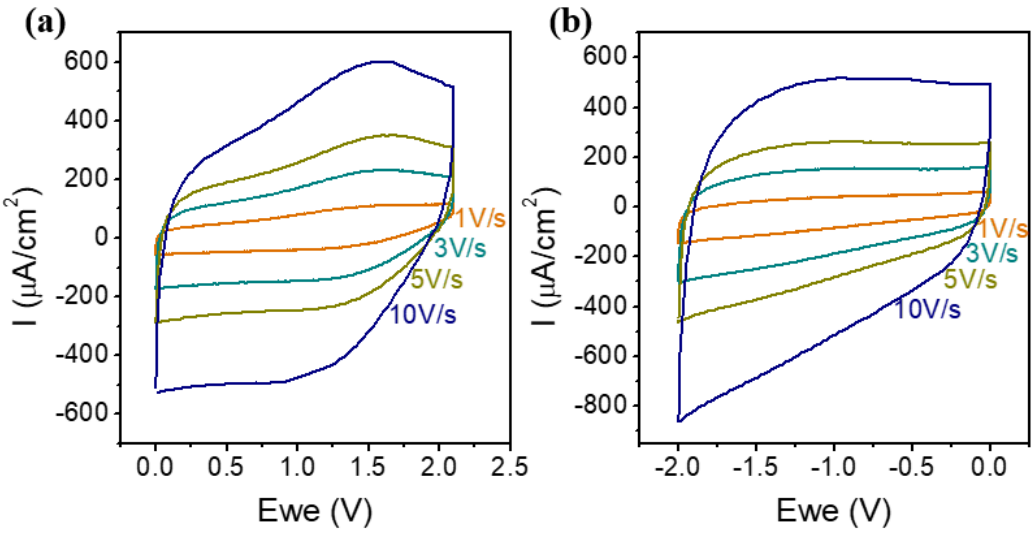

Figure 41: CVs at scan rates form 1 V/s to 10V/s (a) Al as WE (b) Au as WE

5.7 Integration into 3D AAO pores for High Energy Density

The final stage to achieve high energy and high frequency capacitors is to integrate the thin film deposited on planar substrates into the 3D AAO pores. In our prior work, we have observed that the 2D recipe needs to be modified for deposition into 3D AAO pores. This is due to the small pore diameter (<450nm) and greater pore depth (5-10 μm). This high aspect ratio not only requires more precursor dose (double than 2D) but more wait time between each reactor pulse to increase reaction time. Along with more reaction time, carrier gas flow is increased, and the butterfly valve is closed during each pulse to allow precursor to reach deep down into the pores. The new recipe for 3D substrates was then used to deposit the complete capacitor stack. Figure 42 (a,f) shows the complete process flow of the 3D capacitor fabrication. Before the

first process step, the 3D AAO stack was developed on a 3 inch silicon substrate which was then used for the 3D capacitor fabrication. Figure 42 (a) shows a zoomed in image of the AAO pores with diameter less than 450 nm. The AAO substrate was heated to 250°C for an hour before the bottom TiN deposition. The deposition was done at 250°C for 500 cycles. This was followed by a thin layer of TiO_2 at similar reactor pressure and temperature conditions. After the deposition of bottom current collector and electrode, a thin film of LiPON was deposited at 350°C as shown in Figure 42 (d). Post LiPON deposition, the temperature of the reactor was slowly brought down to 250°C and then step 2 followed by step 1 was repeated for complete ALD capacitor stack. The sample was taken to the load lock under vacuum and cooled. The final deposition step was conducted in FABLAB. A similar shadow mask used before for top contacts was designed but with the exact same size as AAO pores stack. 1 μm of aluminum was evaporated on top which was finally etched for complete capacitor stack as shown in Figure 42 (g).

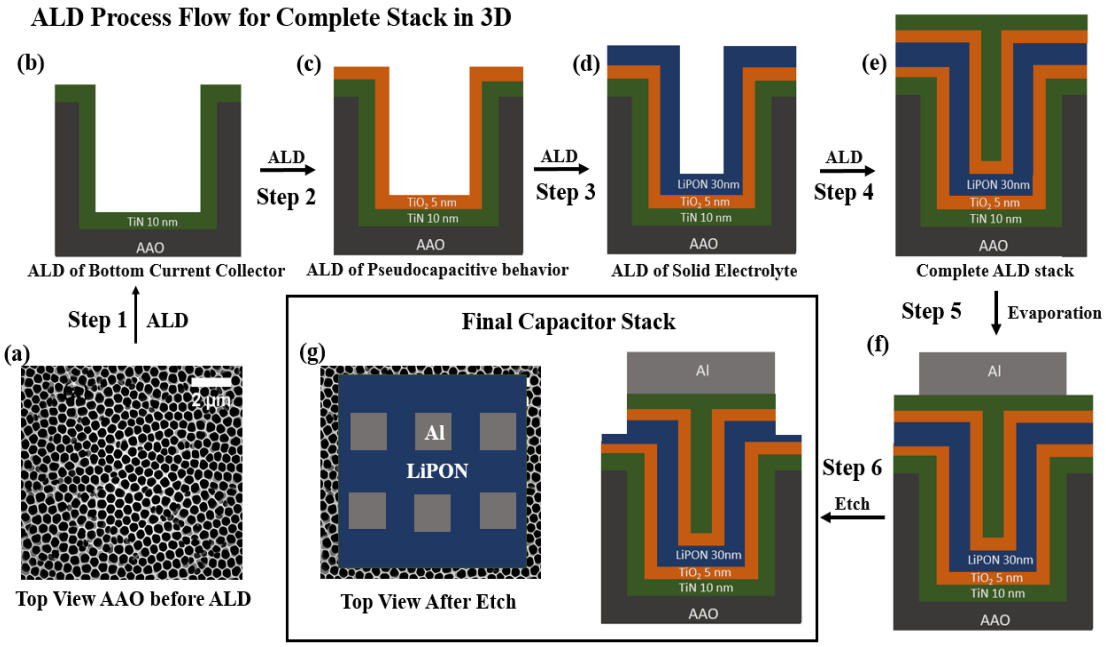

Figure 42: ALD process flow of complete capacitor stack in 3D (a) SEM image of AAO before deposition (b) Schematic after bottom TiN electrode deposition (c) Schematic after bottom TiO2 pseudocapacitive electrode deposition (d) Schematic after solid state electrolyte deposition (e) complete ALD capacitor stack (f) capacitor stack with evaporated aluminum as hard mask (g) full stack view after etching

Figure 43 (A-I) show a schematic of the device structure in the first column, cross-sectional SEM image showing the individual layers in the middle column and electron diffraction spectroscopy confirming the presence of all appropriate elements. The depositions begin with TiN, as can be seen in Figure 43 (A-C). After the deposition a piece of the wafer was removed and cross-sectioned, an example of the results are shown in Figure 43 (B). To confirm the presence of the appropriate elements an EDS line scans were conducted. In each case a monitor element was chosen and tracked across the length of the pores. Figure 43 (c) traces the Ti concentration (blue line) confirming its conformality. The LiPON electrolyte is then deposited, as shown in Figure 43 (D). SEM cross-sections, Figure 43 (E), confirms the presence of the LiPON

layer. Again, an EDS line scan tracking P (red line) confirms its presence. Finally, the last two layers were deposited, as shown in Figure 43 (G). Cross-sectional SEMs confirm the presence of all expected layers (Figure 5.12(H)). Once again, the Ti peak was chosen as the tracking element (red line), confirming the presence of all desired layers.

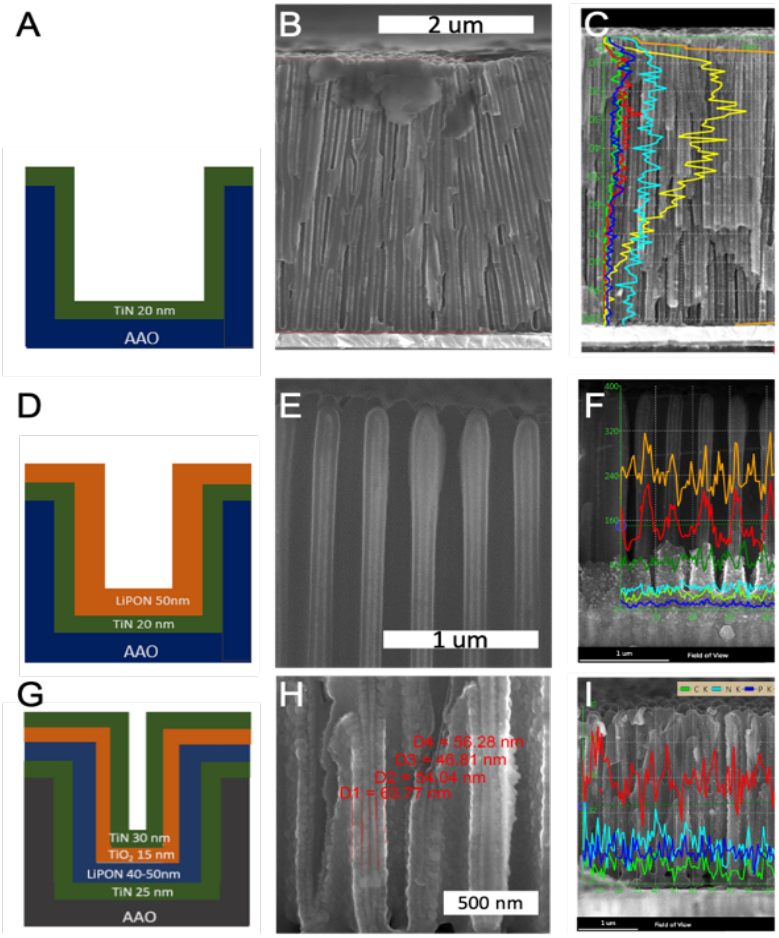

Figure 43: A schematic of the fabrication process along with associated SEM cross-sections and EDS. Conformality of the TiN later is shown in (A-C). LiPON conformality is shown and confirmed in (D-E). Finally, the final two layers, TiO2 and TiN are deposited and their presence is confirmed via EDS

Next, the top aluminum was deposited on the completed stack and etching was performed in the dry etching tool in FabLAB. Figure 44 (a) shows the complete

capacitor stack with top aluminum contact. The samples were then etched with the same etch rates that were developed using the 2D samples. Although, the etch recipe and etch rates were decided but a careful approach was taken to etch the sample. Thus, after every few minutes of etch the samples were electrically tested and an XPS was performed to further understand and confirm the etch progress. Figure 44 (b,d) shows some pictures of the sample after subsequent etching. However, in all the cases the sample was shorted, and we could see presence of Ti everywhere.

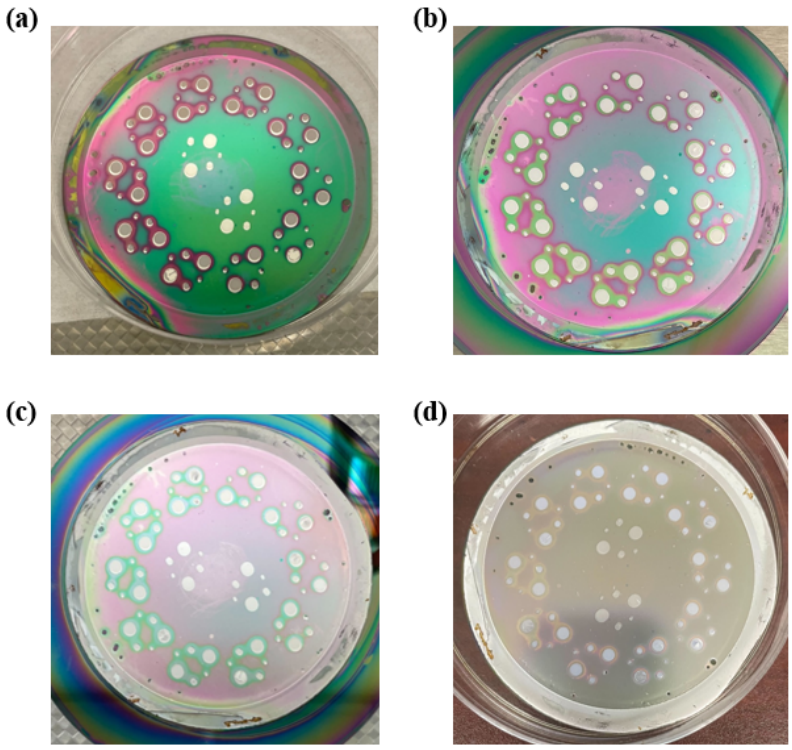

Figure 44: Full stack images after etching (a) 0 minutes (b) 8 minutes (c) 16 minutes (d) 24 minutes

Although, 3D depositions into AAO pores might be the solution for increasing efficiency for future generation energy and power density demands, however a big challenge in 3D thin film ALD fabrication is to detect defects or problems during or

after deposition. There could be several ways for the sample to not work and that could be hard to detect using FIB-SEM images and EDS analysis. One of the reasons could be a short in one of the AAOs where the LiPON is too thin and thus leading to a contact of the top and the bottom TiN. Another reason could be that the LiPON layer is not conformal inside the AAO structure and thus the thin film along with the intermixing of titanium and Li could lead to shorting. Defect density over a 3 inch wafer could be very high. This could be due to a bad run of any of the thin film coating and thus ultimately leading to shorting. AAO is brittle and internal delamination due to temperature changes during the deposition or etching process could also lead to the samples stack not working. Also, etching of TiN using the Ar ion milling in plasma could lead to degradation of films or degradation of AAO, thus further leading to shorting. Another reasons which we could confirm using SEM images is shown in Figure 45 (a). The ALD growth of LiPON tapers off inside the AAO pores and couldn't reach the bottom of the samples. This could leading to shorting of the top and bottom TiN. In Figure 45 (b), which shows a top-down, cross-sectional SEM image of the completed material stack in the UMD 3D template. Again, all of the layers are present

as expected, however further optimization of the individual ALD processes are required to maximize component utilization in the pores.

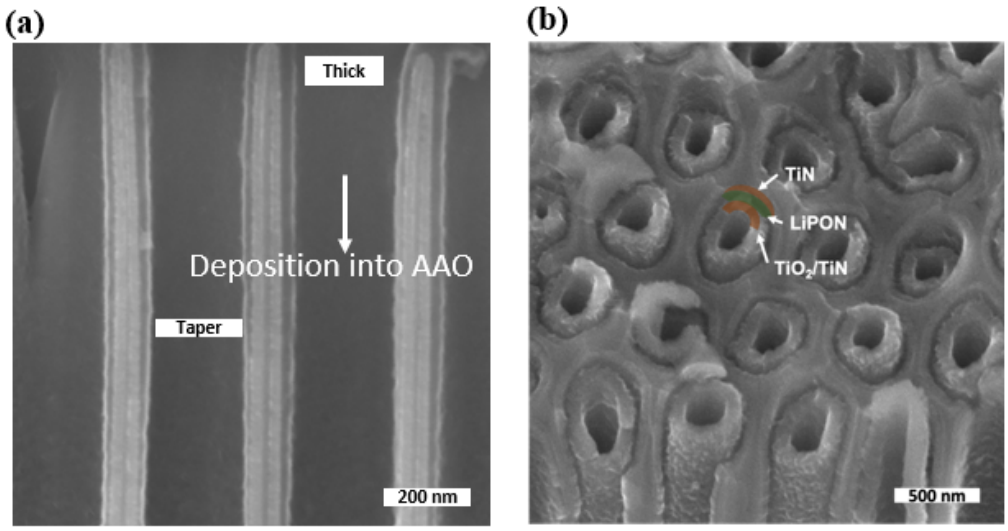

Figure 45: : 3D depositions in AAO pores (a) SEM images showing incomplete deposition inside the pores (b) SEM images showing need for optimized recipes

5.8 Conclusion

The deposition and etching of symmetrical stack provides a cumulative insight into fabrication of nanoscale 2D and 3D solid state LiPON capacitors. During the fabrication of symmetrical stack (TiN-LiPON-TiN), we understood the importance of nucleation site for vapor phase chemistry of different precursors and how changing the precursor order can impact the deposition of thin film materials. XPS and ToF-SIMS characterization provides conclusive evidence of TiN growth on gold substrate but not on LiPON. We observed the influence of 'OH' group using a thin film of TiO_2 allowed for growth of the top TiN current collector. Thus, an all ALD 2D symmetrical stack is an important step in understanding the process development for integration into 3D nanostructures.

Next, the impact of intermixing during ALD deposition was realized during ToF-SIMS etching where Ti and Li signals were seen during the entire etching process. This was further confirmed using XPS depth profile experiments where we could understand the length scales of etching in our samples and the affect that the intermixing can have in ultra-thin film depositions (<20nm). The XPS depth profile clearly indicated an intermixed region close to 12-18 nm. The study of intermixing highlights the important considerations that needs to be taken during the etching process and 3D depositions.

Finally, integration of ALD stack was done into 3D AAO pores to realize the enhanced energy and power density of these all solid state capacitors. However, the challenges outperforms the solutions for 3D integration at this moment. Some of the challenges that need to be worked on for future depositions 1) Optimization of recipe is required at each and every stage of ALD deposition. Deposition of TiN on Al_2O_3 is different from deposition of TiN on TiO_2. 2) The growth rate along with physical properties might alter during the 3D deposition in comparison to 2D deposition. 3) Understanding defect density in our ALD process is critical in designing AAO channel diameter and properties. 4) Impact of etching using Ar ion milling for our stack needs further understanding.

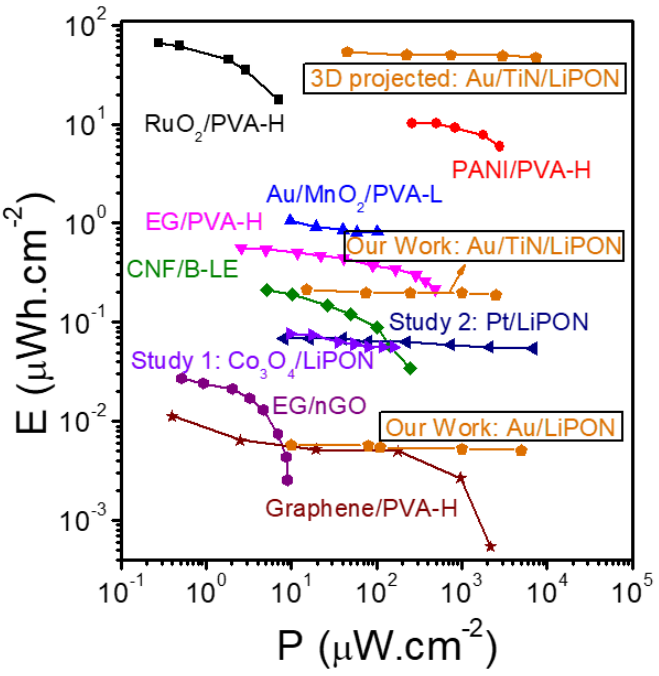

Figure 46: Ragone plot showing a comparison of 2D vs 3D LiPON capacitors

Looking forward, nanoscale 3D structuring with an advantage of on chip deposition is one of the ways to enhance the energy and power density matrix of solid-state electrolyte which are limited by low ionic conductivity in comparison to liquid or gel electrolytes. Figure 46, shows the enhancement in energy density due to 3D Nano structuring in comparison to planar 2D solid state LiPON capacitors. With an enhancement factor of more than 250, these capacitors can compete against the state of the art liquid or polymer gel capacitors with an advantage of high voltage and temperature stability.

Chapter 6: Conclusion and Future work

6.1 Conclusion

In this work, we study and discuss the fabrication, process development, materials, electrochemistry, and application of thin film solid state supercapacitors. The motivation for this work is significantly from previous work by our group and collaborators. Our group demonstrated the development of thin film solid state electrolytes with high ionic conductivity and their application in developing high-performance nanostructured batteries. The significant achievement was the development of new polymorphs of ultra-thin LiPON using ALD. Also, Banerjee et al. in 2009, used 3D nano-structuring to enhance the energy density of Al_2O_3 capacitors using ALD. The contribution of these works leads to the present study where we develop and characterize thin film solid-state electrolytes, mainly plasma and thermal LiPON, for supercapacitors applications using micro-processing techniques.

The primary focus of this thesis is to develop all-solid-state thin film capacitors using ALD for high frequency and energy density applications. The work defines two types of capacitors 1) EDLC for high-frequency application and 2) Pseudocapacitors for high energy density. In the first part of the work, we develop capacitors with two different polymorphs of ALD LiPON (thermal and plasma) as solid-state electrolytes between gold electrodes. The LiPON polymorphs show dual frequency behavior, where in low frequency (<10 kHz) they show ionic behavior, and beyond this, they show electrostatic behavior. This dual frequency behavior allows for the high and wide frequency range of these capacitors, which rivals or surpasses the state-of-the-art MLCCs available in the market for decoupling application.

In the next part of the work, we develop all solid-state supercapacitors with TiO_2 and oxy TiN as electrodes for high energy density supercapacitors. LiPON shows

high voltage stability up to 5V along with high-temperature stability. The energy density of the supercapacitors increases 100 folds as compared to the LiPON EDLCs. The ALD TiN shows a higher surface area than gold electrodes due to the incomplete reaction leading to porous films. The surface oxygen contamination in this porous film leads to pseudocapacitive behavior. Both these effects lead to high energy and power density supercapacitors.

In the last part of the work, we develop process and etch recipes to fabricate all ALD solid-state supercapacitors into 3D nanostructures. We study the intermixing of electrodes and electrolytes to understand better the interface and its impact on the etching using XPS depth profiling experiments. Next, we develop time based etches to fabricate planar symmetrical pseudocapacitors for their fabrication into 3D AAO structures. Finally, we develop recipes for integration into 3D AAO pores. To quantify depositions into 3D structures and understand the process development of ALD LiPON and ALD TiN, we use FIB-SEM, EDS, and XPS. Though unfinished, this works provides profound knowledge and understanding of fabrication and electrochemistry of all solid-state supercapacitor along with integration into 3D nanostructures for high energy and high frequency supercapacitors.

In summary, the major achievements of this dissertation include (1) Development of first reported ALD LiPON capacitor showing dual energy storage behavior and their application into high frequency domain (2) Development of all ALD LiPON supercapacitors for high energy density using pseudocapacitive behavior (3) Demonstration of intermixing of Ti and Li during depositions using ALD and its impact on fabrication and device performance (4) Development of etch recipes for fabrication

of all ALD symmetric capacitors (5) Development of solid electrolyte and electrode recipes for integration into 3D nanostructures.

6.2 Future Work

1.) As seen in chapter 5, during the symmetrical deposition of TiN-LiPON-TiN capacitors, there was no TiN deposition seen on top of LiPON. ALD is a vapor phase chemical process which involves reaction between precursor and nucleation site. Thus, combination of precursor and nucleation site plays an important role in the ALD process development process.

A study can be conducted where the thermal LiPON ALD process can be modified, the process can end either with DEPA or LiO^{t}Bu pulse. This would create different nucleation site for top TiN deposition. Similarly, TiN deposition can be started with NH_3 pulse or TDMAT to understand the chemistry. Further, investigation of the process can be done using XPS analysis. Using XPS depth profiling, cryo-TEM and EELS we can investigate in detail the interface chemistry. Finally, electrochemical analysis can be done to investigate the performance of the capacitors.

2.) Fabricate Au-TiN^{ALD}-LiPON-Au and Au-$TiN^{Sputter}$-LiPON-Au, compare the performance impact from dimethyl amino group leading to higher surface area in case of ALD TiN. XRD and in-situ mass spectroscopy can be conducted to understand the ALD TiN chemical formulation and reaction chemistry. XPS depth profile and cryo-TEM can be used to analyze the interface chemistry and their impact on capacitor electrochemistry.

3.) A study can be conducted to understand the impact of intermixing during the capacitor fabrication. Deposition of LiPON on TiN and understanding the impact of intermixing on the performance of EDLC capacitor using depth profile and electrochemical analysis. Next, introducing a pseudocapacitive TiO_2 in between and understanding the intermixing. Finally, fabricating a symmetrical stack and study the intermixing using XPS depth profile and cryo-FIB. Further, temperature reliability of the stack can be conducted by heating these capacitor and conducting a depth profile to study different interfaces in the capacitor structure.

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