Nuclear Inst. and Methods in Physics Research, A 1046 (2023) 167673

Contents lists available at ScienceDirect

Nuclear Inst. and Methods in Physics Research, A

journal homepage: www.elsevier.com/locate/nima

The MAPS foil

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ARTICLE INFO

Keywords:
Monolithic active pixel sensors
Solid state detectors

ABSTRACT

We present a method of embedding a Monolithic Active Pixel Sensor (MAPS) into a flexible printed circuit board (FPC) and its interconnection by means of through-hole copper plating. The resulting assembly, baptised "MAPS foil", is a flexible, light, protected, and fully integrated detector module. By using widely available printed circuit board manufacturing techniques, the production of these devices can be scaled easily in size and volume, making it a compelling candidate for future large-scale applications.

A first series of prototypes that embed the ALPIDE chip has been produced, functionally tested, and shown to be working.

1. Introduction

Monolithic Active Pixel Sensors (MAPS) have a number of distinctive properties, which make them the technology of choice for numerous tracking and vertex detectors, where low material budgets and high intrinsic resolutions are key (e.g. [1–10]). The ALPIDE chip [11], which was developed for the new ALICE Inner Tracking System ("ITS2"), for instance, achieves an intrinsic spatial resolution of 5 µm and has a nominal thickness of only 50 µm, corresponding to 0.05 % of radiation length (X_0). The ITS2 covers an area of 10 m^2; it has recently been installed and is taking data at LHC, marking the first large-scale application of MAPS in high energy physics. A 60 m^2 tracker is envisaged for the ALICE3 detector, targeting installation during the LHC Long Shutdown 4 (2033–34), and asking for new module concepts that can be industrialised, while at the same time meeting stringent material budget constraints [4].

The R&D for replacing the inner-most layers of ITS2 by new MAPS layers (ITS3 project [3]) based on bent, wafer-scale sensors is currently ongoing. Through a reduction of the material budget by a factor of seven with respect to ITS2 and moving closer to the interaction point, ITS3 aims to achieve unprecedented position resolution figures. First results demonstrate the feasibility of bent MAPS [12], paving the way to new, optimised detector geometries. Within this R&D for bending thin silicon, the here-presented technique to both protect and interconnect sensors was conceived, making the technology potentially even more versatile while adding only a small amount of material.

Current lowest mass detector assemblies are typically based on thin chips that are glued onto thin printed circuit boards and interconnected e.g. with wire bonds or SpTAB bonding (see e.g. [13]). These assemblies are then held in flat position by external support mechanics or stiffeners.

In this paper, we propose, and demonstrate, a method to fully embed 50 µm-thin MAPS into polyimide flexible printed circuit boards. The resulting assembly does not only protect the silicon chip, but also provides the electrical interconnection. Furthermore, the assembly remains flexible and protects the chips from breakage when bending them. Excluding the copper layer, our prototype has a material budget of around 0.1 % X_0, only twice that of the chip alone. Future optimisations of the process can potentially lower this further if required. The fill-factor of the copper layer will be subject to optimisation and hence its relative contribution to the total material budget will be highly application-dependent.

The process is inspired by previous works [14,15], but differs in the choice of interconnection metallurgy and does not require a chip-level redistribution layer, simplifying the procedure and, importantly, making it compatible with industry-standard manufacturing techniques.

Our process can easily be extended to larger areas, integrating and interconnecting several chips. It can also be considered as a means of

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https://doi.org/10.1016/j.nima.2022.167673
Received 30 May 2022; Received in revised form 19 October 2022; Accepted 20 October 2022
Available online 27 October 2022

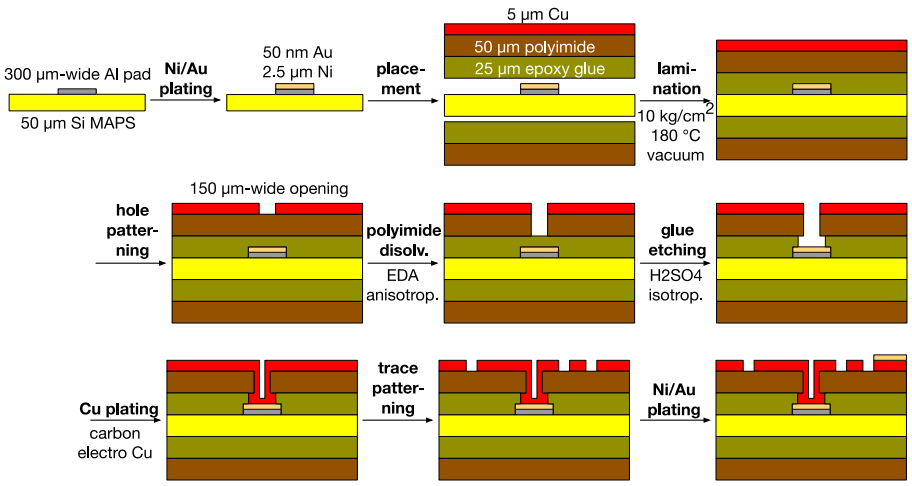

Fig. 1. The MAPS foil production process steps (from top left to bottom right).

adding a coarse routing layer to large, stitched chips, for instance for improved power distribution.

The resulting assembly is a flexible, highly integrated, thin, and yet robust vertexing layer, that can be scaled to large surfaces.

2. The MAPS foil concept

The basic idea of the MAPS foil is to embed MAPS sensors, either single or multiple ones, into flexible printed circuit boards. A sandwich of polyimide films, glue and sensor is made, and the copper traces are connected to the sensor by through-hole metallisation.

The assembly provides three main features at once:

- **Mechanical support:** the polyimide serves as a support structure to which precise mechanical alignment holes can be added; in addition, a number of chips can be placed next to each other to form a multi-chip module
- **Mechanical protection:** the polyimide protects the silicon; it can be manipulated by bare hands easily
- **Electrical interconnection:** the top polyimide film can be copper-clad and structured to form electrical traces, like in ordinary printed circuit boards; they can be interconnected to the chip pads, by opening holes and metallising them

The foil moreover remains flexible (as long as the sensor is[1]) and can be shaped into e.g. cylindrical shapes. It can indeed prevent early breakage by smoothing out the stress distribution over the silicon.

3. Process

The creation of the MAPS foil consists of two main stages: the embedding of the chip(s) between two polyimide films, and the electrical interconnection. The process, which is similar to the production of multi-layer printed circuit boards, is depicted in Fig. 1 and discussed hereafter. The mentioned material thicknesses are those used for the production of the first prototype and can be further optimised.

3.1. Chip preparation

The interconnection to the chip is based on metallisation, in a fashion similar to via plating in ordinary PCB manufacturing. For the metallurgy to work, the aluminium pads of the chip are first nickel–gold plated. A 2.5 µm-thick nickel layer is deposited with a 50 nm-thick gold finish.

3.2. Embedding

To tie the chip(s) to the polyimide, a thin glue layer is applied to the latter. The glue stems from an FR4 pre-preg[2] that is first applied to the polyimide film, and from which the fibres are removed afterwards. The polyimide–glue–chip–glue–polyimide sandwich is then compressed and heated to cure the glue.

3.3. Interconnection

For the interconnection, a copper-clad polyimide is used when embedding the chip. In the next steps a hole is opened over the pad positions, subsequently in the copper layer, the polyimide and the glue. This is done in a wet-chemical fashion, with different chemicals for the different layers.[3] The copper etching is done by applying a UV mask, and the subsequent steps are self-aligned, i.e. they use the layers above as masks. Since the chip can be seen from below (there is no copper cladding underneath the chip), the alignment of the first mask can be done quite accurately, certainly to the required level of the order of 50 µm, which is given by the attainable structure size and the dimensions of the chip pads. Once the hole is opened, copper electroplating is performed, creating the metal interconnection between the pad and the copper layer.

3.4. Trace patterning

The final steps consist in etching the traces on the copper (similar fashion as the hole opening in the copper), and the nickel–gold plating of contacts for interconnection of the foil to other devices.

4. Prototype

A first prototype was realised using ALPIDE sensors developed for the ITS2. ALPIDEs are 30 × 15 mm^2-large MAPS fabricated in the TowerJazz 180 nm CMOS Imaging Technology [17], that are readily thinned down to approximately 50 µm. They feature about 60 large, 300 µm-diameter, pads that are distributed over the chip surface for interconnection to detector modules,[4] making them suited for the process explained here (cf. Fig. 2).

[1] Despite the different layers of material, preliminary tests show that sensors can easily be bent to $R = 30$ mm (and very likely much further). More details will be subject of a future publication.

[2] Ditron PRG-EP-84

[3] The process builds largely on the experience that was gained with GEM foils [16].

[4] Within the ITS2, ALPIDEs are interconnected using wire-bonds through openings in a standard flexible printed circuit board that is placed over the chips, though different schemes were tried during the R&D phase, notably including laser soldering [2].

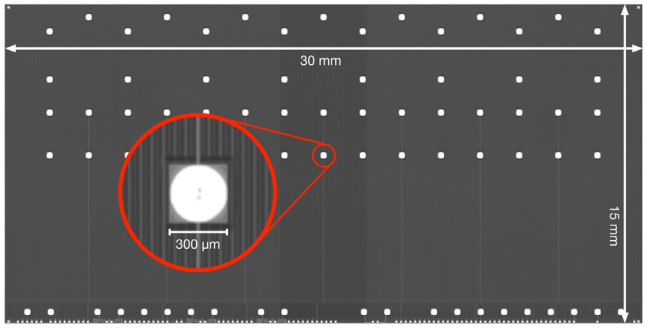

Fig. 2. Photograph of the ALPIDE chip, displaying the pattern of the large pads used for interconnection, zooming on one of them.

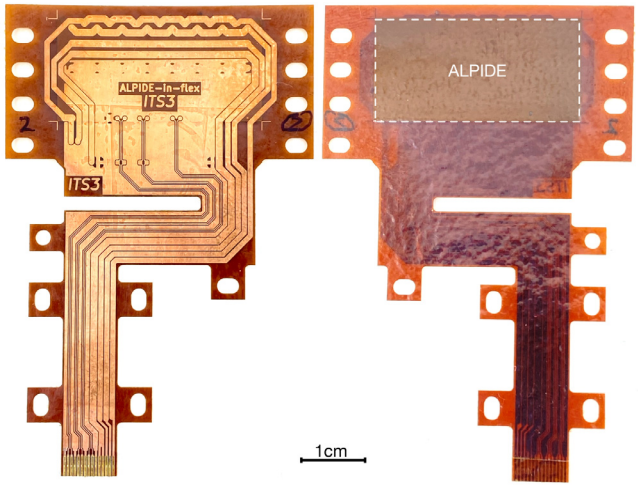

Fig. 3. Photographs (front and back) of the assembly. The ALPIDE is embedded at the top part (annotated on the right).

Fig. 3 shows what the prototype assembly looks like. It is a single-sided circuit board, that can be connected to existing readout hardware developed within the ALICE ITS MAPS R&D [18].

Five of these assemblies were fabricated and electrically tested for possible malfunctions of the sensors.[5] None was showing evidence for breaking the sensor, while two had a slight misalignment of the pads and holes, leading to non-working interconnections. This was spotted already during manufacturing, and we do not consider this a principle problem.

Fig. 4 shows the cross-section through one of the interconnections. The composition of the foil, the different characteristic geometries obtained from polyimide and glue openings, and the deposited copper plating that makes a solid contact are clearly visible. A material budget breakdown is given alongside, showing that the "extra" material accounts for roughly as much as the sensor itself. The copper layer is not included here, as its contribution will scale with the fill-factor of the traces as well as with the total thickness allowed for each specific application.

Three devices were successfully tested for functionality, including their response to an Sr-90 beta source, which created beta scattering images of the copper layers as shown in Fig. 5, nicely demonstrating the functioning of the assembly.

[5] The sensors were tested systematically beforehand by means of probe testing.

5. Discussion and relation to other methods

We would like to point out a few aspects that are key to our method, and make it distinct from other approaches:

- **Subtractive manufacturing:** The application of a solid glue layer and creation of the holes afterwards in a subtractive manner has an advantage over segmented gluing (e.g. by glue dispensing), since its initial application can be controlled more easily.
- **Symmetry:** The polyimide–chip–polyimide symmetry of the assembly reduces deformation after the gluing due to a mismatch of thermal expansion coefficients of chip, glue and polyimide.
- **Copper:** Using copper as metallisation material makes the method compatible with standard PCB/FPC manufacturing. An alternative approach using aluminium is however being investigated, since it allows to reduce the material budget. It would have the advantage of connecting aluminium pads to aluminium traces, but this requires custom equipment. There are, however, important difficulties when working with aluminium, which may motivate the use of copper. Aluminium is more fragile, tending to break more easily, effectively reducing the integration density. It also needs to be sputtered (not electroplated), which makes the creation of metallised holes much more difficult.
- **Interconnection method:** The interconnection by metallisation has a coarser feature size than, for instance, wire bonding. It has the advantage of a solid and robust interconnection, without the need of extra protection. In principle, wire bonds through larger openings could coexist if a higher connection density is needed.

6. Summary & outlook

We demonstrated a method to construct detector modules by embedding sensors in polyimide films. The resulting first "MAPS foils" have outstanding properties, potentially allowing the production of large detector systems in an industrial fashion.

This first successful trial also sparked a number of activities aiming at the construction of multi-chip modules, embedding of wafer-scale chips, as well as using chips produced in a 65 nm process, which is the target technology node for the ITS3. In addition, investigations of using a laser assisted process for the hole formation and using aluminium instead of copper are ongoing. Finally, the robustness, including the ageing of the assemblies, is being studied.

MAPS foils are a novel way to solve the module integration problem, bridging semiconductor sensors to macroscopic detector elements in an integrated fashion. They are protected, versatile, and flexible, yet only adding a minimal amount of material to the bare sensors. This is an appealing combination for many applications that require minimal material budgets.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

Acknowledgements

M. Mager feels indebted to the late W. Dulinski for his inspiring demonstration of a very similar prototype at the Front End Electronics Workshop at the Argonne National Laboratory in May 2014 [15].

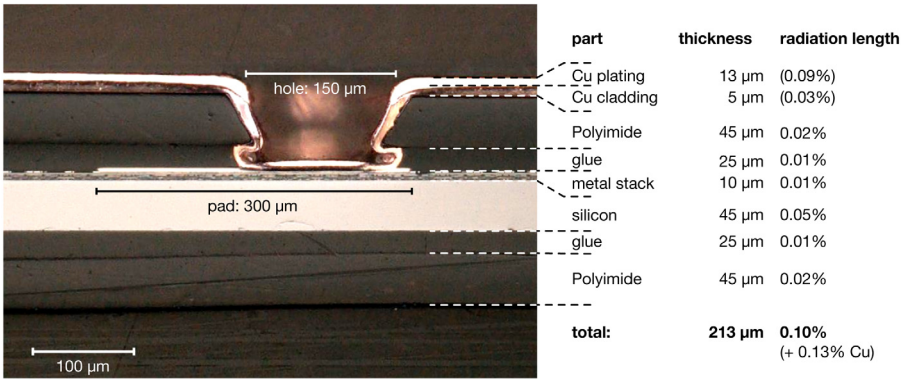

Fig. 4. Cross-section of one interconnection point and associated material budget breakdown. Radiation lengths from [19], and assuming a generic value of 35.5 cm for the epoxy glue.

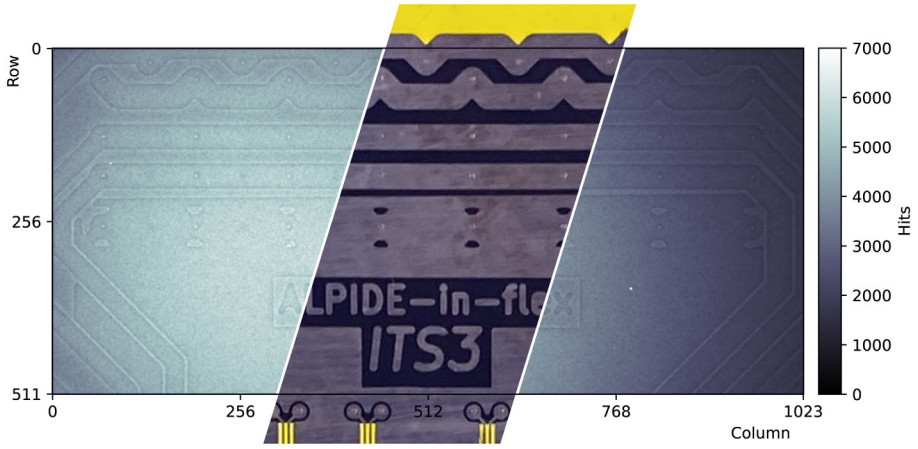

Fig. 5. Beta scattering image, self-portrait, of the assembly as acquired by the embedded chip, while being exposed to electrons from a Sr-90 source. The central part is overlaid with a photograph of the assembly to guide the eye. The drop of hit frequency towards the right and edges of the pixel array is due to the positioning of the source.

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