A Decentralized Power Allocation Strategy for Dynamically Forming Multiple Hybrid Energy Storage Systems Aided With Power Buffer

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Abstract—Multiple hybrid energy storage systems (HESSs) consisting of batteries and super-capacitors (SCs) are widely used in DC microgrids to compensate for the power mismatch. According to their specific energy and power characteristics, batteries and SCs are used to compensate low-frequency and high-frequency power mismatches, respectively. This paper proposes a decentralized power allocation strategy for dynamically forming multiple HESSs aided with a novel power buffer. The power buffer is a device combing a capacitor and a bidirectional DC-DC converter, it is used as an interface between the batteries and DC bus, allowing easy Plug-and-Play of different energy storage units and effective and efficient power allocation. First, the power buffer and SCs split the power mismatch into a low-frequency and high-frequency part with a modified I-V droop control. Then the power buffer transfers the low-frequency mismatch to the batteries for compensation based on their respective state-of-charges (SoCs), while the high-frequency part is dealt by the SCs directly. This new scheme further allows elimination of the DC bus voltage deviations. Finally, the real-time hardware-in-loop (HIL) tests of three case studies confirm the effectiveness of the proposed control strategy.

Index Terms—Power allocation, Multiple HESSs, Power buffer, I-V droop control, SoC balance, Plug-and-Play.

I. INTRODUCTION

WORLDWIDE commitments to reduce environmental pollutions and carbon emissions from burning fossil fuels have led to the rapid development of distributed energy resources (DERs) such as renewable energy sources (RESs) and hybrid energy storage systems (HESSs) [1]. The concept of the microgrid is identified as an effective way to integrate the RESs and the loads [2]. Microgrids can be divided into AC microgrids and DC microgrids, the latter is drawing increasing attention as many existing sources and loads are DC-based. Compared with its counterpart, DC microgrids have the following distinctive features, such as no requirement for frequency control, harmonics cancellation, and the absence of reactive power [3].

Considering the intermittent and stochastic nature of RESs and unpredictable variation of the loads, the HESSs are widely used in the microgrids to compensate power mismatch between RESs and loads. For any power mismatch profile, based on the Fourier analysis, it can be represented as the sum of trigonometric functions with different frequencies. The trigonometric functions with frequencies less and more than f (a preset value) are split into a low-frequency and a high-frequency part, respectively. Since the super-capacitors (SCs) have a faster response time than the batteries, low-frequency and high-frequency power mismatches are compensated by the batteries

and SCs, respectively [4]. Note that the threshold frequency f should be determined according to the response time of batteries and SCs, while the response time of batteries varies from millisecond to second, hence, different f is adopted in different literature. For example, this value was set to 5 Hz in [5] and while it was also set to 0.2 Hz in [6]–[8]. In practical application, a PV panel or wind turbine with a sudden change in solar irradiance or wind speed leads to a high-frequency power, while a load in stable operation mode absorbs low-frequency power from the microgrids.

To develop an adequate power-sharing scheme between different energy storage units in multiple HESSs is a challenge due to the existence of both high and low frequencies in the load power, and inappropriate power allocation leads to poor service life of batteries. Accordingly, various strategies have been proposed. These can be categorized into three different schemes: intelligent control, filter based and droop control based methods. The intelligent control methods include model predictive control (MPC), fuzzy logical control (FLC), and artificial neural network (ANN), etc. For example, Reference [9] proposed an explicit MPC system for single HESS. The separate explicit MPCs for the total output current loop, battery loop and SC loop are designed while the battery and SC current constraints, state-of-charge (SoC) constraints and SC voltage constraints are incorporated. Ni et al proposed a fast MPC based voltage control and power allocation optimization method for single HESS, the DC bus voltage can be regulated quickly by one-step prediction horizon and simplified switching states [10]. Zheng et al proposed a dual MPC strategy for single HESS consisting the superconducting magnetic energy storage (SMES) and battery to improve the electrical performance of naval DC microgrids supplying power pulsed loads [11]. Reference [12] used FLC controller to allocate power for single HESS under the transient power. In [13], an ANN based energy management strategy is designed and applied to single HESS using a multi-source inverter. The intelligent control methods usually achieve a better power allocation performance than the other two types, however, they operate in a centralized way, which introduces extra computational burden and may suffer from the single-point-failure issue.

In filter based methods, References [14] and [15] used a low-pass filter (LPF) to split the power mismatch into an average current component and a transient current component. While the former is tracked by a battery current controller, the latter is compensated by an SC. In [5], authors modified

this power allocation strategy by adding the uncompensated power from the battery to SC current control loop, the modified strategy achieves a faster DC bus voltage regulation and more effective power allocation. Tummuru et al [16] proposed an energy management strategy for renewable grid integrated systems with single HESS. The power mismatch is calculated by monitoring the DC bus voltage deviation from its reference level. Similar to References [14] and [15], the average power mismatch is tracked by a battery and the other is compensated by an SC. Kollimalla et al proposed a two-stage variable rate-limit control approach for the battery. The amount, rate, and time-duration of the energy absorbed/discharged from the battery are optimized [17]. A multi-filter based dynamic power-sharing control strategy is proposed in [18] for single HESS, which is integrated to a wave energy converter for output power smoothing. However, these filter-based methods have the same issue as the intelligent control methods, in that they are also centralized, and need a communication network to transfer the current reference to each energy storage units. Further, the system needs to be redesigned when a new energy storage unit is added to HESS.

Different from the aforementioned methods, the droop control based methods work in a decentralized way and achieve promising results in power allocation for HESS. These methods are either based on V-I droop control [6]–[8], [19], [20] or I-V droop control [21], [22]. In V-I droop control based methods [6]–[8], [19], [20], Xu et al proposed a decentralized control strategy for power allocation in single HESS, where the virtual resistance droop (VRD) controller and virtual capacitance droop (VCD) controller are applied to the battery and SC [6]–[8]. In [6], an SoC recovery loop is added to SC control, which helps automatic SoC recovery of SCs and enables their continuous operation. In [7], the influence of the line resistance on power allocation is discussed, and the design of the converter control loop is also conducted. In [8], the voltage droop caused by the droop coefficient is restored and the control strategy is extended to multiple HESSs. An integral droop is proposed for a cluster of energy storage units with high ramp rates [19], and the coordination of the integral droop and the conventional V-P droop helps the transient power allocation in single HESS in a decentralized manner. Zhang et al used a virtual impedance loop to add a virtual resistor and a virtual capacitor connected in series between the SC converter and the DC bus, which decouples the power flow between SC and the other DERs [20].

Similar to the V-I droop control, the I-V droop control is also a widely used control method in microgrid applications, where the DC bus voltage is used as the feedback signal and accurate current-sharing can be achieved. Some researches have been carried out using the I-V droop control [21]–[25]. For example, Gu et al proposed a mode-adaptive decentralized control for DC microgrids based on I-V droop control [23]. Gao et al proposed a comparative study of the V–I and I–V droop control approaches in the DC microgrids, focusing on steady-state power-sharing performance and stability [24]. In [25], a comparative study on the dynamic responses between the I-V droop and V-I droop control is presented, and the results show that the dynamic response performance of the I-V droop control is much faster than that of the V-I droop control. The authors in [21], [22] modified the I-V droop coefficients to achieve power allocation in single HESS. To implement the I-V droop control, the LPF is often introduced to suppress the high-frequency noise in the DC bus measurement, which introduces a DC bus voltage detection delay due to the phase shift effect of LPF. This effect has not been taken into consideration in selecting the I-V droop coefficients in the aforementioned previous researches. In this study, the I-V droop coefficients are determined considering the DC bus voltage detection delay, while the performance of DC bus, such as the overshooting, response time, and steady-state error, is taken into account simultaneously.

In summary, the power allocation between the battery and SC in single HESS is well-researched. In multiple HESSs, the power allocation patterns between batteries and SCs need to be achieved like that in single HESS. More importantly, the power allocation strategy should allow a Plug-and-Play feature of different energy storage units, and the power allocation among the batteries should be dynamically adjusted according to their SoC values, which can not be addressed with the aforementioned methods. To address the aforementioned issues, this paper proposes a decentralized power allocation strategy for dynamically forming multiple HESSs, while communication links between different energy storage devices are not required. Its key feature lies on the introduction of a novel power buffer which aids the power-sharing, not only between the batteries and SCs, but also among the same type of energy storage devices. The main contributions of this paper are summarized as follows.

1) The I-V droop coefficients are calculated considering DC bus voltage detection delay, where the performance of DC bus, like overshooting, response time, steady-state error, is taken into account simultaneously.

2) The power buffer and SCs split the power mismatch into a low-frequency and high-frequency part with the modified I-V droop control, the former is compensated by the batteries according to their respective SoCs, while the latter is dealt by SCs directly.

3) The power buffer is used as an interface between the batteries and DC bus, allowing easy Plug-and-Play of different energy storage units and effective and efficient power allocation.

To further demonstrate the merits of the proposed method, a comparison with existing decentralized power allocation techniques is presented. The existing decentralized power allocation techniques are either based on V-I droop control [6]–[8], [19], [20] or I-V droop control [21], [22], the fundamental idea of these methods is to modify the droop coefficients of one type energy storage (batteries/ SCs) with time-related components (integrators) to split low-frequency power and high-frequency power. In the V-I droop control based methods, the advantages and disadvantages of V-I droop control are inherited. Compared with the I-V droop control, the V-I droop control does not require DC bus voltage signal detection, however, the current-sharing accuracy is impacted by the line resistance, it will also cause DC bus voltage deviation due to the voltage drop on line resistance and droop coefficient. In I-V

droop control based methods, the accurate current-sharing between single HESS is achieved and DC bus voltage deviation is eliminated. In all aforementioned methods, the integrators are introduced when modifying the droop coefficients, the power allocation between the same type energy storage depends on the 'initial value' of the integrators, which hinders the Plug-and-Play feature and SoC balance when multiple HESSs are connected to the microgrids. This paper will show that with the introduction of the novel power buffer, accurate power allocation, DC bus voltage restoration, Plug-and-Play and SoC balance features are all achieved with the proposed method.

The remainder of this paper is organized as follows. Section II presents the I-V droop control for the DC microgrids, where the droop coefficients selection considering voltage regulation performance is discussed. In Section III, the I-V droop control is modified and applied to the battery and SC of single HESS. The proposed control strategy for multiple HESSs is presented in Section IV. The results of hardware-in-loop (HIL) tests and the practical implementation of the proposed control strategy are given in Section V. Finally, Section VI concludes the paper.

II. I-V DROOP CONTROL FOR DC MICROGRIDS

A. V-I Droop Control and I-V Droop Control

The configuration of a typical DC microgrid is illustrated in Fig.1, where the DC bus is modeled as a large capacitor [26], DERs controlled by the droop control are connected to the DC bus, while other DERs (such as RESs usually work at maximum power point tracking) and loads are also connected to the DC bus. I_{RES} and I_{load} are output current of RESs and absorbed current by loads, respectively. For simplification, these two currents are represented by an equivalent load current I_0, where $I_0 = I_{load} - I_{RES}$. If $I_{load} > I_{RES}$, I_0 is positive, otherwise I_0 is negative. R_{line} is the line resistance between the DER converter and DC bus.
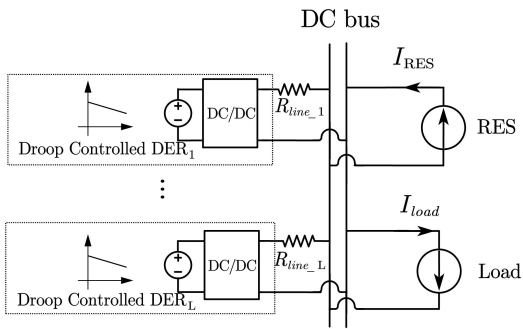

Fig. 1. Configuration of a typical DC microgrid

The V-I and I-V droop controls are two widely used droop control methods for DERs in the DC microgrids. In a V-I droop control, the DERs are controlled in voltage mode, and their expression is given by

$$V_i = V_{ref} - R_i I_i \tag{1}$$

where V_{ref} is the reference voltage of the DC bus, V_i and I_i are output voltage and current the i-th DER converter, respectively. R_i is the droop coefficient. The design of R_i has

been well-researched for the V-I droop control, in general, a higher R_i leads to a more accurate current-sharing but a larger voltage deviation, thus setting of the lower limit for R_i is usually based on the current-sharing requirement while its upper limit is based on the voltage deviation requirement [27].

In the I-V droop control, the converters are usually controlled in the current mode with expression given by Eq (2) and the control algorithm is illustrated in Fig.2

$$I_i = \frac{V_{ref} - V_{bus}}{R_i} \tag{2}$$

where v_{bus} is the measured DC bus voltage, V_{bus} is v_{bus} filtered by a LPF having a transfer function $1/(\tau s + 1)$, which is used to suppress the high frequency noise of v_{bus} signal. The LPF inevitably introduces v_{bus} signal detection delay, and the detection delay approximately equals to time constant τ. $\pm I_{limit\_i}$ and L_i are the output current limit and inductor for the i-th converter, respectively. The reference current is generated by the outer droop loop, and the inner current feedback control loop tracks this reference current and generates a reference voltage for a pulse width modulation (PWM) which is used to control the DC-DC buck-boost converter. It is worth
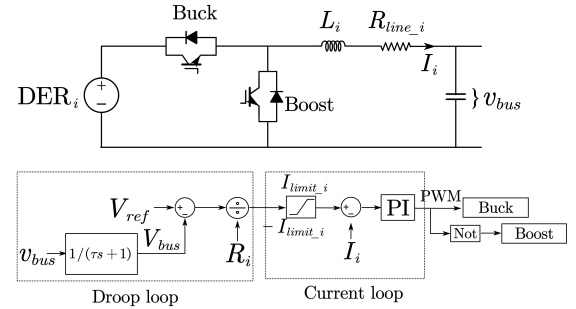

Fig. 2. The I-V droop control algorithm

noting that DER generates power when $I_i > 0$ and absorb power when $I_i < 0$. Assuming the current rating of i-th droop controlled DER is I_{rat_i}, to achieve current-sharing between droop controlled DERs, no matter in I-V droop control or V-I droop control, the droop coefficients should be calculated according to their current ratings [28], i.e.,

$$R_1 : \cdots R_i : \cdots R_L = 1/I_{rat\_1} : \cdots 1/I_{rat\_i} : \cdots : 1/I_{rat\_L} \tag{3}$$

Hence, for any two DERs i and j, their droop coefficients are inversely proportional to their current ratings, i.e.,

$$\frac{R_i}{R_j} = \frac{I_{rat\_j}}{I_{rat\_i}} \tag{4}$$

B. Performance of I-V Droop Control

With Fig.1 and Eq (2), the equation describing the variation of the DC bus voltage is given as

$$v_{bus} = \frac{1}{C_{bus}s} \left[\sum_{i=1}^{L} \left(V_{ref} - \frac{v_{bus}}{1 + \tau s} \right) / R_i - I_0 \right] \tag{5}$$

where C_{bus} is the capacitance of the DC bus. Eq (5) can be rewritten in the standard second-order transfer function with V_{ref} and I_o as input variables

$$v_{bus} = \frac{0.5w_n s/\xi + w_n{}^2}{s^2 + 2\xi w_n s + w_n{}^2} V_{ref} - \frac{0.5R_{eq}w_n s/\xi + R_{eq}w_n{}^2}{s^2 + 2\xi w_n s + w_n{}^2} I_0 \tag{6}$$

where $R_{eq} = 1/\sum_{i=1}^{L} \frac{1}{R_i}$ is the equivalent droop coefficient of L DERs, $w_n = \sqrt{\frac{1}{R_{eq}C_{bus}\tau}}$ is the natural frequency, $\xi = 0.5\sqrt{\frac{R_{eq}C_{bus}}{\tau}}$ is the damping ratio.

Assuming V_{ref} and I_o are set as constant values V_{ref}^* and I_o^*, respectively. Hence, their Laplace transform are V_{ref}^*/s and I_o^*/s, respectively. Applying the final value theorem [29] to Eq (6), the DC bus voltage at the steady-state is expressed as

$$v_{bus}^{ss} = \lim_{s \to 0} sv_{bus} = V_{ref}^* - I_o^* R_{eq} \tag{7}$$

Eq (7) reveals that the voltage deviation between v_{bus} and V_{ref} at the steady-state equals to $I_o^* R_{eq}$, it is evident that for a specific I_o^*, a smaller R_{eq} leads a smaller voltage deviation. Assuming the allowed maximum voltage deviation is δ, the feasible range for R_{eq} is given as

$$R_{eq} < \frac{\delta}{|I_o^*|} \tag{8}$$

Based on the Eq (6), the DC bus voltage dynamics with different R_{eq} and C_{bus} are illustrated in Fig.3, where τ and I_o^* are set 0.01 s and 50 A, respectively. It can be observed that a larger C_{bus} provides a larger DC bus inertia, and a smaller R_{eq} leads to a higher DC bus voltage overshooting because of the DC bus detection delay.
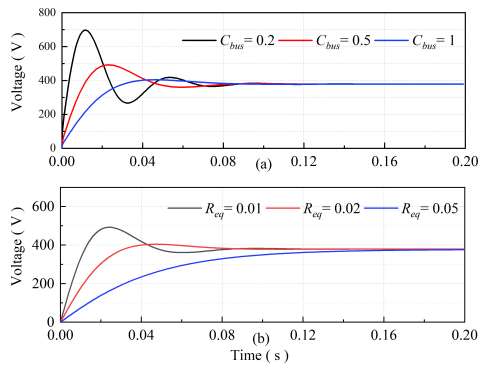

Fig. 3. The dynamic variations of v_{bus} with (a) different C_{bus} at $R_{eq} = 0.02$ (b) different R_{eq} at $C_{bus} = 1$

Apart from the DC bus voltage regulation with I-V droop control, the current-sharing accuracy is also analyzed. Combing Eq (2) and Eq (4), it yields

$$\frac{I_i}{I_j} = \frac{R_j}{R_i} = \frac{I_{rat\_i}}{I_{rat\_j}} \tag{9}$$

Eq (9) reveals that the I-V droop control ensures accurate current-sharing.

In summary, unlike V-I droop control, which has a trade-off between current-sharing and voltage regulation, accurate

current-sharing is achieved with the I-V droop control. Hence, only the DC bus voltage regulation requirement need to be considered in R_{eq} selection. A smaller R_{eq} leads to a smaller steady-state DC bus voltage deviation and a larger voltage overshoot, while a larger C_{bus} provides DC bus a larger inertia and a slower response time. The upper limit of R_{eq} should be calculated based on the steady-state voltage deviation requirement with Eq (8), while C_{bus} the lower limit of R_{eq} and should be determined by DC bus voltage overshoot and response time requirements with Eq (6). Then, according to Eq (4), the droop coefficient of each DER is designed.

III. MODIFIED I-V DROOP CONTROL FOR SINGLE HESS

The I-V droop control uses the DC bus voltage as the feedback signal and achieves accurate current-sharing between parallel DERs irrespective of the line resistance. With this benefit, it is possible to design the I-V droop controller by using different droop coefficients for the battery and SC in single HESS. Considering the life cycle and output characteristics of the battery and SC, the former is usually used to compensate the low-frequency power fluctuation while the latter is for the high-frequency power variations.

To facilitate fast response of SC when power mismatch occurs and causes the DC bus voltage deviation from its reference value, its control law is expressed as

$$I_{SC} = \frac{V_{ref} - V_{bus}}{R_{SC}} \tag{10}$$

where I_{SC} and R_{SC} are, respectively, SC converter output current and droop coefficient.

While in order to let the battery respond slowly when power mismatch occurs which leads the DC bus voltage drifts, the control law for the battery is given as

$$I_b = \frac{V_{ref} - V_{bus}}{R_b} \frac{1}{s} \tag{11}$$

where I_b and R_b are the battery converter output current and droop coefficient, respectively. An integrator is added to the battery droop controller, and the battery converter output current gradually increases from 0, thus, the battery can compensate the low-frequency power fluctuation.

Assuming one battery and one SC are two droop controlled DERs in the DC microgrid in Fig.1, according to Kirchhoff's Current Law (KCL)

$$I_b + I_{SC} = I_0 \tag{12a}$$

$$I_{SC} = F_1(s) \cdot I_0 = \frac{sR_b/R_{SC}}{sR_b/R_{SC} + 1} I_0 \tag{12b}$$

$$I_b = F_2(s) \cdot I_0 = \frac{1}{sR_b/R_{SC} + 1} I_0 \tag{12c}$$

$F_1(s)$ and $F_2(s)$ work as a high-pass filter (HPF) and a LPF with the cutoff frequency $w_c = R_{SC}/R_b$, respectively. It will have impacts on the response speed of SC and the battery. Based on Eq (12), the output current dynamics of the battery and SC with the step response are illustrated in Fig.4, where R_b is set equal to R_{SC}. It is shown that I_{SC} increases immediately due to the voltage difference between V_{ref} and

V_{bus}, and it reduces to zero when the battery helps the DC bus voltage restore to its reference voltage. On the contrary, I_b gradually increases to I_0 at that time. It is also worth noting that the combination of SC and the battery controller works as a PI controller, thus, the voltage deviation is eliminated at steady-state.
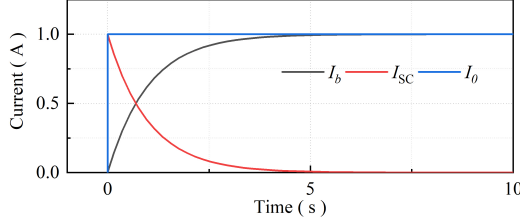

Fig. 4. Output current dynamics of the battery and SC

IV. POWER BUFFER STRATEGY FOR MULTIPLE HESSS

Considering dynamically forming multiple HESSs with M batteries and N SCs used in the DC microgrid, the following two control objectives need to be achieved. Firstly, the power allocation patterns between the batteries and SCs should be maintained as described in the Section III. Secondly, the power allocation among the batteries should be based on their respective SoCs considering the benefit of extending their life cycles. Thirdly, the Plug-and-Play of energy storage units should be maintained in the dynamically forming multiple HESSs.

A. The Principle of Power Buffer

In single HESS, an integrator is introduced in the battery control, the voltage deviation between DC bus and reference voltage will be eliminated when $I_b = I_0$, and the power allocation is then completed, i.e., I_b is kept unchanged unless I_0 varies. If a new battery is connected to the DC bus directly to form a multiple HESSs, taking the new battery connection time as the 'initial time', the integrator in the control law of previous battery will have a different 'initial value' with the integrator for newly connected battery, then the two batteries will supply different output currents and the power-sharing can not be achieved. More importantly, the power allocation among the dynamically forming batteries is supposed to be dynamically adjusted according to their SoCs rather than being kept unchanged. In summary, the control strategy for the single HESS can not be extended to dynamically forming multiple HESSs.

To achieve the aforementioned control objectives, as illustrated in Fig.5 (a), instead of directly connecting batteries to the DC bus, a power buffer consisting of a large capacitor with a bidirectional DC-DC converter is used to interface between them. So that all batteries and their corresponding buck-boost bidirectional converters are connected to the DC bus via the power buffer. All SCs and their associated bidirectional converters are directly shunt connected to the DC bus. The control law for power buffer is expressed by

$$I_{\mathrm{PB}} = \frac{V_{ref} - V_{bus}}{R_{\mathrm{PB}}} \frac{1}{s} \qquad (13)$$

where I_{PB} and R_{PB} are, respectively, converter output current and droop coefficient of power buffer.

In this way, power buffer plays a similar role that the battery plays in single HESS. It provides the low-frequency power compensation while SCs compensate the high-frequency power change. The control strategy for N SCs in multiple HESSs is the same with that in single HESS, which will be demonstrated in the following. Also, the way power buffer helps the power allocation among the batteries will be demonstrated in the next Subsection.

B. Control Law for Batteries

The control law for the batteries in multiple HESSs is expressed as

$$I_{bi} = \frac{V_{\mathrm{PB\_ref}} - V_{\mathrm{PB}}}{R_{bi}} \qquad (14)$$

where I_{bi} and R_{bi} are the i-th battery converter output current and droop coefficient, respectively, $V_{\mathrm{PB}} = v_{\mathrm{PB}}/(1 + \tau s)$ where v_{PB} is the measured voltage of power buffer capacitor, $V_{\mathrm{PB\_ref}}$ is the reference voltage of power buffer capacitor. R_{bi} is designed as

$$R_{bi} = \begin{cases} k_{ci}\mathrm{SoC}_{bi}^n & \text{if } I_{bi} \leq 0 \\ k_{di}/\mathrm{SoC}_{bi}^n & \text{if } I_{bi} > 0 \end{cases} \qquad (15)$$

where n is the index for SoC balance, SoC_{bi} is SoC of i-th battery, its safety operation range in the microgrids is usually set 0.2 to 0.8 [30]. k_{ci} and k_{di} are the charging and discharging coefficients of the i-th battery, respectively. $I_{bi} \leq 0$ denotes the battery is charging and $I_{bi} > 0$ denotes the battery is discharging. The ratio between the i-th and j-th coefficients is given according to

$$\frac{k_{ci}}{k_{cj}} = \frac{k_{di}}{k_{dj}} = \frac{C_{bj}}{C_{bi}} \qquad (16)$$

where C_{bi} and C_{bj} are the capacities of i-th and j-th battery, respectively. And for M batteries their equivalent battery droop coefficient is $R_{b\_eq} = 1/\sum_{i=1}^{\mathrm{M}} \frac{1}{R_{bi}}$.

The DC microgrid draws the low-frequency power from the capacitor in power buffer, which makes v_{PB} deviate to its reference voltage. According to Eq (14), the voltage deviation drives the batteries to supply power to the DC microgrids through power buffer. The battery control law can be considered as a proportional control, the batteries with lower SoCs are assigned with a smaller R_b (large proportional gain) in the charging process to enable them to absorb more power. On the contrary, they are assigned with a greater R_b in the discharging process to help them supply less power. Thus, the power allocation among the batteries are based on their respective SoCs and SoCs of multiple batteries can gradually balance. A detailed discussion on SoC balance process was given in our previous publication [31]. Also, according to our previous study, a greater n leads to a faster SoC balance speed, and a satisfactory SoC balance speed and R_b variation range have been achieved when $n = 2$, thus this value is adopted in the study.
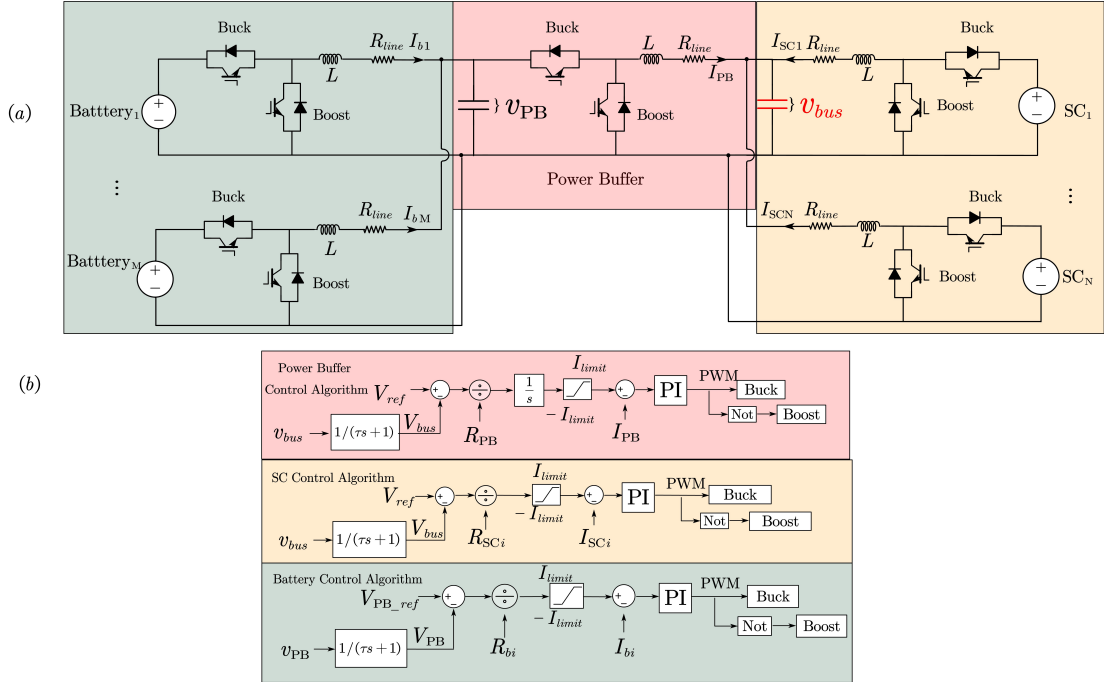
Fig. 5. The proposed control strategy for multiple HESSs (a) Multiple HESSs configuration (b) Block diagram of the control algorithm

C. Control Law for Super-capacitors

In multiple HESSs, as illustrated in Fig.5 (a), SCs are connected to the DC bus directly through the bidirectional buck-boost converters. Their control laws are the same as that when there is only one SC in single HESS and are expressed by Eq (10), the ratio of any two SCs' droop coefficients is inversely proportional to their capacities and given as

$$\frac{R_{\mathrm{SC}i}}{R_{\mathrm{SC}j}} = \frac{C_{\mathrm{SC}j}}{C_{\mathrm{SC}i}} \qquad (17)$$

where $C_{\mathrm{SC}i}$ and $C_{\mathrm{SC}j}$ are, respectively, the i-th and j-th SC capacities, and for N SCs their equivalent SC droop coefficient is $R_{\mathrm{SC\_eq}} = 1/\sum_{i=1}^{N} \frac{1}{R_{\mathrm{SC}i}}$.

As SCs supply power until the DC bus voltage is restored to its reference value, the voltage deviation between V_{bus} and V_{ref} helps power allocation among SCs according to their respective capacities.

In summary, the low-frequency power mismatch at DC bus is supported by the batteries through power buffer. The benefits of connecting the batteries to a power buffer instead of directly connecting to the DC bus are twofolds. Firstly, it facilitates the Plug-and-Play feature of different energy storage units and realization of the power control scheme, namely, the batteries are used to address the low-frequency power fluctuations at the DC buses while SCs for the high-frequency part. Secondly, with the introduction of power buffer and R_b design, the power allocation among the batteries is dynamically adjusted according to their SoCs. Similar to single HESS, the power-sharing speed between multiple HESSs is impacted by w_c', $w_c' = R_{\mathrm{SC\_eq}}/R_{\mathrm{PB}}$.

D. Parameters Design of the Proposed Control Strategy

The design of R_{b_eq} can be referred to the Section II. As the integrator is used in power buffer control law, which works together with SCs to support DC bus, the controller parameters design of SC and power buffer is different from Section II, the details are given below.

The detailed control algorithms for each energy storage units are summarized in Fig.5 (b), they are all controlled by the outer droop loop and the inner current loop. Let L, R_{line} and I_{limit} denote the inductance, the line resistance, and the output current limit of all converters, respectively. It is worth noting that the inner loop is usually designed much faster than the outer loop. Thus, the response speed of the inner current loop can be simplified as '1', and SCs and power buffer converters can be integrated as an equivalent converter, the control block diagram of this equivalent converter is shown in Fig.6. It can be observed that the combination of SCs and power buffer droop control works as a PI controller, and the outer loop can be considered as a voltage loop for reference voltage tracking, the voltage close loop transfer function is expressed by

$$v_{bus} = T_{rans\_CL}(s) \cdot V_{ref} \qquad (18)$$

where $T_{rans\_CL}(s) = \frac{\tau/R_{\mathrm{SC\_eq}}s^2 + (1/R_{\mathrm{SC\_eq}} + \tau/R_{\mathrm{PB}})s + 1/R_{\mathrm{PB}}}{\tau C_{bus}s^3 + C_{bus}s^2 + s/R_{\mathrm{SC\_eq}} + 1/R_{\mathrm{PB}}}$

Generally speaking, w_c' is preset according to the desired power allocation dynamics between the batteries and SCs. Based on Eq (18), Fig.7 and Fig.8 illustrate the bode plot for the voltage close loop at different $R_{\mathrm{SC\_eq}}$ with $w_c' = 0.4$ and $w_c' = 2$, respectively. A smaller $R_{\mathrm{SC\_eq}}$ leads to a higher voltage loop bandwidth, and a higher voltage loop bandwidth leads to a faster voltage response speed.
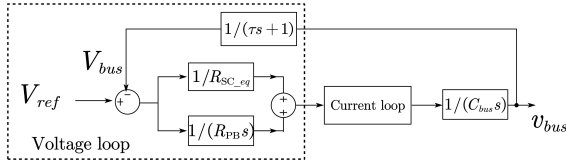
Fig. 6. Control block diagram for the equivalent converter

Note that current loop bandwidth is usually designed at 1/10 of the switching frequency, and the outer voltage loop bandwidth is selected at less than 1/10 of the current loop [32]. Considering that the switching frequency of converters is 10 KHz in this paper, the upper limit of voltage loop bandwidth can be calculated as 628 rad/s. It is shown that the bandwidths with $R_{\mathrm{SC\_eq}} = 0.02$ in the two figures are both less than 100 rad/s. $R_{\mathrm{SC\_eq}}$ is set to 0.02 in the following tests, which leads to a satisfactory DC bus response speed and keeps sufficient bandwidth margin. Then R_{PB} is changed to different values to investigate the power allocation speed between the batteries and SCs. With given $R_{\mathrm{SC\_eq}}$, $R_{\mathrm{SC}i}$ are calculated based on Eq (17).
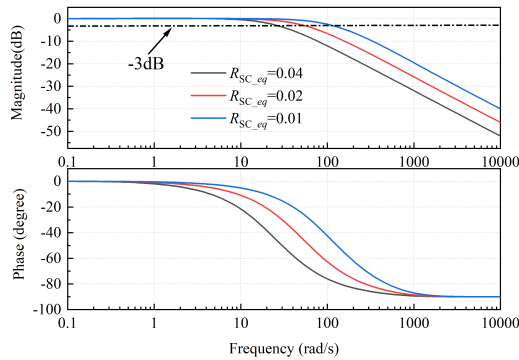
Fig. 7. Bode plot for voltage close loop at different $R_{\mathrm{SC\_eq}}$ with $w_c' = 0.4$
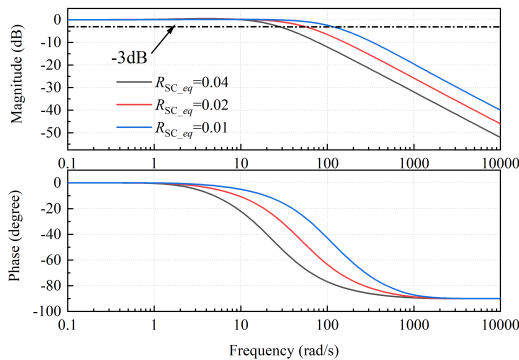
Fig. 8. Bode plot for the voltage close loop at different $R_{\mathrm{SC\_eq}}$ with $w_c' = 2$

V. HARDWARE-IN-LOOP TEST RESULTS AND DISCUSSIONS

To validate the proposed control strategy, the hardware-in-loop (HIL) real-time tests are conducted at the Typhoon HIL-604 platform. This ultra-high fidelity HIL device consists of 8-core processors able for real-time emulation of up to 8 converters, and can test the controller with 20 ns PWM resolution. It can also emulate power stage with up to 2 MHz update rate. This device can interface to external hardware controllers via its 64 analog outputs, 32 analog inputs, 64 digital inputs, and 64 digital outputs. As illustrated in Fig.9, the whole system (converters, HESSs, etc) is emulated by typhoon HIL-604, while the controller for the real-time emulated system is implemented using a Texas Instruments TI LaunchPad (LAUNCHXL-F28069M), which is interfaced with the typhoon HIL device through a Launchpad interface. The controller communicates the emulated system through 16-ADC channels, then sends PWM signals back to typhoon HIL device.

Three cases with 2 batteries and 2 SCs multiple HESSs are used to validate the proposed control strategy. The parameters for the system and controller used in this study are listed in Table I, where the proportional and integral terms of the current loop of all converters are the same and represented as k_p and k_i, respectively. I_0 is changed with time in the three cases to simulate different operation conditions of multiple HESSs.

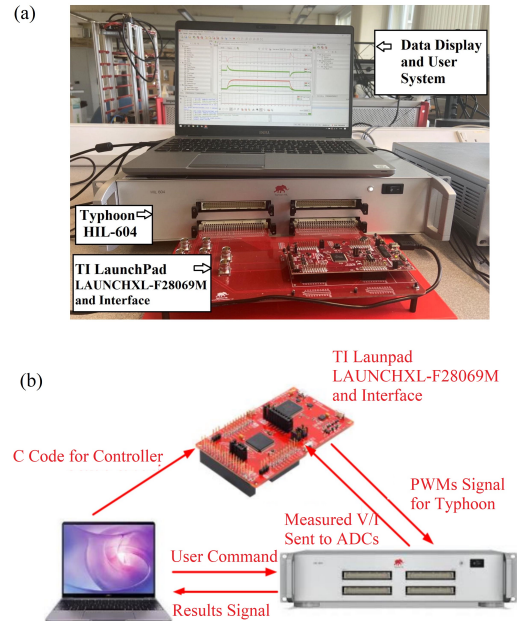Fig. 9. HIL tests (a) Experimental set-up (b) Device operation details

A. Voltage Regulation and Power Allocation in Multiple HESSs

In this case, the voltage regulation and power allocation using the proposed control strategy in multiple HESSs are validated. As illustrated in Fig.10, I_0 is set 0 A from 0 s to 5 s, v_{bus} and v_{PB} are regulated at their reference voltage,

TABLE I
SYSTEM AND CONTROL PARAMETERS USED IN HIL TESTS

Parameters	Value	Parameters	Value
R_{PB}	0.02	$R_{\mathrm{SC}i}, (i = 1, 2)$	0.04
$k_{ci}, (i = 1, 2)$	0.1	$k_{di}, (i = 1, 2)$	0.033
τ	0.01 s	n	2
L	0.1 H	R_{line}	0.001 Ω
V_{ref}	600 V	$V_{\mathrm{PB\_ref}}$	800 V
C_b	50 Ah	I_{limit}	200 A
k_p	50	k_i	30
C_{bus}	1 F	C_{PB}	0.1 F

600 V and 800 V, respectively. At 5 s, both power buffer and SCs are discharged to support the DC bus. I_{SC1} and I_{SC2} increase immediately to compensate the high-frequency power mismatch, then gradually decreases to 0. On the contrary, I_{PB} gradually increases from 0. At 15 s, both the batteries and SCs are charged. It is evident that SCs change immediately to compensate power surplus at high-frequency, and batteries compensate the low-frequency power mismatches. And $I_{\mathrm{SC1}} = I_{\mathrm{SC2}}$ and $I_{b1} = I_{b2}$, which confirms that the power allocation among the same type energy storage units is achieved.

Fig.10 shows that v_{bus} suffers from a voltage surge after I_0 perturbation, then it is restored to its reference value, since the combination of power buffer and SCs controllers work as a PI controller. While the sudden voltage fluctuation does not occur on power buffer, because power demand from power buffer gradually increases from 0. v_{PB} gradually increases/decreases to a stable value (not equal to 800 V) when $I_{\mathrm{PB}} = I_0$, the voltage deviation helps power allocation among the batteries.
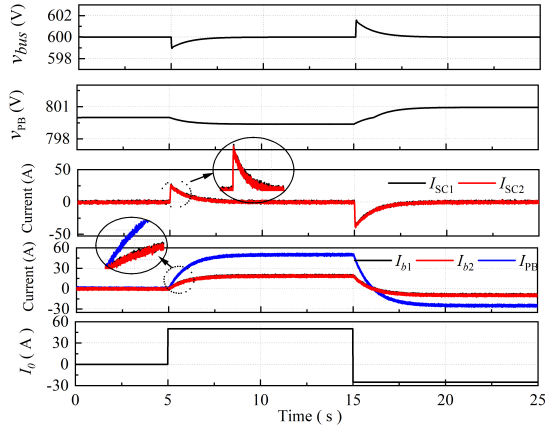

Fig. 10. Voltage regulation and power allocation in multiple HESSs

B. Power Allocation Dynamics with Different $w_c^{'}$

In this case, the power allocation dynamics between power buffer and SCs with different $w_c^{'}$ is validated. As listed in Table II, $R_{\mathrm{SC\_eq}}$ is fixed at 0.02, R_{PB} is set at different values to research different power allocation dynamics, other parameters are kept unchanged with Table I. The power allocation dynamics with $w_c^{'} = 0.4$, $w_c^{'} = 1$, $w_c^{'} = 2$ are illustrated in Fig.11 (a), (b), (c), respectively. Fig.11 shows that power buffer compensates the low-frequency power mismatch

and SCs compensate the high-frequency power mismatch no matter in the charging and discharging process when power mismatch occurs. A greater $w_c^{'}$ leads to a faster power allocation speed, i.e., a faster I_{PB} increase speed and a faster SC converter output current decrease speed. Hence, $w_c^{'}$ should be set according to the output characteristics and life cycle of the batteries and SCs.

TABLE II
PARAMETERS FOR DIFFERENT POWER ALLOCATION DYNAMICS

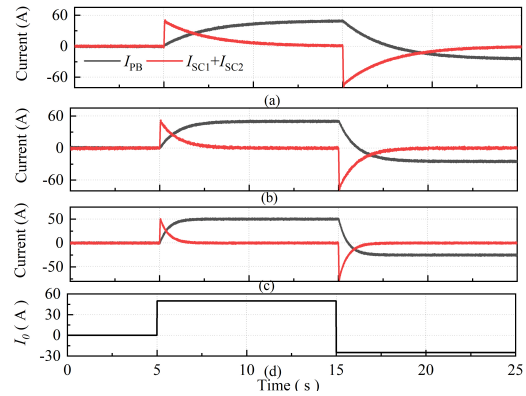| Parameters	Value	Parameters	Value	Parameters	Value
$w_c^{'}$	0.4	$R_{\mathrm{SC\_eq}}$	0.02	R_{PB}	0.05
$w_c^{'}$	1	$R_{\mathrm{SC\_eq}}$	0.02	R_{PB}	0.02
w_c	2	$R_{\mathrm{SC\_eq}}$	0.02	R_{PB}	0.01

Fig. 11. Power allocation between power buffer and SCs with different $w_c^{'}$ (a) $w_c^{'} = 0.4$ (b) $w_c^{'} = 1$ (c) $w_c^{'} = 2$ (d) I_0

C. Comparison with No Power Buffer

The comparison with no power buffer control strategy is conducted in this case, where the batteries are connected to DC bus directly, and its control algorithm is same with the battery in single HESS. The comparison is conducted in two different scenarios. The first scenario is to study the performance of two control strategies with different battery connection time, the second scenario is to study the performance of two control strategies with different battery SoC values.

Scenario C1: Performance with different battery connection times

The performance of two control strategies with different battery connection times is illustrated in Fig.12 to investigate the control performance for dynamically forming batteries. From 0 s to 10 s, only $\mathrm{Battery}_1$ is connected and $\mathrm{Battery}_2$ is activated at 10 s, I_0 perturbs at 5 s and 15 s. As shown in Fig.12 (a) and (b), with the proposed control strategy, $\mathrm{Battery}_1$ and SCs support the equivalent load before $\mathrm{Battery}_2$ is activated, and the $\mathrm{Battery}_2$ equally shared equivalent load immediately when it is activated. After I_0 perturbation, the proposed control strategy still achieves proper power-sharing between different energy storage units. The battery converter output current with no power buffer control strategy is shown in Fig.12 (c), like the proposed control strategy, $\mathrm{Battery}_1$

supports the equivalent load before Battery_2 is activated, but when Battery_2 is activated, the power-sharing among batteries can not be achieved. As explained in the Section IV, the 'initial value' of their respective integrators is different. It can be concluded that the proposed control strategy has a Plug-and-Play feature, however, the integrators need to be reset to same value when a new battery is connected with no power buffer control strategy.
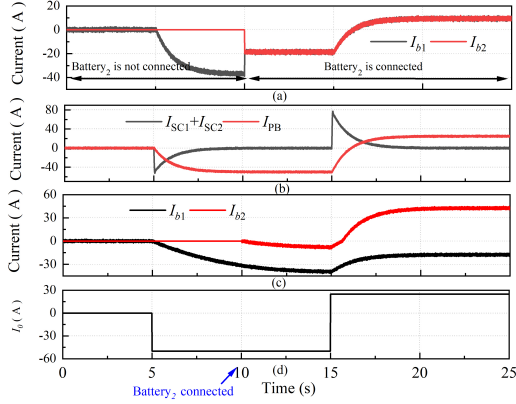

Fig. 12. Performance with different battery connection time (a) I_{bi} with the proposed control strategy (b) I_{SC} and I_{PB} with the proposed control strategy (c) I_{bi} with no power buffer control strategy (d)I_0
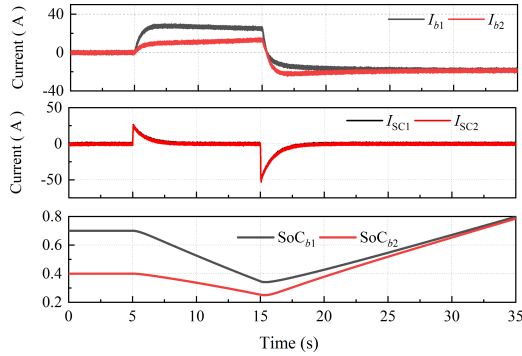

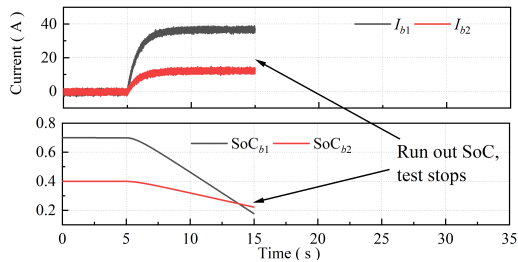Fig. 13. Performance with the proposed control strategy in Scenario C2

Fig. 14. Performance with no power buffer control strategy in Scenario C2

Scenario C2: Performance with different battery SoC initial values

The battery SoC balance using the proposed control strategy is validated and illustrated in Fig.13. To demonstrate the SoC

balancing, the initial SoCs of Battery_1 and Battery_2 are, respectively, set to 0.7 and 0.4. The capacities of two batteries are scaled down from 50 Ah to 0.2 Ah to fully demonstrate the battery SoC balancing dynamics. Other parameters used in this case are kept unchanged as shown in Table I. As illustrated in Fig.13, I_0 increases to 50 A at 5 s, to achieve SoC balance, the battery with higher SoC (Battery_1) supplies more current compared to that having lower SoC (Battery_2). I_0 decreases to -50 A at 15 s, Battery_1 is charged with a smaller current compared with Battery_2. The high-frequency power is equally allocated to SC_1 and SC_2. Further, it can be observed that the difference between I_{b1} and I_{b2} decreases as the SoC difference decreases, and the difference will be eliminated when SoC balance are achieved. In summary, the batteries respond to the low-frequency power based on their SoCs, the SoC difference between two batteries decreases no matter they are in the charging/discharging mode, finally achieving SoC balance.

The performance of battery SoC balance using the no power buffer control strategy is validated in Fig.14, the Battery_1 with higher initial SoC value are assigned with a small droop coefficient and supply more power compared the Battery_2 with lower SoC battery. However, after power allocation is completed, the battery converter output currents are kept unchanged, it can not be dynamically adjusted according to SoC value, which causes Battery_1 keeping supply more power even its SoC is already lower than Battery_2. Hence, the SoC balance can not be achieved. At 15 s, the SoC of Battery_1 is smaller than the low limit (0.2), the test stops.

D. Discussion on Practical Implementation

In the practical implementation of the control scheme with the power buffer, the following procedures should be followed.

1. Connect the batteries to the power buffer capacitor and regulate the capacitor voltage to the preset value.

2. Connect power buffer to DC bus and regulate DC bus voltage to the preset value.

3. Connect the SCs to the DC bus.

4. Plug in/plug out batteries/SCs.

Further, a few other requirements should also be noted.

At least one battery and one SC should be connected to maintain the power allocation and voltage regulation in the microgrids.

The low-frequency power demanded from the equivalent load is compensated by the batteries through the power buffer converter. Hence, the power rating of power buffer converter should be at least 120% of the maximum low-frequency power demanded from the equivalent load to ensure the safe operation of the converter.

The power burden on battery converters increases with the decrease of battery connection numbers. The battery converter bears the heaviest burden when only one battery is connected, therefore its power rating should satisfy the demand in this situation.

VI. CONCLUSIONS

This paper has proposed a decentralized power allocation strategy for dynamically forming multiple HESSs aided with

a novel power buffer. The power buffer is a device combing a capacitor and a bidirectional DC-DC converter, it is used as an interface between the batteries and DC bus, allowing easy Plug-and-Play of different energy storage units and effective and efficient power allocation. First, the power buffer and SCs split the power mismatch into a low-frequency and high-frequency part with the modified I-V droop control. Then the power buffer transfers the low-frequency mismatch to the batteries for compensation based on their respective SoCs, while the high-frequency part is dealt by the SCs directly. This new scheme further allows elimination of the DC bus voltage deviations. Finally, the real-time HIL tests with three case studies confirm the effectiveness of the proposed control strategy.

The test results show that the low-frequency power mismatch can be compensated by the batteries according to their respective SoCs, while SCs compensate the high-frequency power mismatch with the aid of power buffer. The dynamics of power-sharing are determined by w_c', a greater w_c' leads a faster power-sharing speed and vice versa. The proposed control strategy allows Plug-and-Play of different energy storage units and eliminates DC bus voltage deviation.

In the future, the following directions will be researched. First, the power buffer can be introduced for the SCs, and the power buffers for both batteries and SCs can work together effectively using more advanced control methods, like fuzzy logic control, model predictive control, artificial neural network to achieve better power allocation and DC bus regulation performance. Second, w_c' can be adjusted by changing R_{PB} according to various battery conditions to further improve battery service life while meeting the control performance of the DC microgrids.

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