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NATIONAL TECHNICAL UNIVERSITY OF UKRAINE
“IGOR SIKORSKY KYIV POLYTECHNIC INSTITUTE”

ELECTRONIC SYSTEMS-1 LABORATORY GUIDE

Tutorial

Recommended by Methodical council of “Igor Sikorsky Kyiv Polytechnic Institute”
as a tutorial for bachelors
according to the educational program “Electronic components and systems”
specialty 171 Electronics

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The discipline «Electronic Systems» belongs to the cycle of professional and practical training of bachelors in the educational program «Electronic Components and Systems» is read over one semester (7) and is one of the final subjects of the bachelor's degree. In the process of studying the course, students get acquainted with the informational assessments of the ES; a description of the signals used in different purposes of the ES; methods of their processing, storage and transformation; principles of construction and operation of the ES - the selection, transformation, transmission, reception, registration and display of information. Methodical instructions contain information on 5 laboratory works. For each of the works, the topic, purpose, description of the scheme, the program of work and a list of recommended reading are given sequentially.

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INTRODUCTION

The purpose of studying the discipline "Electronic Systems" is to provide students with thorough knowledge of information evaluation of electronic systems (EC), signaling, as well as methods of their transformation and storage, principles of construction and operation of EC selection, conversion, transmission, reception, registration and display of information.

According to the requirements of the curriculum, students after mastering the discipline must demonstrate the following results of learning:

- in the theory of information, processing and conversion of signals in the time and frequency domains using the EC, the principles of construction of information EC for various purposes;

- to carry out information assessment of EC selection, transformation, transmission, reception, registration and display of information, in accordance with the requirements of the technical task to determine the functional composition of the EC of the required level of noise immunity and reliability of functioning;

- general concepts of object-oriented approach to apply the acquired knowledge in the learning process, in the course and final work, in practice and research in the specialty.

This is achieved due to the wide application in the educational process of computer technology and modern software, increasing the cognitive and creative activity of students.

Methodical instructions contain information on 5 laboratory works. For each of the works, the topic, purpose, description of the scheme, the program of work and a list of recommended reading are given sequentially.

The main tasks of laboratory work are:

- formation and development of a comprehensive perception of the electronic system as a functional unit;

- improving the skills of reading electrical schematics, understanding the principles of construction and interaction of individual components of the electronic system;

- development of practical skills of work with hardware of measurement and control;

- improving teamwork skills;

- formation of skills of analysis and critical evaluation of experimental practical material.

The subject of laboratory works is determined by the program of the corresponding discipline. The series of works for the course "Electronic Systems" is based on the principle of gradual increasing complexity of the object of study, and consists of five laboratory works with the following topics:

Lab №1	Analysis of binary counters
Lab №2	Combination devices with logical elements
Lab №3	Synthesis of combinational devices based on multiplexers
Lab №4	Universal code converter
Lab №5	Analog-to-digital converter for double integration

Requirements for the content, scope and design of protocols of laboratory work, as well as criteria for assessing the quality of work and its protection are regulated by the rating system for the course "Electronic systems, below.

Rating points system and evaluation criteria:

- full implementation, defence with an assessment of "excellent".....5 points
- full implementation, defence with a grade of "good"4 points
- incomplete implementation of work, defence with an assessment of "satisfactory".....3 points
- incomplete implementation of work, defence with an assessment of "unsatisfactorily".....2 points
- the work is not done0 points

Since the condition for admission to the exam from the course is to perform a full cycle of laboratory work, the non-performance of laboratory work by the student in the presence of a valid reason must be eliminated. The working time in this case

is set by the teacher in agreement with the engineer (laboratory assistant) of the computer class.

An important part of the work is the independent preparation of the student to answer questions in defense. One of the components of quality defence is the study of theoretical material on the subject of each individual laboratory work. The student selects the literature independently, taking into account the recommended sources.

The laboratory report, as a rule, should contain such structural elements:

1. Title page;
2. The purpose of the work and the tasks to be performed;
3. Schematic electrical circuit, which is modeled;
4. Tables with measurement results (unless otherwise specified by the task);
5. Graphical interpretation of tables and / or oscillograms at control points of the scheme;
6. Conclusions on the work.

To ensure the possibility of performing laboratory work, students must be instructed in safety, the fact of which is recorded by the personal signature of the student in the journal of safety.

The terms of working off and defence of each separate laboratory work are brought to the notice of students by the teacher. In the absence of protection of two laboratory works during a cycle the admission to working off of the following work according to the schedule is impossible.

Instructions for the laboratory work of the cycle are given in Addition 1. An example of the design of the title page to the protocol of laboratory work is given in Addition 2.

LAB № 1**ANALYSIS OF BINARY COUNTERS****I. Purpose of work**

Study of properties of binary counters of the K155 series. A set of integrated meters, as well as a number of logical elements that are part of the laboratory layout, allow you to master the basic principles of construction of meters with a given conversion factor and other digital devices based on them.

II. Layout description

The laboratory layout includes the following main components:

1. Typesetting field, which houses integrated meters of different types and logic elements.
2. Four-bit binary counter based on D-type triggers, which is used as a code generator.
3. LED indicators of the status of meters and logic elements.
4. Gas-discharge decimal indicators of the status of meters.
5. A number of sockets to which the voltage corresponding to logic "1" and logic "0" is brought.
6. Power supply that provides voltage of the required level (+ 5V) all the chips of the layout.

The following elements are located on the typesetting field of the layout:

- decade counter with phase-pulse representation of information type K155IE1;
- binary-decimal 4-bit counter type K155IE2;
- counter divider on 12 type K155IE4;
- binary 4-bit reversible counter type K155IE7;
- frequency divider with variable division factor type K155IE;
- 4 logical elements 2 AND-NO;
- 3 logical elements 3 AND-NO;
- 2 logical elements 4 AND-NO.

The inputs and outputs of counters and logic elements under study are connected to the sockets located on the front side of the typesetting field. The sockets are connected by wires to the plugs at the ends.

4-bit binary code generator is used to control the operation of the meters under study. The code generator is made of four D-type triggers connected in series, each of which operates in recalculation mode. The clock input of the first flip-flop is connected to the output of the master generator (MG), located inside the MG layout can operate in two modes - self-oscillating and external excitation.

In the first mode, the MG frequency can be changed discretely with the "F1-F2" key, as well as smoothly with the "FREQUENCY" knob. In the second mode, the frequency of operation of the MG is determined by the frequency of pressing the "SINGLE" key.

Switching of MG modes is carried out by the AVT-MANUAL key, thus stay of the key in the AVT position corresponds to the auto-oscillating mode of MG operation, and stay in the MANUAL position - the mode with external excitation. Indication of states of counters and logic elements is carried out by means of LEDs like AL310A. When the voltage levels corresponding to logic "1" are applied to the sockets of the LEDs, the LEDs light up. When the voltages corresponding to the logical "0" are applied, the LEDs go out.

The decimal digit indicator is assembled on two gas-discharge indicators type IN12B, which are controlled by a full binary decoder located inside the layout. When a decimal indicator of binary codes with weights of 1-2-4-8 digits is applied to the sockets "1-2-4-8", their decimal equivalents are displayed on the indicator.

III. Work program.

1. Exploration of the decadal counter K155IE1.

To do this, apply to the counting input C pulses from the output of the trigger of the lower digit of the code generator. Pulses can be applied separately to each of the counting inputs C (the second counting input must be a logical "1"), and to both inputs C simultaneously (Fig. 1).

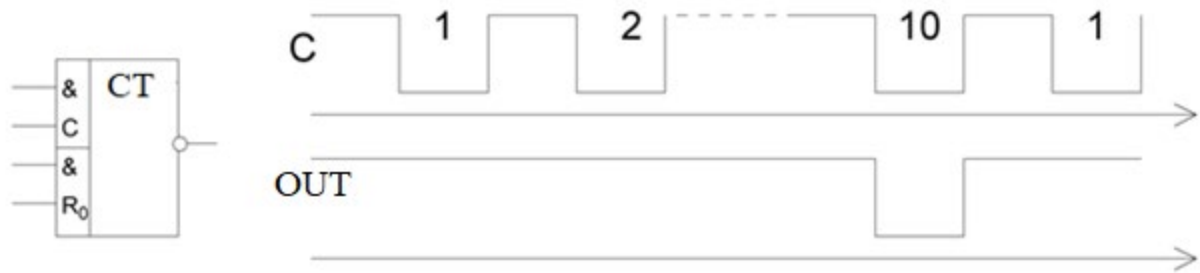


Fig. 1. Scheme and timing diagrams explaining the principle of operation of the decadal counter K155IE1

Use the oscilloscope to observe the shape of the input and output signals. Draw oscillograms of pulses.

Note: Setting the counter to zero is carried out by applying a positive setting pulse to the inputs R₀. Pulses can be applied separately to each of the inputs (the second input must be a logical "1") or to two inputs simultaneously.

Setting the counter to zero can be carried out by a short-term supply to the inputs R₀ level logic "1".

2. Exploration of the binary-decimal counter K155IE2.

2.1. Get acquainted with the purpose of the pins of the chip K155IE2 and its functionality according to the directory [1].

To study work of the K155IE2 counter by means of gas-discharge indicators. The outputs Q_1, Q_2, Q_3, Q_4 of the counter must be connected to the input sockets of the indicators, taking into account the bits. Use the pulses generated by the code generator as counting pulses.

Give time charts.

Note: The counter K155IE2 consists of a trigger with a counting input and a counter with a conversion factor equal to 5. When connecting them together (output Q_1 connected to the input C_2) the consecutive binary-decimal counter works in the code 1-2-4-8 turns out (fig. 2).

The triggers of the counter are set to zero when a positive pulse (logic "1") is applied to the inputs R0. In this case, at least one input R9 must be a logical "0".

To set the counter in state 1001, it is necessary to apply a logical "1" to the inputs R9. In this case, at least one input R0 must be a logical "0".

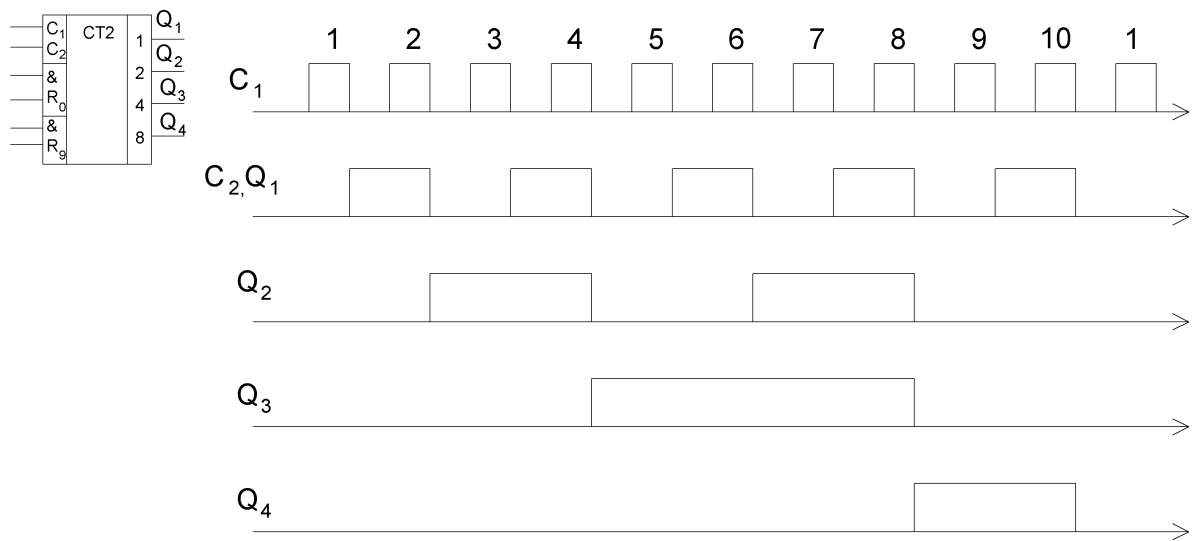


Fig. 2. Scheme and timing diagrams explaining the principle of operation of the binary-decimal counter K155IE2

2.2. Investigate the operation of the counter K155IE2, which provides $\kappa_n \neq 10$. Using inputs R0 and R9 assemble the counter with $\kappa_n = 6$ (fig. 3). Draw time diagrams of input and output pulses.

Note: The principle of operation of the counter is that when the desired state is reached (in this case after the arrival of six pulses) at two inputs R0 appears logical "1" and the counter goes to state "0" (Fig. 3).

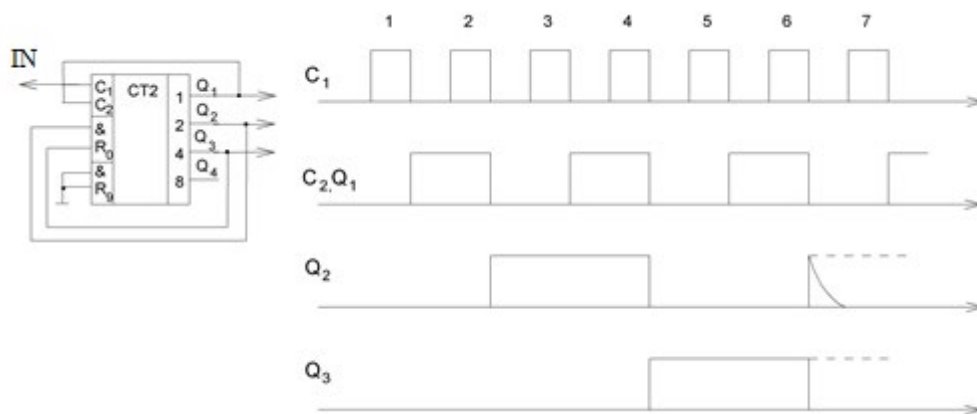


Fig. 3. Scheme and timing diagrams explaining the principle of operation of the binary-decimal counter K155IE2 with $\kappa_n = 6$

Similarly assemble the counter with $\kappa_n = 2; 4; 7; 8$ (on behalf of the teacher).

Give time charts.

Counters with each κ_n on the basis of chips K155IE2 can be obtained using inputs R9. In this case, after a given state, the counter goes to state "9", and then to zero.

Figure 4 shows a diagram of the counter with $\kappa_n = 7$ and timing charts explaining its operation.

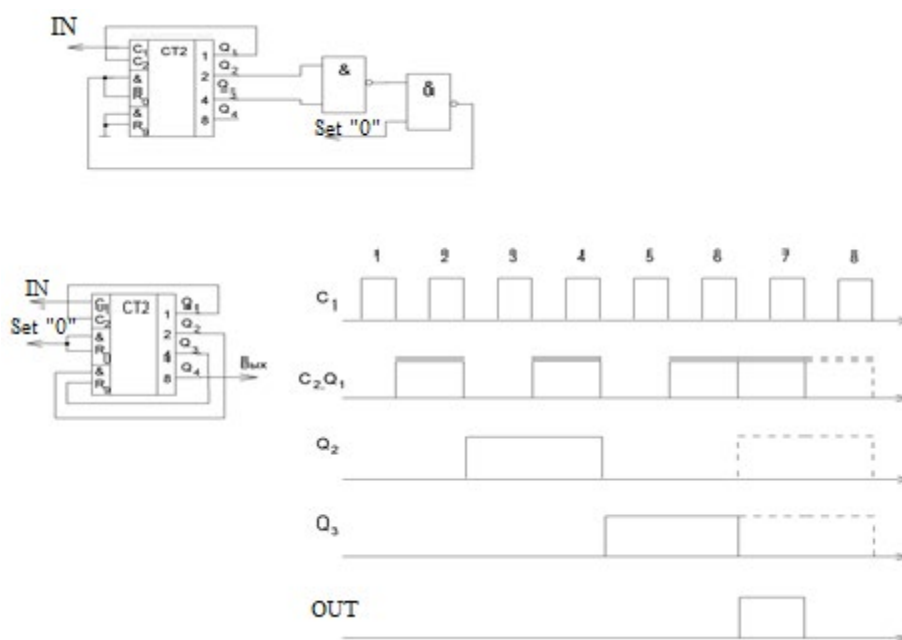


Fig. 4. Scheme and timing diagrams explaining the principle of operation of the binary-decimal counter K155IE2 with $\kappa_n = 7$

Similarly assemble the counter with $\kappa_n = 3;5;6;9$ (on behalf of the teacher).

Give time charts.

3. Study of the properties of the counter-divider by 12 (K155IE4).

3.1. Get acquainted with the purpose of the external pins of the chip K155IE4 and its functionality according to the directory [1].

3.2. Examine the operation of the counter in the mode of division by 6 and 12.

Note: The K155IE4 chip contains a counting trigger (input C_1 , output Q_1) and divider by 6 (input C_2). By connecting output Q_1 with input C_2 you can get $\kappa_n = 12$.

Since the output code of the counter K155IE4 "1-2-4-8" differs from the input code of gas-discharge indicators, it is necessary to use LED indicators to indicate the states of the meter (LED radiation corresponds to the logical "1", no glow to the logical "0").

3.3. Study the principles of construction of meters on the basis of the chip K155IE4 with $\kappa_n \neq 12$. Using inputs R0 assemble the counters from $\kappa_n = 3;4;5;7;8;9;10$ (according to the teacher's instructions).

Note: The principle of construction is similar to that given in paragraph 2.3.

4. Study of the 4-bit binary counter K155IE5.

4.1. Get acquainted with the purpose of the external pins of the chip K155IE5 and its functionality according to the directory [1].

4.2. Study work of the K155 IE5 counter with $\kappa_n = 8;16$ by using the gas-discharge indicators. Connect the counter to external circuits in the same way as in paragraph 2.2.

Note: The counter K155IE5 contains a counting trigger and a divisor of 8, consisting of three triggers connected in series. The polarity of the input pulses is similar to the chip K155IE2.

4.3. Study the work of counter K155IE5 with $\kappa_n = 3;4;5;6;7;9;10;13$ (according to the teacher's instructions). Show time diagrams of input and output signals.

Note: Construction of the counter with arbitrary to carry out similarly to point 2.2. In fig. 5 as an example of construction shows a diagram of the counter with $\kappa_n = 10$.

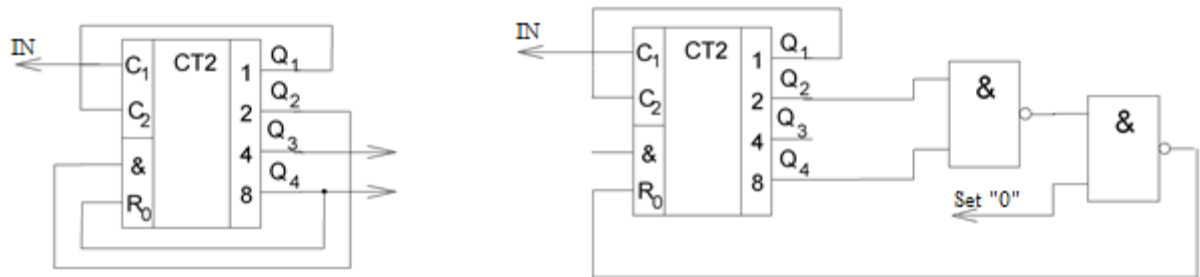


Fig. 4. Diagram and timing diagrams explaining the principle of operation of the 4-bit binary counter K155IE5 with $\kappa_n = 10$

5. Research of the 4-bit binary reversible counter K155IE7.

5.1. Get acquainted with the purpose of the outputs of the counter K155IE7 and its functionality.

5.2. Investigate the operation of the meter in the mode of summation and difference.

To do this, count the pulses from the output of one of the bits of the code generator to apply either to the input +1, or to the input -1 of the counter. In this case, the input R0 must be present logical "0", and the input C - logical "1".

Indication of operation of the counter to carry out gas-discharge indicators.

5.3. Investigate the operation of the counter with pre-installation of the source code. To do this, install the inputs D_1, D_2, D_4, D_8 to submit the code of some number, and the input C is briefly logical "0". The calculated pulses are given similarly to paragraph 5.2.

5.4. Investigate the operation of a reversible counter with a given conversion factor. Build a reversible counter with $\kappa_n = 3...15$ (as instructed by the teacher), using the input R0 to forcibly reset the counter.

Forced zeroing of the counter should be carried out similarly to paragraph 2.2.

6. Study of frequency divider K155IE8.

6.1. Get acquainted with the purpose of the outputs of the chip K155IE8 and its functionality.

6.2. Study the operation of the chip K155IE8 in frequency division mode. Provide output frequency $f_{\text{out}} = \frac{f_{\text{ex}} \cdot N}{64}$ (value N is set by the teacher). Give oscillograms of input and output pulses.

IV. List of recommended reading

1. Handbook of integrated circuits, ed. Tarabrina BV - M: Energy, 1980.
2. Analog and digital integrated circuits. Ed. Yakubovski S.V. - Moscow: Soviet Radio, 1979.

LAB № 2

COMBINATION DEVICES WITH LOGICAL ELEMENTS

I. Purpose of work

Study of the properties of some types of transistor-transistor logic (TTL) elements of the K155 series.

The set of logical elements available in the laboratory layout allows us to explore the main types of logical functions of two arguments, as well as to implement the given functions of three and four arguments. On this laboratory model it is possible to carry out research of various simple control devices, in particular, decoders of a binary code in decimal.

II. Layot description

The laboratory layout includes the following main components:

1. A set of logical elements, the inputs and outputs of which are displayed on the assembly field.
2. A four-bit binary counter used as a code generator.
3. Indicators of the state of logical elements and circuits.
4. Decimal digit indicator.
5. Power supply.

The following logical elements are located on the typesetting field of the layout:

- 8 three-input elements AND;
- 8 two-input elements AND;
- 1 four-input element OR;
- 1 three-input element OR;
- 1 two-input element OR;
- 5 elements NO (inverters).

The inputs and outputs of the logic elements are connected to the sockets located on the front side of the typesetting field. By connecting the sockets with conductors to the plugs at the ends, you can implement different logic circuits within the capabilities of the typesetting field. All logic elements are connected to a power supply that produces a stabilized voltage of +5 V.

Note: Elements I are obtained by sequentially connecting the AND-NO elements with the NO elements. Elements OR are derived from elements 4AND-NO, 3AND-NO, 2AND-NO. In fig. In Fig. 1 shows a diagram of the element 2 OR, assembled from the elements 2I-NO chips type K155LA3.

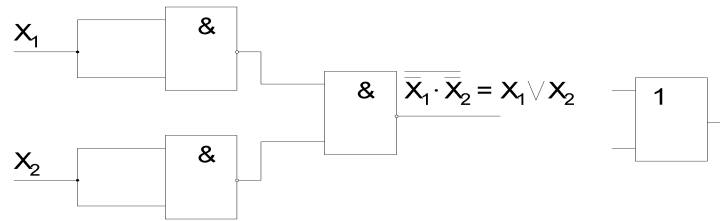


Fig. 1. Scheme of element 2 OR

Similarly, the elements 3 OR, 4 OR are implemented. To obtain elements 4 OR, 4 elements 2AND-NO and element 4AND-NO are used, to obtain element 3 OR - 3 elements 2AND-NO and element 3AND-NO.

The code generator is used to specify sets of arguments to logical functions. The basis of the generator is a 4-bit binary counter on D-flip-flops (K155TM2) (Fig. 2). At the outputs of the counter you can get 16 different four-digit binary numbers.

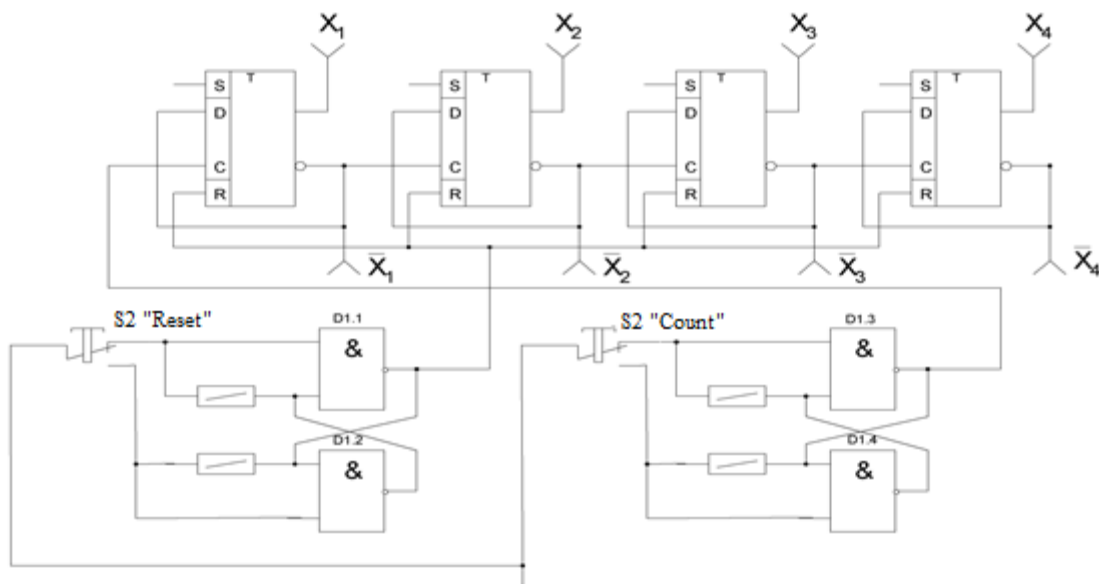


Fig. 2. Scheme of a 4-bit binary counter on D-flip-flops

RS -trigger, assembled on the elements 2 AND-NO (D1.1, D1.2) is designed to reset the counter. To receive the code 0000 at the outputs of the counter, it is necessary to press the "RESET" button. The RS-flip-flop on elements D1.3, D1.4 provides supply to the input of the counter of counting pulses. To obtain the desired binary code, you must press the "COUNT" button the appropriate number of times.

Indication of the states of logic elements and 4-bit binary numbers at the output of the meter is carried out using LEDs type AL310A. The connection of LEDs to the power supply is made by MS type K155LA8 (Fig. 3). When sending X_1, X_2, X_3, X_4 positive signals corresponding to the logical unit, LEDs $V_2... V_5$ light up. The current flowing through each LED is limited by resistors $R_2 ... R_5$ at the level of ~ 15 mA. When the signal "0" on the sockets X_1, X_2, X_3, X_4 LEDs go out.

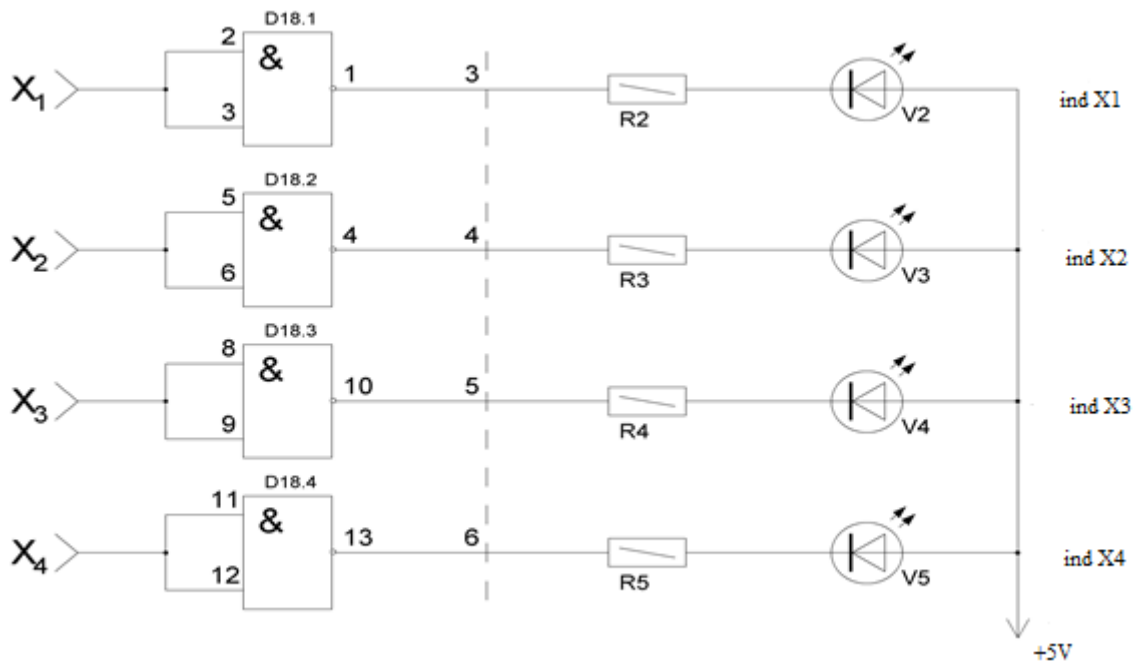


Fig. 3. Scheme of the chip type K155LA8

The indicator of decimal digits is assembled on the gas-discharge indicator H1 type IN12B (Fig. 4). Transistors $V_1 ... V_8$ act as high-voltage switches. When a positive bias is applied to the base of one of the transistors, it opens and connects to the power supply cathode, which forms a number. The resulting digit in the form corresponds to a decimal digit. Resistors $R_1, R_3, R_5, R_7, R_9, R_{11}, R_{13}, R_{15}$ limit the base current of transistors, resistors $R_2, R_4, R_6, R_8, R_{10}, R_{12}, R_{14}, R_{16}$ are

used to lock transistors when the indicator is not connected to logic elements of the typesetting field. Resistor R17 is needed to limit the current through the gas discharge indicator at the level of ~ 1 mA.

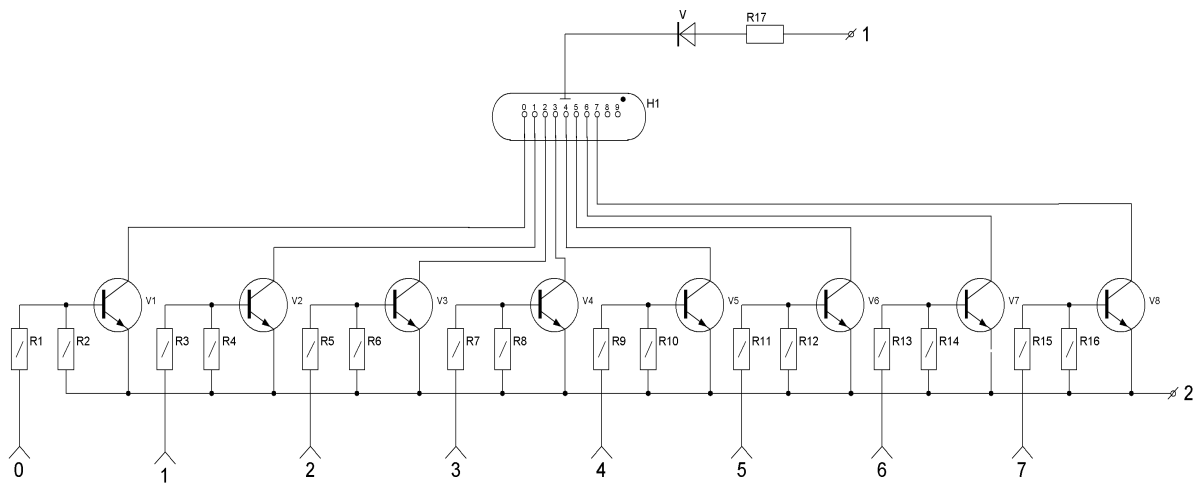


Fig. 4. The scheme of the gas-discharge indicator H1 type IN12B

The power supply is a stabilized voltage rectifier +5 V, mounted inside the models. On the front panel there is a toggle switch to turn on the source and a signal light.

III. Work program

1. Investigate the scheme of a 4-bit counter built on D-flip-flops (Fig. 2). Write the number from 0 to 15 in binary code and, connecting the indicator to the direct output of each digit of the counter, check the operation of the counter by applying pulses to its input by repeatedly pressing the "COUNT(СЧЕТ)" button.

Note: The counter is pre-set to zero.

The counter serves as a code generator for the task of a set of arguments X1, X2, X3, X4 of logical functions in the following task points.

2. Assemble a circuit that implements the majority logic (a unit appears at the output if there is a unit at all three or any two inputs).

3. With the help of logical elements AND, OR, NOT to implement the following functions of 2 arguments (according to the teacher)

$f_1, f_2, f_3, f_4, f_5, f_6, f_7, f_8, f_9, f_{10}, f_{11}, f_{12}$. The logical functions of the 2 arguments are shown in table 1.

Table 1. Logical functions of 2 arguments

Func tion	Variables	X_1	1	1	0	0	Conjunctive and disjunctive form
		X_2	1	0	1	0	
f_0	Zero function		0	0	0	0	-----
f_1	Conjunction "AND"		1	0	0	0	$X_1 + X_2 = \overline{\overline{X_1 + X_2}}$
f_2	Disjunction "OR"		1	1	1	0	$\overline{\overline{X_1} \cdot \overline{X_2}} = X_1 + X_2$
f_3	Schaeffer's stroke		0	1	1	1	$\overline{X_1 \cdot X_2} = \overline{X_1} + \overline{X_2}$
f_4	Pierce's arrow		0	0	0	1	$\overline{\overline{X_1} \cdot X_2} = X_1 + X_2$
f_5	Prohibition X_1		0	0	1	0	$\overline{X_1} \cdot X_2 = \overline{X_1 + X_2}$
f_6	Prohibition X_2		0	1	0	0	$X_1 \cdot \overline{X_2} = \overline{\overline{X_1} + X_2}$
f_7	Inversion X_1		0	0	1	1	-----
f_8	Inversion X_2		0	1	0	1	-----
f_9	Equivalence		1	0	0	1	$(\overline{X_1} + X_2)(X_1 + \overline{X_2}) = \overline{X_1}X_2 + X_1\overline{X_2}$
f_{10}	Nonequivalence		0	1	1	0	$(X_1 + X_2)(\overline{X_1} + \overline{X_2}) = \overline{X_1}X_2 + X_1\overline{X_2}$
f_{11}	Implication X_1		1	1	0	1	$\overline{\overline{X_1} \cdot X_2} = X_1 + \overline{X_2}$
f_{12}	Implication X_2		1	0	1	1	$\overline{\overline{X_1} \cdot \overline{X_2}} = \overline{X_1} + X_2$
f_{13}	Repetition X_1		1	1	0	0	-----
f_{14}	Repetition X_2		1	0	1	0	-----
f_{15}	Logic 1		1	1	1	1	-----

3. Collect schemes for implementing the functions specified in table 2.

Table 2. Functions given in the table

X_1	X_2	X_3	1	2	3	4	5	6	7
0	0	0	1	0	0	0	1	1	1
0	0	1	0	1	0	0	0	1	0
0	1	0	1	0	1	1	1	1	0
0	1	1	0	1	0	1	1	1	0
1	0	0	0	1	1	1	1	0	1
1	0	1	1	0	1	0	1	0	1
1	1	1	0	1	0	0	1	1	1

4. Make a sample from a 4-digit counter of the following numbers (as instructed by the teacher):

- all even;
- all odd;
- all numbers more than 8;
- all numbers multiples of 4;
- all numbers less than 5;
- numbers 0, 1, 2, 3;
- numbers 4, 5, 6, 7;
- numbers 8, 7, 11, 15;
- numbers 4, 6, 12, 14, etc.

5. Assemble the following decoder circuits to indicate the decimal numbers recorded in the first three digits of the counter:

- a) linear decoder (Fig. 5);
- b) rectangular or matrix decoder (Fig. 6);
- c) pyramidal decoder (Fig. 7).

Note: The decoder outputs are connected to the decimal digit indicator input.

In this case, each code combination removed from the counter must correspond to a

certain decimal digit, which lights up on the digital indicator.

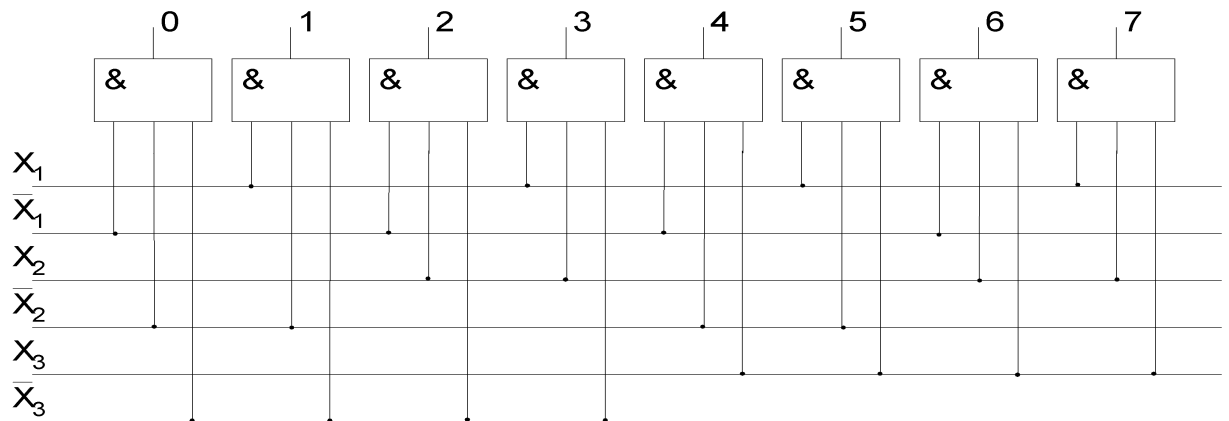


Fig. 5. Scheme of a linear decoder

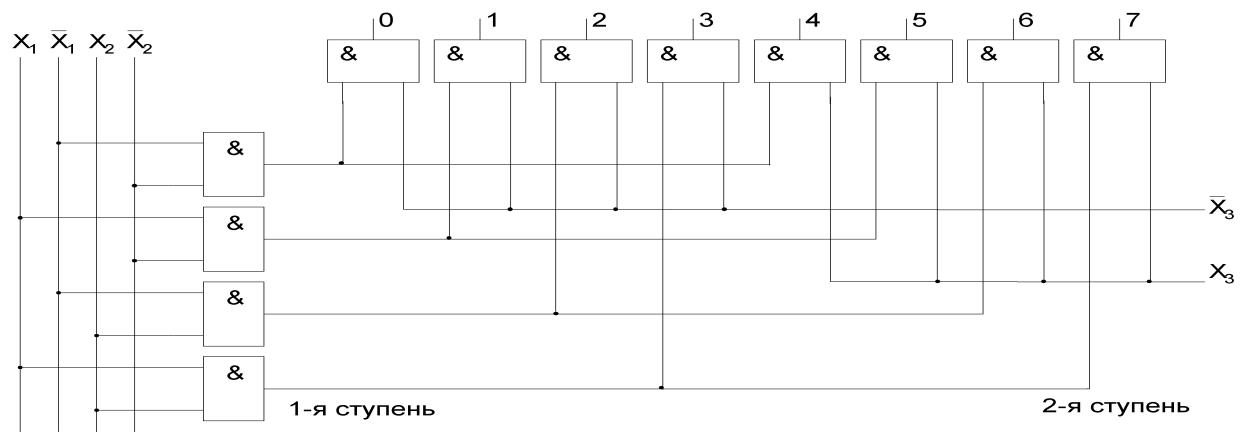


Fig. 6. Scheme of a rectangular or matrix decoder

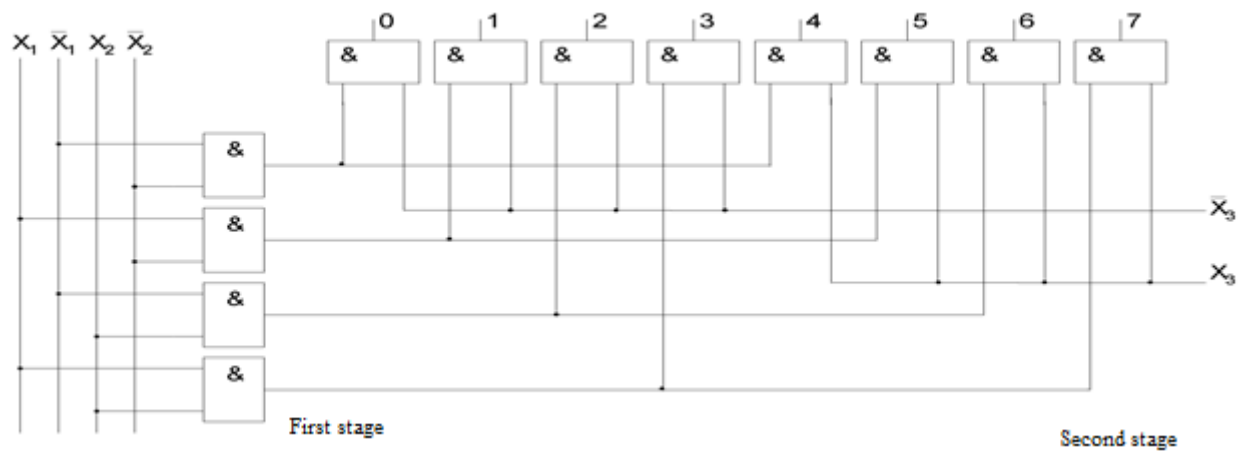


Fig. 7. Scheme of a pyramidal decoder

IV. Instructions for laboratory work

General instructions:

1. Assembly of schemes is made at the switched-off power supply of the model.
2. For each item of the program logical equations are made and their minimization is made.

To item 2. The sequence of construction of the scheme is as follows:

- a) a table of operation, where X_1, X_2, X_3 - input signals; F – output signal.

X_1	X_2	X_3	F
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

- b) the expression of the function is written in disjunctive normal form (DJN), or conjunctive normal form (CJN);
- c) minimization of the logical function using Carnot maps or other methods;
- d) in accordance with the minimized expression of the function in the selected element basis is a diagram of the device that implements the specified function.

To item 4. The sequence of implementation of the functions specified in table 2 is similar to that described in those specified in item 2. For example, $F_1 = \overline{X_1} \overline{X_2} \overline{X_3} \vee \overline{X_1} X_2 \overline{X_3} \vee X_1 \overline{X_2} X_3 = \overline{X_1} \overline{X_3} \vee X_1 \overline{X_2} X_3$. The scheme that implements this function is shown in Fig.8

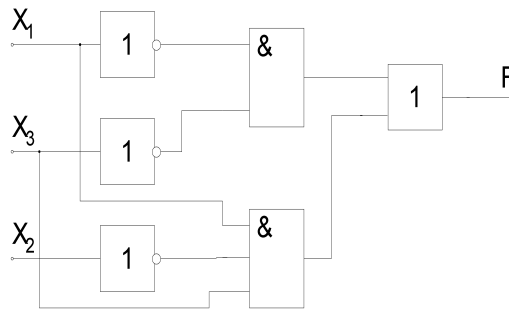


Fig. 8. Scheme that implements a logical function F_1

Schemes that implement other given functions are built in an analytical way.

To item 5. Sampling of the set numbers is made according to the technique described in instructions to item 2.

V. List of recommended reading

1. Kalabekov BA, Mamzelev I.D. "Fundamentals of automation and computer technology." - M.: Communication, 1980, – 296 p.
2. Guliy V.D., Budeniy A.V., Artemenko M.E. "Guidelines for the course of EPU". - K.: KPI, 1984, – 74 p.
3. Shiloh V.L. "Popular digital chips". - M.: Radio and communication, 1987, – 352 p.
4. Zeltsin E.A. "Digital integrated circuits in information and measuring equipment". - L.: Energoatomizdat, 1986, – 280 p.

LAB № 3

SYNTHESIS OF COMBINATIONAL DEVICES BASED ON MULTIPLEXERS

I. Purpose of work

Learn the principles of multiplexers, as well as to develop skills in designing combination devices (CD) on multiplexers.

II. Layot description

The laboratory layout contains a number of multiplexers of the K155 series (two multiplexers 1 of 4 and two multiplexers 1 of 8 types CD 2 and CD 7, respectively), which allow you to build CDs described by the logical functions of 3, 4, 5 variables.

To control the address inputs of the multiplexers, a binary code generator 1-2-4-8 is used, assembled on the basis of a 4-bit asynchronous binary counter on type D triggers. The input of the counter is connected to the output of the rectangular pulse generator.

Checking the correct operation of the synthesized CDs is performed using a control indicator device on gas-discharge indicators, creating a Carnot map of 4 variables. To control the correct operation of the CD, their outputs must be connected to the input of the indicator device and compare the induced Karnaugh map with the Karnaugh map of the specified function.

In addition to these devices, the model has a number of connectors, with the output voltage of logic 0 and logic 1. These connectors are adapted to set the signal levels at the information inputs of multiplexers.

The inputs and outputs of the multiplexers are connected to the connectors located on the front side of the layout field. By connecting the conductor outputs to the plugs at the ends, you can implement different CDs on multiplexers.

All logic elements as well as the display device are connected to the power supply, which is switched on by means of the keys located on the front panel.

III. Work program

1. Learn the principle of operation of multiplexers 1 of 4 and 1 of 8. For this purpose it is necessary to submit logical signals to their information inputs. By applying different combinations of binary numbers to the address inputs, determine the control laws of multiplexers.

Note: Multiplexers 1 of 4 are controlled by a two-bit binary code, and multiplexers 1 of 8 are controlled by a three-bit binary code created by an asynchronous counter.

2. Synthesize the CD circuit described by the logical function of three variables (given by the teacher), on the multiplexer 1 of 4. Assemble the CD, connect its output to the input of the indicator device and compare the induced Karnaugh map with the Karnaugh map corresponding to the logical function of the CD.

3. Synthesize a CD, described by the logical function of 4 variables (given by the teacher), on one multiplexer 1 of 8 and two multiplexers 1 of 4. Assemble the CD schemes and check the validity of the synthesis by comparing the induced Karnaugh maps with the Karnaugh maps corresponding to the logical equations.

4. Synthesize a CD that selects from a complete set of 4-bit binary numbers of combinations corresponding to the following decimal numbers:

- 1) all even;
- 2) all odd;
- 3) numbers 1,2,3,4,5;
- 4) numbers multiples of 3;
- 5) numbers 1,2,3,9,10,11;
- 6) all numbers less than 10 and equal 10;
- 7) all numbers > 10 .

5. Synthesize a CD circuit that performs the operation of comparing two 2-bit binary numbers on multiplexers 1 of 4 and 1 of 8.

Note: Use the corresponding outputs X1, X2 and X3, X4 of the binary counter as comparable numbers.

6. Synthesize the scheme of the adder of two single-digit numbers based on multiplexers 1 of 4.

7. Synthesize the circuit of the pulse sequence generator specified by the teacher, based on multiplexers.

IV. Instructions for laboratory work

Multiplexers (switches) have a number of information inputs B_1, B_2, \dots , address inputs A_1, A_2, \dots , input for gating signal C and one output Q (there is also an additional output \bar{Q}).

The operation of multiplexers is that when a specific code is applied to the address inputs, binary information is received from one of the information inputs. The gating input must have a corresponding signal $C = 1$ ($C = 0$). In the absence of a gating signal ($C = 0$), there is no connection between the information inputs and the output ($Q = 0$). The operation of the multiplexer 1 of 4 is determined by the logic function $F_{1-4} = \bar{A}_1 \bar{A}_2 B_1 + A_1 \bar{A}_2 B_2 + \bar{A}_1 A_2 B_3 + A_1 A_2 B_4$. And the operation of the multiplexer 1 of 8 is determined by the logical function $F_{1-8} = \bar{A}_1 \bar{A}_2 \bar{A}_3 B_1 + A_1 \bar{A}_2 \bar{A}_3 B_2 + \bar{A}_1 \bar{A}_2 A_3 B_3 + A_1 \bar{A}_2 A_3 B_4 + \bar{A}_1 A_2 \bar{A}_3 B_5 + A_1 A_2 \bar{A}_3 B_6 + \bar{A}_1 A_2 A_3 B_7 + A_1 A_2 A_3 B_8$.

Multiplexers can be used to make CDs, which are described by the logical functions of 3, 4 and 5 variables, respectively, on one multiplexer 1 of 4, 1 of 8 and 1 of 16.

Rules for building a CD on one multiplexer:

- 1) compile a truth table of functions describing the CD for all sets of variables;
- 2) $i-1$ variable ($i = 3, 4, 5$) starting from the highest digit, apply to the address inputs of the multiplexer;
- 3) to the appropriate information inputs of the multiplexer to submit values that are determined by the truth table and belong to the set $\{X_1, \bar{X}_1, 0, 1\}$.

Consider an example of the implementation of a logical function given in table. 1.

Table 1. Logical function of three variables

X_3	X_2	X_1	f	B
0	0	0	1	$B_1(1)$
0	0	1	1	
0	1	0	0	$B_2(X_1)$
0	1	1	1	
1	0	0	1	$B_3(\overline{X_1})$
1	0	1	0	
1	1	0	0	$B_4(0)$
1	1	1	0	

This function can be implemented on a multiplexer 1 of 4. Considering the variables X_3, X_2 as address signals (X_2 is fed to the input A_1 , X_3 is fed to the input A_2), we write the right column of table. 1. In it we will represent numbers of those information inputs which will be connected to an output of a multiplexer at corresponding sets of variables X_3, X_2 . Comparing the connected inputs with the values of the given function, as well as the variable X_1 , we determine the signals that must be applied to the information inputs $B_1 \div B_4$ (shown in the right column of Table 1 in parentheses). Schematic diagram of the CD shown in Fig. 1.

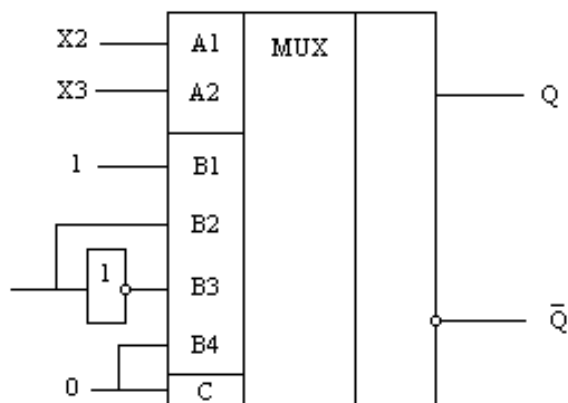


Fig. 1. Schematic diagram of a combination device based on a multiplexer 1 of 4

To implement the CD, described by the logical functions of 4, 5 or 6 variables, respectively, on two multiplexers 1 of 4, 1 of 8 or 1 of 16 you need:

- 1) make a table of truth of a given function for all sets of variables;
- 2) $i-2$ variables ($i = 4, 5, 6$), starting from the highest digit, apply in parallel to the address inputs of both multiplexers;
- 3) the variable with the following value is applied to the gating input of the first multiplexer directly and through the inverter to the gating input of the second multiplexer;
- 4) on the corresponding information inputs of the multiplexer defined by the truth table, to submit values of set $\{X_1, \overline{X_1}, 0, 1\}$;

5) connect the direct inputs of the multiplexers to the input of the OR element, the input of which will be the output of the CD.

Consider an example of CD implementation, which is described by a logical function given in table. 2, on two multiplexers 1 of 4.

Table 2. Logical function of four variables

X_4	X_3	X_2	X_1	f	B
0	0	0	0	0	$B_1(0)$
0	0	0	1	0	
0	0	1	0	0	$B'_1(X_1)$
0	0	1	1	1	
0	1	0	0	0	$B_2(X_1)$
0	1	0	1	1	
0	1	1	0	1	$B'_2(\overline{X_1})$
0	1	1	1	0	
1	0	0	0	1	$B_3(1)$
1	0	0	1	1	
1	0	1	0	0	$B'_3(X_1)$
1	0	1	1	1	
1	1	0	0	0	

1	1	0	1	0	$B_4(0)$
1	1	1	0	1	$B'_4(1)$
1	1	1	1	1	

To implement the given function on two multiplexers 1 of 4 it is necessary to apply variables X_4 and X_3 to the address inputs of both multiplexers (X_3 to input A_1 , X_4 to input A_2), variable X_2 to apply to the gating input of one multiplexer directly, and to the gating input of the other - through the inverter. The information inputs of the multiplexers must be fed the signals shown in the right column of table 2 in parentheses. The schematic diagram of the implementation of a given CD is shown in Fig.2.

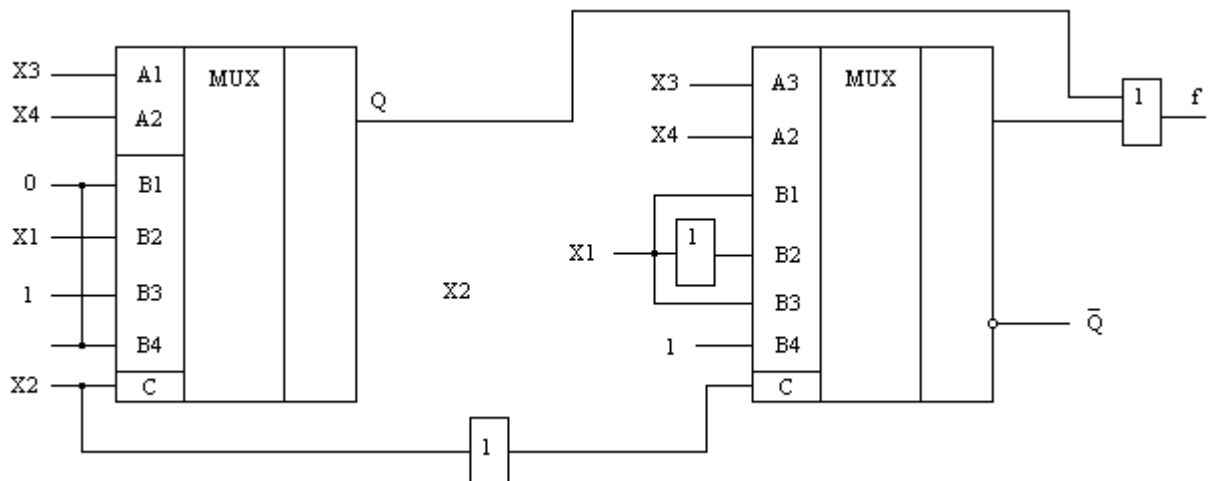


Fig. 2. Schematic diagram of a combination device based on two multiplexers 1 of

4

V. Contents of the protocol

- 1) Purpose of work.
- 2) Synthesis of schemes according to item 2,3,4,5,6,7 of the program.
- 3) Schemes of synthesized CD.

VI. List of recommended reading

1. Kalabekov BA, Mamzelev I.D. "Fundamentals of automation and computer technology." - M.: Communication, 1980, – 296 p.
2. Guliy V.D., Budeniy A.V., Artemenko M.E. "Guidelines for the course of

- EPU". - K .: KPI, 1984, – 74 p.
3. Shiloh V.L. "Popular digital chips". - M .: Radio and communication, 1987, – 352 p.
 4. Zeltsin E.A. "Digital integrated circuits in information and measuring equipment". - L .: Energoatomizdat, 1986, – 280 p.

LAB № 4

UNIVERSAL CODE CONVERTER

I. Purpose of work

Study of the principles of construction and operation of a universal programmable converter of 8-bit input code into 8-bit source code, built on the basis of random access memory (RAM).

II. Layout description

The investigated code converter is built on the basis of RAM (chip 505RU4 with a capacity of 256 bits). Eight such chips are used to obtain bitmap input and output codes equal to eight. The block diagram of the converter is presented in fig. 1.

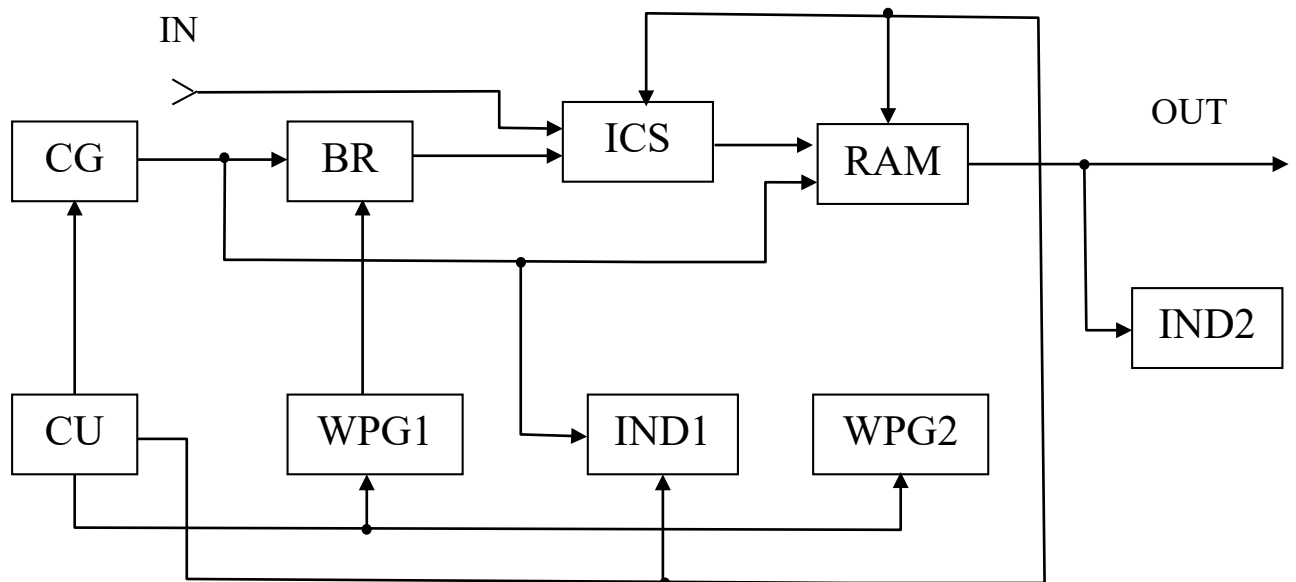


Fig. 1. Block diagram of the code converter

The converter includes the following blocks:

- code generator (GC); (MC01 ... 04)
- buffer register (BR); (MC 06 ... 07)
- input code switch (ICS); (MC 014 ... 017)
- random access memory (RAM); (MC 24 ... 31)

- control unit (CU);
- write pulse generator (WPG1) in the buffer register BR;
- indicator of input code and code of the code generator (IND1);
- recording pulse generator (WPG2) in RAM;
- source code indicator (IND2).

The schematic diagram of the converter is presented in Fig. 2.

The converter works in two modes - programming and working. The code generator serves to ensure the mode of RAM programming. It is an 8-bit parallel register made on RS-flip-flops, which use D-flip-flops (MS 155TM2) in the appropriate inclusion. The register is controlled by nine buttons, eight of which are used to record signals "logical unit" (hereinafter - "1"), and the ninth - to reset to a state corresponding to "logical zero" (hereinafter - "0"). By means of 8 setting buttons input and output codes of the converter in the programming mode are typed. To control the dialed code, IK1 is provided, which after pressing the "RESET(СБРОС)" button is connected to the output of the code generator and displays the code typed on the remote control.

First, enter the input code, then press the "INPUT CODE(ВХОДНОЙ КОД)" button. At the same time the write pulse generator executed on the basis of the RS-trigger works, and the information from code generator is written down in parallel 8-bit BR which is necessary for use of the same code generator for a task of both input, and an output code. BR is based on D-flip-flops (MS 155TM5). Simultaneously with pressing the "INPUT CODE(ВХОДНОЙ КОД)" button, the IR1 code indicator is disconnected from the code generator and connected to the address (input) bus of the RAM, as evidenced by the shutdown of the "RESET(СБРОС)" indicator. In this case, IK1 displays the input code.

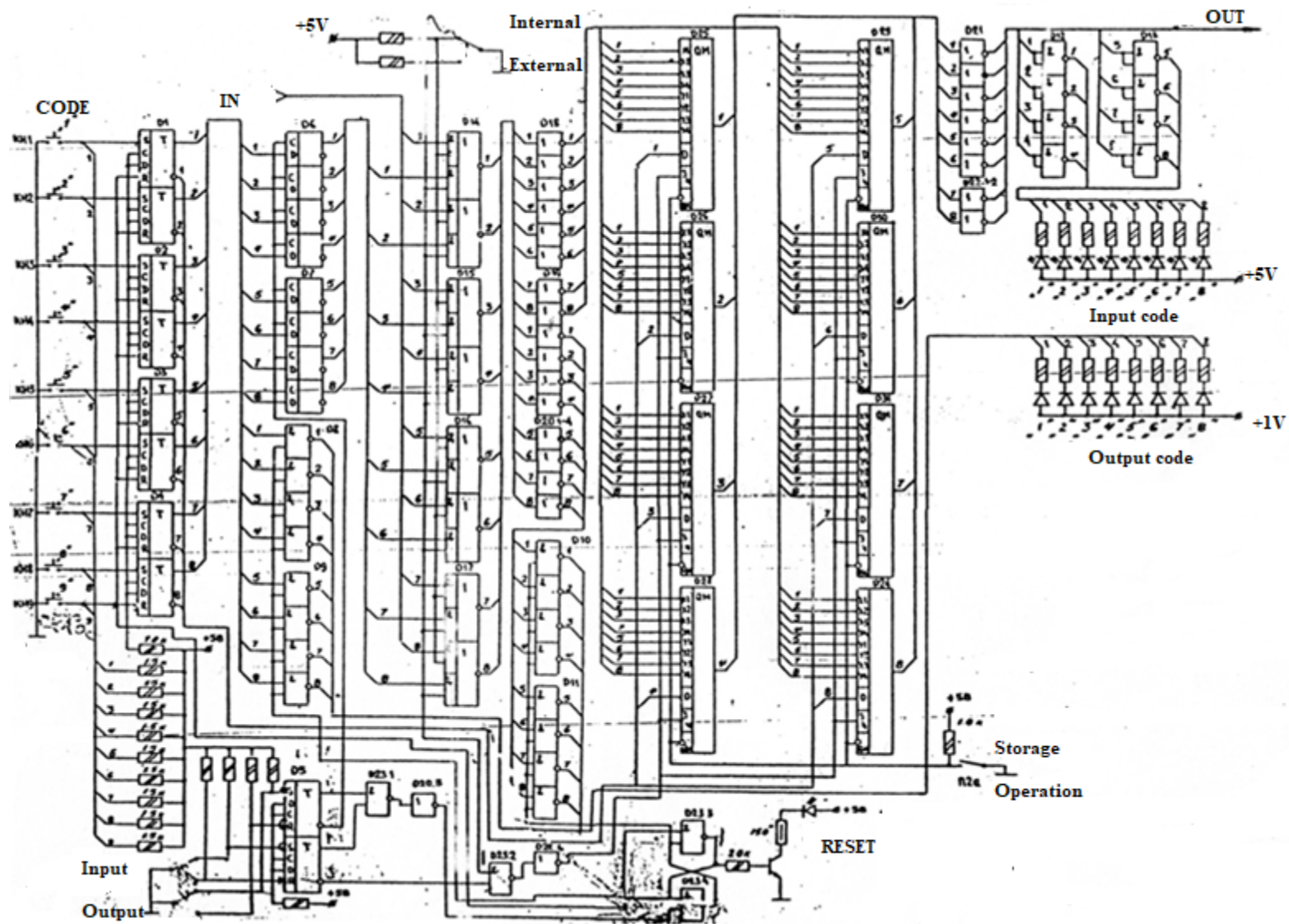


Fig. 2. Schematic diagram of the code converter

To dial the source code that corresponds to the typed input code, you must press the "RESET" button again. At the same time, the "RESET" mode indicator lights up and IK1 is reconnected to the code generator output and displays the reset mode of the latter (zeros in all digits of IK1). After that, dial the source code and press the "OUTPUT CODE" button. At the same time recording pulse generator works. The source code indicator source code indicator shows the source code stored in the RAM, and the IK1 is reconnected to the address bus of the RAM (as evidenced by turning off the "RESET" mode indicator) and displays the input code. Other RAM cells are programmed similarly.

To ensure the programming mode, the toggle switch "EXTERNAL CODE - INTERNAL CODE" must be in the "INTERNAL CODE" position, and the "OPERATION - STORAGE" switch in the "OPERATION" position. The input code switch is made on MS 155LR1 and is intended for connection of the address bus of RAM or BR in the programming mode, or to the input socket in the "OPERATION(PABOTA)" mode. The switch is controlled by the toggle switch "EXTERNAL CODE - INTERNAL CODE". The BU contains all buttons and toggle switches and sets the mode of operation of the converter. Input and output levels of signals of the converter are coordinated with level of signals of TTL logic.

The converter requires two supply voltages "+ 5V" and "+ 12V", which are provided by a power supply operating from 220V, 50Hz.

III. Work program

1. Learn the structural and schematic diagrams of the code converter.
2. Understand the purpose of individual units, the principles of their operation, as well as the sequence of the converter in programming mode and operating mode.
3. Program the transducer to convert the Gray code to binary code (see instructions for laboratory work).
4. Examine the operation of the converter in working mode from an external code generator.

5. Program the converter to convert binary code 8421 to binary code 2421.
6. Program the converter to convert binary code 8421 to code with excess 3.
7. Program the converter to convert 4-bit binary code to Heming code.

IV. Instructions for laboratory work

To item 3. Programming of the converter is carried out in the following order:

1. Make a table of correspondence of the Gray code to the binary code (Table 1).

Table 1. Gray code correspondence table to binary code

Grade	Gray code				Binary code			
№	4	3	2	1	4	3	2	1
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	1	0	0	1	0
3	0	0	1	0	0	0	1	1
4	0	1	1	0	0	1	0	0
5	0	1	1	1	0	1	0	1
6	0	1	0	1	0	1	1	0
7	0	1	0	0	0	1	1	1
8	1	1	0	0	1	0	0	0
9	1	1	0	1	1	0	0	1
10	1	1	1	1	1	0	1	0
11	1	1	1	0	1	0	1	1
12	1	0	1	0	1	1	0	0
13	1	0	1	1	1	1	0	1
14	1	0	0	1	1	1	1	0
15	1	0	0	0	1	1	1	1

2. The toggle switch "EXTERNAL CODE - INTERNAL CODE " is set to the position "INTERNAL CODE".

3. The toggle switch "OPERATION – STORAGE " is set to the position "OPERATION".

4. Turn on the power switch.
5. Press the "RESET" button. The "RESET" mode indicator lights up. The input code indicator should display "0" in all digits, the output code indicator should be set to an indefinite state.
6. Using the bit buttons, enter the input code from the first row of the correspondence table (in this case, all zeros, so do not press the button).
7. Press the "INPUT CODE " button. The "RESET(СБРОС)" indicator goes out, and the input code indicator lights up the input code (in this case, all the LEDs of the indicator will be off).
8. Press the "RESET" button.
9. Type the source code from the first row of the correspondence table (in this case, again, all zeros - do not press the button).
10. Press the "OUTPUT CODE" button. The "RESET" mode indicator goes out, the input code indicator shows the pre-typed input code, the source code indicator shows the source code from the first row of the table.
11. Press the "RESET" button.
12. Go to step 6 and use the second row of the table, etc. to the last row of the correspondence table

After programming, the corresponding source codes are written in the RAM cells, the addresses of which are determined by the input code. Repeating the input code results in the extraction of the pre-recorded source code from the RAM cell corresponding to this code.

To items 5, 6. The sequence of programming of converters is similar to that described in the instructions to item 3. Tables of correspondence for converters are made during independent preparation.

V. Contents of the protocol

- 1) Purpose of work.
- 2) Block diagram of the code converter.
- 3) Tables of correspondence of codes according to items 3, 5, 6, 7 of the program.

VI. List of recommended reading

1. Temnikov F.E., Afonin V.A., Dmitriev V.I. Theoretical foundations of information technology. M.: "Energy", 1979.
2. Analog and digital integrated circuits. Ed. Yakubovski S.V. - Moscow: Soviet Radio", 1979.
3. Ornatsky P.P. Automatic measurements and instruments. K.: "Higher school", 1980.

LAB № 5

ANALOG-DIGITAL DUAL INTEGRATION CONVERTER

I. Purpose of work

Getting acquainted with the principles of measuring electrical quantities, studying the principle of operation of the voltage converter - code (VCC) double integration.

II. Theoretical information

The basis of the model of laboratory work is a multimeter type BP-II. The multimeter is designed to measure basic electrical quantities:

- DC and AC voltages;
- DC resistance;
- DC and AC forces using an external shunt. In fig. 1 shows a block diagram of a multimeter.

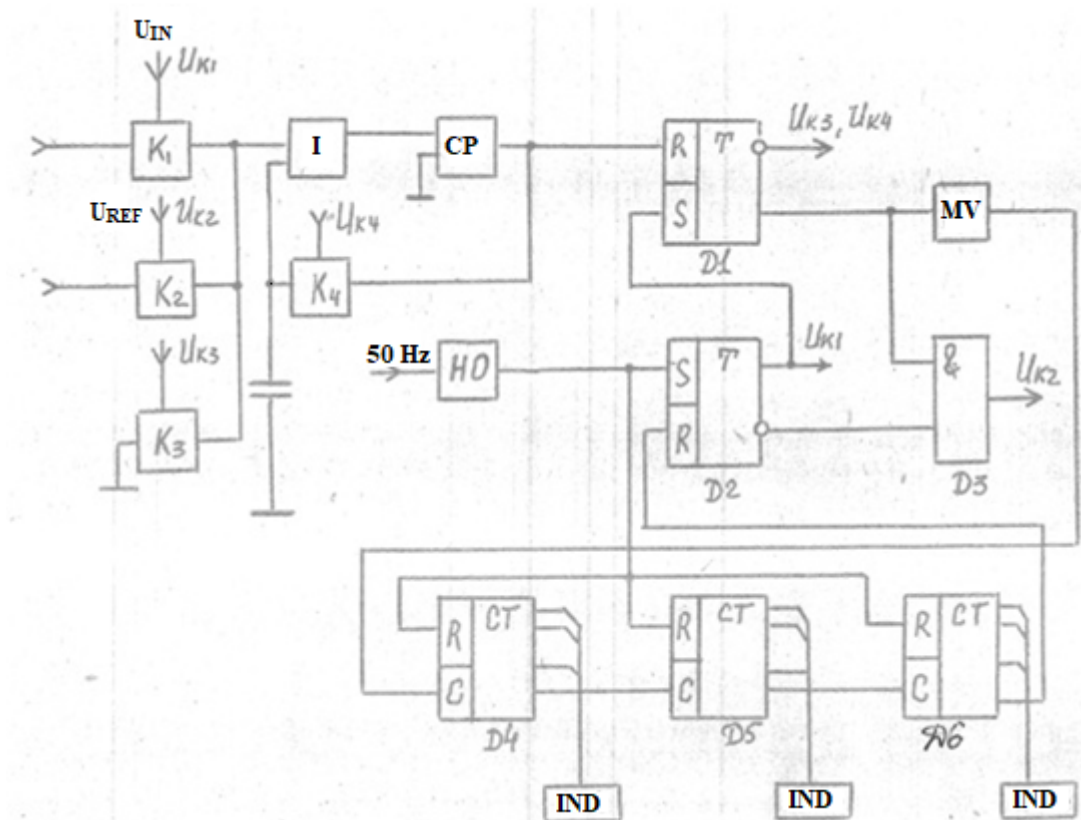


Fig.1. Block diagram of a multimeter

The measured values are transformed into a normalized analog voltage by means of an input voltage divider and a corresponding converter, which is then measured by means of a double integration VCC.

The essence of the method of analog-to-digital conversion by the method of double integration is as follows. In the first cycle, the measured voltage is integrated over the approximate time. The output voltage of the integrator increases according to the law:

$$U_{OUT}(t) = \frac{1}{\tau} \int_0^t U_{IN} dt,$$

where τ – integration time constant.

At the oment of time $t = T_1$ output voltage U_{OUT} reaches the value:

$$U_{OUT}(T_1) = \frac{1}{\tau} \int_0^{T_1} U_{IN} dt.$$

From this moment the second integration cycle begins T_2 , during which the sample voltage U_{samp} with the opposite polarity to the measured one is applied to the integrator input. The duration of the second clock is determined by the time of decrease of the output voltage of the integrator to zero.

To determine the duration of the second integration cycle, we write the equation:

$$U_{OUT}(T_2 + T_1) = U_{OUT}(T_1) - \frac{1}{\tau} \int_{T_1}^{T_1+T_2} U_{samp} dt.$$

Where after the transformations will we find

$$T_2 = \frac{1}{U_{samp}} \int_0^{T_1} U_{IN} dt.$$

Figure 2 shows diagrams of the output voltage of the integrator (dotted line corresponds to a larger value of the input voltage).

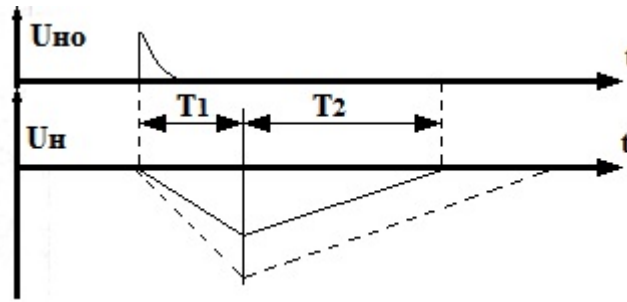


Fig. 2. Output voltage diagrams

Thus, the duration of the second integration cycle is proportional to the average value of the measured voltage, and the value does not depend on the time constant of the integrator, which reduces the error. To obtain a reference in digital form, the interval T_2 is filled with pulses of sample frequency F_0 . At a constant value of the input voltage, the reference value is equal to:

$$N = F_0 T_2 = \frac{T_1 F_0}{U_{samp}} U_{IN}.$$

To simplify the scheme of forming a time interval, its duration is taken equal $T_1 = N_0 / F_0$ where N_0 – the maximum countdown of the meter, which corresponds to the maximum input voltage. The final expression for determining the reference value has the form:

$$N = N_0 U_{IN} / U_{SAMP}$$

Thus, at a stable pulse frequency of the generator, the reference value does not depend on the period of repetition of the pulses of the sample frequency.

The functional diagram of the VCC double integration is shown in Fig.3.

Swth K_1 connects the input voltage to the input of the integrator U_{BX} for time period T_1 during the first integration cycle. Switch K_2 closes during the second clock for a time period T_2 , connecting to the input of the integrator sample voltage $-U_{OH}$. The comparator KP records the moment of passage of the output voltage of the integrator through the zero value.. Switches K_3 and K_4 are locked synchronously in the intervals between measurement cycles and are used to correct

zero drift. At this time, the code equivalent of the measured voltage is stored in the meter D4 ... D6.

The key management system contains 2 triggers D1 and D2 and a logic element D3. The synchronization of the control system is carried out by the moments of transition of the mains voltage, which is used as the primary power supply, through the zero value. In this case, the zero-organ emits a pulse at the beginning of the measurement cycle $T_1 \div T_2$, triggers D1 and D2 are set to a single state and the readings of the counters D4 ... D6 are reset. The MV multivibrator produces pulses of sample frequency F_0 . At the end of the 1000 pulse, the trigger D2 is switched, completing the formation of the interval T_1 , під час якого замкнутий. during which it is closed. Trigger D1 is in a single state during the measurement cycle $T_1 \div T_2$, switching under the action of the output voltage of the comparator КР at a time when the output voltage of the integrator becomes equal to zero. The voltage of its inverse output controls the operation of the keys K_3, K_4 . Voltage which controls K_2 is formed as a result of logical processing of the output signals of the triggers D1 and D2.

III. Work program

1. Learn the principle of operation, functional and schematic diagram of the ADC.
2. For two values of the measured voltage to remove oscillograms of voltages in control points of the model.

IV. Contents of the protocol

- 1) Purpose of work.
- 2) Schematic diagram of the AC to DC converter.
- 3) Functional diagram of the ADC.
- 4) ADC operation time diagrams for two voltage values.

V. List of recommended reading

1. Ornatsky P.P. Automatic measurements and instruments. K .: High school, 1980, – 560 p.
2. Gittis E.I., Piskulov E.A. Analog-to-digital converters. M .: Energoizdat, 1981, – 360 p.

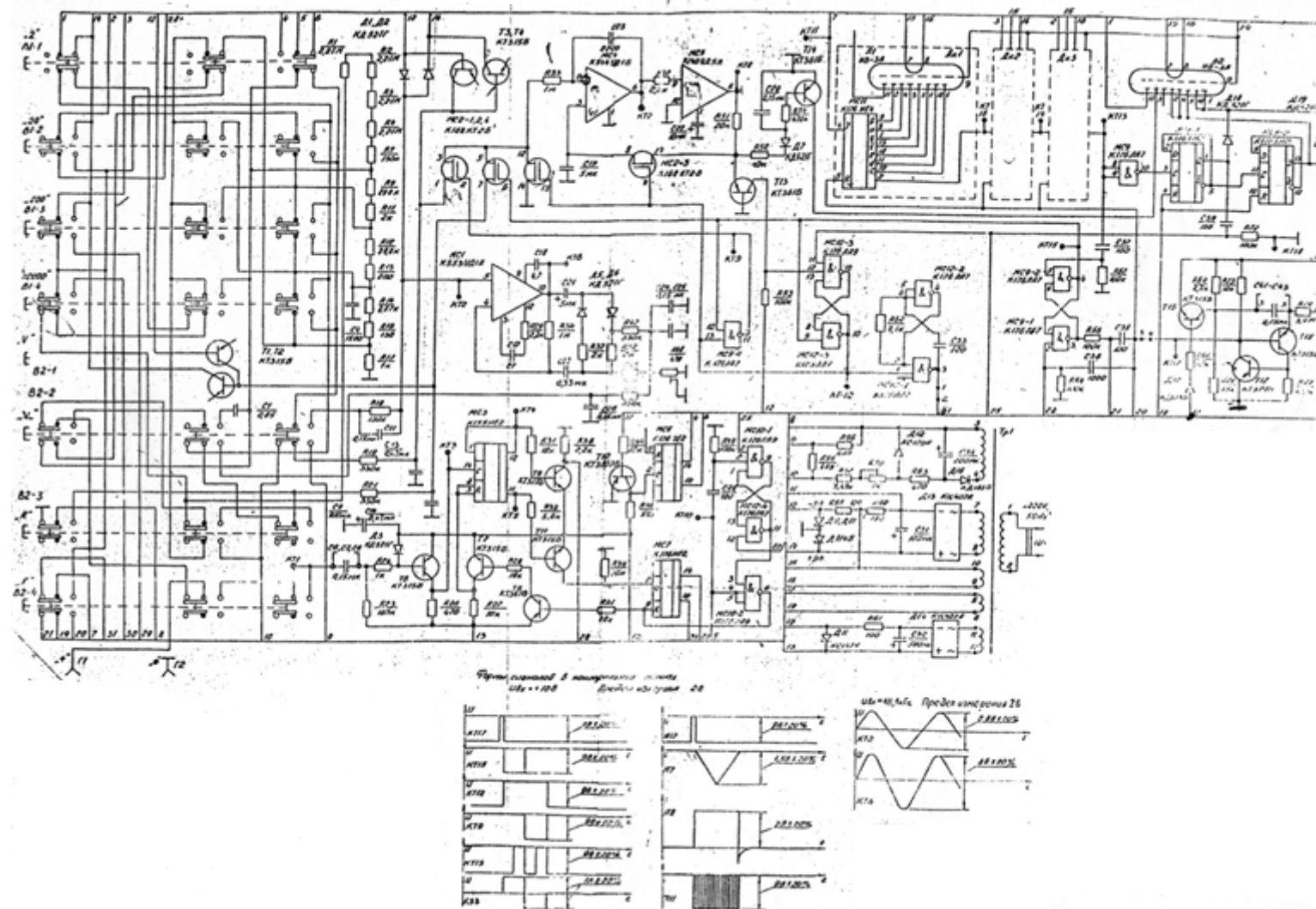


Fig. 3. Functional diagram of VCC double integration

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LAB № 1

Analysis of binary counters