Design of low power fast full adder using Domino Logic based on magnetic tunnel junction (MTJ) and memristor

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https://doi.org/10.54139/revinguc.v27i3.148

Abstract.- Domino CMOS circuits are widely used in high-performance very large scale integrated (VLSI) systems. The topology of domino circuits for high-speed operation, lower power consumption and robustness is of great importance in designing digital systems. The present paper proposes a low-power high-speed full adder circuit, which uses a new CMOS domino logic family based on magnetic tunnel junction (MTJ) elements and memristor in gate diffusion input (GDI) technique. In comparison with a static CMOS logic circuit, a dynamic logic circuit is of importance since it provides higher speed and requires fewer transistors. In comparison with the recently proposed circuits for dynamic logic styles, very low dynamic power consumption and less delay are the features of the proposed circuit. The problem with dynamic circuits is the lack of a stable output at different times, while the proposed circuit preserves the output value using memory elements such as MTJ and memristor during the clock cycle. The proposed technique shows a maximum power consumption of 0,317 μW in MTJ/memristor-based full adders. Moreover, the proposed technique shows a maximum delay of 0,35 ns. The proposed full adder is simulated, and its power dissipation and performance are analyzed using HSPICE in standard 7 nm CMOS technology.

Keywords: MTJ; Memristor; Domino Logic; Full Adder.

Diseño de sumador completo rápido de baja potencia utilizando Domino Logic basado en Unión de Túnel Magnético (UTM) y Memristor

Resumen.- Los circuitos CMOS de Domino se utilizan ampliamente en sistemas integrados de gran escala (VLSI) de alto rendimiento. La topología de los circuitos dominó para operación de alta velocidad, menor consumo de energía y robustez es de gran importancia en el diseño de sistemas digitales. El presente artículo propone un circuito sumador completo de baja potencia y alta velocidad, que utiliza una nueva familia lógica de dominó CMOS basada en elementos de unión de túnel magnético (UTM) y memristor en la técnica de entrada de difusión de puerta (GDI). En comparación con un circuito lógico CMOS estático, un circuito lógico dinámico es importante ya que proporciona una mayor velocidad y requiere menos transistores. En comparación con los circuitos propuestos recientemente para estilos lógicos dinámicos, las características del circuito propuesto son un consumo de energía dinámica muy bajo y menos retardo. El problema con los circuitos dinámicos es la falta de una salida estable en diferentes momentos, mientras que el circuito propuesto conserva el valor de salida utilizando elementos de memoria como UTM y memristor durante el ciclo de reloj. La técnica propuesta muestra un consumo máximo de energía de 0,317 μW en sumadores completos basados en MTJ/Memristor. Además, la técnica propuesta muestra un retraso máximo de 0,35 ns. Se simula el sumador completo propuesto, y su disipación de potencia y rendimiento se analizan utilizando HSPICE en tecnología CMOS estándar de 7 nm.

Palabras clave: MTJ; Memristor; Domino Logic; Sumador completo.

Received: August 25, 2020.
Accepted: September 21, 2020.

1. Introduction

In last few years, the use of internet of things (IoT) devices, cell phones, tablets and sensors has been dramatically increased. Most of these devices are battery-powered, so power consumption (battery life) can be considered as a design challenge. Consequently, researchers have attempted to present new techniques to design low-power electronics [1]. Non-conventional CMOS and nano-technology pave the way for designing low-power electronics, which reduce the leakage

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power consumption, so low-power applications can rely on emerging technologies in this area [2]. For reducing dynamic power consumption, the energy stored in load capacitors can be recovered instead of being dissipated as heat. This technique is referred to as adiabatic (reversible) circuit design [3].

Magnetic tunnel junction (MTJ) is a non-volatile memory with short access time and small dimensions as well as compatibility with CMOS technology [4]. Thus, it is well suited for using in logic-in-memory (LiM) architectures. LiM structures use MTJs and are very suitable for low-power designs because of almost zero static power dissipation. A memristor is also used as a memory element in this paper to design 1-bit full adder based on domino logic, and the results are eventually compared with MTJ family. In the following of this section, we will introduce the works that have been done in these fields.

Low-power designs are of great importance as the demand for battery-operated portable devices is ever-increasing. In a large number of this type of devices, the battery life is more important than the operating speed. Nano-devices and adiabatic designs are used in LiM structures to reduce, respectively, the static and dynamic power consumption. As an emerging technology, MTJ has many advantages when used in LiM structures along with CMOS technology. Sharifi [5] introduces a new adiabatic hybrid MTJ/CMOS structure for designing AND/NAND, exclusive-OR (XOR)//XNOR and 1-bit full adder circuits. The power consumption of the proposed adiabatic MTJ/CMOS full adder is more than 7 times less than those of the previous MTJ/CMOS full adders. In [6], the presented domino logic is based on MTJ elements in gate diffusion input (GDI) technique. A dynamic logic circuit is more interesting than a static CMOS logic circuit since it has higher speed and requires fewer transistors. In comparison with the recently proposed circuits for dynamic logic styles, very low dynamic power consumption and less delay are the features of the proposed circuit. Additionally, the proposed circuit shows extreme fault tolerance. A Monte Carlo simulation proves the fault tolerance of the full adder proposed in this reference. Standard 0,18 µm CMOS technology is used to simulate the proposed full adder. Both memory cell and sensing amplifier in this type of circuit, however, are less reliable, and this greatly limits the practical application of this type of circuit in logic computation. To resolve this issue, a new magnetic full adder (MFA) is presented in [7] based on pre-charge sensing amplifier (PCSA) and thermally assisted switching (TAS)-MTJ cell. Using the 65 nm CMOS technology and a precise TAS-MTJ model, mixed simulations are performed to show the high reliability while keeping low power consumption and small die area.

A few years ago, practical memristors were introduced and very soon attracted the interest of researchers and scientists. A memristor is the fourth basic two–terminal passive circuit element apart from well-known resistor, capacitor and inductor. Recently, memristor-based architectures have gained much attention from many researchers.

In this paper, we design memristor-based AND, OR and XOR gates. Using these gates, a memristor-based full adder circuit is proposed. The simulation results of the proposed circuit with these gates are reported. The remarkable improvements in the proposed circuit, compared to the conventional circuits, are lower power consumption by 54,74 %, less delay by 14,84 and using fewer transistors [8].

2. Background

The noise margin in domino logic is lower than that of static CMOS logic, so a relatively higher sensitivity towards noise source can be expected in domino logic circuits. Downscaling of the technology enhances noise immunity of domino logic circuits, while the power consumption of the circuit also increases. For reducing the consumed power, the supply voltage is scaled down, so the circuit delay increases. To compensate this delay, both the supply and threshold voltage scaling are performed. Reduction in the threshold voltage leads to a higher speed domino logic, while the noise immunity of the circuit decreases due to an increase in subthreshold leakage current [9, 10]. The thickness of the gate oxide is reduced as a result of downscaled technology, and this leads

to an exponential increase in gate leakage and subthreshold currents. These leakage currents may discharge the precharge node of domino circuits. Therefore, at high frequencies, leakage currents, low threshold voltage and noise sources degrade the performance of domino logic circuits [11].

Power consumption of CMOS full adders can be reduced by some techniques:

- Output and input capacitances can be minimized to reduce the dynamic power.
- Simultaneous use of both Vdd and GND in circuit components should be avoided to reduce the short and static power.
- For fewer transistors, we can use a pass transistor in a circuit; this reduces power consumption, while sometimes causes threshold losses.
- By varying the W/L ratio to minimize transistor conduction.

Various components of power consumption can be reduced by scaling down the device dimensions and supply voltage. The scaling down increases the leakage current due to the unfavorable short channel effects (SCEs) [12, 13, 14]. These effects decrease the effective channel length, which in turn, decreases the threshold voltage. Many research works have been conducted for reducing the power consumption in domino logic circuits [15, 16, 17].

2.1. Domino logic styles

To implement high-speed high-performance microprocessors, domino logic is more suitable than other dynamic logic styles since it requires less area and lower power [18]. Domino logic uses only one PMOS transistor in pull-up network (PUN) [13], so the area and the power consumption in domino logic is reduced compared to dynamic CMOS logic that uses n (number of inputs) PMOS transistors in the PUN.

The effects of leakage current and charge sharing on the dynamic node are prevented by the keeper transistor MK. The keeper ratio K is given by equation (1)

$$K = \frac{W_{Keeper}}{W_{PDN}}, \qquad (1)$$

where W_{Keeper} is the keeper transistor width and W_{PDN} is the evaluation transistor width in the PDN. The upsizing of keeper transistor MK enhances the robustness of the circuit by trading off the speed performance [15].

The control of the keeper circuit uses the following items:

1. delayed enabling of the keeper circuit,
2. abrupt keeper control mechanism,
3. keeper control signal with voltage swing variation,
4. keeper mechanisms with process variation tolerance and
5. bias voltage variation of the keeper device.

Other topologies based on PDNs with an additional discharge path have also been proposed in the literature. This modification results in increased operating speed and reduction in leakage current [15, 19]. Figure 1 shows a conventional domino logic circuit.

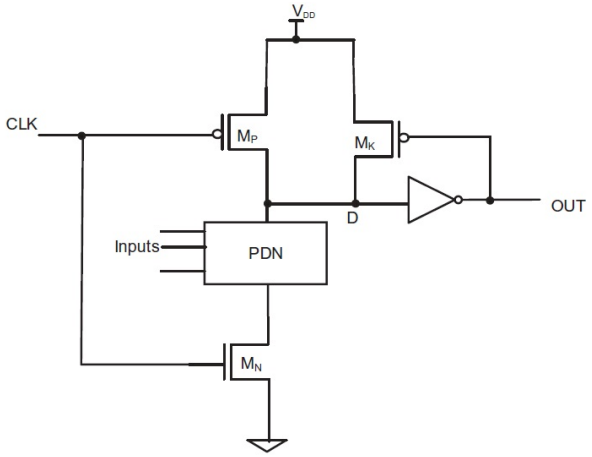
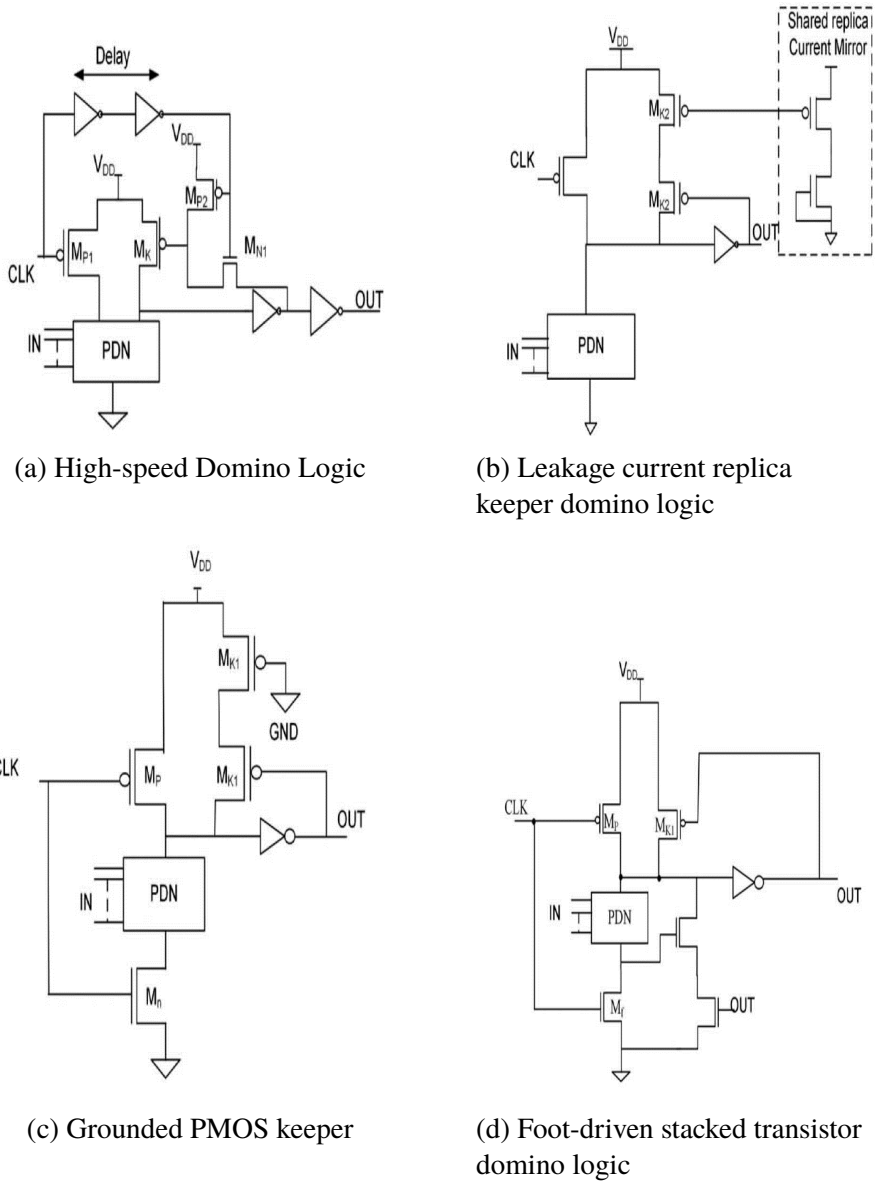


Figure 1: Conventional domino logic circuit

Figure 2a depicts a high-speed domino (HSD) logic [20]. In the leakage current replica (LCR) keeper technique shown in Figure 2b, an analog current mirror circuit controls the strength of the keeper device, which depends on the leakage current of PDN [21].

An additional keeper transistor and the existing conventional keeper transistor decrease the loop



(a) High-speed Domino Logic

(b) Leakage current replica keeper domino logic

(c) Grounded PMOS keeper

(d) Foot-driven stacked transistor domino logic

Figure 2: Existing domino logic circuit

gain and the delay variability in the grounded PMOS keeper structure depicted in Figure 2c [22]. The additional discharge path is controlled by the output and foot node voltages in foot-driven stacked transistor domino logic (FDSTDL) as shown in Figure 2d.

A CDDK circuit uses the principle of delayed enabling of keeper circuit, which consists of two PMOS keeper transistors in series. The delayed enabling of keeper circuit decreases the contention current between the keeper transistor and PDN. Therefore, if the PDN evaluates a TRUE condition, it facilitates faster discharge of the dynamic nodal charge through PDN, and this increases the operating speed of the circuit. In domino logic circuits, variations in the process parameters and feedback loop gain contribute considerably to the delay variability [23, 24]. These issues emphasize the need for identifying appropriate improvement techniques.

2.2. *Magnetic Tunnel Junction (MTJ) Review*

Magnetic tunnel junction comprises two ferromagnetic (FM) layers and an oxide barrier layer sandwiched between these two layers (Figure 3). Parallel and antiparallel configurations can be

realized according to the FM layers alignment. These two configurations are behind the low resistance (RP) or high resistance (RAP) behaviors of MTJ [25]. Therefore, these behaviors can be used in LiM designs.

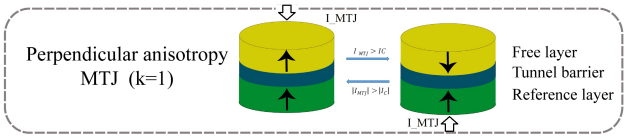


Figure 3: Vertical MTJ nanopillar structure. MTJ states change from P to AP and vice versa by applying a current (IMTJ) higher than the critical current (IC)

The techniques proposed for switching MTJ configurations are as follows: field induced magnetization switching (FIMS), thermally assisted switching (TAS) and spin torque transfer (STT). Spin torque transfer is the most promising technique, which is considered as a replacement for the other two techniques. This technique needs only a bi-directional low switching current. The states of the MTJ are switched when the current of MTJ (IMTJ) becomes higher than a critical current [26]. FIMS is the conventional approach for switching MTJ states, RAP and RP, which depend on the applied magnetic field. The disadvantages of this method are high power consumption, poor selectivity and poor scalability, which result from high switching currents.

2.3. *Memristor*

Custom neuromorphic hardware platforms are of great interest for accelerating neural network algorithms since they can perform complex tasks that are analogous to the physical processes in biological nervous systems [27]. A fundamental feature of these systems is their capability to overcome the restrictions [28]. The modern CMOS technology is employed to mimic the behavior of neurons; however, the lack of a device for effectively performing synaptic operations has hindered the advancement in this area for several years.

We propose a domino logic architecture for memristor-based neuromorphic computing. The architecture uses a simple binary neuron activation function and the delay of memristor RC circuits to perform synaptic computations. Synchronization schemes are presented to communicate information between the layers of neural network, and a simple linear power model is developed to estimate the energy efficiency of the architecture for a particular network size.

2.3.1. *Memristor Modeling*

Chua and Kang introduced physical memristive devices; however, the area of memristors and memristive devices has not drawn any interest for more than 35 years. In 2008, the theory of memristive devices was developed by Hewlett Packard researchers, and this theory was implemented in TiO_2 resistive switches. Hewlett Packard researchers proposed a device, which was claimed to be similar to an ideal memristor when it came to the structure and behavior of the device.

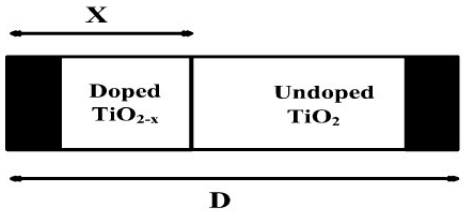


Figure 4: Hewlett Packward original device model

Figure 5: Equivalent circuit of memristor

The proposed structure is shown in Figure 4, and the equivalent electrical circuit of the memristor is shown in Figure 5. Time-dependent voltage and current can be expressed with equations (2), (3) and, (4) [29]:

$$v(t) = R(t) \cdot i(t) \tag{2}$$

$$R(t) = \frac{R_{on}w(t)}{D} + \frac{R_{off}(1 - w(t))}{D} \quad (3)$$

$$\frac{dw(t)}{dt} = \frac{\mu v R_{on}}{D} \cdot i(t) \quad (4)$$

where R_{on} is the resistance for $x(t) = D$, and R_{off} is the resistance for $x(t) = 0$; $x(t)$ is the state variable over $[0, D]$.

Memristors are characterized by relatively short switching time, high endurance and low switching energy (typically 0,1–1 PJ), so memristive technologies are basically studied for memory applications [30, 31, 32, 33].

The symbol of memristor is shown in Figure 6. When current flows into (out of) the black strip, memristance decreases (increases) [34]. However, plotting the current flowing in the memristor versus the voltage across it results in a hysteresis loop (Figure 7), which is always pinched at the origin.

2.3.2. *Physics Of Hysteresis Loop*

Sinusoidal current $i(t)$ can lead to hysteresis. In this case, maxima and minima are shifted with respect to the corresponding memristor voltage $v(t)$. When both $i(t)$ and $v(t)$ become simultaneously zero, pinching occurs. The memristor can reach a maximum value of Roff and a minimum value of R_{on}. The maximum resistance can be expressed by the amplitude of input parameters. Many research works [35, 36, 37, 38, 39] have used mathematical models of memristor but a nonlinear dopant drift memristor model has been used for simulation of the proposed circuits [29].

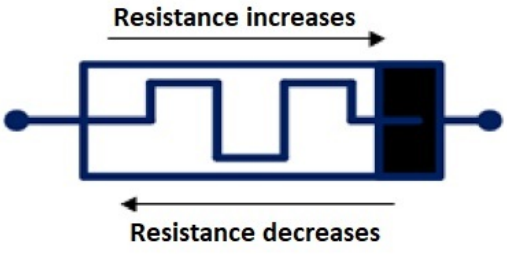


Figure 6: Symbol of memristor

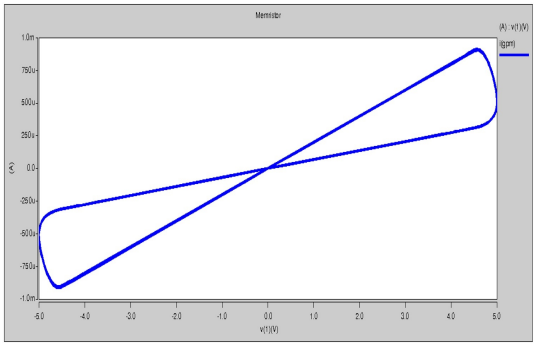


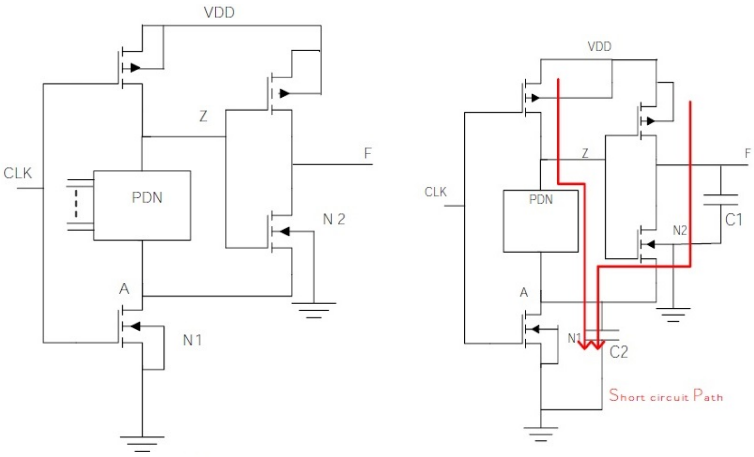
Figure 7: Hysteresis curve of memristor model (current–voltage pinched hysteresis loop)

2.4. *Pseudo Domino Circuit*

The pseudo domino logic outperforms domino logic because of precharge pulse propagation. A pseudo domino circuit [40] connects source node of the nMOS of the inverter to the drain terminal of the evaluation MOS at node A, instead of ground (Figure 8a). Thus, the value at node Z cannot propagate to the output node F in precharge phase, when the evaluation transistor N1 is off. This connection saves up to 32 % more power than conventional domino logic designs. This topology essentially improves the performance during the precharge phase. The pseudo domino logic circuit experience charge sharing and leakage issues because of short circuit paths. These issues can be resolved by using a keeper circuit.

The voltage drop at output node occurs because of charge sharing issue. In Figure 8b, when all inputs of pull-down network are equal to 1 in precharge phase, the threshold voltage drops at the output node Z. This voltage drop can be propagated to node F. The output voltage is redistributed on capacitances C1 and C2 as transistor N2 is ON. Therefore, the speed and power dissipation of the circuit are deteriorated, so a voltage drop occurs at output node F. If the value of output load capacitance C1 is equal to the node capacitance C2, then the voltage at output node reaches VDD/2.

Two methods can be used as solutions: 1) using a load capacitor with a capacitance much greater than any other charge sharing capacitance [40] and 2) using a keeper circuit [41]. Different keeper techniques are used in pseudo domino logic for power dissipation in this reference.



(a) Pseudo domino circuit (b) Charge sharing problem in pseudo domino circuit

Figure 8: Pseudo domino

3. Proposed preamplifier topology

A new method is proposed in this section to design a domino logic. The proposed domino logic circuit shown in Figure 9, has a higher speed than conventional domino logic circuits.

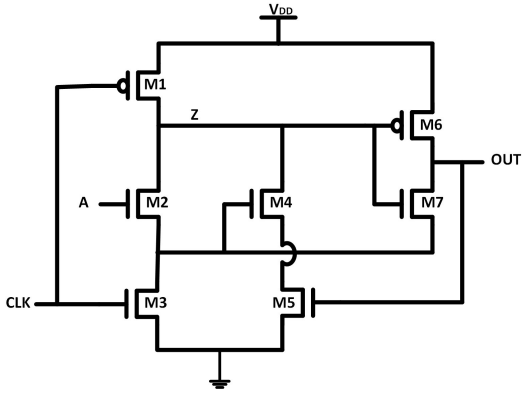


Figure 9: The proposed domino logic circuit

The circuit consists of two clock transistor elements. In this circuit, when the clock and A both are low, Z will be high and the output node will not change. The same is true when the clock is grounded and input A is high. When the clock and A both are high, both Z and the output will be high. When the clock is high and input A is low, Z will not change. In this condition, if Z is high (grounded), the output will be low (high).

Now, a full adder based on the novel domino logic circuit as well as MTJ and memristor components as shown in Figure 10. In the proposed circuit, MTJ components are used in the output inverter to improve the circuit performance to stay at stable values. Additionally, to reduce the delay due to the use of memory elements in these circuits, we use discharge transistors to remove the electric charge from the z-storage node. This reduces the power consumption and delays the main nodes.

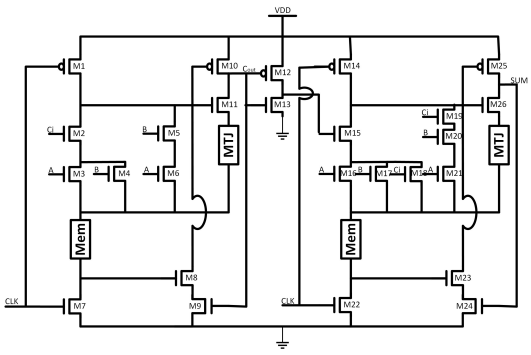


Figure 10: Schematic of the proposed final full adder based on MTJ and memristo

4. Simulation results

The simulation results of the proposed domino logic and full adder are presented in this section.

Figure 11 shows the simulation results of the proposed domino logic. The delay of this domino is plotted in Figure 12. As can be seen, the delay of this circuit is about 2 ns.

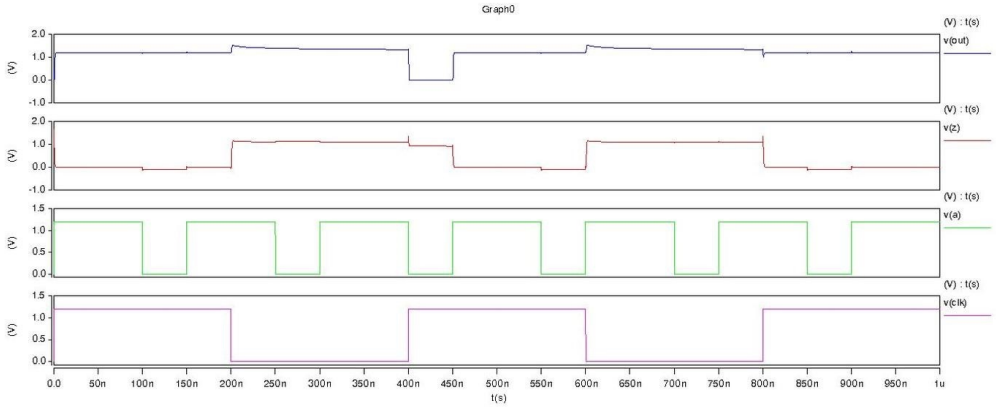


Figure 11: Simulation results of the proposed domino logic

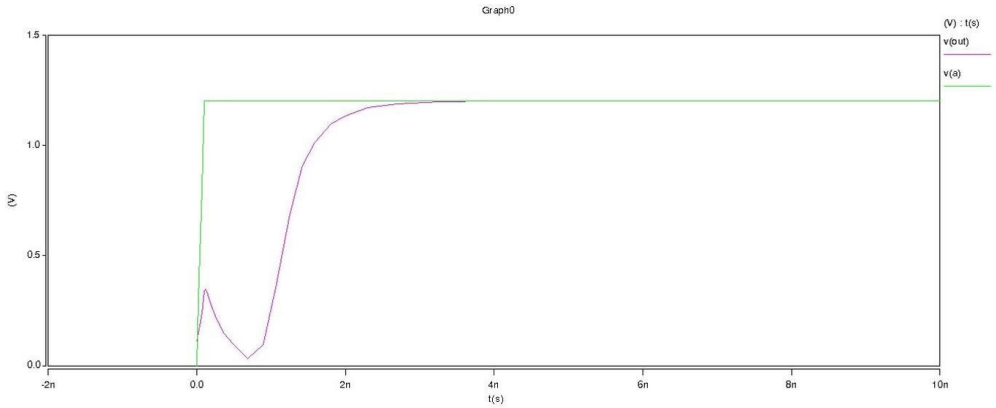


Figure 12: Delay of the proposed domino

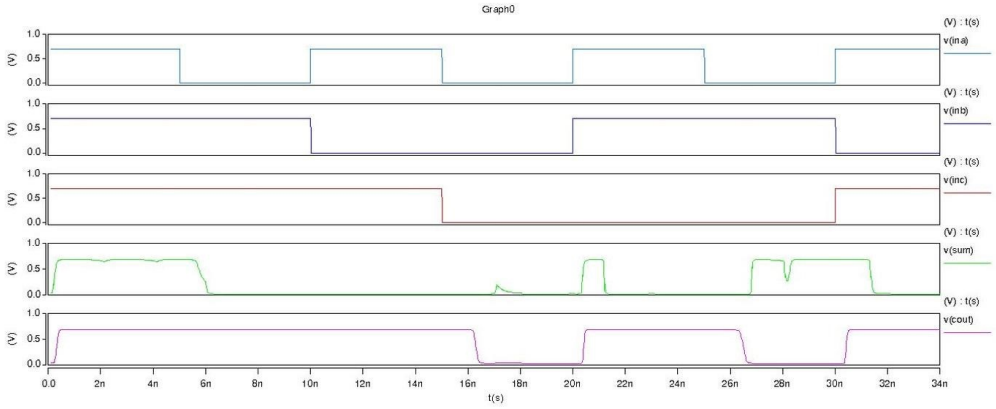


Figure 13: Simulation result of the proposed full adder based on memristor and MTJ

Figure 13 shows the simulation results of the proposed full adder based on memristor and MTJ. As can be seen, when all inputs are high, the sum of both outputs and *Cout* are high. When two inputs are high and the other input is low, one output is low and the other is high.

In Table 1, a comparison is made between the proposed full adder and those in other works.

To show the stability of the circuit against voltage fluctuations, the circuit output for different values of voltage is investigated. Figures 15, 16 and 17 show the circuit output for 0,5; 0,9 and 1,2V

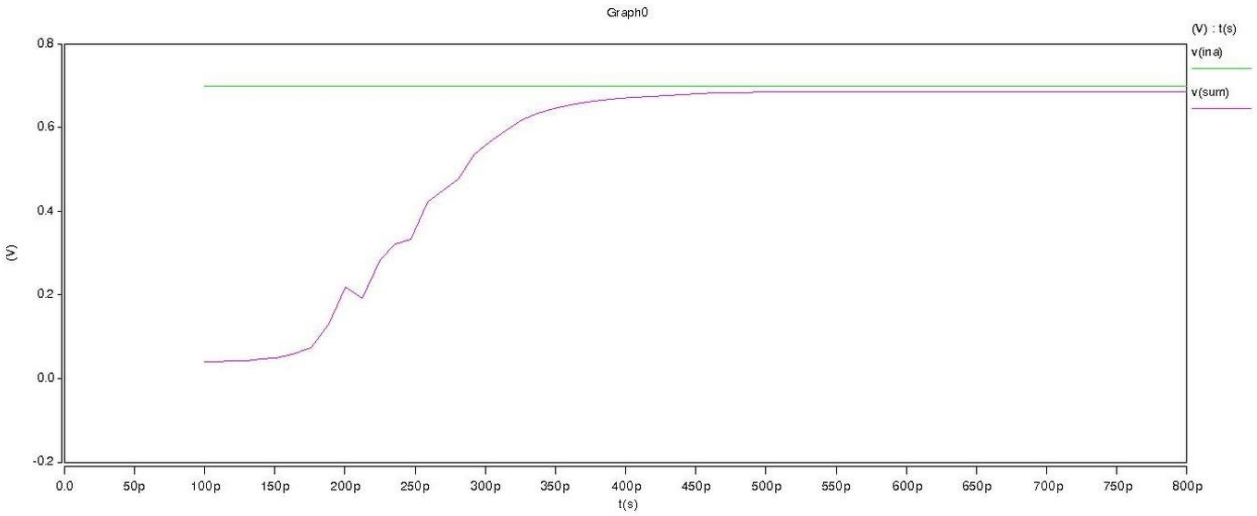


Figure 14: Delay of the proposed full adder

Table 1: Comparison of the proposed full adder and those in other references

Paper	Voltage supply (v)	Power consumption (μw)	Delay (ns)	Technology
5	0,9	0,12	1	32nm CMOS
6	2,5	0,447	0,35	180nm CMOS
43		1730	1,009	
44		5,736	0,179	
45		127	1,117	
This work (MTJ&MEM)	0,7	0,317	0,35	7nm CMOS

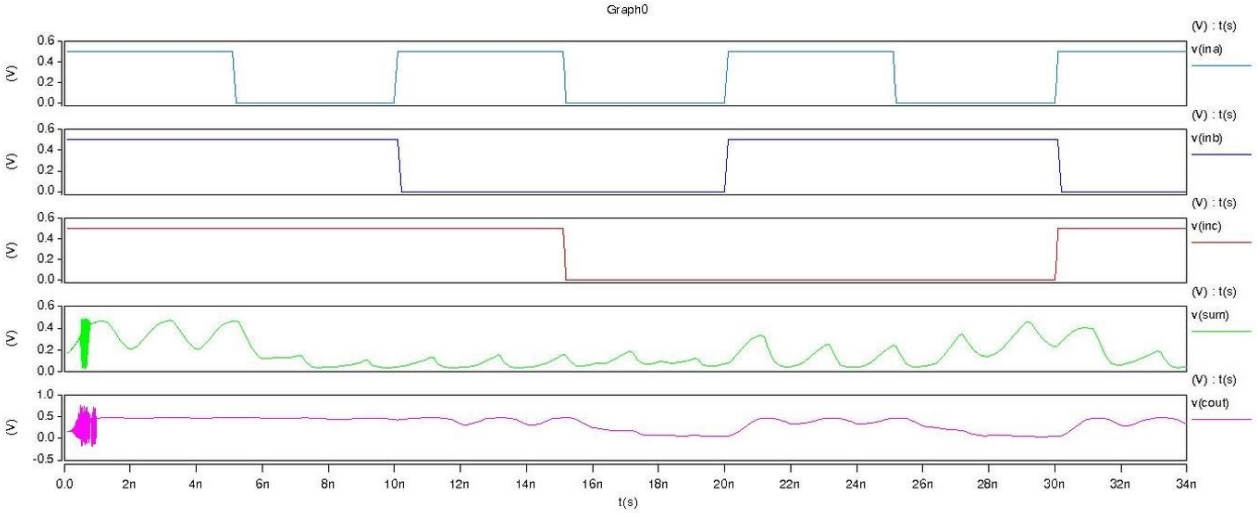


Figure 15: Simulation result of the proposed full adder for 0.5v

respectively.

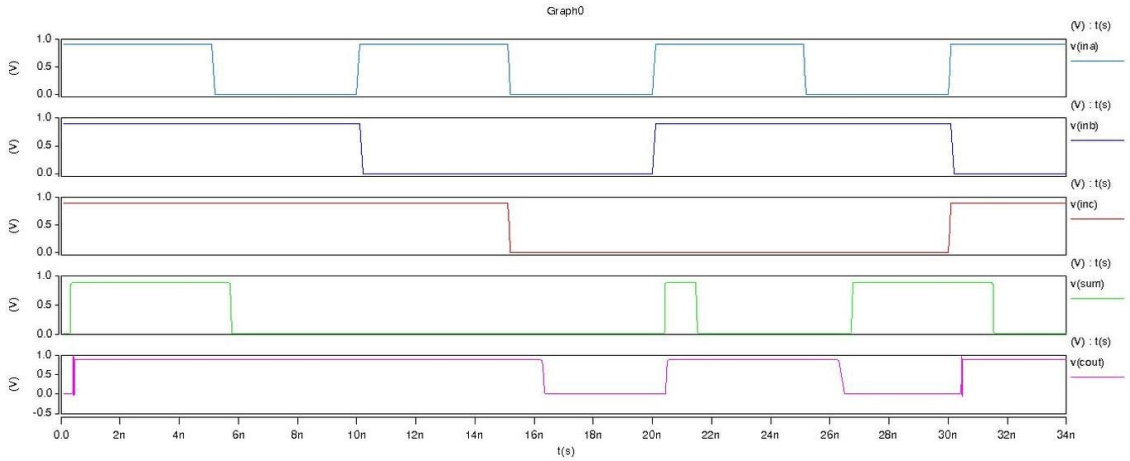


Figure 16: Simulation result of the proposed full adder for 0.9v

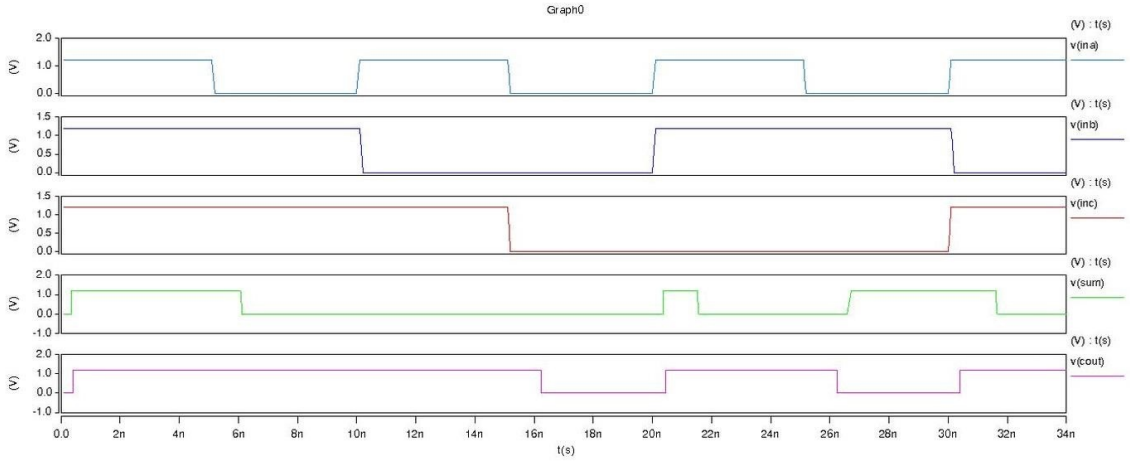


Figure 17: . Simulation result of the proposed full adder for 1.2v

5. Conclusion

A new low-power high-speed full adder circuit, which uses a new CMOS domino logic family, was presented in this paper. A new structure for adiabatic hybrid MTJ and MEM-CMOS circuits was also presented in this work. Moreover, the proposed full adder was compared with other previously presented basic logic gates and full adders. The advantages of the proposed circuits were their simpler architecture, lower power consumption, higher speed and using fewer transistors. The designs were simulated and compared with several state-of-the-art designs. We used Synopsys HSPICE simulator with 7 nm technology files to test the presented designs. The results showed the lower power consumption of the proposed adiabatic MTJ-CMOS designs compared to state-of-the-art designs. In the final full adder circuit, sustainable outputs with optimal power consumption were achieved for hybrid structure of memristor and MTJ. Accordingly, the results of outputs indicated the feasibility of an optimal full adder design.

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