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NOVEL CONTROL STRATEGIES FOR SHIPBOARD POWER CONVERSION SYSTEMS TO MEET THE PULSED LOAD REQUIREMENTS IN MIL-STD-1399

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THESIS

NOVEL CONTROL STRATEGIES FOR SHIPBOARD POWER CONVERSION SYSTEMS TO MEET THE PULSED LOAD REQUIREMENTS IN MIL-STD-1399

by

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13. ABSTRACT (maximum 200 words)

Large, immediate changes in electrical loading cause stresses in power systems. In large power systems, such as the grid used in residential, commercial and industrial applications, the typical change in electrical loading is a very small percentage of the power ratings of the electrical generators. As such, abrupt changes in electrical loading will cause relatively little stress to the power system. In naval applications, however, the distribution systems have a much lower power rating, so the stresses from load changes are much more significant. This thesis presents a novel solution to reduce the undesired effects of these load changes. Through the use of an energy storage system (ESS), switch-mode DC power converter, and an engineered control scheme, the undesired effects of large pulsed loads may be mitigated.

A physics-based model of the system was constructed to provide a proof of concept of the solution, and is verified utilizing a laboratory prototype. The simulated and experimental measurements are compared against the specified constraints provided in MIL-STD-1399.

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List of Acronyms and Abbreviations

AC	alternating current
ACM	average current mode
CCM	continuous conduction mode
DC	direct current
DCM	discontinuous conduction mode
DOD	Department of Defense
DON	Department of the Navy
ESS	energy storage system
FET	field-effect transistor
FPGA	field programmable gate array
HDL	hardware description language
KCL	Kirchoff's current law
MASINT	measurement and signature intelligence
NPS	Naval Postgraduate School
PCM	peak current mode
PDM	pulse density modulation
PI	proportional integral
PLL	phase locked loop
PWM	pulse width modulation

RMS	root mean square
SRWBR	short range wide band radio
TCP	Transmission Control Protocol
USN	U.S. Navy
VSI	voltage source inverter

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CHAPTER 1:
Introduction

1.1 Research Motivation

Every warship in the United States Navy must be capable of generating and distributing its own power to meet various objectives. The power distribution system on a ship is much smaller than the electrical grid in our daily lives, and the two are not connected when a warship is underway completing mission objectives. Because the power generation and distribution system on a warship pales in comparison to the capacity of residential grids, electrical disturbances have a much larger effect on the system stability and electrical power quality. This comes about because the prime movers of the generating station have significantly less inertia than those found in commercial generating stations [1].

The power quality of the electrical system on a ship is not only challenged by the relatively small scale of the warship, but also by the evolution of the operating environment [2]. More sophisticated weapon systems, such as the SPY-6 radar or directed high-energy weapon systems, are needed to maintain maritime dominance in the modern era [3]. These sophisticated weapon systems come at a price of requiring ever-increasing electrical power, and stricter power-over-time requirements. To maintain the power and distribution system within specifications, additional systems or components must be installed or implemented on the warship [4].

1.2 Previous Research

A solution to the pulsed load problem was proposed in [5] to reduce the unwanted effects of large sudden changes in electrical loading. In [5], the load change was implemented on the alternating current (AC) bus. The work was expanded in [6] and is further expanded in this thesis. Both [6] and this thesis examine pulsed load requirements with the pulsed load connected to the direct current (DC) bus. This gives the designer greater control by adding a voltage source inverter (VSI). More research is ongoing concerning the control strategy of the VSI to reduce other electronic undesired effects [7].

1.3 Research Goals

High-power, short-duration electrical loads are becoming increasingly necessary to execute the objectives of the Department of the Navy (DON). The stresses the pulsed loads create must be accounted for to ensure proper operation of the power generation and distribution system, and to ensure the load itself functions properly.

The goal of this thesis is to expand the work listed in the previous section by exploring one option for utilizing an energy storage system (ESS) to reduce the transients due to these abrupt pulsed loads to meet the limits specified by MIL-STD-1399 [8].

Additionally, this thesis aims to explore the use of average current mode (ACM) control of a bi-directional DC converter. The converter control scheme must maintain the DC bus within specification during a pulsed load transient. This will allow us to verify that the pulsed load limits of [8] are met in our simulations and experiments.

1.4 Thesis Structure

This thesis is constructed to allow the reader to understand the pulsed load specifications of [8], including what it states, why it is important to the fleet, and what needs to be added to a power system to meet these specifications. Chapter 2 presents the background knowledge required to understand power converters and control strategies. Chapter 3 presents the architecture used for the simulations and experiments, as well as the key design parameters required to meet the pulsed load specifications. Chapter 4 presents the specific control strategy utilized in this research. Chapter 5 presents the physics-based models and the simulations used for power flow modeling. Chapter 6 presents results of the laboratory hardware implementation, and Chapter 7 concludes the thesis with recommendations for future work.

CHAPTER 2:
Background

In this chapter, general concepts beneficial to understanding the proposed architecture and control scheme are reviewed. This is not intended to be an exhaustive set of information on any of the topics included, but rather a basic overview of topics used in our explanations.

2.1 DC-DC Converters

DC converters are devices used to transform DC electricity from one voltage to another [9]. This thesis focuses on the use of switch-mode DC-DC converters. Buck, boost, and bi-directional boost topologies will be reviewed in this section. At the core of a switch-mode DC-DC converter is one or more transistors that are switched on or off. Over a single switching period, T_s, the transistor is switched on for a time T_{on}, and is switched off for a time T_{off} according to the following equation:

$$T_s = T_{on} + T_{off}. \tag{2.1}$$

A key parameter in the design and control of a DC-DC converter is the duty cycle for the transistor (D), which is determined by:

$$D = \frac{T_{on}}{T_s} \tag{2.2}$$

where the switching period is generally held constant [9]. To determine the state of the transistor, a reference signal is compared to a repetitive waveform or "carrier" as shown in Figure 2.1, where the carrier is a sawtooth waveform. When the amplitude of the reference exceeds the amplitude of the carrier, the gate signal for the transistor is driven high, and vice versa. If the carrier wave is linear and has an amplitude of one, as shown in Figure 2.1, then the value of the reference signal is equivalent to the duty cycle (D) for the transistor. By varying D, the width of the pulse is altered. This control strategy is termed pulse width

modulation (PWM).

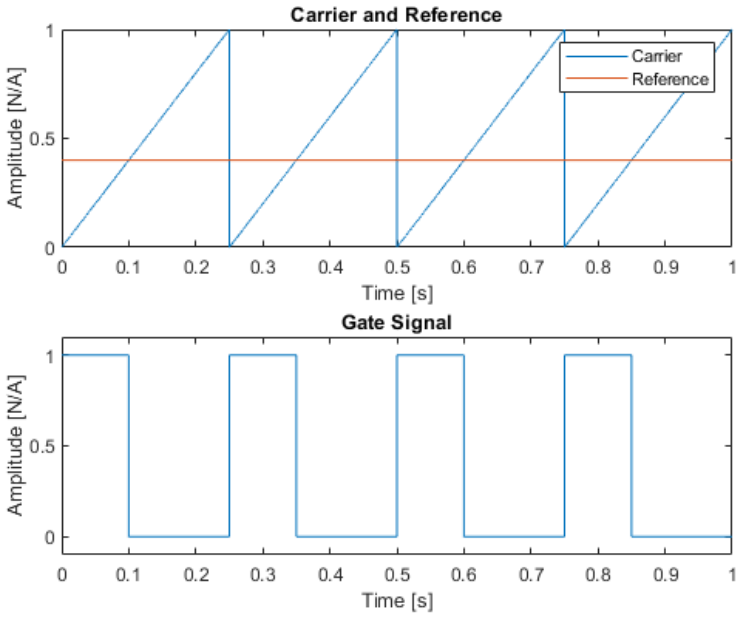


Figure 2.1. Duty Cycle Generation

2.1.1 Topologies

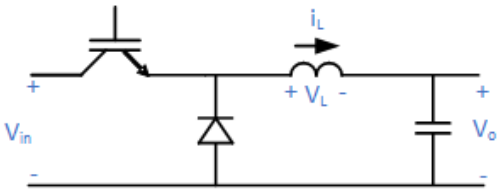
The circuit schematic of a typical buck converter is shown in Figure 2.2(a). In this converter, when the transistor is conducting, the inductor charges while supplying current to the load. When the transistor is not conducting, the inductor and capacitor discharge through the diode to supply power to the load. If the inductor discharges the entirety of its energy during this off time, the load current also dissipates to zero, and the buck converter is said to be in discontinuous conduction mode (DCM). If the inductor maintains some energy through the entire off cycle, then the load continuously draws current and the buck converter is said to be in continuous conduction mode (CCM). Overall, in CCM, the steady state average output voltage is dictated by the equation

$$V_o = V_i \cdot D \tag{2.3}$$

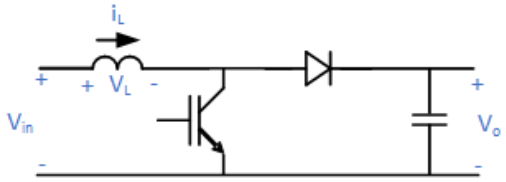
If the goal of the DC-DC conversion is to step up the output DC voltage with respect to the input voltage, a boost converter is used. The schematic of a boost converter is shown in Figure 2.2(b). In this topology, when the transistor is conducting current, the inductor is charging. The diode is open circuit, which means the capacitor must discharge to supply the load. When the transistor is not conducting, the inductor discharges through the diode to supply the load. The inductor also charges the capacitor during this time. The relationship between input voltage and output voltage in steady state and CCM becomes

$$V_o = \frac{V_i}{1 - D} \tag{2.4}$$

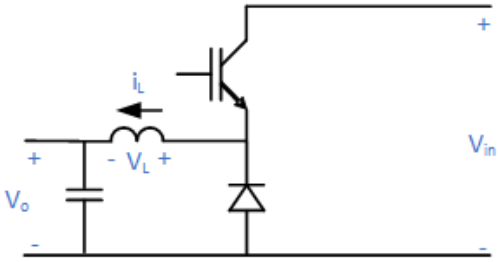
Each of the converters described above is uni-directional, that is, power only flows in one direction. If it is needed for power transfer to occur in both directions (to charge and discharge a battery, for example), then another DC-DC converter topology must be used. Here we analyze a bi-directional boost topology [10]. If the schematics shown in Figures 2.2(a) and 2.2(b) are rearranged, they look like those depicted in Figures 2.2(c) and 2.2(d) respectively. Notice now that the input is on the right-hand side for the buck converter. It is still uni-directional, but power can flow from right to left in this topology. In Figure 2.2(e), the two are combined to provide the bi-directional boost topology. As the converter is bi-directional, there is not a single input and a single output. Instead, there is a high-voltage side and a low-voltage side. The transistor being switched is determined by the direction of the desired power flow. Of note, a bi-directional buck converter has the same layout, but would have the low-voltage side on the right and high-voltage side on the left. The more commonly discussed buck-boost converter does not have a high- or low-voltage side, as it is free to increase or decrease the voltage based on the duty cycle. Since we utilize a bi-directional boost converter in this paper, it is the only one of the three included in Figure 2.2(e).



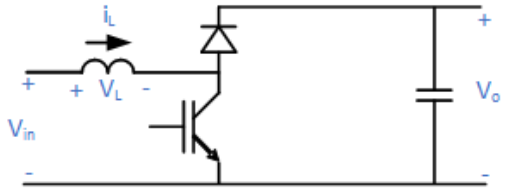
(a) Buck Converter



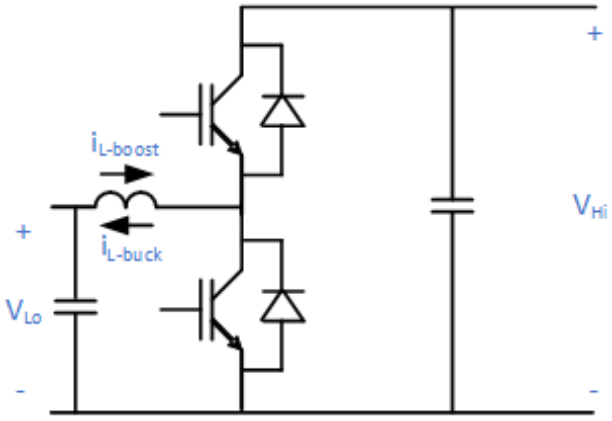
(b) Boost Converter



(c) Buck Converter Rearranged



(d) Boost Converter Rearranged



(e) Bi-directional Boost Converter

Figure 2.2. Buck, Boost, and Bi-directional Boost Topologies

2.1.2 Power Converter Control Systems

Switch-mode power converters require closed-loop control systems to deliver the desired output voltage. Consider the block diagram depicted in Figure 2.3 where a controller is used to ensure the measurement from the plant is matched exactly to the command input.

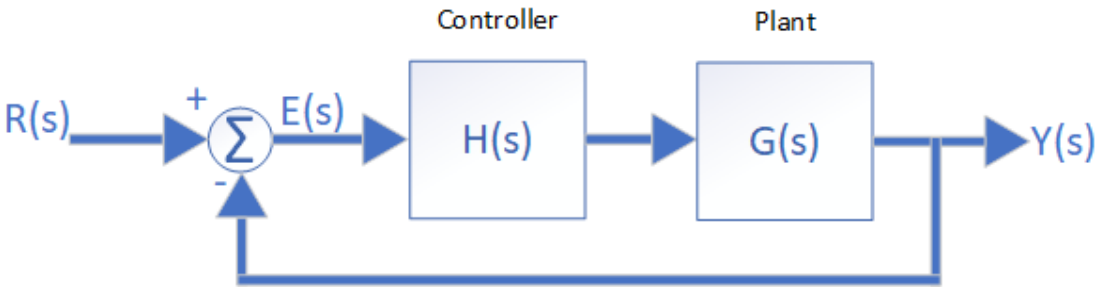


Figure 2.3. Closed Loop Control Block Diagram.

When the measurement and the command are matched, the error $E(s)$ is zero. By utilizing a proportional integral (PI) controller, we can ensure the error is driven to zero. The transfer function of a PI controller in the s-domain is

$$H(s) = K_p + \frac{K_i}{s} \tag{2.5}$$

where K_p is the proportional gain and K_i is the integral gain. The closed-loop transfer function from input $R(s)$ to measurement $Y(s)$ is given by the equation

$$G_{CL} = \frac{Y(s)}{R(s)} = \frac{GH}{1+GH} \tag{2.6}$$

and the transfer function from input $R(s)$ to the error $E(s)$ is given by

$$\frac{E(s)}{R(s)} = \frac{1}{1+GH} \tag{2.7}$$

If we utilize a plant whose impulse response contains no zeros and no poles, we can treat $G(s)$ as a constant. By substituting (2.5) into (2.7), we come up with the result

$$\frac{E(s)}{R(s)} = \frac{1}{1+GH} = \frac{1}{1+(K_p + \frac{K_i}{s})G} = \frac{s}{s(1+GK_p)+GK_i} \tag{2.8}$$

The response of the error to a step input is obtained by setting the input $G(s)$ equal to the frequency response of the step function, which is $\frac{1}{s}$. The final value theorem is then used to obtain the following:

$$\lim_{t->inf} e(t) = \lim_{s->0} sE(s) = \lim_{s->0}(s)\left(\frac{1}{s}\right)\left(\frac{s}{s(1+GK_p)+GK_i}\right) = 0 \tag{2.9}$$

Furthermore, we gain insight to the response of the system by analyzing the denominator, also known as the characteristic equation, of the transfer function. The roots of the characteristic equation are the poles of the system. In equation 2.9 the poles are calculated to be:

$$\begin{aligned} s(1+GK_p)+GK_i &= 0 \\ \therefore\ s &= \frac{-GK_i}{1+GK_p} \end{aligned} \tag{2.10}$$

The speed of convergence is controlled by the placement of the pole on the real axis, and the oscillatory nature is described by the imaginary component. Since there is only one root in this equation, no oscillations will be realized; Only the speed of convergence is controlled in this instance.

2.1.3 Average vs Peak Current Mode Control

There are several techniques to control the switching action of the DC-DC converter. One common method of control for DC-DC converters is current mode control [9], [11], [12]. Two popular current mode control methods are ACM and peak current mode (PCM) control. In either scheme, it is common to design the controller using an inner loop and outer loop structure [9], [11], as can be seen in Figure 2.4. The outer controller compares the measured DC bus voltage to a reference value and ensures the difference is driven to zero, as described in Section 2.1.2. The output of the outer loop controller is a reference current which is used

as the input to the inner loop controller. This reference current is compared to the measured current, as described in Section 2.1, and the comparison is then used to control the duty cycle of the converter. If the measured current in the converter matches the commanded output of the outer loop controller, then the voltage error will converge to zero.

Current mode control differs from the PWM technique described in Section 2.1. The duty cycle D is not strictly set by the controller to obtain a percentage of the pulse width in which the transistor is conducting. Instead, the current is measured and compared against the carrier waveform after being transformed by a transfer function.

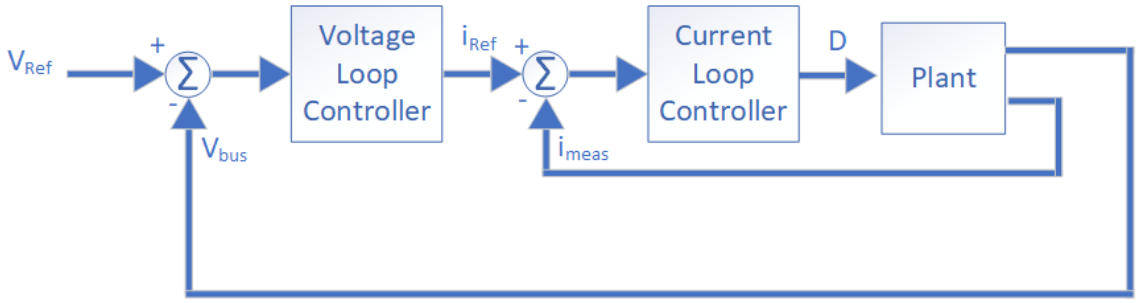


Figure 2.4. Current Control with Outer Voltage Loop

In the peak current mode control method, the current reference produced by the outer loop voltage controller is set to the desired maximum current of the converter. The control diagram in Figure 2.5 shows a flip flop which is set using a clock signal. This will ensure that at the start of each switching cycle the transistor of the converter will be conducting. Because the transistor is conducting, the current of the converter will increase. When the measured current meets the commanded peak current value, the transistor turns off, which causes the measured current to decrease. The system remains in this state through the remainder of the switch cycle. At the start of the following switch cycle the flip flop is again set by the clock, and the measured current begins to rise. Peak current mode control is entirely counter to what is depicted in Section 2.1 because the sawtooth carrier waveform is not applied to the comparator; its only function is to reset the transistor. The carrier waveform is set to the desired peak value of current which is one input to the comparator.

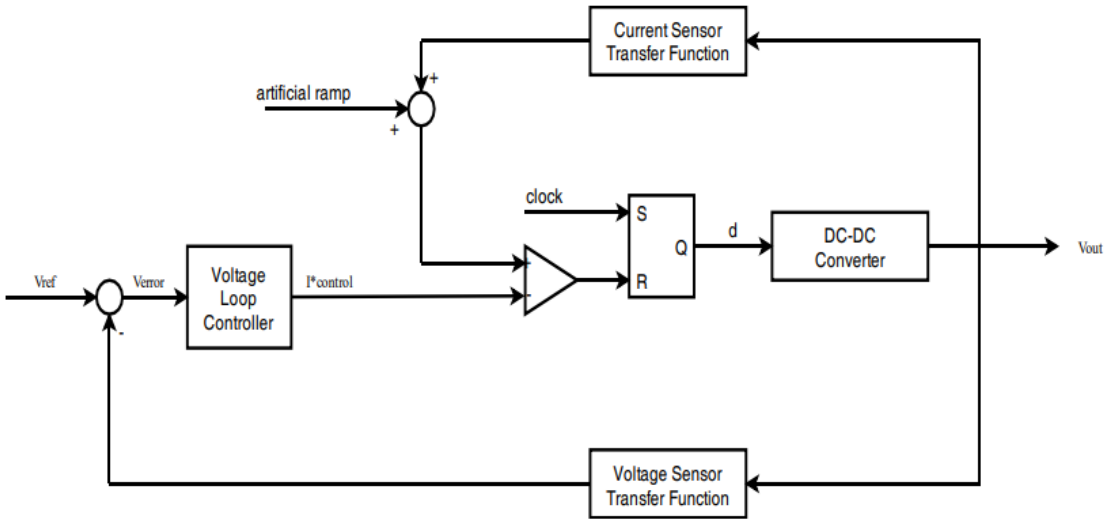


Figure 2.5. Peak Current Control Block Diagram. Source: [13]

Peak current mode control is reliable and easy to implement, but does contain a few key disadvantages. In a digital implementation, the current must be sampled at discrete intervals. If the sampling rate is too low, the actual current value may exceed the commanded maximum for a period of time until the next sample is taken. Another disadvantage is the presence of noise. When the transistor changes state, the transient current often oscillates around the new steady state value. These oscillations may overshoot the commanded peak current and force the transistor off immediately. Further, if the slope of the measured current is low, noise can cause the flip flop to reset prematurely. Any of these events will cause the converter to operate differently than it was intended by the designer.

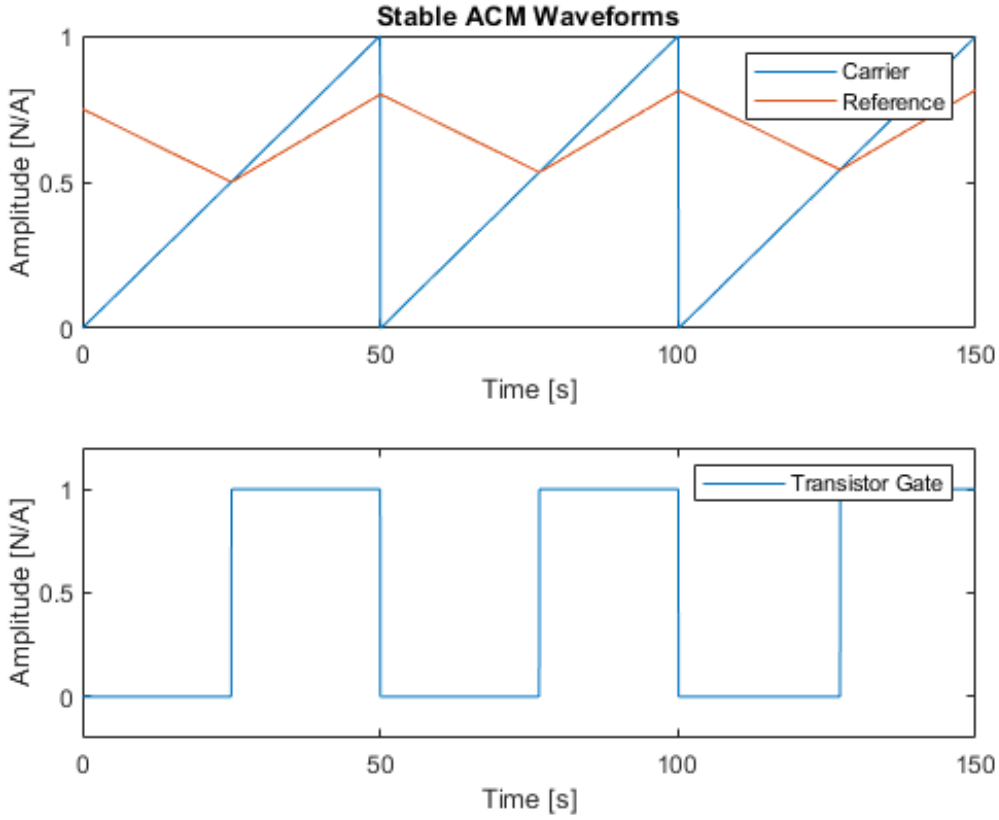


Figure 2.6. ACM Controller Comparator Inputs

Average current mode control is similar to peak current mode control in that a current waveform is compared against the carrier waveform. In this mode of control, however, the average current is compared against the carrier waveform, not the peak current. A flip flop is not necessary to reset the transistor at each clock cycle. By analyzing the comparator inputs plotted in Figure 2.6, we notice a few elements that must be true for average current mode control to work effectively. First, when the saw-tooth carrier waveform resets to zero, the reference waveform must be decreasing as the carrier waveform increases. By designing the system in this manner, the two waveforms will intersect in the clock cycle. Once the two waveforms intersect, the transistor will change state, and the measured current slope will change direction. Until the end of the clock cycle, the reference and carrier waveforms will trend in the same direction, which poses a limitation on the controller design. Consider

the comparator input waveforms depicted in Figure 2.7. After the carrier waveform and reference waveform intersect, the transistor changes state. In this example, the gains of the controller are set such that the slope of the reference waveform exceeds that of the carrier. This forces the reference waveform to rise over the carrier, and the transistor will change state another time during a single switching cycle. The system has become unstable as the transistor now switches at frequencies higher than the engineered switching frequency. To avoid this, the gains must be set so that the reference waveform does not rise faster than the carrier waveform.

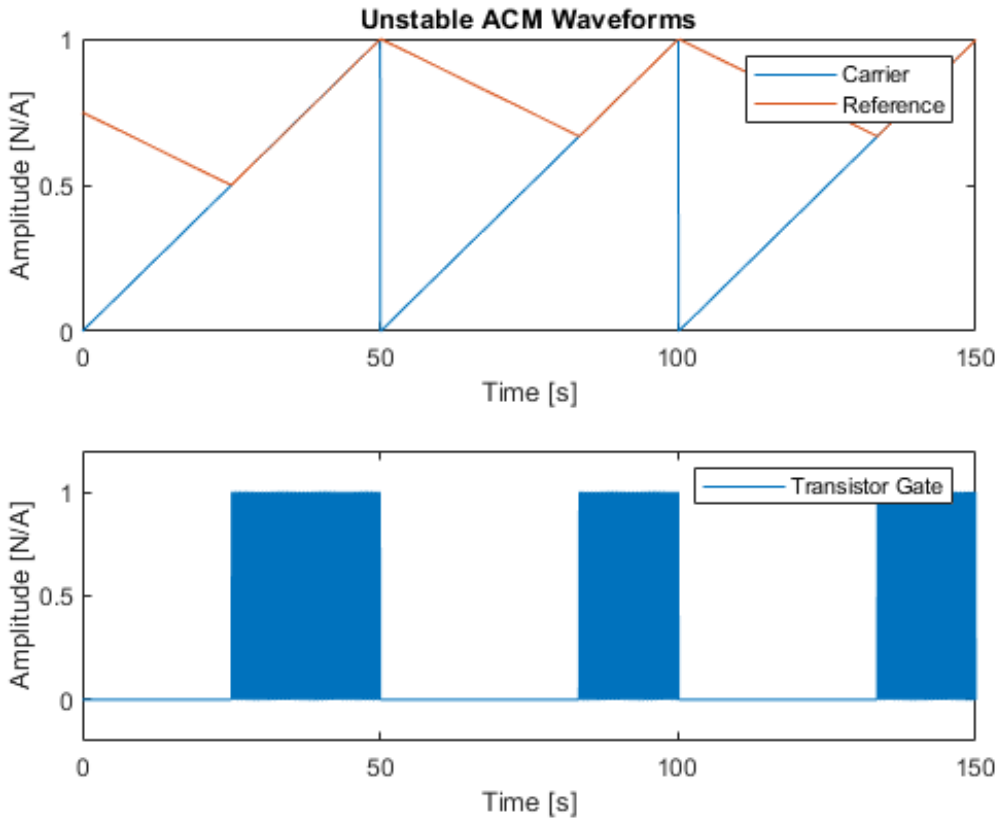


Figure 2.7. Unstable ACM Controller Comparator Inputs

In summary, the pros and cons between average current mode control and peak current mode control are given in Table 2.1 [11], [12].

Table 2.1. Average Current Mode Control vs. Peak Current Mode Control

Pros vs Cons between ACM and PCM	
Pros PCM	**Cons PCM**
The transistor is inherently protected from overcurrent	Poor noise immunity
Voltage regulators are easily applied to the controller	Slope compensation may be required
	Peak current is only inherently limited for the transistor
Pros ACM	**Cons ACM**
No flip flop is required	Gains must be set to prevent instability
High resistance to noise	Gain restrictions become very strict in DCM
Slope compensation is not required	Additional circuitry is required to obtain average current
Capable of controlling any current in the circuit, not just inductor current	

2.2 Voltage Source Inverters

A VSI is a power converter capable of converting AC to DC, or DC to AC. When converting from AC to DC, the process is known as rectification. When converting from DC to AC, the process is known as inversion. A schematic of one such topology can be seen in Figure 2.8. The inverter voltages can be controlled to adjust the real and/or reactive power flow between the AC and DC distribution systems. In essence, each of the inverter legs is an individual bi-directional boost converter, which is used to control the relationship between the DC voltage and the phase voltage at the leg. By using a sinusoidal reference waveform, the output voltage is also sinusoidal. And since both phase and magnitude of the reference waveform can be controlled, both real and reactive power flow of the inverter can be controlled.

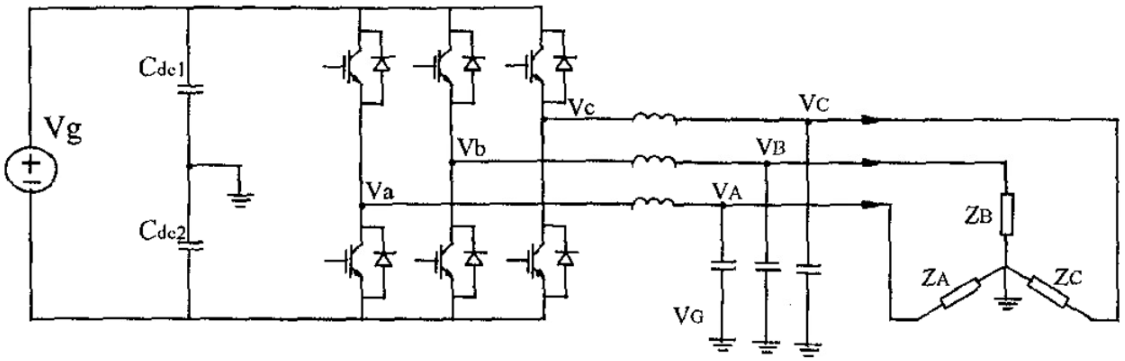


Figure 2.8. Three Phase Voltage Source Inverter. Source: [14]

2.2.1 Four-Leg Three-Phase Inverters

A schematic of a four-leg three-phase inverter is shown in Figure 2.9. The inverter utilized in this paper is a four-leg three-phase inverter, and is selected for use based on its common mode voltage elimination ability [15], which is covered extensively in [7]. The benefit to eliminating the common mode voltage is a substantial reduction in the size of inductive filter needed to suppress the common mode voltage [16], [15], which has a fundamental frequency in excess of 100 kHz. This high frequency voltage causes undesirable current to flow to the equipment casing.

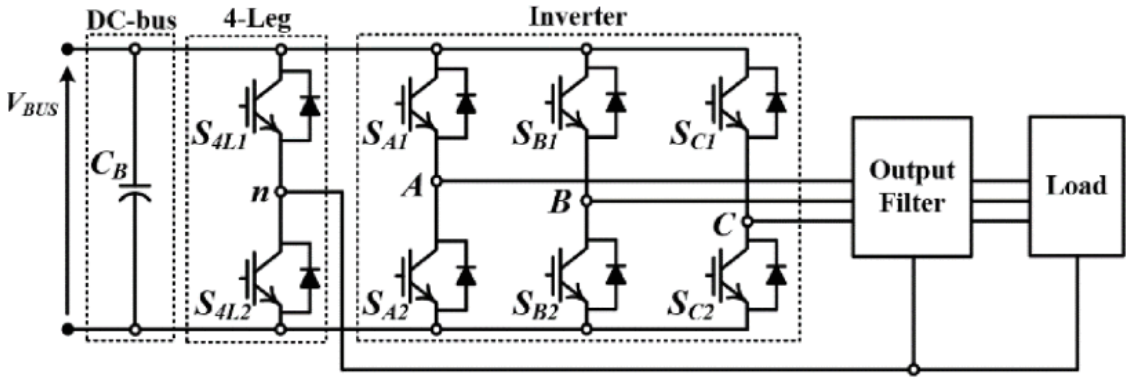


Figure 2.9. Four-Leg Three-Phase Inverter Schematic. Source: [17]

Either a three-leg or a four-leg VSI can be used in the circuit. The VSI can be connected to an existing grid, or can be used to form a standalone grid. If the VSI is controlling current flow into or out of the AC side, then it is said to be in grid-following mode. Since the VSI is regulating current flow and not bus voltage, there must be another device regulating the AC bus voltage. On the other hand, if the VSI is used to generate an AC voltage to which other devices can connect and draw current from, then the VSI is said to be operating in grid-forming mode [18], [19].

2.3 MIL-STD-1399-300-1 Requirements

MIL-STD-1399 is the reference document which "...defines the standard interface requirements for and the constraints on the design of shipboard user equipment that will utilize shipboard AC low voltage electric power" [8]. Pulsed power requirements are contained in Section 5.2.8. The reason these requirements are laid out is to ensure appropriate power stability and prime mover operation under conditions where the magnitude of the load changes substantially, and possibly frequently. Reference [8] provides for two separate types of pulsed power: infrequent and repetitive. Infrequent events are those occurring no more than once every two minutes. Loads that fall into this category could be charging electromechanical prime movers, like those which were found in the railgun, or potentially directed high energy weapons systems, depending on the desired firing rate of the system. This thesis focuses on the repetitive loads, which could also contain directed high energy weapons systems. However, it is more aptly characterized by radar and sonar systems, such as the AN/SPY-6 radar developed by Raytheon, which is currently being installed on surface ships.

The repetitive pulsed load requirement, summarized briefly, is that power supplied by the service system shall not deviate by more than 50 kW over a 1 second integration period. The integration period thus begins 500 ms in the past, and extends to 500 ms in the future. This rolling integration occurs over the entire duration examined by the test. The example provided in [8] is also shown in Figure 2.10.

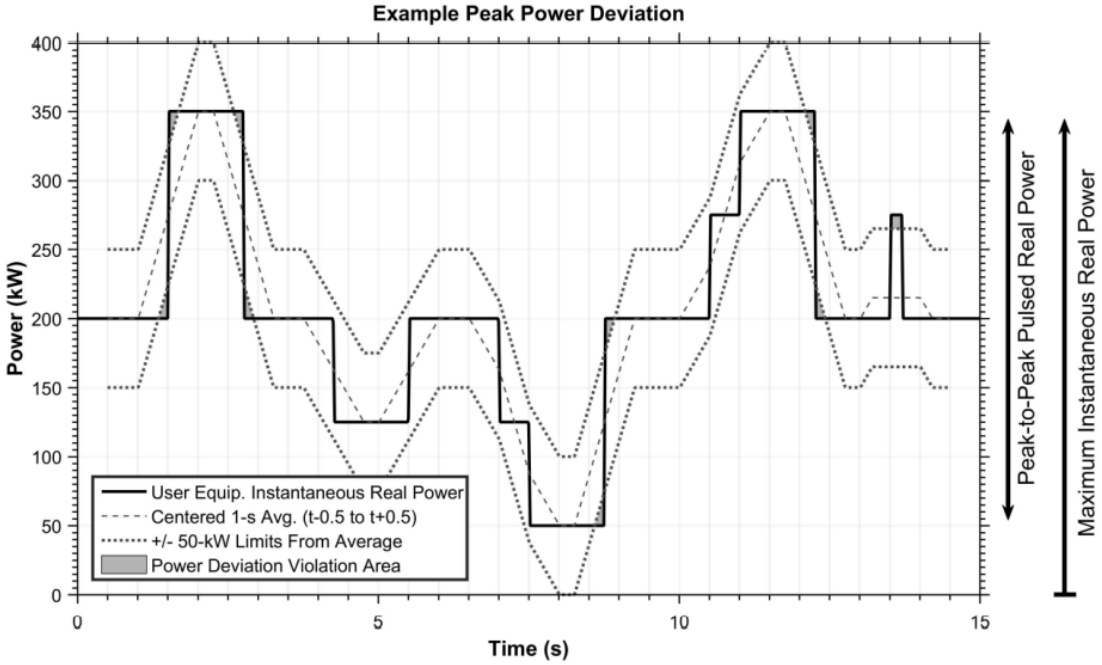


Figure 2.10. Pulsed Power Waveform and Deviation Example. Source: [8]

Violations are highlighted in gray, and depict periods of time where the pulsed power changes exceed the allowable limits. There are many ways to smooth out the power response of the AC distribution system to meet these limits. For example, resistive contacts could be closed in sequence to bring the output power of the generator up, thus raising the integration output and raising the allowable limit for the pulsed power to acceptable levels. To power the load, the resistive contact would open simultaneously with the load contact shutting. The reverse would be true for turning off the load. An example of this type of fix is shown in Figure 2.11, where the limit violations are shaded in red. The same pulse is again demanded a short time later, but another, smaller, load is commanded right before and right after the pulse. No violations are noticed under these conditions. This crude example shows how stepping the output power in stages could bring the system into limits, but comes at a cost of increased complexity and lower efficiency due to power dissipating through a resistive load. This thesis aims to analyze a more sophisticated solution to this problem.

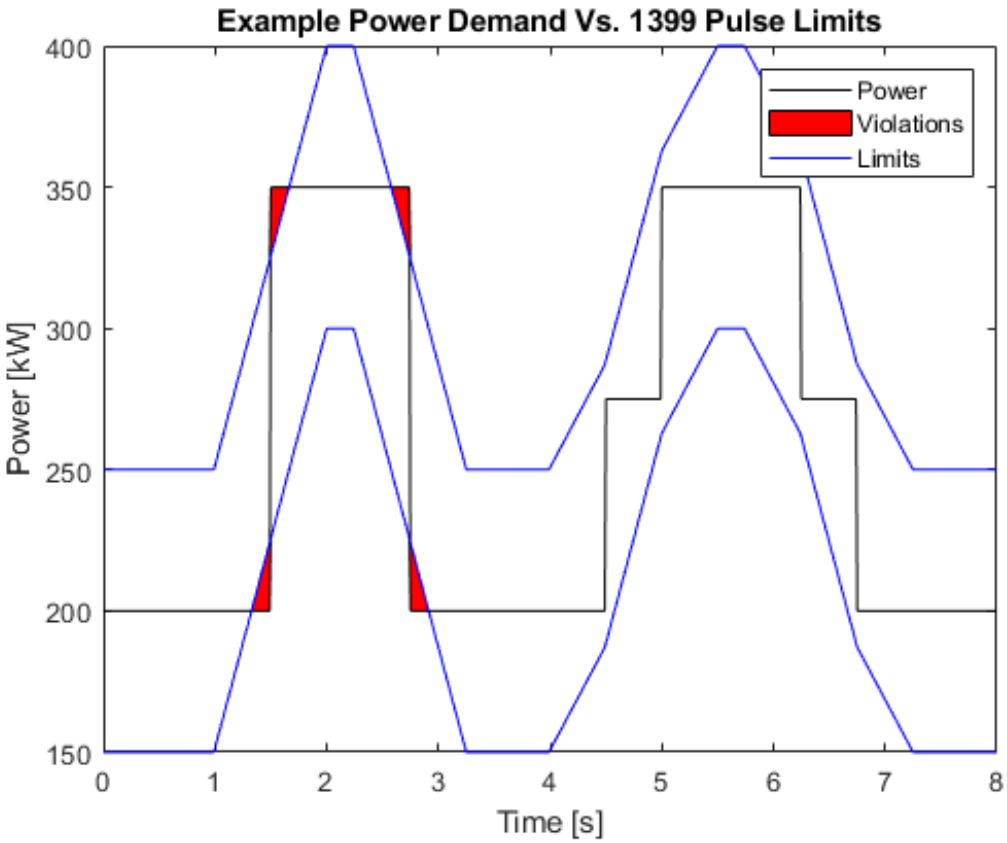


Figure 2.11. Power Limit Violation and Simple Fix

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CHAPTER 3:
Power Conversion System Architecture

In this chapter we analyze power flow between an ESS, an AC grid, and a pulsed load. The control of power flow is the key to meeting the pulsed load specifications in [8].

3.1 Overview

A schematic diagram of the system under investigation is depicted in Figure 3.1 and it is comprised of an ESS, a DC-DC converter, a DC bus, a grid-following VSI, an AC bus, and an AC power supply. The grid-following VSI is used to control power flow between the AC bus and the DC bus. The DC-DC converter is used to exchange power between the ESS and the DC bus, and it is responsible for maintaining DC bus voltage within specification. This thesis explores the use of ACM control of the DC-DC converter to manage the power exchange into and out of the DC bus in response to a change in load that would otherwise cause the power drawn from the grid to violate the specifications of [8] as outlined in Section 2.3.

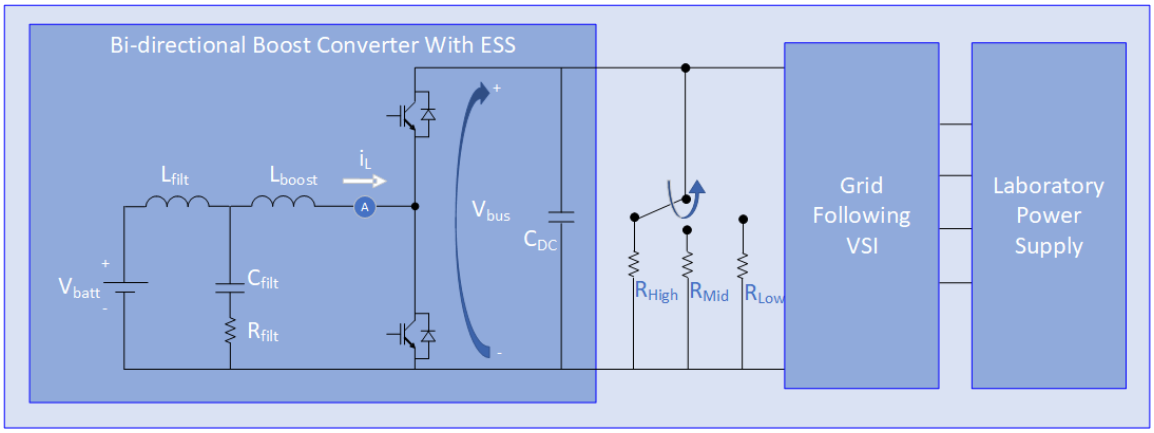


Figure 3.1. Top Level Schematic of Proposed System.

3.2 Energy Exchange

The central node for energy exchange in this system is the DC bus, which can receive energy from either the ESS or the grid-following VSI, and deliver energy to either the DC load or the ESS. When the DC load increases, the power delivered initially comes from the capacitor (C_{DC}). As the capacitor discharges, the voltage on the DC bus decreases. The ESS will then deliver more energy to the DC bus to increase voltage back to the commanded value. The ESS is a temporary source of power not meant to maintain prolonged power delivery. The grid-following VSI is designed to increase power delivery to the DC bus, thereby powering the load. Figure 3.2 depicts this energy exchange.

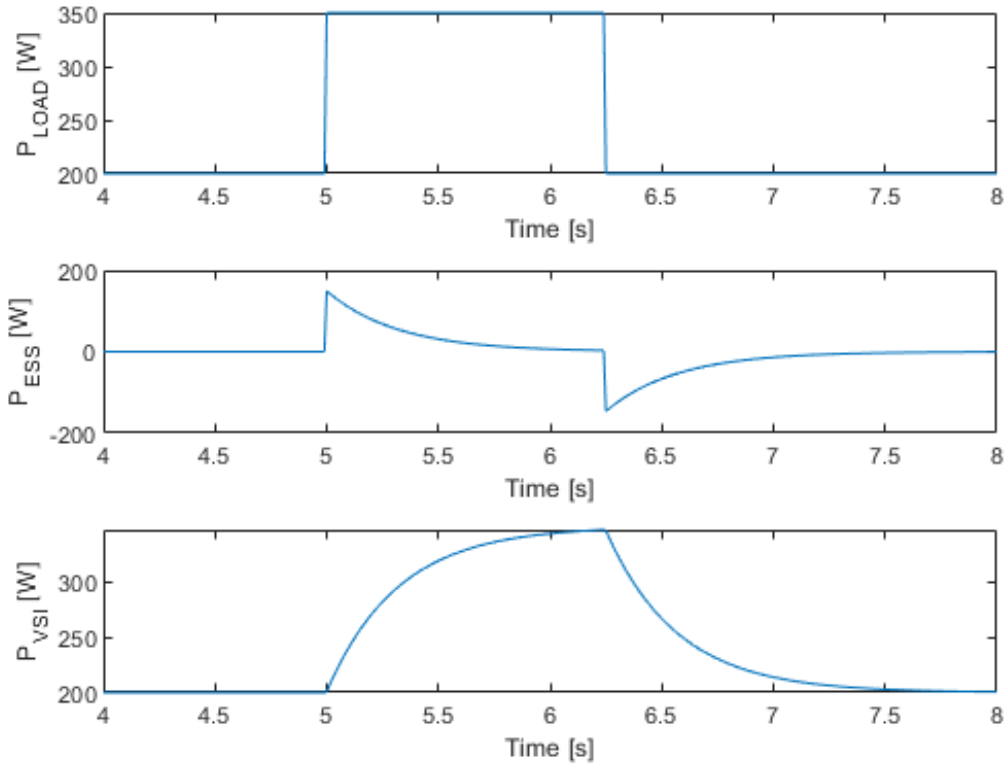


Figure 3.2. Energy Exchange Between Load and Sources.

By controlling the power delivery of the grid-following VSI, the change in power from the AC bus is controlled. The pulsed power limits described in Section 2.3 can therefore be met. For example, in Figure 3.3, we show the same pulse as we did in Figure 2.10, except the VSI

power response is damped (in contrast to using a resistive step). Notice the violations do not appear, as was the case for the simple fix in Figure 2.11. The elegance of this solution is that power is not consumed by an otherwise unnecessary resistive load. It is instead sourced and subsequently returned to the ESS.

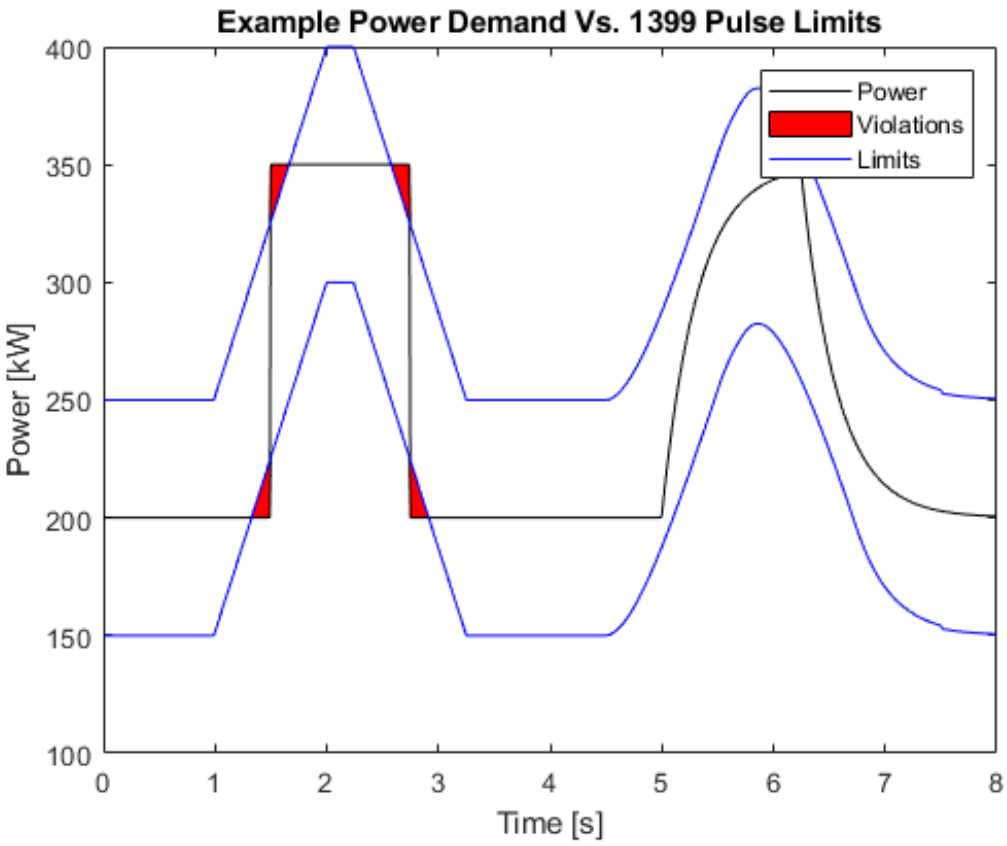


Figure 3.3. Proposed Architecture Pulsed Power Example.

3.2.1 Energy Storage System

Without an ESS, changes in load would need to be immediately handled by the AC bus. To meet the pulsed load requirements of [8], another energy source must be introduced. The ESS is used for this purpose, and it is bi-directional so it is capable of sourcing power to, or sinking power from, the DC bus. A few devices may be used to accomplish this task; notably either a battery or a capacitor could suffice. The requirement, however, is that the energy capacity of the ESS is capable of delivering the required energy, and in sufficient time. For

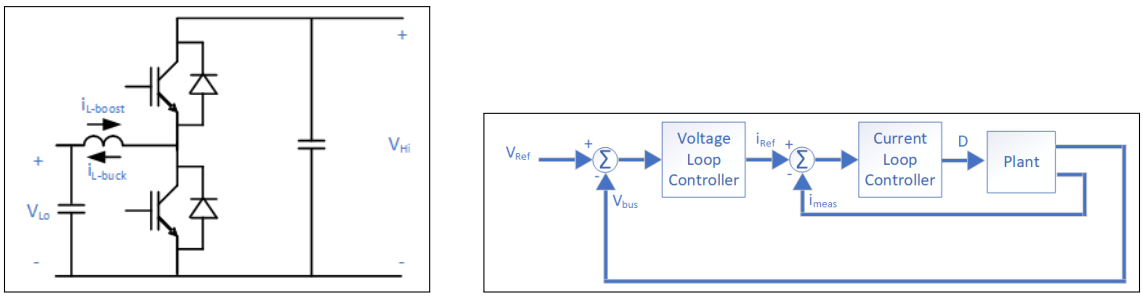
example, the power displayed in Figure 3.2 would require the total power capacity of the ESS to be at least as high as the peak of the ESS power curve. The total energy capacity must be at least as large as the integral under the power curve. These characteristics of the power curve are determined by the size of the load change, as well as the control scheme applied to the grid-following VSI, which is covered in detail later in this thesis. Additionally, to smooth the power response caused by the switching effect of the DC-DC converter, an LCL filter is connected to the ESS.

3.3 DC-DC Converter

The DC bus voltage is controlled utilizing a DC-DC converter. Since in this thesis the converter is bi-directional, and needs to boost the voltage from the battery to a higher voltage DC bus, a bi-directional boost converter is used. The layout of the converter can be seen in Figure 2.2(e). A traditional buck-boost converter has the same layout as our bi-directional boost converter. The difference being that in a traditional buck-boost converter, one of the two switches is always shut. With a bi-directional boost converter, when the reference waveform falls below the carrier waveform both transistors are commanded off. By not maintaining one of the switches shut, the bi-directional boost converter enters DCM during times of low load, which reduces both conduction and transistor switching losses. The converter architecture and control system are depicted side by side in Figure 3.4.

An inner loop-outer loop control scheme is used to operate the bi-directional boost converter. The outer loop generates an error based on the difference between measured DC bus voltage and commanded DC bus voltage. This error is fed to a proportional-integral (PI) controller, whose output is a current command. The current being commanded and measured is the inductor current shown in Figure 3.4. The current error is passed into another PI controller, and the duty cycle is generated from the output of this second PI controller. If the DC bus loading is increased, the DC bus voltage will decrease. The reduction in voltage generates a positive error at the input of the outer loop PI controller, which in turn generates a current command that trends in the positive direction. The duty cycle then increases, which will cause the inductor to push more current to the DC bus (or pull less current from the DC bus, depending on the mode of operation). The increase in current will cause the DC bus capacitor to charge, which increases the DC bus voltage. In summary, a deficiency in stored

energy on the DC bus will result in commanding the inductor to push more energy from the ESS to the DC bus, and a surplus of energy stored on the DC bus will result in commanding the inductor to shed energy from the DC bus to the ESS. The end result is maintaining a constant DC bus voltage by varying the energy flow into and out of the ESS.



(a) DC-DC Converter Architecture (b) Control Block Diagram

Figure 3.4. Bi-directional Boost Details

3.4 Grid-Following VSI

The goal of the power system is to ensure that the AC source supplies the entirety of the load in the steady state. In doing so, the power system must meet the pulsed power specifications of [8]. With the solution proposed, the load is on the DC bus, which separates it from the AC source. Independent control of the power flow from the AC bus to the DC bus can now be realized. To achieve this end, we utilize a grid-forming VSI with a phase locked loop (PLL) as described in [5] and [7]. The current to the DC load is sensed and used to control the line current of the VSI. Our control scheme meets the specifications of [8] by controlling the VSI power utilizing a low pass filter as shown in Figure 3.5.

The effect of the corner frequency of this filter can be seen in Figures 3.6. If the corner frequency is set too high, such as in Figure 3.6(a) and Figure 3.6(b), violations occur. If the corner frequency is set too low, such as in Figure 3.6(d) the AC system never achieves steady state, and an unnecessarily large ESS is required. The design choice of the corner frequency will therefore depend on the applied load changes, the capacity of the ESS, and the desired response of the system.

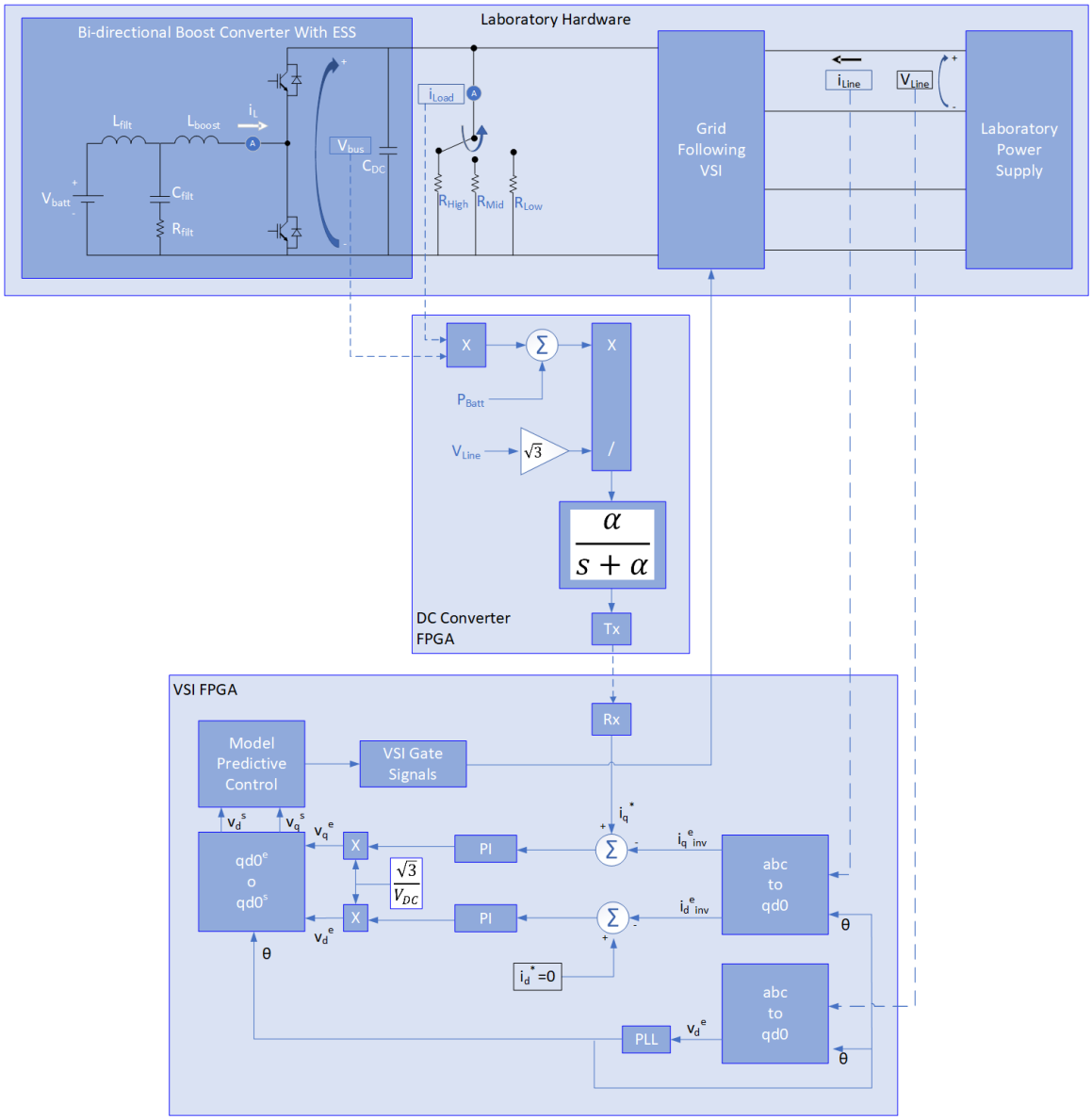
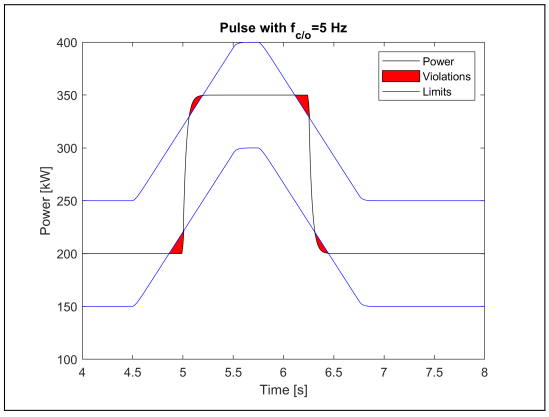
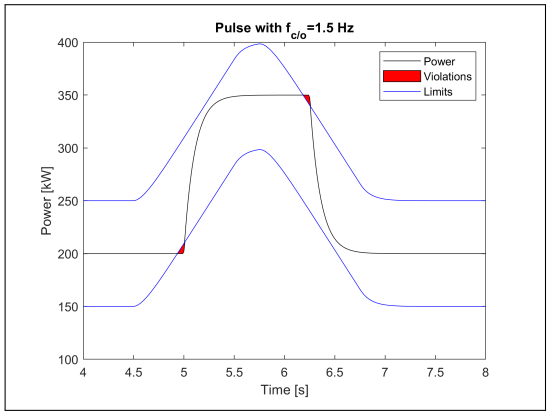


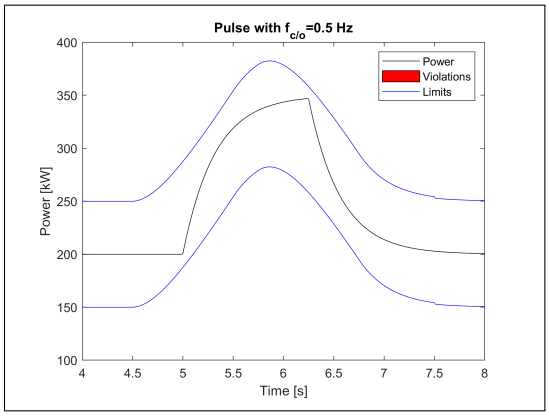
Figure 3.5. System Control Flow



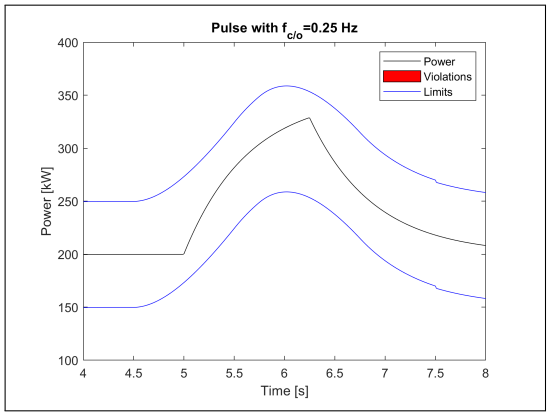
(a) cutoff frequency = 5 Hz



(b) cutoff frequency = 1.5 Hz



(c) cutoff frequency = 0.5 Hz



(d) cutoff frequency = 0.25 Hz

Figure 3.6. Voltage Source Inverter Power vs. Pulsed Limits for Different Filter Cutoff Frequencies

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CHAPTER 4:
Laboratory Setup and Control System Implementation

The system operation is verified utilizing a hardware setup. In this chapter, we present the hardware utilized, its configuration, and the software architecture for the control of power flow.

4.1 Laboratory Setup

A block diagram of the system depicting a high level control flow is shown in Figure 4.1, while the corresponding system schematic was shown previously in Figure 3.1. Two field programmable gate array (FPGA) development boards are used: one to control the AC power flow from the AC bus to the DC bus, and another to control the bi-directional boost converter. The control of the VSI FPGA is covered extensively in [7], where the author details the use of model predictive control to achieve common-mode elimination in a four-leg three-phase inverter. This thesis utilizes the same VSI hardware, although the software is modified for use in this experiment to accept an input communication that commands the peak AC line current into the grid-forming VSI from the AC bus. We do not analyze the power quality of the AC side of the VSI as in [7], rather utilize the same hardware for the purpose of controlling the power flow between the AC and DC buses. The DC converter FPGA controls the power flow through the system, is the point of user interface for system control, and is the focal point to understand this laboratory experiment. The corresponding hardware in the laboratory is shown in Figure 4.2.

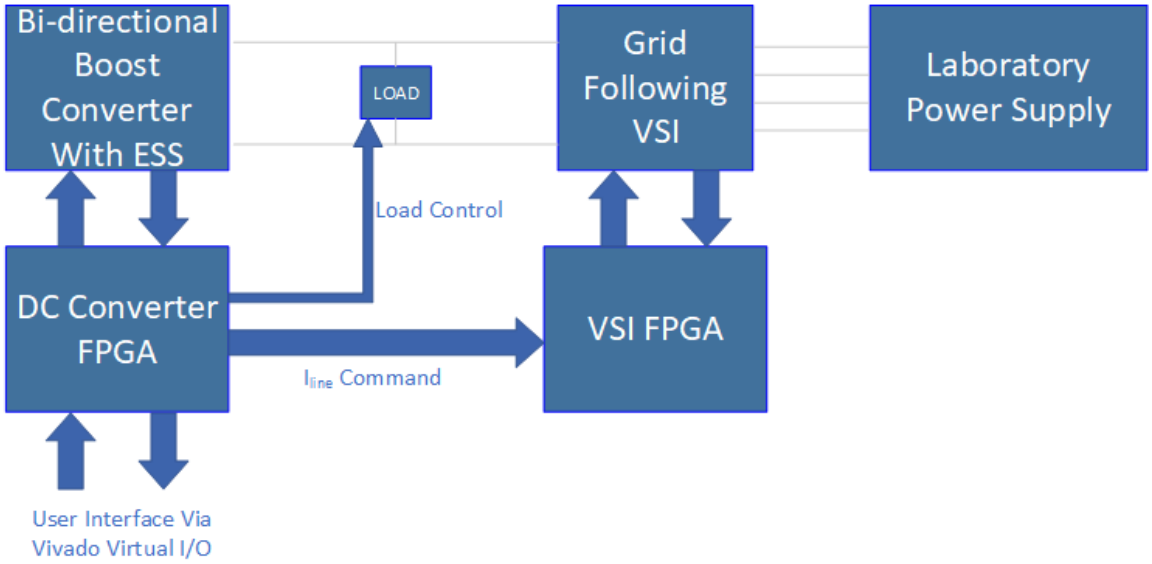


Figure 4.1. System Diagram with FPGA Communications

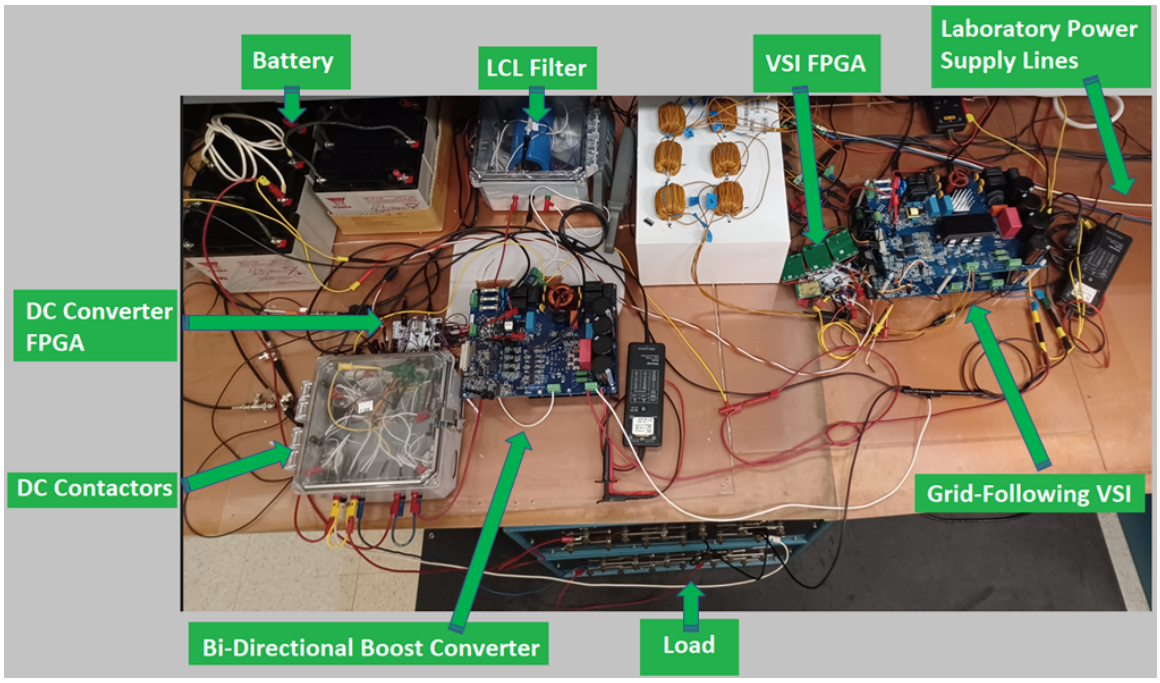
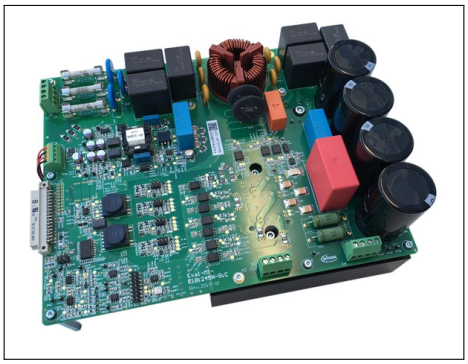
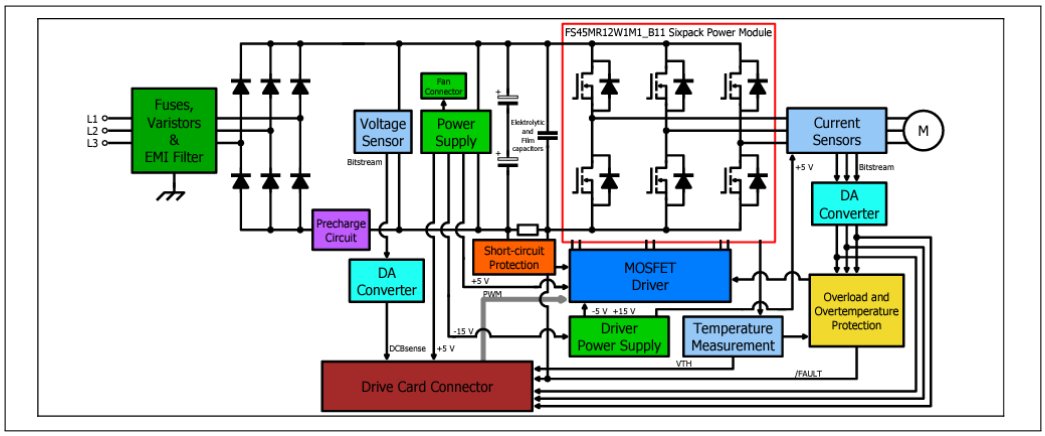


Figure 4.2. Laboratory Setup with Corresponding Block Diagram

The FPGA development boards are used to control the bi-directional boost converter, the grid-following VSI, and DC contactors used in the system. Both the bi-directional boost converter and the VSI are implemented on Infineon Evaluation Boards: Eval-M5-E1B1245N-SiC [20]. The Infineon evaluation board and its associated block diagram can be seen in Figure 4.3.



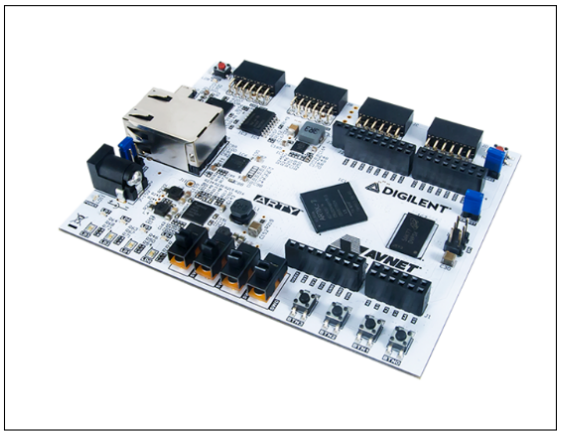
(a) Infineon Evaluation Board Hardware



(b) Infineon Evaluation Board Block Diagram

Figure 4.3. Infineon Evaluation Board Source: [20]

The FPGA used in this thesis is included on an ARTY-a7 FPGA development board made by Diligent [21]. A picture of an ARTY-a7 is seen in Figure 4.4(a), while an example of a DC contactor used in the laboratory setup is seen in Figure 4.4(b).



(a) Arty-a7 FPGA Development Board

(b) DC contactor

Figure 4.4. Laboratory Hardware

4.2 FPGA Control System Implementation

A mid-level block diagram of the bi-directional boost converter FPGA control strategy is shown in Figure 4.5 where the major signals for understanding of the system are provided. Any system identified as a module was constructed using the Simulink hardware description language (HDL) coder function [22].

At the highest level of operation, the bi-directional boost converter operates in one of four states: Off, Startup, Regulating, and Faulted. In the Off state, the user has intentionally shut down the system. The ESS is disconnected from the bi-directional boost converter, the load is disconnected, and the grid-forming VSI is secured. In the Startup state, the ESS is connected to the DC bus by connecting, and then bypassing, a starting resistor to limit the inrush current. In the Regulating state, the bi-directional boost converter is controlling the DC bus voltage to the commanded value, the load contactors are free to shut, and the grid-following VSI is free to drive the AC line current. In the Fault state, the ESS is disconnected from the bi-directional boost converter, load contacts are opened, and the grid-following VSI is secured. The system remains in the Fault state until the fault condition has been cleared and the user has reset the system to the Off state. Only when both conditions are met is the system free again to return to the startup state. The State Determination Module determines which of the four states the system is in and informs all blocks and modules that require that information.

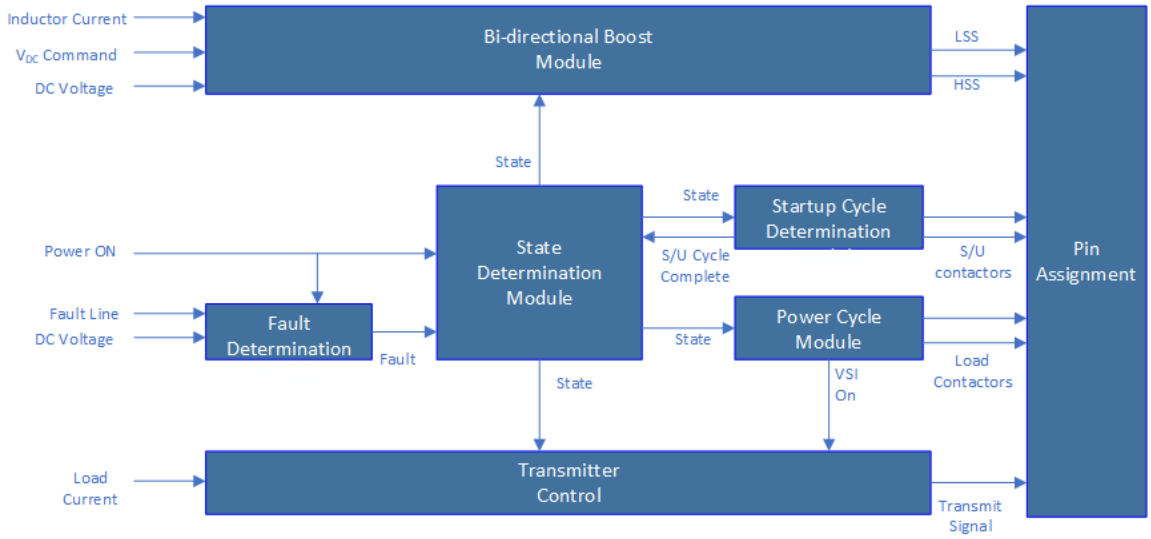
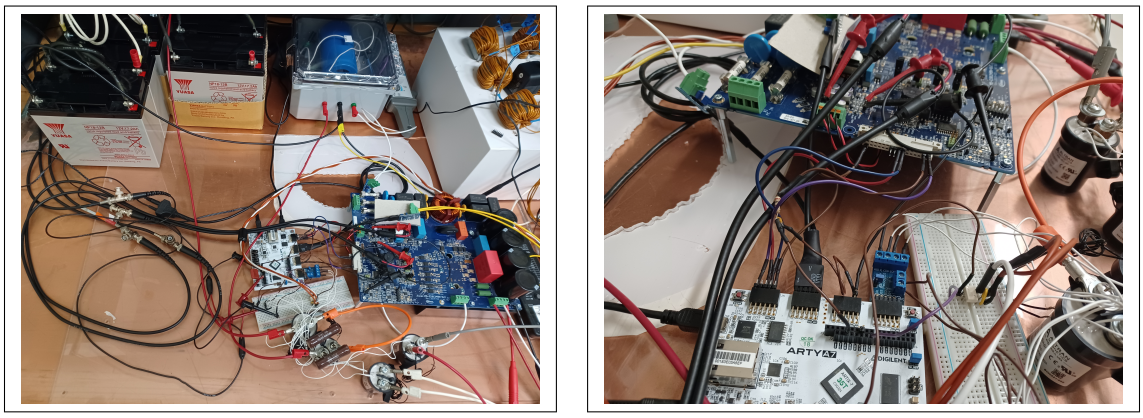


Figure 4.5. FPGA High Level Communications

The Power Cycle Module is responsible for determining the value of the DC load and for commanding the grid-following VSI on or off. It does not determine the AC line current command for the grid-following VSI; how the line current command is generated will be discussed in the next paragraph. The DC load is stepped through one of three states: low, medium and high. The values of the impedances are given in Section 6.1. The hardware and connections corresponding to those found in Figure 4.5 can be seen in Figure 4.6.



(a) Bi-directional boost converter with ESS (b) FPGA Signal Routing

Figure 4.6. Bi-directional Boost Converter Hardware

The transmitter control block generates the commanded AC line current that the grid-following FPGA receives, as seen in Figure 4.1. It consists of several sub-blocks and modules to determine the output, which is seen in Figure 4.7. The Pin Assignment block seen here is the same block as shown in Figure 4.5. The transmitter is allowed to operate in two distinct modes: power-correcting and user-defined. The selection between these two modes is made through the FPGA virtual input output communication, and the signal is passed into the Command Selector block. In user-defined mode, the user can command any AC line current. In power-correcting mode, the AC line current command is generated via the Power To Current Command Module. This module performs the following calculation:

$$i_{Line-pk} = \frac{V_{DC} i_{load} + P_{batt}}{\sqrt{3/2} V_{Line}} \tag{4.1}$$

P_{batt} and V_{Line} are input by the user via Vivado virtual I/O. When P_{batt} is set to zero, this calculation ensures that when the converter is in steady state, the ESS will not be charging or discharging. By changing P_{batt}, the steady state current to the ESS can be adjusted to trickle charge, or trickle discharge. The value of V_{line} is set manually in this process, but the control system is ready to accept an input measurement from the system in real time as part of future research. Even with a measured line voltage, the line current control is open loop. Losses and inaccuracies can cause the commanded line current to be different from what is needed to keep the ESS delivering zero average power. The inaccuracy caused from open loop control can be corrected by designing a closed control loop around the load current measurement, which is another area of interest for future research.

The Low Pass Filter Module is responsible for the damped response of the AC system described in Section 3.4. Any change in commanded AC line current will be damped before being sent to the Transmitter Module. The enable line for the Low Pass Filter Module comes from the Power Cycle Module and determines whether or not to allow the grid-following VSI to inject current. When changing to the Off state, for example, the grid-following VSI will reduce the AC line current in a damped fashion.

The Transmitter Module is shown in Figure 4.7. This module accepts a current command and generates a pulse whose width is proportional to the AC current command. The VSI FPGA will receive this pulse and generate an AC line current based on the width of the

pulse. Finally, the FPGA will only map the transmitter signal to the pin if the converter is not in the Fault state. A Fault state will, without filtration, command the grid-following VSI to zero.

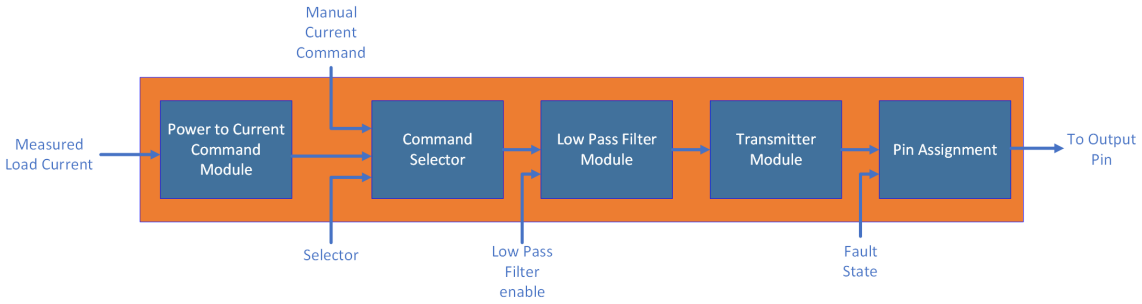


Figure 4.7. Transmitter Control Block Diagram

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CHAPTER 5:
Modeling and Simulations

In this chapter we present the physics-based models used to verify the control architecture of the circuit. We include the results of the Simulink simulations run on these models as well.

5.1 Physics-based Model

To test the power electronics system, a physics-based model of the system was designed and run utilizing Simulink. The model consists of two parts: the control model for the bi-directional boost converter and a higher level power transfer model. Since this model utilizes the switching frequency of 20 kHz, the Nyquist sampling rate dictates that a sampling rate of at least 40 kHz be used. At this high of a sampling rate, even short time simulations require ample data storage. To appropriately simulate the model at this high of a switching frequency would make the simulation excessively cumbersome for analyzing the power flow over longer periods, such as when analyzing the damped power response to meet the pulsed load limits in [8]. A second model is developed for this purpose, and both models are discussed below.

5.1.1 ACM Control

The Simulink model designed to test the bi-directional boost converter is shown in Figure 5.1. The ACM control block is the module programmed into the FPGA for the laboratory experiment. This block accepts as inputs the proportional and integral gains, the measured inductor current, the measured DC bus voltage, the commanded DC bus voltage, and a run signal.

The internal components of the ACM control block are shown in Figure 5.2. The two PI controllers form the inner-outer loop architecture described in Section 2.1.3. The measured voltage is compared against the reference voltage to develop a voltage error. The outer loop PI controller develops a current command that will drive the voltage error to zero. This current command is fed into the inner loop PI controller, which takes as reference a filtered

version of the inductor current. The output of the inner loop PI controller is the reference waveform to be compared against the carrier. The current error is passed as an output for testing and diagnostics, as it can be read from Vivado virtual I/O.

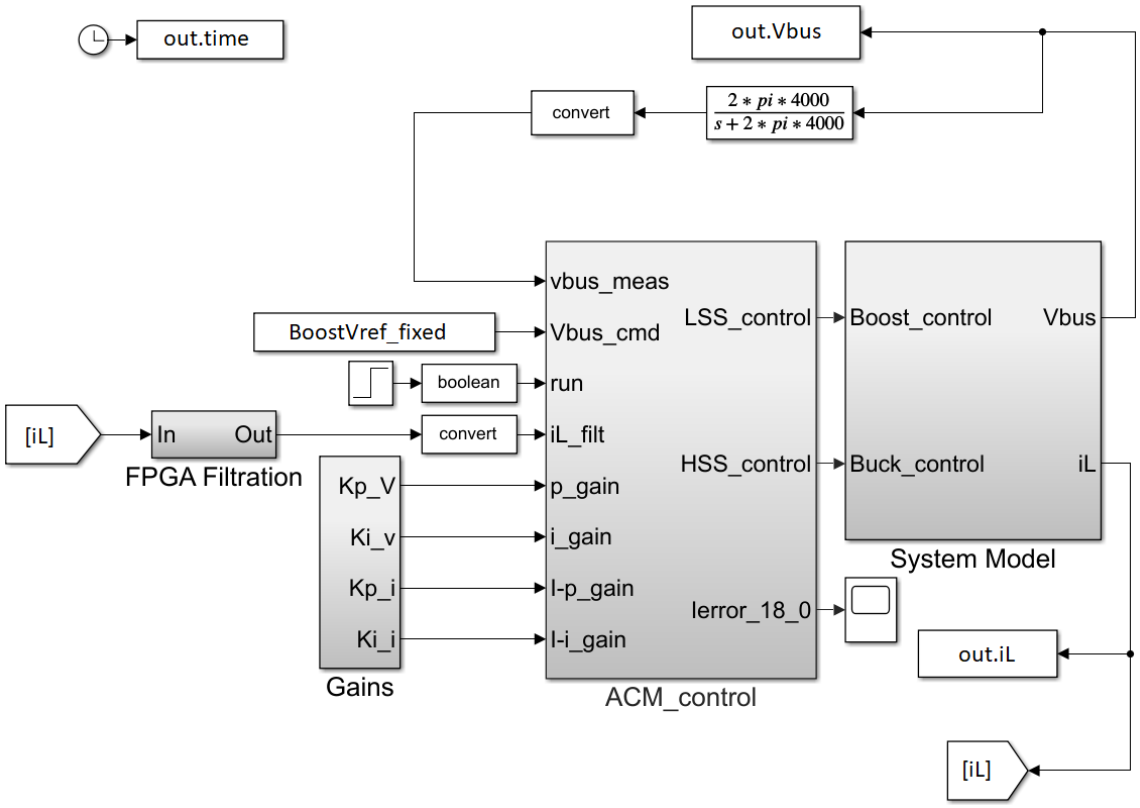


Figure 5.1. DC-DC Converter Simulation Model

The carrier waveform is generated using a free running counter set with a maximum value. The step time of the simulation is set to 40 ns. With each step of the simulation the free running counter increments by one. This repeats until the maximum value of 1250 is reached. On the subsequent clock, the free running counter will reset to zero. By doing so, the duration for the free running counter to complete one cycle is 50 μs, which results in a frequency of 20 kHz; therefore, the switching frequency of the bi-directional boost converter will also be 20 kHz. The gain block is used to normalize the carrier to a peak value of one. Notice the summation blocks both accept the carrier waveform into the negative port, whereas the reference port is different between the two. By switching the sign on the reference port, we ensure that if a positive reference is commanded, then more

positive current will be produced by allowing the LSS-control signal to switch. Under this condition, a negative reference compared to the carrier waveform will be less than zero, and thus ensure the HSS-control switch will always be off. Both reference waveforms, can be seen in Figure 5.3. Notice the reference waveforms are a mirror image of each other around the x-axis. In order to allow the HSS-control line to switch, the reference would need to be less than zero. Under this condition, the LSS-control line will always be less than zero and therefore controlled off. This ensures that only one of the two MOSFETs is controlled ON at any given time.

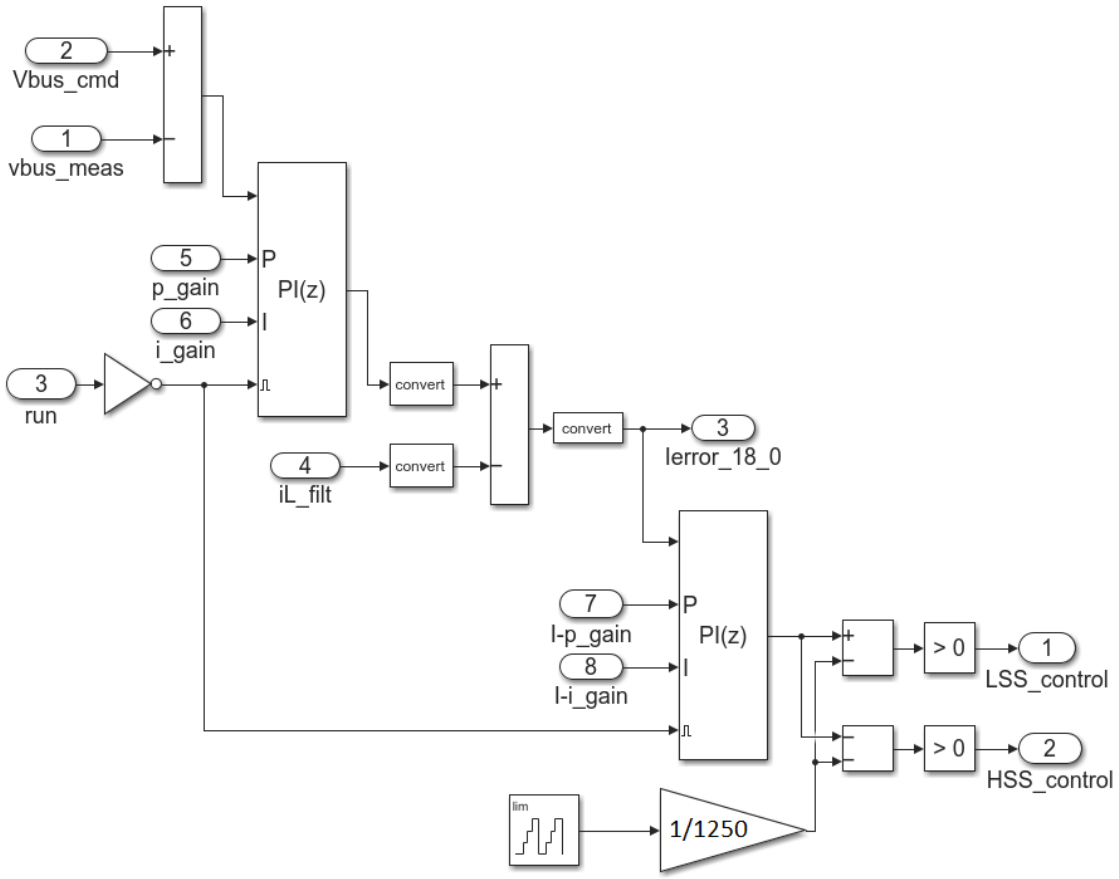


Figure 5.2. DC-DC Converter Simulation Model

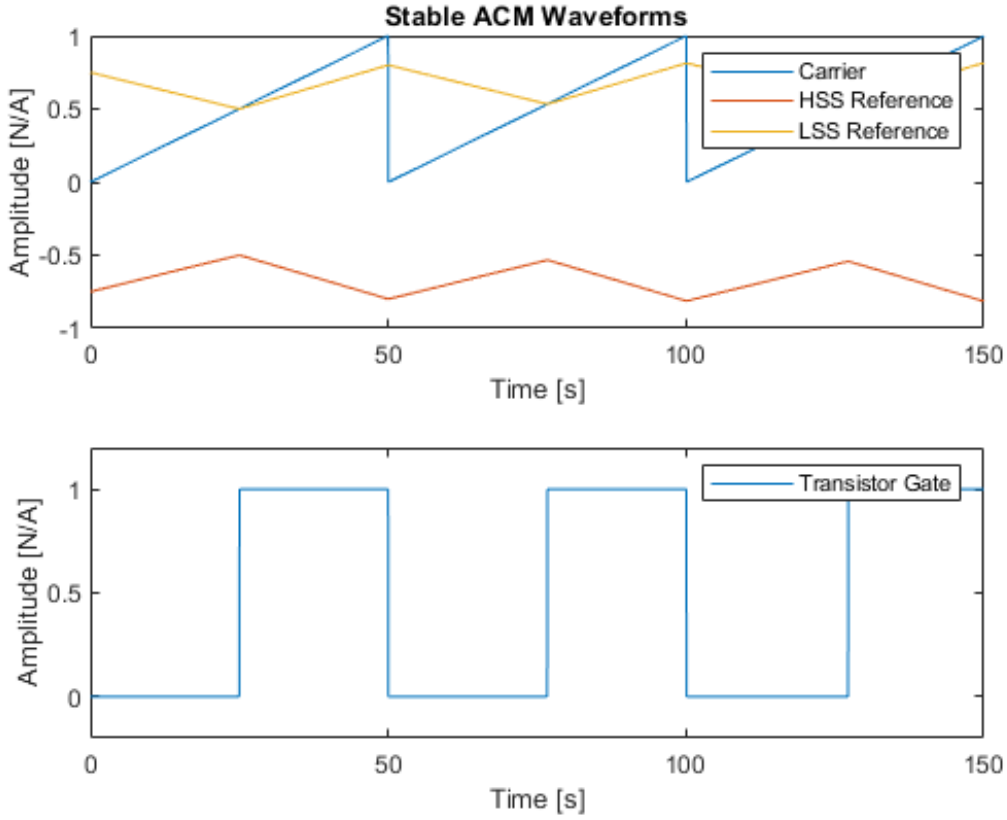
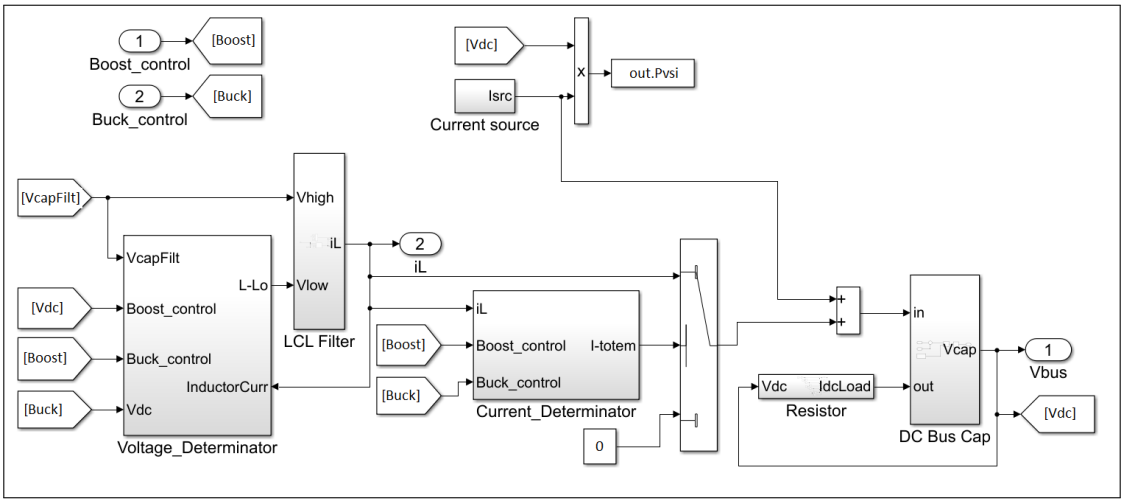


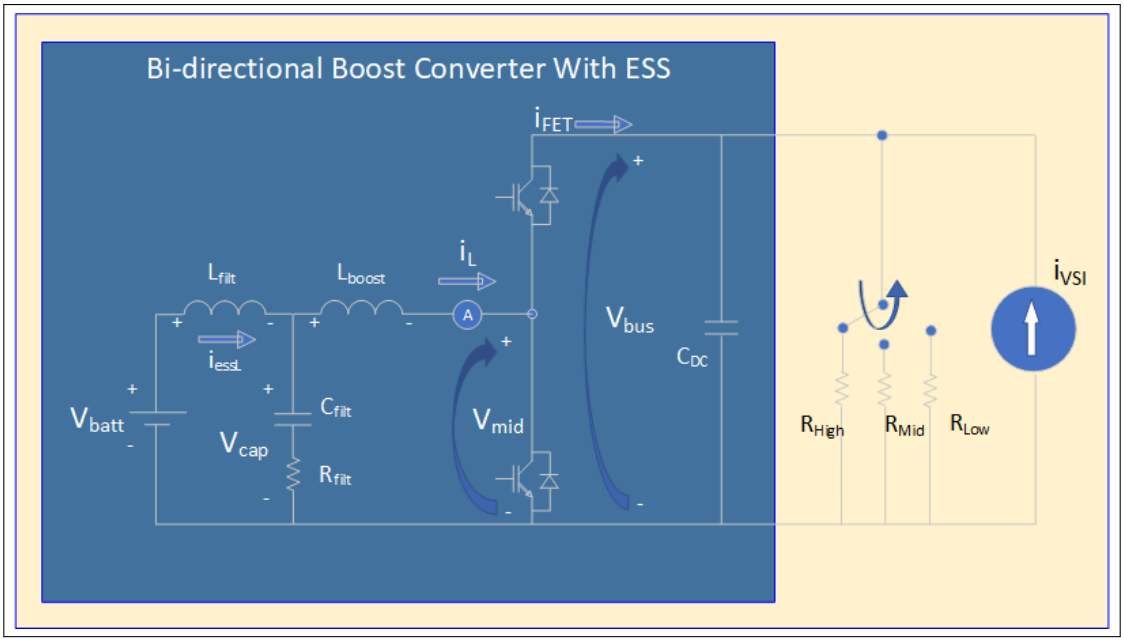
Figure 5.3. HSS and LSS Reference Signals

The System Model block seen in Figure 5.1 is used to determine inductor current and bus voltage, given the LSS-control and HSS-control signals from the ACM control block. In Figure 5.4 we see the internal components of the System Model Block on top, with the corresponding schematic on the bottom.

First, we analyze the LCL filter. The internal components of the LCL-essL, LCL-cap and LCL-boostL blocks are expanded and shown in Figure 5.5.



(a) System Model Block Diagram



(b) System Model Schematic

Figure 5.4. System Model

For the modeling, the passive sign convention is used in which the current through each component is as shown in Figure 5.4(b). This means if the current is reversed, then the value of the current becomes negative, and the voltage definitions remain in their shown polarities. Overall, the blocks then estimate the differential equations:

$$i_L = \frac{1}{L}\int (V_L - i_L R_L)dt \tag{5.1}$$

$$V_{cap} = i_c R_{filt} + \frac{1}{C}\int i_c dt \tag{5.2}$$

$$i_{essL} - i_L - i_{cap} = 0 \tag{5.3}$$

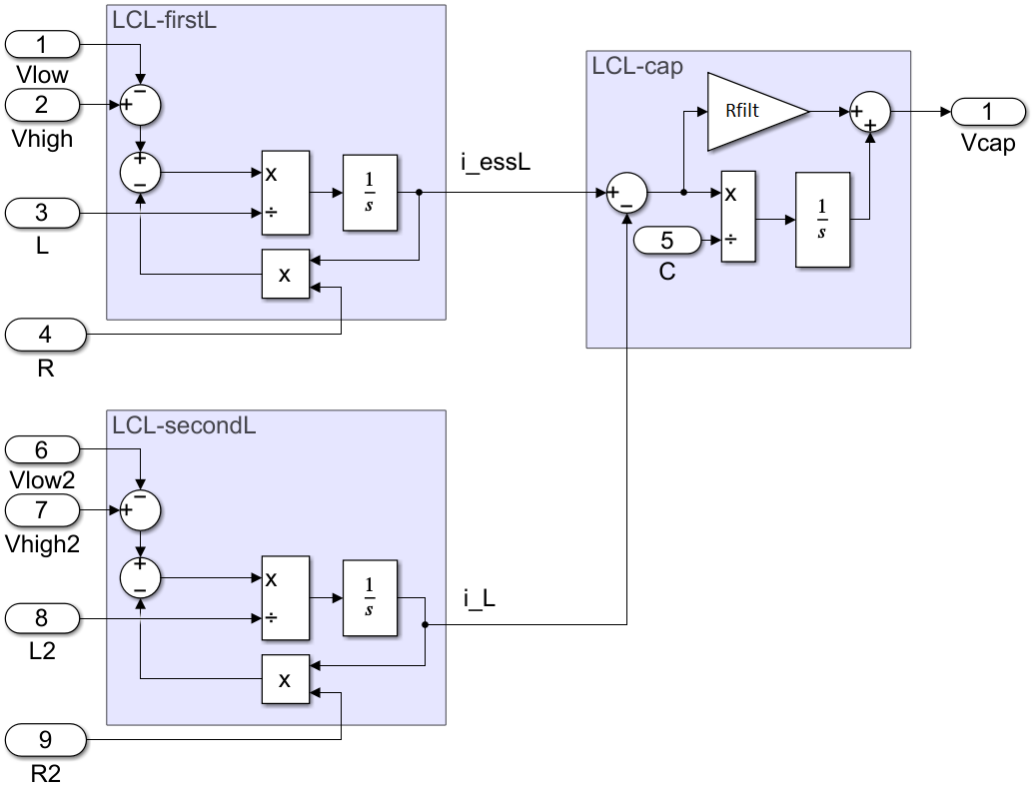


Figure 5.5. LCL Filter Model

Inside the LCL filter we placed a physical resistor in series with the capacitor. This resistor is used to dampen oscillations caused by the resonance from the LCL filter. A bode plot demonstrating this damping effect is shown in Figure 5.6.

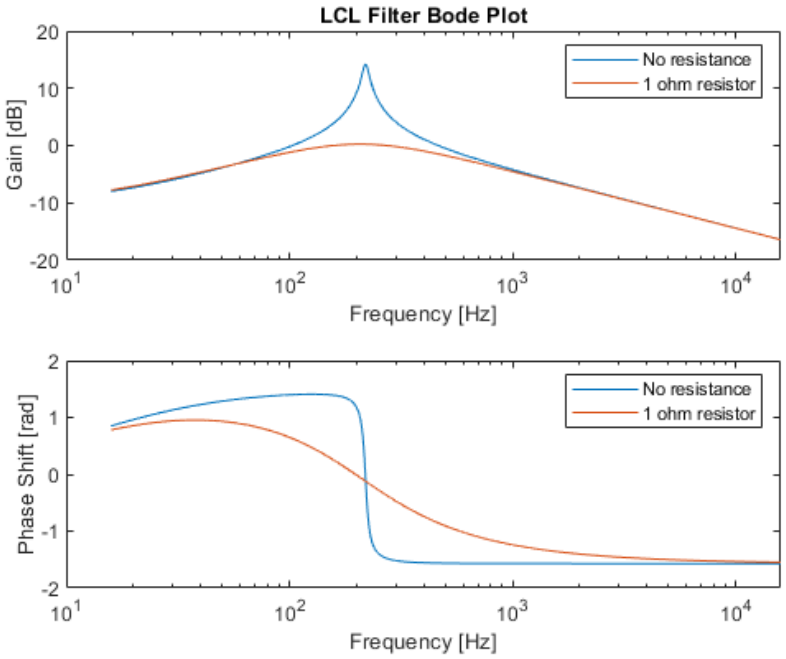


Figure 5.6. LCL Bode Plot

Next, we look at the Voltage Determinator block. This block is required to determine V_{mid}. Based on which FET is conducting and the direction of current, V_{mid} will be different. Assuming zero voltage drop across the FETs, V_{mid} will take on one of three values: DC bus voltage, ground, or floating. Floating implies there is no voltage drop across the inductor, so V_{mid} will assume the same value as V_{cap}. The truth table for the logic implemented in the Voltage Determinator block is shown in Table 5.1.

Table 5.1. V_{mid} Truth Table

Inductor current:	**Positive**	**Zero**	**Negative**
HSS Shut	V_{DC}	V_{DC}	V_{DC}
None Shut	V_{DC}	$V_{filtCap}$	0
LSS Shut	0	0	0

The Current Determinator block is used to calculate whether or not the inductor current is flowing to the DC bus. This knowledge is needed to perform a Kirchoff's current law (KCL) calculation on the DC bus. There are two paths for the current to flow from the inductor to the DC bus: The high side FET, or the associated anti-parallel diode. The high side FET will be conducting when the inductor current is negative and the HSS-Control line is ON. The anti-parallel diode will be conducting if the LSS-Control line is OFF and inductor current is positive. In either of these conditions, the inductor current is carried into or out of the DC bus. If neither of these conditions are met, the inductor current is not carried into or out of the DC bus.

Finally, the Current source, DC Bus Cap and Resistor blocks compute a KCL calculation on the DC bus. To simulate the functionality of the bi-directional boost converter while either charging or discharging the ESS, however, an active source must be included in the model. Since the functionality of the grid-following VSI is not desired to be simulated in this experiment, the grid-following VSI is modeled as an ideal current source, as shown in Figure 5.4.

5.1.2 Power Flow Simulation

The power flow simulation is designed to run over a longer period of time than the bi-directional boost converter simulation. For example, a cutoff frequency of 0.5 Hz requires about 1.5 s to analyze out to five time constants. To reduce the quantity of data recorded, the step size must be increased. We therefore approximate the switching action of the bi-directional boost converter instead of calculating the switching action. The model can be seen in Figure 5.7.

The inner loop and outer loop PI controllers are contained in the PI Controllers block. The output of the inner loop PI controller is the reference waveform compared against the carrier. Since the carrier is normalized to 1, the reference waveform is analogous to the duty cycle (D). The steady state average inductor current is computed using the same LCL filter in equations (5.1), (5.2), and (5.3). Since V_{mid} is equal to V_{DC} for the percentage of time equal to the duty cycle, the steady state value must be the average over time: $V_{mid} = (1 - D)V_{DC}$. The average steady state current entering the DC bus from the bi-directional boost converter, i_{FET}, is calculated: $i_{FET} = (1 - D)i_L$. The internal components of the DC Bus KCL block

are shown in Figure 5.8. Notice this is identical to the DC bus KCL portion of the ACM Control simulation, except instead of an ideal current source, the current entering the DC bus from the VSI is now replaced with an input i_{VSI}.

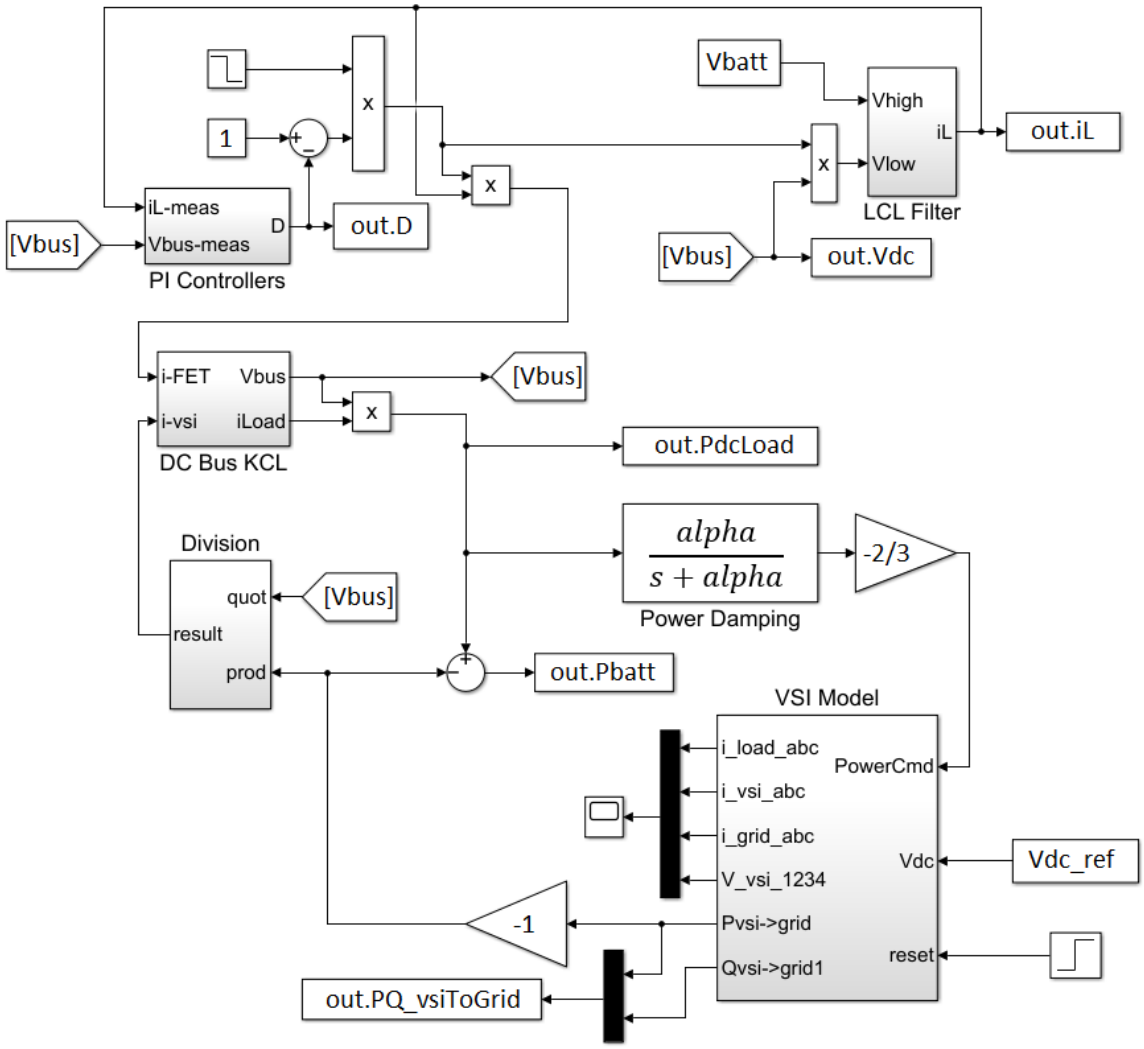


Figure 5.7. Power Flow Model

The VSI model block takes as input a power command, and it outputs the AC grid-side real and reactive power flowing into the VSI from the AC grid. The details inside this block are shown in Figure 5.9.

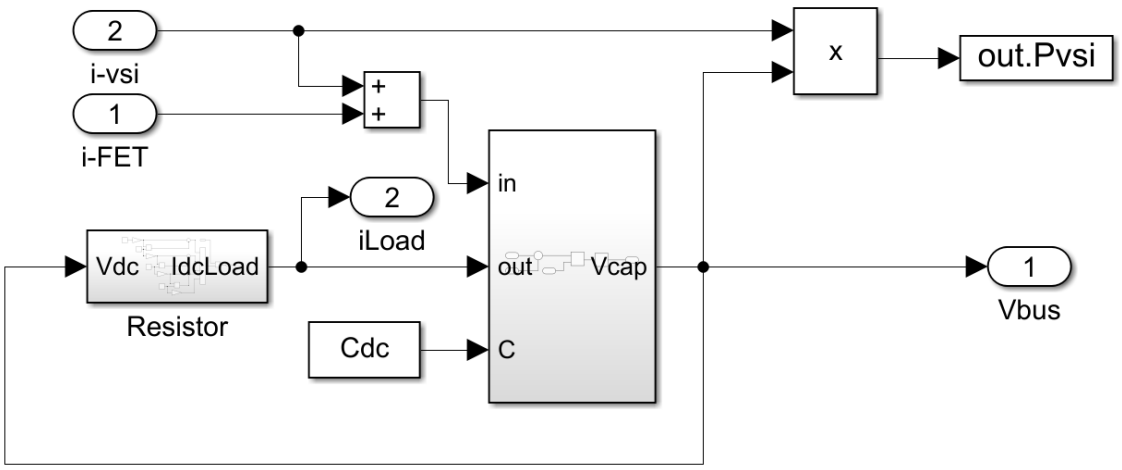


Figure 5.8. DC Bus KCL Block

The grid-following VSI uses a PLL to control the reactive power produced or consumed by the VSI. The function of a PLL is to compute the phase angle of the voltages as described in [5]. Once the phase angle of the voltage is determined, the reactive power can be adjusted by commanding the phase angle of the current to be leading, in phase with, or lagging the voltage angle. Since real power is always orthogonal to reactive power, a reference frame transformation can be utilized as described in [23]. This transformation will convert a three phase waveform, each with its own phase angle, to a direct-quadrature (dq) synchronous frame. In the dq synchronous frame we can control the in-phase magnitude of all three phases simultaneously with the direct (d) variable, and we can control the reactive magnitude of all three phases simultaneously with the quadrature (q) variable. The function of the abc2dq blocks is to convert the phases of the input into a two parameter output, where the parameters are direct and quadrature. The power control block accepts the voltage and current, in the dq synchronous frame, as well as the power command, also notably in the dq synchronous frame, as inputs. The block diagram of the Power Control block is shown in Figure 5.10.

The PI controllers depicted in 5.10 will ensure the in-phase voltage is commanded to reach the desired real power, while the quadrature voltage command remains zero, since no reactive power flow is desired. Since this model is designed to operate over longer periods, the switching action of the VSI is assumed to be ideal. That is, the voltage command in the dq synchronous frame is assumed to be the exact voltage that the VSI produces. The VSI

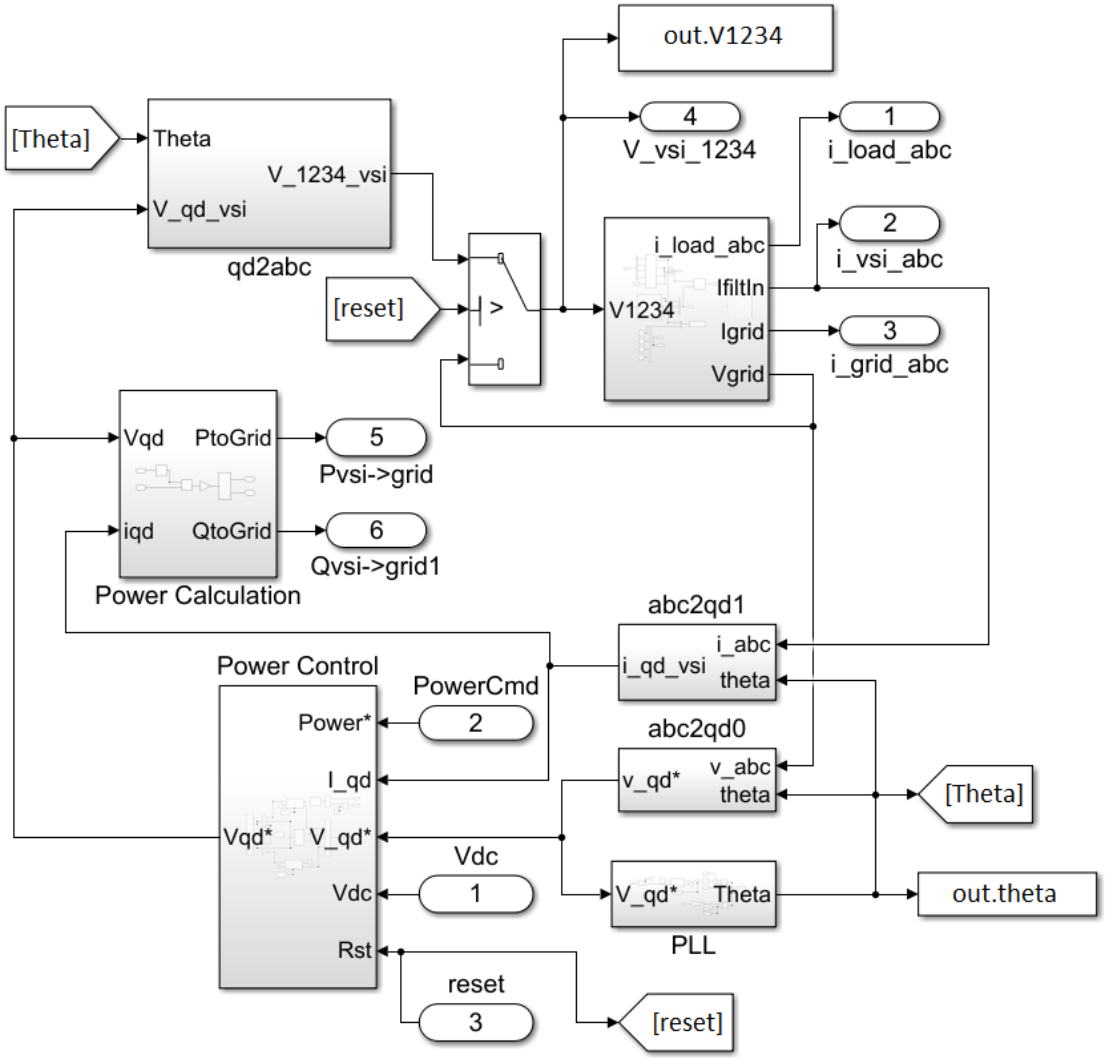


Figure 5.9. VSI Model Block

switching operation is covered in [7]. The voltage level at each leg of the VSI is computed in the qd2abc block. Note that the fourth leg is assumed to be zero voltage for this experiment. Next, the real and reactive power flowing into the VSI from the AC grid are computed in the Power Calculation block, which computes the following calculation:

$$P + jQ = \frac{3}{2} V_{qd}^{*} I_{qd} \tag{5.4}$$

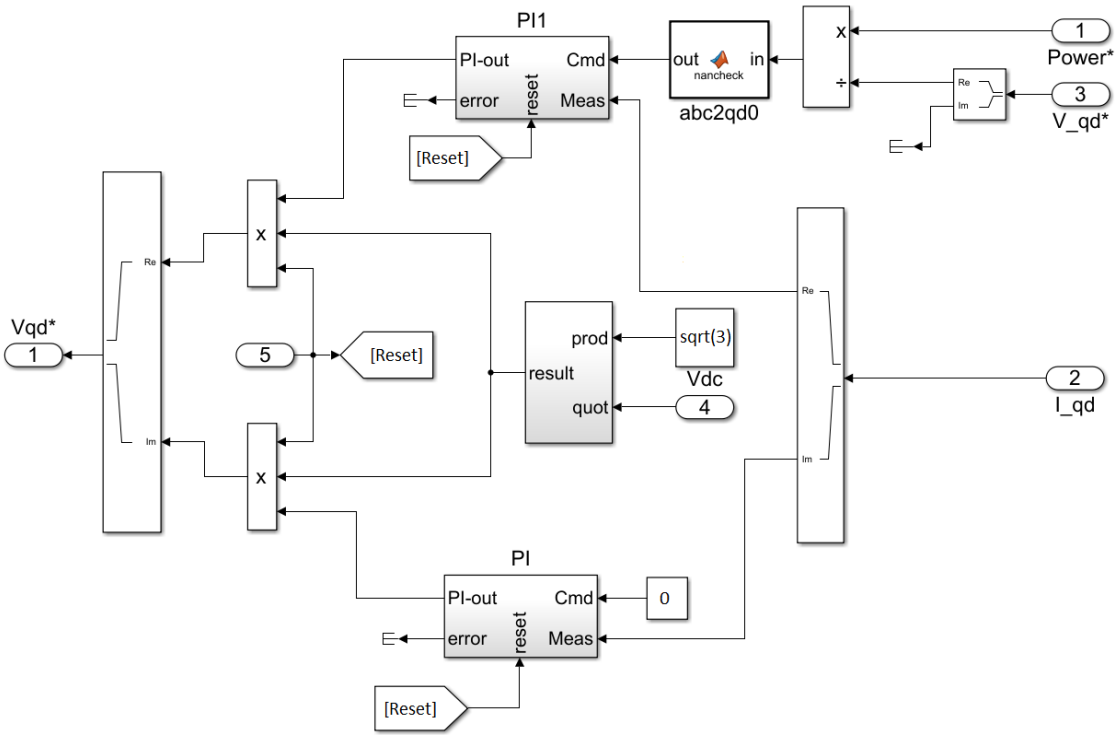


Figure 5.10. Power Control Block

Finally, looking back to the higher level power flow model in Figure 5.7, we compute the real power entering the DC bus from the VSI as the negative of the real power flowing into the VSI from the AC bus. The reasoning for the sign inversion is that the VSI is sourcing current to the DC bus, whereas it was consuming current from the AC bus. Notice the battery power is calculated as the difference between the power consumed by the load and the power injected by the VSI. Any inaccuracies created by assuming perfect switches that always operate in steady state are thus assumed by the battery, which implies the battery bus is the "slack bus". The damped response of the VSI to meet the limits of the pulsed load in [8] is modeled by the transfer function at the power command input of the VSI model block. This low pass filter performs the actions described in Section 2.3.

5.2 Simulation Results

The physics-based model of the system discussed in Chapter 4 was simulated utilizing MATLAB and Simulink to model the behavior of the system and verify appropriate power

flow. The simulation is broken into the two physics-based models discussed in Chapter 4. The objectives of the physics-based model were twofold; 1) Ensure proper operation of the bi-directional Boost Converter Module block prior to programming the module onto the FPGA and 2) Model the performance of the power flow in the system to ensure the pulsed load specifications in [8] are satisfied.

5.2.1 Bi-directional Boost Converter

The bi-directional boost converter discussed in Section 5.1.1 is analyzed first. This simulation is intended to verify the switching operation of the bi-directional boost converter satisfactorily maintains the DC bus voltage under different disturbances. Converter stability needs to be ensured as discussed in Section 2.1.3, and component values for the simulation parameters are provided in Table 5.2.

Table 5.2. Simulink Bi-directional Boost Physics-based Model Parameters.

Component	Value
LCL Filter Inductors	400 μH
LCL Filter Capacitor	2000 μF
LCL Filter Resistance	1 Ω
Load Resistance (Low)	460 Ω
Load Resistance (Mid)	58 Ω
Load Resistance (High)	29 Ω
DC Bus Capacitance	3600 μF

The grid-following VSI is modeled as an ideal current source to predict its impact on the bi-directional boost converter. The load is modeled as an ideal resistance with step changes inserted. The DC bus voltage and VSI current values used in the simulations are provided in Table 5.3.

Table 5.3. Bi-directional Boost Converter Commanded Values.

Parameter	Value
V_{DC}	100 V
I_{VSI}	3 A

The proportional and integral gains were tuned using the time-domain simulation and are provided in Table 5.4.

Table 5.4. Bidirection Boost Converter PI Gains.

Parameter	Value
Outer Loop K_p	2.6
Outer Loop K_i	18.7
Inner Loop K_p	0.2
Inner Loop K_i	2.0

Four simulations are run, each modeling two step changes in a single parameter: one step away from the initial conditions, and one step back to the original conditions. The initial conditions and the parameter to be varied in each simulation are given in Table 5.5. The difference between simulations 3 and 4 is that in simulation 3 the load is held constant at the Low value during the VSI change, and in simulation 4 the load is held constant at the Mid value during the VSI change.

Table 5.5. Simulated Parameters

Simulation	Parameter	Initial	Intermediate	Final
1	Load Resistance	Low	Mid	Low
2	Load Resistance	Mid	High	Mid
3	VSI Current	0 A	3 A	0 A
4	VSI Current	0 A	3 A	0 A

The first two simulations are run using a stepped change in load. In Figure 5.11 the load is stepped from Low to Mid, and in Figure 5.12 the load is stepped from Mid to High. In both instances the load is increased at time 0.08 s and decreased at time 0.24 s. Prior to 0.08 s, the converter is not in steady state. Since the step time is small compared to the total simulation time, the load is changed before allowing the converter to achieve steady state to conserve resources. At 0.08 s, the converter is operating in DCM with the battery discharging. The increase in load moves the converter into CCM with the battery discharging. The grid-following VSI is secured in these two simulations, which implies the bi-directional boost converter must supply the entire load from the ESS. In both simulations, the voltage does not deviate beyond 97 V to 102.2 V, or -3% to +2.2% from the commanded value. The magnitude of this deviation, as well as the inductor ripple current are observed to be larger in Figure 5.12, where the change in load is more aggressive.

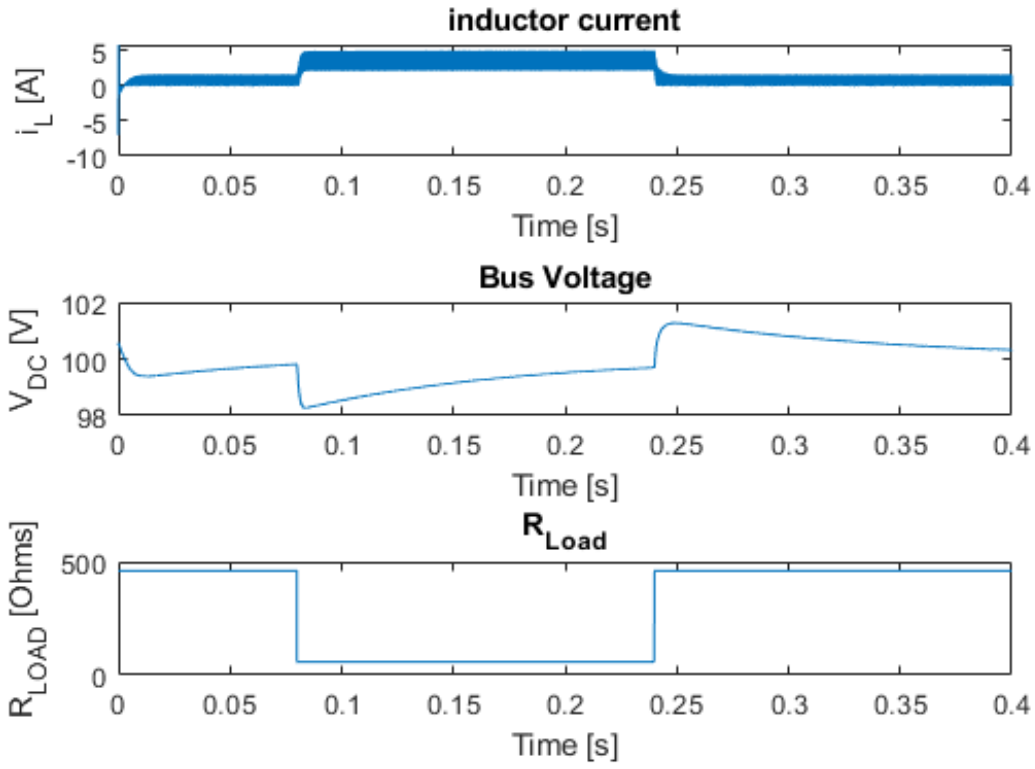


Figure 5.11. Simulation Result for a Small Load Change

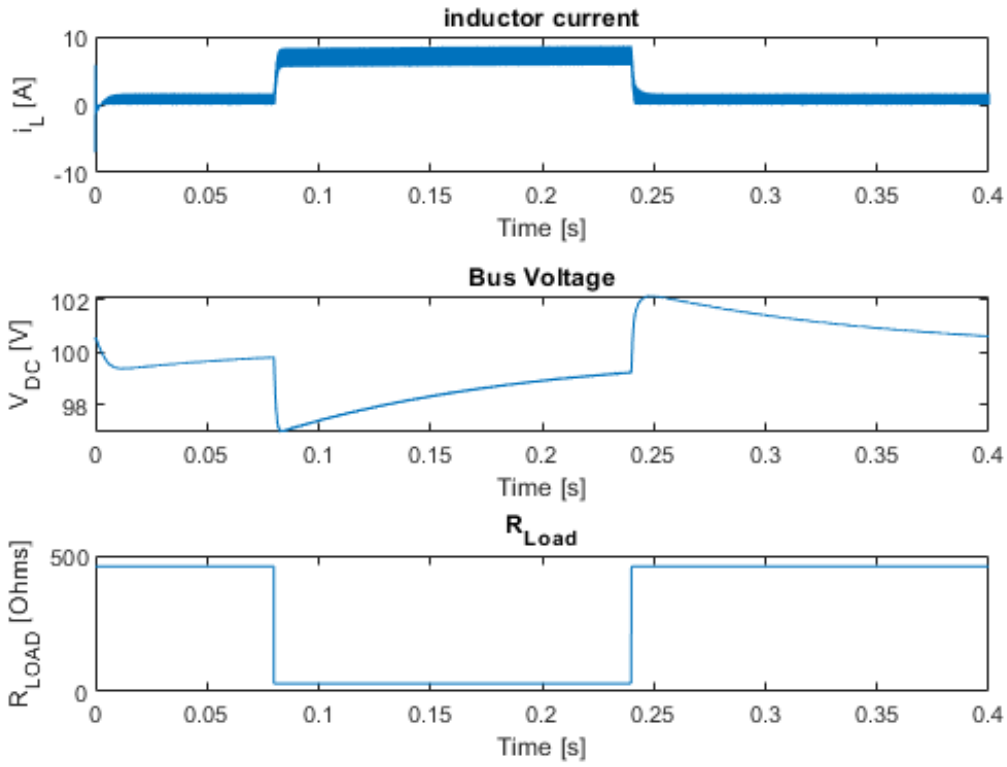


Figure 5.12. Simulation Result for a Large Load Change

The next two simulations are run utilizing a constant load, and applying a step change in VSI current. In these simulations, the VSI current is modeled as an ideal DC current source. The first current step simulation results are shown in Figure 5.13. The applied load in this simulation is constant, and held at the Low resistance value. At time 0.08 s, the ideal DC current source begins injecting 3 A of DC current. This additional energy reduces the demand on the bi-directional boost converter, resulting in a reduction in i_L. The bi-directional boost converter is operating in DCM, with the battery discharging, while the VSI is injecting current. In the second current step simulation, all parameters remain the same except the load is held constant at the Mid resistance value. The results are shown in Figure 5.14. The VSI is injecting more power than is required by the load. This changes the direction of i_L, and the bi-directional boost converter is now operating in CCM with the battery charging.

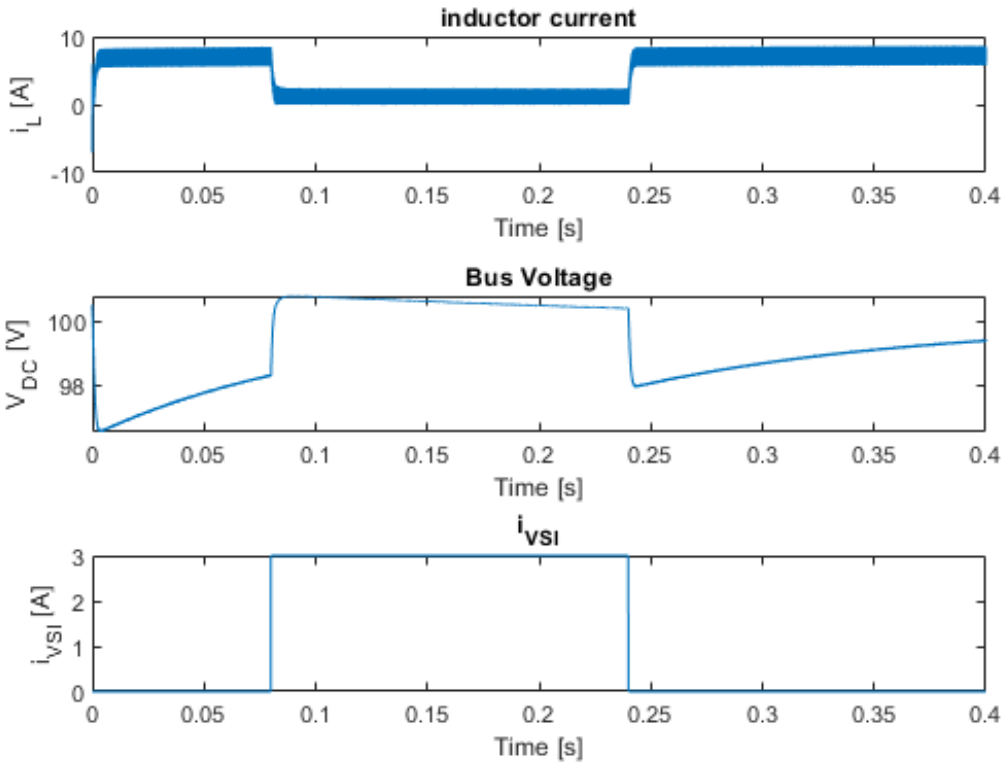


Figure 5.13. Simulation Result for a Small VSI Current Change

5.2.2 Power Flow

The power flow model discussed in Section 5.1.2 is now run in simulation. These simulations utilize a larger step size to observe power flow over longer time periods, which allows us to analyze the effect of the damping caused by the low pass filter. The switching that occurs in both the bi-directional boost converter and the grid-following VSI are approximated in order to support the use of a larger step size, as discussed in Section 5.1.2.

The system schematic and associated component parameters can be seen in Figure 5.15 and Tables 5.6 and 5.7 respectively. There are four PI controllers in this model, one for the inner loop, one for the outer loop, and two for the AC line current. The AC line current PI controllers are in the dq synchronous frame, and as such, there is one controller for the in-phase parameter, and one for the quadrature parameter.

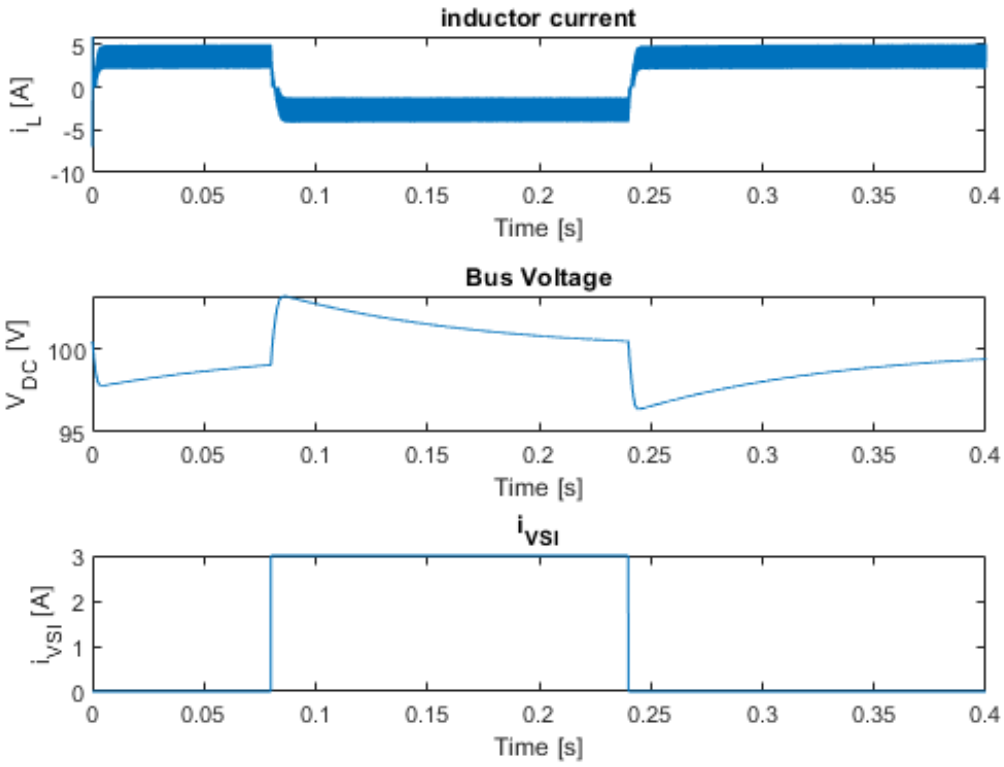


Figure 5.14. Simulation Result for a Large VSI Current Change

Table 5.6. Simulink Power Flow Physics-based Model DC Parameters.

Component	Value
V_{DC}	100 V
V_{BATT}	48 V
LCL Filter Inductors	400 μH
LCL Filter Capacitor	2000 μF
LCL Filter Resistance	1 Ω
Load Resistance (Low)	460 Ω
Load Resistance (Mid)	58 Ω
Load Resistance (High)	29 Ω
DC Bus Capacitance	3600 μF

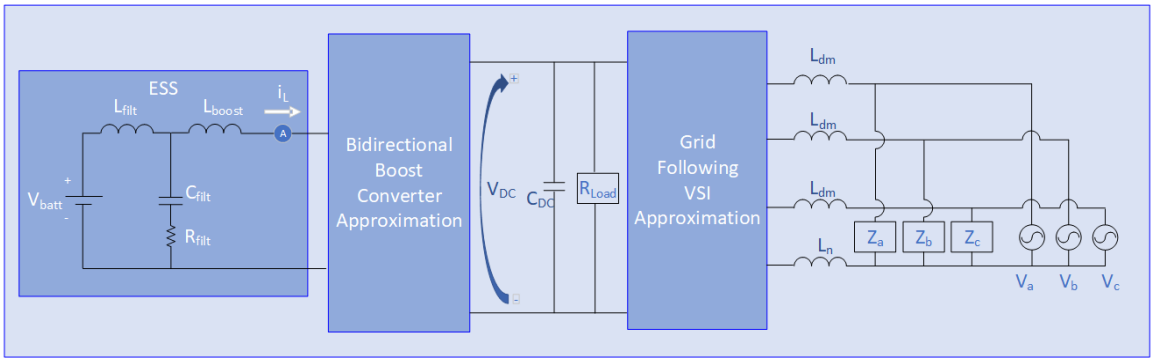


Figure 5.15. Power Flow Simulation Schematic

Table 5.7. Simulink Power Flow Physics-based Model AC Parameters.

Component	**Value**
Phase Voltage	30 V
Frequency	60 Hz
L_{dm}	400 μH
L_n	400 μH
Z_a, Z_b, Z_c	116 Ω

Table 5.8. Power Flow Model PI Gains.

Parameter	**Value**
Outer Loop K_p	2.6
Outer Loop K_i	18.7
Inner Loop K_p	0.2
Inner Loop K_i	2.0
In-Phase current K_p	25
In-Phase current K_i	50
Quadrature current K_p	25
Quadrature current K_i	50

The simulation runs in six stages. Each stage lasts two seconds. The stages are summarized in Table 5.9. The corresponding power flow results of the simulation are shown in Figure 5.16. The DC bus voltage and bi-directional boost converter inductor current are shown in Figure 5.17.

Table 5.9. Power Flow Model Stages.

Stage Number	Time Duration [s]	Load	VSI Status
1	10 - 12	Low	Off
2	12 - 14	Medium	Off
3	14 - 16	Medium	Power Correcting
4	16 - 18	High	Power Correcting
5	18 - 20	Medium	Power Correcting
6	20 - 22	Low	Power Correcting

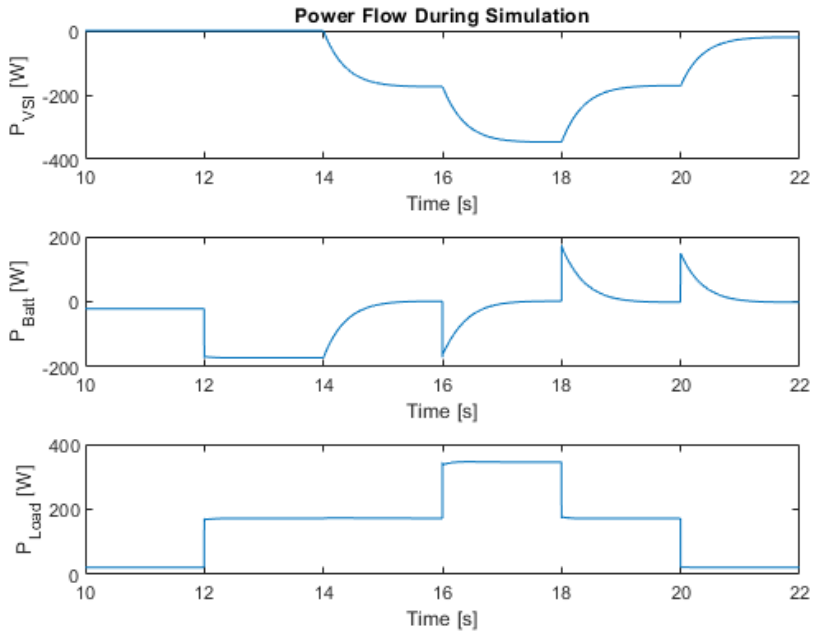


Figure 5.16. Simulation Power Flow Results

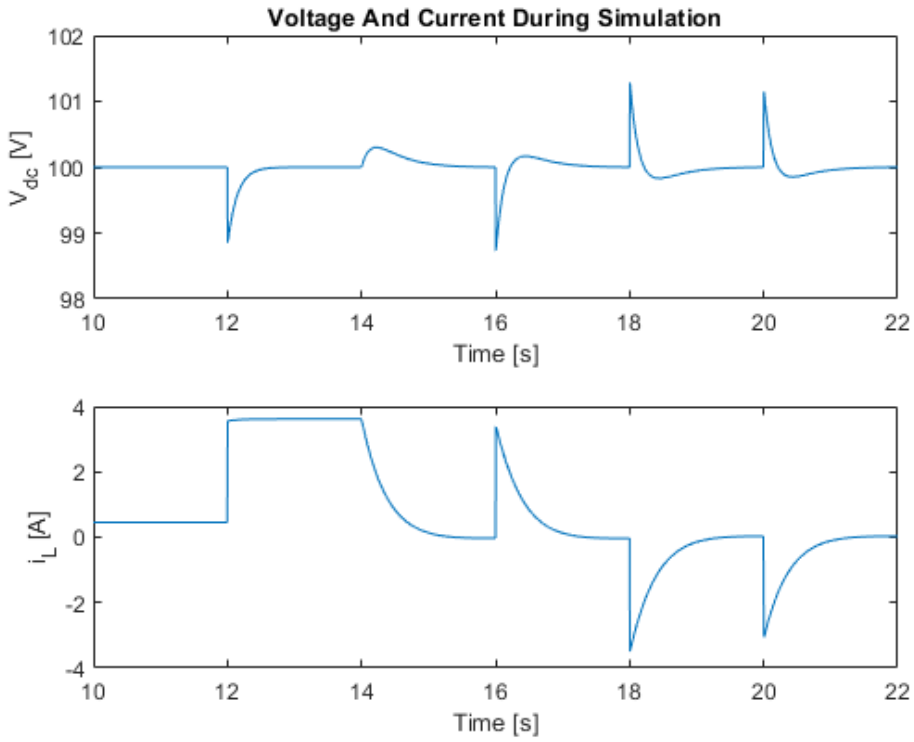


Figure 5.17. Simulation DC Bus Voltage and Bi-directional Boost Converter Inductor Current

The simulation begins at 10 s to allow the integrators in the PI controllers to achieve steady state, and begins with a trickle discharge on the ESS. The load is increased to place a larger demand on the ESS without power correction from the VSI. This is why during stage 2 P_{ESS} remains negative. In this figure, positive power implies power consumption from the DC bus, while negative power implies power supply into the DC bus. At 14 s the simulation enters stage 3, in which the VSI is commanded to supply power equal to the entirety of the load. It does so in a damped fashion through the low pass filter in which the cutoff frequency is set to 0.5 Hz. The VSI remains in power-correcting mode for the remainder of the simulation as the load is varied in the remaining stages. In each stage we notice P_{ESS} returns to zero, meaning the VSI picks up the entirety of the load. P_{VSI} is plotted against the pulsed power requirements of [8] in Figure 5.18.

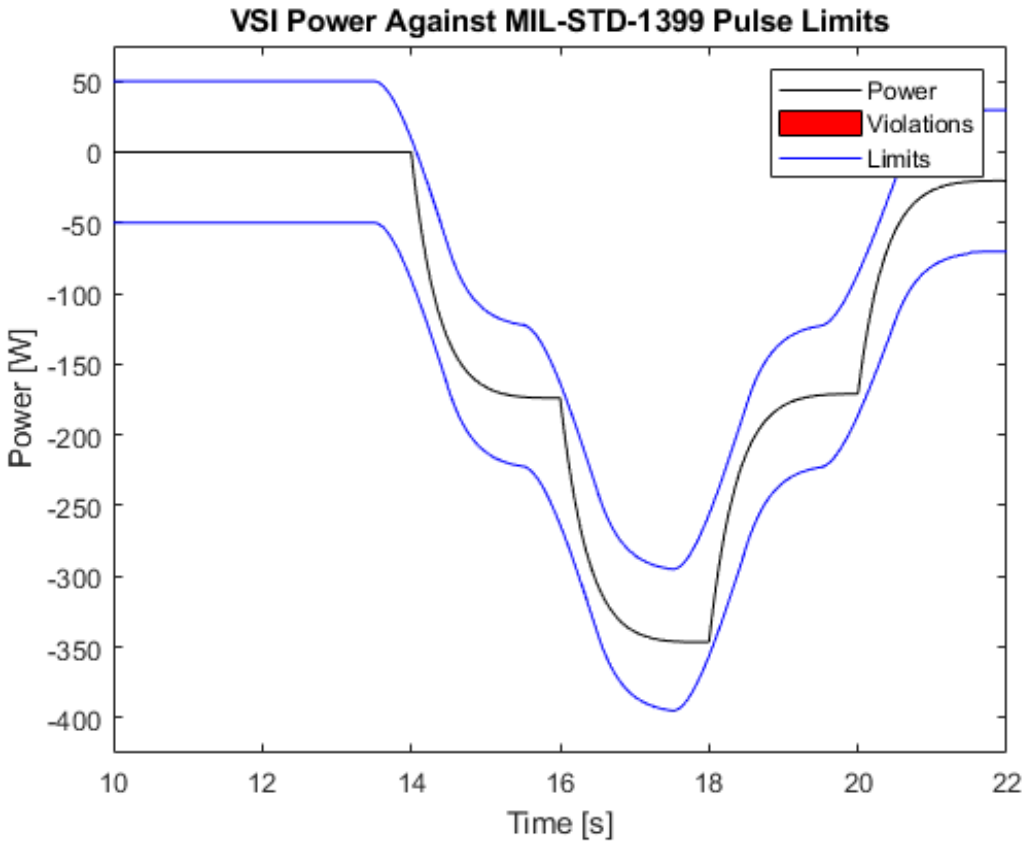


Figure 5.18. Simulation VSI Power vs. 1399 Pulsed Load Limits

CHAPTER 6:
Experimental Results

In this chapter we present the results from running the circuit in the Naval Postgraduate School Power Electronics Laboratory. First, we present an experimental setup designed to match the simulations presented in the previous chapter. We then increase the voltage to Type 1 voltage, as specified by [8], and provide those results as well.

6.1 Experimental Results

The DC converter and grid-forming VSI were utilized in the laboratory setting to obtain the results in this section. Four 12 V batteries were connected in series inside the ESS, and the measured voltage at the time of the experiment was 50 V. The line voltage at the AC side of the grid-following VSI was set to 54 V RMS line-to-line. All component values, and the PI gains used are included in Table 6.1. The load is changed by shutting and opening the DC contactors described in Section 4.2. The experiment is conducted using the stages included in Table 6.2. The experiment is designed as detailed in Table 5.9, but uses different time references.

Table 6.1. Experimental Parameters

Component	Value
V_{DC}	100 V
V_{BATT}	48 V
LCL Filter Inductors	400 μH
LCL Filter Capacitor	2000 μF
LCL Filter Resistance	1 Ω
Load Resistance (Low)	464 Ω
Load Resistance (Mid)	51.56 Ω
Load Resistance (High)	19.3 Ω
DC Bus Capacitance	3600 μF
Outer Loop K_p	2.6
Outer Loop K_i	18.7
Inner Loop K_p	0.2
Inner Loop K_i	2.0

Table 6.2. Power Flow Experiment Stages.

Stage Number	Time Duration [s]	Load	VSI Status
1	0.0 - 0.5	Low	Off
2	0.5 - 2.5	Medium	Off
3	2.5 - 4.5	Medium	Power Correcting
4	4.5 - 6.5	High	Power Correcting
5	6.5 - 8.5	Medium	Power Correcting
6	8.5 - 10	Low	Power Correcting

To describe the parameters measured and calculated, refer to the simplified schematic in Figure 6.1. The measured values are: I_L, V_{bus}, I_{Load}, and I_{Line}. The parameters that are set, but not measured in real time are V_{batt}, and V_{Line}. The capacitor C_{DC} is a bank of capacitors

included on the Infineon development boards as seen in Figure 4.3(a) [20]. Each board contains a capacitor bank, and there are a total of three boards used. Each of the capacitor banks are connected in parallel, so the value of C_{DC} is the sum of all these capacitors. The capacitors are board mounted and there is not an exposed line to place a current sensor, so this value is estimated from the equation:

$$i_{Cap} = C\frac{dv}{dt}. \tag{6.1}$$

I_{FET} is calculated by assuming battery power is equal to power delivered to the DC bus from the bi-directional boost converter using the following equation:

$$i_{FET} = \frac{P_{batt}}{V_{Bus}} = \frac{(V_{batt})(V_{i_L})}{V_{Bus}} \tag{6.2}$$

The final current is i_{VSI} which is calculated using the following KCL equation:

$$i_{VSI} = i_{Load} - i_{FET} + i_{Cap}. \tag{6.3}$$

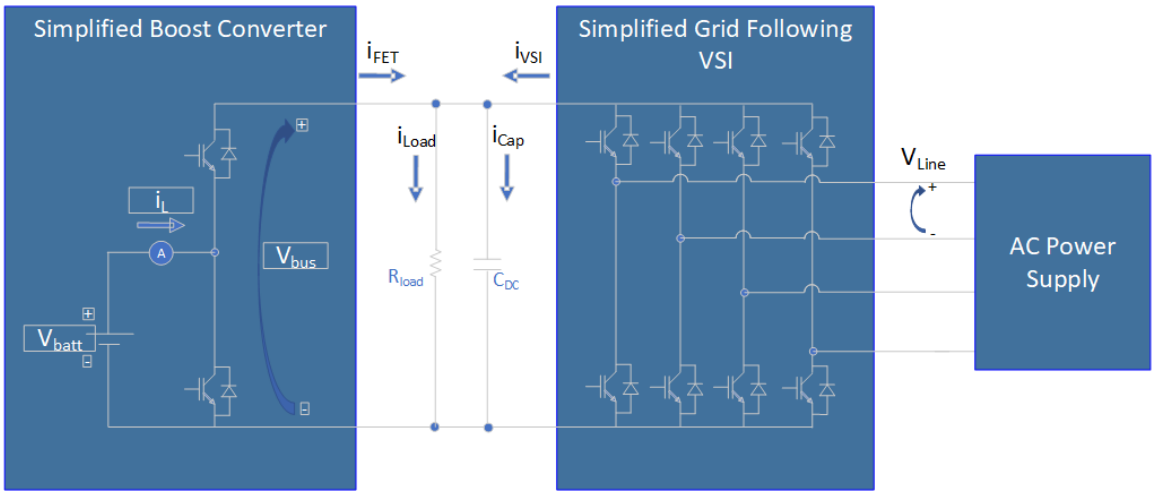


Figure 6.1. Simplified Experimental Schematic

From the data above, the following results are obtained. DC bus voltage, bi-directional boost converter inductor current, and load current are shown in Figure 6.2. The four parameters i_L, V_{Bus}, i_{Load}, and i_{Cap} were post processed by passing each through a low pass filter with cutoff frequency of 100 Hz. The filtered waveforms are shown in Figure 6.3. The filtered data is used to calculate the power flow in the system, and is shown in Figure 6.4. The power from the ESS is obtained by multiplying the inductor current by the battery voltage, which was measured at the time of the experiment at 50 V. Any losses in the bi-directional boost converter are neglected. The load power is obtained from the product of the DC bus voltage and the load current.

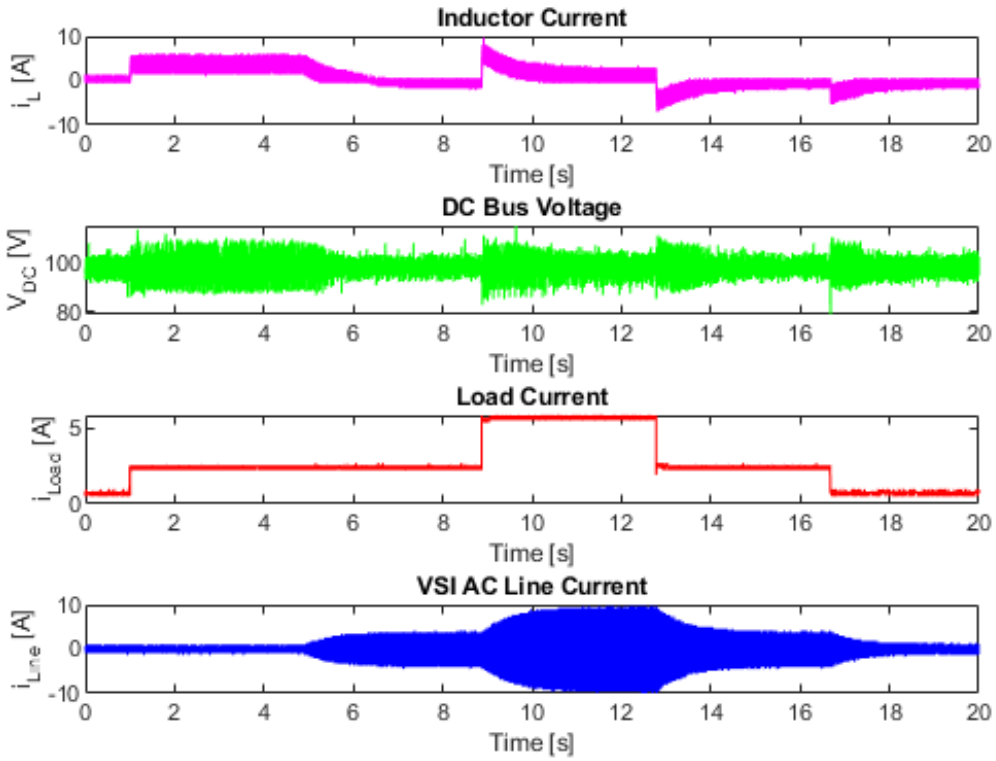


Figure 6.2. Experimental Measurements

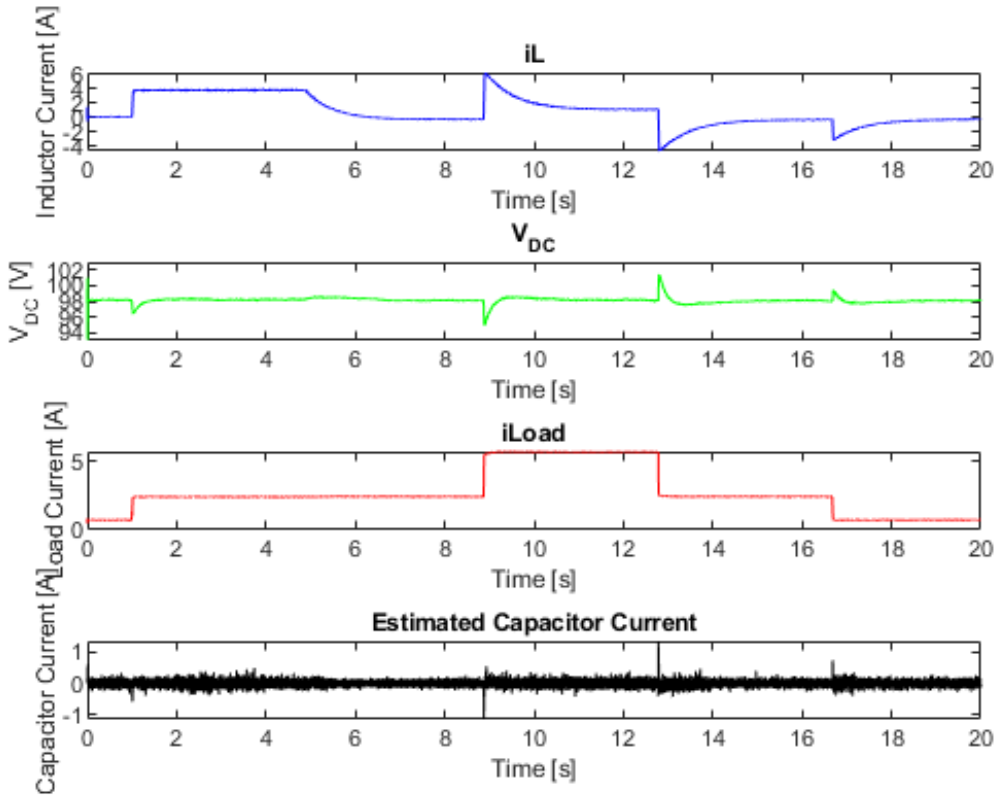


Figure 6.3. Experimental Measurements Post Low-Pass Filter

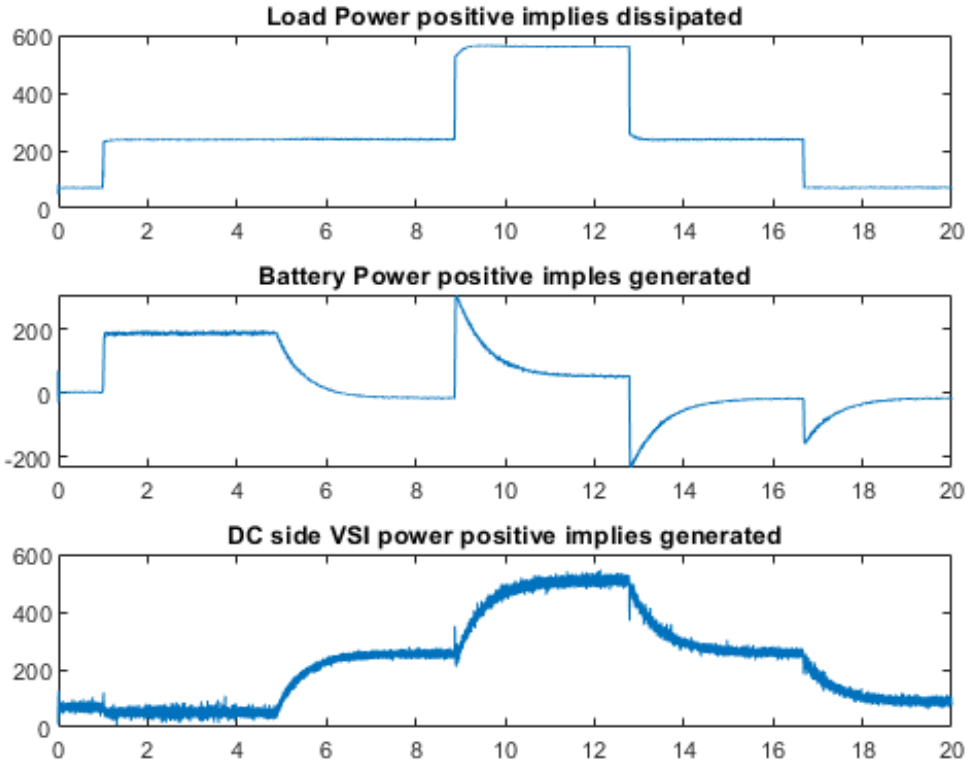


Figure 6.4. Experimental Power Flow

The bi-directional boost converter is able to maintain DC bus voltage to within between 115.21 V and 78.85 V, or +15.2 to -21.15 percent of the commanded value. The converter is set to maintain 100 V_{DC}, yet we notice the voltage remains at 98 V_{DC}. This is caused by an offset in the voltage sensor digital to analog converter. Between t=0.5 s and t=2.5 s, the VSI is commanded off, so the ESS is supplying the DC load. The grid-following VSI is not disconnected from the circuit, and the AC line voltage is still applied. This means current can still pass between the AC and DC sides of the VSI. The way we secure the VSI in the laboratory experiment is to send a commanded line current of zero.

The power flow shown in Figure 6.4 after t=2.5 s shows that the VSI supplies the power required to keep the current flowing into or out of the ESS zero, and does so in a damped fashion. To apply the limits of [8], the VSI power must be scaled up through post processing.

We chose to scale up the power enough to ensure the stepped rise in power at t=4.5 s is equivalent to a 150 kW increase in power. The resulting VSI power is run through the pulsed power algorithm described in Section 2.3 and is shown in Figure 6.5. The large power spikes at t=8.5 s and t=12.5 s are caused by the capacitor current. This current is not measured, and the same spikes are seen in the capacitor current of Figure 6.3. The estimation is not perfect and is the reason some of the capacitors effect is reflected in the VSI power plot.

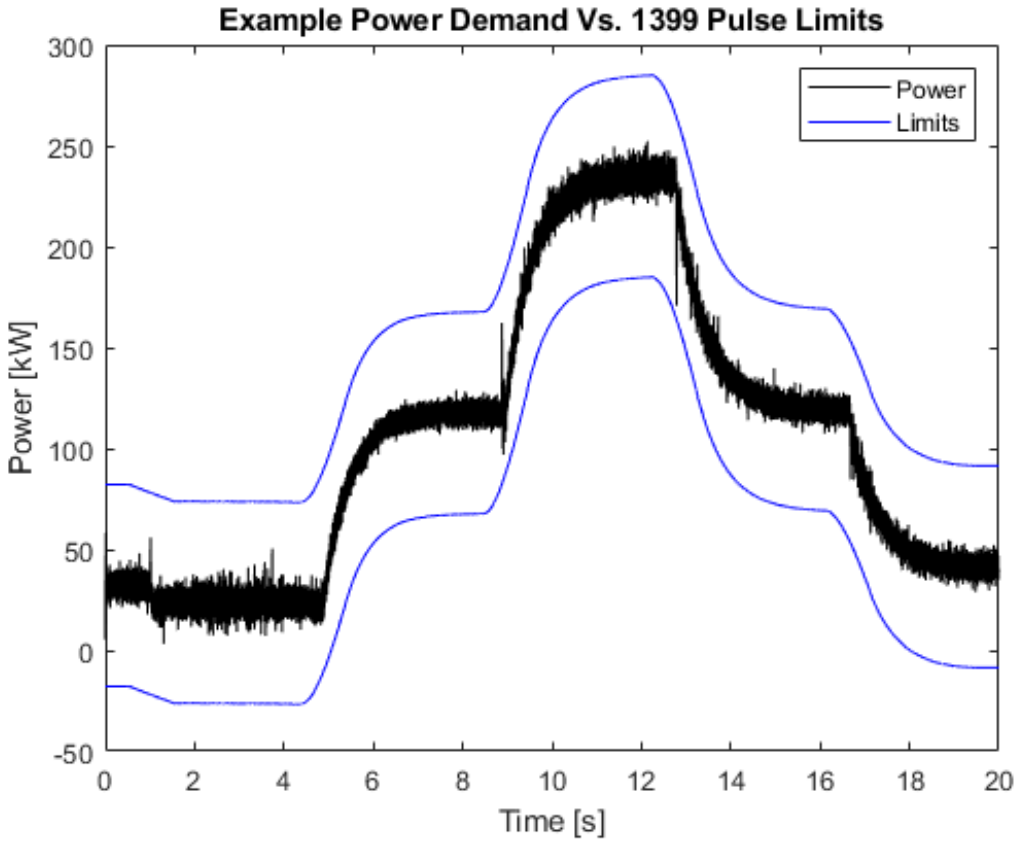


Figure 6.5. Scaled Experimental VSI Power vs. Limits of MIL-STD-1399

6.2 Transient Response and Fault Mode

When the bi-directional boost converter is delivering power to the DC bus, the inductor charges over the period that the low side switch is conducting. The ESS does not pass energy to the DC bus due to anti-parallel diode for the high side switch. This means the DC bus

capacitor discharges to supply the load. By doing so, an interesting phenomenon is created; when the bi-directional boost converter is commanded to a higher voltage, it will initially lower the DC bus voltage in order to charge the inductor. The resulting effect is known as a right half plane zero [24]. One undesirable effect this can cause is increasing the duty cycle beyond what the system is designed to handle. An example is shown in Figure 6.6, where yellow is the inductor current, green is the DC bus voltage, and blue is the fault signal produced by the Infineon development board.

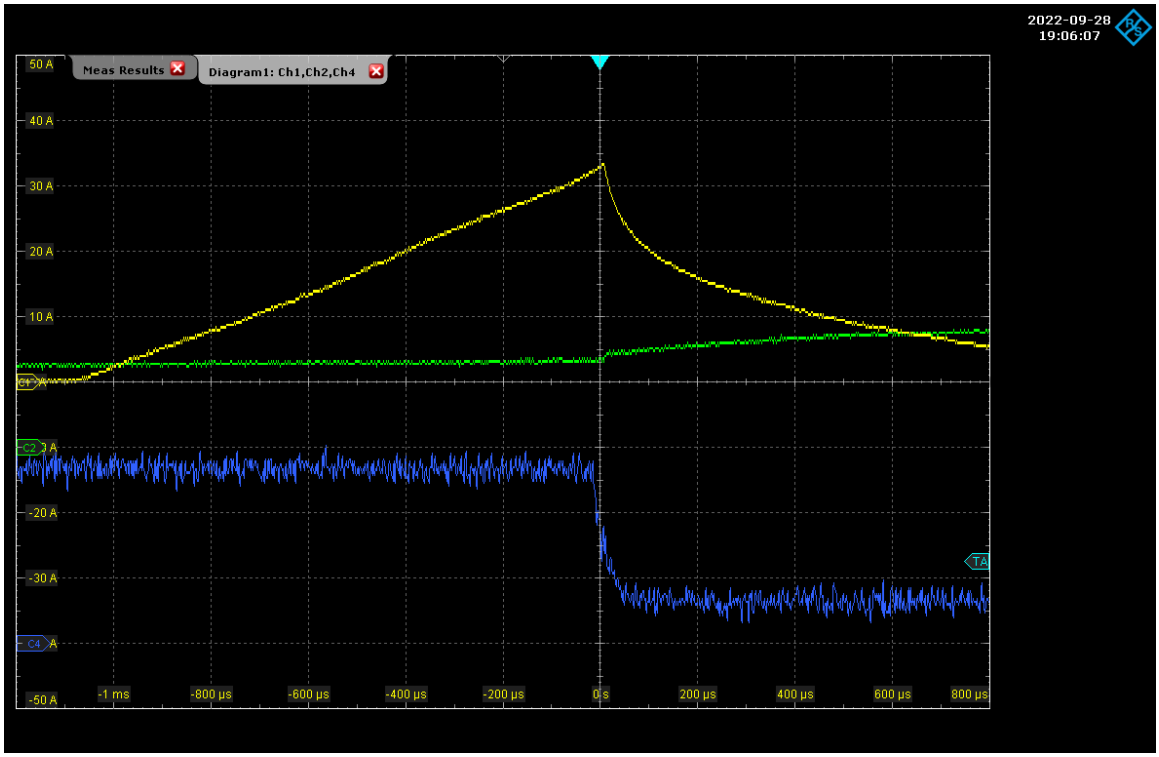


Figure 6.6. System Fault Detection

This capture shows the initial regulation of the DC bus by the bi-directional converter. The commanded voltage exceeds the measured voltage by enough to cause the reference waveform to exceed one (which is the maximum value of the sawtooth carrier). In turn, the low side switch remains shut, and inductor current increases until the Infineon development board issues a fault. The Infineon board is designed to issue this fault at 32 A through a thermal trip [20]. The fault signal is received by the FPGA, which then enters Fault Mode,

as discussed in Section 4.2. The result is the FPGA opens all DC contactors and commands both FETs off.

Since the ESS is capable of driving more current than the Infineon board is designed to carry, a design correction is implemented. If the sensed inductor current exceeds 20 A, the transistors will open until the next switching cycle. The result is shown in Figure 6.7. When the inductor current exceeds 20 A, it begins fluctuating as the protection scheme operates. As the DC bus voltage increases, the inductor current reduces back to 0 A. This occurs without causing the FPGA to enter Fault Mode, and voltage regulation continues uninterrupted.

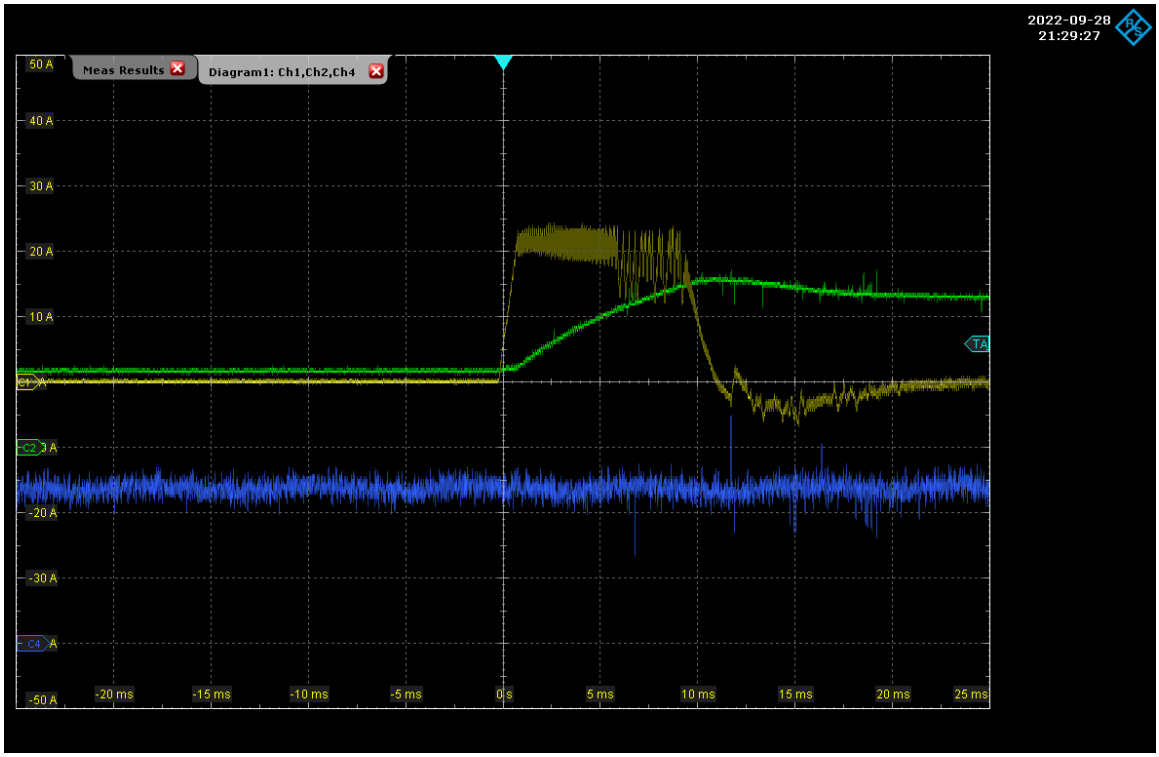


Figure 6.7. Surge Current Design Fix

6.3 Type 1 Voltage

The experimental parameters were increased to demonstrate the ability of the system to meet the pulsed load specifications of [8] while operating at Type 1 voltage. Due to the higher

voltage, the PI controller gains were adjusted down to produce a less aggressive response to a change in load or voltage. The parameters for this experiment are included in Table 6.3.

Table 6.3. Type 1 Experimental Parameters

Component	**Value**
V_{DC}	350 V
V_{BATT}	120 V
LCL Filter Inductors	400 μH
LCL Filter Capacitor	2000 μF
LCL Filter Resistance	1 Ω
Load Resistance (Low)	348 Ω
Load Resistance (High)	69.6 Ω
DC Bus Capacitance	2400 μF
Outer Loop K_p	2.6
Outer Loop K_i	18.7
Inner Loop K_p	0.2
Inner Loop K_i	2.0

In this experiment, the load is only pulsed once, so there is only a low resistance and a high resistance. The resulting power produced from the VSI is shown in Figure 6.8. The steps implemented in this experiment are shown in Table 6.4. The rise in power at t=2.5s is caused by the VSI shifting from zero power to meeting the power of the DC load (Low). The pulse from 4.5s to 6.5s maintains the VSI in power-correcting mode while stepping the load from low to high and subsequently high to low. The same post-processing of the data is done as described in Section 6.1. The experimental measurements presented demonstrate that the system is able to meet the pulsed load limits while operating at Type 1 voltage.

Table 6.4. Power Flow Experiment Stages.

Stage Number	Time Duration [s]	Load	VSI Status
1	0.0 - 2.5	Low	Off
2	2.5 - 4.5	Low	Power Correcting
3	4.5 - 6.5	High	Power Correcting
4	6.5 - 10	Low	Power Correcting

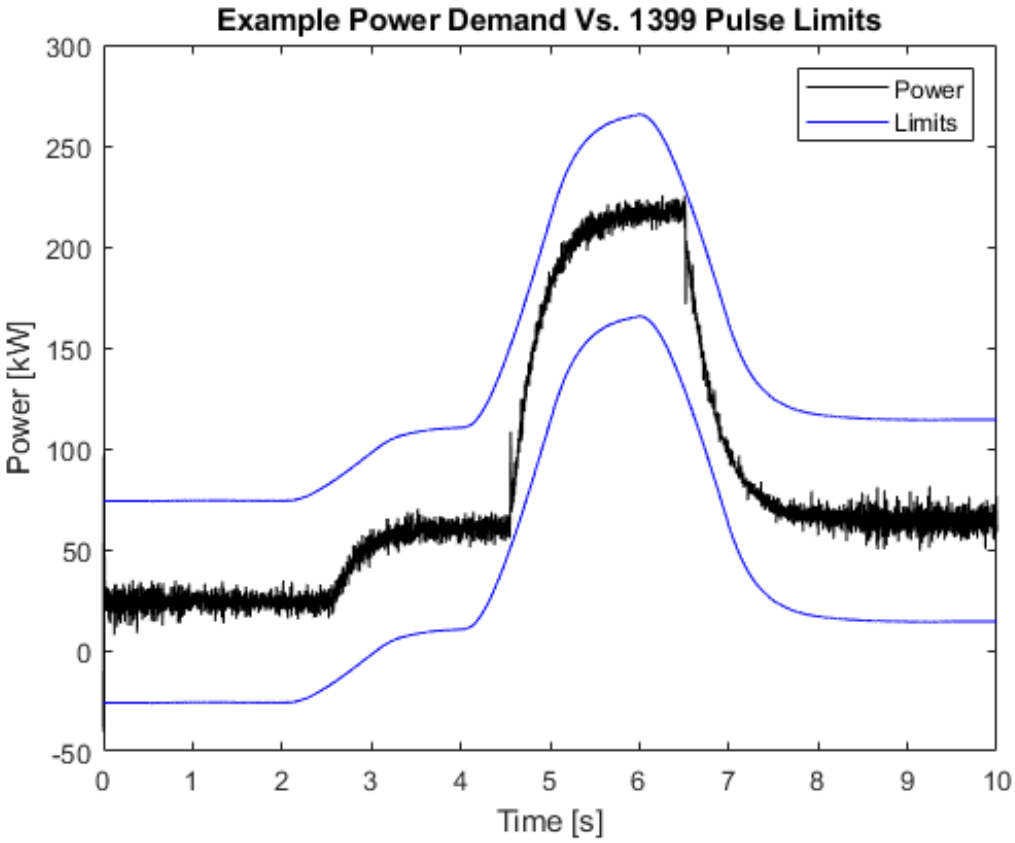


Figure 6.8. Pulsed Load Under Type 1 Voltage

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CHAPTER 7:
Conclusions and Future Work

7.1 Conclusions

This thesis presents a system-level solution to mitigate the transients caused by large, immediate changes in electrical loading on power distribution systems. The result is important because shipboard power distribution systems operate at a much lower power and are far more compact than those found on land-based residential, commercial and industrial applications. A lower power rating for a power distribution network will cause the electrical generators to be more susceptible to voltage and frequency variation in the presence of pulsed power loads. The 2018 revision of MIL-STD-1399 section 300 includes strict requirements to limit the disturbance caused by pulsed power loads on the shipboard power distribution system.

The physics-based models and laboratory experiments presented in this thesis demonstrate that through the use of an ESS, switch-mode DC-DC power converter, and an engineered control scheme, the undesired effects of large, pulsed loads may be mitigated. The results specifically demonstrate that the proposed control scheme was effective at reducing power disturbances caused by a pulsed load to the limits specified in MIL-STD-1399 [8].

7.2 Future Work

Future work could progress in a large number of very different aspects. Whereas the ESS used in this paper contains lead acid batteries for energy storage, a super capacitor could be used as an alternative to analyze system response. Another opportunity for future research includes analyzing the DC-DC converter control system transfer function of either the inner loop or outer loop controller. The use of PI controllers is only one solution, and alternative transfer functions could be analyzed. Finally, the problem of conducted electromagnetic emissions could be explored by controlling the bi-directional boost converter in a manner that could reduce these emissions without passive components like inductors or capacitors.

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