Editorial

Memristive Devices and Systems: Modeling, Properties and Applications

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1. Introduction

The memristor is considered to be a promising candidate for next-generation computing systems due to its nonvolatility, high density, low power, nanoscale geometry, nonlinearity, binary/multiple memory capacity, and negative differential resistance. Novel computing architectures/systems based on memristors have shown great potential to replace the traditional von Neumann computing architecture, which faces data movement challenges. As the field of materials science continues to develop, novel preparation and modeling methods for different memristive devices have been recently put forward, which opens up a new path for realizing different computing systems/architectures with practical memristor properties. The purpose of this Special Issue on "Memristive Devices and Systems: Modeling, Properties and Applications" is to provide a comprehensive overview of key computational primitives enabled by these memory devices, as well as their applications in spanning edge computing, signal processing, optimization, machine learning, deep learning, stochastic computing, and so on. More specifically, we invited researchers and practitioners to contribute original research articles that examine challenges that are related, but not limited to, the following topics:

- Memristive device preparation;
- Memristive device modeling and analysis;
- Novel electronic devices that show memristive properties;
- Novel memristive circuit design solutions for neuromorphic systems;
- Memristive circuit fault diagnosis and analysis;
- Memristive systems for different applications (e.g., edge computing, signal processing, optimization, machine learning, deep learning, and stochastic computing);
- Nonvolatile memory solutions with computing capabilities;
- Memory devices and systems for in-memory computing.

2. Short Presentation of the Papers

Ji et al. [1] analyze the mathematical models of memristors and discuss their applications in conventional image processing based on memristive systems, as well as in image processing based on memristive neural networks, to investigate the potential of memristive systems in image processing. In addition, they present recent advances and implications of memristive system-based image processing comprehensively, and explore development opportunities and challenges in different major areas as well. By establishing a complete spectrum of image processing technologies based on memristive systems, this review attempts to provide a reference for future studies in the field, and it is hoped that scholars can promote development in this area through interdisciplinary academic exchanges and cooperation.

Romero et al. [2] gathered together the current main alternatives presented in the literature for the emulation of both memcapacitors and meminductors. Different circuit emulators have been thoroughly analyzed and compared in detail, providing a wide range of approaches that could be considered for the implementation of these devices in future designs.

Wang et al. [3] develop an optoelectronic memristor model (containing a mathematical model and circuit model). Moreover, they discuss the composite memristor circuit (series- and parallel-connected configuration) with a rotation mechanism. Further, a multi-valued logic circuit is designed, which is capable of performing multiple logic functions from 0–1, verifying the validity and effectiveness of the established memristor model, as well as opening up a new path for the circuit implementation of fuzzy logic.

Qiu et al. [4] present a novel two-neuron-based memristive Hopfield neural network with a hyperbolic memristor that emulates synaptic crosstalk. The dynamics of the neural networks with varying memristive parameters and crosstalk weights are analyzed via the phase portraits, time-domain waveforms, bifurcation diagrams, and basin of attraction. Complex phenomena, especially coexisting dynamics, chaos, and transient chaos emerge in the neural network. Finally, the circuit simulation results verify the effectiveness of theoretical analyses and mathematical simulation and further illustrate the feasibility of the two-neuron-based memristive Hopfield neural network hardware.

Li et al. [5] propose a globally passive but locally active memristor, which has three stable equilibrium points and two unstable equilibrium points, exhibiting two stable locally active regions and four unstable locally active regions. They found that when the memristor operates in a stable local active region, the memristor-based second-order circuit with a parallel capacitor or a series inductor can produce periodic oscillation. Moreover, the memristor-based third-order circuit with two energy storage elements, a capacitor and an inductor, can produce complex chaotic oscillation, forming the simplest chaotic circuit.

Ying et al. [6] propose a modified Chua corsage memristor endowed with two symmetrical locally active domains. Under the DC bias voltage in the locally active domains, the memristor with an inductor can construct a second-order circuit to generate periodic oscillation. Based on the theories of the edge of chaos and local activity, the oscillation mechanism of the symmetrical periodic oscillations of the circuit is revealed. The third-order memristor circuit is constructed by adding a passive capacitor in parallel with the memristor in the second-order circuit, where symmetrical periodic oscillations and symmetrical chaos emerge either on or near the edge-of-chaos domains. The oscillation mechanisms of the memristor-based circuits are analyzed via domain distribution maps, which include the division of locally passive domains, locally active domains, and the edge-of-chaos domains. Finally, the symmetrical dynamic characteristics are investigated via theory and simulations, including Lyapunov exponents, bifurcation diagrams, and dynamic maps.

Qin et al. [7] investigate a fractional-order memristive model with infinite coexisting attractors. The numerical solution of the system is derived based on the Adomian decomposition method (ADM), and its dynamic behaviors are analyzed by means of phase diagrams, bifurcation diagrams, the Lyapunov exponent spectrum (LES), and dynamic maps based on SE complexity and the maximum Lyapunov exponent (MLE). Simulation results show that it has rich dynamic characteristics, including asymmetric coexisting attractors with different structures and offset boosting. Finally, the digital signal processor (DSP) implementation verifies the correctness of the solution algorithm and the physical feasibility of the system.

Shen and Wang [8] propose a cellular neural network (CNN) based on a VO2 carbon nanotube memristor. The device is first modeled by SPICE, and then the cell dynamic characteristics based on the device are analyzed. It is pointed out that only when the cell is at the sharp edge of chaos can the cell be successfully awakened after the CNN is formed. In this paper, they provide the example of a 5 × 5 CNN, set specific initial

conditions, and observe the formed pattern. Because the generated patterns are affected by the initial conditions, the cell power supply can be preprogrammed to obtain specific patterns, which can be applied to the future information processing system based on complex space–time patterns, especially in the field of computer vision.

Shen and Wang [9] study the history erase effect of a Hewlett-Packard (HP) TiO2 memristor and the Self-Directed Channel (SDC) memristor of the Knowm Company. The DC and AC responses of the HP TiO2 memristor are given, and it is pointed out that there is no AC history erase effect. However, considering the parasitic memcapacitance effect, it is found that it has the effect. Based on the theoretical model of the SDC memristor, its history erase properties are studied by considering and not considering parasitic effects. It should be noted that this study method can be useful for other materials such as Al_2O_3 and MoS_2.

Quesada et al. [10] analyze and evaluate three different RRAM compact models that are implemented in Verilog-A to reproduce the multilevel approach based on the switching capability of experimental devices. These models are integrated in 1T-1R cells to control their analog behavior by means of the compliance current imposed by the NMOS select transistor. Four different resistance levels are simulated and assessed with experimental verification to account for their multilevel capability. Further, an artificial neural network study is carried out to evaluate in a real scenario the viability of the multilevel approach under study.

Author Contributions: Writing—original draft preparation, C.S.L. and Z.D.; writing—review and editing, D.Q. All authors have read and agreed to the published version of the manuscript.

Conflicts of Interest: The authors declare no conflicts of interest.

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