

Memristive Circuit Design of Sequencer Network for Human Emotion Classification

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Abstract— Mental health problem is an increasingly common social issue leading to diseases such as depression, addiction, and heart attack. Facial expression is one of the most natural and universal signals for human beings to convey their emotional states and behavior intentions. Numerous studies have been conducted on automatic human emotion classification that can effectively establish the relationship between facial expression and mental health, while still suffer from intensive computation and low efficiency. Here, we present a memristive circuit design of Sequencer network for human emotion classification, which offers an environmentally friendly approach with low cost and easily deployable hardware. Specifically, a kind of eco-friendly memristor is fabricated using two-dimensional (2D) materials, and the corresponding testing performance is conducted to make sure its efficiency and stability. Then, the memristor-based Sequencer block, as a core component of Sequencer network, consisting of bidirectional long short-term memory (BiLSTM) circuit and some necessary function circuit modules is proposed. Based on this, the memristive Sequencer network can be achieved. Furthermore, the proposed memristive Sequencer network is applied for human emotion classification. The experimental results demonstrate that the proposed circuit has advantages in computational efficiency and cost, comparable to the main existing software-based methods.

I. INTRODUCTION

Mental health problems are an important and pervasive public health issue leading to diseases such as depression, addiction, and heart attack, which can severely affect quality of life [1]. Early detection of mental health problems is particularly important, since unattended, they can be life-threatening. Facial expression is one of the most natural and universal signals for human beings to convey their emotional states and behavior intentions [2]. Recently, advanced research on artificial intelligence and psychology technology, numerous studies have been conducted on automatic human emotion classification because of its can effectively establish the relationship between facial expression and mental health [3]. Among them, deep learning-based methods have achieved the state-of-the-art recognition accuracy and exceeded previous results in human emotion classification [4-6]. However, these methods based on von Neumann computer architecture still suffer from computationally challenging problems with unattainable energy efficiencies.

In recent computer vision research, a large number of deep neural networks have been proposed to solve complex problems. Sequencer network, one of the most important

models for machine vision, has achieved state-of-the-art image classification performance [7]. However, the Sequencer network has many parameters and complex calculations, which requires computing systems with ‘big data’ transmission capabilities and large computing units [8]. The emerging of the memristor provides a new approach to realize the circuit implementation of Sequencer network, offering benefits in terms of good privacy, low cost, and easily deployable software. As the fourth basic circuit element, memristor was first proposed by L. O. Chua in 1971 [9] and was further associated with physical devices by R. Stanley Williams and his team from Hewlett-Packard Labs in 2008 [10]. With the development of memristor technology, this neuromorphic computing device has been proved effective in the fields of artificial intelligent and image processing. While memristor-based Sequencer network has not been developed due to the complex calculation process and data storage.

In this work, we propose a full circuit implementation of memristive Sequencer network for human emotion classification. With such design concept and deep learning integration, the proposed network can realize human emotion classification for mental health monitoring. The main contributions are briefly summarized as below:

- 1) The Ag-Au/MoSe₂-doped Se/Au-Ag memristor with high stability is prepared. It can serve as a promising candidate to emulate high-accuracy neuromorphic computing in human emotion classification.
- 2) The circuit design of memristor-based Sequencer network is proposed and validated by applying it to human emotion classification, which provides benefits in term of less computational overhead and time consumption.

II. MEMRISTOR FABRICATION AND PERFORMANCE TESTING

A. Fabrication of Ag-Au/MoSe₂-doped Se/Au-Ag Memristor

The Ag-Au/MoSe₂-doped Se/Au-Ag memristor is fabricated based on hydrothermal synthesis method and magnetron sputtering method, in which the former is used to fabricate MoSe₂-doped Se microwires and the latter is used to prepare Ag-Au electrodes, with details as shown in Fig. 1.

Step 1: 0.1mol Se powder and 0.1mol ammonium molybdate (NH₄)₆Mo₇O₂₄·H₂O are dissolved into 25mL deionized water, as labelled solution A.

Step 2: 0.05g surfactant (i.e., hexadecyl trimethyl ammonium bromide) is added to the solution A and continuously sonicated using a magnetic stirrer for 3 hours, as labelled solution B.

Step 3: The solution B is transferred to a 25mL Teflon-lined container and heated at 227°C for 48 hours in a muffle furnace.

Step 4: After 3 times centrifugation operation, MoSe₂-doped Se microwire is obtained from the heated solution B.

Step 5: The Au electrode (space = 400μm, area = 2500μm²) on the Si/SiO₂ substrate is fabricated by using magnetron sputtering method.

Step 6: The MoSe₂-doped Se microwire is picked out using a four-probe test system, the ends of the microwire are embedded in the Au electrode and covered with a layer of Ag adhesive to form the Ag-Au/ MoSe₂-doped Se/Au-Ag memristor.

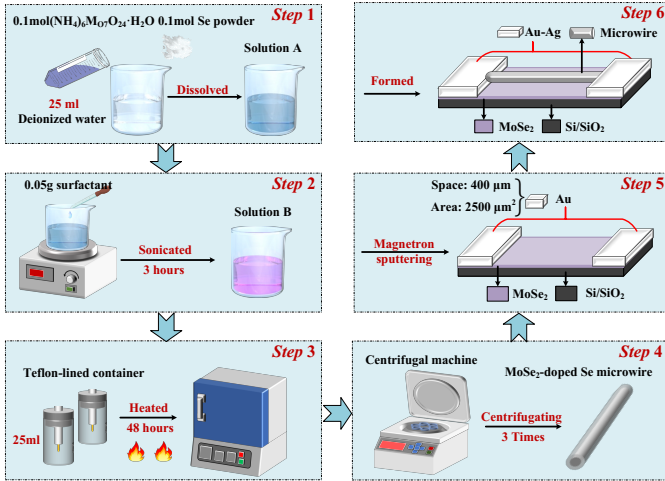


Fig. 1. The fabrication flow of Ag-Au/MoSe₂-doped Se/Au-Ag memristor

B. Performance Testing

The performance testing of Ag-Au/ MoSe₂-doped Se/Au-Ag memristor is carried out through an electrochemical workstation CHI-600D. The electrical characteristics are measured with $\pm 3V$ scanning voltages scan rate of 0.05V/s, as shown in Fig. 2.

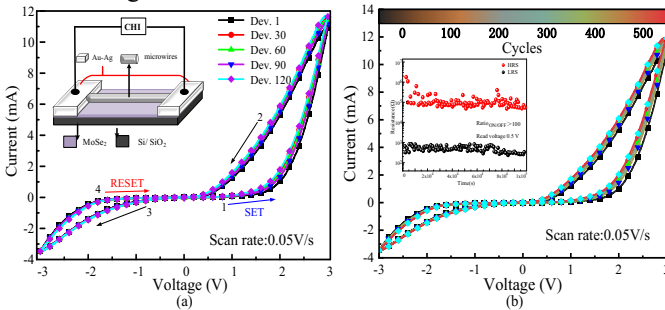


Fig. 2 The performance testing of Ag-Au/ MoSe₂-doped Se/Au-Ag (a) device-to-device analysis; (b) cycle-to-cycle analysis

From Fig. 2(a), the measured I-V curves obtained by 120 memristors show a high degree of overlap, and the inset is a structural representation of the fabricated memristor. The testing results demonstrating that the Ag-Au/ MoSe₂-doped Se/Au-Ag memristors have good device-to-device stability. The overall I-V curves are asymmetrical in the positive and negative voltage regions, indicating that the fabricated memristors exhibit electronic resistive switching memory

(ERSM) behavior. Specifically, in the first stage, the memristors keep in the high resistance state (HRS) at beginning. As the scanning voltages increase from 0V to 3V, the devices currents are almost unchanged until the scanning voltages exceed 1.5V, the devices currents start to increase and reach a maximum at 3V, meaning that the “SET” process is completed; in second and third stages, the memristors remain in low resistance state (LRS) when the scanning voltages decrease from 3V to -3V; in fourth stage, the current gradually decreases as the scanning voltage changes from -3V to 0V. When the scanning voltage is higher than -1.5V, the memristor changes from LRS to HRS, meaning that the “RESET” process is completed.

To investigate the stability of the memristor, the I-V curves for the 1st, 10th, 50th, 200th and 500th cycles are measured, and the inset is the resistance variation curve with the 0.5V reading voltage for 10⁵ seconds. It can be seen that the high degree of overlap in I-V curves and the resistance ratio between the HRS and LRS can be maintained well, indicating the good stability of the fabricated memristor.

III. CIRCUIT DESIGN OF MEMRISTIVE SEQUENCER NETWORK

According to [7], Visual Transformer (ViT) and its variants based on self-attention module have been proved effective in many computers vision tasks. Several works have tried to replace the self-attention module with different other modules (e.g., the global filter) [11]. Following this trend, Sequencer network replaces the self-attention layer with BiLSTM, the specific structure of Sequencer network can be seen in Fig. 3:

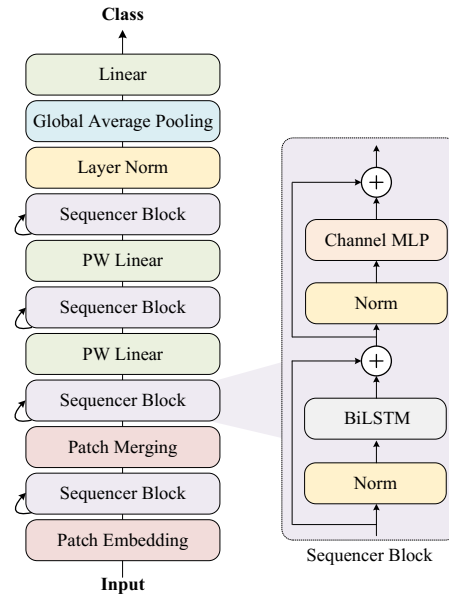


Fig. 3: The structure of Sequencer network

From Fig. 3, the Sequencer network can be roughly divided into two parts, i.e., the Sequencer block and the other necessary function modules (e.g., the PW linear module). In particular, the BiLSTM cell is the key to realize the Sequencer block. Based on this, we illustrate the circuit design of Sequencer network from the “circuit design of BiLSTM cell”.

A. Circuit design of BiLSTM cell

LSTM is a kind of recurrent neural networks (RNNs) for modelling long-term dependencies of sequence without

worrying about the gradient vanishing and exploding issues. A standard LSTM cell has three gates, i.e., the input gate, the forget gate, and the output gate. Notably, the input gate i_t controls the storage of input x_t , the forget gate f_t decides which information to be discarded from the previous cell state c_{t-1} , and the output gate o_t controls the cell output h_t from the current cell state c_t . The mathematical expression of LSTM is given below:

$$\begin{bmatrix} a_t \\ i_t \\ f_t \\ o_t \end{bmatrix} = \begin{bmatrix} W_a & U_a & b_a \\ W_i & U_i & b_i \\ W_f & U_f & b_f \\ W_o & U_o & b_o \end{bmatrix} \begin{bmatrix} x_t \\ h_{t-1} \\ 1 \end{bmatrix} \quad (1)$$

$$c_t = \sigma(i_t) \odot \tanh(a_t) + \sigma(f_t) \odot c_{t-1} \quad (2)$$

$$h_t = \sigma(o_t) \odot \tanh(c_t)$$

where W (W_a, W_i, W_f, W_o), U (U_a, U_i, U_f, U_o), and b (b_a, b_i, b_f, b_o) are the weight, recurrent weight, and bias of LSTM, respectively. Symbol σ denotes the logistic sigmoid and \odot is Hadamard product.

A BiLSTM consists of two parallel LSTM layers: one takes the input in a forward direction (i.e., LSTM_{forward}), while the other takes it in a backward direction (i.e., LSTM_{backward}). Specifically, we assume \vec{x} be the input series, and \overleftarrow{x} is the corresponding rearrangement of \vec{x} in reverse order. Then, the outputs of these two LSTM layers can be written by:

$$\begin{cases} \vec{h}_{forward} = \text{LSTM}_{forward}(\vec{x}) \\ \overleftarrow{h}_{backward} = \text{LSTM}_{backward}(\overleftarrow{x}) \end{cases} \quad (3)$$

We let the $\vec{h}_{backward}$ be the rearrangement of $\overleftarrow{h}_{backward}$ in the normal order, the final output of BiLSTM can be written by:

$$h = \text{concatenate}(\vec{h}_{forward}, \vec{h}_{backward}) \quad (4)$$

Based on Eqs. (1) ~ (4), the specific circuit design of BiLSTM is illustrated in Fig. 4.

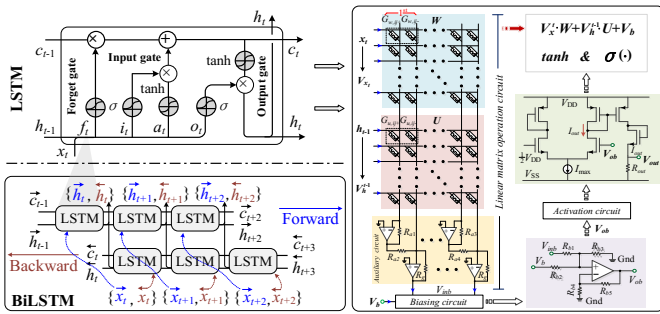


Fig. 4: The BiLSTM structure and its circuit design

From Fig. 4, the fundamental component of BiLSTM structure is the standard LSTM, which means the LSTM circuit design and implementation are very important. Notably, the specific hardware implementation of LSTM can be separated into two components, i.e., the linear matrix operation circuit and the nonlinear activation circuit.

B. Circuit Design of Sequencer Network

Notably, the Sequencer block is the core module of the Sequencer network (need four Sequencer blocks). Based on the BiLSTM circuit module, the circuit design of Sequencer block is provided in Fig. 5:

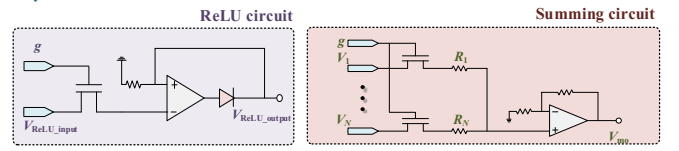
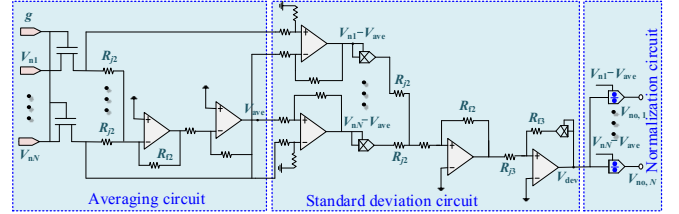
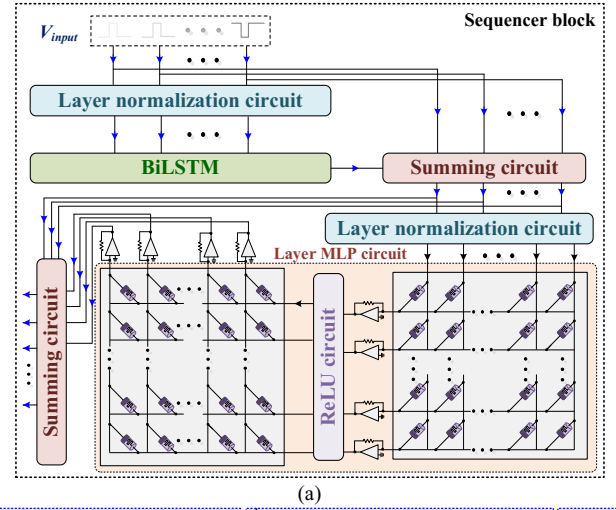


Fig. 5: The circuit design of Sequencer block. (a) The schematic diagram. (b) The necessary function circuit modules.

From Fig. 5(a), the Sequencer block circuit is composed by many necessary function circuit modules, including the layer MLP circuit module, the layer normalization circuit module, the summing circuit module, the BiLSTM circuit module (illustrated in Section III-A), and the ReLU circuit module. The corresponding circuit diagrams are provided in Fig. 5(b).

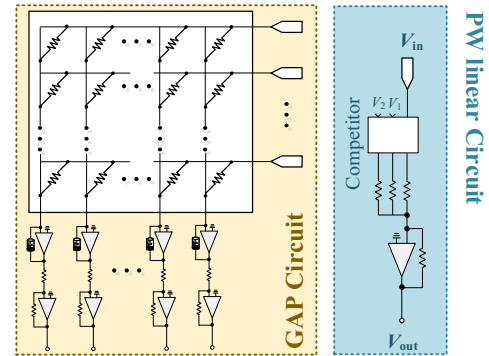


Fig. 6: The circuit design of other necessary function modules

Furthermore, Fig. 6 provides the global average pooling (GAP) circuit module [12] and piece-wise (PW) linear circuit module. It is noted that the input and output signals of all these function circuit modules are voltages, which guarantees that all these modules can be connected in cascaded configuration. Based on this, the circuit design of Sequencer network can be obtained.

IV. APPLICATION IN HUMAN EMOTION CLASSIFICATION

For verification, the proposed memristive Sequencer network can be applied to human emotion classification. The specific algorithm flow is provided in Fig. 7:

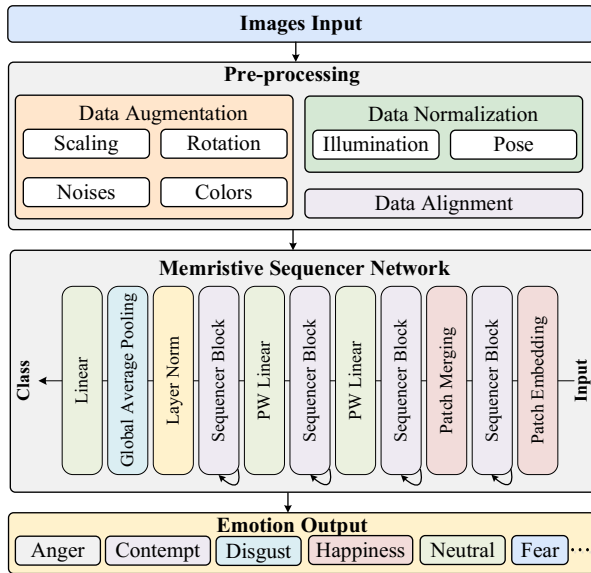


Fig. 7: The pipeline of the human emotion classification

During the classification process, we use the FER-2013 dataset and CK+ [3] dataset as the input images. Then, some necessary pre-processing operations (e.g., the data alignment, data augmentation, and data normalization) are carried out. Next, all the input images can be converted to the normalized voltage signals. These voltage signals are further injected to the memristive Sequencer network (execute training and testing). the output result can classify different human emotions (i.e., Anger, contempt, disgust, happiness, neutral, fear and so forth). Notably, the entire process can be divided into two parts, i.e., the feedforward computation and back propagation. the feedforward computation is carried out in the memristive Sequencer network, the back propagation (mainly referring to the weight updating) is performed on MATLAB 2018b. The results are provided in Table 1.

Table 1: The initial results of human emotion classification

Methods	CK+	FER-2013	Mean time
	Accuracy	Accuracy	
Our work	92.3%	72.3%	125.4 Sec
Reference [4]	96.8%	75.2%	2013.7 Sec
Reference [6]	96.7%	73.7%	2252.7 Sec
Sequencer [7]	92.4%	72.5%	2335.9 Sec

From Table 1, although the proposed system has an inferior performance (in accuracy) as compared with the soft-based methods, the difference can be accepted. Meanwhile, considering the speed advantage brought by the hardware implementation of Sequencer network, the proposed system has benefits in computational efficiency and cost (the minimum running time).

V. CONCLUSIONS

In this work, we investigate the circuit design of memristive Sequencer network for human emotion classification. Firstly, a kind of eco-friendly memristor is fabricated using two-

dimensional (2D) materials, and the corresponding testing performance is conducted to make sure its efficiency and stability. Then, the memristor-based Sequencer block consisting of bidirectional long short-term memory (BiLSTM) circuit module, layer normalization circuit module, summing circuit module, and ReLU circuit module is proposed. Based on this, the circuit design of memristive Sequencer network can be achieved after combining some other necessary function circuit modules (i.e., the AGP circuit module and PW linear circuit module). Furthermore, the proposed memristive Sequencer network is applied for human emotion classification. The experimental results demonstrate that the proposed system has advantages in computational efficiency and cost, comparable to existing software-based methods.

ACKNOWLEDGMENT

This work was jointly supported by the National Natural Science Foundation of China (grant no. 62001149) and the Natural Science Foundation of Zhejiang Province (grant no. LQ21F010009).

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