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Characterization of Active Device through Load-pull for Wideband Applications Using CAD Tool Based Simulator

Caracterização de Dispositivo Ativo através de Load-pull para Aplicações de Banda Larga usando Simulador Baseado em CAD

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Dissertação apresentada à Universidade de Aveiro para cumprimento dos requesitos necessários à obtenção do grau de Mestre em Engenharia Eletrónica e Telecomunicações, realizada sob a orientação científica do Doutor Nuno Borges de Carvalho, Professor do Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro.

Dissertation presented to the University of Aveiro to fulfil the necessary requirements to obtain the degree of Master in Electronics and Telecommunications Engineering, developed under the scientific guidance of Professor Nuno Borges de Carvalho, of the Department of Electronics, Telecommunication and Informatics of the University of Aveiro.

o júri / the jury

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palavras-chave Amplificadores de potência, Caracterização load-pull, Efeitos de memória, Tecnologia sem fios

Resumo

Com a evolução das aplicações de tecnologias de comunicações, é esperado que os sitemas de telecomunicações sem fios sejam mais robustos e eficazes a nivel de performance/custo. Conforme um inquérito de mercado, o tráfego de dados está a evoluir em conjunto com as aplicações de tecnologia e é esperado que em 2030 tenha aumentado até às centenas de Exabytes por mês. Para suportar quantidades de tráfego tão grandes, são esperados transrecetores com apoio para larguras de banda maiores, eficiência espectral e de potência. No processo digital interno das comunicações sem fios, os esquemas de modulação tornam-se mais complexos para melhorar a taxa de dados. Contudo, nas comunicações sem fios, a qualidade de serviços é maioritariamente determindada pela camada física, especialmente por componentes tais como os amplificadores de potência. Considerando este facto, nesta dissertação, a caracterização do dispositivo ativo através do processo de load-pull é estudada para o entendimento do comportamento no cenário de aumento de banda larga. Load-pull é realizado com tecnologia LDMOS e GaN com o uso de ferramentas de desenho assistido (CAD) tais como advanced design system (ADS). A impedância de banda base também é estudada com análise de dois tons para estudar o efeito de memória que causa degradação na linearidade e eficiência.

keywords Load-pull characterization, Memory effect, Power amplifiers, Wireless technology

Abstract With the evolution of communication technology applications, wireless telecommunication systems are expected to be more and more robust and performance/cost effective. As per the market survey, data traffic is evolving with the technology applications and is expected to go up to 100s of Exabyte/month by 2030. To support such high data traffic, wireless transceivers are expected with larger bandwidth, high spectral and power efficiency support. On the digital back-ends of the wireless communication, modulations schemes become more and more complex to improve the data rates. However, in the wireless communication, quality of services (QoS) is majorly determined by the physical layer, especially by components such as power amplifiers. With considering this fact, in this dissertation, characterization of the active device through the load-pull process is studied for understanding the behavior of increased wideband scenario. Load-pull is performed with LDMOS and GaN technology using computer-aided design tool (CAD) such as advanced design system (ADS). Baseband impedance is also studied with the two-tone analysis to study the memory effect that causes the degradation in linearity and efficiency.

Contents

List of Figures

List of Tables

Acronyms

ACPR Adjacent Channel Power Ration.

ADS Advanced Design System.

ADT Active Device Technology.

AM Amplitude Modulation.

AMPS advanced mobile phone system.

ASK Amplitude Shift Keying.

BJT Bipolar Junction Transistor.

BPSK Binary Phase Shift Keying.

CAD Computer-Aided Design.

CW Continuous Wave.

DC Direct Current.

DC-IV Direct Current to Current Voltage.

DUT Device Under Test.

EMT Electromechanical Tuners.

ETS Electronic Tuners.

EVM Error Vector Magnitude.

FDM Frequency Division Multiplexing.

FM Frequency Modulation.

FoM Figure of Merit.

FSK Frequency Shift Keying.

GaAs Gallium Arsenide.

GaN Gallium Nitride.

GPRS General Packet Radio Service.

HBT Heterojunction Bipolar Transistor.

IMD Intermodulation Distortion.

IMD3 Third Order Intermodulation Distortion.

IMD5 Fifth Order Intermodulation Distortion.

IQ In-phase Quadrature.

LDMOS Laterally-Diffused Metal-Oxide Semiconductor.

LTE Long Term Evolution.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

NF Noise Factor.

NMT Nordic Mobile Telephone.

OFDM Orthogonal Frequency Division Multiplexing.

P1dB 1db Compression point.

PA Power Amplifier.

PAE Power Added Efficiency.

PAPR Peak-to-Average Power Ration.

PM Phase Modulation.

PWM Pulse Width Modulation.

QAM Quadrature Amplitude Modulation.

QPSK Quadrature Phase Shift Keying.

RF Radio Frequency.

SC-FDMA Single-Carrier Frequency Division Multiple Access.

SNR Signal to Noise Ratio.

TACS Total Access Communication System.

UMTS Universal Mobile Telecommunications Service.

Chapter 1

Introduction

1.1 Background and Motivation

Over the years, telecommunication technologies have been subject of an incredible evolution and improvement for advanced communication applications. The first generation (1G) of mobile networks dates back to the 1980s and is composed of advanced mobile phone system (AMPS), total access communication system (TACS), and nordic mobile telephone (NMT) technologies. These were developed without data services and were mainly targeting voice calls. To facilitate data services, second generation (2G) was introduced in the 90s and it was the first digital mobile network. It added the functions of sending texts and roaming. Around 1997 several updates followed with a specific improvement called general packet radio service (GPRS) with data services. However, the data transfer wasn't continuous with the limited data rates of 100s of kbps. With 3G, UMTS (Universal Mobile Telecommunications Service) were put in place and provided faster data rates with the use of packet switching. Together with 4G-LTE (Long Term Evolution) it provides a faster internet access. Nowadays, the race for evolution in telecommunication is for the higher data rate and for support of higher data traffic over wider bandwidth.

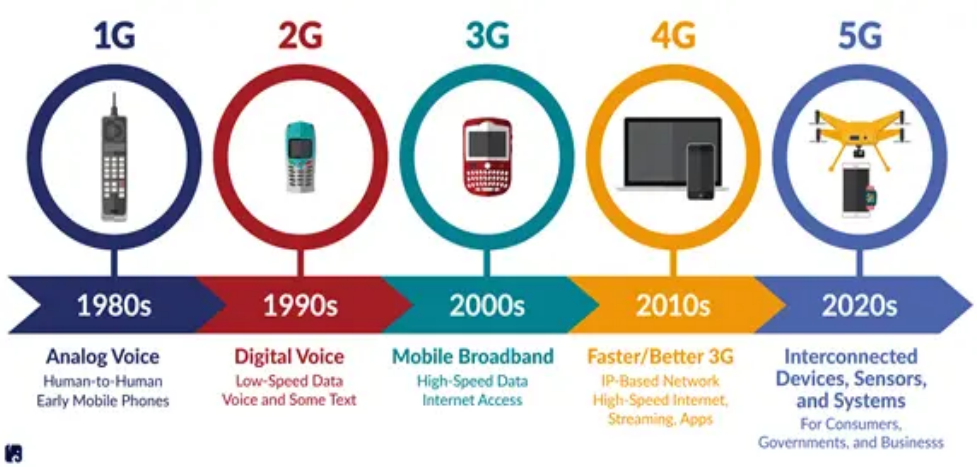


Figure 1.1: Telecommunication generation evolution [1]

On the digital end, modulation scheme also evolved from analog to digital modulation to

support the demand of efficient ways for distant communication. Data needs to be modulated into a signal that can be transmitted, received and processed over an RF system with more information over limited bandwidth standards.

Modulation started with three basic analog modulation schemes adapted by 1G and early 2G telecommunication systems. It is categorised by amplitude modulation (AM), frequency modulation (FM) and phase modulation (PM). The amplitude, phase, and frequency are three quantities that can be varied in proportion to the modulated signal. The first scheme is called amplitude modulation and the second two are called angle modulation schemes (frequency and phase modulation). It provides more efficient long distance communication but still limited to the data rates and spectral efficiency. This leads the communication to the digital modulations. Digital modulation, such as, amplitude shift keying (ASK), frequency shift keying (FSK), and phase shift keying with two types called binary phase shift keying (BPSK) and quadrature phase shift keying (QPSK) are adapted by 3G to reach higher data transmission rate over limited bandwidth at a cost of complex time domain statistics.

Digital modulation evolved further to quadrature amplitude modulation (QAM) also called IQ modulation, which uses both amplitude and phase in order to modulate the desired signal. It is composed of two signals, one "in-phase", I, and the other in "quadrature", Q, which is shifted by 90^{o} when compared to the in-phase signal. Since the data is normally binary, the number of points in a constellation will be a power of 2 (4, 16, 64, etc) giving place to 4-QAM, 16-QAM, ..., 256-QAM, etc. Using more points per constellation has the advantage of more bits being carried per symbol but that also means that every symbol is closer together leading to a system more prone to interference.

Furthermore, Frequency Division Multiplexing (FDM) is a modulation scheme also introduced that overlaps signal without interference in different sets of frequency over the bandwidth becomes a key modulation scheme to the new 3G to 4G-LTE for more efficient spectral usage [2]-[4]. This evolved with two further most advanced modulation schemes, such as single-carrier frequency division multiple access (SC-FDMA) and orthogonal frequency division multiplexing (OFDM). These improve spectral efficiency and data rates drastically over constant bandwidth [4]-[8]. Further evolution of the modulation towards 5G and beyond makes information signal more and more complex in terms of the time domain statistics. This increases the peak-to-average power ration (PAPR) and hence reduces the dynamic range of the wireless hardware. Figure 1.1 summarizes how telecommunications evolved over the years from 1G to 5G. 6G is now being studied and is expected to enhance some capabilities such as data rates, latency and efficiency. With higher data rates, it is important that energy consumption increase is controlled. Expectations for 6G are bigger than for the previous 5G and modulation schemes and technology have to accompany these demands.

As telecommunication networks evolve, power amplifiers need to accompany these changes by providing more power and having more spectral efficiency while keeping a linear performance in the wireless transceivers.

1.2 Dissertation Objective

With increasing modulation scheme complexity time domain dynamics of the modulated signal become more complex in terms of the signal statistics. This leads to other figures of merit that need to be considered such as PAPR.

This impacts the power amplifier by the linearity and efficiency trade-off over the modu-

lation bandwidth. Efficiency and linearity are two of the most important characteristics in a PA. Linearity is directly related to the spectral leakage and information quality of services, whereas power efficiency is directly related to the power consumption of the base stations and user equipment. This trade-off is also reflected from the PA operation mode. And hence, load-pull of the active device technology gives early stage experimental characterization without the advanced design stage. The goal of this thesis is to understand the load-pull characterization for the wideband applications with simple to more advanced characterization of the memory effects.

1.3 Dissertation Organization

This dissertation is organized in 4 chapters as follow:

Chapter 1 introduces how telecommunications have developed over the years and the type of modulation schemes that followed that development. PA as a part of wireless network and its role in quality of service is explained as well. At the end the objective for the work done in this dissertation is explained.

Chapter 2 gives a theoretical background of power amplifiers like DC-IV characterization and PA classes and introduces the concept of load-pull as well as its features and hardware set up. Lastly it describes some important figures of merit (FoM) of the PAs.

Chapter 3 displays all the simulation work starting with DC-IV characterization for LDMOS and GaN technologies and then moving to load-pull analysis, load-pull characterization over a wide band and a 2-tone load-pull for LDMOS followed by the impact of baseband impedance on PA.

The dissertation is complete with *Chapter 4* which gathers the conclusions from the simulation work done and possible future work.

Chapter 2

Basics of Power Amplifiers

2.1 Introduction

In this chapter, power amplifier design and its characterization aspects are discussed in detail. After the selection of the active device technology (ADT) according to the application, power amplifier design is mainly divided into four stages: first, DC-IV characteristics study, that helps to decide the biasing point, DC power consumption, and load-line. Second, source/load-pull characterization, that characterizes the ADT with more advanced figure of merits in early design stage followed by the third stage, which is the biasing network design. And the final stage is the matching of the circuit according to the fundamental and harmonic frequency termination. Load-pull characterization of the ADT is discussed with more details.

2.2 Active Device Technologies Used in Major PA Design

HBT: Heterojunction Bipolar Transistor (HBT) are a type of Bipolar Junction Transistor (BJT). What distinguishes them is that HBT uses different types of materials for the base and emmiter junctions, hence the name 'heterojunction'. The reason to use HBT transistors over the normal BJT is that they are capable of working in the hundreds of GHz. The collector-base junction is reversed biased and the base-emitter is forward biased junction and when there is disruption, the electrons go from the emitter to the base of the transistor.

GaAs: Gallium Arsenide (GaAs) is a wide direct band gap semiconductor. It shares the same advantages as GaN, such as smaller devices, faster switching speed and lower cost of production, since it is a wide band gap semiconductor. In addition, and because it is a direct band gap semiconductor, it absorbs and emits light more efficiently than silicon. GaAs transistors are capable of working in the hundreds of GHz.

LDMOS: Laterally-Diffused Metal-Oxide (LDMOS) are RF power Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) used in high power applications working at high frequencies. Compared to GaAs transistors, they are more reliable and have a better RF performance. LDMOS show high breakdown voltage meaning they can have higher input voltage resulting in higher voltage at the output.

GaN: Gallium Nitride (GaN) is a wide band gap semiconductor and for that reason, GaN devices are smaller, meaning more amount of transistors in the same area or smaller components. They provide faster switching speed, resulting in faster devices, and cost less to produce than silicon based transistors. Devices made out of GaN also work at higher

frequencies, voltages and temperatures making them more energy efficient.

2.3 DC-IV Characterization

DC-IV characteristics is performed when applying DC supply to the ADT and measuring output voltage (Vds) and current (Ids) characteristics. In the following subsections, biasing condition and mode of operation of the PA is explain in more detail followed by a subsection that describes the load-line theory as a beginner approach to the optimum load condition selection.

2.3.1 Biasing Point and Mode of Operation for PA

Biasing consists on setting fixed operating conditions (voltage or current) that determine the mode of operation of an active device such as a PA. This biasing point is called quiescent point or Q-point and is obtained from the DC-IV characteristics shown in Figure 2.1. The Q-point is located somewhere along the load-line which intersects the vertical axis at the saturation point and the horizontal axis at the cut off point.

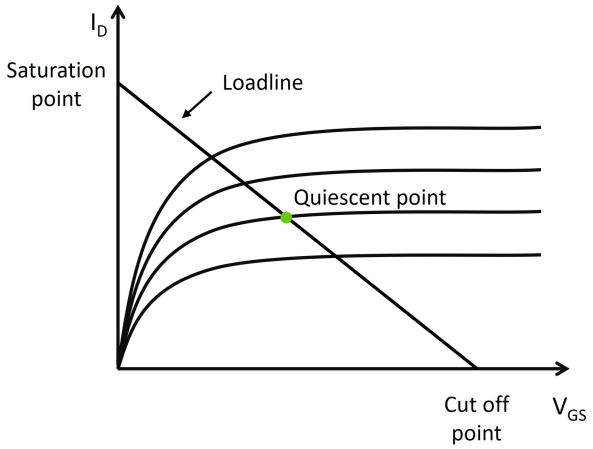


Figure 2.1: Quiescent Point

The operation mode for power amplifiers can be divided into three categories as shown in Figure 2.2. A linear mode of PA is an amplifier in which the output is linearly related to the input power. Digital and switching mode PAs are nonlinear and work with digital signals as opposed to linear PAs.

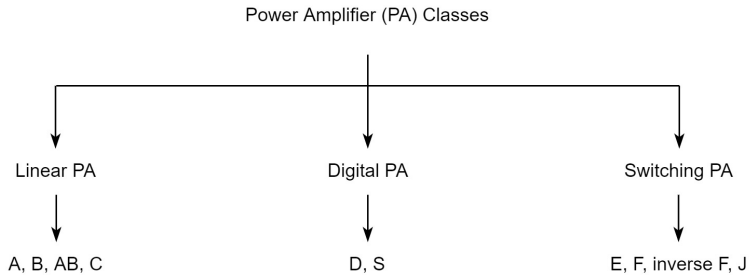


Figure 2.2: Power Amplifier classes

The class A amplifier conducts current over the full cycle of the signal (conduction angle of 360^{o}) without going to off mode. The conduction angle corresponds to the amount of degrees in which the PA will conduct. It is an extremely linear amplifier, has a high gain and low signal distortion but has the lowest efficiency since it loses performance through heat. The quiescent point for this class is normally about half way between the saturation point and the cut off point. In the class B amplifier, the active device only conducts through half of the cycle. As a result, there are losses only during half of the cycle, making this class more efficient and less prone to heating compared class A at a cost of linearity [9]. The quiescent point in this case, is at the cut off point.

The class AB amplifier combines class A and class B amplifiers operations to have the benefits of the linearity of class A and the efficiency of class B. The active devices in the amplifier conduct just over a half cycle meaning that the conduction angle can go from 180^{o} to 360^{o}. The quiescent point for this class, is between the half way point of the load-line and the cut off point.The class C amplifier has the highest efficiency when compared to the classes mentioned before but as consequence is the least linear. The transistor conducts for less than half of the cycle which results in higher efficiency but also adds heavy distortion in the output signal. The conduction angle is less than 180^{o} and the quiescent point is bellow the cut off point.

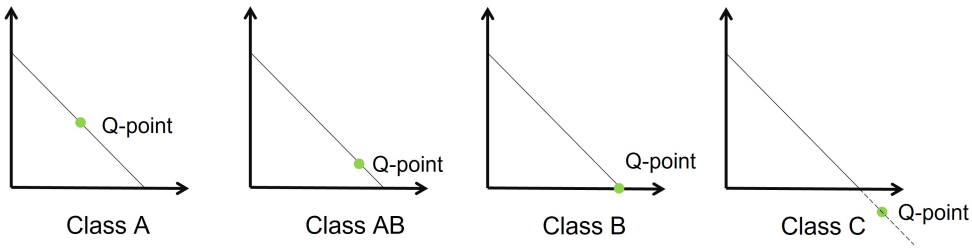


Figure 2.3: Q-point for classes A, AB, B and C

In the class D amplifier, the analogue input is converted into a PWM (Pulse Width Modulation) signal and decoded back into analogue signal at the output. There are only two states, ON and OFF and in theory there is no power dissipation leading to nearly 100% of efficiency. The class S amplifier is very similar to a class D-E-S amplifier in the way that it modulates the input signal into a PWM signal. They are very efficient since there is little dissipation of power. Digital and switching mode PA is usually operated in class B biasing conditions.

A class F amplifier uses harmonic resonators at the output network so that the output signal is a square waveform. In theory, the efficiency for this class could reach 100% but that would mean infinite harmonics. Since that is impractical a more reasonable value for efficiency is around 80%. An inverse class F amplifier is more efficient than the simple class F. In this class, contrary to a class F amplifier, the even harmonics are tuned instead of the odd.

Class J amplifier has an inductive load for the fundamental frequency and a capacitive termination in the second harmonic. Together, these two procedures improve the performance of a class B amplifier creating a class J amplifier. Its efficiency is around 60%.

In theory, all classes of amplifiers that have poor linearity, have an efficiency of 100% but as mentioned before, most amplifiers don't reach such high values of efficiency due to different types of losses. And hence, to select the mode of operation one needs to consider the linearity - efficiency over bandwidth trade-off. Table 2.1 summarizes some of the theoretical characteristics of the power amplifiers previously mentioned and Figure 2.4 represents visually the efficiency and conduction angle for each class.

Class	**Conduction angle**	**Efficiency[10]**
A	360^{o}	30%
B	180^{o}	50%
AB	180^{o}-360^{o}	50%-60%
C	$<180^{o}$	80%
D, E, F, inverse F, J, S	0^{o}	100%

Table 2.1: Power Amplifier Characterization

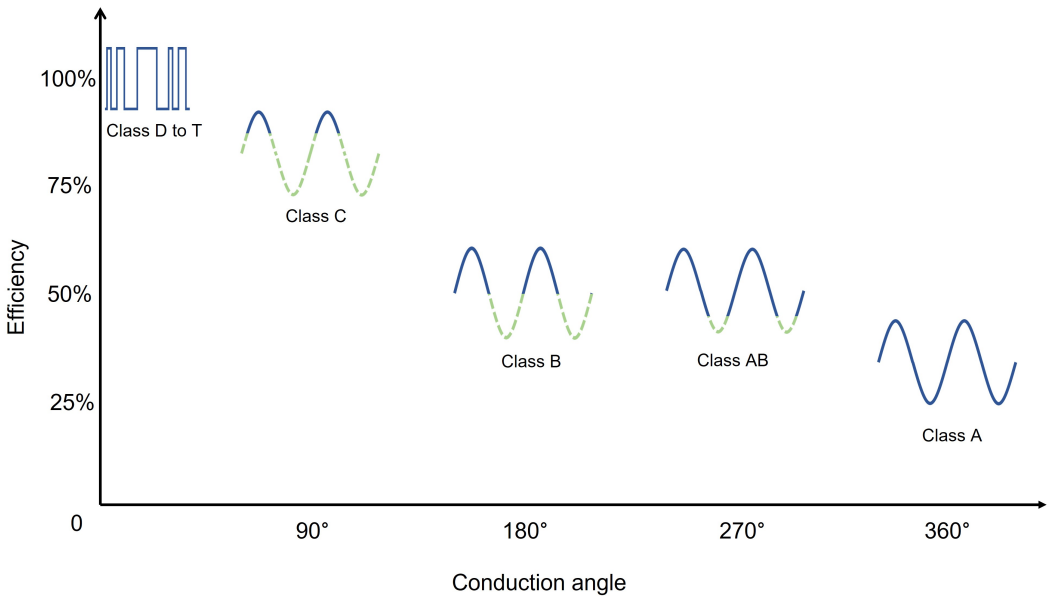


Figure 2.4: Efficiency vs Conduction angle for power amplifier classes

2.3.2 Load-line Analysis Based on DC-IV Characteristics

The load-line theory can be more comprehensive with the help of exemplification of load-line match. Conjugate matching is widely used in classical electronics but for RF, load-line matching is more efficient and provides better results. Taking as an example a generator with a load expressed as Z_g=R+jX, the conjugate match for this case would be Z_{load}=R-jX. Figure 2.5 is a representation of the circuit mentioned above.

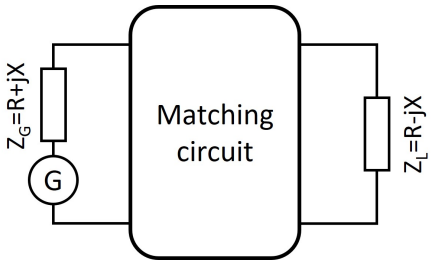


Figure 2.5: Matching circuit

This type of matching doesn't allow for the whole range of voltage and current to be used. For that reason, a better value of Z_{load} would be $R_{load}=V_{max}/I_{max}$ instead of the conjugate of Z_g. This allows the circuit to get the maximum power while still keeping the values of voltage and current limited. This characteristic is necessary for practical scenarios since there is a limited range of voltage and current available.

Load-line principles have been used for a long time and aid at designing load-pull contours in theory. The optimum load for the circuit of Figure 2.6 [11] when ideally matched is ($R_{\text{opt}} = V_{\text{DC}}/I_{\text{DC}}$) if a load-line match is applied. This circuit represents a typical class A amplifier.

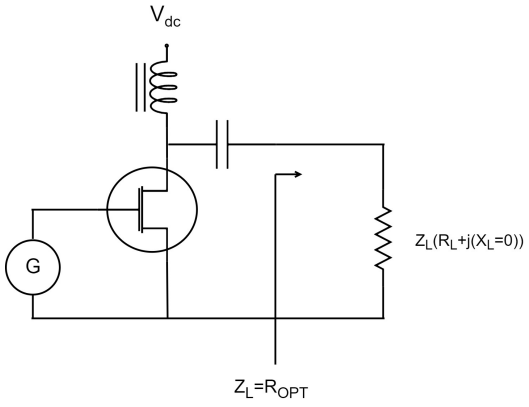


Figure 2.6: Class A amplifier

Let's consider this model of load-line which can help find load-pull contours. By changing the power in the circuit with a fixed ratio, a range of optimum loads is created instead of just one value. The minimum and maximum value have the most interest in this analysis. When

the resistive component of the load is changed a few things can be observed. For the minimum load value, the amplitude of the voltage wave decreases while the amplitude of the current wave is maintained constant. When the resistive component changes for the maximum load, the opposite happens and the amplitude of the current decreases while the voltage amplitude is kept constant.

The minimum and maximum load will provide two points on the smith chart and the change of the reactance or susceptance component will create two segments of arc in the chart. For the minimum optimum load to which a series reactance is added, an arc segment with constant power and constant resistance is created. The current wave is kept at its maximum amplitude and the voltage wave is now able to go back to its maximum value, as the reactance is changed. For the maximum optimum load to which a shunt susceptance was added, an arc segment with constant power, but now constant conductance, is created. The maximum amplitude for the voltage wave is kept and the maximum value for the current's amplitude is now achieved. The arc segments follow the arcs already designed on the smith chart, one of constant resistance for the minimum load and one of constant conductance for the maximum load. Thus, a contour is created and the only thing left to prove is that the interception points of the arc segments coincide with the two points of limiting power. This can be done with some mathematical manipulation and the detailed procedure is present in [11]. Figure 2.7 shows, with the green color, a contour formed with a load-line theory.

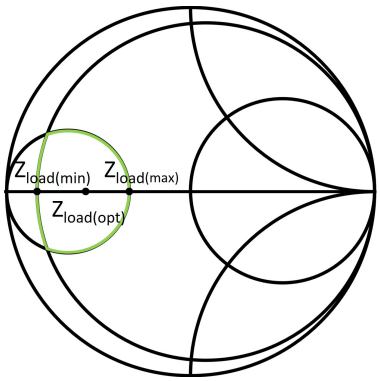


Figure 2.7: Load-line theory contour

2.4 Load-Pull Characterization beyond Load-line Theory

Load-pull consists on systematically varying the load impedance at the fundamental frequency of the device under test (DUT) in order to determine the behavior of the device for optimum performance. It offers the early characterization and prediction of the performance parameters for the best trade-off between gain, efficiency, and output power.

To perform load-pull the reflection coefficient is changed, in order to achieve the desired load values. This can be achieved trough mechanical tuners or the active injection of a signal or some times both. This lead to the classification of load-pull characterization systems into passive load-pull, active load-pull and hybrid load-pull. In a later section, all of the load-pull systems are explained in more detail.

When the load impedance is modified, the incident wave (a_2) also suffers change, causing the reflection coefficient (Γ_L) to change, as desired. Figure 2.8 shows a load-pull circuit where

[12]:

$$\Gamma_{\mathrm{L}} = \frac{a_2}{b_2} \tag{2.1}$$

$$\Gamma_{\mathrm{L}} = \frac{Z_{\mathrm{L}} - Z_0}{Z_{\mathrm{L}} + Z_0} \tag{2.2}$$

and

a_2	incident wave at the output port
b_2	reflected wave at the output port
Z_L	matching impedance
Z_0	characteristic impedance (normally 50)

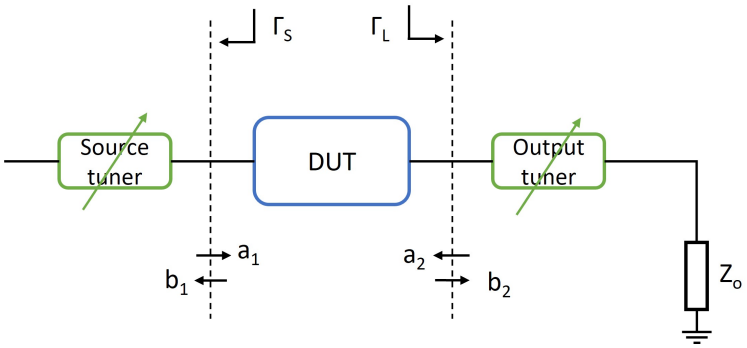


Figure 2.8: Simplified load-pull circuit

Figure 2.9 represents the extracted performance parameters on smith chart from the load-pull characterization. Load-pull contours are oval instead of an expected circle even if the equipment is calibrated perfectly or if it is working in the maximum linear power [11].

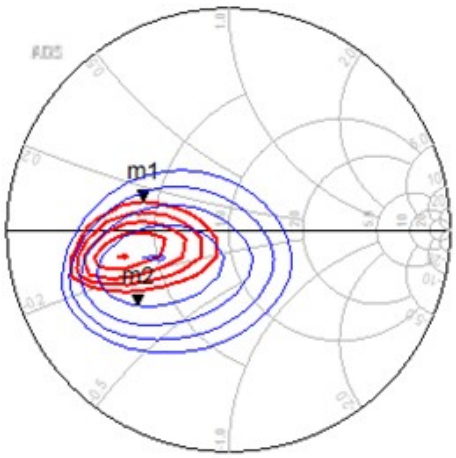


Figure 2.9: ADS simulation load-pull. Red lines represent PAE, and the blue lines represent output power

Load-pull process can be categorized into three parts with the offered measurement features summarized in 2.10. Features relate to the frequency at which the load is analyzed. Load-pull at the fundamental application frequency analyzes the main application oriented performance characterization. Load-pull at the harmonics (also called harmonic load-pull) characterizes the load at the harmonics of the fundamental frequency. This can be significantly useful for the load characterization of switching mode PAs. Load-pull at the baseband frequency of the modulation stimulus, also called baseband load-pull offers further performance enhancement and DUT characterization for linearity.

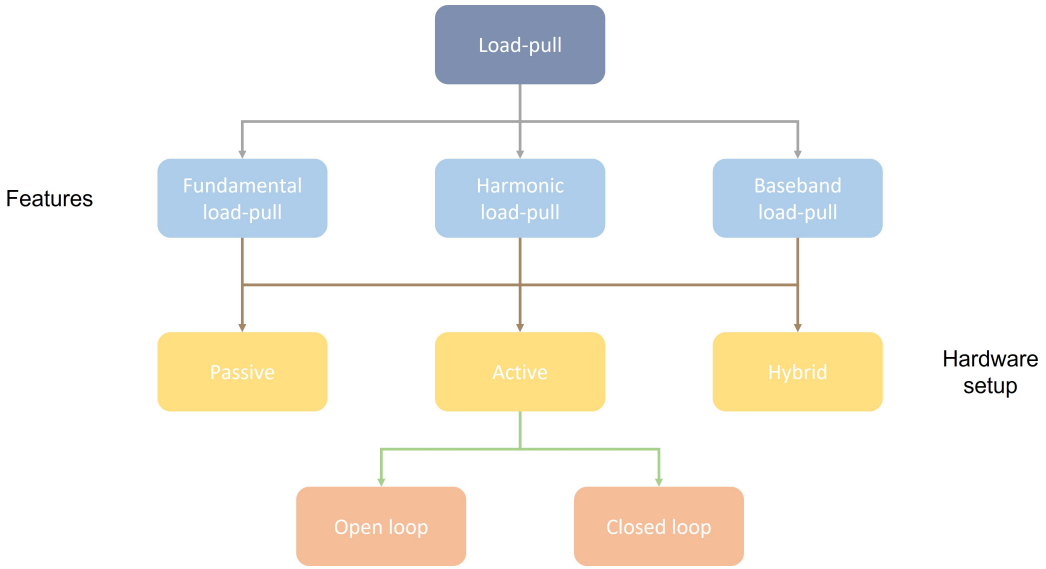


Figure 2.10: Load-pull features and hardware setup

2.4.1 Load-pull Characterization Defined by Features

2.4.1.1 Harmonic Load-Pull

Harmonic load-pull is a type of load-pull where more than just the fundamental frequency impedances are controlled. The load impedance (and possibly the source) is tuned at harmonic frequencies, frequently the second and third harmonics. To achieve an efficient harmonic load-pull system, it is necessary to chose the best tuning device. There are three main types of tuners available [13]; Multiplexer (Triplexer, in case of the use of two harmonic frequencies), Stub Resonator and Cascade Tuner.

A multiplexer separates the harmonic frequencies from the fundamental through the use of filters so that each harmonic can be tuned separately. The stub resonator uses quarter wave open stubs in specific (dual quarter-wave stubs are normally used instead of single as they are more effective). These are connected through a sliding connector to the center conductor. In the case of using two harmonics, the 3rd harmonic stub is the closest to the DUT and reflects the 3rd harmonic signal. Next to it is the 2nd harmonic stub and it reflects the 2nd harmonic signal. Once the signal is through both stubs, only the fundamental frequency is left which is tuned with a normal tuner. Lastly, the cascade tuner uses two cascaded tuners after the DUT and creates about 400.000 impedance states. With so many states a fundamental frequency will be specified and there will be a variety of second harmonic impedances. For a

second harmonic load-pull, states with constant fundamental frequency impedance's will be measured.

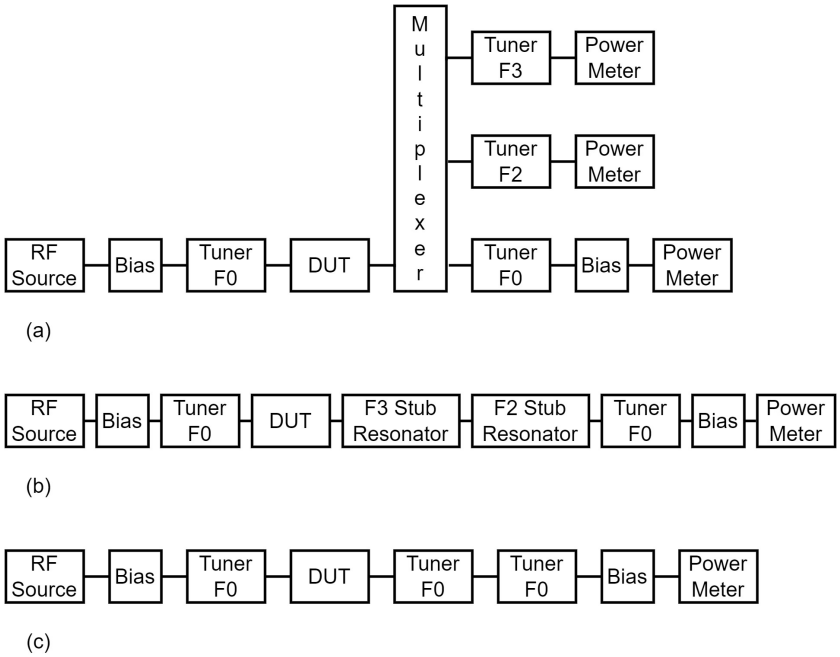


Figure 2.11: (a) multiplexer (b) stub resonator (c) cascaded. Adapted from [13].

The most important characteristic is tuning isolation since the fundamental frequency impedance is far more susceptible to changes caused by the harmonic impedances than the other way around. A small change of fundamental impedance can have a big impact on the overall system and can lead to doubts if the change was caused by the harmonics or the tuner. Tuning isolation is therefore very important. Out of the three methods explained, multiplexers show the best tuning isolation [13].

2.4.1.2 Baseband Load-Pull

Baseband load-pull has the same purpose as fundamental and harmonic load-pull do, which is to find the optimum performance of the PA by varying the source or load impedance. But in the case of baseband load-pull, it is done for the baseband frequency. This form of load-pull can be important to have good control over the baseband impedance.

Baseband impedance is a contributor for memory effects. Memory effects are changes of amplitude and phase of distortion as a response to a tone difference of a two-tone signal. Distortion itself isn't a memory effect but the changes in phase and amplitude of distortion are [14]. Small changes of amplitude or modulation are not harmful to the PA but when linearization methods are used, for example to cancel intermodulation sidebands, the impact of memory effects is noticeable meaning that the attempt of linearization becomes ineffective [14].

Baseband frequency, which is determined by the baseband impedance, has the ability of changing intermodulation levels as explained in detail in [15]. So controlling the baseband impedance becomes important to control memory effects in hopes to improve linearization of the power amplifier. This control can be done with an active baseband load-pull [15].

2.4.2 Load-pull Characterization Defined by Hardware Setup

2.4.2.1 Load-pull Characterization with Passive Tuners

Passive load-pull encompasses all types of load-pull that use mechanical tuners. There are two types of tuners [12]: electromechanical tuners (EMTs) and electronic tuners (ETSs). Electromechanical tuners change the impedance by the positioning of probes, stub or slugs as represented in Figure 2.12.

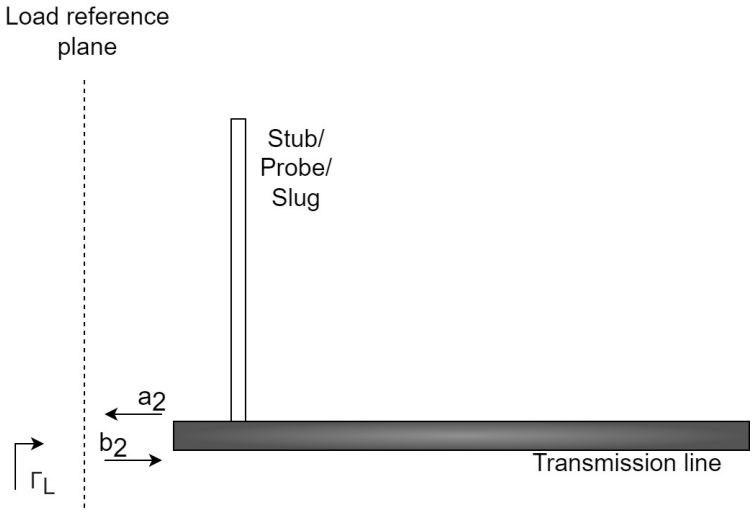


Figure 2.12: Simplified version of a EMT

The horizontal and vertical movement of the stub/probe/slug defines the reflection coefficient change of phase and magnitude respectively. Most electronic tuners used for load-pull measurements are based on PIN diodes since they work well with high power. The change of reflection coefficient is processed through changing the impedance state of some of the PIN diodes. The diodes can be connected in parallel or in series in order to create a great amount of impedance states, since each diode has two states (on and off). When cascaded, the states are increased by a power of 2. ETSs are quicker in changing from impedance to impedance and are also smaller when compared to EMTs. ETSs have lower insertion loss than EMTs but EMTs offer higher repeatability than ETSs. The choice of which tuner to use will come down to which characteristics of the tuner are more important for the system in use.

2.4.2.2 Load-pull Characterization Through Active Injection

As mentioned in 2.4.2.1, tuners are used for passive load-pull, which is a mechanical way to change the impedance. In that case, the magnitude and phase of the reflected signal, a_2, are changed, causing a change in the load impedance. However, in load-pull with active injection, the intention is to make that change through the injection of a magnitude and phase controlled signal towards the DUT. One of two methods is used to change the impedance seen by the DUT [16]: reintroducing a modified version of the signal (change in magnitude and phase) on the DUT which produces a closed loop system or the introduction of a new signal back towards the device in an open loop system as Figure 2.13 illustrates.

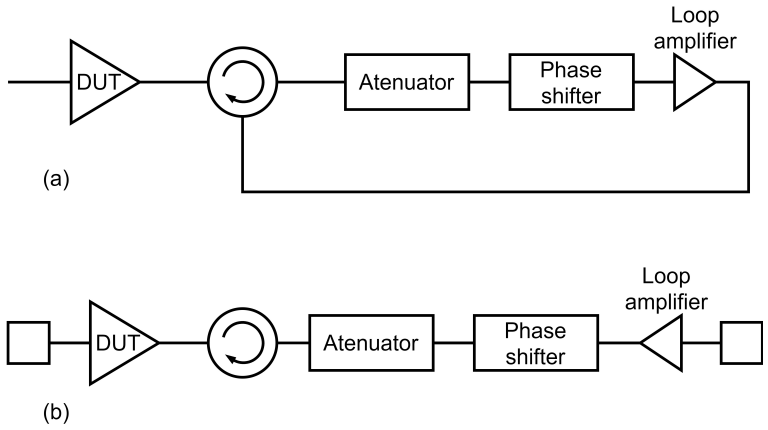


Figure 2.13: (a) closed loop (b) open loop. Adapted from [12]

The closed loop configuration is beneficial since it uses pre-existing signal but for that reason, it can be susceptible to oscillations. The open loop configuration mitigates the problem of possible oscillations and is easier to implement but creates the added need of an exterior signal generator. Open loop is the type of active load-pull most used since it is easy to implement and robust. Active load-pull can be used either in substitution or together with a tuner by adding reflected power on top of the reflected power of the tuner. This translates into a larger value of gamma (Γ_L).

2.5 Biasing and Matching Circuits

2.5.1 Biasing

Biasing circuit is correlated with two things: biasing point and biasing network. The biasing point has been explained in 2.3.1 and consists on setting the starting conditions for a device which are normally fixed values of current and/or voltage. A biasing network consists mainly of a DC block and a RF choke. The RF choke is meant to have very high impedances at working frequencies and prevent leakages from the RF through the biasing network [17]. Figure 2.14 represents a basic biasing circuit.

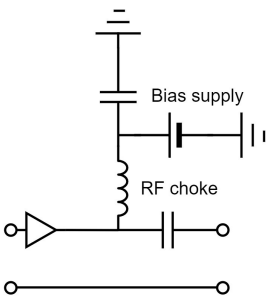


Figure 2.14: Biasing circuit. Adapted from [17].

2.5.2 Baseband matching circuit

In the modulation domain, impedance at the baseband frequency defines influence on the memory effect as a result of the linearity deviation of the DUT. In most of the PA design, baseband impedance matching is designed with the biasing network to avoid the complexity of the output matching networks. Theoretically, short circuit is the optimum baseband match.

2.5.3 Harmonics matching circuit

A harmonic is a signal that is an integer multiple of the fundamental signal. Harmonics can be the result of nonlinear loads that draw current in abrupt pulses instead of sinusoidal shape. These pulses cause distortion on the current waves which causes harmonics [18]. Classe S-E-F-Inv F have controlled harmonics while classes A to C short circuit the harmonics at higher order. The use of harmonics is important to improve drain efficiency. Class E and class F work with voltage and current waves that are intended to avoid overlapping in order to gain efficiency [19].

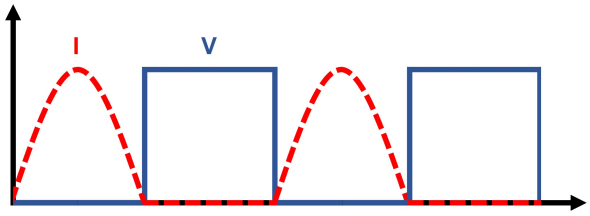


Figure 2.15: Current and voltage waves for class E and class F

2.5.4 Matching strategies

In order to extract the maximum power from a device, it is necessary to terminate the circuit with a load that will match the source load. In 2.3.2, conjugate and load-line matching are explained. If a circuit has a component that isn't matched, there are two options: modify the component or add a matching network. The mismatch can also be a result of a change of frequency. A match that works for a frequency, won't produce the maximum power for a different frequency and for that reason, a different match is necessary. The most efficient choice is to have a matching network which will adjust the impedance as necessary as represented in Figure 2.5.

Some of the most used matching network technologies are [20]: (1) L Networks which name represents how the L and C components are placed. (2) π and (3) T Networks are alternative to L networks. These also receive their name accordingly to how L and C components are placed. Compared to L networks, π and T Networks do not change the impedance match but improve the quality factor. (4) Inductor-Only Networks won't deliver voltage boosting but are cheaper to manufacture and test and are more efficient with high-power loads.

(5) Transformer-based Networks achieve voltage magnification and resistive transformation, relative to the coil ratio, through the coupled inductors from the transformer [20]. Figure 2.16 is a visual representation of the five topologies mentioned.

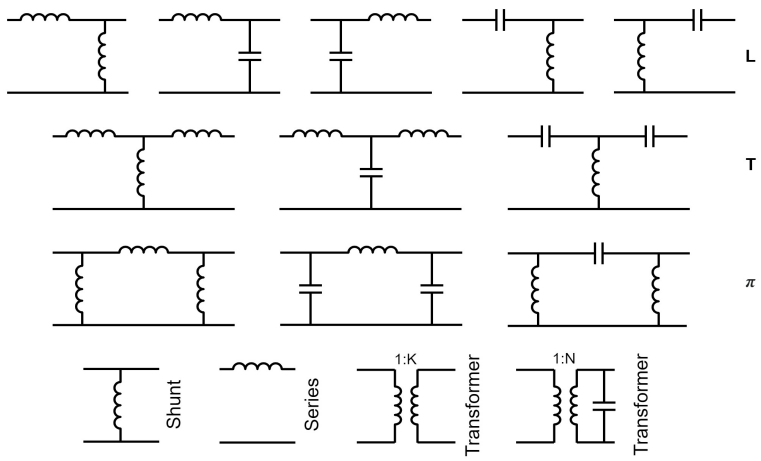


Figure 2.16: Matching strategies. Copied from [20]

2.6 Figure of Merits of the PA

When working with power amplifiers in a nonlinear region, distortion becomes a problem. This section addresses some types of distortion caused by the nonlinearities of PAs.

2.6.1 AM-AM

AM-AM characterization relates the input amplitude with the output amplitude at specific frequencies. This means, it helps in characterizing the gain compression level that helps to define the PA compression caused by the ADT limitations of the linear amplification. This characterization aids in the analysis of the 1dB compression point [21]. The 1dB compression point (P1dB) is where the output signal is 1dB bellow the expected signal, after the power amplifiers reaches saturation. However, depending on application, XdB compression point is considered from the load-pull characterizations.

2.6.2 AM-PM

AM-PM characterization quantifies the change in phase from the input and output signals which result from a nonlinear behavior of the power amplifier. AM-PM normally starts to affect the linearity some dBs after the compression point [22]. For this reason, AM-PM has the most impact on systems that work with phase modulation like modern telecommunications and wireless systems [21].

2.6.3 Intermodulation Distortion (IMD)

Intermodulation distortion represent the nonlinearities in adjacent frequencies for more than one frequency application scenario. The output will contain the original signal and also a sum and difference of the input signals together with the harmonics [23]. Considering a system with two input signals at frequencies f_1 and f_2, at the output f_1+f_2, f_2+f_1, $2f_1$ and $2f_2$ will also be present. These are the 2nd order intermodulation products. $2f_1$ and $2f_2$ are harmonics which have been introduced in 2.5.3.

The 3rd order intermodulation products are a mixture of 2nd order intermodulation signals with the original signals. Most of the intermodulation products are far enough from the original signals, f_1 and f_2, and can be removed through filtering. But the 3rd order intermodulations of $2f_1$-f_1 and $2f_2$-f_2 are close to the fundamental frequencies which makes them hard to be filtered and can cause interference in the original signal. Figure 2.17 shows a visual representation of each intermodulation order. The 3rd order intermodulation products that are closer to the fundamental frequencies are often known as "spectral regrowth".

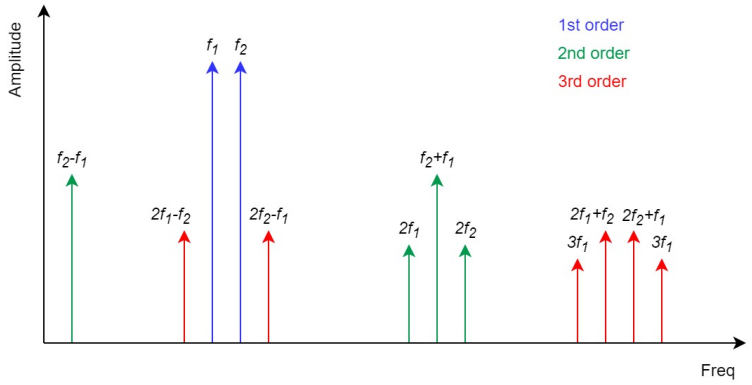


Figure 2.17: Intermodulation products and harmonics [23].

2.6.4 Adjacent Channel Power Ratio (ACPR)

As mentioned in the previous subsection, 2.6.3, when a device is operated at a nonlinear region, intermodulation distortion appears and causes spectral regrowth. Adjacent Channel Power Ratio (ACPR) is used to characterize and quantify spectral regrowth and is the ratio between the power in the adjacent channels of main channel and the power of the main channel.

$$ACPR_{[\mathrm{dBc}]} = 10 * log(\frac{\mathrm{P_{adj}}}{\mathrm{P_{ch}}}) \tag{2.3}$$

2.6.5 Error Vector Magnitude (EVM)

Error Vector Magnitude (EVM) is used to quantify the performance of a system and is the vector difference between the expected and the actual signal as seen in Figure 2.18. This measurement helps qualify a communication system in modulation domain.

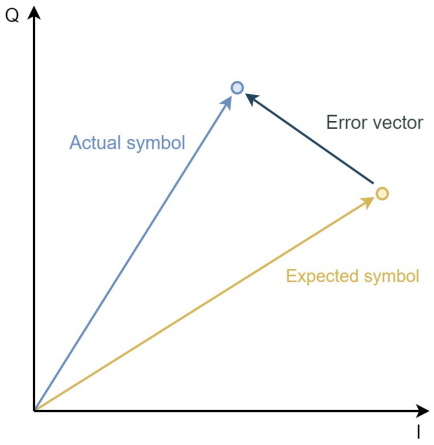


Figure 2.18: Error Vector Magnitude

2.6.6 Noise Factor

Noise Factor, NF, quantifies the degradation of the signal to noise ratio (SNR) where SNR relates the desired signal to the background noise. NF is the ratio between the input signal to noise ratio to the output signal to noise ratio and is calculated by

$$NF = \frac{\frac{S_{in}}{in}}{\frac{S_{out}}{N_{out}}} \tag{2.4}$$

where,

S_{in}	Signal level at input
N_{in}	Noise level at input
S_{out}	Signal level at output
N_{out}	Noise level at output

2.6.7 Gain

Gain is the ratio between the output and input of voltage or current. It quantifies the amount a signal is amplified and is a very important figure of merit for power amplifiers.

$$Gain = \frac{\text{Output signal}}{\text{Input signal}} \tag{2.5}$$

2.6.8 Power Added Efficiency

Power Added Efficiency, PAE, is an efficiency measurement which provides more information as it also considers the gain. It is normally analysed as a percentage.

$$\text{PAE}(\%) = \frac{\text{Pout - Pin}}{P_{\text{DC}}} \times 100 \tag{2.6}$$

Chapter 3

Wideband Load Characterization using Load-pull

3.1 Introduction

This chapter is dedicated to detailed experiments about ADT characterization analysis using CAD tool. It includes two parts of the PA characterization, DC-IV and load-pull characterization while considering important FoMs and its trade-offs. DC-IV characterizes the the DC optimum load at maximum power capacity. Load-pull characterization is performed with CW (continuous wave) and 2-tone stimuli.

3.2 DC-IV Characterization using ADS

As discussed in Chapter 2, DC-IV characteristics of the active device helps understand the DC power consumption, transconductance (gm), purely resistive optimum load for maximum power (R_{Load}), DC load-line, and boundaries of the operation of it. It defines the linear and nonlinear operating region for the PA operation that helps to characterize the class of PA. In practice, advanced pulsed DC-IV characterization can be used to avoid the trapping and temperature effect for the IV characterization for more precision. Analysis is carried out with the LDMOS in the following sub section 3.2.1 and same can be applied to the GaN as well.

3.2.1 DC-IV Characterization of LDMoS

For the analysis, 55W LDMOS device model is used from Ampleon. Figure 3.1 shows the circuit schematic and the plot, drain voltage (VDS) and drain current (IDS) with the load-line between knee voltage and expected breakdown of the device. From the analysis, class B operation can be considered with (VDS, VGS), (28V, 2.18V) biasing conditions for the rest of the dissertation for LDMOS. From the analysis R_{opt} is characterized by 3.1, from the load-line theory [11]. For our case it is 14Ω.

$$R_{opt} = \frac{V_{DD} - V_k}{I_{max}/2} \tag{3.1}$$

Where, V_{DD} is DC drain voltage, V_k is knee voltage and I_{max} is maximum drain current at the knee voltage.

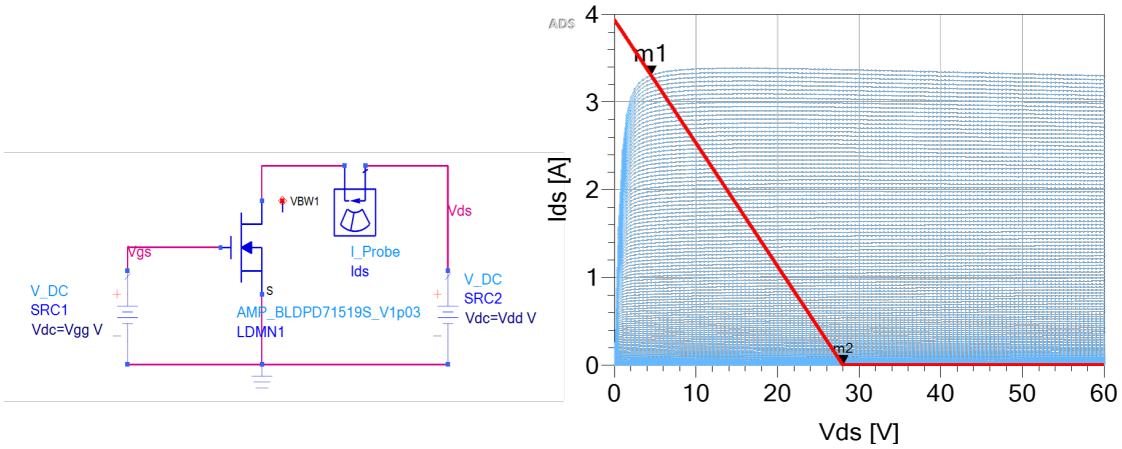


Figure 3.1: DC-IV characteristics of LDMoS device

3.2.2 Load-pull Characterization of LDMoS and GaN

As seen in a previous section, optimum resistive load can be extracted from the DC-IV characteristics. However, it purely depends on the DC characteristics at the current reference plane/very intrinsic plane. With the packaging and internal matching added to the ADT the impact of the intrinsic parasitic needs to be eliminated with the complex conjugate match at the external load to achieve the maximum power transfer to the load. To achieve the maximum power transfer condition, where the optimum load compensates the intrinsic parasitic impact, load-pull characterization plays a significant role. Figure 3.2 is used in rest of the dissertation with different operating conditions and DUT. For the load-pull analysis, ADT is operating in class B mode with biasing voltages characterized in DC-IV characteristics. In addition, a biasing network is implemented with the ideal DC feed and DC block components. The higher order harmonics are set to open circuit at the source and open circuit at the drain to provide ideal fundamental load-pull environment.

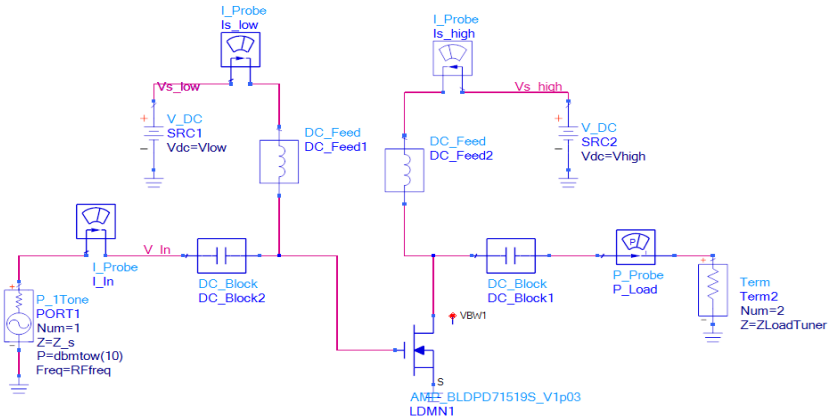
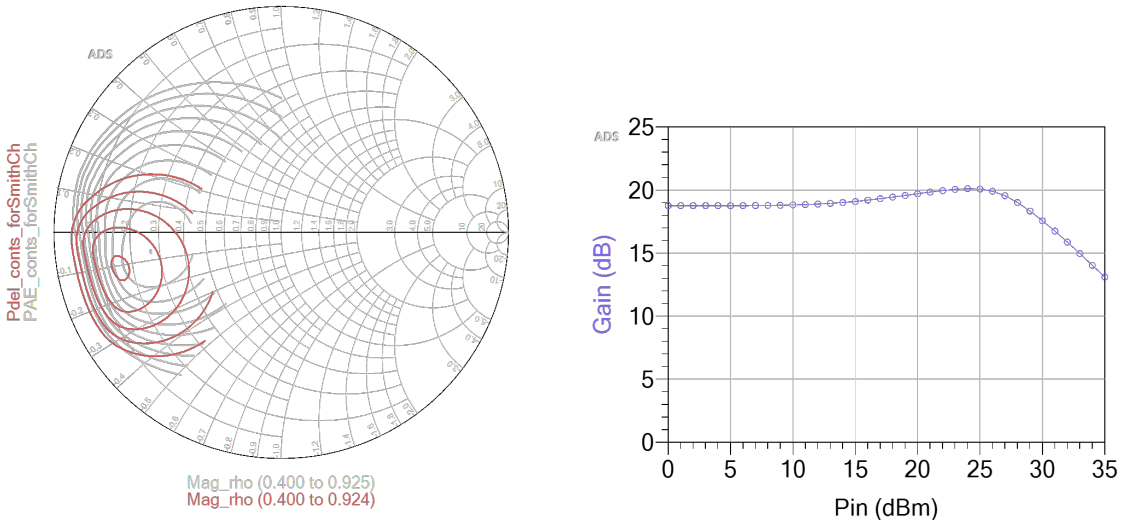


Figure 3.2: Load-pull characterization schematic

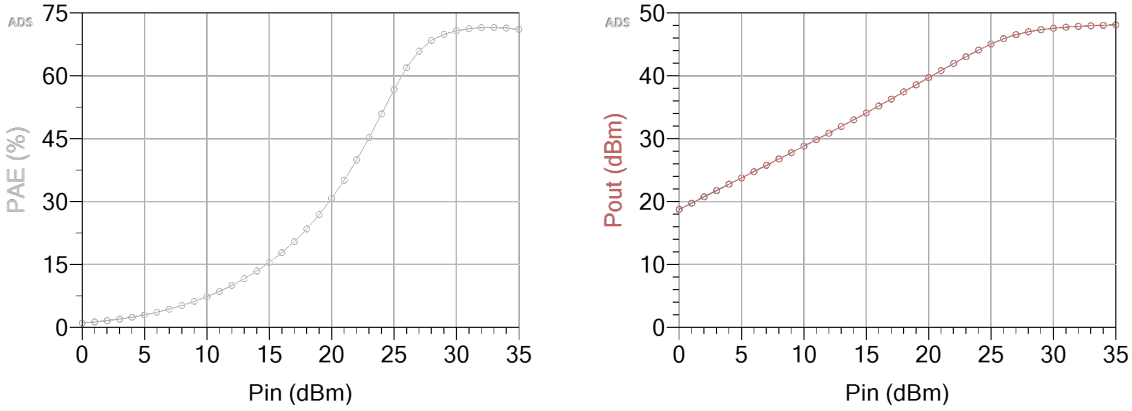
LDMoS Load-pull Analysis

Figure 3.3 summarizes the load-pull analysis contours for the LDMOS. As discussed in Chapter 2, contour plot reveals the trade-off between the FoM such as output power and efficiency with relevant load. The optimum value for P_{out} and PAE is 47.31dBm and 74.06% at 8.242-j5.544Ω and 13.352-j3.248Ω load respectively. Figures 3.3-3.4 show the performance parameters at the maximum optimum power and 1800MHz frequency load. It can reflect the compromise of data that needs to be made between optimum values of the FoMs.



(a) FoMs Contour (b) Gain

Figure 3.3: Trade-off contour and optimum gain of LDMOS at optimum load defined at maximum output power



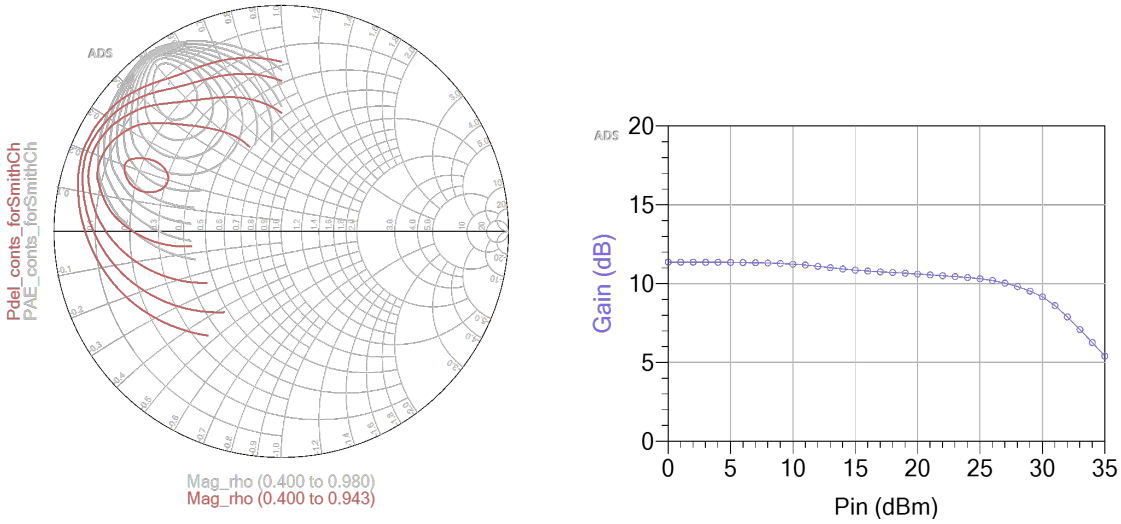
(a) PAE (b) Pout

Figure 3.4: PAE and Pout at the optimum load defined at the maximum output power for LDMOS

GaN Load-pull Analysis

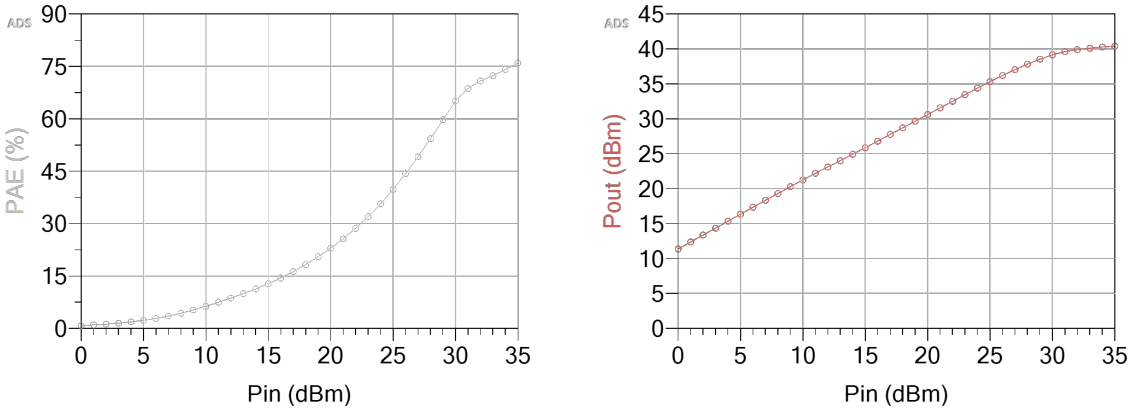
For the GaN analysis, CGH40006P GaN Model is used. Similar to the LDMOS, DC-IV

characterization is also performed to study the biasing characteristics. From the analysis, GaN is biased in class B operation mode with drain bias of 27V and gate bias of -2.9V, and in ideal fundamental condition. Figure 3.5 summarizes the load-pull analysis contours for the GaN transistor. The optimum values for P_{out} and PAE are 37.82dBm and 77.52% at 10.647+j9.729Ω and 6.159+j24.625Ω load respectively. Figures 3.5-3.6 show the performance parameters at the optimum power and optimum frequency loads at 3700MHz. Like for LDMOS, it can reflect the compromise needed between optimum values of FoMs.



(a) FoMs Contour (b) Gain

Figure 3.5: Trade-off contour and optimum gain of GaN at optimum load defined at maximum output power



(a) PAE (b) Pout

Figure 3.6: PAE and Pout of GaN at the optimum load defined at the maximum output power

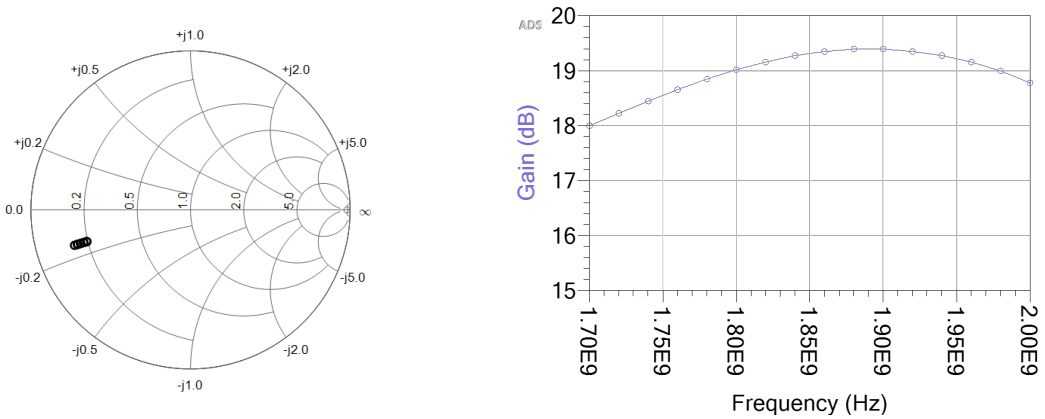
3.3 Load-pull Characterization Over the Wide Bandwidth

The performance presented in the previous section is for single carrier frequency and relevant FoMs. In telecommunications applications complex modulated signals are used with finite bandwidth. In this section, optimum load in different range of frequency for 4G-LTE band n25 and 5G band n77, n78 is extracted to try and show how the optimum load for the finite bandwidth changes and how FoMs changes with it.

3.3.1 Optimum Load Characterization for Wide Bandwidth

Since the LDMOS used for the analysis is limited to the 4G band n25, GaN is used to analyse the wide bandwidth 5G band n77, n78. For the analysis with the LDMOS, frequency range 1700MHz - 2000MHz is used with 20MHz of spacing.

From Figure 3.7, it can be observed on the smith chart that the optimum load is different for the different frequencies within the band. In practice, the single optimum load is used at the center frequency. However, single load at the entire frequency band creates a non match at the frequency on the other edge. This leads to non maximum power transfer conditions at the application bandwidth and becomes one of the reason of performance degradation. The value of the gain varies within band from 18dB to 19.5dB, P_{out} varies from 46dBm to 47.5dBm, and PAE varies from 73% to 74.5% at 3-dB compression which can be seen in 3.7-3.8. In the case of constant optimum load at center frequency over the bandwidth of 1700MHz - 2000MHz, the performance of P_{out} and PAE over frequency can be seen in Figure 3.9-3.10. In the linear region of the graphs from Figures 3.9-3.10, the variation of PAE is of $10 - 20\%$ while P_{out} and Gain vary between 2-5dB. This variation of the FoMs with respect to the constant load depends on the ADT.



(a) Impedance over frequency

(b) Gain over frequency

Figure 3.7: Optimum impedance over the frequency and for the same impedance optimum gain variations of LDMOS

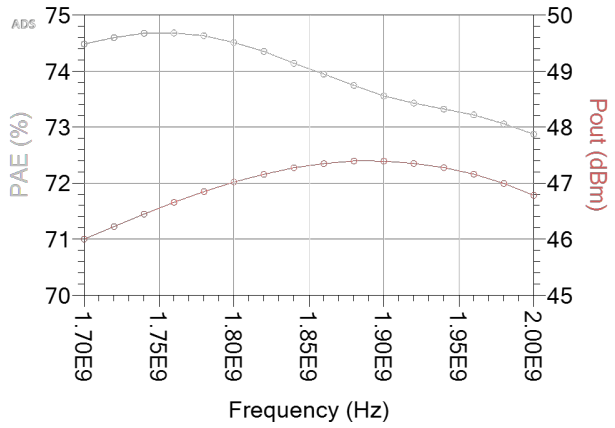
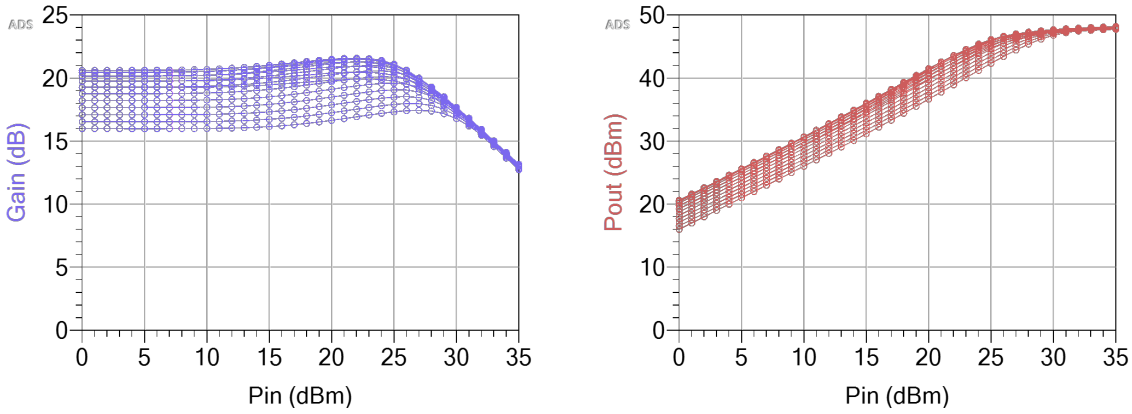


Figure 3.8: Pout and PAE of the LDMOS for the optimum loads with relevant frequency shown in the smith cart of Figure 3.7



(a) Gain variations over frequency

(b) Output power variations over frequency

Figure 3.9: Gain and output power of LDMOS as a function of frequency with constant load over bandwidth

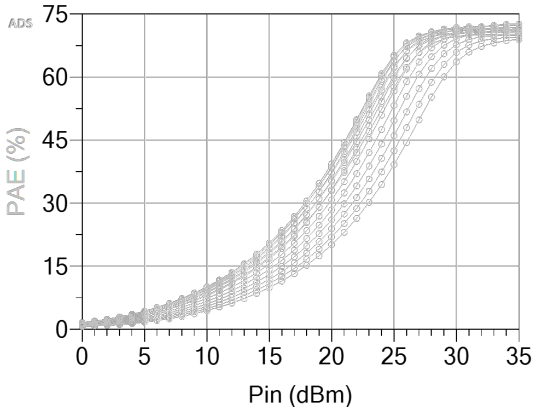
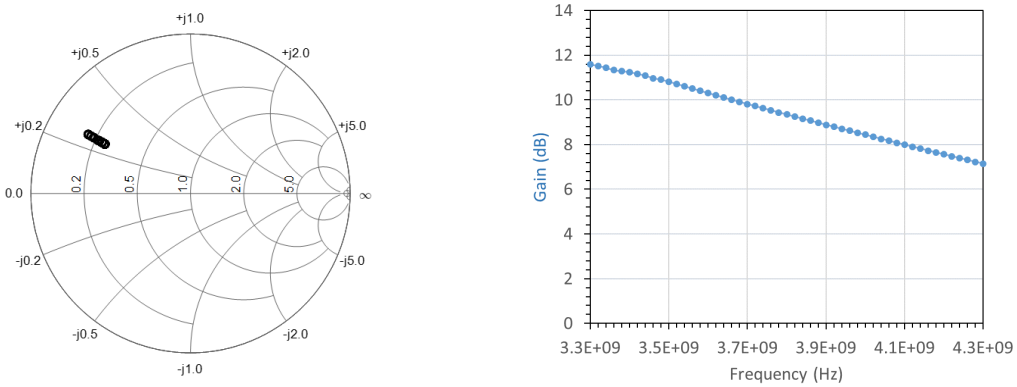


Figure 3.10: PAE of the LDMOS as a function of frequency with constant load over bandwidth

Similarly, from Figure 3.11, the variation of the optimum load can be analyzed within the 5G n77, n78 band from 6Ω to 12Ω. This leads to the variation in P_{out}, and gain within band from 2dB to 8dB, and PAE varies from 5% to 10% which can be seen in 3.11-3.12. In the case of constant optimum load at center frequency over the bandwidth of 3300MHz - 4300MHz, the performance of P_{out} and PAE over frequency can be seen in Figures 3.13-3.14. In the linear region of the graphs from Figures 3.13-3.14, the variation of PAE is of $10 - 20\%$ while P_{out} and Gain vary between 5-8dB. As compared to the LDMOS the FoMs with respect to the constant load over the wide range of frequency, GaN device shows more significant variations.



(a) Impedance over frequency

(b) Gain over frequency

Figure 3.11: Impedance over the frequency and for the same impedance optimum gain variations of GaN

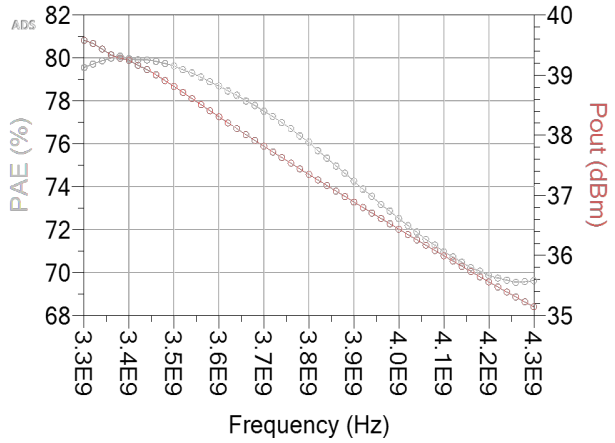
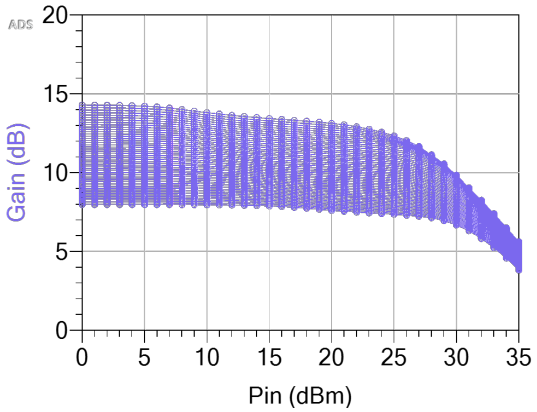
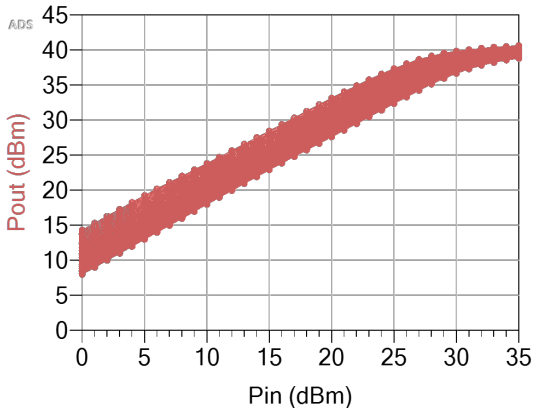


Figure 3.12: Pout and PAE of GaN for the optimum load defined in the smith cart of Figure 3.11



(a) Gain variations over frequency



(b) Output power variations over frequency

Figure 3.13: Gain and output power of GaN as a function of frequency with constant load over bandwidth

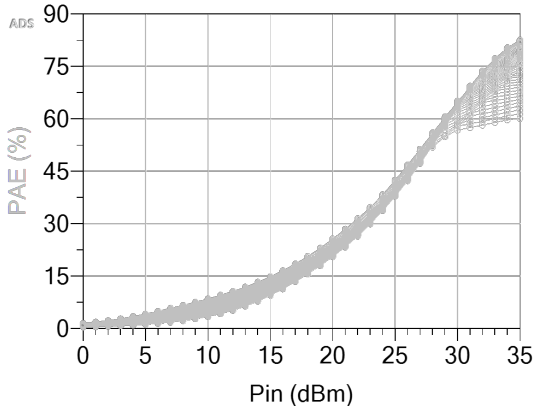


Figure 3.14: PAE of GaN as a function of frequency with constant load over bandwidth

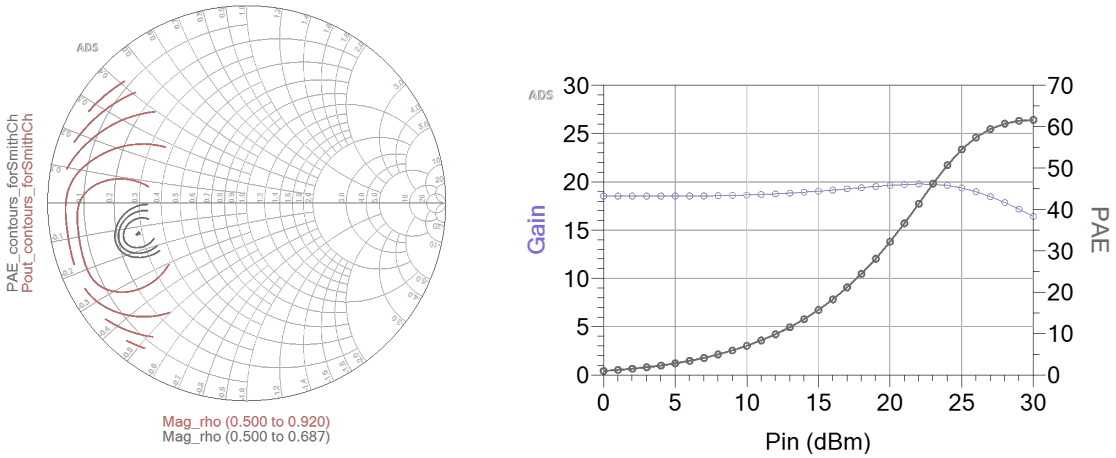
3.4 2-tone ADT characterization using ADS

In the previous Section 3.3, CW based load-pull characterization is performed to study the relation between optimum load and frequency for 4G and 5G applications with LDMOS and GaN ADTs. In this section, further study is carried out with 2-tone load-pull analysis. It offers a platform to characterize the intermodulation distortion (IMD) and behavior with the finite bandwidth. The relation between IMD (and other performance parameters) and baseband effect is also analyzed with finite bandwidth. The analysis is performed with LDMOS.

3.4.1 2-tone Characterization of LDMOS

For the analysis, the schematic shown in Figure 3.2 is used with a 2-tone power source and the optimum load. ADT is biased in class B operation with biasing drain at 28V and gate at 2.18V. For the 2-tone load-pull, similar to CW load-pull, biasing network is implemented with the ideal DC feed and DC block. And to avoid any mismatch caused at the

baseband, baseband impedance is matched to short circuits. A later case is discussed where a 2-tone analysis with constant optimum load but with different baseband impedance is performed. When compared to the CW load-pull in Figure 3.3, Figure 3.15 shows performance degradation caused by the finite bandwidth. Maximum PAE degradation is from 74% to 63%. Output power at 3dB compression point is also reduced from 47dBm to 45dBm. Figure 3.16 represents the 3rd order and 5th order intermodulation distortion for the ADT. IMD is defined depending on the application, but here for a IMD3 of 30dBc, the performance of the ADT shows a 40dBc IMD5 and 25% of PAE. From the analysis, performance variation between CW and finite bandwidth can be evaluated.



(a) Pout-PAE contour contour

(b) Gain

Figure 3.15: 2-tone Pout and PAE trade-off contours and (Gain,PAE) at the optimum load

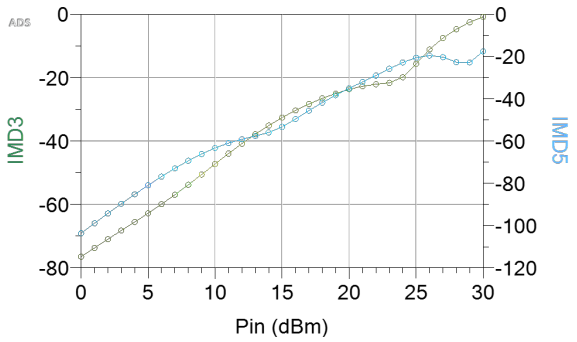
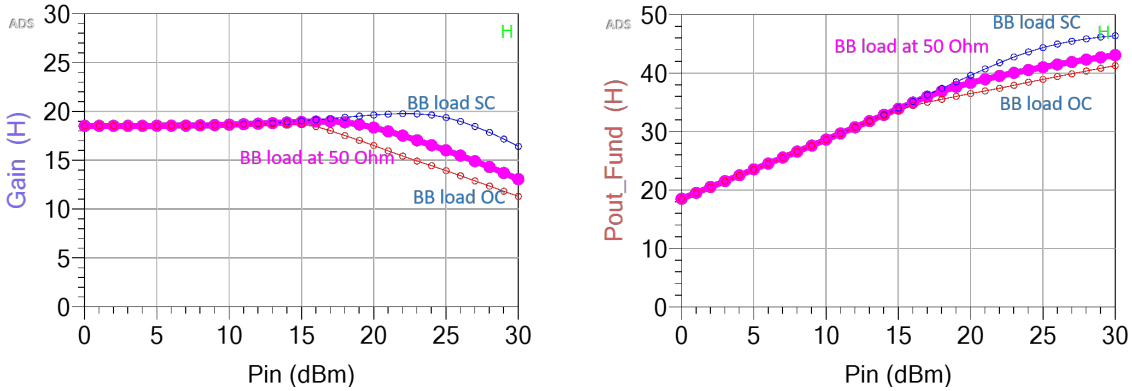


Figure 3.16: 3^{rd} and 5^{th} Order inter-modulation distortion (IMD) for optimum load at maximum power extracted from Figure 3.15

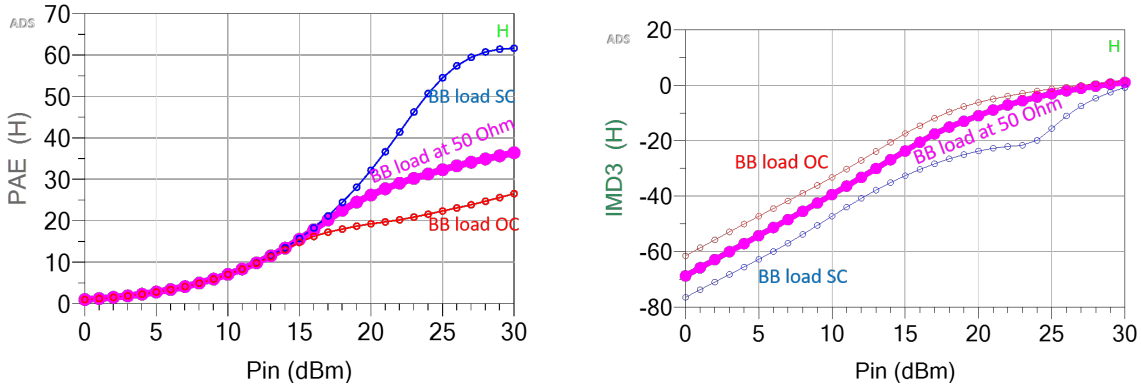
With increasing bandwidth, baseband component of the 2-tone also appears due to hard nonlinearities. This causes memory effect in the PA. Baseband components create a re-modulation of the drain bias and this leads to further performance degradation. Ideally, baseband impedance needs to match a short circuit at the bias-tee to reduce the memory effect of the PA. However, practically, due to packaging and intrinsic/extrinsic match, other optimum impedances need to be matched to compensate the parasitics effects at the baseband.

Load-pull at the baseband is nowadays a very popular characterization tool for the non-linearity assessment and enhancement. Baseband impedance load-pull is a future scope of the dissertation. However, impedance of the different baseband match, short circuit, 50Ω, open circuit impedance is analyzed with ADS. From the results, presented in Figures 3.17-3.18, the performance variation with respect to the baseband impedance match can be observed. PAE has significant changes between short circuit and open circuit match, around 40% of the PAE. At 3db compression output power is reduced by about 8dB and IMD3/IMD5 are also degraded by 10dBc.



(a) Gain (b) P_{out}

Figure 3.17: Gain and Pout at different baseband impedance match



(a) PAE (b) IMD3

Figure 3.18: PAE and IMD3 at different baseband impedance match

Chapter 4

Conclusion and Future Work

The evolution of wireless technology to facilitate the advanced applications, such as augmented reality and virtual reality leads to more complex back-end processes. From the first generation of telecommunications to the future 6G, expectation from the wireless networks increased drastically in terms of the data traffic supports. Nowadays, wireless systems are expected to support much higher data traffic. To support such increasing demands, wireless networks are expected to offer more linear and spectral efficiency. For such, digital modulation schemes are providing more efficient methods to support the higher data rates over defined bandwidth at a cost of more complexity on the time domain stimulus. However, in the wireless network, physical layer imposes more limitations in terms of the linearity and bandwidth support trade-off. Moreover, increasing statistical complexity of the signal affects the physical layer quality of services.

In wireless transceivers, power amplifier is the most crucial component that largely affects the overall quality of service of the physical layers. Power amplifier imposes a limitations of linearity and power efficiency trade-off over wide bandwidth.

In this dissertation, we have tried to show the performance behaviour of the ADT in wideband scenario with load-pull characterization in ADS simulator. Firstly, we have tried to study the performance of the ADT with CW load-pull characterization. For the analysis, ADT operating condition is extracted from the DC-IV characteristics. It helps to evaluate the purely resistive optimum load (R_{opt}) from the load-line theory. Later, using load-pull characterization around that R_{opt}, further optimum load Z_L is characterized to eliminate the intrinsic and extrinsic parasitics. In this study two different wideband ADTs are used, LDMOS for 4G band n25 application and GaN CGH400P for 5G band n77-78 applications.

Afterwards, load-pull analysis is performed with frequency sweep to study the optimum load behaviour over frequency. In this analysis, it was shown that optimum load strongly depends on the operating frequency where the load-pull analysis is performed. It is also observed that the constant optimum load over wideband degrades the performance when compared to using only the carrier frequency. It means that in the case when the optimum load varies with the frequency, the performance of the wideband application can be further enhanced

With the 2-tone analysis, it is also shown that with the finite bandwidth, PA performance can degrade. Moreover, with the 2-tone analysis, intermodulation products can also be characterized for the linearity analysis. The IMD3/IMD5 also deviate depending on the bandwidth and signal statistics. Moreover, in the 2-tone analysis, the baseband component

of the PA starts dominating the effects that lead to the hard nonlinearity and memory effect. This degrades the performance parameters. To eliminate this baseband effect, baseband impedance needs to match to a short circuit. In Chapter 3, baseband impedance with short circuit, 50Ω and open circuit is characterized. From the analysis, it can be concluded that the performance of the PA can be further enhanced with a short circuit baseband impedance.

As a scope of the future work, load-pull analysis with frequency dependent load can be extended with more complex stimulus, such as multi-tones, and complex modulated signals. In addition, the study on the behaviour of the ADT with respect to the optimum load and frequency can be extended to the modeling of the transfer function to design a matching network that supports the optimum load variation with respect to frequency to optimize the overall performance of the PA. Moreover, baseband impedance load-pull can also be extended for the baseband load characterization and with the multi-tone and modulated stimulus, baseband impedance effect can also be studied. With the help of the analysis presented in this dissertation, PA can be designed with more insight on performance and practical implementation of it leads to more comprehensive characterization setup.

Bibliography

[1] https://mark-kalin.com/the-evolution-from-1g-to-5g/

[2] *What is Frequency Division Multiple Access (FDMA)?* - Definition from Techopedia. Techopedia.Com. Obtained from http://www.techopedia.com/definition/5669/frequency-division-multiple-access-fdma

[3] Myung, H. G., & Goodman, D. J. (2008). *Single Carrier FDMA: A New Air Interface for Long Term Evolution.* John Wiley & Sons, Ltd. https://doi.org/10.1002/9780470758717

[4] Myung, H. G., Lim, J., & Goodman, D. J. (2006). Single carrier FDMA for uplink wireless transmission. *IEEE Vehicular Technology Magazine,* 1(3), 30–38. https://doi.org/10.1109/MVT.2006.307304

[5] Myung, H. G. (2007). Introduction to single carrier FDMA. *2007 15th European Signal Processing Conference*, 2144–2148.

[6] Fawzy, A., & Elnaby, M. M. A. (2018). *Application of a Class of Companding Techniques On SC- FDMA System.* 11.

[7] Meerut Institute of Engineering & Technology, Sharma, A., & Kr. Singh, A. (2016). Orthogonal Frequency Division Multiplexing and its applications. *International Journal of Computer Trends and Technology*, 38(1), 21–23. https://doi.org/10.14445/22312803/IJCTT-V38P105

[8] Chide, N., Deshmukh, S., Borole, P. B., & Chore, N. (2013). *An Overview of OFDM Variants and Their Applications.* 4, 5.

[9] Jiang, X. (2017). Fundamentals of Audio Class D Amplifier Design: A Review of Schemes and Architectures. *IEEE Solid-State Circuits Magazine, 9(3)*, 14–25. https://doi.org/10.1109/MSSC.2017.2712368

[10] Amplifier Classes and the Classification of Amplifiers. (2013, July 25). *Basic Electronics Tutorials.* https://www.electronics-tutorials.ws/amplifier/amplifier-classes.html

[11] Cripps, S. C. (2006). *Rf power amplifiers for Wireless Communications.* Artech House.

[12] Ghannouchi, F. M., & Hashmi, M. S. (2013). *Load-Pull Techniques with Applications to Power Amplifier Design* (Vol. 32). Springer Netherlands. https://doi.org/10.1007/978-94-007-4461-5

[13] Simpson, G. S. (2009) *A Comparison of Harmonic Tuning Methods for Load Pull Systems.* Retrieved from https://www.maurymw.com/pdf/datasheets/5C-053.pdf

[14] Vuolevi, J. H. K., Rahkonen, T., & Manninen, J. P. A. (2001). Measurement technique for characterizing memory effects in RF power amplifiers. *IEEE Transactions on Microwave Theory and Techniques, 49(8)*, 1383–1389. https://doi.org/10.1109/22.939917

[15] Manjanna, A. K. (2011). *Design and Development of Active Baseband Load-pull.* [Master's thesis, Delft University of Technology]

[16] Simpson, G. S. (2015) *A Beginner's Guide To All Things Load Pull.* Retrieved from https://www.maurymw.com/pdf/datasheets/5A-062.pdf

[17] Bahl, I. J. (2009). *Fundamentals of RF and Microwave Transistor Amplifiers.* John Wiley & Sons, Inc. https://doi.org/10.1002/9780470462348

[18] *How to find harmonics in electrical systems.* Retrieved from https://www.fluke.com/en/learn/blog/power-quality/how-to-find-harmonics-in-electrical-systems

[19] Andrzej, Samulak. (2010). System Analyses of Class-S Power Amplifier.

[20] Soyata, T., Copeland, L., & Heinzelman, W. (2016). *RF Energy Harvesting for Embedded Systems: A Survey of Tradeoffs and Methodology.* IEEE Circuits and Systems Magazine, 16(1), 22–57. https://doi.org/10.1109/MCAS.2015.2510198

[21] Pedro, J. C., & Carvalho, N. B. (2003). *Intermodulation distortion in microwave and wireless circuits.* Artech House.

[22] Aikio, J. P., & Rahkonen, T. (2009). A Comprehensive Analysis of AM–AM and AM–PM Conversion in an LDMOS RF Power Amplifier. IEEE Transactions on Microwave Theory and Techniques, 57(2), 262–270. https://doi.org/10.1109/TMTT.2008.2011161

[23] *What is Intermodulation Distortion?.* everythingRF. (2020). Retrieved from https://www.everythingrf.com/community/what-is-intermodulation-distortion