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Impact of the gate geometry on adiabatic charge pumping in InAs double quantum dots†

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We compare the adiabatic quantized charge pumping performed in two types of InAs nanowire double quantum dots (DQDs), either with tunnel barriers defined by closely spaced narrow bottom gates, or by well-separated side gates. In the device with an array of bottom gates of 100 nm pitch and 10 μm lengths, the pump current is quantized only up to frequencies of a few MHz due to the strong capacitive coupling between the bottom gates. In contrast, in devices with well-separated side gates with reduced mutual gate capacitances, we find well-defined pump currents up to 30 MHz. Our experiments demonstrate that high frequency quantized charge pumping requires careful optimization of the device geometry, including the typically neglected gate feed lines.

Introduction

Fast and accurate manipulation of individual charge carriers in nanoscale electronic devices is a key technology in research and development, from quantum information processing with quantum dots (QDs)[1,2] to modern quantum metrology.[3–6] In particular, the controlled transfer of electrons one-by-one provides a fundamental standard for the electrical current based on the quantized electron charge.[3] This process is achieved by quantized charge pumping (CP), in which a periodic modulation of one or several external parameters leads to a DC current of one electron per cycle, thus relating the current to the frequency standard.[3–6] The ideal pump current is thus given by $I = nef$, with n an integer corresponding to the number of electrons shuttled per cycle, e the electron charge, and f the frequency of the modulation. Recent theoretical proposals

suggest that CP can be used to investigate and characterize exotic electronic states, such as fractional quantum Hall states,[7] or Majorana bound states.[8] CP has been reported in various material systems,[9–23] ranging from MHz pump rates[9,10,17–19] to GHz frequencies.[11–13,16,20,23] Several pump modes such as single-gate ratchet pumping, two-gate pumping and turnstile pumping have been used to increase the pump frequency and accuracy in non-adiabatic[6,11,12,17] and adiabatic pump modes.[17,18,23] The impact of the device geometry in non-adiabatic CP has been investigated in single QDs.[22] Though adiabatic CP seems better suited for coherent transport of individual carriers, the impact of the device geometry in double quantum dot (DQD) pumps has not been investigated so far.

InAs NW QDs are an ideal material platform due to a large energy level spacing, originating from the small effective electron mass[24] which helps to obtain wide and flat pump current plateaus and suppresses errors due to co-tunneling in adiabatic pumps and back-tunneling in non-adiabatic pumps. Clean and stable InAs NW QDs with large charging energies deterministically formed using arrays of narrow bottom gates have been used as spin qubits[25–28] and non-adiabatic CPs.[15,16] As an alternative one may use side gates, compatible with a large variety of other nanoelectronics device designs, for example in Majorana bound state research,[29,30] Cooper pair splitters,[31,32] QD based spin valves,[33] or spin–orbit coupling[34] experiments. Side-gated QDs exhibit as clean and stable QD properties as bottom gated QDs.[29–34]

In this work, we compare adiabatic quantized CP in two InAs NW DQD devices, one based on narrow bottom gates (device A) and one on well-separated side gates (device B). We compare the pump currents in these two devices as a function of the modulation frequency and amplitude. In device A, the expected

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quantized pump currents are only observed at low frequencies up to a few MHz, while in the side gated DQD, the quantization of the CP currents is maintained up to 30 MHz. The main difference in the device designs is the mutual capacitances between the gate lines, which are significantly reduced in the side gate version. Our experiments show that the control of cross-talk between gates is crucial for the performance of adiabatic quantized CP in DQDs.

Results and discussion

Fig. 1(a) shows a schematic side view and a scanning electron microscopy (SEM) image of a suspended InAs NW DQD device (device A) with an array of bottom gates.[27] The device is fabricated by first defining an array of Ti/Au narrow bottom gates on a highly resistive oxidized Si substrate. The gates are 25 nm thick, 50 nm wide, and spaced at a 100 nm pitch. Two supporting bars with a thickness of 70 nm are then defined at both sides of the bottom gate array, creating the bridgeheads to suspend the NW. In the next step, a single InAs NW ($\sim$100 nm diameter) is transferred on top of the two supporting bars using a micromanipulator. This method results in very clean and electronically stable NW devices. Finally, source and drain contacts of Ti/Au (10/120 nm) are fabricated using conventional lift-off techniques, after using an Ar plasma etch and an ammonium polysulfide ($(NH_4)_2S_x$) wet etch to remove the native oxide on the contact areas of the NW. The NWs of both devices

are grown by solid-source molecular beam epitaxy,[35] implementing a two-step growth process to suppress stacking faults.[36]

The measurement setup is shown in Fig. 1(a). All electrical measurements were performed at 20 mK. Although we occasionally fine signatures of Pauli spin blockade at zero magnetic field in the DC measurements of device B, we note that such a spin blockade would not occur in the CP process because only a single electron tunnels through a DQD per CP cycle and the intermediate charge state is filled and emptied independently.[37,38] Two of the gates, G2 with the applied voltage V_L and G4 with V_R, are connected to semirigid coaxial cables *via* on-chip bias-tees to simultaneously apply DC and RF signals. We first characterize a single QD and a DQD without RF signals to demonstrate the flexibility of the device structure. First, we define a small single QD using the three gates G2, G3 and G4. As shown in the inset of Fig. 1(b), gates G2 and G4 form tunnel barriers between the QD and the source and drain reservoirs, while G3 acts as a tuning gate. Fig. 1(b) shows the resulting Coulomb blockade diamonds measured as a function of V_{G3} and the applied bias voltage, V_{SD}. The clean single QD characteristics, including a regular spectrum of excited states, indicates that the NW is very clean and no unintentional QD is formed in the long NW leads between the QD and the source and drain contacts, with only weak signs of closely spaced lead state resonances.[39] We note that the length between the QD and the metal contact (*i.e.* the NW lead) is $\sim$400 nm, while the QD
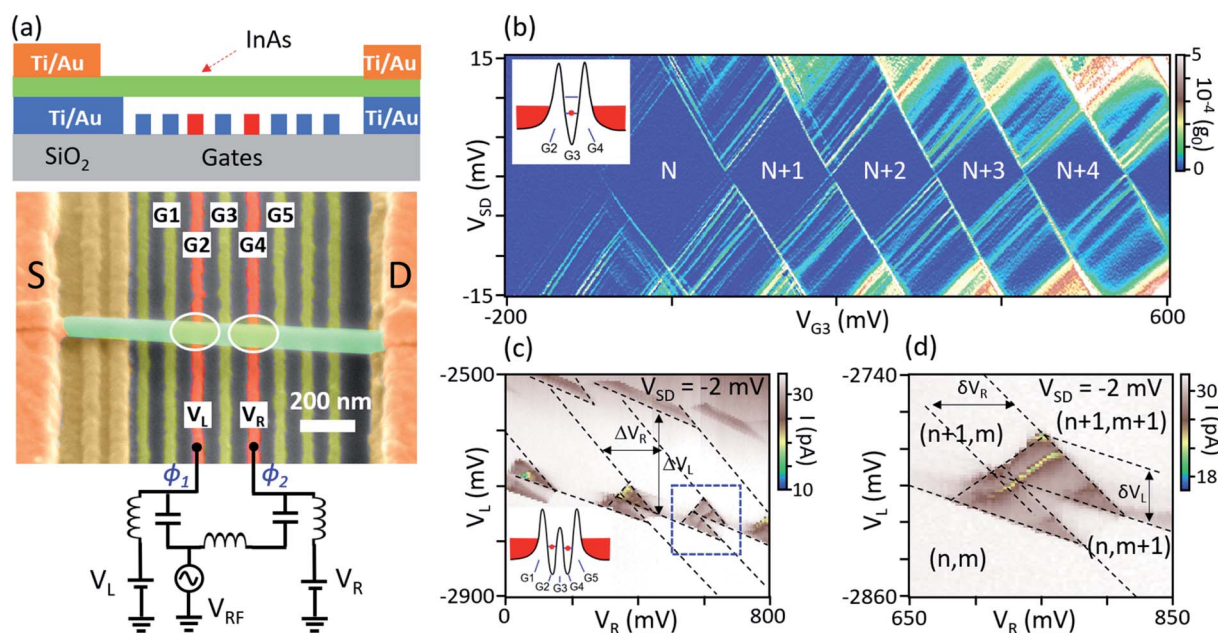

Fig. 1 (a) Schematic side view (upper inset) and scanning electron microscopy image of a suspended InAs double quantum dot (DQD) device (device A) with an array of bottom gates and a diagram of the measurement circuit. RF voltages for charge pumping with different phases are added to the DC gate voltages V_L and V_R using bias-tees. ϕ_1 and ϕ_2 are the phases of left and right RF signals, respectively. (b) Differential conductance, G, as a function V_{SD} and V_{G3} in a single dot confined between the two bottom gates G2 and G4 (see inset) by setting $V_{G2} = -6.8$ V and $V_{G4} = -4.265$ V. The differential conductance is the numerical derivative of the measured current with respect to the bias, $G = dI/dV_{SD}$. (c) Charge stability diagram of the InAs DQD measured as a function of the two gate voltages, V_L (G2) and V_R (G4) with a bias voltage $V_{SD} = -2$ mV. The DQD is formed using the three bottom gates G1, G3 and G5 (inset) by setting $V_{G1} = -2.67$ V, $V_{G3} = -2.35$ V and $V_{G5} = -2.35$ V. (d) Magnification of a bias triangle marked by the dashed rectangle in (c). The double dot charge pumping is performed in this charge state at $V_{SD} \approx$ 0 mV. The electron occupation numbers of the QDs are indicated by the ordered pairs (n, m).

size is ∼200 nm. For the QD, we obtain an addition energy of $E_{\mathrm{add}} \approx 14$ meV with an energy level spacing of ∼4.3 meV, showing the strong confinement in the small dot. Similarly, a larger QD can be formed using the G1 and G4 as barrier gates, with clean and stable Coulomb blockade resonances of a large single QD (see ESI, Fig. S1†).

We then form a DQD using the five gates, G1–G5, as shown in the inset of Fig. 1(c). G1, G3 and G5 induce the tunnel barriers, while G2 and G4 are used as plunger gates to tune the electron numbers in the individual QDs. The resulting charge stability diagram is shown in Fig. 1(c), with the current I plotted as a function of V_{L} (G2) and V_{R} (G4) at $V_{\mathrm{SD}} = -2$ mV. Fig. 1(c) displays the characteristic honeycomb pattern of a DQD with the dashed lines as guides to the eye. The total number of confined electrons is fixed in each honeycomb cell and co-tunneling is not resolved, except for a few charge transitions in the left QD, demonstrating that the DQD is in the weak-coupling limit. For this DQD, we extract the gate capacitances (C_{L} and C_{R}) between the gates G2 and G4 and the corresponding QD1 and QD2 from Fig. 1(c) as $C_{\mathrm{L}} = e/\Delta V_{\mathrm{L}} = 0.85$ aF and $C_{\mathrm{R}} = e/\Delta V_{\mathrm{R}} = 0.85$ aF, respectively. The lever arms are extracted from the extensions δV_{L}, δV_{R} of the bias triangles and the applied bias V_{SD} (Fig. 1(d)) as $\alpha_{\mathrm{L}} = V_{\mathrm{SD}}/\delta V_{\mathrm{L}} \approx 0.07$ and $\alpha_{\mathrm{R}} \approx 0.03$ for gates V_{L} and V_{R}, respectively. The total capacitance of the two QDs are $C_1 = C_{\mathrm{L}}/\alpha_{\mathrm{L}} = 12.1$ aF and $C_2 = C_{\mathrm{R}}/\alpha_{\mathrm{R}} = 28.3$ aF, while the mutual capacitance is $C_{\mathrm{m}} = (\Delta V_{\mathrm{L}}^{\mathrm{m}}/\Delta V_{\mathrm{R}}^{\mathrm{m}})C_2 = 3.6$ aF. Correspondingly, we estimate the charging energy of the left and right dot as $E_{\mathrm{C}}^{\mathrm{L}} \approx 13.7$ meV and $E_{\mathrm{C}}^{\mathrm{R}} \approx 6$ meV from the equation[40]

$$E_{\mathrm{C}}^{\mathrm{L(R)}} = e^2/C_{2(1)} \left\{ 1 - \frac{C_{\mathrm{m}}^2}{C_1 C_2} \right\}^{-1}.$$ The charging energy of the right QD is markedly smaller than that of the left QD, probably due to unequal capacitances and different QD size. We summarize the obtained parameters of the DQD (device A) in Table 1 in the ESI.† Fig. 1(d) shows a more detailed map of the bias triangle marked with the blue dashed rectangular in (c), showing clean DQD characteristics for the gate voltages for which we now discuss CP.

We perform charge pumping through DQDs by applying two phase-shifted sinusoidal voltages (ϕ_1 and ϕ_2) to two gates at $V_{\mathrm{SD}} \approx 0$ mV, using bias-tees and an arbitrary waveform generator as illustrated in Fig. 1(a). The resulting DC pump current through the DQD is measured by a current–voltage (IV) converter. The mechanism of adiabatic charge pumping using a DQD is explained in ESI, Fig. S2.†[9] The occupation number (n, m) of the DQD is varied periodically by applying two sinusoidal modulations of the voltages V_{L} and V_{R} with a 90° phase shift to the plunger gates of the respective QD, resulting in circular periodic trajectories around a triple point in the charge stability diagram. When the path on the stability diagram encircles a triple point, exactly one electron, or one hole, is shuttled per cycle from one contact to the other. The pump current is then expected to be only related to the drive frequency, i.e., $I = \pm ef$, with e an elementary charge, where the polarity of the current is defined by the pump direction.

Fig. 2(a) shows the pump current around the triple points shown in Fig. 1(d) measured as a function of V_{L} and V_{R} at a modulating frequency of $f = 5$ MHz at an RF power of $P = -32$ dBm and the bias $V_{\mathrm{SD}} \approx 0$ V. We find two elliptical regions of roughly constant current in the vicinity of a pair of triple points, highlighted by arrows in Fig. 2(a). The sign of the current is reversed around the second triple point. We optimize the phase between the two applied AC signals to obtain the widest quantized plateaus as a function of V_{L} and V_{R}. Here, the left and right phases are set to $\phi_1 = 0°$ and $\phi_2 = 70°$ (i.e. $\Delta\phi = \phi_1 - \phi_2 = 70°$), respectively. Fig. 2(b) shows the line traces of the pump current measured along the dashed line in Fig. 2(a) for $f = 3$ and 5 MHz. The pump current plateaus are observed at ∼0.48 and 0.8 pA for $f = 3$ and 5 MHz with respect to the offset current of 25.2 pA in this experiment, respectively, which corresponds accurately to $I = ef$, within the measurement accuracy of ∼40 fA. As expected, when we increase the amplitude of the RF signal from $P = -33$ to -31 dBm, the plateaus in the pump current around each triple point are extended (see ESI, Fig. S3†). We note that optimizing the phase shift between the modulated gate voltages is not trivial in this device, likely due to the capacitive coupling between the two gate lines and a non-identical frequency response of the RF components such as the bias-tees and RF cables.

As we increase the pump frequency, the deviation of the pump current from the expected value, $I = ef$, increases (see ESI, Fig. S4†). Fig. 2(c) and (d) show the current maps for $f = 25$ and 50 MHz, respectively. As shown in Fig. 2(c), the forward and reversed bias triangles with the positive and negative current form two triangles at each degeneracy point and the pump currents at both triple points are not quantized exactly according to $I = ef$. For the two frequencies in Fig. 2(c) and (d), we would expect CP currents of 4 and 8 pA, respectively, clearly not reached in both cases, especially well visible in the insets of Fig. 2(c) and (d). The triangular gate dependence of the CP current observed in device A was explained before (ref. 18) as resulting from a non-optimal phase between the two RF signals. However, here it was not possible to find the circular gate dependence expected for the ideal pump phases. This behavior could occur when a mutual gate–gate capacitance (cross-talk) significantly reduces the relative phase difference. An alternative explanation could be asymmetric tunnel couplings between the QDs and the respective reservoirs. In an ideal electron cycle at the triple point, the empty left level goes below the Fermi energy and is filled by the left reservoir. Then, it tunnels to the right dot before the left dot is filled by the right reservoir, resulting in the desired forward current. However, the direction of the current flow is very sensitive to the tunneling dynamics and the time-dependent QD occupations. If the tunnel coupling between the right dot and the right reservoir is much stronger than the coupling between the left dot and left reservoir, an electron fills the right dot first instead of the left dot and tunnels into the left dot to exit the system to the left reservoir, resulting in a reverse current. To account for phase shifts and such non-adiabatic processes, a refined model is needed, which is beyond the scope of this work. Here, we now focus on the first explanation, which suggests that the performance of the CP could be improved by reducing the RF capacitive coupling between the gate lines.[17,18,22]
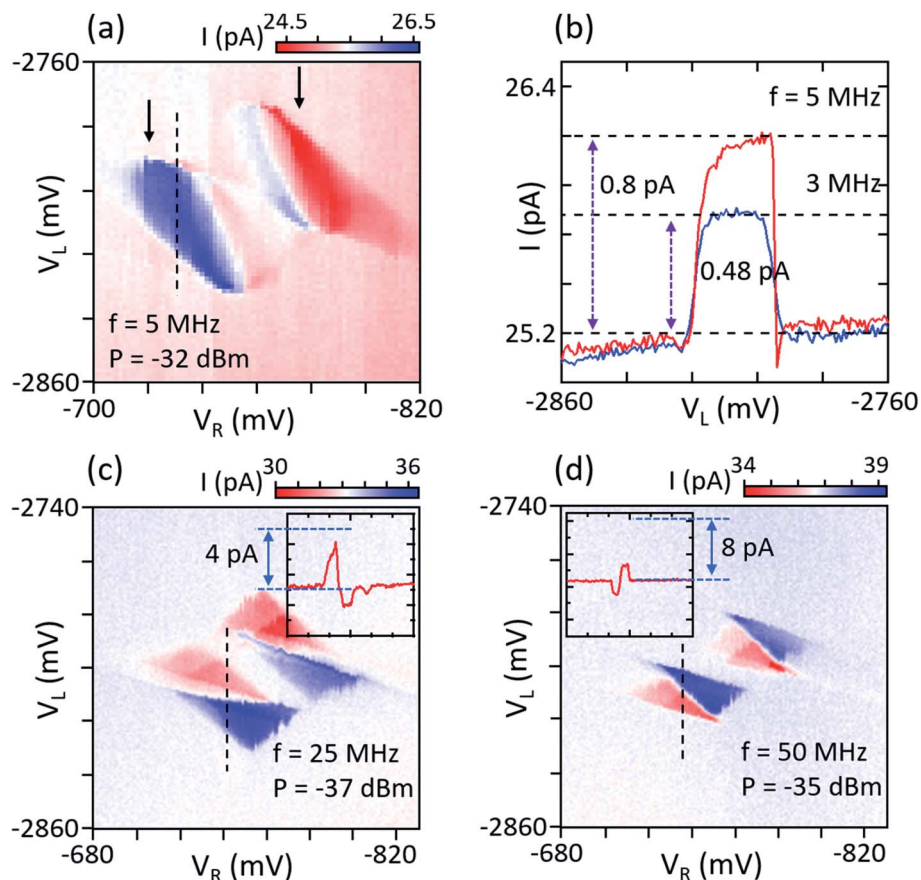
Fig. 2 (a) Pump current generated by the DQD (device A) as a function of V_L and V_R at $f = 5$ MHz and $P = -32$ dBm ($V_{PP} = 15.884$ mV). (b) Line traces of the pump current along the electron pumping cycle as indicated by the dashed line in (a) for $f = 3$ and 5 MHz. The expected level of the quantized pumping current, $I = ef$, is indicated by horizontal dashed lines. (c) Pump current measured at $f = 25$ MHz and $P = -37$ dBm ($V_{PP} = 8.932$ mV). (d) Pump current measured at $f = 25$ MHz and $P = -35$ dBm ($V_{PP} = 11.245$ mV). The insets show the line traces taken along the dashed lines. The pump currents at both triple points are not quantized exactly according to $I = ef$.

To minimize the capacitive coupling between the gate lines, we fabricated a DQD with side gates, with reduced capacitances between the gates due to a significantly increased distance between the gate lines (device B), as shown in Fig. 3(a). A nanowire taken from the same growth-batch as the one used for device A and with a similar diameter is transferred to the SiO₂ surface. Source and drain electrodes are separated by 950 nm and a DQD is formed in between. We fabricated multiple side gates to the NW, with a maximally increasing separation between gate lines away from the NW to minimize the capacitive coupling between the side gates. The separation between the left and right gates (V_L and V_R) are ~400 nm near the DQD and gradually increases further. Therefore, the distance between the gates near the DQD in device B is four times wider than the uniform bottom gates of 100 nm pitch and 10 μm long in device A (see Fig. 1(a)). We estimate the capacitances between two gates in device A and B to be ~13 aF and 0.7 aF, respectively, using a simple rectangular parallel plate capacitance model as a crude approximation, showing that the inter-gate capacitance is reduced by almost a factor of 20 in device B compared to device A. The typical resistance of the gate lines is $R \sim 1$ kΩ for both device A and B. These result in $T_{RC} = RC \sim 1.3 \times 10^{-14}$ s

and 0.7×10^{-15} s for device A and B, respectively. Similar to device A, we performed measurements with device B at 20 mK and form a DQD with the three gate voltages, V_L, V_M, and V_R as illustrated in Fig. 3(a). Fig. 3(b) displays the DC current of the DQD measured as a function of V_R and V_L at $V_{SD} = 2$ mV, showing similar bias triangles as we found in device A, including well resolved excited states. The charging energies of the two QDs are estimated from the charge stability diagrams to yield $E_{C, L} = 7.8$ meV and $E_{C, R} = 11.4$ meV for the left and right QDs, respectively. The extracted device parameters can be compared directly to device A in Table 1 of the ESI.†

We now discuss the achieved charge pumping for device B, for which we have optimized the phase shift and RF power of the two sinusoidal pump voltages (ESI, Fig. S5†). The RF signal phases have a significant impact in device B, in stark contrast to our findings for device A, consistent with a reduced capacitive cross-talk in this design. We find the optimal gate phases at $\phi_1 = 0°$ and $\phi_2 = 90°$, respectively, at which the device shows the best quantized current plateaus, as one would expect in the case without cross-talk. Fig. 4(a) and (b) show the pump current around a pair of triple points of the DQD measured as a function of V_L and V_R at a modulation frequency $f = 20$ and 30 MHz,
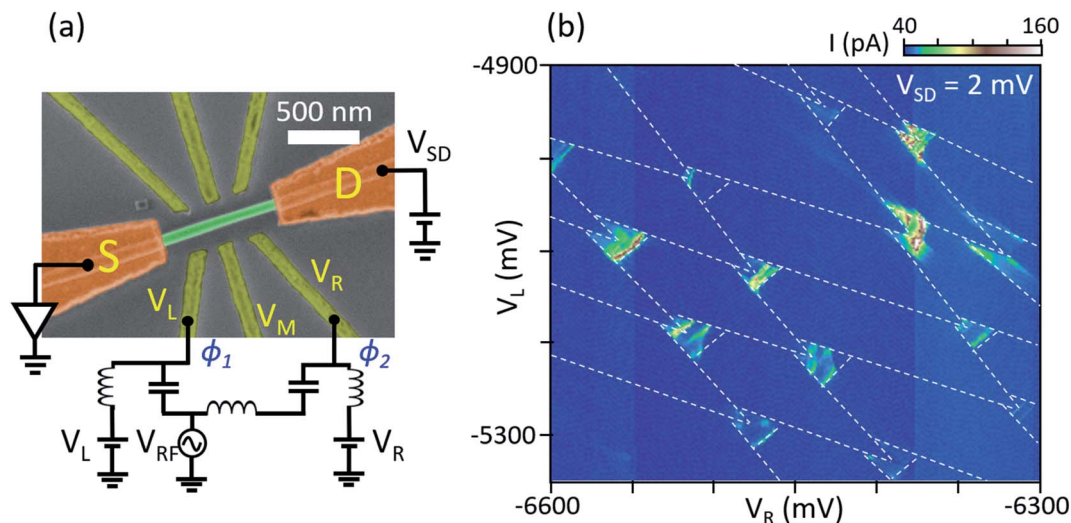
Fig. 3 (a) SEM image of side gated InAs DQD device (device B) and a diagram of the measurement circuit. All side gates are designed with a maximum separation to reduce capacitive coupling. Three gates with the applied voltage V_L, V_M, and V_R are used to form a DQD in the nanowire by setting $V_M = -4.7$ V. (b) DC current through the InAs DQD measured as a function of the two gate voltages, V_L and V_R with a source-drain bias of $V_{SD} = 2$ mV.

respectively, significantly higher than for device A and an RF power of $P = -32$ dBm. Two elliptical shapes with positive and negative currents around the respective triple point exhibit a shape much closer to the ideal case, again in stark contrast to device A. The elliptical instead of circular shapes are likely caused by asymmetric lever arms of the gates. The current plateaus correspond very well to the expected value of $I = ef$.

These findings do not change significantly up to $f = 30$ MHz, as shown in Fig. 4(b). Fig. 4(c) and (d) display the line traces of the pump current for $f = 20$ MHz, along the electron and hole pumping cycles indicated by the dashed lines in (a). Though there is a smoothly changing background current, the device shows the quantized pumping current around $I = \pm ef = \pm 3.2$ pA, indicated by the blue horizontal lines shown in Fig. 4(c) and
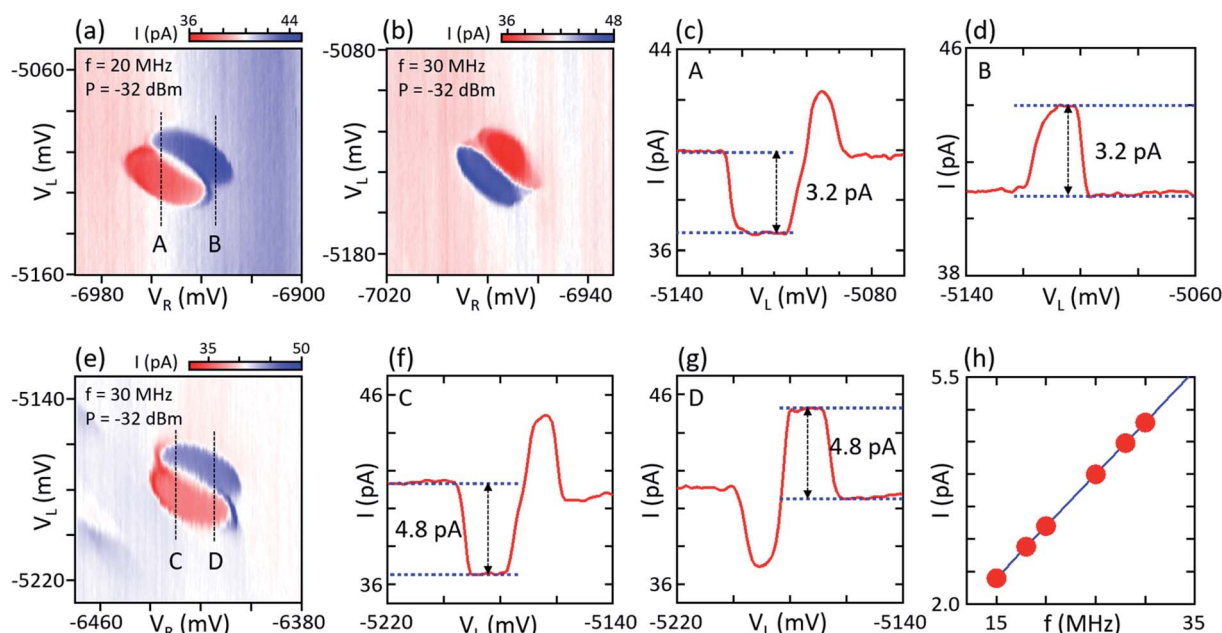

Fig. 4 Pump current at the triple points measured as a function of V_L and V_R at (a) $f = 20$ MHz and (b) $f = 30$ MHz, both with $P = -32$ dBm ($V_{PP} = 15.884$ mV). (c) and (d) Line traces of the pump current for $f = 20$ MHz along the electron and hole pumping cycle as indicated by the dashed lines (A and B) in (a). The expected quantized current value of $I = \pm ef$ ($= \pm 3.2$ pA) is indicated by horizontal dashed lines. (e) Pump current measured at a different pair of triple points for $f = 30$ MHz. (f) and (g) The line traces of the pump current along the electron and hole pumping cycles indicated by the dashed lines (C and D) in (e). (h) Frequency dependence of the pump current.

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(d). We also measure the pump current at a different pair of triple points for $f = 30$ MHz and observe similar characteristics, as shown in Fig. 4(e). Fig. 4(f) and (g) show the line traces taken along the dashed lines (C and D) in Fig. 4(e). The pump current plateaus are observed around $I = \pm ef = \pm 4.8$ pA, as expected for an ideal charge pump. As shown in Fig. 4(h), the CP current at these gate voltages scales linearly with the pump frequency up to 30 MHz, with a slope of $\mathrm{d}I/\mathrm{d}f = \pm e$, as expected. We note that at frequencies larger than $f = 30$ MHz, the pump current again starts to deviate from the fundamental relation $I = \pm ef$. Nevertheless, the quantization of the pump current is significantly improved in device B compared to device A in the range up to $f = 30$ MHz.

To check whether the asymmetric QD configuration affects the charge pump performance in our devices, we tuned the charging energies of the left and right QDs of device B to be comparable with that of device A. Table 1 and Fig. S6 in the ESI† show that the charging energy of the left QD is larger than that of the right QD, thus its QD formation is now similar to device A; the charging energies of the left and right QD are $E_\mathrm{C}^\mathrm{L} \approx 16$ meV and $E_\mathrm{C}^\mathrm{R} \approx 10$ meV, respectively. We observed very similar behaviors with the first tuning condition of device B, as shown in Fig. S6 in the ESI.† Future devices for high speed CP will benefit from such design improvements related to the capacitive cross-talk, like side gates from alternating sides of the nanowire.

The optimization of the gate line geometries is a very general approach that can in principle be employed for all CP platforms. In earlier work by Fuhrer *et al.*[15] in which InAs DQDs were fabricated on a heavily doped Si substrate and measured with DC lines for the pulse sequences, the CP operating frequency was limited to around 3 MHz and exhibited less pronounced plateaus. This suggests that capacitive coupling and RF cutoff frequencies limit higher frequency adiabatic CP. In previous experiments on non-adiabatic CP with a single gate,[16] quantized CP on a single InAs QD was possible up to frequencies larger than 1 GHz using improved high frequency cabling and a reduction of the RF losses by using undoped Si substrates. With a single gate and for non-adiabatic CP, the phase of the RF signal is irrelevant, allowing these significantly larger frequencies.

The unique advantages of a semiconductor platform come from the insight that, in addition to the capacitive cross-talk between the gate lines, other parameters are relevant for adiabatic DQD quantized CP as well. For example, the dwell times on the QDs is often characterized by the RC time constants of the tunnel barriers, where R and C are an effective resistance and capacitance characterizing the charging dynamics of the QDs. The error rate caused by missed tunneling events is expected to increase exponentially with increasing RC values for the same operation frequency, roughly $\sim \exp(1/RCf)$.[23,41,42] Recently, in a graphene DQD device with a factor-of-ten smaller value of the RC time constant compared to conventional metal-oxide junction devices, GHz adiabatic quantized CP has been demonstrated.[23] In this device, well-separated side gates were used-in accordance with our results. However, in graphene, the tunnel barriers are formed by constrictions and cannot be controlled by gate voltages, because graphene is a semimetal. In contrast, a semiconductor can have gate tunable barriers, which, in principle, should allow one to tune also the RC time and thus to obtain significantly higher pump frequencies.

To further improve the charge pump performance in DQDs with multiple gates, it is essential to reduce the cross-talk of gate voltages to QD potentials and interdot tunnel couplings. Recently, an efficient calibration technique for reducing such cross-talk in multi-dot systems with multiple gates has been developed by introducing virtual gates as linear combinations of physical gate voltages.[43-47] As shown in our experiments, a minimal cross-talk between gate lines and DQDs is essential for CP, so that it should also be possible to employ the technique of virtual gates to improve CP, resulting in additionally optimizing the relative amplitudes of the drive signals.

Conclusions

We have demonstrated adiabatic quantized charge pumping in InAs nanowire DQDs with two different device geometries, one with an array of narrow bottom gates and one with well-separated side gates for which we have investigated the pump current as a function of the modulation frequency and amplitude. For the closely spaced bottom gate array, the charge pumping is quantized accurately only up to a few MHz, with CP current patterns consistent with a non-ideal phase between the two RF signals, which cannot be corrected due to a strong capacitive coupling between the bottom gates. For a very similar device with well-separated side gates, we find close to ideal pump current patterns and quantized current levels for frequencies up to 30 MHz. Our experiments demonstrate that it is essential to optimize the device geometry for the accurate operation of high speed single electron adiabatic CPs, including the gate feed lines.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

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