A built-in self-test module for 16-bit parallel photon counting circuit using 180 nm CMOS process

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S. Isaak[1], H.C. Yeo[1, 2], C.K. Chang[1,3] and Y. Yusuf[1]

[1]School of Electrical Engineering, Faculty of Engineering, Universiti Teknologi Malaysia, 81300, Johor Bahru, Johor, Malaysia

*Corresponding author: stalinyeo97@gmail.com

Abstract. This study investigated the use of a built-in-self-test (BIST) module detecting catastrophic errors in photon-counter accumulator for liquid contamination level measurement. Efficient algorithms are exceptionally demanded for a high-count rate and low voltage system photon counting circuit on-chip. The photon counter sensors are also required high sensitivity digital counter that encodes the arrival of photon in precise timing to prevent any count erroring the absence of light. The proposed BIST is integrated on the data acquisition system, where the accumulator is located. The design circuit, functionality and topology tests of BIST and circuit under test are realized with 180 nm Silterra CMOS Process. The same Verilog codes are verified using field programmable gate array (FPGA) to predict the hardware functionality prior fabrication. The measurement was able to detect at least 90 % fault coverage within 16-bit data acquisition system at minimum operating frequency of 166.7 MHz.

***Keywords*:** photon counting, data acquisition, BIST, FPGA, ASIC.

1. Introduction

Error screening or fault diagnosis is highly demanded as the device scaling of Complementary Metal Oxide Semiconductor (CMOS) shifts towards the deep submicron range. This evolution boosts up into a compact and high-speed device integration, but also initiating the problem with dark or leakage current, propagation delay sensitivity and reliability issues [1], [2]. A fast data acquisition (DAQ) counting system is also considered the error diagnosis method to minimize the metastability effects due randomly toggling the asynchronous input at high-speed domain [3]. A very large-scale integrated circuit (VLSI) sector has been used parallel prefix adder (PPA) for digital counting system due to its feature of small computation delay. The accumulator module in PPA is acted as the binary adder element in arithmetic logic unit (ALU) contributes to the impact of high-speed processing task. Besides, PPA is capable in reducing the area consumption of large binary counter [4]. Kogge Stone Adder (KSA) has the potential as the high-speed PPA that can produce bounded fan-out and minimum logic depth domain which can create the least number of black cells on die [5].

Single photon counting system is widely used in many applications involved with very weak signal detection including in biomedical sensing, astronomy, light-wave sensing and imaging. In general, the avalanching effect by the Single Photon Avalanche Diode (SPAD) will generate coincidence current signal due low-level detected photon absorbed in medium element such as water, soil, and metal. The current signal will be converted to voltage by SPAD and amplified before converted into digitized signal.

As reported earlier, the total photon detected can be computed using integrated data acquisition (iDAQ) with sparse tolerant system at high frequency beyond 100 MHz [6]. The iDAQ consist of 16-bit photon buffer, 16-bit sparse KSA and parallel-in parallel-out (PISO) shift register, whereby spares KSA is acted as fault tolerance module. Hence, Chong et. al [7] work is improved by Chang et.al [6] using sparse KSA module with fault tolerance capability.

One way to aid the iDAQ designed by Chang et. al [6] with hardware testability feature is by the integration with built-in self-test (BIST) scheme due to its advantages on the rated clock test and economical advantage compared to Automatic Test Equipment (ATE) [8]. In general, BIST scheme is replicated the function of ATE for error screening on circuit under test (CUT). BIST scheme is explicitly performed as fault diagnosis method for integrated digital module such multiplier chain, embedded memory and bootstrapped switches [9]. However, there are few works or findings on the fault diagnosis schemes for photon counter accumulator circuit, specifically can test the normal count and false count [6], [7].

In this study, a BIST scheme which is designed using 180 nm Silterra CMOS Process is proposed for detecting metastability faults in iDAQ. Section 2 describes the integrated BIST-iDAQ structure. Section 3 presents the characterization performance with the addition of BIST scheme. The fault coverage, functionality and physical design optimization of the proposed approach is discussed in Section 4. Finally, the conclusions of this study are outlined in Section 5

2. Integrated BIST-iDAQ Module

In this study, the BIST-iDAQ consist of iDAQ as CUT and and proposed BIST. The CUT consists of three CUTs including 16-bit photon buffer (CUT-1), KSA (CUT-2) and PISO(CUT-3). The proposed BIST scheme is the integration circuit of built-in-logic block observer (BILBO), test pattern generator (TPG), output response analyzer (ORA) and the test controller as shown in Figure 1. BILBO has four multifunctional control modes when screening the incoming signal. The control modes of BILBO circuit as shown in Figure 2 are tabulated in Table 1. When B_1B_2 are asserted to *00*, BILBO will perform serial scan mode. If the B_1B_2 are changed to *01*, Linear feedback shift register (LFSR) is activated, then BILBO would become a pseudo-random pattern generator. BILBO is acted as normal D flip-flop when the B_1B_2 are *10* to save all the parallel data for 1 clock cycle. In multi-input signature analyzer (MISR), BILBO would turn into a signature analyzer [10]. The design and characterization are implemented using Synopsys EDA tools.

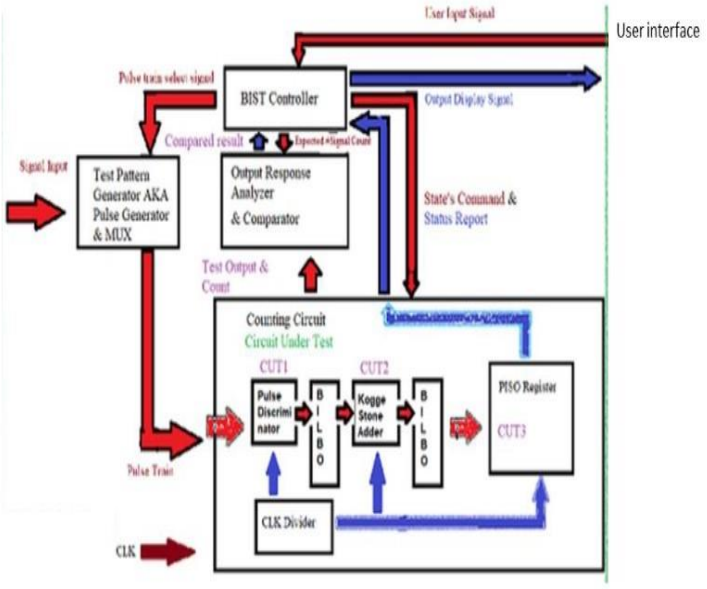

Figure 1. The block module of the Datapath unit (DPU)

Table 1. The control modes of BILBO [10]

B_1B_2	Mode
00	Serial Scan Chain
01	LFSR Pattern Generator
10	Normal D-flip-flop
LFSR	MISR Response Compactor

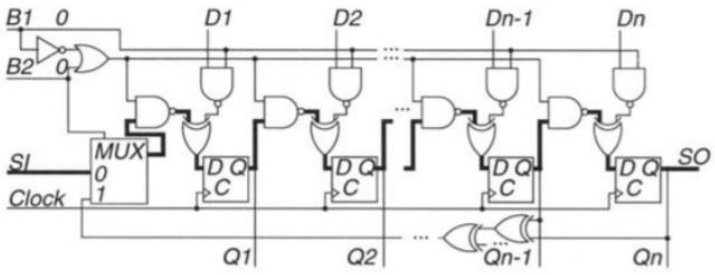

Figure 2. BILBO circuit [9]

2.1. Datapath Unit

Figure 3 shows the block diagram of the datapath unit (DPU) of integrated BIST module. The DPU uses multiplexer to control the processing mode, including normal and test modes. When the normal mode is selected, the data flow N [15:0] would only pass the sampling data to the CUT-1, CUT-2 and PISO and CUT-3 based on their behavior without fault diagnosis test.

During test mode, the incoming data would be blocked using entrance multiplexer, whereby the entrance multiplexer would generate test pattern from test pattern generator module. When CUT1 receives the data, BILSO-1 produces the output response signatures and the comparator would compare the produced signatures with existing signature stored in ROM. To test CUT-2, the BILBO-1 would act as the test pattern generator, meanwhile BILBO-2 generates output signature. The generated signature tested on CUT2 will be analyzed in comparator module to verify the functionality of CUT-2. BILBO-2 acts as test pattern generator for testing CUT-3. The generated signature will then be analyzed by the output response analyzer. The BIST controller would then report the faulty part of three CUTs.

2.2. Controller Unit.

The controller unit (CU) was designed to test the CUT-1, CUT-2 and CUT-3 in sequence order. Any CUT fails in the test mode is prohibited to the next stage of data processing until the algorithm is reconstructed to overwrite the error as illustrated in Figure 4. The controller has a reconfigurable timing system to control the number of test pattern generator cycle. It is also having a critical timing scheme to extract the signal from the output response analyzer.

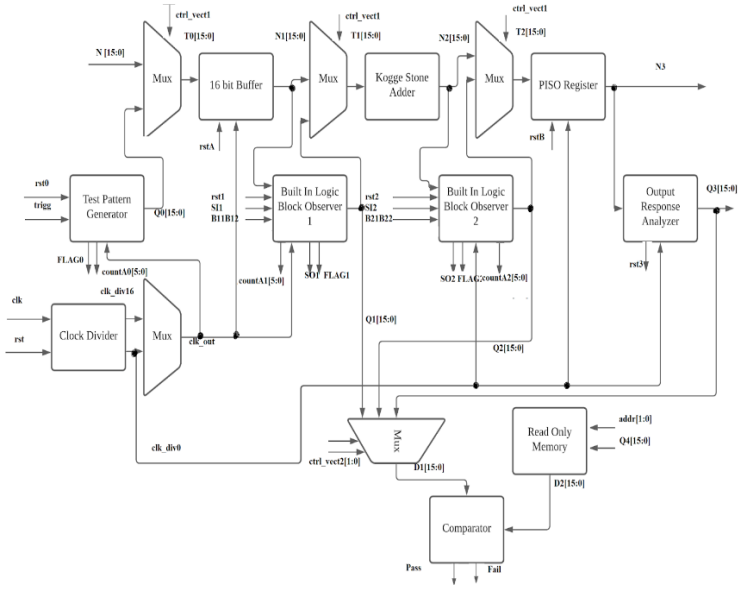

Figure 3. The block module of the Datapath unit (DPU)

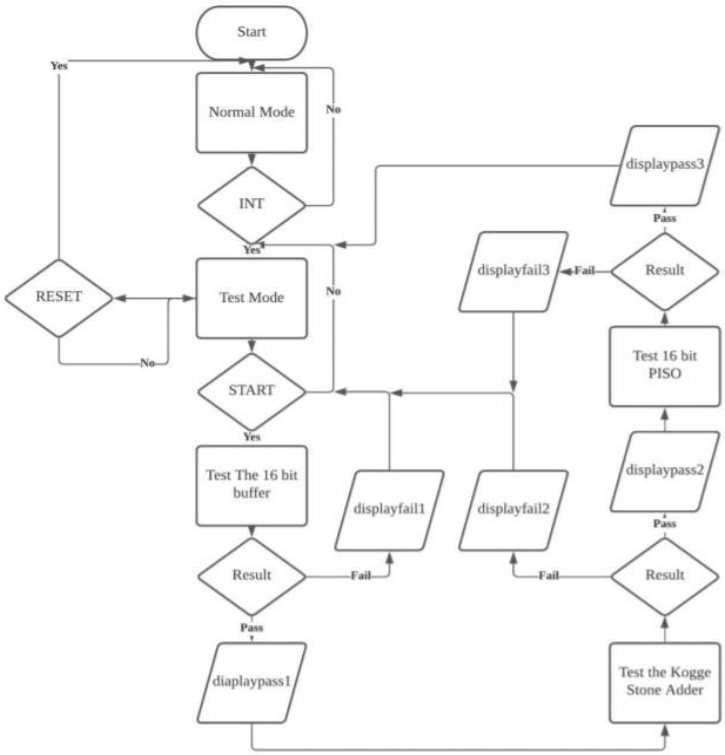

Figure 4. The controller unit algorithm

3. Characterisation and Functionality Results

In this section, the finding results from both ASIC and FPGA implementations are explained to verify the functionality of the proposed BIST module for photon counting system. The results analysis is reported the determine whether the metastability was caused by the timing system or the other factors like delay due to size of integrated circuits on BIST module. To evaluate the proposed BIST module, three CUT circuits were tested including CUT-1, CUT-2 and CUT-3.

3.1. Simulation Results

In general, the testing would be in "pass" mode if the CUT doesn't have any physical defects or capacitances failure. As shown in Figure 5 (a), when the Q1 output of BILBO-1 and Q4 data from ROM are matched, then CUT-1 is permitted at the output display module as the passed data (logic '1' is asserted). This process is repeated to test CUT-2 and CUT-3 and the simulated results are depicted in Figure 5 (b) and Figure 5 (c) respectively.

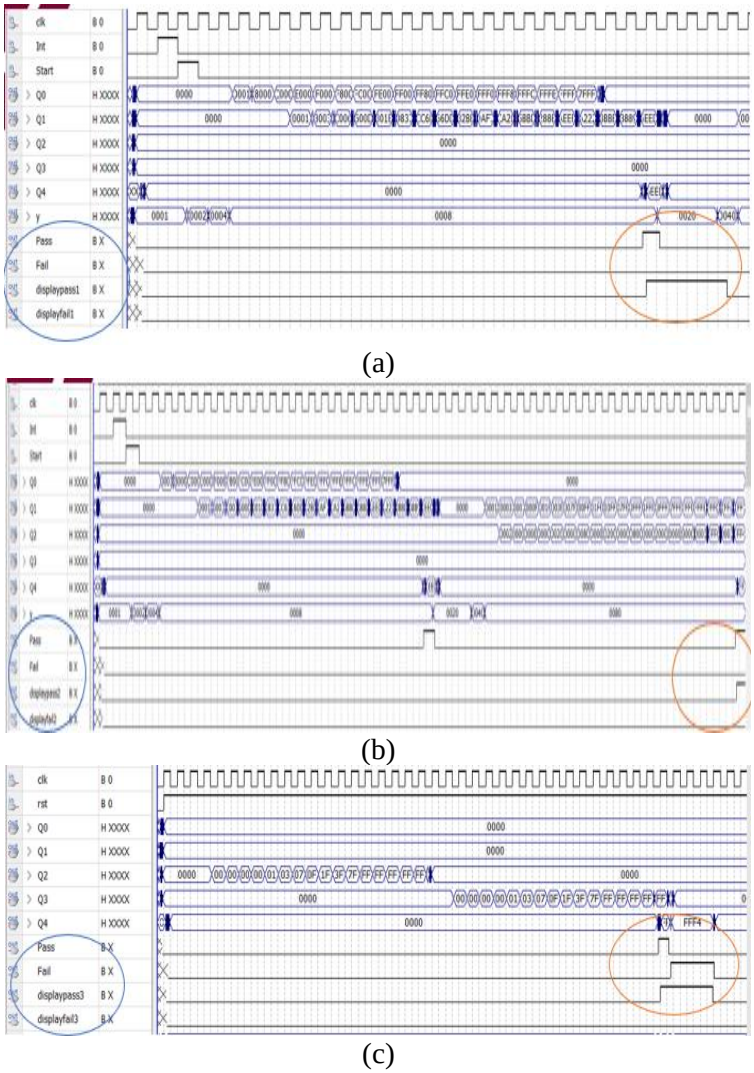

Figure 5. (a) Pass Test CUT-1 **(b)** Pass test CUT-2 **(c)** Pass Test CUT-3

3.2. Physical Implementation ICC

In order to examine the core utilization of the proposed BIST, Integrated Circuit Complier (ICC) test was implemented. The constraint core utilization is set as 0.90 (ratio number, no unit) for best performance of power and area, which is similar reported by earlier findings iDAQ system without fault testing circuit using 180 nm CMOS Process [7]. The setup time (t_S) and the hold time (t_H) are simulated as 0.36 ns and 0.26 ns of the slack time. Hence, the integrated DAQ with BIST scheme can operated with frequency nearly 2.77 GHz. The dynamic power consumptions, leakage power and total power obtained are 2.86 mW, 963.64 mW and 2.86 mW. The simulated cell area is 0.0312 mm^2, where 0.00835 mm^2 by means 26 % of the cell area is consumed by CUT circuits. These finding results are defined in Table 1. The BIST module which is integrated with CUT schemes showed significant improvement of fault diagnosis by examine each CUT in sequence and is able to tolerate with signal verification to ensure all incoming signal can be processed. The ASIC performance comparison between the earlier iDAQ without BIST scheme [7] and with BIST scheme is tabulated in Table 2.

Table 2. Parameters comparison with and without BIST module.

	CUT	CUT with BIST
Operating frequency (MHz)	166.67	166.67
Cell Area (μm^2)	8349.26	31244.87
Cell Leakage Power (nW)	295.96	963.64
Total power (mW)	0.573	2.856

Figure 6 shows the layout of integrated BIST-iDAQ module. The layout had passed the design rule check (DRC) and layout versus schematic (LVS) that can ensure no post fabrication problem in the future.

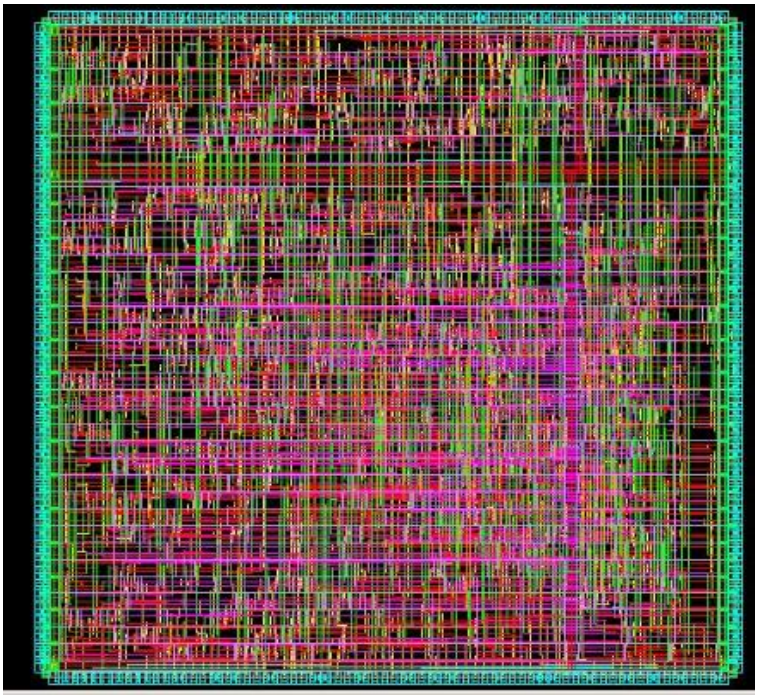

Figure 6. ASIC layout implementation of BIST System.

3.3. Hardware test using FPGA

Prototype hardware test is required to predict the functionality of BIST-iDAQ prior fabrication. The same DAQ design which is implemented by Chong et. al [7] already tested using prototype circuit on De2-FPGA. However, this prototype circuit encountered with the error occurs due to the analog to digital signal conversion. The percentage of error between the actual counting and the experimental counting is about 10 -15 % [11]. This weak performance has encouraged the prototype hardware test using DE1-Soc which promising more accurate digital processing module. The De1-SoC board is programmed using the same RTL algorithm of integrated BIST-iDAQ module for ASIC implementation. The internal clock is reduced to 1 Hz for visual inspection on BCD display and LEDs on De1-SoC board. The photodetector module is interfaced with BIST scheme on FPGA. The test is conducted using contaminated water with blue dye with various contamination ratio. The detected signal will be amplified using transimpedance amplifier, when the photodetector receives photon which

penetrates through the sample. The amplified signal is sent Analog to Digital (ADC) [12] and the digitized signal is accumulated and tested for count error on FPGA board.

During the Normal Mode, the contamination level of 90 % and photon count of 145 per second were measured using BIST scheme on FPGA, as shown in Figure 7. Figure 8 shows the generated BCD display when the FPGA is performed the BIST Mode for CUT-3. The BCD displays indicate which CUT module has passed with fault free. When any of LEDR 1, 5, and 8 (count from right to left) is light up, represent either CUT-1, CUT-2 or CUT-3 has passed the Test Mode on FPGA. At the same time, the BCD display point out which CUT circuit is tested for error. The BCD displays will display 0020, 0200 and 2000 when CUT-1, CUT-2 and CUT-3 are tested in sequence.

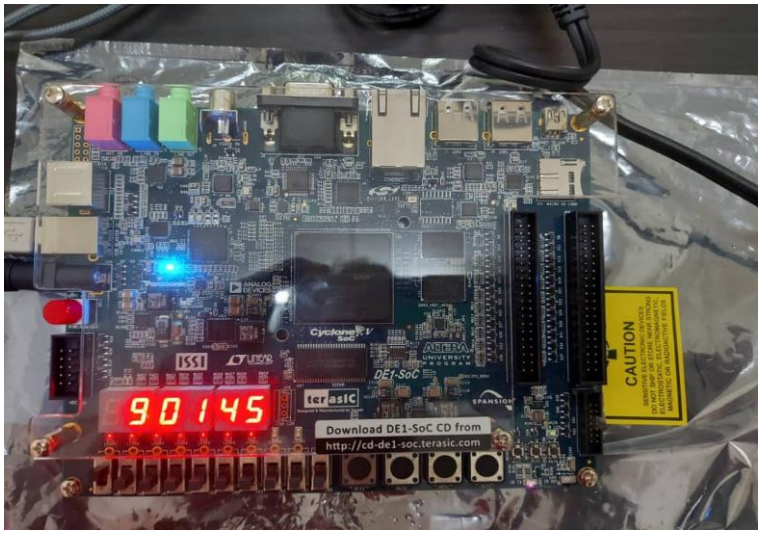

Figure 7. The normal mode of BIST scheme on FPGA

Figure 8. CUT-3 is tested with BIST scheme on FPGA

4. Discussions

The metastability problem when injected with a randomly toggling asynchronous input at high speed [6, 7] has been overcome with the proposed BIST-iDAQ module. The functionality of chip without

using automatic testing equipment (ATE) is explicitly performed using FPGA. Due to optimized lowest cell area, dynamic power and propagation delay at 0.5 ns, these findings extend the possibility of BIST-iDAQ to be perform for high-speed photon counting system. As observed from the area report, CUT with BIST took a large cell area due to the existence of 16-bit KSA. Several verification and ICC test of another parallel prefix adder is suggested to replace the 16-bit KSA module. Brent-Kung Adder (BKA) is one of the best options in reducing the complexity and area consumption of the BIST system [13], [14]. Currently, the BKA designed by Ndottiwa et. al [13] is already integrated with the DAQ design by Chong et. al [7] at counting rate of 2.5 GHz. Therefore, this result is promising optimized performance with the inclusion of BIST scheme. In addition, parallelized the testing procedures need to be considered to support the BIST system with small operation time, which then possible to produce better power and area performance.

5. Conclusions

We have demonstrated that the data sent by TPG can be tested for fault diagnosis using proposed BILBO-1 and BILBO-2 architectures. We have also shown that the BIST-iDAQ system on chip can provide high speed counting system with optimized lowest cell area, dynamic power and propagation delay at 0.5 ns. By using hardware implementation on FPGA, the BIST controller is able to generate similar fault diagnosis found with simulation using Synopsys with operating frequency at 166.7 MHz. However, a large cell area due to the existence of KSA and its complexity affected the propagation delay, which limits the count rate beyond 2 GHz. Therefore, BKA design will be considered to obtain smaller propagation delay to encounter the problem with lower BIST module performances after fabrication process. To our knowledge, the external ATE is costly when CUT has high clock rate of 1 GHz due to poor inductance and expensive tester pin costs. We expect this approach to allow new variations of CUT design and frame time settings for BIST module on photon counter circuit.

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