Coupling of photonic waveguides to integrated detectors using 3D inverse tapering

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***Abstract*—We report on the design, fabrication, and characterization of a Silicon Nitride (SiN)-based integrated photonic chip in which the dielectric waveguides are coupled to photodetectors integrated homogeneously into the Silicon substrate. The photonic-electronic coupling was realized by a 3D inverse tapering of SiN waveguides. The novelty of our approach consists in tapering the waveguide in the vertical direction by means of an engineered wet chemical etching. This allows for a smooth transition from a full-height to an arbitrarily thin waveguide thickness at the detector location, expanding adiabatically the optical mode towards the latter. The measured chips showed a responsivity $R \approx 109$ μA/mW and a corresponding quantum efficiency of 16% at an excitation wavelength of 850 nm. Our technological solution offers a versatile method for a top-down monolithic integration of lightwave circuitries with substrate-located photon sensing devices.**

I. Introduction

In recent years Photonic Integrated Circuits (PIC) experienced enormous growth [1], [2], [3]. By sharing a large common basis with the mature semiconductor technology, silicon and silicon nitride materials are used to fabricate photonic devices within CMOS facilities, permitting the development of PICs in well-established fabrication plants.

Integration of PICs with photon detectors requires a coupling scheme to transfer the optical power from the waveguide to the detector region. Recently, several strategies have been developed to couple photonic and electronic components for example with SiGe detectors [4] mainly in SiN, SOI and SIN/SOI platforms, as summarized In Table I.

This has become an important topic, especially to foster emerging quantum technologies where the coupling efficiencies with external detectors hampers the development of quantum integrated photonic circuits, and thus research toward integrated solutions is thriving [12], [13], [14], [15].

This work demonstrates a novel approach to inverse tapering which enables the coupling of SiN waveguide to a Si photodetector integrated in the substrate.

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We acknowledge the support of the MNF Laboratory staff of FBK during sample fabrication. We wish to thank Lucio Pancheri and Georg Pucker for useful discussion. We acknowledge financial support from the Autonomous Province of Trento, under the initiative *"Quantum at Trento - Q@TN"*, projects *Q-PIXPAD* and *CoSiQuP*. This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreements No 777222, ATTRACT *INPEQuT* and No 899368, *EPIQUS*.

TABLE I
PERFORMANCE COMPARISON

Measured Responsivity		
Work	active layer thickness [μm]	R [A/W]
This work	3	0.11
[5]	10	0.3
[6]	other (polysi) 0.15	0.8
[7]	other (SOI) 0.22	0.44
[8]	other (SOI) 0.22	0.32
[9]	other (SOI) 0.25	0.74
[10]	other (transf. SOI) 0.22	0.19
[11]	other (SOI,λ =685nm) 0.25	0.83

The conventional approach for the realization of an inverse tapering consists in reducing the waveguide width during the pattern definition stage. While this option does not require additional fabrication steps, it is often challenging to reduce the waveguide to an arbitrarily small width without incurring in lithographic limits on critical dimensions. Here, we exploit a chemical wet-etching process to reduce locally the cross-section of the waveguide in the vertical direction (Fig. 1). This, combined with conventional lateral tapering, enables a complete 3D inverse tapering that allows the waveguide losses towards the substrate to be locally enhanced in the region where the photodetector is located. Our approach is largely independent on the lithographic constraints on the waveguide. The fabricated devices show up to 16% quantum efficiency at NIR wavelengths, subject to large improvements upon further optimization of the fabrication process.

The paper is structured as follows: in section II, we describe the device concept and simulations used to design it. Section III illustrates the fabrication process. In section IV, the optical and electro-optical characterization of the device are discussed. Finally, section V summarizes the results and draws conclusions.

II. Numerical simulations

Our approach to waveguide-detector coupling exploits the mode expansion by inverse tapering which allows the optical mode to leak efficiently into the substrate at the detector position. This can be achieved by tailoring the waveguide dimensions from a large cross-section to a weakly guiding small-core one by reducing the thickness of the waveguiding layer, as sketched in Fig. 1(d). The technique used for a shallow-angled wedge formation on thin films is used to shape photonic structures in the vertical dimension, allowing the creation of a smooth transition between two regions in the same photonic layer having different thicknesses [16], [17], [18]. Such transition in the vertical direction can be eventually

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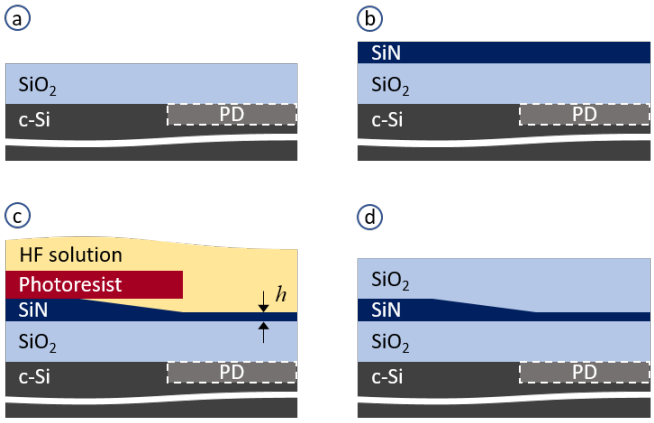

Fig. 1. The sketch of the fabrication process to realize wedge profiles in photonic waveguides. (a) The Si substrate, in which the photodetector devices are already realized, is covered by a thick SiO_2 cladding, (b) followed by the deposition of the waveguiding SiN film. (c) The photoresist patterned SiN film is etched in a buffered HF solution to realize a wedge profile. The thickness h of the etched SiN film can be controlled via the etch duration. (d) The 3D-shaped PIC layer is covered by an SiO_2 top cladding.

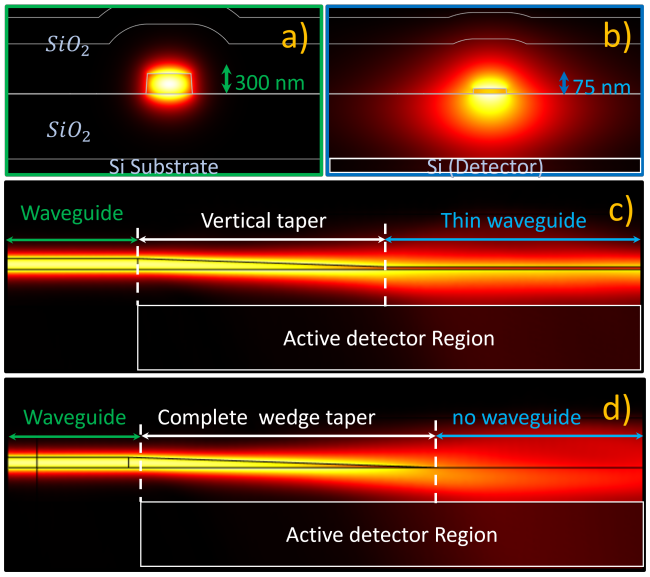

Fig. 2. Numerical simulation of electromagnetic field intensity in (a) the PIC region, where the waveguide is large enough to contain the field, (b) at the detector region, where the reduced waveguide height does delocalizes the mode and leaks into the substrate. (c) A side-view of the waveguide. The waveguide is 300 nm thick in the PIC (left), and is progressively thinned in the vertical taper region via wet-etching (center). Finally, the waveguide with a reduced height of 74nm allows the mode to leak energy into the underlaying photodetector (right). (d) The wedge-terminated waveguide does not scatter towards the top due to cladding confinement while it couples to the substrate at the bottom.

paired with an in-plane tapering by using standard lithographic techniques to create a complete 3D tapering of the waveguide.

The device under study consists of an electronic-photonic integrated circuit structured as follows. The epitaxial Silicon substrate hosts the photodetectors, formed by ion-implanted p-n junctions. The photonic layer is formed on top of the substrate and consists of single-mode waveguides which allow for

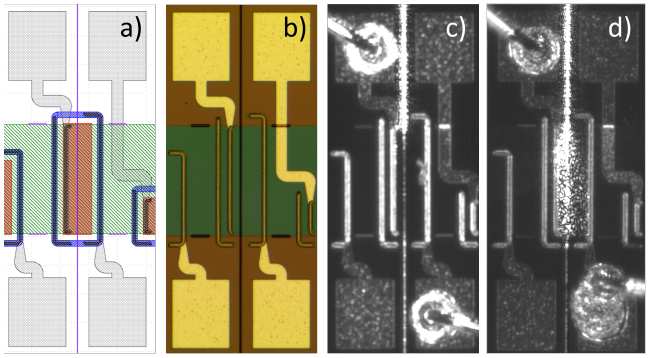

Fig. 3. (a) The CAD layout of the detector showing the active p- (red) and n-doped (blue) regions, (purple) waveguide and (grey) pads. The green area represents the region where the waveguides height is reduced. (b) An optical micrograph of the fabricated device. (c) Light coupling from the thin waveguide to the detector. (d) Light coupling from a wedge-terminated waveguide to the detector.

guided mode propagation without losses towards the substrate. At the location of the p-n junctions, the light is transferred from the waveguide to the underlaying photodetector via 3D inverse tapering of the waveguide. While our numerical simulations are performed for SiN-based single-mode channel waveguides, the method described here is general and can be extended to other photonic material platforms and waveguide geometries. Numerical simulations, performed using the Finite Elements Method (FEM), allow to obtain the geometrical parameters and the modal characteristics of the waveguides. In particular, the channel waveguides of 300 nm height and 700 nm on top of $\sim 1\mu$m SiO_2 bottom cladding allow for single mode propagation with low loss towards the Si substrate (Fig. 2(a)). Figure 2(b) shows the small core region after the tapering, where most of the mode energy is squeezed out of the core of the waveguide down into the substrate-integrated photodetector with a corresponding loss of 2400 dB/cm. In this case the waveguide width and the height are reduced to 500 nm and to 75 nm, respectively. Figure 2(c) shows the distribution of the electromagnetic field intensity in the transverse cross-section of the waveguide. In this case, light propagates from the thick waveguide on the left towards the small waveguide on the right, passing through the wedge transition. Underneath the thin portion of the waveguide, the light is collected within the active region of a photodiode. The complete inverse tapering case, where the waveguide thickness is brought down to zero, is shown in Fig. 2(d). Here, above the photodetector, the light is essentially confined within the top SiO_2 cladding and the highly absorbing Si substrate.

III. Device Fabrication

The devices were fabricated starting from 6-inch epitaxial Si substrates in which, first, the photodetectors were realized by ion implantation of Phosphorous and Boron to form the p-n junctions. The photodetectors have an elongated shape following the waveguide trace in order to permit an efficient collection of the evanescent light field within an extended region. Figure 3(a) shows the CAD layout of the detector region, where the Phosphorous and Boron doping regions are

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visible highlighted in red and blue, respectively. On top of the Si substrate, a 1050 nm thick bottom SiO_2 cladding layer of is deposited in order to isolate the PIC from the substrate (see the sketch in Fig. 1(a)). Next, the wafer is covered with a 7 nm thin film of Si_3N_4 via Low-pressure Chemical Vapour Deposition (LPCVD) to realize an etch-stop layer, the utility of which will be explained in the following. Then, a SiN film of 300 nm is deposited via Low-frequency (380 kHz) Plasma-enhanced Chemical Vapour Deposition (PECVD) to form the the photonic device layer (Fig. 1(b)).

At this stage, the definition of the vertical tapering is realized by opening a window in the photoresist at the location of photodetectors and wet etcing the SiN film in a buffered HF solution (BHF) (Fig. 1(c)). While the wet etching consumes slowly the SiN film isotropically, at the same time, the BHF erodes progressively the interface between the photoresist film and the SiN layer, promoting an additional etching front at the photoresist-SiN interface. For appropriate combinations of the etched material, the adhesion promoter and the curing process of the photoresist, the etching speed along the photoresist-SiN interface can be made faster than the isotropic etching rate of the SiN film itself. This situation generates a triangular-shaped etching front, producing the wedge-shaped transition shown in Fig. 1(c). We have produced different wafers in which the SiN film was either thinned down to 75 nm or eliminated completely to form a complete inverse tapering. The latter situation can be achieved precisely due to the presence of the etch-stop Si_3N_4 film which prevents ethcing of the bottom SiO_2 cladding. The procedure, physics, and mathematical description of the wet-etching process are described in more detail in [19], [20].

After the realization of the wedge tapering, the waveguides were patterned with i-line stepper lithography and reactive ion etching (RIE), shown as purple lines in Fig. 3(a). Then the waveguides were treated thermally at 975°C for 1 hour in an N_2 atmosphere to release the residual hydrogen from the PECVD film, and to activate the doping in the epitaxial substrate. Next, the wafer was covered with another 7 nm thick LPCVD Si_3N_4, followed by a deposition of 1μm thick Tetraethylorthosilicate (TEOS) SiO_2 which acts as a top cladding (Fig. 1(d)).

The wafer was then patterned with stepper lithography to realize vias through the top cladding, the intermediate Si_3N_4 film and the bottom SiO_2 to allow the deposition of metal contacts in the doped regions. The vias were formed via Deep RIE. Additional non-contacting vias were etched in various regions of the chips close to the waveguides and the detectors, which were later filled with Aluminium to form barriers for stray light travelling in the oxide layers. The wafer was then covered with a 1.2μm thick layer of Al-1% Si alloy, sputtered at 200°C, in order to contact the p-n junction. The metallic film was patterned into wires and contact pads via lithography and defined with RIE. Figure 3(b) shows an optical micrograph of the realized device. It's worth noting the elongated shape of the Aluminium vias that form a mirror-cage in the cladding all around the photodetector region except in the proximity to the waveguides. Finally, the diced chips were wire bonded to PCB boards for optical/electrical characterization. Figure 3(c) and Fig. 3(d) show two devices with bonded electronics, with thinned waveguide and complete inverse tapering, respectively. The light here is injected into the waveguide from the top part of the figure towards the bottom.

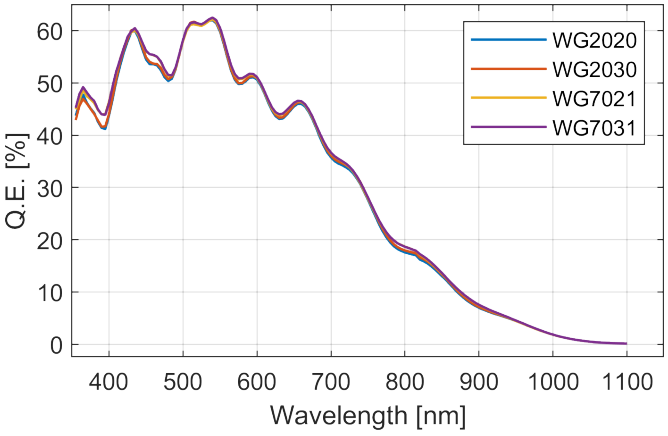

Fig. 4. The quantum efficiency of the diodes exposed to a normal illumination from an external spectral source. The spectral features with ≈ 50 nm of period are due to thin-film interference of the cladding covering the photodiode.

IV. Measurements

First, the photodiodes were characterized for normal incidence responsivity, that is, from external illumination from an external source directly impinging on the detector surface. The current at -1 V bias, generated by excitation from a spectral lamp, was measured and power-normalized with a calibrated detector. Figure 4 shows the spectral responsivity to normal incidence of four photodiodes. The responsivity remains substantially identical for the different devices, with spectral features with a period of ≈ 50 nm due to thin-film interference of the cladding film on top of the photodiode. We have investigated the waveguide-coupled quantum efficiency (Q.E.) at a wavelength of 850 nm, where the PIC is expected to operate. However, the responsivity of the silicon detectors is higher at shorter wavelengths, and thus the method is more efficient for devices operating with visible light.

Next, the devices were tested for excitation from the integrated waveguide by using the setup shown in Fig. 5(a). Light from a laser diode emitting at 850 nm is injected into the waveguide using a tapered lensed fiber. The light travels in the waveguide until it reaches the region above the detector. Here, the waveguide geometry is varied to expand the mode profile into the underneath detector, where a photocurrent is generated and measured with the sourcemeter. After the detector region, the waveguide cross-section is tapered back to its original dimensions. The residual light is then collected at the output facet with another tapered lensed fiber and sent to an external Si detector. In order to estimate the Q.E. of the photodetectors with respect to the PIC we have estimated the light power in the waveguide right before the coupling region with the photodetector. This estimation is realized by subtracting from the calibrated 5 mW source the optical losses that occur in the chip before the detector. Optical losses are mostly due to the insertion loss at the input fiber-to-waveguide coupling

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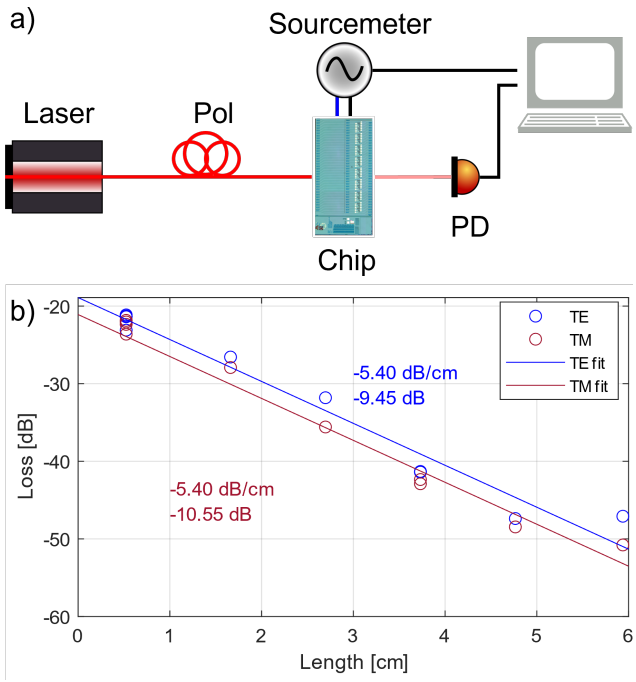

Fig. 5. (a) Experimental setup used to measure the responsivity of the diodes from waveguide excitation. The light of a laser diode (Thorlabs LP850-SF80) is injected into the chip via tapered lensed fibers. The light polarization is set by an in-fiber polarization control stage. The light travels through the waveguide and is coupled to the integrated photodetector. The photocurrent at -1 V bias is measured by a sourcemeter (Ketheley 2450), while any residual light in the waveguide is collected with another tapered fiber and sent to an external Si detector (PDA100A2). (b) Experimental characterization of the samples optical losses. The power transmission of waveguides of different lengths is measured and fitted via a Beer-Lambert law to estimate insertion and propagation losses for the chips.

interface and the propagation loss in the waveguide from the edge of the sample to the detector region.

Both insertion and propagation losses were estimated via cut-back method on a twin chip, realized on the same wafer next to the one hosting the photodetectors. On the testing chip, spiral waveguide structures with lengths from 0.5cm to 6cm were present, allowing for a loss estimation through Beer-Lambert law fitting of the transmission data. Figure 5(b) represents the propagation loss data samples for both transverse-electric (TE, blue) and transverse-magnetic (TM, red) input polarizations. While TE polarization exhibits slightly lower propagation loss, the devices are expected to show better operation in TM polarization, where the coupling towards the substrate is higher, and hence the generated photocurrent is larger. Once the propagation losses are estimated, the detector responsivity is measured with the setup shown in Fig. 5a. This time, variable optical power is injected into the optical waveguides coupled to the detectors. The optical power before the detector, P_{in}, is calculated by subtracting insertion and propagation losses inside the chip from the laser power, which is monitored with a calibrated power-meter (S120VC). For each level of input optical power an IV-curve is measured on the detector, as shown in Fig. 6(a). In Fig. 6(b) we plot the generated photocurrent I_{ph} at -1 V bias as a function of the input optical power P_{in}. From fitting the data with

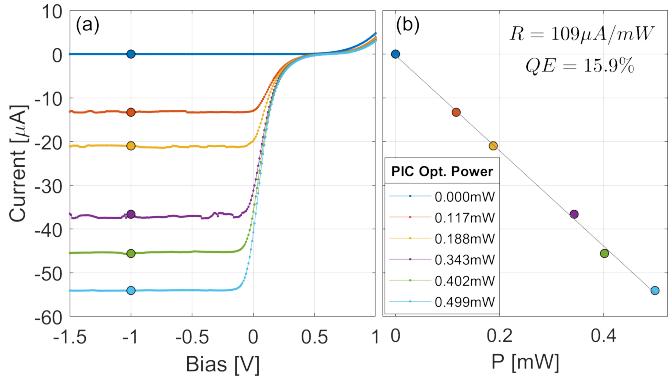

Fig. 6. (a) IV-curves with varying input optical power and (b) the responsivity of the photodiode coupled to a thinned waveguide.

a linear regression, the responsivity $R = I_{\text{ph}}/P_{\text{in}}$ of the detector can be estimated, which in our case is 0.109 A/W. The quantum efficiency of our devices has been estimated as $Q.E. = I_{\text{ph}}/P_{\text{in}} \times h\nu/e$ where h is the Plank constant, ν is the frequency of the photons and e is the elementary charge. From the measurements, the Q.E. of the device resulted as high as 15.9%, which is very close to the predicted 16.7% from FEM simulations. We have also characterized chips with complete inverse tapering (Fig. 2(d)). Here, the light diffuses into the SiO_2 cladding, which can be appreciated from the optical image shown in Fig. 3(d). The photodetector still absorbs the light trapped in the cladding, but at a slower rate. In this case, an efficient coupling in the active region is ensured by caging the light with deep trenches filled with metal which act as mirrors. Thanks to the lateral confinement provided by the metal cage, these devices achieve a Q.E. of 15.4%, similar to that of the thinned waveguides.

We note, that the measured responsivities are comparable with the state-of-the-art R's in waveguide-integrated photodetectors, which are typically of the order of 0.3 A/W [6], [7], [5]. Here, the lower values of R can be explained by the fact that the absorbance value of the realized devices is mostly limited by the thickness of the epitaxial layer, which is 3 μm in our devices. The epitaxial layer, determines the detector's active volume where the photo-generated electron-hole pairs are collected. Even though the light couples to the substrate from a waveguide parallel to the surface, Snell refraction bends the light to about $60°$ with respect to the SiN/Si interface, thus reducing the optical path within the active layer to approximately $3\mu\text{m}/sin(60°) \approx 3.5$ μm. In fact, in Ref. [5], which uses a 10 μm epitaxial Si, an $R \approx 0.3$ A/W has been demonstrated. Nevertheless, as in the case for the devices described in [5], this issue can be mitigated with the use of thicker epitaxial layers or with back-side reflector strategies.

V. Conclusions

The geometries we tested for substrate-coupling of the light at the end of a PIC show promising results to be used in integrated devices fabricated with optical lithography, especially where monitor photodiodes are required. Our coupling strategy provides a simple reliable coupling method which

is broadband, resolution-insensitive and robuts to fabrication toleracies. We believe that our method could provide an excellent alternative to grating couplers that, being essentially resonant structures, are bandwidth-limited and sensitive to fabrication tolerances. In particular, the vanishing-waveguide variation is efficient for short-wavelength applications where a thick oxide impedes the evanescent coupling and the definition of a grating coupler is particularly challenging. With respect to other approaches developed for waveguide-photodetector coupling, the technology described in this paper permits an independent development of arbitrary electronics within the epitaxial Si substrate, followed by an integration of arbitrary PIC architecture on top of the substrate. The future perspective is to use this technology to couple SiN photonic circuitries with single-photon avalanche diodes [21] in order to make a step forward towards the development of VIS-NIR operating quantum photonic platform in silicon.

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