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HIGH POWER, MEDIUM FREQUENCY, AND MEDIUM VOLTAGE
TRANSFORMER DESIGN AND IMPLEMENTATION

by

Ahmad El Shafei

A Dissertation Submitted in
Partial Fulfillment of the
Requirements for the Degree of

Doctor of Philosophy
in Electrical Engineering

at

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December 2022

ABSTRACT

HIGH POWER, MEDIUM FREQUENCY, AND MEDIUM VOLTAGE TRANSFORMER DESIGN AND IMPLEMENTATION

by

Ahmad El Shafei

The University of Wisconsin-Milwaukee, 2022

Under the Supervision of Professor Adel Nasiri

Many industrial applications that require high-power and high-voltage DC-DC conversion are emerging. Space-borne and off-shore wind farms, fleet fast electric vehicle charging stations, large data centers, and smart distribution systems are among the applications. Solid State Transformer (SST) is a promising concept for addressing these emerging applications. It replaces the traditional Low Frequency Transformer (LFT) while offering many advanced features such as VAR compensation, voltage regulation, fault isolation, and DC connectivity.

Many technical challenges related to high voltage stress, efficiency, reliability, protection, and insulation must be addressed before the technology is ready for commercial deployment. Among the major challenges in the construction of SSTs are the strategies for connecting to Medium Voltage (MV) level. This issue has primarily been addressed by synthesizing multi-cellular SST concepts based on modules rated for a fraction of the total MV side voltage and connecting these modules in series at the input side. Silicon Carbide (SiC) semiconductor development enables the fabrication of power semiconductor devices with high blocking voltage capabilities while achieving superior switching and conduction performances. When compared to modular lower voltage converters, these higher voltage semiconductors enable the construction of single-cell SSTs by avoiding the series connection of several modules, resulting in simple, reliable, lighter mass, more power dense, higher efficiency, and cost effective converter

structures.

This dissertation proposes a solution to this major issue. The proposed work focuses on the development of a dual active bridge with high power, medium voltage, and medium frequency control. This architecture addresses the shortcomings of existing modular systems by providing a more power dense, cost-effective, and efficient solution. For the first time, this topology is investigated on a 700kW system connected to a 13kVdc input to generate 7.2kVdc at the output. The use of 10kV SiC modules and gate drivers in an active neutral point clamped to two level dual active bridge converter is investigated. A special emphasis will be placed on a comprehensive transformer design that employs a multi-physics approach that addresses all magnetic, electrical, insulation, and thermal aspects. The transformer is designed and tested to ensure the system's viability.

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LIST OF TERMS AND ABBREVIATIONS

AFF Active Front End	34
BIL Basic Impulse Lightning	4
CHB Cascaded H-Bridge	56
CM Common Mode	91
CTI Comparative Tracking Index	101
DAB Dual Active Bridge	14
DBC Direct Bonded Copper	93
DESD Distributed Energy Storage Devices	45
DM Differential-Mode	158
DPS Dual Phase Shift	24
DPT Double Pulse Test	183
DRER Distributed Renewable Energy Resources	45
DVC Decisive Voltage Classification	101
DVR Dynamic Voltage Restorer	33
EEL Equivalent Elliptical Loop	121
EMC Electromagnetic Compatibility	157
EPRI Electric Power Research Institute	43
EPS Extended Phase Shift	22
FACTS Flexible AC Transmission System	36
FB Full Bridge	16
FC Flying Capacitor	56
FEM Finite Element Method	7
FREEDM Future Renewable Electric Energy Delivery and Management	1
FWC Flux Waveform Coefficient	126
GSE Generalized Steinmetz Equation	125

GTO Gate Turn-off Thyristor	89
HEV Hybrid Electrical Vehicle	vi, 14
HFL High Frequency Link	27
HV High Voltage	11
HVDC High Voltage Direct Current	55
IBDC Isolated Bi-directional DC-DC Converter	16
IGCT Integrated Gate-Commutated Thyristors	89
iGSE improved Generalized Steinmetz Equation	125
KBM Krylov Bogoliubov Mitropolsky	18
LFT Low Frequency Transformer	ii
LISN Line Impedance Stabilization Network	159
LV Low Voltage	11
MF Medium Frequency	3
MFT Medium Frequency Transformer	3
MM Mixed-Mode	158
MSE Modified Steinmetz Equation	124
MV Medium Voltage	ii
NPC Neutral Point Clamped	55
OSE Original Steinmetz Equation	123
OVC Over Voltage Category	100
PD Partial Discharge	4
PE Power Electronic	38
PI Proportional-Integral	32
PLD Pollution Degree	101
PR Proportional-Resonant	32
PWM Pulse Width Modulation	26
RMS Root Mean Square	21

S-DAB Semi-Dual Active Bridge	56
SiC Silicon Carbide	ii
SiC-JFET Silicon Carbide Junction Gate Field-Effect Transistor	56
SMC Sliding Mode Control	34
SMPS Switch Mode Power Supply	10
SOA Safe Operating Area	74
SPS Single Phase Shift	21
SRC Series Resonant Converter	48
SST Solid State Transformer	ii
STATCOM Static Synchronous Compensator	36
SVC Static Var Compensator	2
THD Total Harmonic Distortion	61
TPS Triple Phase Shift	25
UNIFLEX Universal and Flexible	50, 51
UPQC Unified Power Quality Conditioner	2
UPS Uninterruptible Power Supply	15
WBG Wide Band-gap	157
WCSE Waveform Coefficient Steinmetz Equation	125
ZCS Zero Current Switching	13
ZVS Zero Voltage Switching	13

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CHAPTER 1

Introduction

1.1 Trends and Motivations

Some define a smart grid as an "electric grid using digital technologies". "Smart grids" are a relatively broad concept with several definitions. A smart meter allows two-way communication between a utility and its customers (bi-directional smart metering), and a variable electricity rate based on demand during the day. In addition to the self-healing capabilities of power grids, another definition of a smart grid is the ability of power grids to recover from faults in transmission lines and substations by utilizing distributed sensors and automatic controllers. As a result of incorporating Future Renewable Electric Energy Delivery and Management (FREEDM) into the smart grid, the concept has broadened and includes the deeper penetration of distributed renewable electric power generation, as well as greater interaction between utility services and consumers [1] - [2].

Energy routers provide direct control of power flows, facilitating bi-directional power flow and the sale of electric energy back to the utility. Additionally, the energy router provides additional features to the distribution power system, including power factor correction, fault current limits, and ride-through capability for sags and swells. A distributed communication and control protocol enables utilities and consumers to communicate more effectively beyond two-way communication through smart meters. All of these characteristics will contribute to improved

power quality at the distribution level. It is the supervisor and controller of the distribution system, enabling management and ensuring optimal power generation and distribution. In the current state of technology, it is not possible to create a device that performs all the functions discussed above in an energy router. In addition, conventional passive transformers are unable to control power flow; switched capacitor banks and Static Var Compensator (SVC) are merely reactive power compensators. The concept of SST was introduced to fill the void that was left by the Unified Power Quality Conditioner (UPQC) of offering power factor correction and harmonic compensation. However, none of these devices have the functionality of a router. This is where the concept of SST is introduced. An SST is a high-speed switching frequency power electronic converter that has the following functionalities: provides galvanic isolation between the input and output, and provides active power control in both directions. It also provides ports or interfaces for connecting distributed power generators or energy storage devices and compensates for power grid disturbances, including variations in input voltage, and short-term sags or swells.

An SST serves as a buffer between the power grid, loads, distributed energy sources, and energy storage devices in the FREEDM system as a whole. As a result of decoupling the load from the source, consumers would not be affected by grid disturbances since the SSTs compensate for the disturbance. Moreover, since the SSTs compensate for reactive power generated by loads, the power grid would not observe it. This is one of the advantages of SSTs. One of the benefits of SSTs for the power grid is their ability to enhance the efficiency and stability of the distribution system. Besides serving as buffers for renewable energy sources, SSTs minimize the impact of unpredictable and unschedulable fluctuations on power grids and loads that result from renewable energy sources. SSTs offer this advantage for the generation of renewable energy [3].

As an interface between the inherently fluctuating power sources and the grid, power conversion systems based on Medium Frequency (MF) DC-DC converter isolated with Medium Frequency Transformer (MFT) shown in Fig.1.1 are becoming more and more significant. Compared with conventional LFTs, MF power conversion systems operating at the kilo-hertz range feature significant reduction of weight and size, dynamic control of power flow, and enhanced power quality. Such a compact system is also attractive for railway applications where space is limited [4].

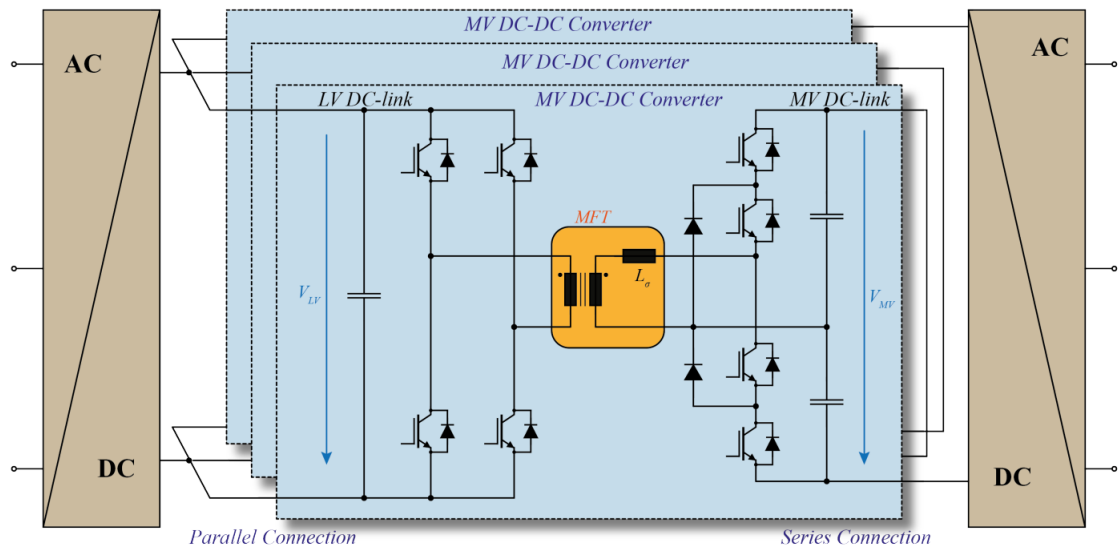


Fig. 1.1 Medium frequency power conversion system

With the proliferation of power electronic semiconductor switches for high-power SST applications, the notion of substituting the traditional LFT in MV distribution grids (e.g all-DC offshore wind farms) and onboard traction applications with the system consisting of much smaller and lighter MFTs driven by power electronic converters, namely the SST, has been gaining popularity [5]. One major application that is seeking MV SST deployment is data centers. Due to the increasing use of cloud computing and big data, the power consumption of data centers alone reached 10% of the total electrical power consumption in the world by the year 2020. Considering the booming data center industry, the high copper cost and conduction

loss associated with low voltage (480Vac) power distribution outside the server hall need to be addressed. Despite increased global research effort [6], SST is still at a level of advanced academic and industry prototypes.

The LFT has been one of the most widely used technologies in electrical engineering for many years, however high-power, high-voltage MFT has not yet reached a mature and standardized state. In terms of electromagnetic modeling, insulation coordination, electrical parameter control, thermal coordination, and overall design optimization, numerous areas need to be investigated. In the documented research on modeling and design optimization of the MFT [6] - [8], the design considerations tied to the proper insulation coordination are usually neglected and there is no information about any insulation testing (e.g. Partial Discharge (PD) and Basic Impulse Lightning (BIL)). Furthermore, besides the discussion, selection and application of the available analytical sub-system models (e.g. leakage inductance [9], core [10] - [12], and winding losses [13] - [22]), from the often quite old literature, there has not been many efforts directed into improving the accuracy and precision of these estimations [23].

Over the past decade, there has been a great deal of attention given to moving towards higher power densities in power conversion units, especially in applications that are highly restricted, such as remote offshore wind farms and traction systems [24] - [25]. Increasing the operational frequency is the most common solution to achieve higher power densities, since the weight and volume of the magnetic part, perhaps the bulkiest element in power electronic converters, are then decreased [8]. In low-power and high-frequency applications, this solution is well established, but in recent years, there has been considerable interest in utilizing high-frequency at higher power and voltage levels. In addition, power electronic interfaces are used in smart grids as well as traction converter systems, which require full control of the power flow and high power density [26] - [27]. Due to the increased isolation requirements and

thermal stress that result from reduced size, MFTs become more challenging to design [4]. As a result of electrical, magnetic, dielectric, and thermal performance limits encountered in the system, a high-power, high-voltage MFT presents multiple technical challenges. Moreover, the outcome of a generic multi-objective optimization depends on how well the models used are selected. Furthermore, various technological choices need to be carefully selected before being incorporated. Therefore, all relevant phenomena within the physical subsystems of this complex multi-physical system must be modeled as accurately as possible to understand their impact on the given application. For resonant converters, electric parameters must be controlled precisely since the transformer is part of a resonant circuit. In addition, there is still much discussion and citation about the issue of correct insulation and thermal coordination, as well as choosing the technologies involved in transformer design [23].

For high-power applications, the DC-DC converters are usually cascaded and connected to the MV grid. The design challenges are mainly high efficiency, thermal management, and high voltage insulation due to the reduced size and higher frequency. Previous research focusing on MFT design has been reported in [28] - [29] for traction applications and in [30] - [31] for renewable energy and smart grid applications. Although transformer design and optimization are widely discussed in numerous publications, the detailed design and optimization procedure for MFT can be found only in a few recent publications. In [32], a design methodology for MFT based on amorphous alloy is proposed, a simplified thermal model is used and the heat dissipation capability is considered for optimization. In [33], different core materials are considered and temperature calculation is included in the optimization process. However, as simplified thermal models for windings are employed in these studies, the heat transfer between different layers of windings is not included and the electric field distribution which is essential for insulation design is also not included in the optimization procedure [4].

Operating higher up in frequency is the most common solution to achieve higher power density. This is because the weight and volume of the magnetic part, the bulkiest element in power electronics converters, is decreased. However, on the other hand, it will lead to increased loss density due to enhanced core loss and more importantly enhanced winding loss [34] - [35]. One of the potential applications of the high-power MFT is high-power isolated DC-DC converters for wind energy DC collection and transmission grids. This could lead to a significant weight and size reduction, which is of a particular value for offshore wind installations as stated in [30], in which a 3MW, 500Hz transformer is shown to be more than three times lighter than the equivalent 50Hz one. Most of the classical attempts for high-power MFT designs were focused on a parameter called area product whereby the power handling capability of the core is determined [36]. Petkov in [37] presented a more detailed design and optimization procedure of high power high frequency transformers. Some years later, another work reported a similar approach accounting for non-sinusoidal excitations. However, parasitics are essentially ignored in both approaches [38].

It is important to consider the effects of high power, high voltage, and high frequency. This is because the technology in this area has not yet advanced to a mature level. These challenges essentially originate from the basic requirements of SSTs, i.e., simultaneous fulfillment of high power, high voltage, and high-frequency requirements [8].

1.2 Research Objectives and Contributions

Typical LFTs are used for electrical isolation between systems as well as to fulfill the voltage-matching requirement. However, the 50/60Hz transformers are bulky and large in size and weight [39]. Through the use of power electronic converters, the gap between the old power system and the proposed microgrid concept will be minimized. The SST idea was born for this application. It is defined as a high/medium frequency transformer implemented with a power converter. In contrast to traditional LFTs, this will have a direct impact on the size, compactness, and power density. Recent developments in advanced magnetic materials with low power loss and high saturation flux density as well as high power-high frequency switching devices have made it possible to design high-efficiency high power density SSTs [40] - [43].

SSTs represent a suitable candidate for DC-DC converters in DC grid applications, such as future offshore wind farms collection networks [39] - [44]. SSTs also allow better efficiency and a lower weight, which can be very useful for offshore applications. The gain in performance obtained by the use of SSTs is mainly due to the possibility of increasing semiconductor density, which allows using MFTs which are more compact and more efficient than the traditional 50-60Hz transformers [45]. However, high power high voltage applications combine electromagnetic, insulation, electrical, and cooling constraints on the MFT. Therefore, the MFT design must take into account all of these specifications, which represent a multi-objective optimization process [41], [46].

As a novelty, this work presents an integrated multi-physics design that covers all aspects of a medium voltage medium frequency high power SST, including power converter and transformer electromagnetics, insulation, EMI, and thermal analyses. The research will include numerical Finite Element Method (FEM) validation of the selected design utilizing novel hands-

on experience in terms of electromagnetic/power-electronic transient co-simulation, electrostatic, EMI, and thermal simulations. A special focus is also placed on the development of a 700kW, 13/7.2kV, 20kHz transformer. To the author's knowledge, this transformer is the highest-designed, prototyped, and tested transformer out there. Experimental validation of the transformer was performed after a prototype transformer was built.

1.3 Dissertation Organization

This dissertation will be presented in the following format:

The first chapter discusses the trends that led to this work and the motivation for it, as well as the challenges and opportunities involved in fully implementing a medium voltage medium frequency high power solid state transformer.

The second chapter provides an overview of DC-DC converters, with a focus on dual active bridge topology, as well as the difficulties and current state of the art in terms of power and voltage levels for its transformer design.

The third chapter delves deeper into the ANPC-2L topology chosen for this study, from which the voltages and currents are calculated. A thermal analysis is also presented, as well as the use of HV SiC power modules and the coordination of insulation between the various DAB power converter components.

The fourth chapter of this thesis discusses the electromagnetic, thermal, electromagnetic interference (EMI), and overall parameter optimization and compilation aspects of the transformer's multi-physics design.

The fifth chapter presents Ansys FEA electromagnetic, electrostatic, and thermal simulations, as well as PLECS/Simulink for EMI results. The transformer prototype's construction is discussed, and the experimental findings obtained thus far on the transformer are broken down and clarified.

Finally, the sixth chapter is where the conclusions drawn from the research work developed in this dissertation are gathered, as well as areas for further research are proposed.

CHAPTER 2

DC-DC Converters

2.1 Overview

The dependence and use of electronic devices in our daily lives has grown exponentially over the past few years. Since the majority of these devices are battery-operated, different levels of DC voltages are required to meet their unique requirements. The use of DC-DC converters allows for these different voltage levels [47] - [48]. DC-DC converters take DC voltage at the input and step it up or down at the output according to the given requirement. Small electronic devices requiring few volts to very high voltage levels (i.e., transmission lines) can all be powered by DC-DC converters. Regulated Switch Mode Power Supply (SMPS) and DC motor drive applications both widely use DC-DC converters. It uses very high-frequency switches, such as MOSFET, that is controlled by a microprocessor to regulate the duty cycle of the switches. In essence, the duty cycle determines the feature of stepping up or down the output DC voltage. It can control whether the converter steps up or down as well as how much the output of the converter steps up or down [49] - [51].

Distribution using DC level is becoming more and more enticing as renewable energy generation is integrated into power grids on a larger scale. For instance, because no reactive power is generated or consumed by the transmission cable, DC transmission is more efficient than AC transmission. This is similar to installing wind farms offshore. Additionally, a significant

reduction in weight/volume and consequently installation costs could be achieved by substituting the massive 50/60Hz transformers with higher-frequency transformers. This new concept has been evaluated in [52], where high power DC-DC converters in the MW range are required to interface different voltage levels within the wind farm. This novel idea has been evaluated in [52], where different voltage levels within the wind farm are interfaced with high power DC-DC converters in the MW range. On the other hand, the generation of energy using renewable resources is extremely susceptible to changes in the natural conditions [53]. For instance, photovoltaic panels can only produce energy during the day, so they must be combined with sizable storage systems to produce the necessary energy when there is insufficient sunlight. Here, a high-power bidirectional DC-DC converter that can dynamically control the power within the system and to the power grid is required to connect the photovoltaic generators with their respective storage systems. High-power DC-DC converters are, as can be seen, key technologies for this upcoming power generation scene [24]. A schematic representation of a high-power DC-DC converter interfacing two voltage levels, i.e. Low Voltage (LV) and High Voltage (HV), is shown in Fig. 2.1.

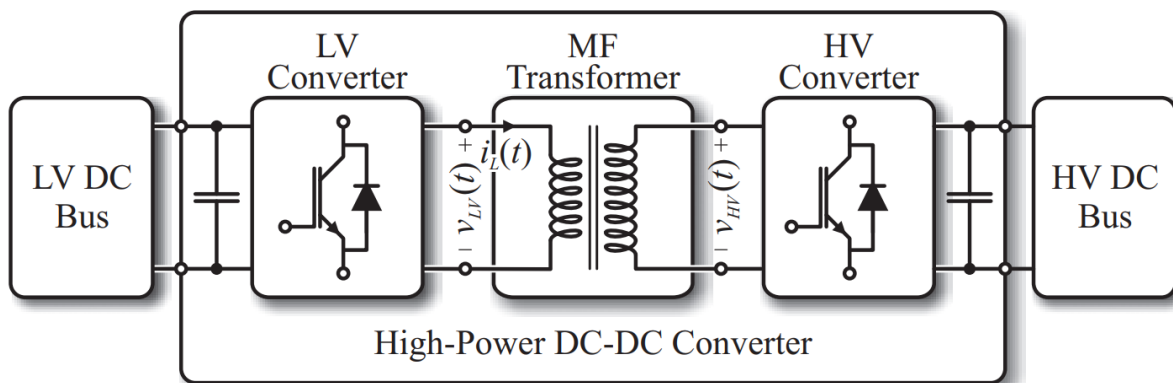


Fig. 2.1 DC-DC converter interfacing two DC grids with different voltage levels

Providing step-up/down in voltage levels and ensuring electrical isolation between LV and HV sides, which must adhere to international standards [54], are the main duties of the MFT,

which are essentially the same as with 50/60Hz transformers. In this MFT, the excitation frequency offered by the power electronic components is several times higher than in conventional 50/60Hz systems, resulting in a significant reduction in the transformer's overall size and weight. In Fig.2.2, a map of transformer designs from various research groups, along with their operating frequencies and achieved volumes is shown. Here, with higher operating frequencies, a significant volume reduction is noticeable where the break in the fitted line is given by a change in the utilized core material [33].

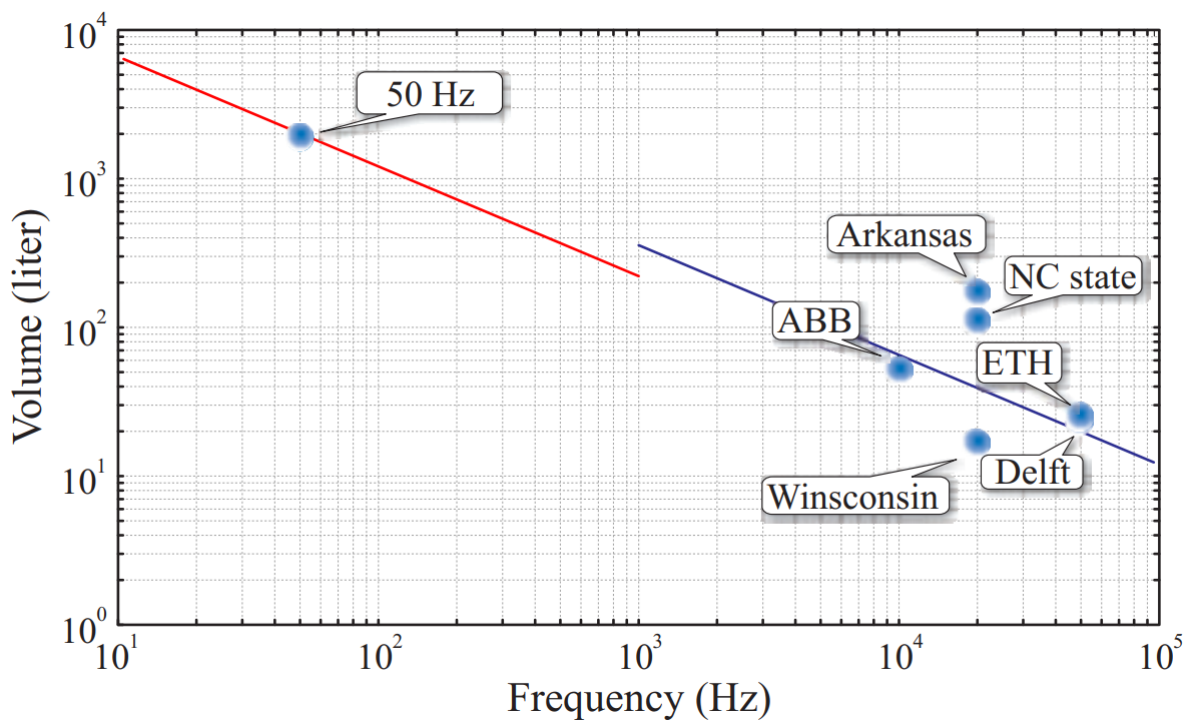


Fig. 2.2 Volume reached by different transformer designs with different operating frequencies (all scaled to 1 MW power rating)

The below subsections briefly discuss two properties of DC-DC converters namely: hard/soft switching and unidirectional/bidirectional power flow.

2.1.1 Hard switching/Soft switching

Switching based on the relationship between current and voltage is referred to as hard switching and soft switching. Hard switching is a simple method to accomplish this. It is the method

where the transistor is turned on or off by increasing the current or voltage to enable the state change. Switching loss, which is caused by the non-instantaneous transition time in transistors, is a major drawback of this method. It occurs when the voltage and current intersect. As a result, as switching frequency increases, switching loss also increases. However, high switching frequency is required to reduce the circuit size. In contrast, soft switching converters significantly reduces switching loss [55] - [57]. This is achieved due to the LC resonant circuit, which allows the device to turn on or off at zero current (Zero Current Switching (ZCS)) or voltage (Zero Voltage Switching (ZVS)). As a result, DC-DC converters can be operated at high switching frequency without experiencing significant switching loss [58] - [60].

2.1.2 Unidirectional/Bidirectional

The main purpose of fundamental DC-DC converters is to provide a unidirectional power supply to the load [47] - [61]. Due to the use of unidirectional components like a diode, the power flow is unidirectional. However, by implementing current bidirectional switches, such converters can be converted into bidirectional converters [62]. A schematic of a bidirectional DC-DC converter is shown in Fig. 2.3 [49].

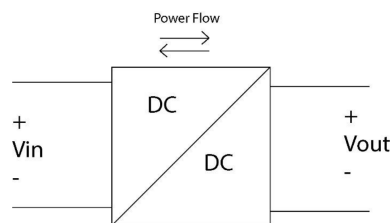


Fig. 2.3 Bidirectional DC-DC converter

2.2 Dual Active Bridge

One enticing type of DC-DC converters is Dual Active Bridge (DAB). The isolated bidirectional DAB DC-DC converters illustrated in Fig. 2.4 have many benefits over conventional DC-DC converter circuits, such as electrical isolation, high reliability, easiness in realizing soft-switching control, and bidirectional energy flow [63].

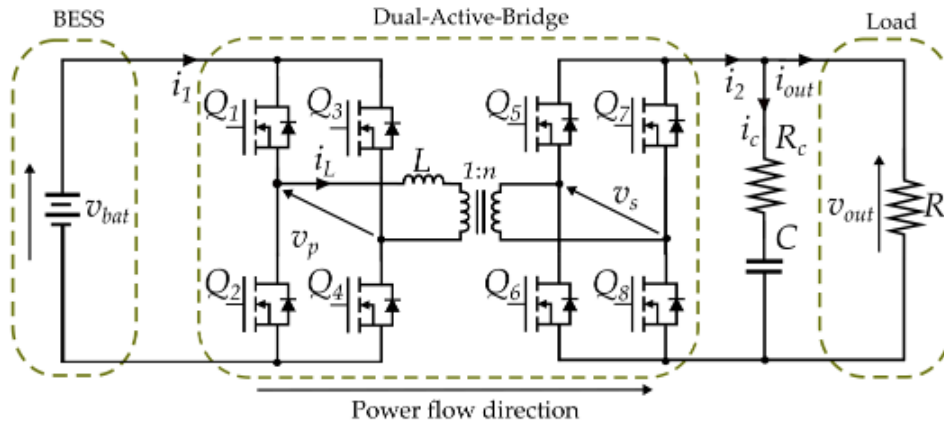


Fig. 2.4 Electrical systems in a series Hybrid Electrical Vehicle (HEV)

A DAB converter is a high-power, high-power-density, and high-efficiency power converter with galvanic isolation. One high-frequency transformer and two active power switching H-bridges make up the converter. The high-frequency transformer provides both galvanic isolation and energy storage in its winding leakage inductance. The phase shift between the two H-bridges regulates the amount and direction of power flow and the two H-bridges typically operate at a fixed 50% duty ratio. There are DC-DC DAB converters and AC-AC DAB converters based on the configuration of switching devices.

Bidirectional isolated DC-DC DAB converters were initially proposed as candidates for high power density and high-power DC-DC converters. ZVS, bi-directional power flow, and lower component stresses contribute to making the DAB topology desirable. Two H-bridges and one high frequency transformer constitute a DAB converter. The input voltage is converted

by one of the H-bridges into an intermediate high-frequency AC voltage, while the other H-bridge converts the high-frequency square wave AC voltage back to the output voltage. A high frequency transformer is used in conjunction with high-frequency switching devices because they reduce the weight and volume of passive magnetic devices. The primary and secondary windings of the high-frequency transformer have some leakage inductance in addition to galvanic isolation, which together function as an energy storage component. Additionally, the leakage inductance enables achieving soft switching. During switching transients, transformer current resonates with the capacitors in parallel with switching devices, limiting the dv/dt and di/dt across the switches. Soft switching contributes to higher power efficiency and the reduction of switching loss. DAB converters, in contrast to other isolated DC-DC converters using asymmetrical topologies, have symmetrical circuit configuration that enables the bi-directional power flow required for SSTs. Varying the phase shift between those two bridges, the power flow of a DAB converter can be controlled. The voltage across the transformer leakage inductance is altered by such phase shift. In this manner, both the amount of power transferred and direction of power flow are controlled. Power is transferred from the leading bridge to the lagging bridge [3].

2.2.1 Applications

The DAB DC-DC converter has been utilized in battery application systems, such as Uninterruptible Power Supply (UPS), auxiliary power supplies for electric or hybrid vehicles, battery management systems, microgrids, and energy storage systems. Research literature for instance examines multiple DAB applications such as offline UPS design based on the DAB topology, control of the bidirectional energy transfer between an energy storage system and a DC power system, and being a crucial element for automotive applications. DAB converters are also

recognized as the central component of the power electronic converter system that links a renewable energy source and an AC power system. Multiple input/output ports are now enabled by the expanded topology of DAB converters [3]. The application of DAB converters in high power renewable power generation is detailed in [64].

2.2.2 Principle of Operation

A high-frequency transformer is included in the conventional Full Bridge (FB) based Isolated Bi-directional DC-DC Converter (IBDC) (Fig. 2.5) and is primarily used to maintain galvanic isolation between the input and output terminals. For this converter, the input and output voltages are V_A and V_B , respectively. In addition, n is the transformer turns ratio, the phase shift between the two AC voltages ($V_{ac,A}$ and $V_{ac,B}$) is ϕ , and the sum of the primary-referred leakage inductance and an optional external inductor is represented by L_k .

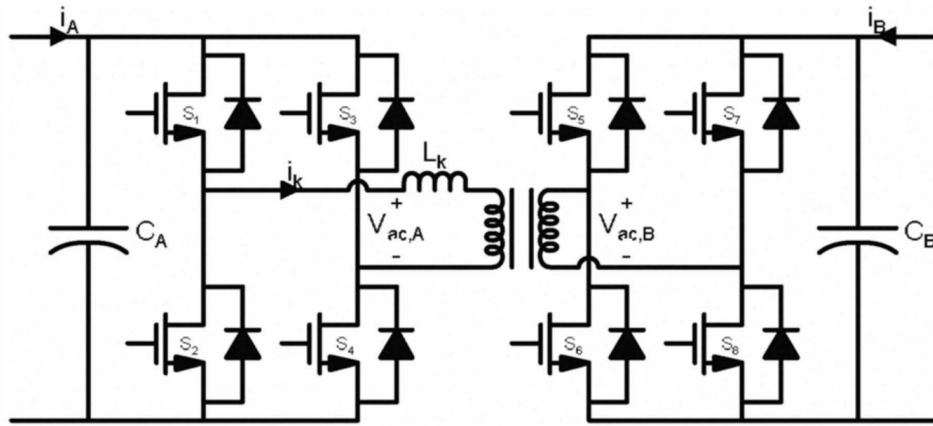


Fig. 2.5 Conventional full bridge based isolated bidirectional DC-DC converters

In Fig. 2.6, the main waveforms of this converter are displayed. Each bridge in this converter produces a square-wave voltage. To regulate the amount of power flowing through the inductor L_k , the two voltages ($V_{ac,A}$) and ($V_{ac,B}$) are phase-shifted with respect to one another

at an angle of ϕ . The average of transferred power can be expressed as:

$$P = \frac{V_A V_B}{n w w_k} \phi \left(1 - \frac{\phi}{\pi}\right) \quad (2.1)$$

Proper timing control of the converter switches enables leading or lagging phase shift (to transfer power from A to B or B to A, respectively). The DC voltage conversion ratio, defined as $d = \frac{V_B}{nV_A}$, determines the soft-switching range. The soft-switching may be lost if the input voltage varies widely. When $d > 1$, side-A can experience hard switching.

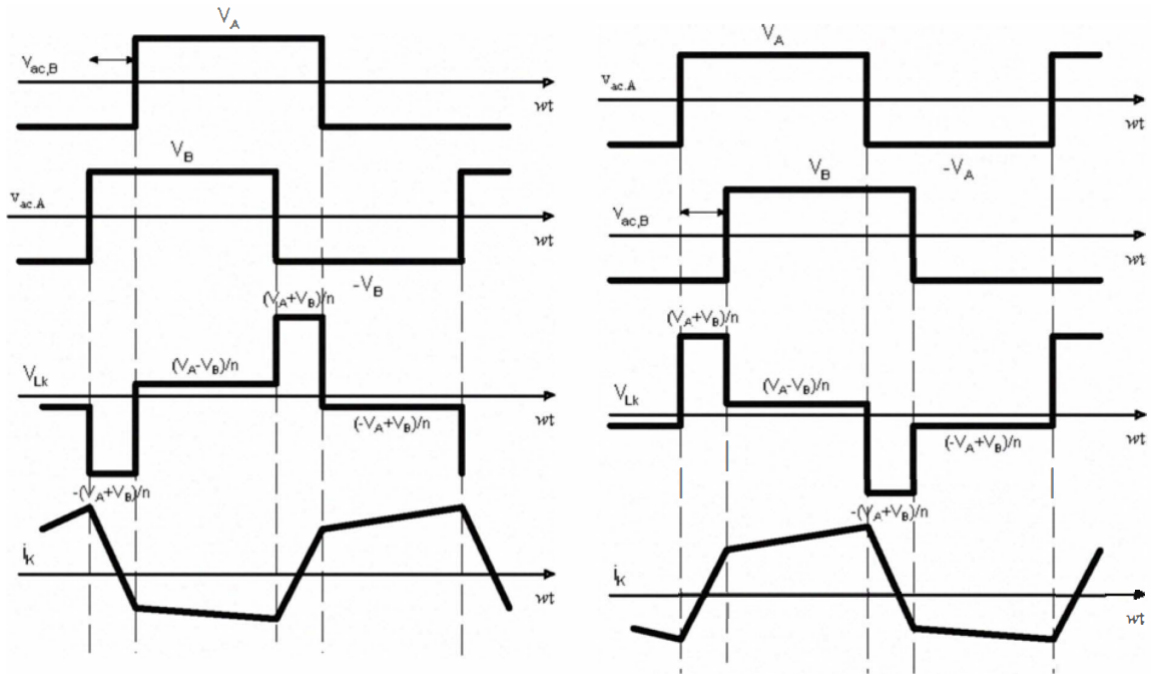


Fig. 2.6 Key waveforms of conventional FB BOC: (a) A-to-B mode, (b) B-to-A mode

Under idealized conditions, the soft-switching operation range is as:

$$|\phi| > \frac{\pi}{2} \left(1 - \frac{1}{d}\right) \quad (2.2)$$

For side-B, hard-switching can be occurred when $d < 1$ and the soft-switching operation range

is as:

$$|\phi| > \frac{\pi}{2}(1 - d) \quad (2.3)$$

Full control range under soft-switching is achievable for $d = 1$ [65].

2.2.3 Modeling of DAB

Good plant models are necessary for a good DAB controller design. Due to its switching nature, a high switching frequency power converter is essentially a nonlinear and time-varying system. However, a linear and time-invariant plant is more desired by the majority of control methodologies. In order to provide a linear and time-invariant approximation of the relevant power converter, various modeling techniques have been proposed to approximate the non-linearity and time-varying behaviors of a power converter. State-space averaging is one modeling method that is commonly applied. This traditional method makes the assumptions that the switching frequency is significantly higher than the frequencies of interest and that the state variables' ripples (such as inductor current and capacitor voltage) are sufficiently small. It eliminates all quadratic terms, produces a time-invariant model, and approximates the matrix exponentials in the solution of the power converter state equations using only linear and bilinear terms. A linear, time-invariant small-signal model is produced by further linearizing this model around a steady-state operating point. The DC terms in the Fourier series of state variables are essentially accounted for in state-space averaging. Generalized state space averaging is another averaging method that preserves more terms in the Fourier series of state variables (normally the switching frequency terms). The fact that generalized averaging does not assume that state variable ripples are small is one of its advantages. This method could produce more accurate models while discarding less data. The Krylov Bogoliubov Mitropolsky (KBM) averaging method is another averaging method along with generalized averaging. The KBM

method approximates converter state variables using piecewise-polynomial equations rather than applying Fourier series of state variables. This will include the effect of ripples brought on by switching. The KBM method is simpler than generalized averaging and does not require small ripples either. When modeling pure AC state variables, KBM method might not be as helpful as generalized averaging. All three of the aforementioned modeling methods operate in the continuous-time domain. On the other hand, sampled-data models are in the discrete-time domain. A sampled-data model makes use of the fact that power converter state variables have cycle-by-cycle repeatable trajectories in steady state. It is frequently derived by integrating the switched piecewise linear differential equations of the state variables over a single control cycle. Given a set of initial conditions, the integration entails multiplying and integrating exponentials in order to solve the state equations. The Taylor series expansion is a common method for simulating this process. Like other power converter controller designs, the DAB converter controller design also needs an average model of DAB converters.

There are two different ways to model a DAB converter: (1) a simplified reduced-order model that ignores the dynamic of the transformer current, and (2) a full-order discrete time model that maintains the dynamic of the transformer current. One method to model those converters with high variation and resonant operations is discrete-time modeling. However, because it offers more physical insight and makes control design easier, a continuous-time model is typically preferred. Negligible current ripple is required by the standard state-space averaging method for DC-DC converters. The transformer current of a DAB converter is entirely AC, so this condition is not met by DAB converters. Instead, the effect of pure AC current on converter dynamics can be captured using the generalized averaging method, which employs more terms in the Fourier series of state variables. By choosing the appropriate converter parameters, it is generally recommended to separate the dynamics of current and voltage in a

DC-DC converter design. The previously mentioned simplified reduced order model assumes that the output capacitor voltage dynamics are significantly slower than those of the transformer current. This presumption hasn't been analytically verified, though. The conditions for the separation of the dynamics are provided by singular perturbation theory, along with an analytical method for doing so. In the literature, [3] reports the time-scale separation criteria for state variables in DC-DC boost converters.

2.2.4 Switching and Modulation Techniques

Researchers work to advance DAB modulation techniques. For DAB converters, dual phase-shift modulation has been suggested to reduce reactive power and loss. Hybrid modulation methods have been developed to increase soft-switching range. To increase the degree of control freedom, phase shift modulation and duty-ratio control have been applied to DAB converters. In the literature, various modulation techniques are analyzed and compared. To decrease switching loss and boost DAB converter efficiency, new switching strategies are presented. In order to address some of the parasitic and nonlinear effects of DAB converters, more detailed circuit models are created and analyzed. Several circuit design optimizations are published, and some published works concentrate on efficiency evaluation of DAB converters [3] in which one of the key areas of research for DAB-IBDC is control strategy.

In the following section, control methods which are the most widely researched methods for DAB-IBDC will be introduced and analyzed. To achieve improved topologies and variant, the control techniques may differ; however, all of these methods can be derived from the following ones [66]:

2.2.4.1 Single Phase Shift Control

The most widely used control method for DAB-IBDC is Single Phase Shift (SPS) control which is shown in Fig. 2.7. $S_1 - S_4$ and $Q_1 - Q_4$ are square-wave gate signals with 50% duty ratio for the corresponding switches in Fig. 2.8. v_{h1} and v_{h2} are the equivalent AC output voltages of full-bridges H_1 and H_2 , respectively, and i_L is the current of inductor L . Cross-connected switch pairs in both full bridges are switched in-turn during SPS control to produce phase-shifted square waves with a 50% duty ratio for the primary and secondary sides of the transformer. It is only possible to control the phase-shift ratio (or angle) D . The voltage across the leakage inductor of the transformer can be altered by adjusting the phase-shift ratio between v_{h1} and v_{h2} . Thus, the power flow's magnitude and direction can then be easily controlled. SPS control is becoming more popular as a result of its benefits, including its low inertia, high dynamic, and ease of realizing soft-switching control. However, in this method, the control of the power flow is dependent on the transformer's leakage inductor, which causes significant circulating power when the voltage amplitude of the transformer's two sides is not matched. As a result, both the peak current and Root Mean Square (RMS) increase. Additionally, in this scenario, the converter is unable to operate under ZVS in the whole power range. As a result, the efficiency is considerably reduced, and the power loss increased [66].

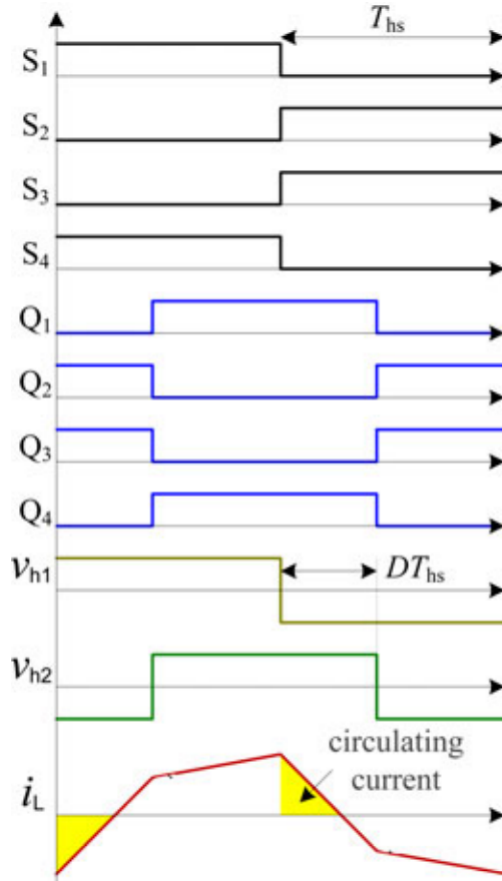


Fig. 2.7 SPS control

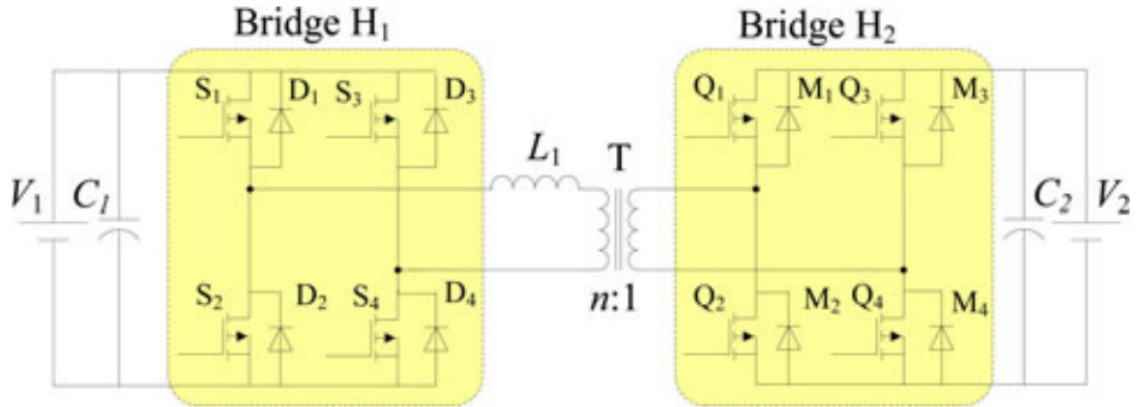


Fig. 2.8 Topology of DAB-IBDC

2.2.4.2 Extended Phase Shift Control

An improved method of SPS control is Extended Phase Shift (EPS) control, as shown in Fig.

2.9. Switch pairs in one bridge that are cross-connected are switched in-turn during EPS con-

trol, whereas switch pairs in the other bridge are switched with an inner phase-shift ratio. After that, one bridge's output AC voltage changes to a three-level wave, while the other produces a two-level 50% square wave. Since the backflow power is zero when the three-level wave's zero voltage occurs, the circulating power drops for a given transmission power. In the literature, it is discussed how the EPS control works and how well transmission power, current stress, power loss, and soft switching perform. In comparison to SPS control, EPS control increases regulating flexibility and efficiency while also reducing current stress and expanding the ZVS operation range. In contrast to the single phase shift ratio D in the SPS control, the EPS control has two phase shift ratios: an inner phase shift ratio D_2 and an outer phase shift ratio D_1 . The inner phase-shift ratio is used to reduce circulating power and increase ZVS range, whereas the outer phase-shift ratio is used to control the power flow direction and magnitude.

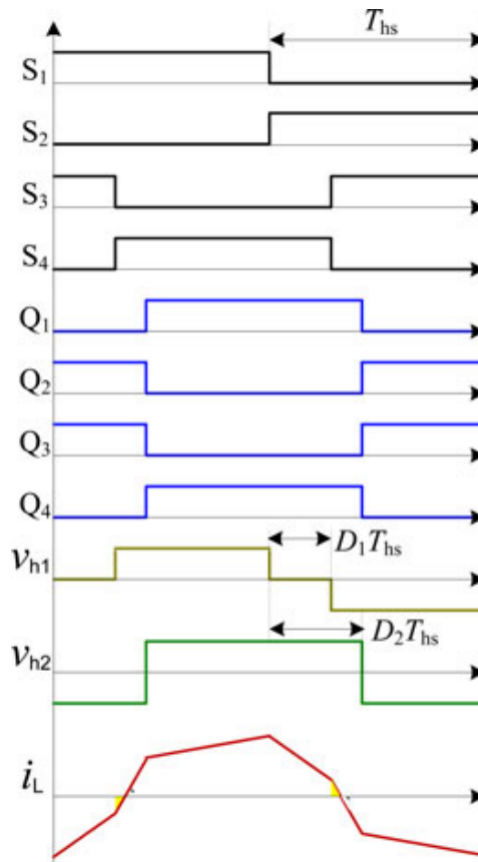


Fig. 2.9 EPS control

However, in order to achieve the decreased circulating power for the EPS control [66], the operating states of the two bridges must be switched. The switching occurs when the voltage conversion states are switched between the boost and buck states and the power flow directions are switched between the forward and reverse power flow.

2.2.4.3 Dual Phase Shift Control

Similar to the EPS control, the Dual Phase Shift (DPS) control was proposed as shown in Fig. 2.10. In contrast to EPS control, the cross-connected switch pairs in both full bridges in DPS control are switched using an inner phase-shift ratio, and the inner phase-shift ratios are identical. After that, both bridges' output AC voltages are three-level waves. Other research works included extensive information about the operation principle, transmission power, current stress, power loss, soft switching, and optimization design methods for the DPS control. When compared to SPS control, DPS control can reduce output capacitance and steady-state current, increase efficiency, and extend the ZVS operation range. Dead-band compensation can be easily implemented in the DPS control even if there is no current sensor, depending on the operating circumstances. When the states of voltage conversion or the direction of power flow are altered, the operating states of the two bridges will remain the same in comparison to the EPS control. Hence, DPS control is simpler to implement and may have better dynamic performance [66].

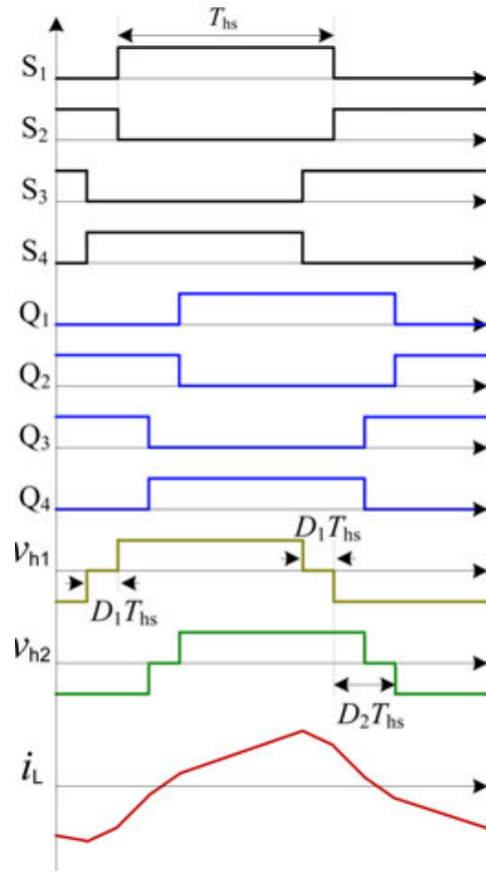


Fig. 2.10 DPS control

2.2.4.4 Triple Phase Shift Control

Researchers proposed the Triple Phase Shift (TPS) control, as shown in Fig. 2.11. Similar to the DPS control, The cross-connected switch pairs in both full bridges are switched with an inner phase-shift ratio. The inner phase-shift ratios, however, might not be equal. TPS control can also control three degrees of freedom. As a result, research on TPS control mainly focuses on the optimization operation field. Small signal model for digital control of DAB-IBDC with TPS control was studied in research literature. For DAB-IBDC with TPS control, an optimal modulation scheme that enables minimum copper losses and conduction was presented. Based on this, a design method and efficiency-optimized modulation scheme were created for an existing DAB-IBDC prototype. To increase the power range for ultra-capacitor application,

a hybrid modulation scheme and a feedback-linearized control were developed. In another research, an ideal modulation strategy for TPS control's reverse-mode operation was analyzed. Additionally, a stability analysis technique to improve the systematic and accuracy of DAB-IBDC with TPS control stability determination was discussed. Additionally, a composite TPS control scheme that extends the soft-switching range down to zero-load conditions, lowers RMS and peak currents, and significantly reduces transformer size was explored. This control method used an extensive analysis and experimental verification with Pulse Width Modulation (PWM) control.

In fact, the TPS control—a unified type of phase-shift control—was proposed after SPS, EPS, and DPS controls. SPS, EPS, and DPS control can also be regarded as special cases of TPS control. SPS control only requires one control degree to be implemented, EPS and DPS controls require two control degrees, and TPS control needs three control degrees. TPS control is therefore the most challenging to implement, and there is currently no common implementation standard. When the voltage conversion states or power flow directions change, the operating states of the two bridges for EPS control should also be altered. Additionally, there are problems with the SPS control's effectiveness, ZVS range, etc. Thus, considering both performance and implementation difficulty, DPS control may be a relatively optimal method for the large-scale practical application [66].

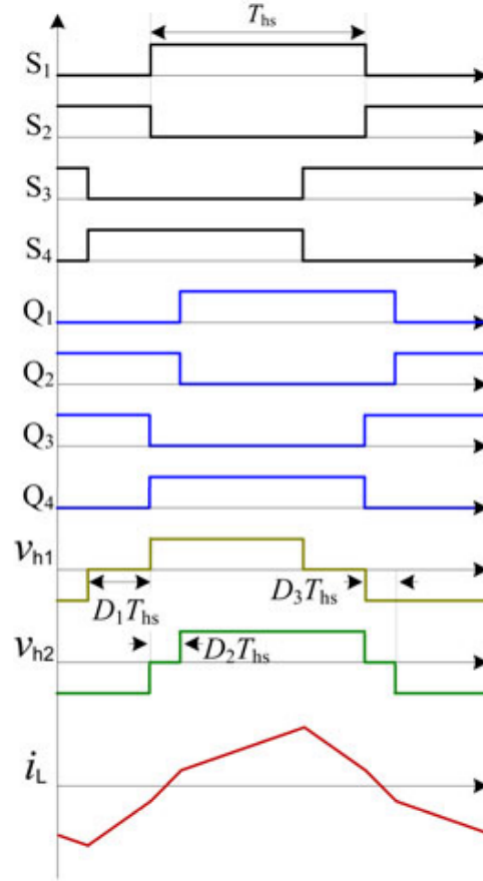


Fig. 2.11 TPS control

2.2.5 Soft-Switching Operation

DAB-IBDCs transcend other topologies through the easiness of realizing soft switching, their ability to transfer power in both directions, and their modular and symmetric structure. However, when the voltage amplitude of the transformer's two sides doesn't match, the circulating current increases significantly and the efficiency decreases rapidly. Additionally, the soft-switching range decreases under light load. To solve these problems, soft-switching technology is researched to improve the performance, as of now, the main research ideas center on the expansion of the DAB-soft IBDC's switching range through the improvement of the High Frequency Link (HFL) resonant tank. This section gives three typical solutions to discuss the soft-switching solution of DAB IBDC.

LC-type resonant topology based on DAB IBDC is shown in Fig. 2.12. Due to its operational advantages over conventional DAB IBDC, the converter can be operated at higher frequency and with greater efficiency; however, the addition of resonant components increases the converter's size and cost. Phase-shift control with fixed frequency (all switches in both full bridges are driven with 50% duty cycle) serves as the converter's control method, and two AC equivalent (with fundamental component) circuit analysis approaches are used for design purposes. The LC-type resonant DAB IBDC has common features with the conventional series resonant unidirectional full-bridge DC-DC converter and still has some unique features due to the secondary-side bridge, such as the capability of bidirectional power flow. ZVS for primary-side switches and ZCS for secondary-side switches could be accomplished from soft-switching performance.

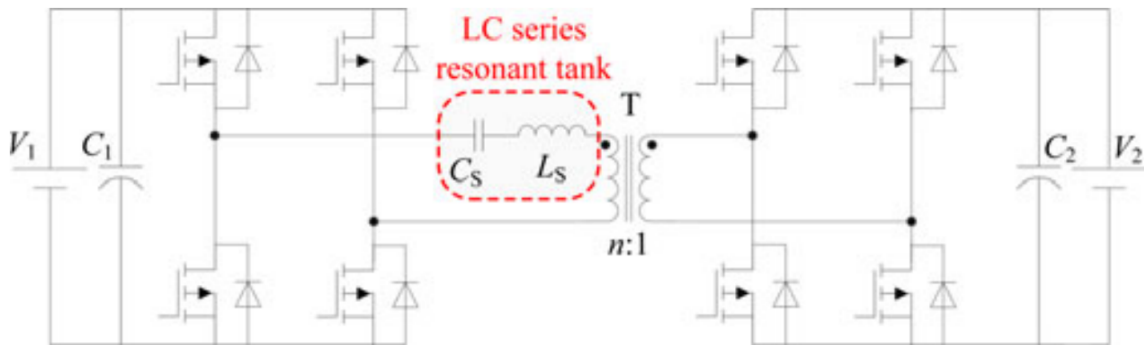


Fig. 2.12 LC-type resonant DAB-IBDC

Fig. 2.13 shows a CLLC-type asymmetric resonant topology based on DAB IBDC. Both the power flow directions are modulated under variable frequency modulation above resonance. The inverter switches are driven with a 50% duty cycle, and the rectifier switches are driven by the additional resonant signals. Similar to the LC-type converter mentioned above, ZVS for inverter switches and ZCS for rectifier switches could be achieved for a wide variation of voltage gain [66].

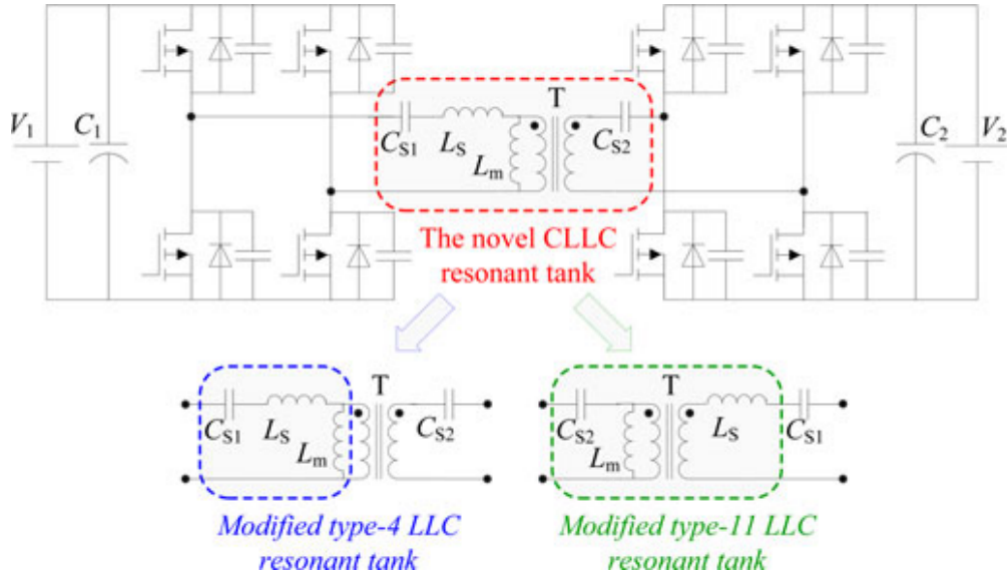


Fig. 2.13 CLLC-type asymmetric resonant DAB-IBDC

On this basis, the symmetric resonant DAB IBDC was also analyzed in several literature. Fig. 2.14 displays a DAB IBDC that employs a new symmetric CLLC-type resonant network. The position of the switches' operating stages determines the direction of power flow. The power switches produce AC power for the transformer in the inverting stage and are driven with a 50% duty cycle. All switches are turned off during the rectifying stage, and the anti-parallel diodes of the switches rectifies the transferred power. The transmission power and the output voltage are both modulated under variable frequency modulation, similar to the CLLC-type asymmetric converter mentioned above. Because the symmetric CLLC resonant network has soft commutation capability for rectifier switches and ZVS capability for inverter switches, this converter can operate under high power conversion efficiency. Additionally, the efficiency and operation of power conversion are identical to those of other power flow directions.

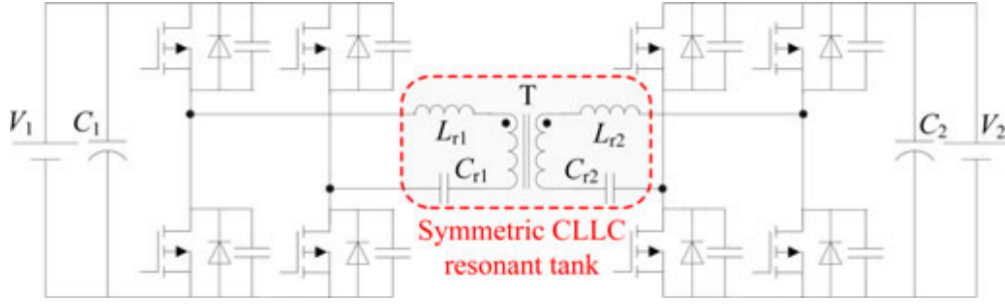


Fig. 2.14 CLLC-type symmetric resonant DAB-IBDC

Table 2.1 provides comparison between different soft-switching solutions. From Table 2.1, with different topologies, the control strategies are different, which also cause different soft-switching performance.

Table 2.1 Comparison of Different Soft-Switching Solutions

Converter	Resonant network structure	Power control	Drive	Soft-switching characterization	Soft-switching range	Additional component	Bidirectional transition speed
Traditional-type	No	Phase-shift modulation	50% duty cycle for all switches	ZVS for few switches	Narrow	No	Fast
LC-type resonant	Series resonant tank	Phase-shift modulation	50% duty cycle for all switches	ZVS for primary switches, ZCS for secondary switches	Narrow	A capacitor	Fast
CLLC-type asymmetric resonant	Series-parallel resonant tank	Frequency modulation	50% duty cycle for inverter switches, additional resonant signals for rectifier switches	ZVS for inverter switches, ZCS for rectifier switches	Wide	Two capacitors and a inductor	Slow
CLLC-type symmetric resonant	Series resonant tank	Frequency modulation	50% duty cycle for inverter switches, turn off for rectifier switches	ZVS for inverter switches, soft commutation for rectifier switches	Wide	Two capacitors and a inductor	Slow

Compared to the traditional and LC-type resonant DAB IBDCs, the CLLC-type resonant converters utilize frequency modulation which increases the control difficulty and the CLLC network requires more resonant components, which increases size and cost. Moreover, knowing the transition speed of bidirectional power flow, the direction of CLLC-type converters can be determined by the position of the switches' operating stage. However, the traditional

and LC-type DAB IBDCs are easily controlled by phase-shift angle through phase-shift control, thus the bidirectional transition speed of phase-shift control is faster. From soft-switching range, the CLLC-type resonant converters, on the other hand, have a wider soft-switching range than conventional and LC-type DAB IBDCs, making them more appropriate for applications with a wide voltage and power range. In addition, the CLLC-type asymmetric resonant converter displays various operations between forward and backward power flow directions in comparison to symmetric resonant converter because the turn numbers of the transformer and the structure of the resonant networks are asymmetric.

Besides the representative solutions with voltage-voltage fed converters, some studies also discussed the soft-switching solution based on current-fed DAB IBDC. Fig. 2.15 gives a typical topology as an example.

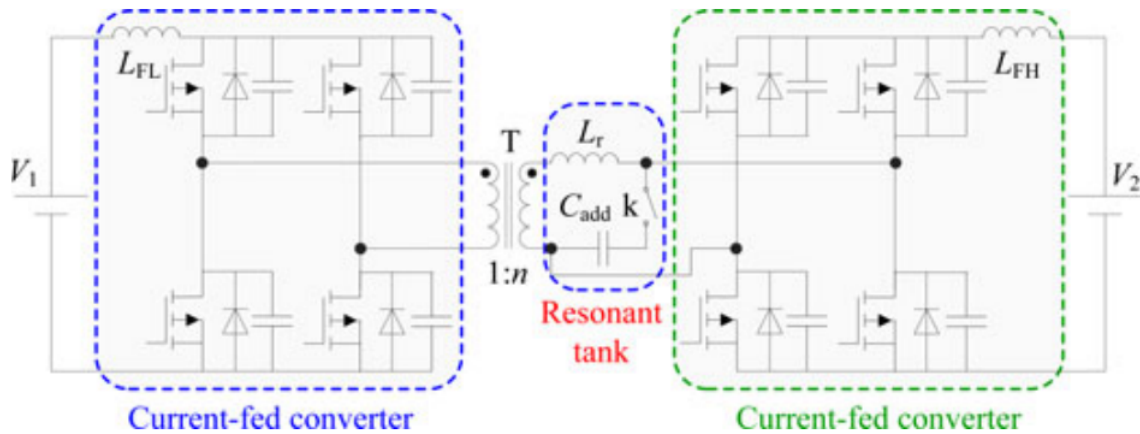


Fig. 2.15 Current-current-fed resonant DAB-IBDC

In the literature, a current-current fed resonant DAB-IBDC with two class-E resonant converters is proposed. When the key k is closed during the power transfer from the LV side to the HV side, an extra capacitor C_{add} is introduced. The LV converter transistors are controlled, and the converter operates as a class-E boost converter, whereas the HV converter transistors are not controlled, and the converter operates as a class-E rectifier composed of transistor body

diodes. The HV converter transistors operate as a class-E rectifier made up of transistor body diodes, whereas the LV converter transistors are not controlled and the converter functions as a class-E boost converter. Changes in control pulse frequency are used to control the bidirectional power flow. The relationship between the control pulses of the switch pairs, which are positioned diagonally in the bridge, determines whether the device operates in boost or buck mode. The converter's high operating frequency and zero switching loss value are its primary advantages. However, the experimental efficiency is not satisfactory, the converter control is complex, and further studies for the performance of the converter are required [66].

2.2.6 DAB Controller

When the output voltage of a power converter needs to be regulated and source/load disturbances need to be compensated, a closed-loop controller is necessary. With closed-loop control, the error between the output's reference and actual value is used to either eliminate or reduce the error. The typical approach for designing a controller for a power converter is to first derive a small-signal model around a steady-state operating point, then identify the converter's control-to-output transfer function, specify the expected loop gain based on design requirements, and finally design the controller transfer function to correspond to the desired loop gain. For power converters that demand zero steady-state error when the reference is a DC signal, a Proportional-Integral (PI) controller is commonly applied. The phase-margin of the loop gain is increased by a lead compensator, another type of power converter controller. Because neither the PI controller nor the lead compensator can achieve infinite gain at dc, it is challenging to achieve zero steady-state error when the reference or disturbance is a low-frequency AC signal.

It is suggested to use a Proportional-Resonant (PR) controller to achieve infinite gain at a given frequency. PI controllers in a D-Q rotational frame are equivalent to PR controllers in a

stationary frame. Due to the 120Hz power fluctuation in single phase systems (second-order harmonic), a PR controller is appropriate for single phase AC applications. In order to achieve zero steady-state error and to compensate for voltage harmonics and/or unbalanced contents caused by nonlinear loads without the need for time-consuming coordinate transformations, three-phase inverters also use a PR controller. PR controllers have been applied to single-phase active rectifiers, grid-tie inverters, UPS, distributed power generation, and Dynamic Voltage Restorer (DVR). In one work, a thorough analysis of single-phase DC-AC inverter PR controllers is presented. Another discusses the sensitivity of single-phase inverters controlled by PR. In the literature, it is discussed how to implement PR controllers as digital filters and how to match the impedance of a PR-controlled inverter. The controllers previously mentioned were primarily created for a single operating point. In order to guarantee stable dynamic response when the operating point deviates, large phase margin and gain margin are required. However, when there is a significant disturbance that causes a significant operating point deviation, the dynamic performance is not guaranteed. Gain-scheduling control is one method of enhancement. The aforementioned techniques are used to choose a set of controllers for various operating points. A supervisory controller improves performance over a broad operating range by switching between parameters in response to feedback data.

Adaptive control is a wider variant of gain-scheduling control. An adaptive controller dynamically modifies its control parameters. In gain scheduling control, on-line parameter adjustment provides better performance than the off-line adjustment. When the system's structure is known but its parameters are uncertain or variable, adaptive control is appropriate. An adaptive PI controller, for example, achieves better output voltage regulation by treating load resistance as an unknown parameter. Adaptive control has also been implemented in active rectifiers, inverters, and fuel cell power generation systems. There are other nonlinear methods that use

large signal models for controller design in addition to the control design methods based on (typically linear) small-signal average models.

Lyapunov-based back-stepping design is one approach. The large signal converter average model is used to define a Lyapunov function, which is a positive-definite energy-like function. Control design is accomplished when the control input can make the time derivative of the Lyapunov function negative-definite. The Lyapunov-based control technique has been applied to voltage-source inverters, Active Front End (AFE) rectifiers, and DC-DC converters. Sliding Mode Control (SMC) is another nonlinear control technique. SMC is a method of variable structure control, it defines a set of control structures. The state variables are controlled to slide along a predetermined expected trajectory by alternating between the control structures. SMC is an effective power electronic converter controller due to its switching nature. SMC has been utilized to control doubly-fed inductor generators, AC-AC converters, and DC-DC converters. Nonlinear-based designs have the benefit of allowing for the study and analytical validation of global stability and performance. Another advantage of such control methods is the ability to compensate for the non-minimum phase effect of boost-type converters.

Power converter controllers can also use computational intelligence paradigms. Fuzzy logic is an example of computational intelligence paradigm. Fuzzy logic control has several benefits, including simplicity of use and resistance to disturbances. Active front-end rectifiers, grid-tied solar inverters, and adaptive energy management for electric vehicles have all used fuzzy logic. When two converters are cascaded connected, stability problems might arise. When the load converter is tightly controlled by a fast control loop, it appears to be a negative impedance. It would be difficult to create a stabilizing controller with such negative impedance. For DC-DC converters, this issue has received extensive research. The rule-of-thumb is that the driving converter's output impedance should be less than the loading converter's input impedance.

According to some state space model-based studies, adding active damping or filtering can be used to solve the problem of destabilizing negative impedance.

In summary, there are a number of literature on the control of DAB converters. The most recent technology employs PI controllers with some simplified assumptions regarding converter models. A DC-DC DAB converter and a DC-AC inverter are cascaded, just as in multi-stage SSTs. To reduce the voltage ripple caused by a second order harmonic, a sizable DC-link capacitor is utilized. Instabilities may occur when bus voltage and output power are not balanced when several DC-DC DAB converters are connected in input-series-output-parallel configuration. As a result, other works introduce voltage and balance control techniques to address these issues [3].

2.3 DAB - High Frequency Transformer

Conventional LFTs are ubiquitously used in today's distribution grids to provide galvanic isolation and voltage scaling at the interfaces between various voltage levels. LFTs are typically big, heavy devices due to their low operating frequency of 50Hz or 60Hz. Their low complexity and passive nature have both advantages (high reliability) and disadvantages (no control options). The latter is becoming more significant considering recent developments such as the propagation of distributed generation systems at lower voltage levels and the smart grid paradigm generally, which implies a high degree of controllability of loads and power flows. However, controllability is a built-in characteristic of power electronic converter systems, which have found use in grid-related systems like, for instance, Flexible AC Transmission System (FACTS) and Static Synchronous Compensator (STATCOM). While these technologies can enhance the functionality of passive LFTs, they do not replace them. The logical next step is to completely replace LFTs with SSTs, which provide galvanic isolation via MFTs and use power electronic converters to interface the grids on either side.

Although the first "electronic" transformer was already patented in the early 1970s, it took nearly three decades for the idea to be taken seriously for grid level ratings at the start of the twenty-first century. Additionally, SSTs are suggested for traction systems, where the MF potential separation can lead to a decrease in size and weight as well as an increase in efficiency. This is especially advantageous for distributed traction systems [45].

The miniaturization of power supplies is the current trend. Generally, magnetic components get smaller in size as switching frequency increases. However, to achieve a high efficiency and a low temperature rise, magnetic components must be increased after a certain frequency because core loss and copper loss increase with frequency [67]. SMPS is another example of high

frequency transformers. It instantly and effectively transmits power from an external electrical source to an external load. In doing so, the transformer provides valuable extra capabilities as well:

- The primary to secondary turns ratio can be established to effectively accommodate input/output voltage levels that range widely.
- Multiple secondaries with various numbers of turn can be used to produce a multiple outputs at various voltage levels.
- Independent primary and secondary windings make it possible to isolate high voltage input and output, which is crucial for safety in off-line applications.

A switching converter's building blocks are capacitors and magnetic components. To eliminate the harmonics and thus increasing the converter's efficiency, a filter circuit (low pass filter) is provided. The presence of magnetic components makes the converter bulky at low frequencies, but it also makes analysis simpler. However, due to eddy current losses and the converter's pulsating, harmonic-rich waveforms, the converter is scaled down at high-frequency, which adds to the analysis's complexity. Forward PWM power converter is a buck-derived isolated converter and can be used in low to medium power applications [68]. SSTs have many benefits over conventional transformers, including high power density, power flow control, fault current limits, maintaining the power factor, providing voltage regulation and communication facilities. The development of SSTs is necessary to handle the constantly shifting demands of the smart grid [69].

2.3.1 Overview

The main component of the electrical power transmission and distribution systems are line frequency (50/60Hz) transformers. Nevertheless, they are bulky, huge, and expensive. Further-

more, due to magnetic saturation, they can produce more harmonics under heavy loads. The SST topologies have recently been studied as an alternative to LFT because of their superior advantages. Smart control features, such as voltage regulation, reactive power compensation, and bi-directional power flow control, are possible with SST topologies but are not feasible with conventional transformers [70].

One of the most exigent parts in FREEDM is SST which is a high frequency power electronic device. According to the Massachusetts Institute of Technology review from 2010, the SST is one of the most popular research topics right now. Utilizing SST gives the power system greater tenacity. It improves the back-and-forth flow of power, controls real and reactive power in the line, and addresses power quality problems like voltage sag or swell. Furthermore, it provides a DC link for renewable energy sources like solar to connect to, which is a notable and distinguishing characteristic. For SST, there are some dense structures developed to replace the typical large transformer [71].

Given the advancements in the Power Electronic (PE) converter and magnetics, which have led to higher power densities, compact sizes, etc., transformer design at medium/high switching frequencies has received a lot of attention. A medium/high-frequency transformer is used in a variety of applications, including traction and the integration of renewable energy sources (such as wind farms and SST topologies), serving the dual purpose of galvanic isolation between input and output stage as well as power conversion unit. When operating on higher switching frequencies, the volume of magnetics is lesser, however, the loss density is higher. This is because higher switching frequencies cause eddy current effects, which result in increased core loss and more prominent winding loss. An assembly for a high-power transformer consists of many different components, such as insulation, conductors, and cores, which altogether exhibit a heterogeneous thermal behavior. Surface area, material properties, and coolant all have an im-

pact on the different processes that are used for heat transfer in various parts of the transformer assembly. As a result, estimating thermal behavior is necessary for an accurate characterization of the transformer's design. Based on conductor geometry and subsequent equivalent thermal network of the transformer, the thermal resistances are driven using analytical model. Temperature gradient is calculated under unidirectional steady-state heat conduction and finally expressed through a bounded closed-form equation. A more straightforward and general approach is discovered, which models various heat transfer mechanisms involved in various transformer parts and, in turn, characterizes various heat transfer coefficients. The two most significant and influential inputs are core and winding losses [72].

Compared to the conventional LFT, SST transfers electrical power through a high-frequency transformer of which the flux linkage is established by the switching power converters. The maximum flux is reduced by the high-frequency operation of power converters, which results in a lighter and smaller magnetic core [73].

The basic concept behind the SST is to transform voltage by medium- to high-frequency isolation, potentially resulting in a reduction in volume and weight when compared to a conventional power transformer. As seen in Fig. 2.16, the 50/60-Hz AC voltage is first converted to a high frequency voltage (typically in the range of several kilohertz to tens of kilohertz), which is then stepped up or down by a high frequency transformer with significantly reduced volume and weigh, and finally, recovered to the desired 50/60-Hz voltage to feed the load.

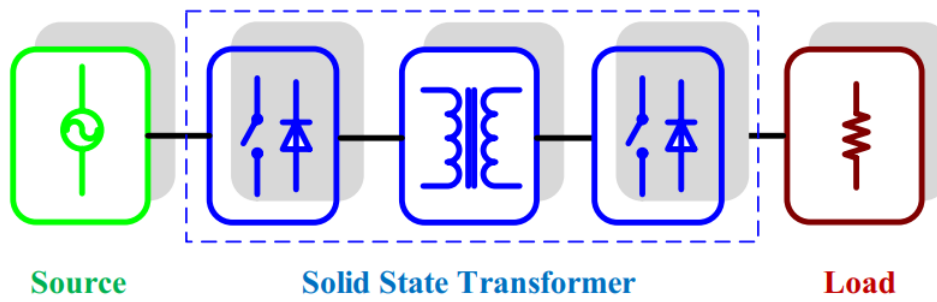


Fig. 2.16 SST configuration

Furthermore, it can be seen from the SST's configuration that it may be possible to obtain some additional functionalities not offered by the conventional transformer. First, similar to FACTS devices, voltage and current regulation is achieved by the use of solid-state semiconductor devices and circuits. This offers promising benefits that are impossible for conventional transformers, such as power flow control, voltage sag compensation, fault current limitation, and others. Second, to enable a new microgrid architecture, voltage source converters connected from the secondary terminal of the SST could easily support a regulated DC bus that could be connected to DC microgrids [74].

2.3.2 Applications

In recent years, a lot of research has been done on the use of power converters that offer medium-frequency galvanic insulation. SSTs provide means to enhance productivity and power density in various applications. The MFT is a crucial component of the conversion stage. It enables a very effective inductive power transfer using frequencies in the range of several kilohertz. Due to the MFT's crucial function, there has been a lot of research done on subjects like power density, winding design, insulation materials, and acoustic noise. Studies of design principles, converter topologies, and semiconductors have been extensively conducted because they directly affect MFT specifications [75].

In addition to exploring SSTs' potential use in the distribution system, efforts have been made to design and implement SSTs with satisfactory performance. On one hand, Fig. 2.17 depicts the conventional distribution system, where the transformer is used to integrate renewable energy sources and energy storage devices, power the traction/locomotive system, and interface the FACTS devices, such as reactive power compensators and active power filters. On the other hand, Fig. 2.17 also depicts the envisioned SST-based distribution system of the future. It has been found that the SST can functionally replace some power electronics converters and the traditional transformer, suggesting a system that may be more integrated and compact. Additionally, the SST's cost and efficiency problems may be justified. Nonetheless, the reliability and lifetime of the SST interfaced distribution system are a concern for the utilities.

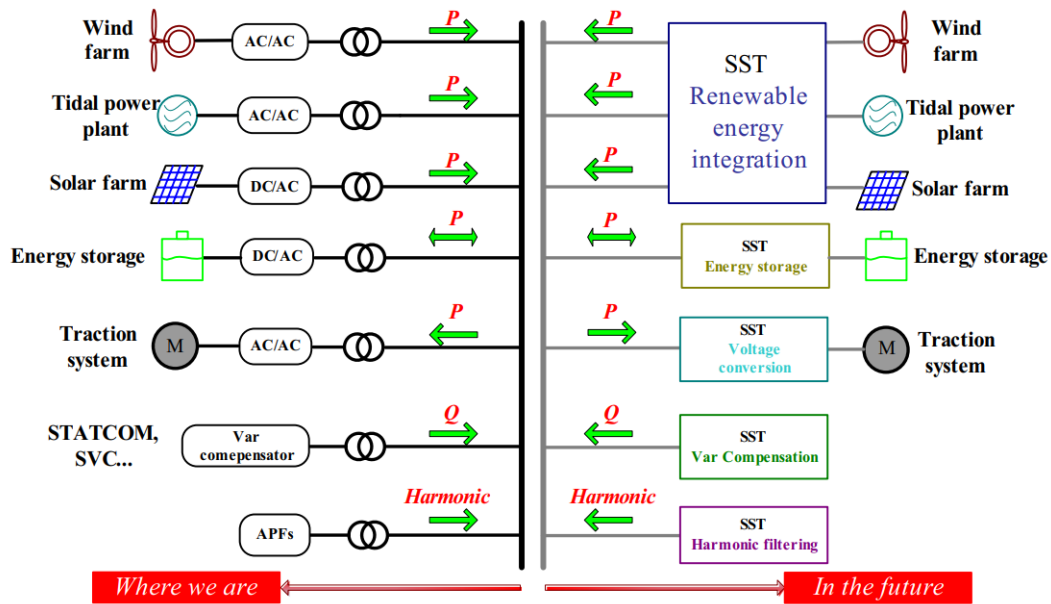


Fig. 2.17 Potential application of SST in the future distribution system

2.3.2.1 Voltage Transformation and Regulation

As shown in Fig. 2.18, the SST has found its application in traction systems. The efficiency of the conventional traction system, which consists of traditional LFT and back-to-back converter, ranges from 88 to 92 percent. As seen in Fig. 2.18, if the system is replaced by the SST,

efficiency will increase to over 95%, allowing for the creation of a more compact and lighter system.

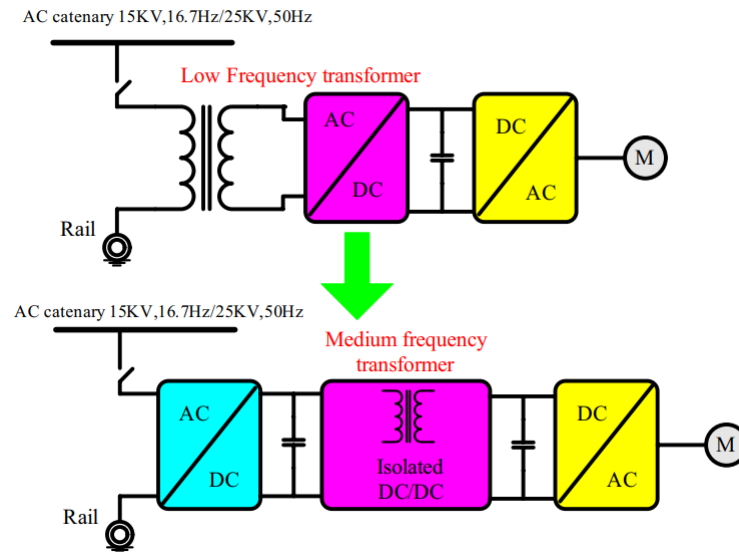


Fig. 2.18 SST-based tractions system

As an illustrative example, ABB declared the deployment of the first MW-level power electronic traction transformer in the field in 2012. More space for the passengers is provided by the smaller size. Additionally, compared to the 0.2 to 0.35kVA/kg of the traditional transformer plus rectifier structure, the power density, of such a system, ranges from 0.5 to 0.75kVA/kg.

The SST can be used to directly connect renewable energy sources like solar, wind, and tidal power plants with the distribution system due to the high penetration of these power sources. To achieve more compact system, an SST replaces the power converters and the LFT. As an illustration, consider the wind energy system with the squirrel cage induction generator in Fig. 2.19. Reactive power compensator may be required for this type of system to stabilize the point of common coupling voltage. As shown in Fig. 2.19, a novel wind energy system can be created by utilizing and combining the active power transfer, reactive power compensation, and voltage conversion functions of SST. A single SST can effectively replace two transformers, one STATCOM, and one local capacitor.

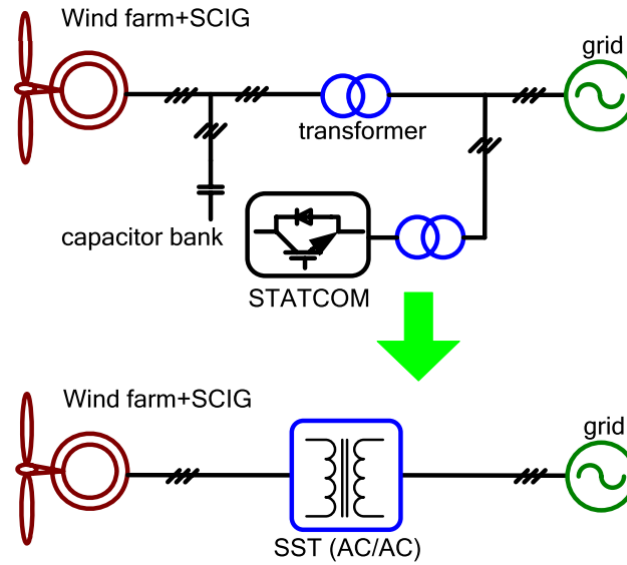


Fig. 2.19 Wind energy system interfaced by SST

From this perspective, the cost gap between traditional transformers and SST technology will be narrowed. When DC link is accessible, SST can also possibly be integrated with energy storage systems. A 45kVA, 2.4kV fast charging station based on SST technology has been demonstrated by Electric Power Research Institute (EPRI). Fig. 2.20 illustrates this technology's basic concept. The electric vehicle is charged using a transformer, AC-DC, and DC-DC converter in the conventional configuration; the system's efficiency is approximately 90%. With the help of SST technology, efficiency can be increased to over 95%. Additionally, it can significantly reduce weight and cost, and it costs half as much as conventional technology, thus overwhelming its counterparts.

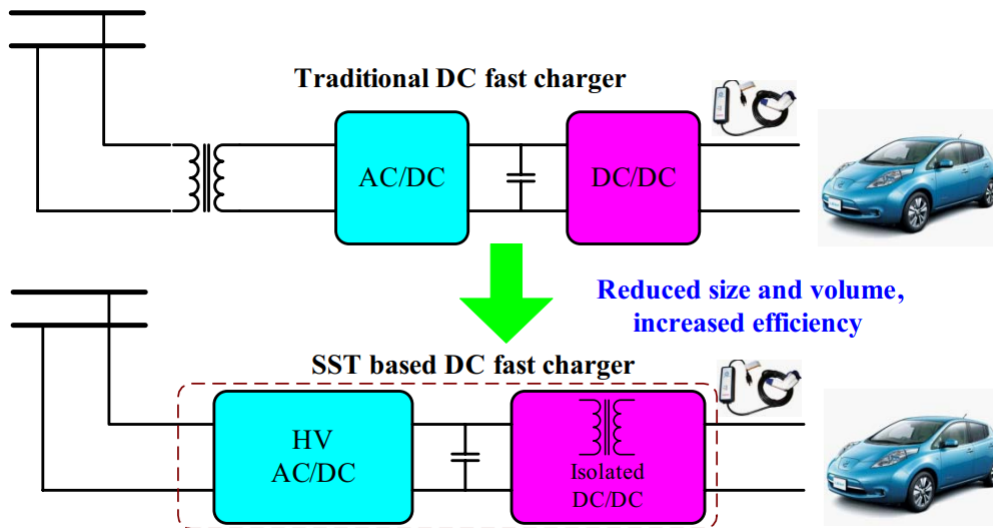


Fig. 2.20 SST-based DC fast charger

2.3.2.2 Reactive Power Compensation and Active Filtering

Depending on the topology adopted, SST may also provide VAR compensation. An SST interfaced wind energy system was proposed with integration of active power transfer, reactive power compensation, and voltage conversion functions. It is demonstrated that the system volume and weight can be further reduced by utilizing the SST's potential reactive power compensation capability. Likewise, dynamic voltage restorers based on SST were investigated. The SST can also handle harmonic current filtering, whereas its capability is influenced by the controller's bandwidth, which is in turn controlled by the switching frequency of the SST. SST can also be used as UPQC by combining these two functions. The high-frequency link UPQC structure used in the distribution system is depicted in Fig. 2.21. Both the series and shunt transformers, which are both running at line frequency, are eliminated by this UPQC. As a result, the system's size and weight can be drastically decreased. This UPQC can be viewed as an SST from the standpoint of isolation and voltage conversion.

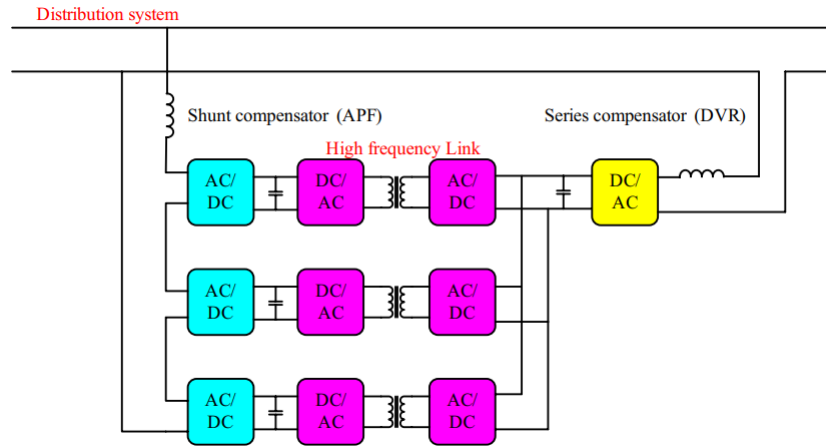


Fig. 2.21 High-frequency link UPQC structure

2.3.2.3 Smart Grid Integration

The SST has also been proposed as an energy router to integrate smart grid applications. The envisioned SST-based microgrid system, which achieves a three-port power flow, is shown in Fig. 2.22. The basic concept is to connect Distributed Renewable Energy Resources (DRER) and Distributed Energy Storage Devices (DESD) using the LV DC link as the common bus. In contrast to the conventional AC grid, which requires a DC-DC plus inverter to connect those DC-type source and load to the mains, only a single stage of conversion is therefore required. In addition, the AC residential grid is also integrated using the SST's LV AC port. As a result, a microgrid system that is more integrated, lighter, and compact can be created. Along with power management techniques that have been suggested, the problem of SST and microgrid integration has also been researched.

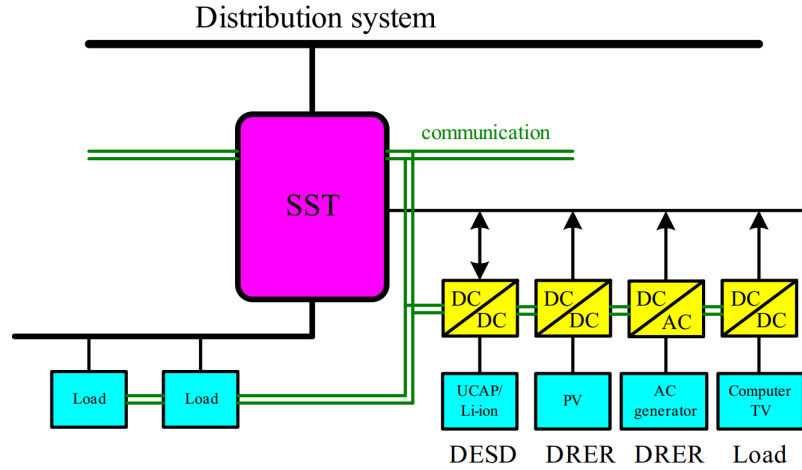


Fig. 2.22 SST for smart grid integration

2.3.2.4 Fault Isolation and Limitation

SST embedded with specific control functions may also implement fault isolation and limitation, in contrast to the passive power transformer. Using the SST in the FREEDM system, a protection method was suggested, and satisfactory performance was shown in real-time digital simulations. Additionally, the SST's potential VAR compensation capability can be used in the power system for transient-fault ride-through, similar to how STATCOM did it in the weak grid system. Additionally, when a fault occurs in the distribution line, the renewable energy sources and energy storage devices connected at the DC port of the SST can continue to function as an uninterrupted power supply, which ensures the critical load receives high-quality power [74].

2.3.3 Challenges

In high frequency medium-voltage SST, the high frequency transformer is a crucial part of the isolated DC-DC converters. Traditionally, the lack of power semiconductor devices with fast switching speeds and low on-state resistance lead to the loss in momentum of the application. The SST's advantages are constrained by its inability to switch at high switching frequencies, which prevents a significant reduction in the size of the magnetic components. With the de-

development of MV power devices like 15kV IGBTs and 10kV MOSFETs, which not only offer low on-state resistances but can also switch at frequencies up to 100kHz, recent research in MV wide band-gap semiconductor devices has closed this gap. As a result, it is now possible to design MV converters for use in systems like SSTs [69].

The loss, cooling rate, and insulation level however, limited the size-reduction enabled by the high frequency. When a high level of isolation is required, the insulation is especially crucial. For transformers with higher isolation voltage levels, which request thick insulation layers, the insulation's restrictions are especially severe. Considering the scenario shown in Fig. 2.23, where SST is coupled to a MV power system, the insulation typically needs to handle transient over-voltage caused by abnormal events (like a system fault and lightning strike) in addition to the rated AC voltage [73].

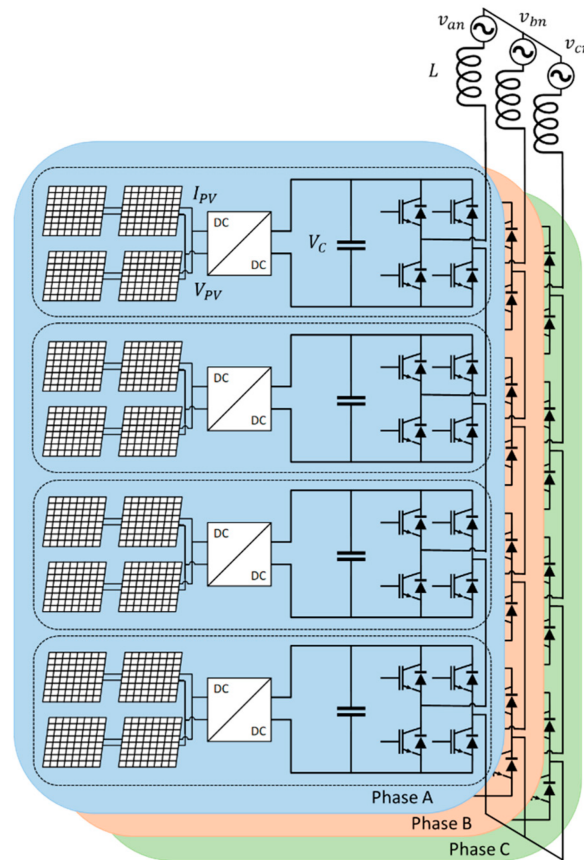


Fig. 2.23 MV grid-connection using SST based power electronics building block

The main goal of high frequency transformer design is to achieve high power density and low loss while not exceeding the materials' limits (maximum electric stress, magnetic flux density, temperature, etc.), which adversely affect the converter's overall efficiency. There is a design conflict, specifically because of the combined cooling and insulation requirements. While pure air insulation provides effective cooling, the resulting MFT size is unacceptable. On the other hand, complete casting of the MFT causes a cooling issue and, due to thermal stresses- is crucial in terms of internal PD [75].

Comparing SST to conventional transformer and technologically advanced counterparts, many additional challenges arise. A feature of the aforementioned power electronic converters, MFTs typically operate with square voltages and non-sinusoidal currents on higher frequencies while LFTs operate at low grid frequencies. This affects coordination of the insulation as well as the losses in the core and winding, which still needs further study. Moreover, in the case of Series Resonant Converter (SRC) based topologies, where the MFT is a component of a resonant circuit, proper design of the MFT electric parameters, magnetization, and leakage inductance is essential for the correct operation of the converter. As a result, the modeling and manufacturing margins associated with parameter control are stricter. Additionally, the desired increase in transformer power density is strongly related to the increase in heat loss density and excess losses in the windings. This is due to enhanced skin and proximity effects that lead to higher temperature gradients unless properly addressed. High density high frequency transformers have a very poor thermal dissipation path, which directly contributes to the thermal challenge. Because of the close proximity of the inner and outer windings, the bobbin and the core, and the inner winding and the bobbin, it is difficult to dissipate the heat generated in these areas [76].

Due to the increased use of insulation media, detailed thermal modeling and coordination

are required to consider these more complex thermal conditions. When oil is eliminated and a compact design is necessary, the transformer power density will be a trade-off between the operating frequency and insulation requirements. Due to this, there are design trade-offs that must be properly handled [74], [77].

Other parts of the SST include power devices, gate drivers, heatsinks, control circuits, cooling systems, auxiliary power, and other ancillary circuitry in addition to the high-frequency transformer. As a result, without careful design, the desired lower volume and weight reduction may not be possible. In fact, only when the proportion of the high-frequency transformer is reasonably larger than the rest of the parts, the effective size and weight reduction of the SST, compared to the traditional transformer, can be achieved. Consequently, significant efforts are still required for the SST to develop quickly [74].

Therefore, one of the solutions for high-voltage operation could be the series connection of LV power devices. The drawback of this approach is the large loop inductance that comes naturally with this configuration, which, once again, prevents the modules from operating at higher frequencies due to the additional induced voltage that could harm both the devices and other SST components. The standard series connection method mentioned above could be replaced by integrated module packaging of series-connected power device chips, which would minimize loop inductance and allow for high-frequency operation. However, the resultant power module's increased conduction voltage drop reduces system efficiency, making it very challenging to reach efficiency levels on par with those of conventional 50/60Hz transformers [74].

2.3.4 State-of-the-art Power and Voltage Levels

More and more power electronics converters with typical power ratings of tens of kilowatts are used in vehicle and aircraft power systems. In this range, MOSFET switches are not ad-

vantageous. IGBTs predominate in applications with a power range above ten kilowatts, so the corresponding magnetics used operates at frequencies below 100kHz. These applications typically operate at frequencies between 20 and 50kHz, and power ratings greater than 10kW can be categorized in this range. For 50kHz and 50kW DAB DC-DC converter systems, a novel coaxial wound transformer was proposed in one research paper. The coaxial transformer uses a number of toroidal cores and has coaxial type wires wound across them with the goal of decreasing leakage and increasing coupling between primary and secondary windings. The coaxial wire is made up of an inner Litz wire and an outer copper tube for various windings. For this specific structure, the calculation of the leakage inductance is investigated. A high voltage (50kV) transformer for an electrostatic precipitator power supply was developed through research; its main contributions were insulation and electrostatic analysis. For this 25kHz and 25kV (pulsed-power) transformer, no special loss and parasitic calculation considerations have been discussed. A 350kW transformer for a 10kHz DAB DC-DC converter system was described in another work. Coaxial cables and a wound core made of nanocrystalline material are used to build transformers. An active cooling system was implemented inside the winding, and calculations were made for the frequency-dependent resistance and leakage inductance of the winding. The largest nanocrystalline core ever reported in the literature, 330kW and 20kHz nanocrystalline cut-core transformers have recently been developed for accelerator klystron radio frequency amplifier power systems. To increase density, nanocrystalline magnetic material has been used. High power transformers typically have cable or Litz wire windings instead of planar structures, and ferromagnetic materials are used to achieve higher density. For all of the aforementioned transformers, according to [78], there is a lack of precise and practical methods for calculating loss and parasitics.

The fact that four well-known high-voltage SST designs—namely, the Universal and Flex-

ible (UNIFLEX), EPRI, GE, and ABB—have already been created and thoroughly tested for various applications makes them stand out. The four topologies’ performance comparisons are listed in Table 2.2.

Table 2.2 Performance Comparison of Four SST Topologies

	<i>UNIFLEX</i>	<i>EPRI</i>	<i>GE</i>	<i>ABB</i>
Power rating	300 KVA	45 KVA	1MVA	1.2MVA
Phase number	Three	Single	Single	Single
Voltage rating	3.3 KV	2.4 KV	13.8 KV	15 KV
Transformer frequency	2 KHz	20 KHz	20KHz	1.8KHz
Eliminates oil	No	Yes	Yes	Yes
Var compensation	Yes	Yes	No	Yes
Voltage sag compensation	Yes	Yes	No	Yes
Voltage regulation	Yes	Yes	Yes	Yes
Harmonic isolation	Yes	Yes	Yes	Yes
Common DC link	No	Yes	Yes	Yes
Energy storage option	Yes	Yes	Yes	Yes
Fault isolation	Yes	Yes	Yes	Yes
Bidirectional power flow	Yes	No	Yes	No
Control complexity	complicated	Average	Easy	Average
Efficiency	92%	96%	98%	95%
Delivery Year	2009	2012	2011	2012
Application	Smart grid	DC charge station	Substation	Traction

The UNIFLEX SST topology for a smart grid application is shown in Fig. 2.24. It functions essentially as a three-stage, three-port power electronics converter for UNIFLEX power management in a future electricity network. The front-end stage is a cascaded multilevel converter, and the intermediate stage is a number of interleaving DC-DC converters. It connects LV grids, like the 415V system, with 3.3kV distribution level voltage. The transformer's core material is chosen to be amorphous, and the operating frequency is set at 2kHz. For this MFT, oil is used for cooling and insulation.

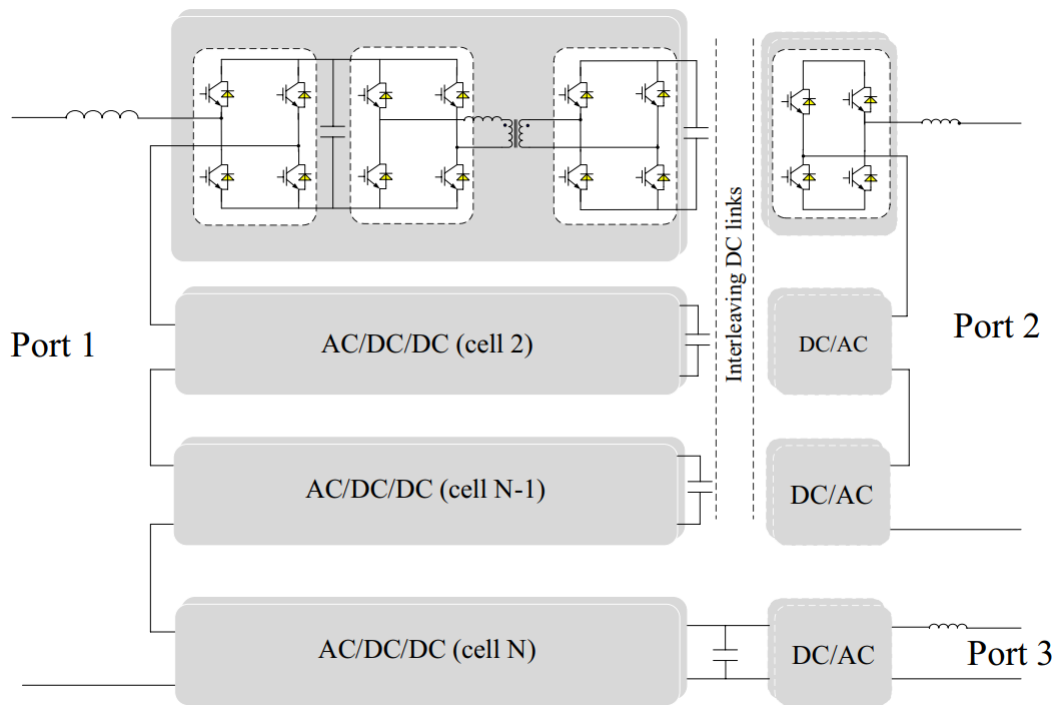


Fig. 2.24 UNIFLEX SST topology for smart grid application

The EPRI SST topology for a DC fast charger application is shown in Fig. 2.25. For both the rectifier stage and the primary side of the DC-DC stage, the diode clamped multilevel converter is used, and the 18kV/60A multilevel IGBT module using the integrated module packaging method is used. To create the LV DC link, the secondary side of the DC-DC stage is where the simple diode rectifier is used. The high-frequency transformer, which operates at a frequency of 20kHz, uses a ferrite core. Another high-efficiency DC-DC converter is connected

to interface with the battery pack in the DC fast charger application.

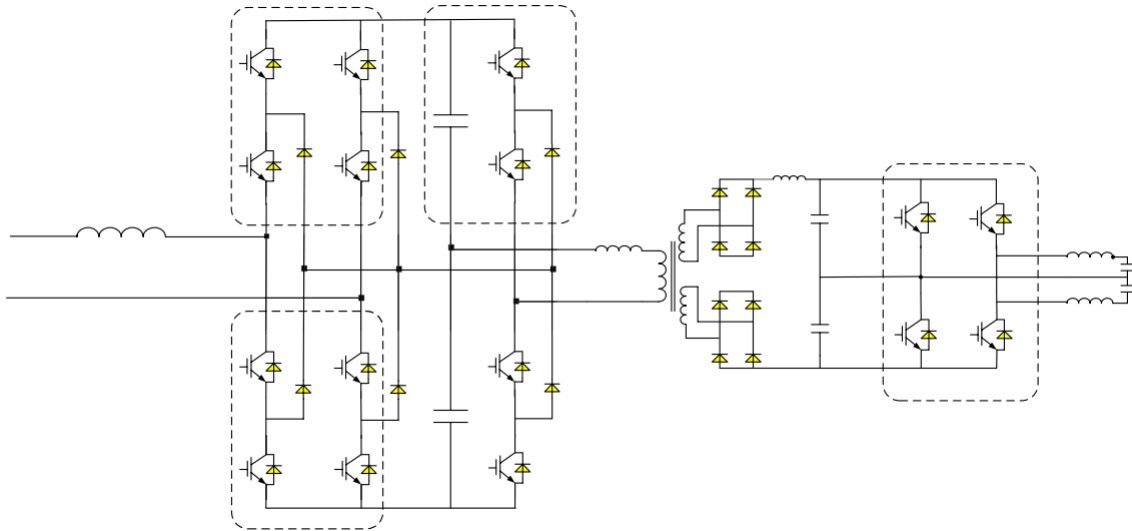


Fig. 2.25 EPRI SST topology (with inverter stage) for DC fast charger application

The fundamental component of the GE SST topology for substation application is shown in Fig.2.26. For the HV side, the 10kV/120A SiC half bridge module is used, and they are linked in series to lessen the voltage stress. In order to lower core loss, the transformer's switching frequency is set to 20kHz, and nanocrystalline core is accordingly chosen as the transformer's core material. This unit's high efficiency is one of its distinguishing features, thanks to line-frequency switching on the high- and low-voltage rectifier/inverter sides as well as soft switching capabilities in the DC-DC stage. However, since this device can only perform the fundamental voltage transformation and isolation tasks of a conventional transformer, it might not be appropriate for use in traction and smart grid applications.

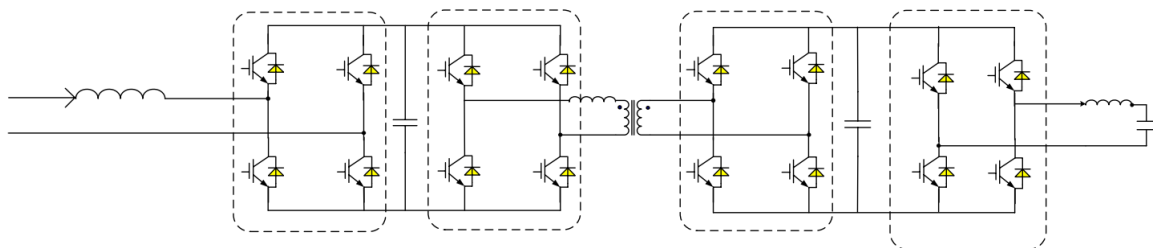


Fig. 2.26 Basic unit of GE SST topology for substation application

The ABB SST topology for traction application is shown in Fig. 2.27. The input stage to connect to the 15kV grid is a cascaded multilevel converter, and the main switch for the H-bridge module is a 6.5kV IGBT. The secondary side is then connected in parallel to step-down the voltage, and a nanocrystalline core is used for the transformer design. LLC resonant converters are then cascaded to each DC link. The LLC converter operates in open-loop mode at its resonant frequency point for maximum available efficiency operation because the DC-DC stage of the system lacks a dedicated control [74].

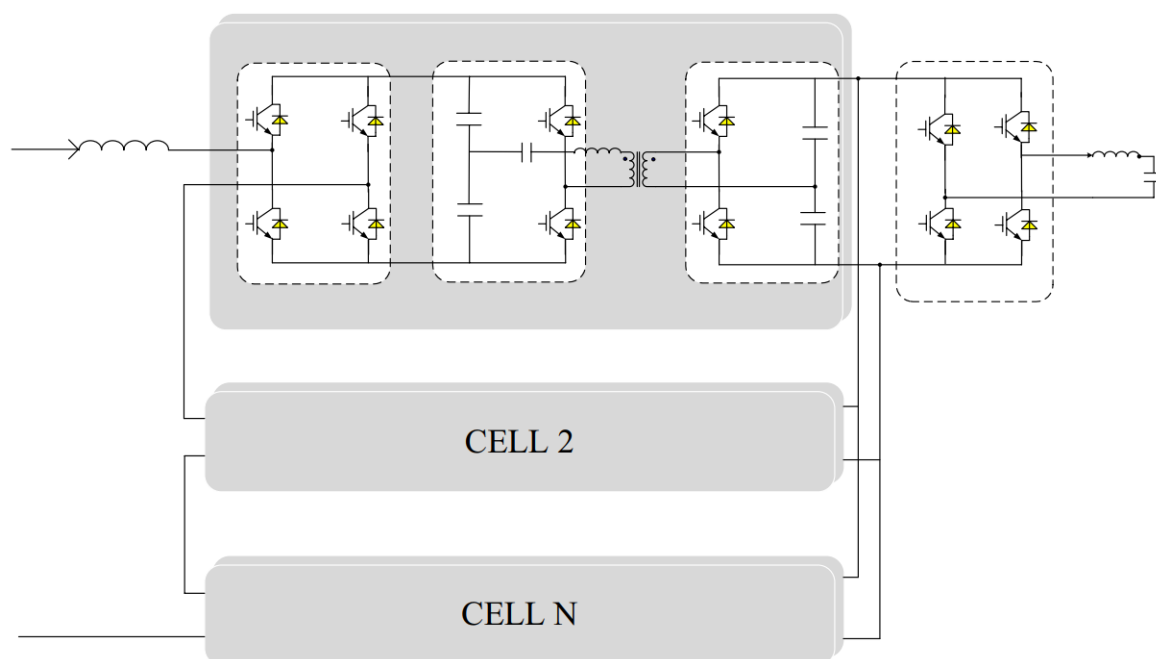


Fig. 2.27 ABB SST topology for traction application

CHAPTER 3

Power Converter Topology

3.1 Three-Level to Two-Level Topology

The conventional bidirectional isolated DC-DC topology can be reduced in voltage stress by utilizing the three-level structure. Recently, researchers have reported the development of bidirectional isolated DC-DC converters with three levels topologies. Literature has studied the modulation strategy of Neutral Point Clamped (NPC) DAB converters to minimize losses. The detailed operation principle of the three-level DAB converter with DPS control was presented along with the developed control algorithm to ensure that the voltage stress of each switch is half of the port voltage. In addition, literature investigated the characteristics of the three-level three-phase DAB converter as well as the soft switching range of the three-level three-phase DAB converter [79]. The voltage limitations of commercially available semiconductor switches result in DAB converters being cascaded to achieve high voltages for medium and high-voltage applications. This voltage constraint of semiconductor switches has been investigated with IGBTs. Multilevel DAB (ML-DAB) can be utilized to overcome this voltage constraint in semiconductor switches. ML-DAB can be used without cascading in medium voltage (generally 2.3kV to 6.6kV) applications, or, if cascaded, reduce the number of cascading modules for high voltage power conversion applications, such as High Voltage Direct Current (HVDC).

Traditionally, power converters that synthesize more than two voltage levels, such as the

NPC, Cascaded H-Bridge (CHB), and Flying Capacitor (FC), are referred to as multilevel converters. Multilevel topologies are typically used in high-voltage inverter applications. CHB topologies are commonly used in combination with cascaded DABs to achieve increased voltages, and DAB modules themselves do not synthesize voltages at multiple levels (e.g. 3L, 5L, 7L, etc.). In various industrial applications, the 3L NPC is an advantage because of its simple control and modulation scheme and simple circuit structure. There has not been a lot of publications on ML-DAB. One research work on Silicon Carbide Junction Gate Field-Effect Transistor (SiC-JFET)-based 25kW, high switching frequency DAB is proposed with both primary and secondary bridges producing two-level voltages, though the second bridge is arranged in the NPC configuration. The power flow of a Semi-Dual Active Bridge (S-DAB) is regulated by phase-shifted voltage waveforms produced by the primary and secondary bridges. With a secondary bridge based on NPC technology, symmetric modulation of 2L-to-5L bridge voltages has been introduced, allowing ML-DABs to define voltage waveforms and control power flow by having a simple mathematical representation and a minimal number of parameters. The capacitor voltage balance of an NPC-based multilevel DAB is reported as well.

3.1.1 Symmetric Phase-Shift Modulation

Two bridges are assumed to have different DC bus voltages in this ML-DAB configuration. The voltage step-up and step-down schematics of the NPC-based 2L-5L DAB are shown in Figs. 3.1 and 3.2, respectively. There are different voltage levels at the two ends of most DAB-based power electronic converters, and this ML-DAB is ideal for these types of applications. The higher voltage level can be achieved by cascading multiple ML-DABs if the required voltage level is much higher than the DC bus voltage, thereby facilitating the conversion of large quantities of power (in the order of megawatts) using fewer ML-DAB modules. As a result of this

methodology, the overall efficiency is improved and the power density is increased.

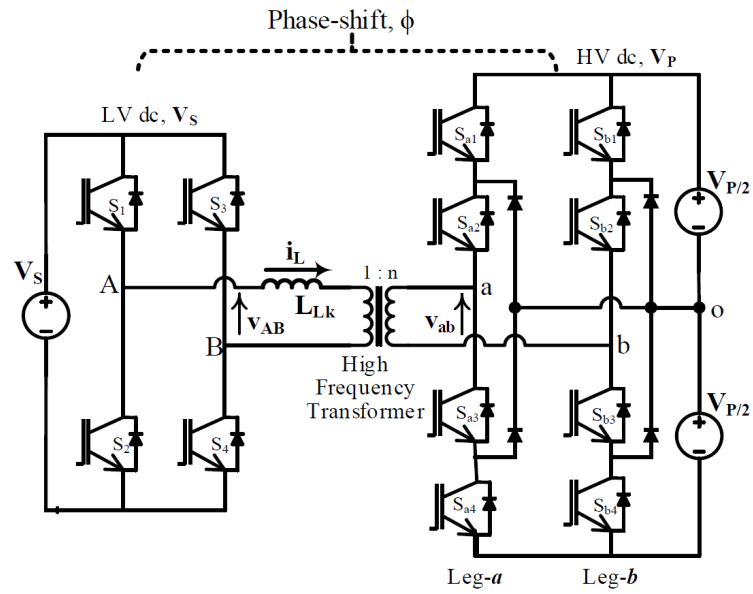


Fig. 3.1 Boost configuration ($V_P > V_S$) a multilevel dual active bridge (ML-DAB), where the transformer primary voltage (v_{AB}) two-level (2L) and the secondary (v_{ab}) of 5L

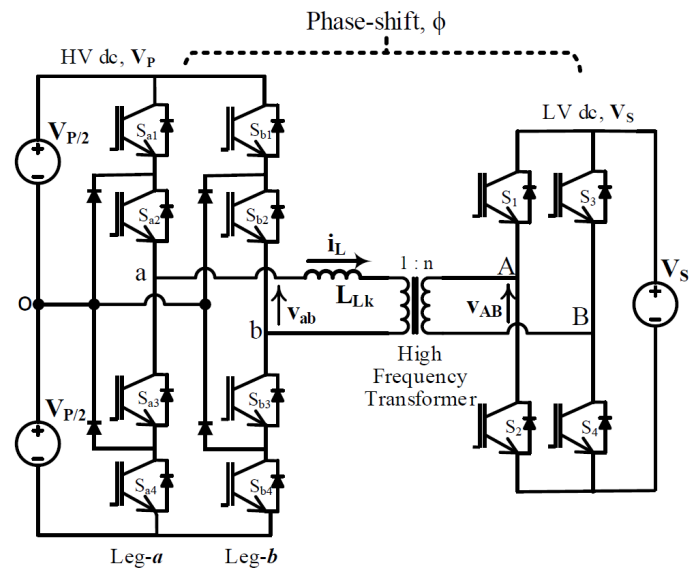


Fig. 3.2 Buck configuration ($V_S < V_P$) of the ML-DAB where the transformer primary voltage (v_{ab}) is of 5L and the secondary (v_{AB}) is of 2L

3.1.2 Neutral Point Diode Clamped Configuration

Multilevel topologies such as NPC are commonly used in medium and high-voltage low-voltage industrial applications because of their high power level and flexibility. A leg-to-leg

five-level (5L) voltage waveform v_{ab} is generated by using three-level (3L) diode clamped legs (leg-a, b in Fig. 3.1 and Fig. 3.2). At the transformer LV side, a two-level (2L) square waveform v_{AB} is generated via the low-voltage bridge. In contrast to the 2L voltage source converter, the 3L-NPC configuration utilizes clamping diodes to connect the phase output to the neutral point "o", as shown in Figs. 3.1 and 3.2, which produce a 3L voltage at each NPC leg. The voltage sources in Figs. 3.1 and 3.2 (i.e. V_s , $V_p/2$) are replaced by bulk capacitors, and the input and/or output of the ML-DAB are usually followed by a source, a load, or other converters in real applications. A suitable modulation scheme and current bi-directional switches can be used to configure this ML-DAB for single-phase or three-phase with bi-directional power-flow capability.

3.1.3 Switching States of the 3L-NPC Bridge

In 1980, numerous aspects of the NPC inverter concept were developed by researchers. These include modulation schemes, voltage levels, capacitor voltage balancing, harmonic mitigation, and active clamping instead of diodes for this converter. A three-phase inverter using a 3L-NPC has been extensively studied in the literature in terms of switching and modulation. ML-DAB is an inverter with a switching pattern that is a bit different from conventional inverters. In contrast to 3L-NPC line frequency inverters at 50/60Hz, the switching frequency of an ML-DAB is considered the fundamental frequency. It is possible to visualize the three-level voltage synthesized in a 3L-NPC leg in Table 3.1 for both positive and negative current flows ($i_a > 0$) ($i_a < 0$).

Table 3.1 Switching states in a 3L-NPC leg

Switching States	Status of the Switches in 3L-NPC Leg- <i>a</i>				3-Level LEG Voltage, v_{ao}
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	
+	ON	ON	OFF	OFF	$+\frac{V_P}{2}$
0	OFF	ON	ON	OFF	0
-	OFF	OFF	ON	ON	$-\frac{V_P}{2}$

Based on the combination of major switching states shown in 3.3, a 3L voltage waveform can be formed. As an advantage over the two-level inverter, the 3L-NPC only has the capability of withstanding half (i.e. $V_P/2$) of the DC bus voltage during the transition between states, resulting in lower dv/dt . Since this scheme involves switching all four switches (S_{a1} to S_{a4}) in a leg, two of which are activated and the other two are turned off, it is not possible to switch between positive and negative states. As well as double switching losses, leg-b switches in a similar fashion to produce a three-line voltage waveform with a small dead time between different states. This modulation scheme illustrates how v_{bo} is phase-shifted by $\alpha + \beta$ to produce a leg-to-leg voltage waveform across the transformer (Fig. 3.4).

Two complementary switches operate on each leg of the two-level bridge at a 50% duty cycle. When S_1 and S_4 are activated, the leg-to-leg square wave voltage v_{AB} is $+V_S$, whereas when S_2 and S_3 are turned on, the voltage v_{AB} is $-V_S$. Fig. 3.4 illustrates gate pulses across 12 switches, from S_1 to S_4 , S_{a1} to S_{a4} , S_{b1} to S_{b4} for both 2L and 5L bridges in a boost topology. Also, it illustrates voltage waveforms (v_{AB} , v_{ab}) across the high frequency transformer and currents (i_L and i_L/n) through the leakage inductor.

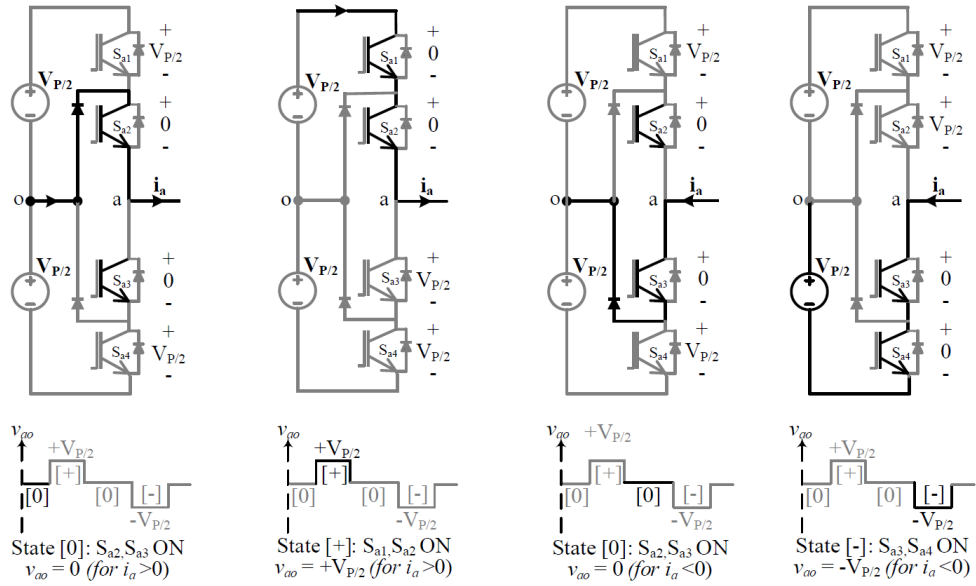


Fig. 3.3 Switching states and corresponding 3L voltage v_{ao} synthesized from leg-a of a 3L-NPC bridge

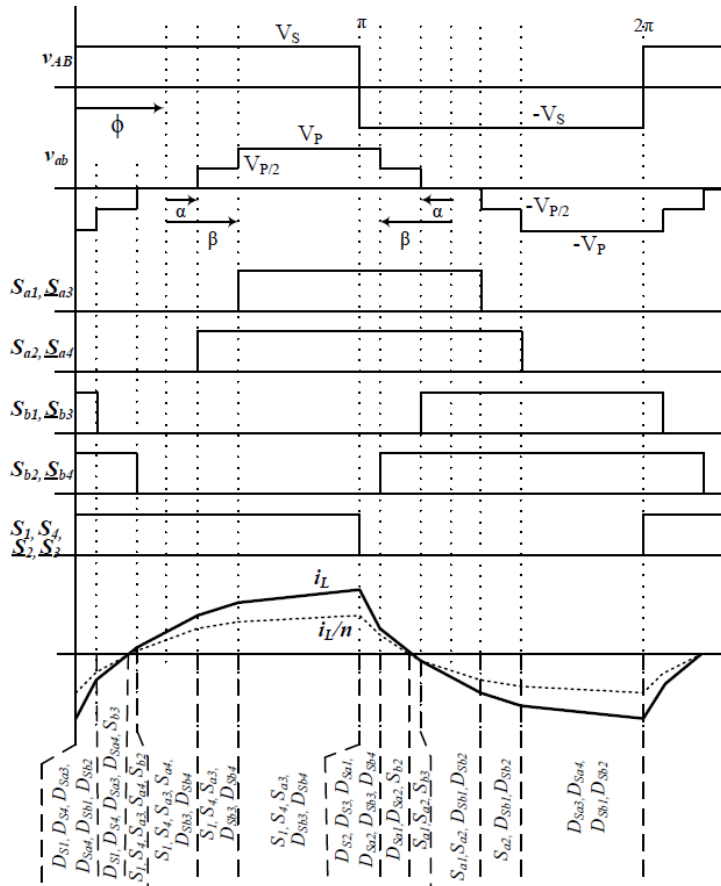


Fig. 3.4 Switch pulses and corresponding voltage waveforms and primary current in a 2L-5L DAB boost topology

3.1.4 Symmetric Modulation

A 5L voltage v_{ab} is synthesized using angular distances (i.e. α, β) instead of the duty cycle, by defining the switching pulses and resulting voltage waveforms. Throughout a switching period, these angles α, β are symmetrically measured at zero, π , and 2π (Fig. 3.5).

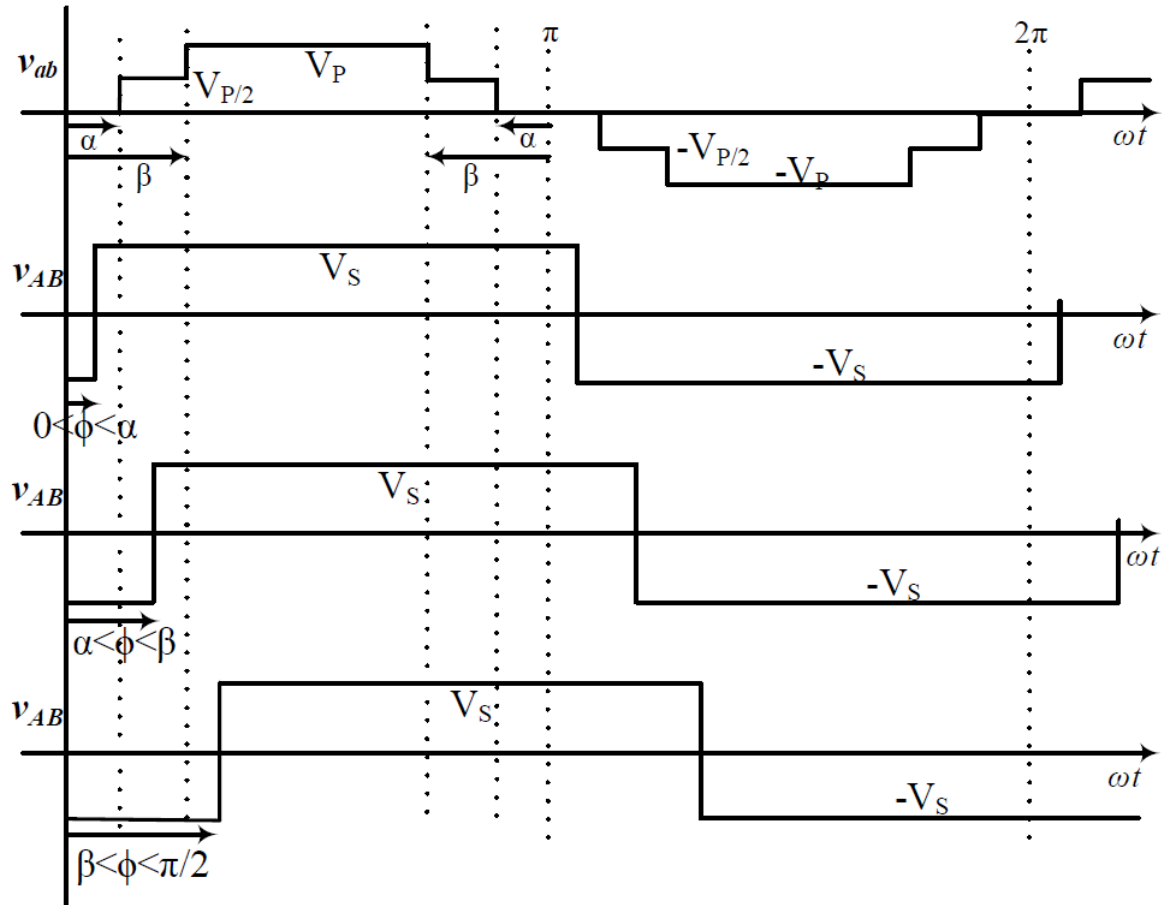


Fig. 3.5 Voltage waveforms in a 5L-2L DAB for three different cases of buck topology when formed using $D = 0.5$

The zero voltage level, v_{ab} , and π are considered at the midpoint of the 5L voltage level. Zero and π are considered at the midpoint of the zero voltage level of the 5L voltage v_{ab} . Defining v_{ab} in a symmetrical manner is advantageous as only a few parameters are required (α, β), which can be described and calculated using the ML-DAB equation. It is possible to use these parameters α and β for improving the Total Harmonic Distortion (THD) and voltage

balancing of capacitors by shaping the multilevel voltage waveform. As a control parameter for power flow in the ML-DAB, the phase-shift angle ϕ is independent of α, β .

To produce a zero-average symmetric alternating waveform, the low-voltage (V_S) bridge legs should be switched complimentary at the duty cycle (D) in a range of zero to 50% ($0 < D < 0.5$). If $D = 0.5$, a 2L ($v_{AB} = +V_S, -V_S$) voltage v_{AB} will be formed, and if $D < 0.5$, a 3L ($v_{AB} = +V_S, 0, -V_S$) voltage will be produced (Fig. 3.6). This 3L voltage at the low voltage bridge is also generated symmetrically and equally spaced from zero and π by an angle γ . This single parameter γ can define the 3L v_{AB} for the whole range of 0.5.

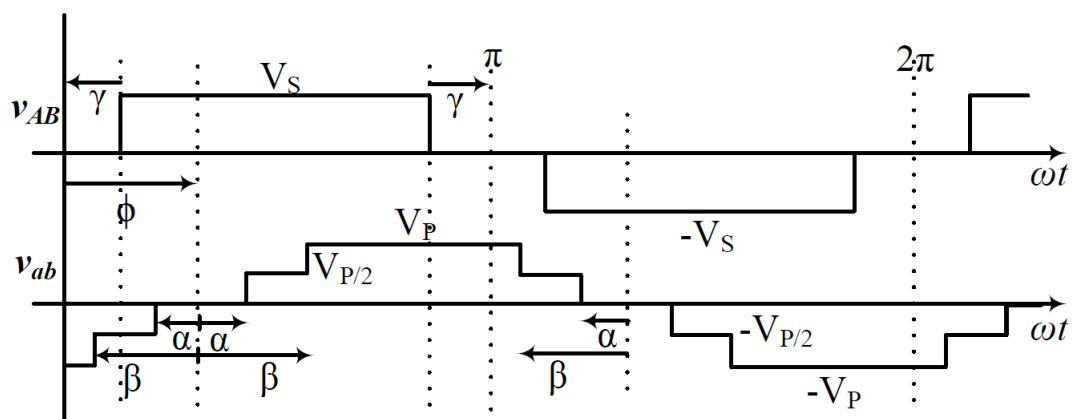


Fig. 3.6 Voltage waveforms in a 3L-5L DAB boost topology when v_{AB} formed using $D < 0.5$

3.1.5 Power Flow Equations and Soft Switching

A phase-shift angle (ϕ) between v_{AB} and v_{ab} determines the flow of power in ML-DAB, as is the case with conventional DAB. A primary referred leakage inductance is assumed as L_{LK} in Fig. 3.1 and 3.2. To analyze the power flow through each of the ML-DABs shown in the Figs. 3.4 - 3.6, the current i_L through the leakage inductor should be analyzed.

3.1.5.1 2L-5L DAB Boost Topology

The switching and modulation for a 2L-5L DAB boost topology are shown in Fig. 3.4. The 2L v_{AB} assumed to start at angle zero, and 5L v_{ab} is lagging v_{AB} by the phase-shift angle ϕ , ($0 < \phi < \pi/2$). From the basic inductor voltage relation we get:

$$\begin{aligned}
 v_L &= L \cdot \frac{di_L}{dT} \\
 \text{or, } i_L(t) &= \frac{1}{L} \int_{t_1}^{t_2} v_L dt \\
 \text{or, } i_L(\theta) &= \frac{1}{wL} \int_{\theta_1}^{\theta_2} v_L d\theta \\
 \text{where; } \theta &= wt
 \end{aligned} \tag{3.1}$$

One switching cycle period has been converted to 2π radians in the following equations. Now, writing this $i_L(\phi)$ equation for each segment of v_L from zero to π as shown in Fig. 3.4, we get:

for $0 < \theta < (\phi - \beta)$:

$$\begin{aligned}
 i_L(\theta) &= \frac{V_s + \frac{V_P}{n}}{wL} \cdot \theta + i_L(0) \\
 i_L(\phi - \beta) &= \frac{V_s + \frac{V_P}{n}}{wL} \cdot (\phi - \beta) + i_L(0)
 \end{aligned} \tag{3.2}$$

for $(\phi - \beta) < \theta < (\phi - \alpha)$:

$$i_L(\phi - \alpha) = \frac{V_s + \frac{V_P}{2n}}{wL} \cdot (\phi - \alpha - \phi + \beta) + i_L(\phi - \beta) \tag{3.3}$$

for $(\phi - \alpha) < \theta < (\phi + \alpha)$:

$$i_L(\phi + \alpha) = \frac{V_s}{wL} \cdot (\phi + \alpha - \phi + \alpha) + i_L(\phi - \alpha) \tag{3.4}$$

for $(\phi + \alpha) < \theta < (\phi + \beta)$:

$$i_L(\phi + \beta) = \frac{V_S - \frac{V_P}{2n}}{wL} \cdot (\phi + \beta - \phi - \alpha) + i_L(\phi + \alpha) \quad (3.5)$$

for $(\phi + \beta) < \theta < \pi$:

$$i_L(\pi) = \frac{V_S - \frac{V_P}{n}}{wL} \cdot (\pi - \phi - \beta) + \frac{V_S - \frac{V_P}{2n}}{wL} \cdot (\beta - \alpha) + \frac{V_S}{wL} \cdot (2\alpha) + \frac{V_S + \frac{V_P}{2n}}{wL} \cdot (\beta - \alpha) + \frac{V_S + \frac{V_P}{n}}{wL} \cdot (\phi - \beta) + i_L(0) \quad (3.6)$$

Assuming zero average current through the transformer, $i_L(0) = -i_L(\pi)$, or

$$\begin{aligned} -2i_L(0) &= \frac{V_S}{wL} \cdot (\pi) - \frac{V_P}{2nwL} \cdot (2\pi - 4\phi) \\ \text{or, } i_L(0) &= \frac{V_P}{nwL} \cdot \left(\frac{\pi}{2} - \phi\right) - \frac{V_S}{wL} \left(\frac{\pi}{2}\right) \end{aligned} \quad (3.7)$$

Putting this expression of $i_L(\text{zero})$ from in the above equations, we can get $i_L(\theta)$ at different points,

$$\begin{aligned} i_L(\phi - \beta) &= \frac{V_S}{wL} \left(\phi - \beta - \frac{\pi}{2}\right) + \frac{V_P}{nwL} \left(\frac{\pi}{2} - \beta\right) \\ i_L(\phi - \alpha) &= \frac{V_S}{wL} \left(\phi - \alpha - \frac{\pi}{2}\right) + \frac{V_P}{nwL} \left(\frac{\pi}{2} - \frac{\alpha}{2} - \frac{\beta}{2}\right) \\ i_L(\phi + \alpha) &= \frac{V_S}{wL} \left(\phi + \alpha - \frac{\pi}{2}\right) + \frac{V_P}{nwL} \left(\frac{\pi}{2} - \frac{\alpha}{2} - \frac{\beta}{2}\right) \\ i_L(\phi + \beta) &= \frac{V_S}{wL} \left(\phi + \beta - \frac{\pi}{2}\right) + \frac{V_P}{nwL} \left(\frac{\pi}{2} - \beta\right) \end{aligned} \quad (3.8)$$

The average power flow expression from the primary to secondary bridge through the leakage inductance can be written as follows:

$$P_o = \frac{1}{\pi} \int_0^\pi V_{AB}(\theta) \cdot i_L(\theta) d\theta \quad (3.9)$$

Using (3.3) to calculate the above power equation, we obtain the simplified power equation as follows:

$$P_o = \frac{V_P V_s}{nwL} \cdot \left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi} \right) \quad (3.10)$$

$$\text{or, } P_{o,pu} = m \left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi} \right), \text{ where, } m = \frac{V_P}{nV_s}, P_{base} = \frac{V_s^2}{wL} \quad (3.11)$$

Where P_O is the average power ($P_{Op.u}$ the per unit power) measured at the output of the converter with the variables defined as, $w=2(\pi)(f_s)$ where f_s is the switching frequency, n is the transformer turn ratio, m is the voltage conversion ratio defined as $m=V_P/(nV_s)$ and L is the primary inductance (L_{LK}) used at the high-frequency link. The per unit power vs. ϕ and β , while α is chosen to be fixed at 10° , is shown in Fig. 3.7 for different m values. Power vs. ϕ and β planes with different m -values for a 2L-5L DAB boost topology are shown in Fig. 3.7.

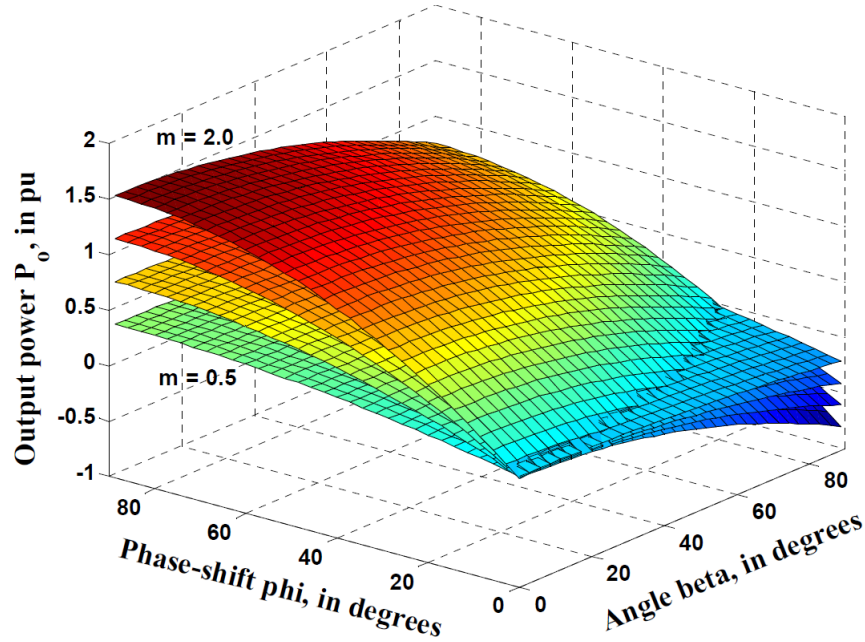


Fig. 3.7 ML-DAB output power $P_{Op.u}$ vs. ϕ and β with $\alpha = 10^\circ$ for $m = 0.5, 1, 1.5$ and 2

3.1.5.2 5L-2L DAB Buck Topology

The voltage waveforms for a 5L-2L DAB buck topology are shown in Fig. 3.5. The 5L v_{ab} is assumed to start at angle zero, and 2L v_{AB} is lagging by the phase-shift angle ϕ . In this topology, based on the value of ϕ , there may be three cases; Case I: $0 < \phi < \alpha$, Case II: $\alpha < \phi < \beta$, and Case III: $\beta < \phi < \pi/2$. In each case, a power flow equation has been formulated using the same procedure described in (3.1) to (3.11):

$$Case I : P_o = \frac{V_P V_S}{nwL} \phi \left(1 - \frac{\alpha}{\pi} - \frac{\beta}{\pi}\right); 0 < \phi < \alpha \quad (3.12)$$

$$Case II : P_o = \frac{V_P V_S}{nwL} \left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\phi\beta}{\pi}\right); \alpha < \phi < \beta \quad (3.13)$$

$$Case III : P_o = \frac{V_P V_S}{nwL} \left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}\right); \beta < \phi < \frac{\pi}{2} \quad (3.14)$$

Using equation (3.14) as a starting point, the following expression can be rewritten as follows:

$$P_o = m \frac{V_s^2}{wL} \left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}\right) \quad (3.15)$$

where, $m = \frac{V_p}{nV_s}$

By analyzing the phase shift between the primary and secondary side bridge voltages, equations (3.10) and (3.15) confirm the bidirectional power-flow capability of this ML-DAB converter. According to the three different scenarios outlined above, Fig. 3.8 displays the flow of power from the 5L to 2L bridge.

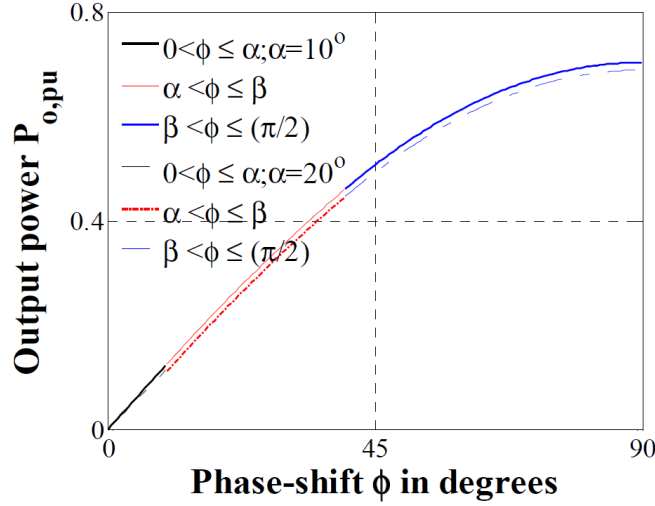


Fig. 3.8 Power flow through DAB for all three cases (3.12) to (3.14), concerning phase-shift ϕ ; here, $\alpha=10^\circ$ and 20° , $\beta=40^\circ$ are assumed for calculation

3.1.5.3 3L-5L DAB Boost Topology

The primary and secondary voltage waveforms for a 3L-5L DAB boost topology are shown in Fig. 3.9. The 3L v_{AB} assumed to start at angle γ after zero, and 5L v_{ab} is lagging v_{AB} by the phase shift angle ϕ . The pulse width of the 3L waveform is assumed symmetrically reduced by an angle of γ , which results from switch duty cycles $D < 0.5$. Using the same sector-wise inductor current analysis, as shown in (3.1) to (3.10), the power flow equation for this topology has been derived as,

$$P_{o,pu} = \left[m \left(\phi - \frac{\phi^2}{\pi} + \frac{\beta\gamma}{\pi} + \frac{\gamma}{2} - \frac{\beta^2}{2\pi} - \frac{\alpha^2}{2\pi} \right) + \gamma \left(\frac{\pi + \beta - \phi - \gamma}{2\pi} \right) \right] \quad (3.16)$$

If we put $\gamma = 0$ in (3.16), it reduces to the 2L-5L power equation in (3.11). Similarly, if the condition is such that $\alpha = \beta = 0$, equations (3.11) and (3.16) reduce to the conventional two-level DAB converter equations.

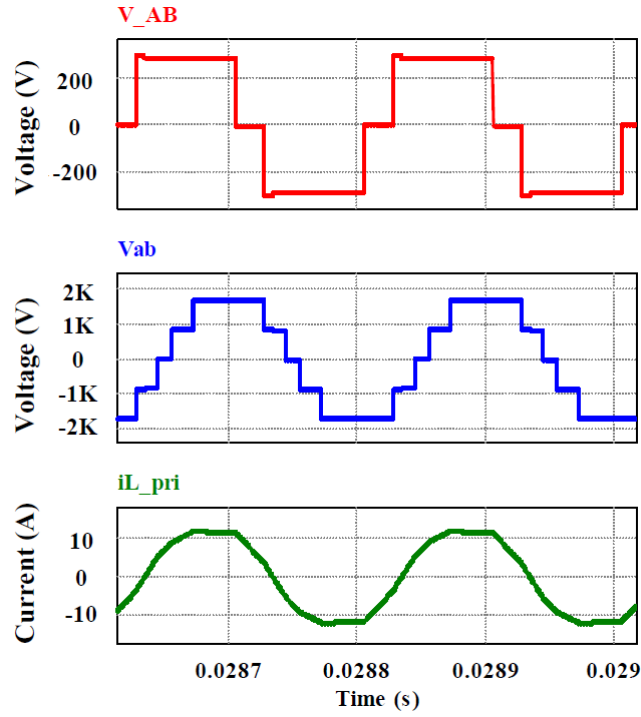


Fig. 3.9 Primary 3L voltage v_{AB} , secondary 5L voltage v_{ab} and current through the primary referred leakage inductance i_L ; where test case was done for $V_S = 290\text{V}$, $V_P = 1868\text{V}$, $\alpha = 10^\circ$, $\beta = 40^\circ$, $\gamma = 20^\circ$ and $\phi = 60^\circ$.

3.1.5.4 Soft Switching

The per unit output power vs. ϕ - β characteristics is shown in Fig. 3.10, where α is chosen as 15° , as this value gives the minimum THD in five-level v_{ab} . In Fig. 3.11, the two-dimensional view of ϕ - β planes eases the visualization of the boundary values of $\phi > 55^\circ$ and $\beta > 46^\circ$ for achieving soft-switching both in primary (2L) and secondary (5L) bridges, as described in the following subsections. The conventional 2L DAB topology can achieve ZVS for all switches in the entire power range when m is equal to unity. The switching pulses for the 2L-5L DAB switches are shown in Fig. 3.4. It is possible to achieve the same in the primary bridge (S_1 to S_4) with the condition of $i_L(0) < 0$ as shown in Fig. 3.12.

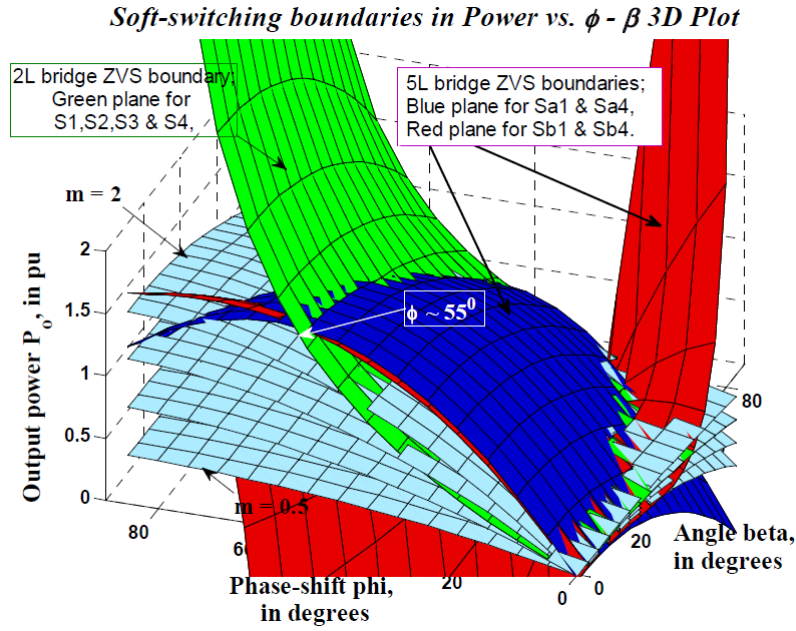


Fig. 3.10 Soft switching boundaries shown in three-dimensional power vs. ϕ - β planes (where $\alpha = 15^\circ$, $0 < \beta < 90^\circ$ and $0 < \phi < 90^\circ$); the grey planes (3.15) show the power vs. ϕ - β relations for $m = 0.5, 1, 1.5, 2$; the green plane (3.17) is for two-level bridge, and the ZVS is possible while operating under this plane; the blue (3.18) and red (3.19) planes are for five-level bridge leg-a and leg-b, respectively

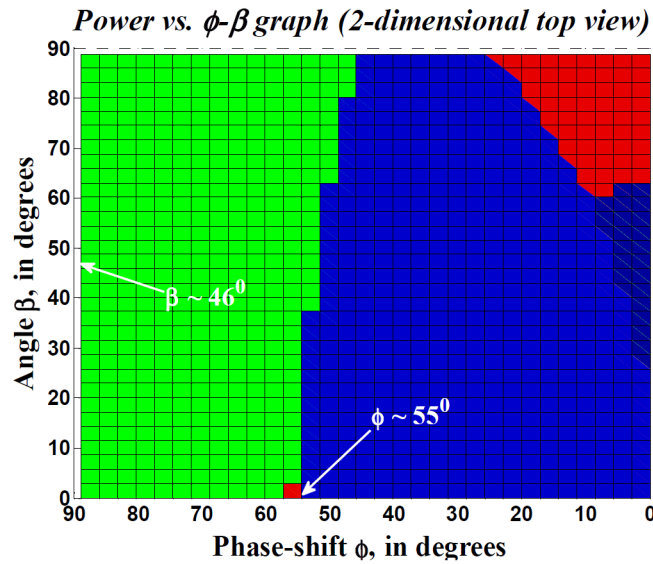


Fig. 3.11 Two-dimensional view of Fig. 3.10 showing the ZVS boundaries of ϕ and β

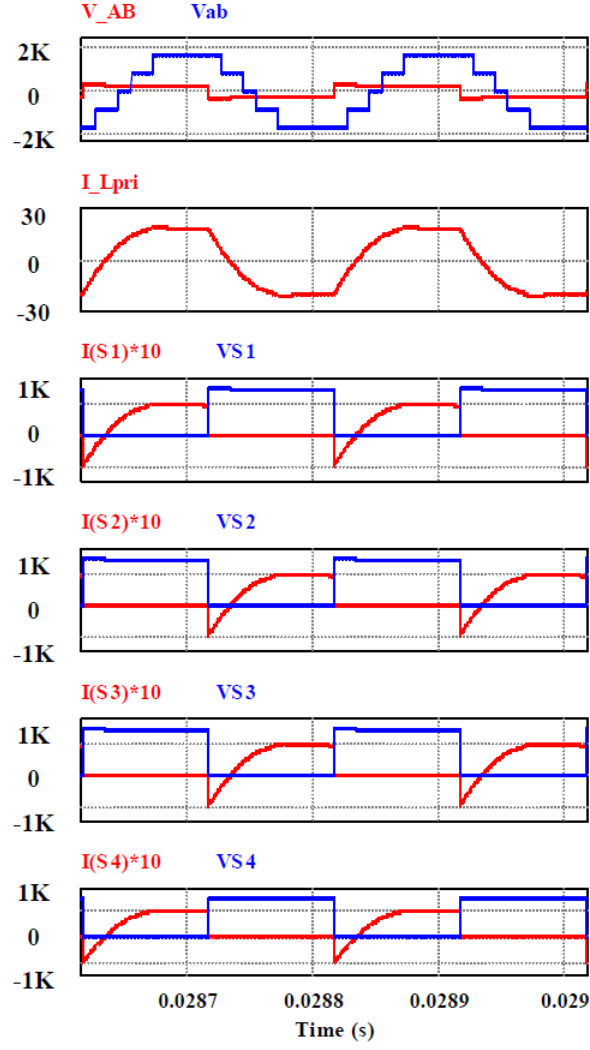


Fig. 3.12 Voltage across the transformer v_{AB} and v_{ab} , inductor current i_L and switch currents and voltages for S_1 to S_4

3.1.5.5 Soft Switching Conditions for the Two-Level (V_S) Bridge

From the current and voltage waveforms of the switches in the primary two-level (V_S) bridge (Fig. 3.12), we can say that the condition for soft-switching in the primary bridge should be,

$$\begin{aligned}
 i_L(0) &< 0 \\
 \text{or, } \frac{V_P}{nwL} \left(\frac{\pi}{2} - \phi \right) - \frac{V_s}{wL} \frac{\pi}{2} &< 0 \\
 \text{or, } \frac{V_P}{nV_s} = m &< \frac{\frac{\pi}{2}}{(\frac{\pi}{2} - \phi)}
 \end{aligned} \tag{3.17}$$

3.1.5.6 Soft-Switching Conditions for the Leg-a of NPC (Five-Level) Bridge

Condition for S_{a1} and S_{a4} to be turned-on at ZVS: $i_L(\phi + \beta) > 0$, or:

$$m > \frac{(\pi - 2(\phi + \beta))}{(\pi - 2\beta)} \quad (3.18)$$

Boundary condition for S_{b1} and S_{b4} to be turned-on at ZVS: $i_L(\phi - \alpha) = 0$, or

$$m = \frac{(\pi - 2(\phi - \alpha))}{(\pi - (\alpha + \beta))} \quad (3.19)$$

In the NPC bridge, ZVS happens in the switches $S_{a1}, S_{a4}, S_{b1}, S_{b4}$ during turn-on at $m = 1$.

The rest of the switches ($S_{a2}, S_{a3}, S_{b2}, S_{b3}$) are also turned-on at a favorable condition when the current through the switch is already zero, as shown in Figs. 3.13 and 3.14 [80].

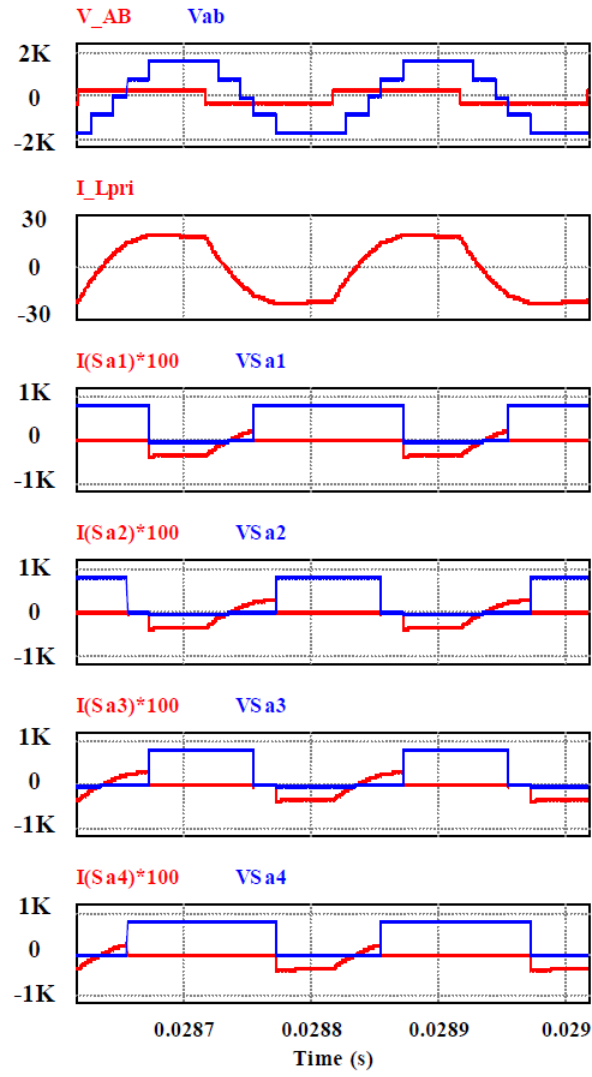


Fig. 3.13 Voltage across the transformer v_{AB} and v_{ab} , inductor current i_L and switch currents and voltages for S_{a1} to S_{a4}

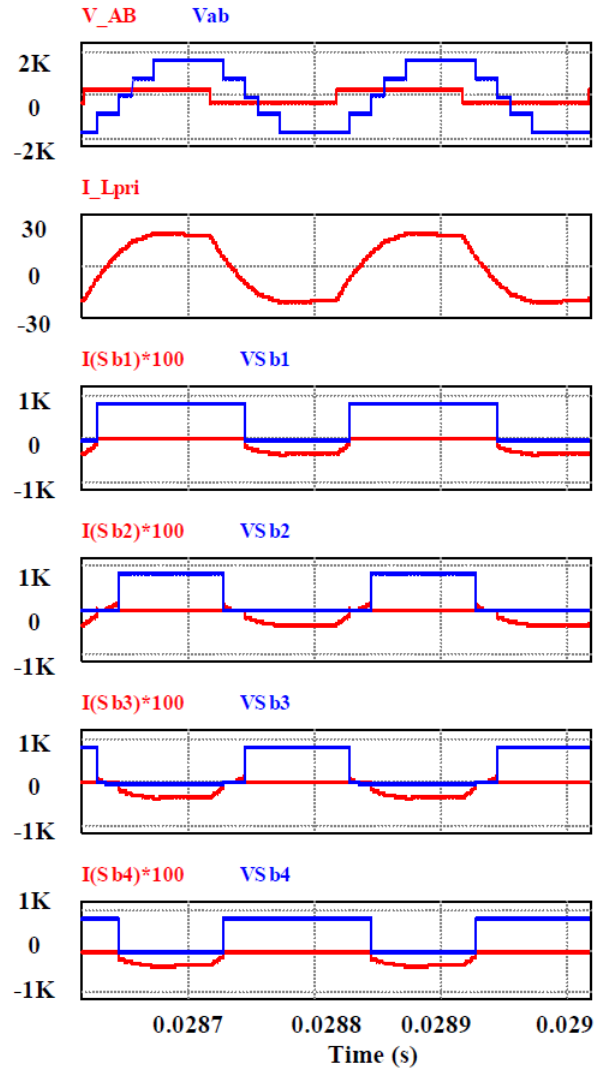


Fig. 3.14 Voltage across the transformer v_{AB} and v_{ab} , inductor current i_L and switch currents and voltages for S_{b1} to S_{b4}

3.2 Thermal Analysis

SiC switches are a potential candidate for high-current and high-voltage power electronic applications because they have improved performance and low conduction loss. The power loss estimation of SiC modules used in a HV high-power DAB DC-DC converter is presented in this chapter. Using derived mathematical models, the power loss calculation is explained. The analysis here was done with a 2L to 2L DAB converter. Chapter 5 includes the simulation results and the losses calculations and numbers for this research on a 3L - 2L DAB system.

3.2.1 Overview

A HV SiC module is used to achieve the optimum design of a DAB converter based on the consideration of the device and transformer characteristics. However, the high dv/dt of the SiC switches causes a huge spike and ringing in the currents during hard switching at high voltage levels. An optimization algorithm for non-active power loss minimization in the DAB DC-DC converter is discussed in research to improve the converter efficiency. Another work presents an advanced control strategy to reduce DAB converter losses. A survey of material-level developments in the key components of PWM power converters and the potential for improving system power density using advanced components is presented in another paper. Some literature indicates that a reduction of the switching by tenfold is achievable with the use of such advanced devices. Although wide band-gap devices have merits over Si devices, most have not been commercialized due to various reasons, such as the difficulty of mass-producing large-diameter SiC wafers, the difficulty of controlling the impurity level of these devices, and the high cost. Several parameters must be considered to select the correct power semiconductor device for any power electronic circuit. Device output characteristics, thermal characteristics, switching characteristics, blocking voltage, leakage current, and Safe Operating Area (SOA)

are all important factors concerning reliability. It is important to note that at any point of time during device operation, the maximum ratings specified in the device datasheet should not be exceeded. The gate charge characteristics and gate driver requirements of a power device and the associated driver circuit loss are also important factors to be considered when selecting an appropriate power device. The focus of this chapter is to estimate the conduction and switching power losses.

The converter has two H-bridge circuits interfaced via a high-frequency transformer. In addition to the device voltage and current handling capabilities and the power density, the anti-parallel diode's on-state voltage and soft recovery characteristics should be taken into consideration. The mathematical model of the device's current equations is presented below.

3.2.2 Loss Estimation of HV-side Devices

A power loss calculation for the converter's worst-case scenario for the chosen application should be done in order to choose the right device. Applying the worst-case operating scenario to the equations derived based on the mathematical model of the DAB converter results in the main component values of the converter. For the devices offered for a 20kHz switching frequency, a loss calculation is made. Fig. 3.15 shows the theoretical waveforms of the converter and the device currents.

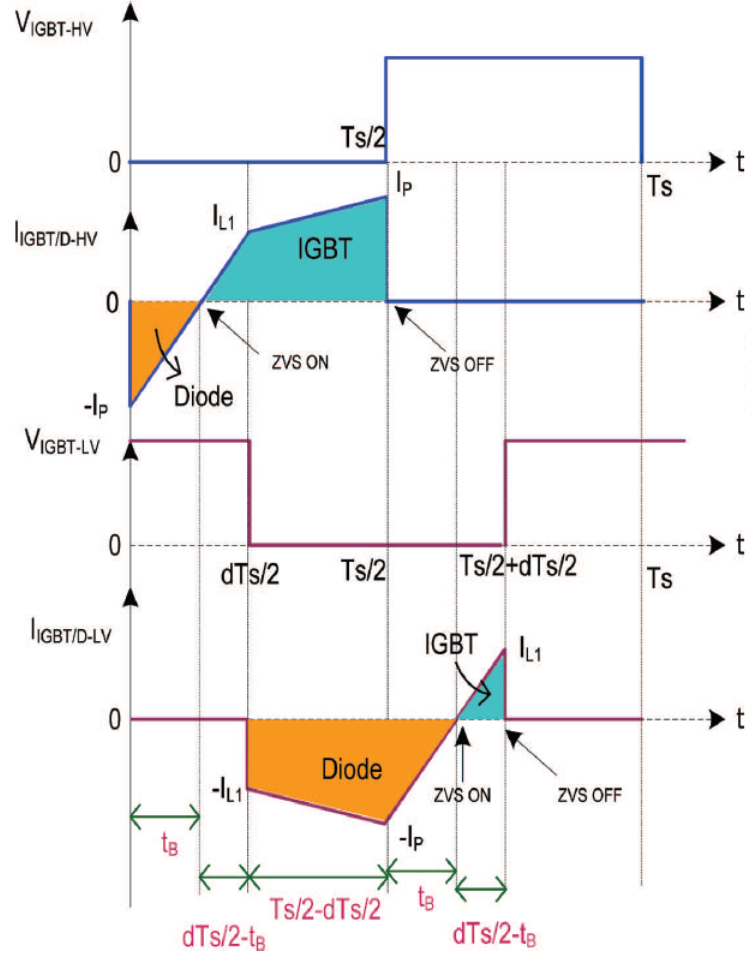


Fig. 3.15 Theoretical waveforms of devices on the HV side and LV side of the DAB DC-DC converter (Device conduction intervals are marked in pink)

Piece-wise linearity is assumed for the device's current waveforms. Hence, the average current flow through the switch on the HV side of the converter during the on-time is given by:

$$I_T = \frac{0.5I_{L1}\left(\frac{dT_s}{2} - t_B\right) + 0.5(I_{L1} + I_P)\left(\frac{T_s}{2} - \frac{dT_s}{2}\right)}{\frac{T_s}{2} - t_B} \quad (3.20)$$

The switch has a constant voltage drop during the on-state. Hence, the conduction loss can be calculated using the average switch current and the duty cycle, which is given as:

$$P_{CondT} = V_{CE(sat)}xI_Txd \quad (3.21)$$

The ratio of the transistor's on-period to its switching period is known as the duty cycle. The anti-parallel diode (V_F) and transistor ($V_{ce(sat)}$) forward voltage drops relative to the main terminals of the modules are described in the datasheet along with the voltage drops across the terminals. Because of the high power density of the devices, terminal losses cannot be disregarded in comparison to conductor losses. As a result, it's crucial to specify the voltage drop separately at the chip level and across the terminals (r_{CE}). The voltage drop across the terminals is given as:

$$V_{CE(sat)} = V_{CEO} + (r_{CE}xI_T) \quad (3.22)$$

The average diode current on the HV side of the converter during the on-state, as shown in Fig. 3.15, is given as:

$$I_D = 0.5xI_P \quad (3.23)$$

Since the diode conduction interval and base interval in (3.23) are equal on the HV side, the diode current can be calculated at any time. The diode's conduction losses are calculated as follows under the assumption of a constant voltage drop:

$$P_{CondD} = V_FxI_Dxd \quad (3.24)$$

On the HV side of the DAB converter, there are four transistors and four anti-parallel diodes. Consequently, the converter's HV side semiconductor devices' total conduction loss, P_C , is given as follows:

$$P_C = 4(P_{CondT} + P_{CondD}) \quad (3.25)$$

The turn-on (E_{ON}) and turn-off (E_{OFF}) energy loss curves, which are typically provided as a function of the module current at the switching instants of a switch, as provided in the manu-

facturer datasheet, are used to calculate switching losses. The diode always turns off with zero current in the DAB converter configuration under ZVS, eliminating the diode reverse recovery losses. As a result, the following are the power loss equations for the turn-on and turn-off instants:

$$P_{ON} = E_{ON}xf \quad (3.26)$$

and

$$P_{OFF} = E_{OFF}xf \quad (3.27)$$

where f is the switching frequency, P_{ON} is the power loss during the turn-on instant, and P_{OFF} is the power loss during the turn-off instant. The energy loss curves for turn-on and turn-off may not be present in some manufacturers' datasheets. In those circumstances, the simplified voltage and current waveforms must be taken into account when switching. During the rise-time and fall-time periods, switching losses predominate. The approximate loss equations for the turn-on and turn-off instants are as follows:

$$P_{ON} = 0.5xV_{CE}xI_Cxt_rxf \quad (3.28)$$

and

$$P_{OFF} = 0.5xV_{CE}xI_Cxt_fxf \quad (3.29)$$

The anti-parallel diode current is always transferred to the switches during DAB converter operation during ZVS. Therefore, it is possible to ignore the turn-on switching losses. As a result, the total switching losses (P_{SW}) are roughly as follows:

$$P_{SW} = 4xE_{OFF}xf \quad (3.30)$$

The junction temperature of the devices is calculated as:

$$T_{jIGBT} = T_s + (P_T x R_{th(c-s)}) + (P_{IGBT} x R_{th(j-c)}) \quad (3.31)$$

and

$$T_{jDiode} = T_s + (P_T x R_{th(c-s)}) + (P_{Diode} x R_{th(j-c)}) \quad (3.32)$$

where P_T is the total power loss of the switch module and T_s is the temperature of the heat sink. The device datasheet contains the case to sink ($R_{th(c-s)}$) and junction ($R_{th(j-c)}$) thermal resistances. By comparing the power losses of devices from various manufacturer studies, the power losses of switches and anti-parallel diodes are predicted for the worst-case operating condition and are shown in Fig. 3.16. Due to the high switching frequency and high turn-off current, the switches suffer significant switching power losses, which significantly contribute to the overall power loss, as shown in Fig. 3.16.

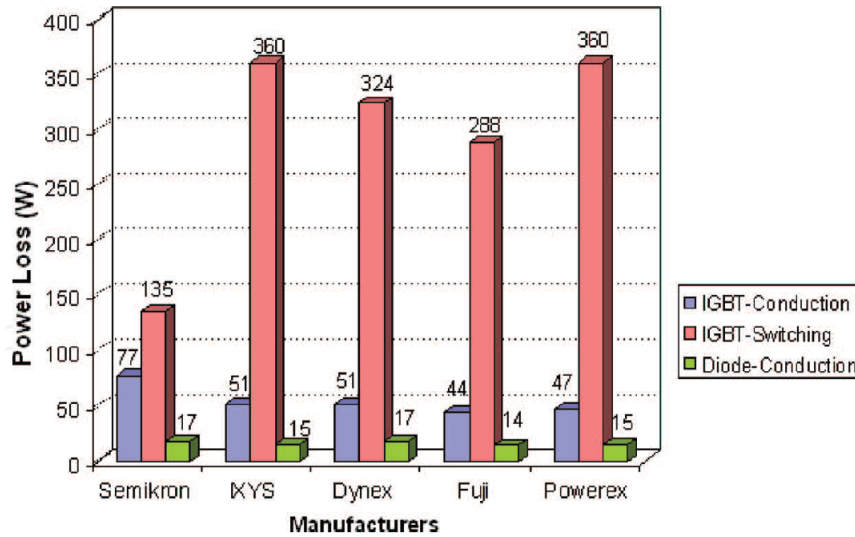


Fig. 3.16 HV-side switch and anti-parallel diode power loss comparison for various manufacturers

3.2.3 Loss Estimation of LV-side Devices

A method similar to that described in the previous section is used to predict the power loss of LV-side devices. The primary distinction is that, as shown in Fig. 3.15, the phase shift introduced between the HV- and LV-side bridges causes the shape of the LV-side device currents to differ from those of the HV-side devices. The equations for transistor and diode current in the on-state are:

$$I_T = \frac{0.5xI_{L1}x(\frac{dT_S}{2} - t_B)}{(\frac{dT_S}{2} - t_B)} \quad (3.33)$$

and

$$I_D = \frac{0.5(I_Pxt_B) + 0.5(I_{L1} + I_P)x(\frac{T_S}{2} - \frac{dT_S}{2})}{(\frac{T_S}{2} - \frac{dT_S}{2} + t_B)} \quad (3.34)$$

3.2.4 Converter Cooling System Design

The chosen power converter's cooling system makes use of liquid cooling which was implemented in this design. The design stage went through a few iterations, each of which was predicated on a different combination of materials for the cold plate, as well as a different shape and size for the channels. On the primary side, the power converter consists of six different devices, where each one of them is a half bridge SiC MOSFET module rated for 10kV. For an increased power density level, a double-sided cold plate has been chosen. This helped in placing three modules on each of its two faces. Each layer of this 10kV SiC MOSFET module is constructed using a unique material that possesses a unique set of properties, such as thermal conductivity and density. The exact layers dimensions, dies, and chips placements have been drawn and designed carefully for proper and accurate utilization in Ansys Fluent FEA simulation Fig.3.17.

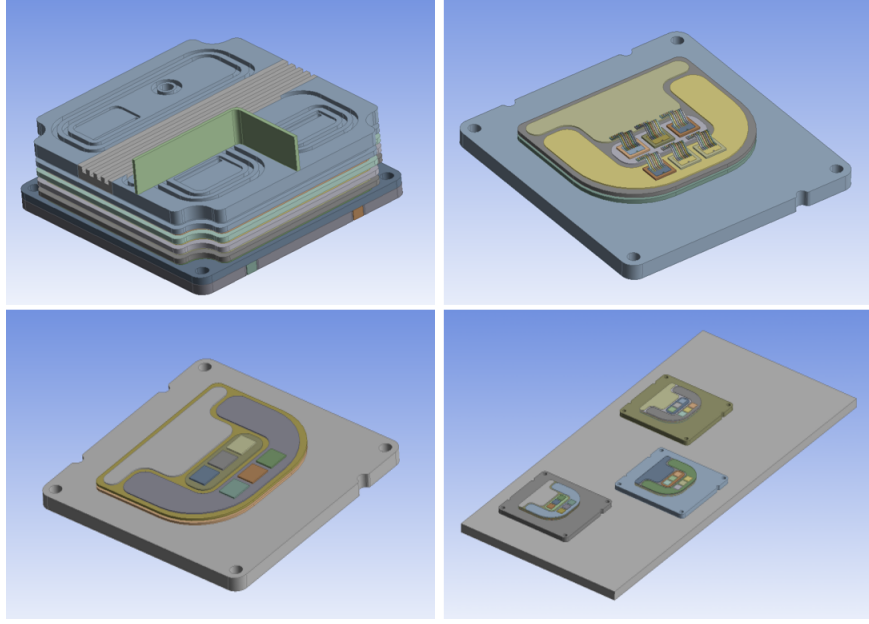


Fig. 3.17 SiC power modules and designed cold-plate

Each switch has 3 dies in parallel, so that the SiC MOSFET module consists of 6 dies of which each dissipates heat because of the switching and conduction nature. Simulation of a 3L ANPC to 2L DAB is carried out using Simulink. The RMS current through each switch and anti-parallel diode is measured for calculating the conduction and switching losses Fig. 3.18.

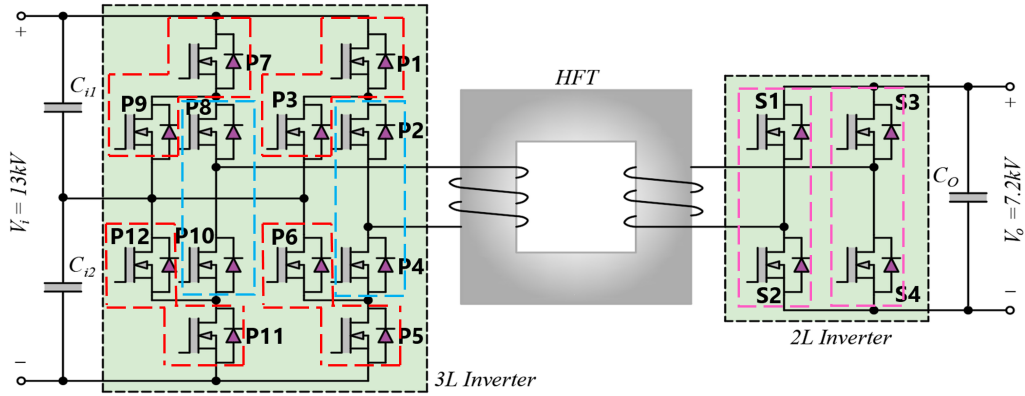


Fig. 3.18 SiC MOSFET half-bridges configuration to create ANPC-2L converter

Using the aforementioned formulations and the fact that $R_{DS,ON} = 0.65\Omega$ at 125C is used for calculating conduction losses and extracting switching loss energy at various current levels, the switching and conduction losses associated with each switch can be determined. The fol-

lowing equation (3.35) provides a sample calculation example for $P1$ and $P7$, and the results are tabulated in Table (3.2):

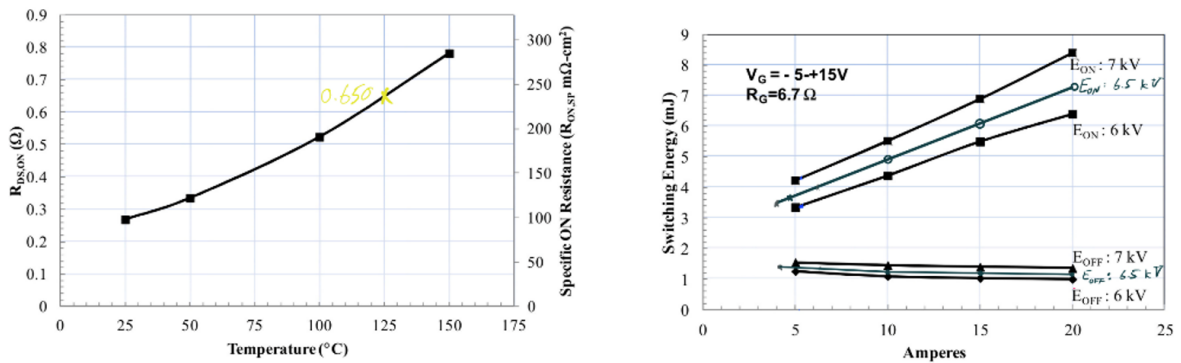


Fig. 3.19 Module $R_{DS,ON} = 0.65\Omega$ and switching energy plots

$$i_{P1} = i_{P7} = 10.5A$$

$$P_{cond} = 0.65\left(\frac{10.5}{3}\right)^2 = 8W$$

$$P_{sw} = (3.3 + 1.4)20 = 94W \quad (3.35)$$

$$P_{loss,P1,die} = 8 + 94 = 102W$$

$$P_{loss-P1,total} = 102 * 3 = 306W$$

Table 3.2 Calculated conduction and switching losses

Switch Pair	Current (A)	P _{cond} (W)	P _{sw} (W)	P _{loss-die} (W)	P _{loss-total} (W)
P1,P7	10.5	8	94	102	306
P2,P8	13.5	13.16	94	107.16	321.48
P3,P9	3.5	0.88	84	84.88	254.64
P4,P10	7.5	4.1	87	91.1	273.3
P5,P11	6	2.6	87	89.6	268.8
P6,P12	1.5	0.16	85	85.16	255.48
S1,S3	31	69.4	142	211.4	634.2
S2,S4	14.5	15.18	112	127.18	381.54

After that, these losses numbers are plugged into the thermal cooling design stage. The design began with aluminum as a cold plate material; however, due to its poor thermal con-

ductivity, the design material was switched to stainless steel, and finally to copper. Initially, our cooling system had semicircle-shaped channels. However, it was discovered after several simulation iterations that switching to rectangular micro channels for the cooling system would result in improved overall performance.

For the primary side cold plate, the first set of simulations uses copper as the cold plate material. The cold plate measures 500 millimeters by 220 millimeters by 20 millimeters and has three channels measuring 5 millimeters by 8 millimeters on each side. The inlets and outlets of the top and bottom channels must be on opposite sides of each other Fig.3.20.

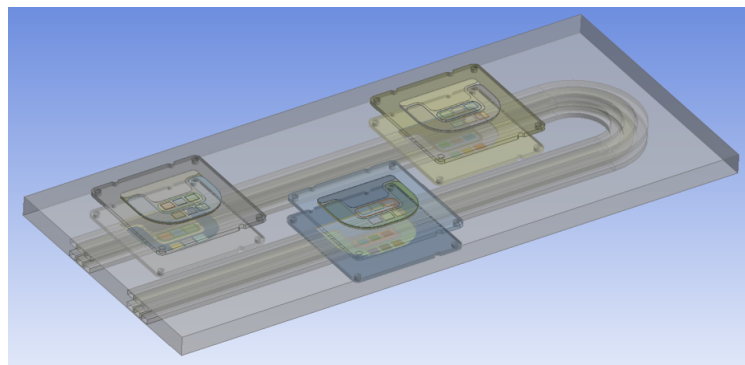


Fig. 3.20 Primary double sided cold plate

The model was then given a fine mesh texture. As can be seen in Fig. 3.21 below, the orthogonal and skewness quality of the mesh, which are two important factors that contribute to having a good mesh, have satisfactory numbers.

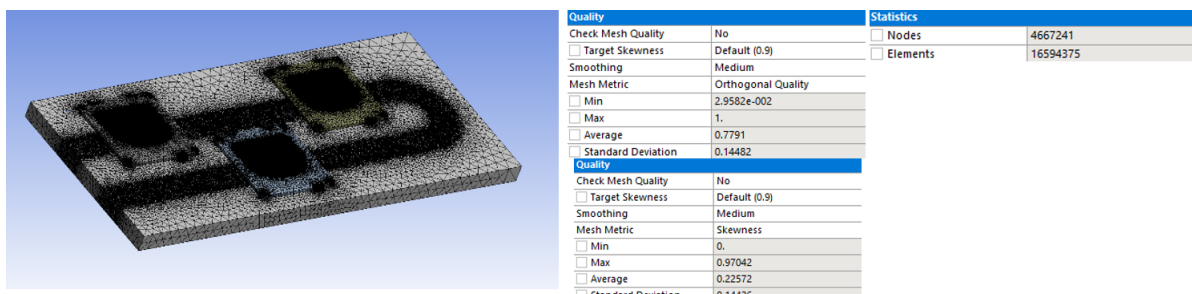


Fig. 3.21 FEA meshing texture

Once the proper mesh has been applied, the FEA simulation is carried out. The coolant,

de-ionized water, was given an input temperature of 20 and an input velocity of 0.5 meters per second. The goal is to keep the chips at around 120C. Because of the cooling system that we designed, the highest temperature that was experienced is in the neighborhood of 109C, which is ideal for proper operation and module utilization (Fig. 3.22).

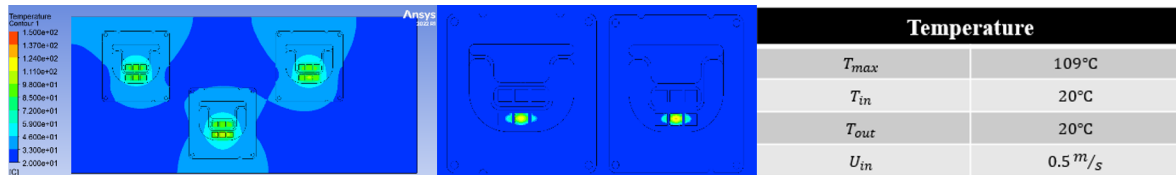


Fig. 3.22 First iteration temperature distribution

However, there is a significant challenge to overcome: the weight of the cold plate. This model's cold plate weighs 19.7kg, which is significantly more than what can be managed. As a result, a second design iteration was created to reduce the thickness of the cold plate, resulting in a decrease in overall weight. However, before showing the results of that modification, it is useful to see below the effect of two different materials when used as a cold plate.

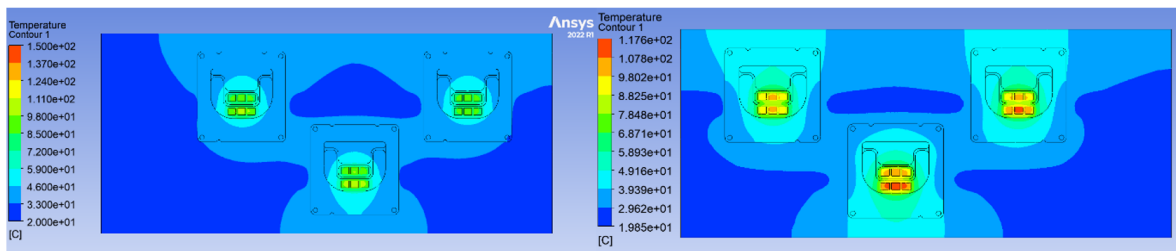


Fig. 3.23 Copper vs. Aluminum cold material material temperature comparison

In reference to Fig. 3.23, copper is depicted on the left side of the figure, while aluminum is depicted on the right hand side. As a result of aluminum's lower thermal conductivity than copper, the temperature has risen by 8C. Because the cold plate's thickness was reduced, its weight was dropped down to 7.9kg, and the temperature was raised to 120C, which is still within acceptable limits. In this simulation, the coolant entered the system at a velocity of 0.5

meters per second. The top of the cold plate is depicted on the left side in Fig. 3.24, while the bottom is depicted on the right. The two figures at the bottom show the middle modules, which have the highest level of loss, as expected.

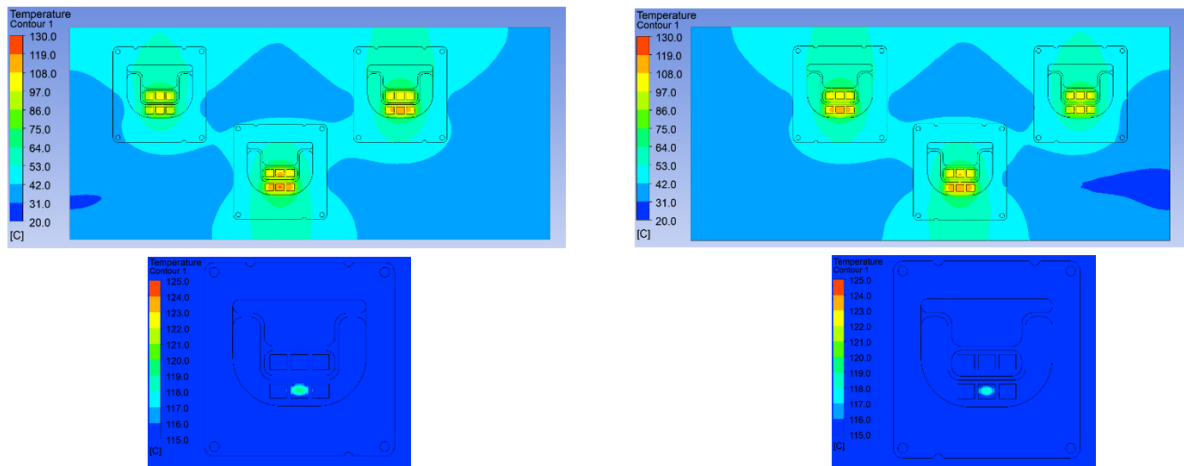


Fig. 3.24 Reduced copper cold plate thickness temperature distribution

This temperature is within the module's comfort range and corresponds to the one that is required. It is therefore suitable to reduce the weight of the cold plate by cutting the free spaces that are unused for thermal expansion on it. Therefore, the cold plate evolved into the form in Fig. 3.25. The cold plate in this model has dimensions of 480 by 190 by 8 millimeters and weighs 3.03kgs. All the parameters of the de-ionized water coolant (temperature, velocity, and pressure) is exactly the same as it was in the previous model.

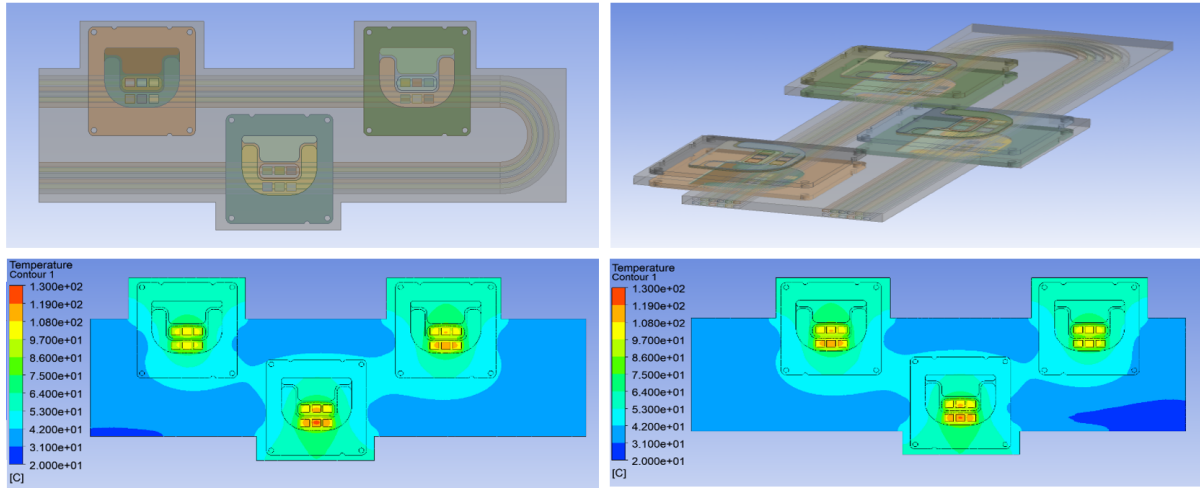


Fig. 3.25 Primary double-sided cold plate

As for the secondary side cold plate, two modules are used for the 2L H-bridge. As calculated in Table 3.3, the losses are significantly higher than on the primary side; as a result, the temperature is expected to be higher. The two modules are initially positioned on opposite sides of the cold plate and used various channel configurations Fig. 3.26; for example, the inlet and outlet are placed on opposite sides of the cold plate; nevertheless, couple of iterations showed having both modules on the same side leads to better results. The cold plate in this model measured 200 mm by 115 mm by 8 mm were six channels on each side, and each measuring 2 by 4. This was the first iteration of the secondary side's primary version. The temperature at the inlet was 20 degrees Celsius, and the velocity was 0.5 meters per second.

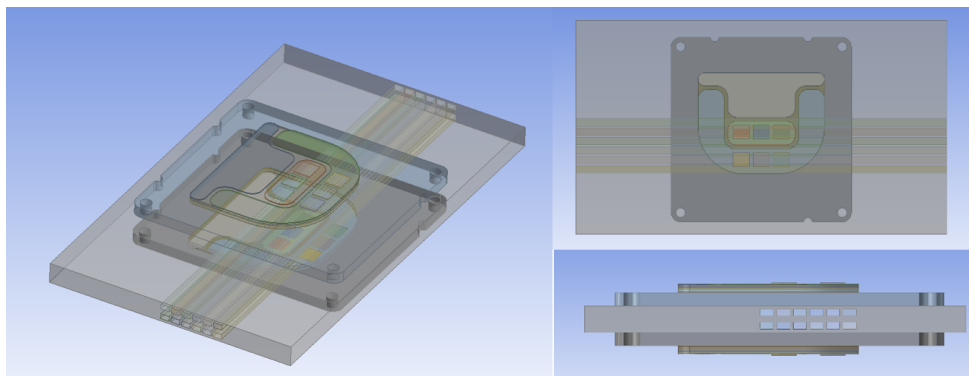


Fig. 3.26 1st iteration: secondary double-sided cold plate

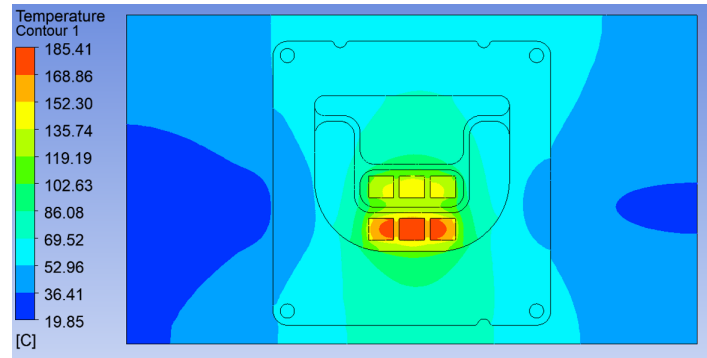


Fig. 3.27 1st iteration: secondary double-sided cold plate temperature distribution

After running a few simulations on cold plates with both sides, it was decided to switch to using single-sided cold plates instead of double-sided ones (Fig. 3.28). Again, for this model, the cold plate has two layers of channels, with six channels in each layer. Furthermore, the cold plate measures 330 millimeters long by 205 millimeters wide by 8 millimeters high. The inlet velocity was increased to 1.4 meters per second for the purposes of this simulation. The device's temperature dropped to 135C (Fig. 3.29), but efforts are still going on to get it down to 120 degrees Celsius, which is the ultimate goal for both the primary and secondary sides of our system.

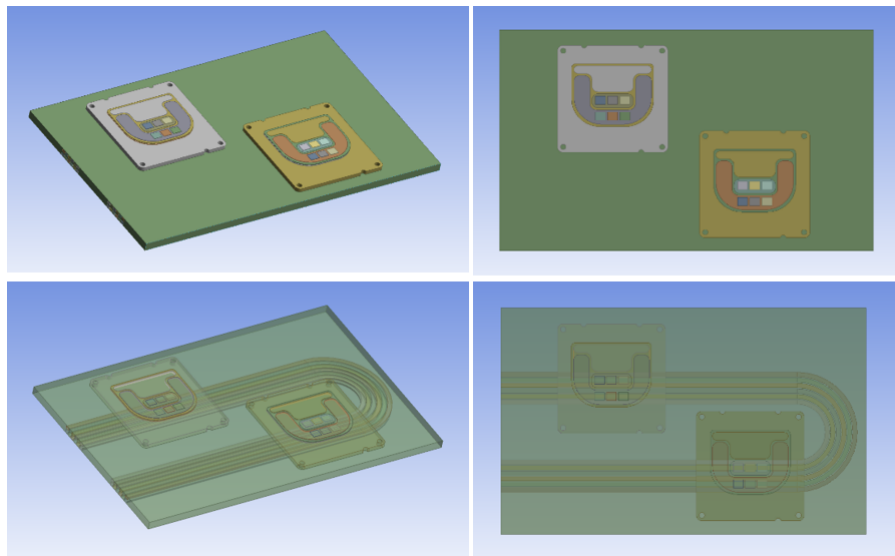


Fig. 3.28 Secondary side single-sided cold plate

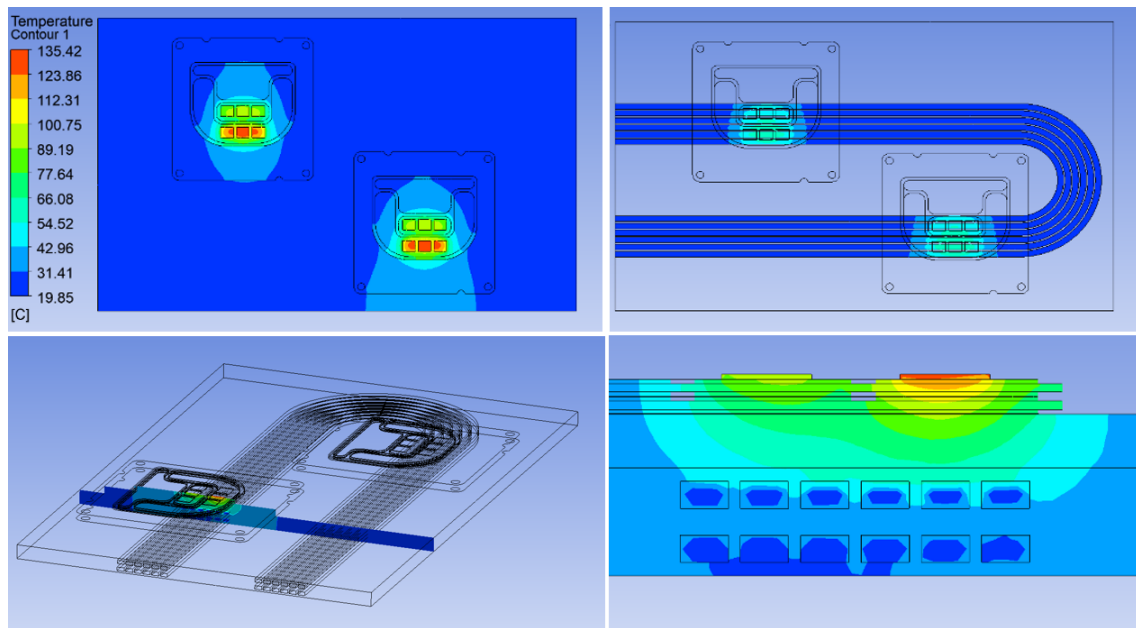


Fig. 3.29 Secondary side single-sided cold plate

3.3 HV SiC Power Module

Si-based MOSFETs have high on-resistance and output capacitance, which result in high conduction and switching losses in high voltage level applications. IGBT can achieve this voltage level, but because of the trailing current effect, it reduces switching frequency and power density. Thus, this application does not suit the silicon-based power semiconductors. In comparison to Si devices, the SiC-based MOSFET has better thermal characteristics and has lower on-resistance, higher withstand voltage, and lower switching loss [79].

3.3.1 Semiconductor Switches

Due to the MW, kV, and kHz ranges of the considered SSTs, the current semiconductor technologies, e.g., IGBTs, Integrated Gate-Commutated Thyristors (IGCT), and emitter turn-off thyristors should undergo a revolutionary phase to be able to handle these high voltages and current stresses as a single device. This seems to be very unlikely in the immediate future. Within this scope, one of the most significant concerns is the rating of power devices. One possible solution is to consider the newly developed wide-bandgap materials, i.e., SiC material which has the potential to be the basis for the next generation of ultra-HV devices. Researchers have recently focused on the characterization of these devices, particularly the 10kV/10A SiC MOSFETs and the 15kV/20A SiC IGBTs. The overall investigation indicates that in future high-power electronics, SiC MOSFETs and IGBTs will be natural choices at voltage levels below 20kV, whereas for higher voltage levels SiC Gate Turn-off Thyristor (GTO) or thyristors are likely to be used. Although SiC devices are likely to improve over time, Cree Inc. recently manufactured 15kV/10A SiC MOSFETs, but they are still far from commercial availability. They have a long way to go before they are competitive with silicon devices. Therefore, they should only be viewed as a possible future solution. Series connection of LV devices, Fig.

3.30, might be another solution to achieve higher blocking voltages, however, voltage balancing during the dynamic transient is a challenge dictating lower switching frequencies. Extra snubber circuits are also necessary for this solution. Besides modularity at the device level (series connection of LV devices), modularity at the converter level is another factor for voltage scalability (Fig. 3.30)(b). This can be achieved by making series or parallel connections of converter modules as building blocks in MV or LV DC links or even on the AC side of the SST when a multi-stage conversion system is considered. Each power cell in this topology requires an MFT which should handle the entire voltage of the MV DC link [8].

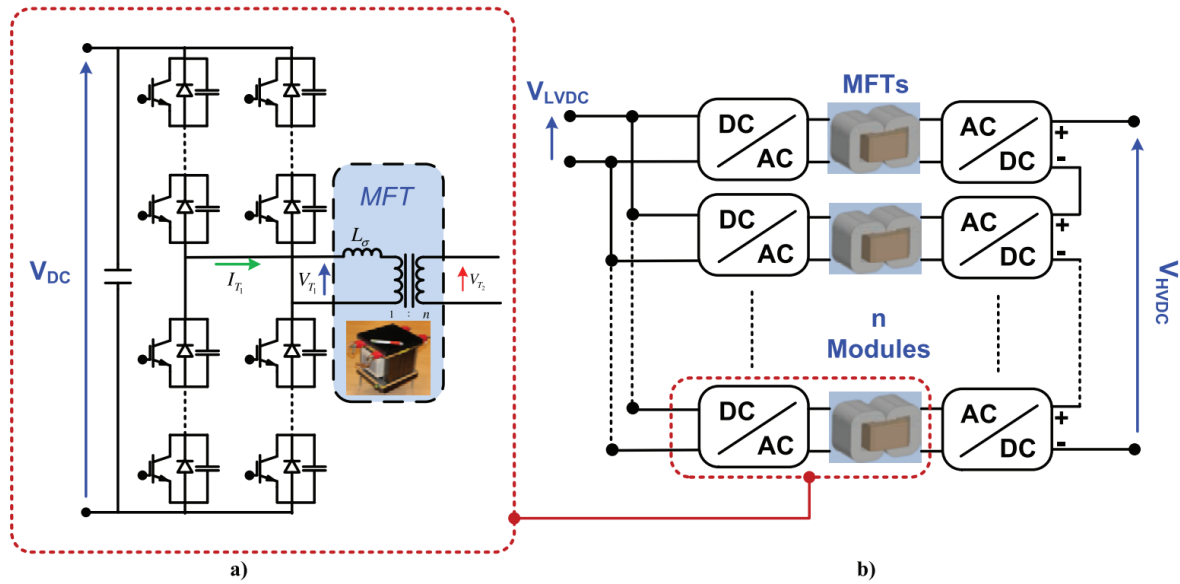


Fig. 3.30 (a) Modularity from device-level (b) modularity from converter level as series/parallel connections of building blocks

The application of SiC MOSFETs with enhanced breakdown voltages from MV (3.3kV, 6.5kV) to HV (10kV, 15kV) in high-power systems is anticipated. These include high-speed traction systems, electric ship power conversion, SSTs, high voltage circuit breakers, and renewable energy generation systems capable of generating megawatts of electricity. A SiC device exhibits a 10 times higher breakdown voltage and 40 times higher switching frequency (0.5kHz to 100kHz) than the Si counterpart. To achieve a high power density, higher switch-

ing frequencies reduce bulk passive components, thus reducing the complexity of HV power systems by avoiding multiple devices in series, thus reducing power system complexity. For high-voltage SiC devices used in high-voltage applications, there is a significant problem with the packaging. To fully exploit the capabilities of high-voltage module packages, it is necessary to balance the insulation distances necessary with the full realization of their capabilities. On the one hand, the fast switching speed (e.g., 100V/ns for HV SiC compared to 3V/ns for HV Si) offered by HV SiC devices is limited by module packaging parasitics. On the other hand, the module terminal-to-terminal distance plays an important role in determining the parasitic inductance and parasitic capacitance, which is crucial to the SOA, Common Mode (CM) current, and EMI issues. As a result, module terminal layout, or module-system interface, plays an important role in determining the performance, reliability, and efficiency of a HV system. It is generally possible to avoid breakdown at the terminal-busbar interface by increasing the insulation distance between terminals of different potentials, which will introduce parasitics and increase footprint. In addition to utilizing high dielectric materials to withstand high electric field strengths, there is also the use of high dielectric material. To avoid the terminal-busbar interface in the IIT power module, Virginia Tech used FR4 as a dielectric material. To achieve both insulation and thermal management, APEI developed a compact packaging technique immersed in a dielectric liquid. In addition, this SiC power module can withstand up to 24kV/30A and 200C. In industrial applications, however, it is always a challenge to ensure that both liquid and solid insulations are adequately degassed. To ensure safe operation and power efficiency, HV module packaging has been designed with terminal configurations in mind. The following terminal layout is designed to meet the high insulation requirements and minimize parasitics for 10kV power module packaging. This study examines the relationships between parasitics and voltage levels at voltages ranging from 600V to 10,000V. As a result of the comparison

of three standard terminal arrangements and their associated system-level parameters, a typical HV power module terminal layout is recommended for laminated busbar applications. In the third section, the concept of arranging the terminals into electric potential groups to minimize parasitics is proposed and an optimized internal layout with EMI control is provided.

3.3.2 Module Parasitics

HV modules require accurate clearance and creepage distance calculations. Insulation distances greatly exceed the dimensions of the assembled components and determine the footprint based on their insulation distances. Two of the most significant insulation requirements for grid-supplied circuits are functional insulation within the circuit and basic insulation between the grid-supplied circuit and the earth. Fig. 3.31 illustrates the parasitic inductance and insulation requirements for different voltage ratings based on a typical module packaging architecture. Although clearances and creepage distances are proportionate to rated voltages, parasitic inductance depends on voltages differently. Due to the chips' dimensions, parasitic inductance is almost constant for power modules rated from 600 to 3,300 volts. For 3,300V to 10,000V, the parasitic inductance increases linearly with insulation distance as the insulation requirements begin to drive the overall footprint of the module. According to Fig. 3.32, parasitic capacitance is unlikely to be significantly correlated with voltage rating, even though parasitic capacitance is supposed to depend on insulation similarly to inductance.

Overvoltage category 3, pollution degree 2

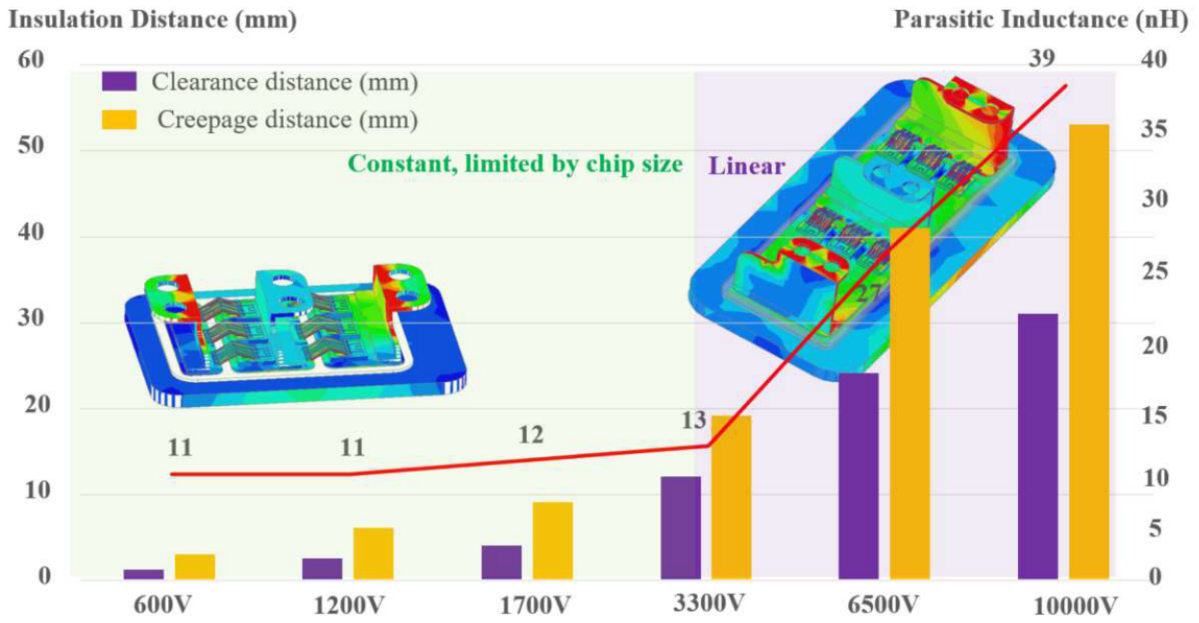


Fig. 3.31 Insulation distance and parasitic inductance at typical voltage levels

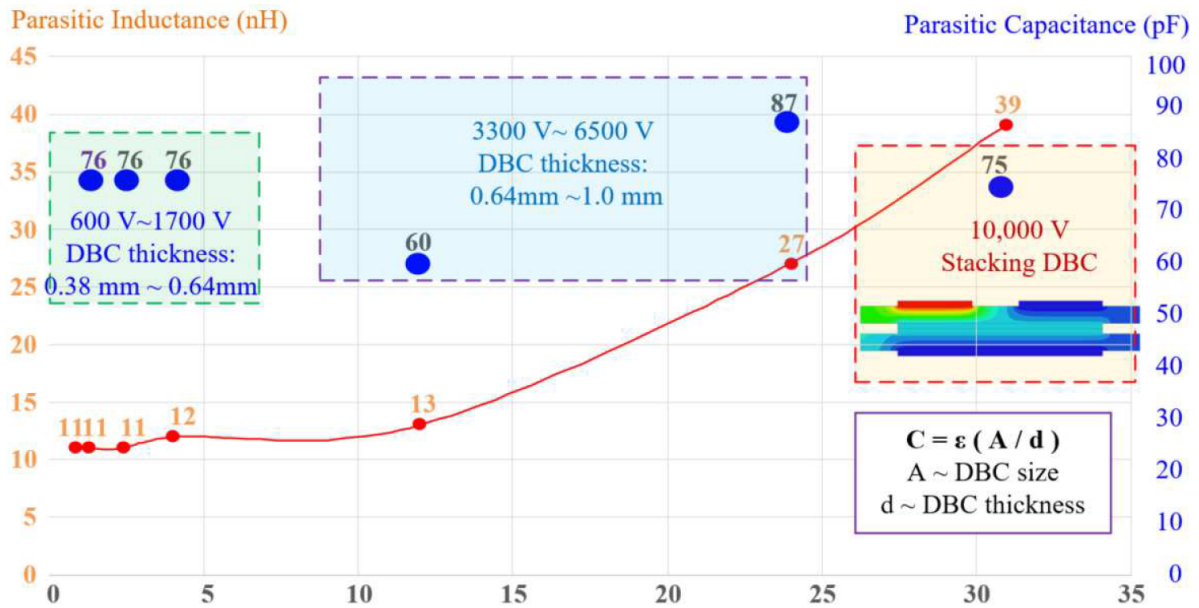


Fig. 3.32 Parasitic inductance and parasitic capacitance at typical insulation distance

LV ratings require a thin Direct Bonded Copper (DBC) substrate (0.38mm or 0.64mm) for lower thermal resistance because capacitance is determined by both area of overlap between the two metal plates and the thickness of the dielectric layer. To ensure basic insulation for

3,300V and 6,500V power modules, a larger ceramic thickness is required. Considering that the 10,000V power module is supposed to possess a parasitic capacitance of about half of its stated size, it is noteworthy to note that this is not the case. The fact that stacked DBC substrates, which act as two capacitors in series, can be used to increase the partial discharge inception voltage. The reason for this is that the partial discharge inception voltage can be increased. For the HV module to satisfy insulation requirements and ensure low parasitics, optimizing the packaging architecture is crucial. An outline of the insulation distance and parasitics of each type of insulation is presented in Table 3.3 by IEC 60664-1 and IEC61800-5.

Table 3.3 Insulation Distance and Parasitic Distance at Typical Voltage Level

Insulation	Functional insulation		Basic insulation		Parasitics	
Definition	Within a circuit e.g. from phase to DC		between earth and the power circuit e.g. input terminals, output terminals		-	
Determining factor	Recurring peak of the working voltage. (worst case: semiconductor blocking voltage)		Impulse voltage (determined by system voltage & overvoltage category.		-	
Voltage level	Clearance distance	Creepage distance	Clearance distance	Creepage distance	Parasitic inductance	Parasitic capacitance
600 V/650 V	0.8 mm	3.1 mm	1.2 mm	3 mm	11 nH	75 pF
1,200 V	0.8 mm	6.1 mm	2.4 mm	6 mm	11 nH	75 pF
1,700 V	1.7 mm	8.5 mm	4 mm	9 mm	12 nH	76 pF
3,300 V	4.6 mm	16.5 mm	12 mm	19 mm	13nH	60 pF
6,500 V	12 mm	33 mm	24 mm	41 mm	27 nH	87 pF
10,000 V	21 mm	50mm	31mm	53mm	39 nH	75 pF

3.3.3 Layout and System Interface

The module architecture itself is one aspect of the power system that is significant, but the module's system interface structure is also an influential factor in determining its performance. As shown in Fig. 3.33, three typical terminal arrangements as well as the corresponding system interface are co-designed. As shown in Fig. 3.34, the parasitic inductances of each module are compared. While layout (a) has positive and negative DC terminals at the same end, the extra insulation distance or insulation rings required between the two laminated busbar layers results in a narrow current conduction section due to the extra insulation distance or insulation rings.

As with layout (b), this layout has both positive and negative DC terminals. As shown in Fig. 3.34, layout (b) requires a busbar structure that is even more complex, which results in nearly twice the parasitics as the other layouts. The busbar structure in layout (c) without an insulation ring is relatively simple. The insulation between the terminals is addressed by an insulation wall or creepage extender on the housing. As shown in Fig 3.34, layout (c) also achieves the lowest parasitic inductance of 13nH with the largest insulation distance of 40mm.

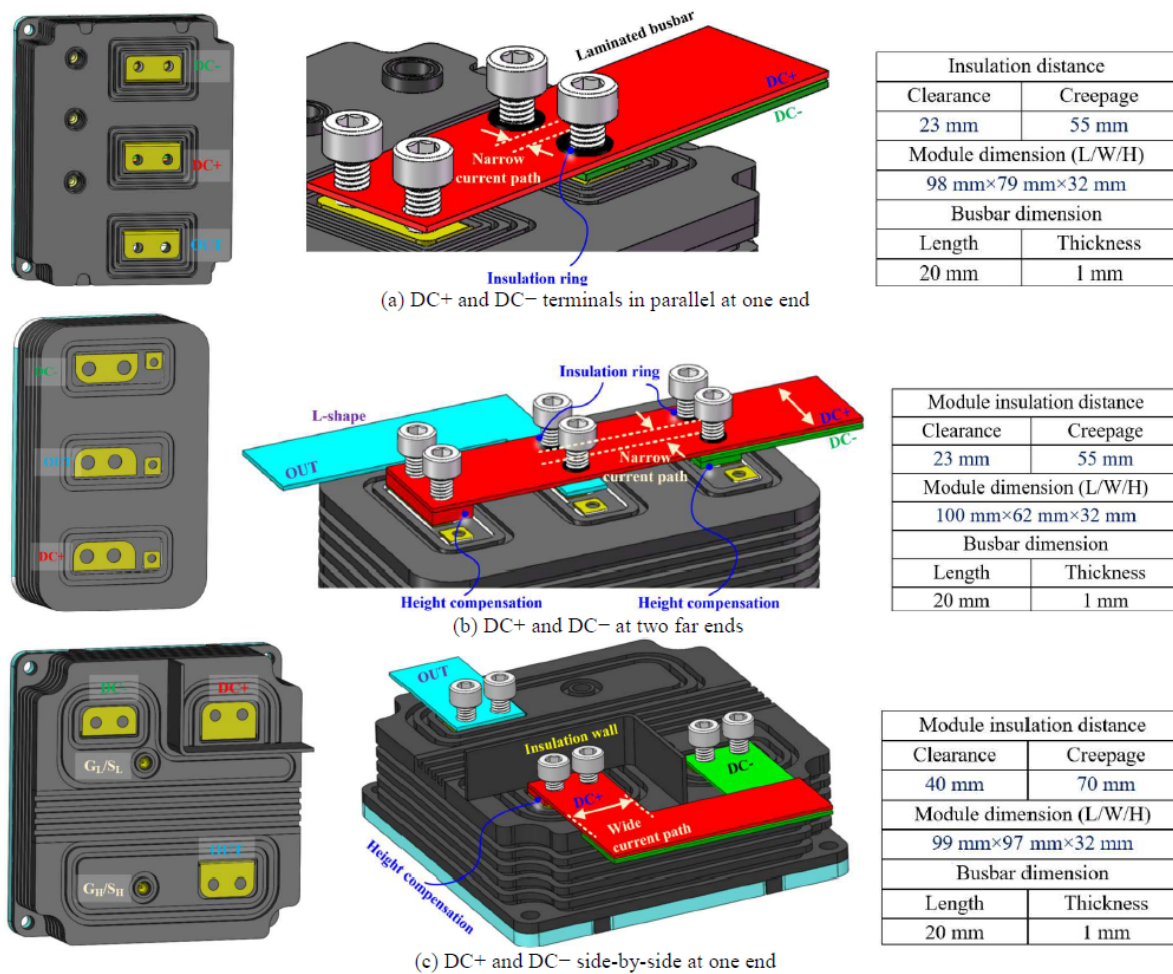


Fig. 3.33 Typical layouts and the busbar arrangements

In practical applications, the power electric performance is determined by both the internal inductance of the module as well as the external inductance of the busbar. These busbars are uniformly set to a length of 50mm, exceeding the edge of the modules. Although the parasitic inductance of busbars in layouts (a) and (c) is almost the same, layout (c) has a clearance

distance of 40mm, compared with layout (a) with 23mm. Despite having the simplest internal layout of the modules, layout (b) has the most complex busbar structure and the largest parasitic inductance.

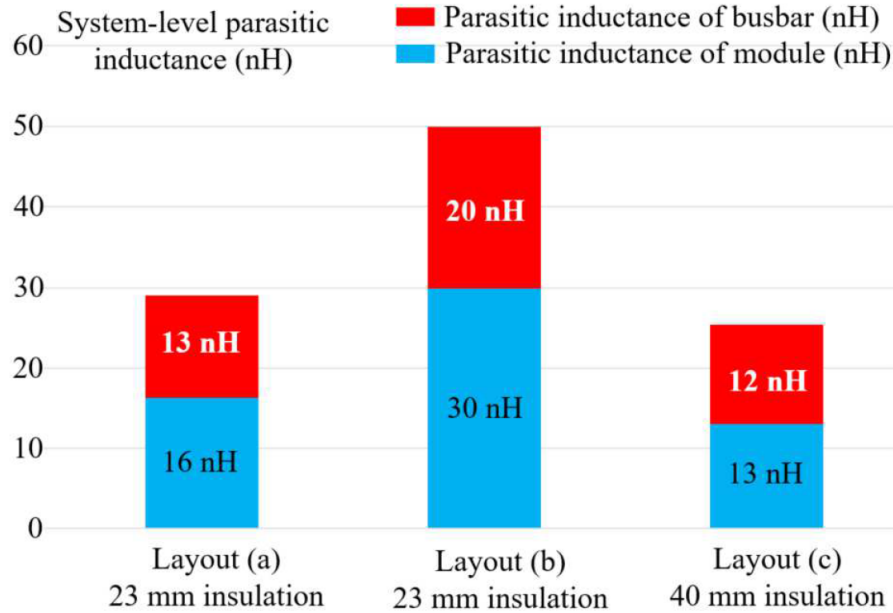


Fig. 3.34 Parasitic inductance of typical layouts with 50mm laminated busbar

3.3.4 Terminal Arrangement

A concept of organizing power module terminals according to electrical potential is illustrated in Fig. 3.35 to achieve the desired results of high insulation and low parasitics. In addition to positive DC and high-side connection terminals, there are AC OUT terminals and high-side control terminals. In addition, there are negative DC terminals and low-side control terminals. In the proposed electric potential-oriented terminal arrangement, only two functional insulation distances ($2 \times 23\text{mm}$) are required between the three groups of terminals.

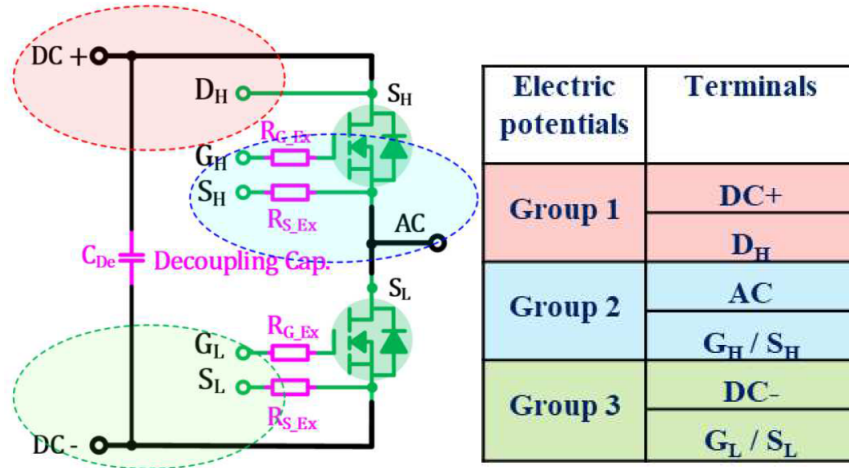


Fig. 3.35 Electric potentials groups in a half-bridge topology

Furthermore, parasitic capacitance contributes significantly to the common mode current, electric field distribution, and EMI issues associated with high voltage power modules, along with induced inductance. Fig. 3.36 demonstrates the two methods used to optimize parasitic capacitance. One method uses shield materials with a low relative dielectric permittivity, while the other uses a negative DC shield trace. As opposed to AlN with a dielectric permittivity of 9.0, FR4 with a relative dielectric permittivity of 4.4 covered half of the AC trace. The FR4 layer is attached to the negative DC trace, shielding half of the AC trace from parasitic capacitance, thereby reducing parasitic capacitance and obtaining an electric potential-oriented terminal arrangement. To improve the overall performance of the high-voltage power electric system, a comprehensive module-system optimization was performed to minimize parasitics and guarantee sufficient insulation capability. The parasitic and system interface of three typical module layouts, which are positive and negative DC terminals in parallel, at two far ends and side-by-side. These layouts are compared and analyzed. The side-by-side terminal structure with an insulation wall is analyzed and demonstrated to be the most promising structure, which has a minimized parasitics of 13nH and an attractive busbar interface. Moreover, the concept of an electric-potential-oriented terminal arrangement is proposed to provide a compact module

layout with sufficient insulation. Thus, the traditional wire bond-based power module can achieve low parasitics with up to 40mm insulation distance [81].

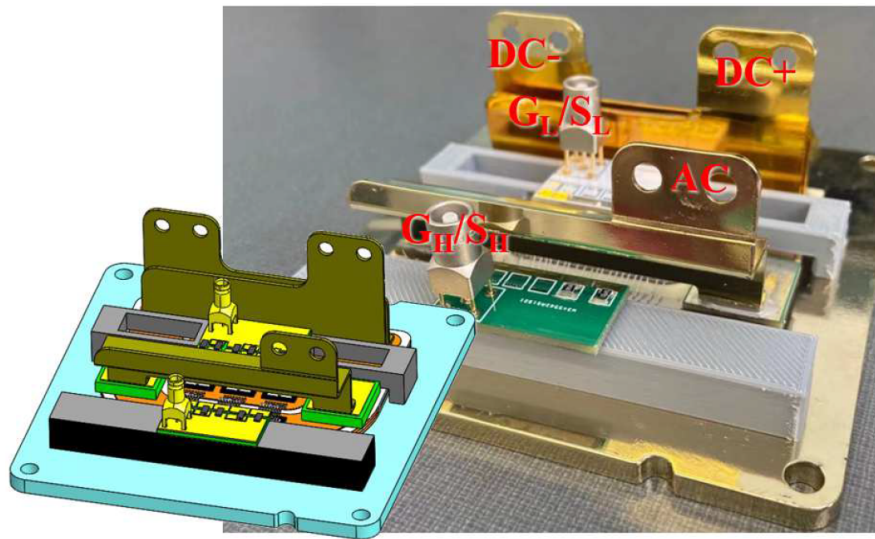


Fig. 3.36 Module inner layout for layout (c)

3.4 Insulation Coordination

This study examines the insulation coordination of three isolated DC/DC converter modules included in the MF 3L-2L DC/DC converter structure. Each DC/DC converter is supplied with its input voltage by a single-phase AC/DC active-front-end converter connected to the three-phase 13.8kVac grid supply. All the DC/DC converter modules receive their input voltages from single-phase active-front-end rectifiers rated at 13kVdc, while their output voltages are 7.2kVdc. To provide the required voltage level for three-phase 4.16kVac voltage-level inverters, three DC/DC converter modules are connected in parallel. The converter structure is illustrated in Fig. 3.37. The minimum clearance and creepage distances vary according to the operating frequency. This study utilizes a switching frequency of 20kHz, which falls below the 30kHz limit when determining creepage and clearance distances. For higher frequencies, it is recommended to adhere to IEC-61800-5-1.

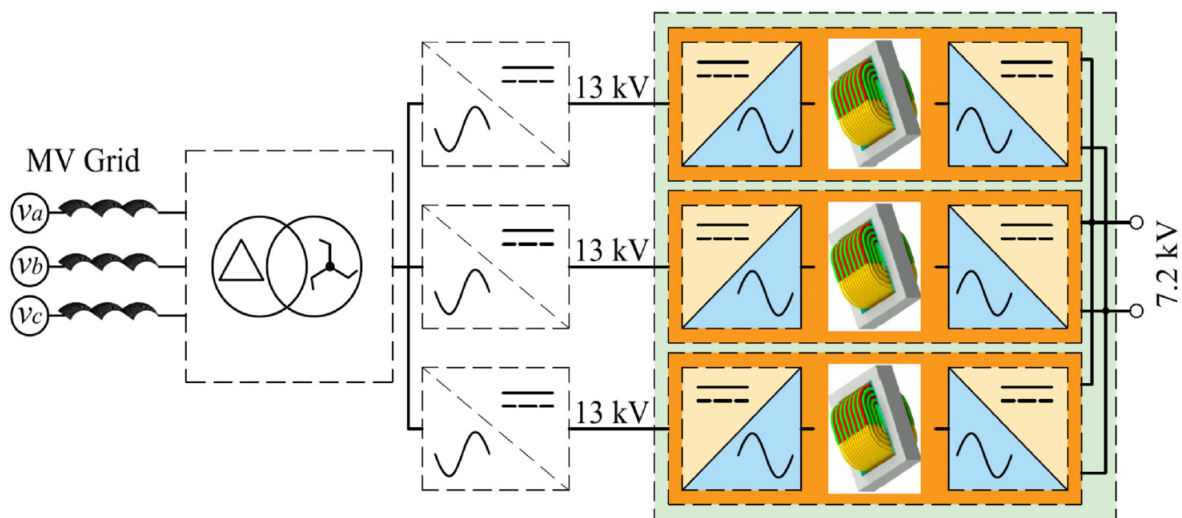


Fig. 3.37 Converter Structure

A limited number of standards exist for power electronics converters over 1.5kV. Previously, MV adjustable motor drivers were the most common use of MV power electronics. However, as distributed generation applications and solid-state transformers become increasingly avail-

able, this status is changing, especially after high-frequency MV wide-bandgap devices become increasingly available. Despite the necessity for establishing proper standards directly describing MV converters, existing standards must be adapted for such applications until appropriate standards are approved. For this reason, this case study utilizes the IEC-61800-5-1 standard. By using the Basic Insulation and Reinforced Insulation rules to convert lower-rated building blocks into system-compatible building blocks, IEC 618500-5-1 aims to build up an entire system.

Initially, some characterization is required to determine the minimal creepage and clearance distances. The first parameter that needs to be determined is the Over Voltage Category (OVC) that defines the impulse voltage level required to determine the clearance distance. Some converters are sufficient with OVC-I when there is no direct connection to the converter, as stated in IEC-61800-5-1. According to the same standard, under the heading "Insulation to the Surroundings", OVC definitions are classified from OVC-II to OVC-IV, depending on parameters such as whether the device is connected directly to the supply mains or directly to the source of the installation's supply mains and the type of connection used. Due to the high power level of the converters examined in this study, they cannot be wired to a plug owing to their supply by another converter. IEC-61800-5-1 provides definitions of "Basic insulation evaluation for circuits connected directly to the supply mains" under the heading "Insulation to the Surroundings." Circuits and parts affected by external voltage transients (in this case inverter parts such as SiC devices, capacitors, etc.) should be categorized as functionally isolated as OVC-II. Even though this standard states that OVC-III can be applied as OVC-II in a reduced type when measures are provided to reduce transient over-voltages, OVC-II is selected for circuits and parts, and OVC-III is selected for accessible parts. The clearance distances would be smaller if OVC-I was selected.

The second parameter required is the material group which is determined by the Comparative Tracking Index (CTI) index. Using a material such as plastic, or melamine with a CTI index greater than 600 (Class-I) will provide an optimal design as creepage distances change significantly with this index.

The last parameter is the Pollution Degree (PLD). Under the assumption that there is no pollution or only dry and non-conductive pollution, the pollution degree can be selected as PLD-1. However, in most situations, this assumption is unlikely to be accurate, so pollution is changed to PLD-2. It is critical to note that the material group is only significant in the determination of creepage distance. In contrast, the PLD is only relevant in the determination of clearance distance for systems with impulse voltages up to 1.5kV. Consequently, both of these parameters are relevant only in the determination of creepage distance.

The pollution degree, CTI, and OVC definitions provide information regarding which categories should be considered in determining clearance and creepage distances. The parameters do not determine the type of insulation to be constructed such as functional, basic, etc. IEC-61800-5-1 specifies class D for Decisive Voltage Classification (DVC) above 1.5kVdc. Direct contact protection is required for this classification. Earthed components require basic insulation while accessible unearthed components call for protective separation. For adjacent circuits, basic insulation is needed. IEC/UL-950, on the other hand, grades insulation levels. Combining these standards can help define insulation grades. This is shown in Fig. 3.38, indicating insulation classifications required for converter control circuits, other modules, input power supplies, and parts that are accessible. F, B, and R refer to functional, basic, and reinforced insulation, respectively.

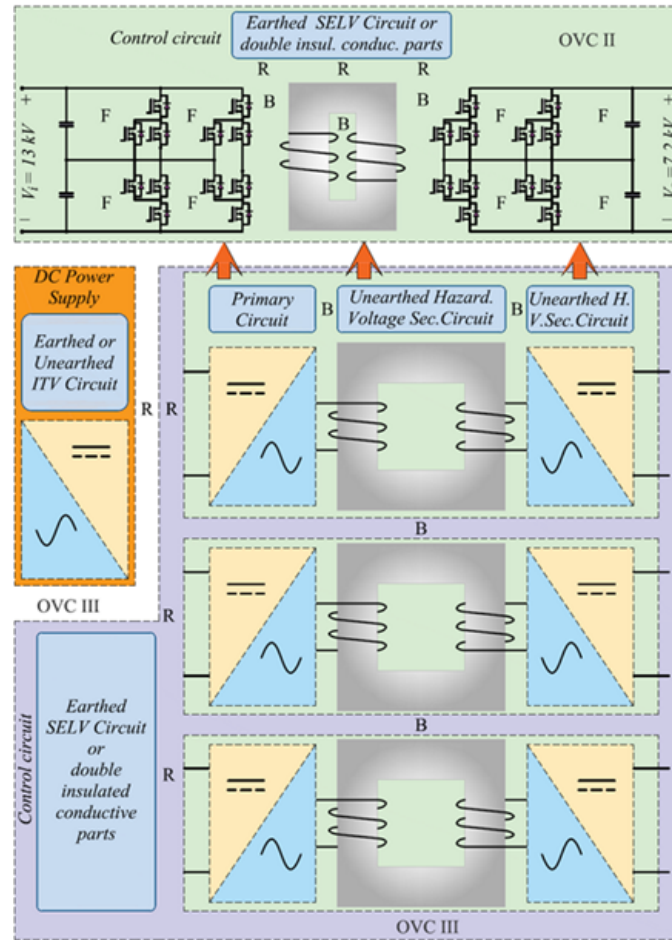


Fig. 3.38 Required insulation and OVC levels

Fig. 3.39 provides a structure describing each of the three levels of the research study system converter. The voltage levels at each point were calculated based on the given input and output voltage levels as well as possible switching signals. These voltage levels are given in Table 3.4.

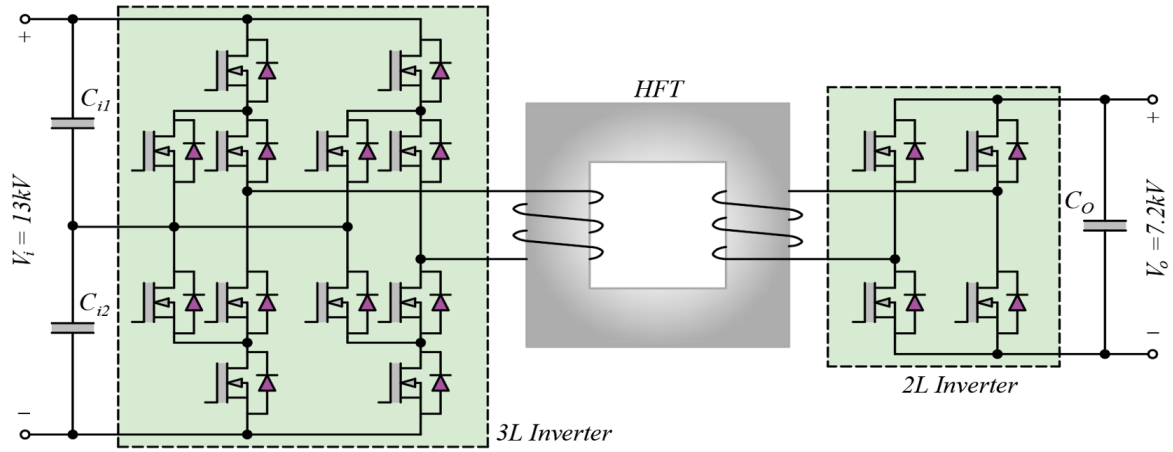


Fig. 3.39 A single stage of the 3L-2L converter

Table 3.4 Working Voltage, Clearance, and Creepage Distances

		Working Voltage Level (kV)																					
		(DCi+	DCi-	Ni	L1iup	L2iup	L1ilw	L2ilw	L1i	L2i	Core	Cold P1	Cold P2	L2o	L1o	L2olw	L1olw	L2oup	L1oup	No	DCo-	DCo+
Clearance/Creepage distance (mm)	DCi+		13	6.5	6.5	6.5	13	13	13	13	13	13	13	13	13	13	13	13	13	13	13	13	
	DCi-	67.2/65.5		6.5	13	13	6.5	6.5	13	13	13	13	13	13	13	13	13	13	13	13	13	13	
	Ni	36.4/33	36.4/33		6.5	6.5	6.5	6.5	6.5	6.5	6.5	6.5	6.5	13	13	13	13	13	13	13	13	13	
	L1iup	36.4/33	67.2/65.5	36.4/33		6.5	6.5	13	6.5	13	13	13	13	13	13	13	13	13	13	13	13	13	
	L2iup	36.4/33	67.2/65.5	36.4/33	36.4/33		6.5	6.5	13	6.5	13	13	13	13	13	13	13	13	13	13	13	13	
	L1ilw	67.2/65.5	36.4/33	36.4/33	36.4/33	36.4/33		6.5	6.5	13	13	13	13	13	13	13	13	13	13	13	13	13	
	L2ilw	67.2/65.5	36.4/33	36.4/33	67.2/65.5	36.4/33	36.4/33		13	6.5	13	13	13	13	13	13	13	13	13	13	13	13	
	L1i	67.2/65.5	67.2/65.5	36.4/33	67.2/65.5	67.2/65.5	36.4/33	67.2/65.5		13	13	13	13	13	13	13	13	13	13	13	13	13	13
	L2i	67.2/65.5	67.2/65.5	36.4/33	67.2/65.5	19.5/18	67.2/65.5	36.4/33	67.2/65.5		13	13	13	13	13	13	13	13	13	13	13	13	13
	Core	67.2/65.5	67.2/65.5	36.4/33	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5		13	13	13	13	13	13	13	13	13	13	13	13
	Cold P1	67.2/65.5	67.2/65.5	36.4/33	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5		13	13	13	13	13	13	13	13	13	13	13
	Cold P2	67.2/65.5	67.2/65.5	36.4/33	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5			7.2	7.2	7.2	7.2	7.2	7.2	7.2	7.2	7.2
	L2o	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	40.8/36.3			7.2	3.6	7.2	3.6	7.2	3.6	7.2	7.2
	L1o	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	40.8/36.3	40.8/36.3	40.8/36.3		7.2	3.6	7.2	3.6	3.6	7.2	7.2
	L2olw	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	40.8/36.3	19.5/18	40.8/36.3		3.6	3.6	7.2	3.6	3.6	7.2	7.2
	L1olw	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	40.8/36.3	40.8/36.3	19.5/18	19.5/18		7.2	3.6	3.6	3.6	7.2	7.2
	L2oup	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	40.8/36.3	19.5/18	40.8/36.3	19.5/18	40.8/36.3		3.6	3.6	7.2	3.6	7.2
L1oup	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	40.8/36.3	40.8/36.3	19.5/18	19.5/36.3	19.5/18	19.5/18		3.6	7.2	3.6	7.2	
No	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	40.8/36.3	19.5/18	19.5/18	19.5/18	19.5/18	19.5/18	19.5/18		3.6	3.6	7.2	
DCo-	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	40.8/36.3	40.8/36.3	40.8/36.3	19.5/18	19.5/18	19.5/36.3	19.5/36.3	19.5/36.3	19.5/18		7.2	
DCo+	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	67.2/65.5	40.8/65.5	40.8/36.3	40.8/36.3	40.8/36.3	40.8/36.3	19.5/18	19.5/36.3	19.5/18	19.5/18	40.8/36.3		

The insulation analysis of transformers is discussed in the next chapter. The transformer

is considered a component of the system, and it is assumed that it has been designed properly and is equipped with the necessary insulation system. Since the insulation requirements of the transformer may result in significant leakage inductances and capacitances. This may limit the power transfer capacity and may cause additional problems. In MV high-power isolated converters, galvanic isolation is distributed over several transformers. While this may increase the transformer size and volume, smaller transformers in this topology allow for higher frequency values, thereby balancing some of the disadvantages associated with this topology.

There is an insulation requirement IEC 60076-11: Power transformers - Part 11: Dry-Type Transformers applicable to high-frequency transformers. For equipment up to and including 36kV, IEC 60076-11 covers dry-type power transformers (including auto-transformers) with the highest voltages and at least one winding operating at 1.1kV. In this standard, insulation voltage levels based on European and North American practice are presented in Table 3 and Table 4, respectively, referencing IEC-60071. For low voltage levels, IEC-61800-5-1 refers to IEC60664-1, while for high voltage levels, it refers to IEC-62103 (the same as IEC 60076-11) and IEC-60071 (the same as IEC-60076-11). A comparison of Table 3 of IEC 60076-11 and Table 8 of IEC-61800-5-1 reveals that the voltage levels provided for OVC-III and OVC-IV in IEC-61800-5-1 are identical to those in IEC 60076-11, except for the system voltage of 36kV. Additionally, IEC 60076-3: Power Transformers-Part 3: Insulation Levels, Dielectric Tests, and External Clearances in Air provides guidelines on the appropriate dielectric tests and minimum dielectric test levels for power transformers. A range of standard test voltages up to 420kV is listed in Table 2 of IEC 60076-3. The highest voltage is identified by reference to IEC60071-1 for equipment U_m of a winding. IEC 60076-3 contains Table 2 which provides the Chopped Wave Lightning Impulse voltage in contrast to IEC 60071-1. In addition, while the switching impulse voltage is provided for equipment rated at 300kV and above in IEC 60071-1,

it is provided for equipment rated at 100kV and above in IEC 60076-3.

In IEC-61800-5-1, the insulation voltage for the high voltage circuits table determines the impulse voltage levels for each point of OVC-II. Based on the defined impulse voltage level, the clearance distance table is used to determine the required clearance distance. The creepage distance table can be used to calculate creepage distances based on material groups, pollution levels, and system voltage parameters. It is valid for functional, basic, and supplementary insulation. For functional, basic, or supplementary insulation, creepage distances can be determined directly, as in the clearance selection procedure. According to the corresponding voltage level, the clearance and creepage distances are shown in Table 3.4 in the form of clearance/creepage.

As explained in IEC-61800-5-1, in the case of strengthened insulation, the clearance and creepage distances cannot be used directly. In reinforced insulation, the impulse test voltage level should be selected at 1.6 times the regular case level. The creepage distances determined previously need to be doubled for reinforced insulation. Using these explanations, 13kV impulse voltage can be obtained by interpolating the table provided in IEC 61800-5-1 for OVC-II and OVC-III, respectively. Due to the basic insulation evaluation for circuits connected directly to the main supply section in the given standard, OVC-III should be used for reinforced insulation rather than OVC-II. Therefore, we conclude that the clearance and creepage distances indicated in Fig. 3.38 as 67.2mm and 65.5mm. The impulse voltage, which needs to be defined for determining the clearance distance for 13kV, is highly affected by both the increase of the OVC from OVC II to OVC III and the requirement to select this impulse voltage 1.6 times higher than other calculations for reinforced insulation. Accordingly, this distance is defined as 170.73mm. To calculate the creepage distance, the calculated values should be doubled, giving 131mm. A DC link voltage or part of it is applied to the gate driver board in MV power converter applications, depending on the converter topology. Since these applications require

careful insulation design, clearance, and creepage distances, gate drivers used in these applications must also be carefully designed. Different gate driver options including voltage-based gate driver, current loop gate driver, and wireless gate driver can be considered. By using IEC-61800-5-1 and related DVC, OVC classes, and CTI of the PCB material, required clearance and creepage distances can be calculated. Once these distances are calculated, V grooves, air gaps, and insulated barriers are designed to meet the creepage and/or clearance distance requirements.

In Fig. 3.40, the transformer is connected to the 10kV SiC modules while maintaining the appropriate clearance and creepage distances. This design is to be prototyped in the near future. As described in section 3.2, double-sided cold plates with liquid cooling are employed. Furthermore, MV DC capacitors are employed. Electrostatic simulation results of the power converter stage are provided in Chapter 5.

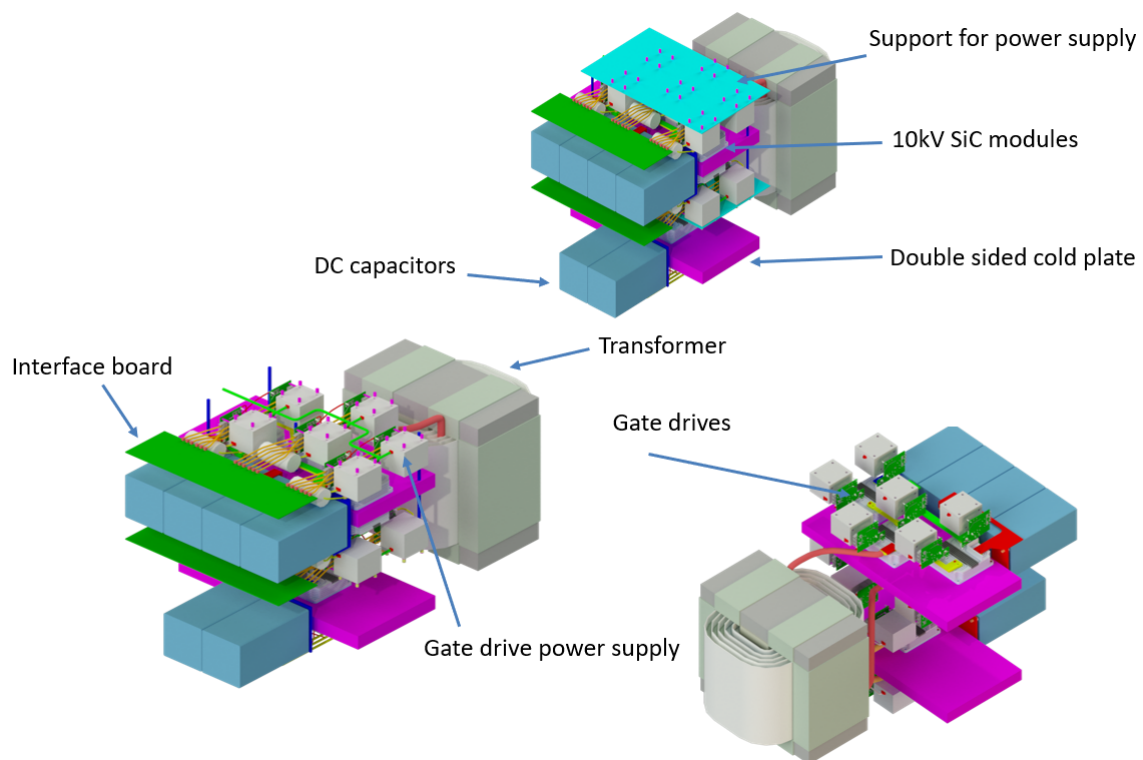


Fig. 3.40 Power Converter Design Assembly

CHAPTER 4

High Power, MV, and MF Transformer

The main components of SSTs, which may eventually replace conventional LFTs, are medium frequency power transformers. By carefully designing MF power transformers, the primary requirements of SSTs—high power density, low specific losses, voltage adaptation, and isolation requirements—are entirely or largely met. However, there are a number of issues that need to be resolved when high power, high voltage, and high frequency effects are taken into account. These difficulties are primarily caused by excess switching losses in the power semiconductors, which are typically the dominant power losses at higher frequencies, as well as additional losses brought on by eddy current in the magnetic core, enhanced skin and proximity effects, and parasitic elements, such as leakage inductance and winding capacitances. These additional losses combined with the smaller transformer size result in higher loss densities, necessitating an effective thermal management strategy to dissipate these power losses from a smaller component. When the transformer must meet MV isolation requirements while an oil-cooled design is not preferred, as opposed to line-frequency power transformers, this would be even more difficult. Majority of the designs for high frequency transformers concentrated on an area product parameter that measures the core's capacity to handle power. Research work reported an approach that was comparable and accounted for non-sinusoidal excitations. However, this approach essentially ignored the impact of parasitics. Additionally, it was demon-

strated in the literature that design considerations for a 3MW, 500Hz transformer can result in a transformer that is more than three times lighter than the 50Hz equivalent. Additionally, two 400kVA transformers based on silicon steel and nanocrystalline material, operating at 1 and 5kHz, respectively, were developed for use in railway traction applications. Another work provided a systematic analysis, design, and prototyping of two 166kW/20kHz SSTs. One of the MFTs was able to achieve a high power density of 32.7kW/liter using round-litz conductors and water-cooled aluminum plates, but doing so came at the expense of sizable additional losses—nearly 50% of the copper losses—because aluminum plates were used. Despite the successes in the aforementioned works, further research into the design and optimization of MFTs is necessary to ensure an effective and compact design. This can be accomplished by including unique thermal management strategies, new magnetic materials, careful conductor type and winding strategy selection, better insulation mediums, among other important design considerations. The validity of the traditional theoretical and empirical methods to evaluate the power losses and parasitics has also received relatively little attention, despite the fact that significant research has been devoted to the design of high frequency transformers. Given the aforementioned facts, it is crucial to examine the efficacy of conventional techniques and, in some cases, to modify and enhance their accuracy. This is crucial for high power and high frequency applications because they put a strain on the design and necessitate more accurate evaluation of these losses by researchers and designers in order to properly implement a thermal management strategy [8].

In Fig.4.1, the general MFT design flow is described. Pre-design, analytical design, and design validation are its three distinct phases. Each phase is completely independent of the others and has its own outputs.

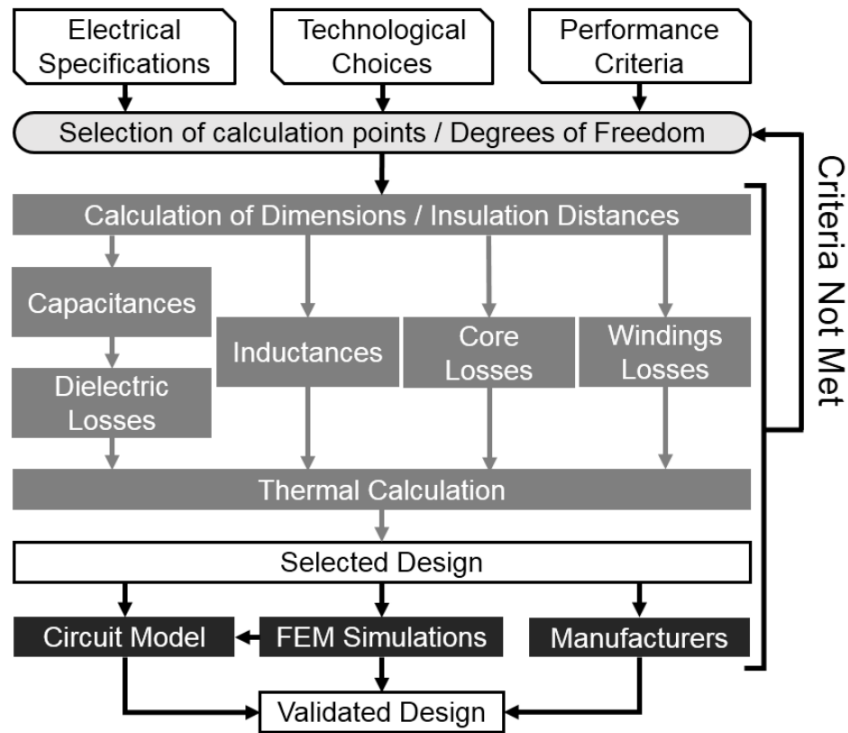


Fig. 4.1 Design flow chart showing pre-design steps (top-white), analytical design calculation (middle-light grey) and validation steps (bottom-black)

1) The goal of the pre-design phase is to collect all necessary inputs. It includes converter voltages, currents, and waveforms in addition to the standards-compliant insulation requirements, material characteristics, and performance standards. The accepted and/or desired values for efficiency, volume, weight, inductances, capacitances, and temperatures must be specified in these criteria. It is now possible to keep only the pertinent technological options thanks to a qualitative analysis of the requirements and limitations.

2) The computation of numerous designs based on variations of the various degrees of freedom constitutes the analytical design phase. This stage results in the choice of an MFT design that meets the requirements. This phase includes equations and models that analytically calculate every aspect of the transformer. First, the degrees of freedom and insulation distances are used to calculate the transformer's dimensions. Then, using the appropriate models, inductances, capacitances, and losses are computed. The maximum temperatures in each active part

are then determined by a thermal calculation.

3) The third phase, design validation, verifies that the chosen design will function as intended. To achieve this, it is necessary to confirm with the manufacturers the viability of a design with calculated dimensions. Additionally, FEM simulations will be run to get more accurate results on crucial transformer components. In order to ensure the proper operation of the entire converter, a circuit model of the MFT is also constructed based on analytical or numerical results and integrated into the converter simulation scheme [46].

In the sections below, a theoretical analysis of transformers is conducted. The following is a summary of the main issues and tradeoffs: a) Minimize leakage inductance => maximize power throughput b) Avoid core saturation at high voltage c) Minimize core and copper losses => Maximize efficiency level d) Insulation/ creepage/ partial discharge/ parasitics/ shielding/ EMI e) Thermal analysis and cooling requirements for high power SST system f) Power electronic ANPC – 2level circuit implementation g) High-computation FEA simulation/ resources/ and time requirements h) System optimization at component level i) Securing new-generation high voltage SiC switches and gate drives j) Maximizing power density k) Prototype building and packaging as a building block l) and HV, HF, high power testing.

4.1 Electromagnetic Analysis

4.1.1 Overview

Magnetic core, windings, insulation, cooling, and geometry all work together to make up a transformer's structure. SiFe sheets are the best candidate for low frequencies up to hundreds of Hz, followed by amorphous materials, followed by nanocrystalline materials for applications up to some and a few tens of kHz, and finally ferrites, which can operate up to several tens of kHz [46].

Since the magnetic materials in modern converters experience non-sinusoidal excitations, estimating the total loss is challenging. Size and weight are crucial factors in offshore wind farms that significantly affect the price and difficulty of the installation, foundation, and tower. In order to reduce the weight and size of the transformer, higher frequencies are sought to be used. These transformers have non-sinusoidal voltage and current waveforms. Therefore, it is important to look into how these non-sinusoidal waveforms affect the overall loss. By using the Fourier transform and superposition, winding loss calculations can account for this non-sinusoidal nature. However, due to the nonlinear nature of the magnetic materials, core loss evaluation is more challenging. According to the aforementioned facts, an accurate investigation of magnetic losses, particularly for non-sinusoidal waveforms, is necessary for the best design of a medium (high) frequency high power transformer.

The choice of magnetic material is another crucial factor in MF high power transformers. The magnetic materials with the lowest core losses, the highest saturation flux densities, and the highest continuous operating temperature are the most suitable for magnetic components operating at higher frequencies and powers. It is necessary to comprehend and consider each of these qualities in the proper order to make an appropriate choice. Due to their higher saturation flux densities than ferrites, ferromagnetic materials are preferred to be used in higher power density applications up to 10-15kHz among all categories of magnetic materials that are suitable for high frequency applications. Low loss and high saturation level ferromagnetic materials, in particular, include amorphous and nanocrystalline materials.

This chapter's investigation of core losses in high power density transformers exposed to non-sinusoidal waveforms aims to determine how much the magnetic loss depends on the waveform shape. First, the general properties of various soft magnetic materials are examined. Following an explanation of the three main core loss evaluation techniques, modified empirical

expressions for switch-mode magnetics are derived and examined across a broad range of duty cycles and rise times.

4.1.2 Magnetic Material Selection

In designing high power density transformers, choosing the right magnetic material is probably one of the most crucial steps. Studying the properties of magnetic materials will help make the best choice. In reality, one must compromise depending on the application because there is no perfect magnetic material for high frequencies that offers low losses, high saturation flux density, high permeability, and low magnetostriction. According to their uses as well as their magnetic properties, magnetic materials are categorized. A material that is easily magnetized and demagnetized is said to be "soft magnetic." Hard magnetic materials, on the other hand, need an external magnetic field to become magnetized and demagnetized. Transformer cores, which focus and hold the magnetic flux, are typically made of soft magnetic materials. There are four key factors that need to be considered in high frequency, high power applications:

- Specific core loss or core loss density
- Saturation flux density, B_{sat} ,
- Relative permeability μ_r ,
- Temperature characteristics

Different types of magnetic materials may meet high frequency requirements depending on these parameters. These materials' performance has been improved by altering ingredients, regulating process quality, and other factors. Table 4.1 provides a thorough explanation of the properties of magnetic materials used in medium- to high-frequency applications.

One can group these materials according to their saturation flux density, starting with the silicon steel family, which shows the highest B_{sat} , and moving on to XFlux, amorphous material,

nanocrystalline, KoolMu, and ferrite. Since powdered iron cores have low relative permeabilities and relatively high specific core losses, these magnetic materials are not the first choice for high power, high frequency applications.

Table 4.1 Magnetic Material Characteristics

Magnetic Material Type	Material	B_{sat}	Specific Losses @ 0.1 T, 100 kHz
Sil.Steel	10JNHF600 [95]	1.87 T	0.24 kW/kg
Sil.Steel	10NEX900	1.6 T	0.19 kW/kg
Amorphous	2605SA1 [96]	1.56 T	0.2 kW/kg
Ferrite	N87 [116]	0.39 T	0.009 kW/kg
Ferrite	3C85 [97]	0.45 T	0.009 kW/kg
Ferrite	3C93	0.52 T	0.009 kW/kg
Powder	Xflux 60 [98]	1.6 T	0.26 kW/kg
Powder	KoolMu 125	1.05 T	0.14 kW/kg
Nano.Crys	Vitroperm500F [99]	1.2 T	0.01 kW/kg
Nano.Crys	Finement [100]	1.23 T	0.011 kW/kg

Because the core of a transformer operates at high temperatures, thermal stability of the materials is a major concern. The maximum operating temperature is theoretically constrained by the Curie temperature, but in practice, the maximum temperature is determined by the thermal limits of the lamination and coating. The cooling of the core is instead controlled by the material's thermal conductivity. The lowest value of thermal conductivity is found in ferrite, while powder cores typically have the highest value. The laminated cores' anisotropic thermal conductivity is much higher in the rolling direction than it is across the lamination. This needs to be taken into account in the design process and heat transfer modeling.

The specific core losses of various magnetic materials are plotted against magnetic flux density at 5kHz in Fig.4.2 and Fig.4.3. The lowest specific loss and relatively high saturation level, B_{sat} , are observed in nanocrystalline materials (Vitroperm500F and Finement). For

high frequency, high power applications, ferrite and nanocrystalline soft magnetic materials are preferred over all other soft magnetic materials. However, using ferrite requires making a compromise with larger core cross sections due to a lower saturation level, which results in larger and heavier components—something that is not ideal for high power density applications.

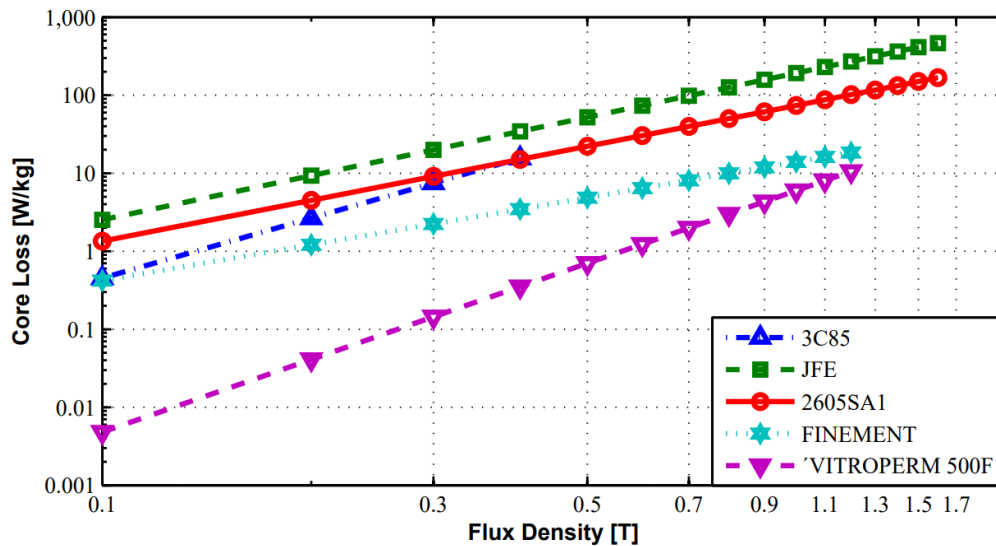


Fig. 4.2 Specific core loss comparison of different soft magnetic material versus magnetic flux density at 5kHz

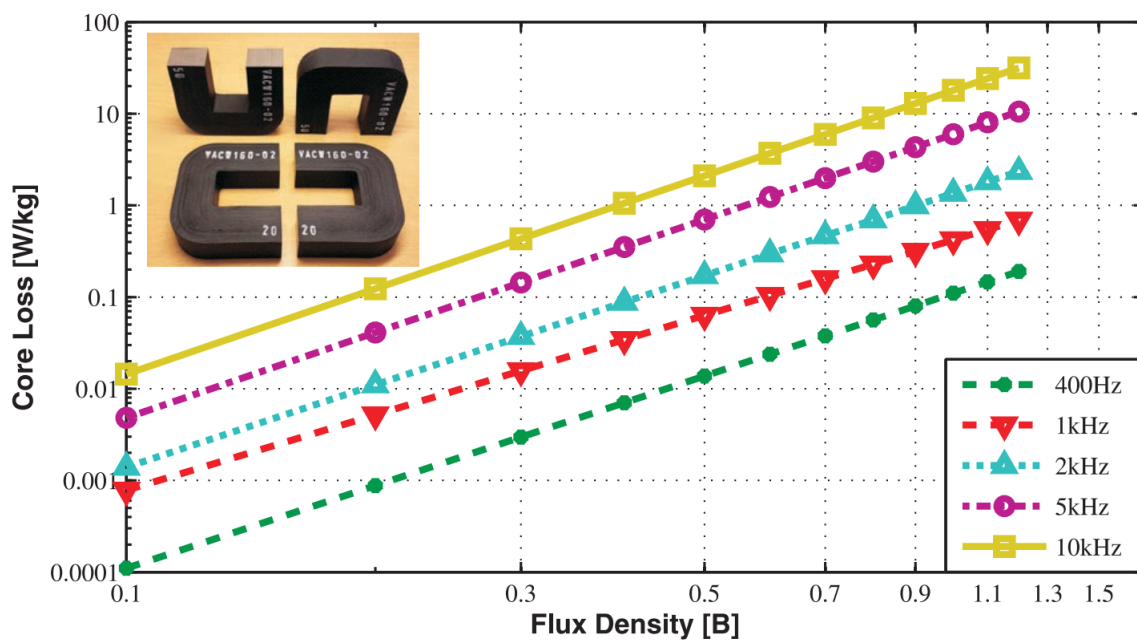


Fig. 4.3 Specific core loss of Vitroperm500F at different frequencies

Based on the application at hand, amorphous cores' performance at high frequency is not advised due to core loss, nanocrystalline has a limited market for C-cores, and they are expensive, especially if they are made to order. In comparison to nanocrystalline, ferrite MnZn 3C94, BFM8, and N97 have more readily available shapes and dimensions, acceptable core losses, and peak flux densities. Due to the availability of large E-cores, ferrite BFM8 material was chosen for high power, high voltage applications. The properties of the selected ferrite material are shown in Table 4.2. The B-H curve, power loss vs frequency, and power loss vs temperature plots are also shown in Figs. 4.4, 4.5, and 4.6, respectively. It can be demonstrated that, in order to fully utilize the transformer core without under-utilizing or over-utilizing it, which could cause the core to enter non-linear saturation mode, the optimal B-H curve operation point is around the knee point at 0.3-0.35T. Additionally, it can be inferred that running the core between 90 and 100C results in the least amount of core loss.

Table 4.2 Magnetic Material Characteristics

Characteristics	Symbol	Unit	Condition	Temperature	BFM8
Material	-	-	-	-	MnZn
Frequency Range	-	-	-	-	<500kHz
Initial Permeability	μ_i	-	-	-	2400 +/- 25%
Relative Loss Factor	$\tan(\delta/\mu_i)$	x1e-6	100kHz	25 C	<5
Saturation Flux Density	Bmax	mT	1194 A/m	25 C	490
				100 C	390
Coercivity	Hc	A/m	-	-	-
Power Loss	Pv	kW/m ³	25kHz/200mT	100 C	60
			100kHz/200mT	100 C	400
Curie Temperature	Tc	Degree Celcius	-	-	>215
Resistivity	p	Ω m	-	-	10
Density	d	kg/m ³	-	-	4800

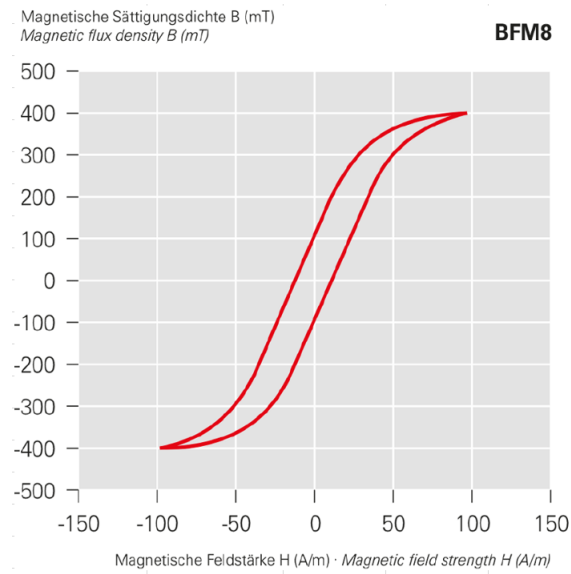


Fig. 4.4 Ferrite BFM8 B-H curve at 100C

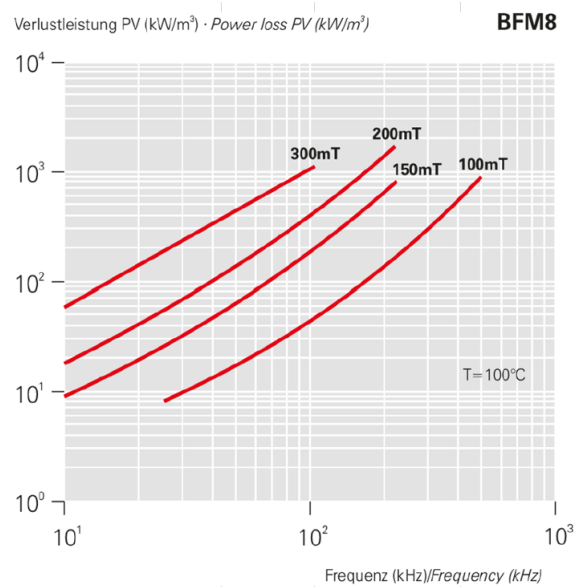


Fig. 4.5 Ferrite BFM8 power loss vs. frequency at 100C

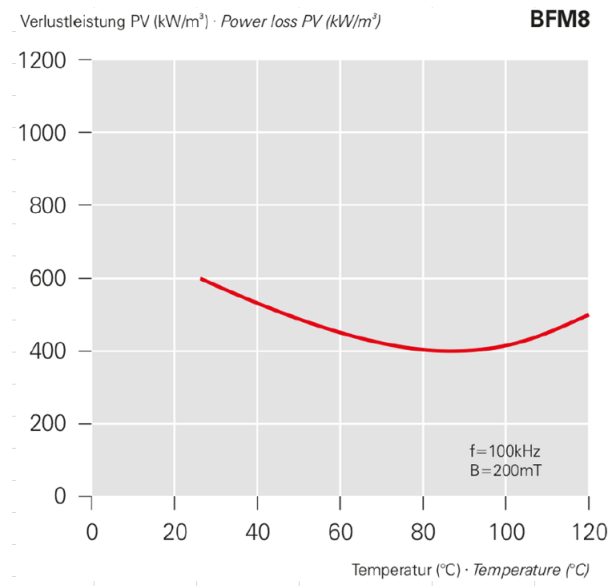


Fig. 4.6 Ferrite BFM8 power loss vs. temperature

4.1.3 Core Loss Calculation Methods

There is a specific working temperature limit for each magnetic material that must not be exceeded. Therefore, the allowed loss for a specific design will be restricted. Therefore, modeling and comprehension of losses within the winding and core are of utmost significance and are the fundamental knowledge to have a transformer designed as efficiently as possible, especially in high frequency applications. There are, in theory, three ways to calculate the core losses of magnetic materials: the time domain approach, empirical methods, and loss separation methods, which are covered next.

4.1.3.1 Loss Separation Methods

The total losses in this method are split into three groups: static hysteresis loss (P_h), dynamic eddy current loss (P_e), and excess loss or anomalous loss (P_{ex}).

- Losses from eddy current: eddy currents are created when a conductive material is exposed to a magnetic field that changes over time. A thin lamination exposed to a single-direction

magnetic field is taken into consideration to create these currents. One can compute the eddy current losses' time-averaged value by:

$$P_e = \frac{\sigma d^2}{12T} \int_0^T \left(\frac{dB(t)}{dt} \right) dt \quad (4.1)$$

where d is the thickness of each lamination, T is the excitation voltage period, and σ is the conductivity of the core material. If sinusoidal excitation occurs, (4.1) results in:

$$P_e = \frac{\sigma d^2}{12T} \int_0^T w^2 B_m^2 \sin^2(wt) dt = \frac{\sigma d^2}{24} w^2 B_m^2 \quad (4.2)$$

- Hysteresis Losses: for magnetic materials (ferromagnetics), the dependence of magnetic induction on the field is typically non-linear and takes the form of a so-called hysteresis loop. The hysteresis loss is caused by the rotation and movement of microscopic magnetic domains, and it also depends on the material's composition and grain size. Eddy current loss is negligible at very low frequencies, so the total measured loss is equal to hysteresis loss, also known as static hysteresis loss.

- Extraordinary Losses: in reality, especially for higher frequencies, there is a difference between the total magnetic loss as measured and the sum of static hysteresis and classical eddy current losses. This distinction is regarded as excess or unusual losses. This loss is brought on by domain wall movement during magnetization which produces microscopic eddy current loss. Bertotti put forth a statistical loss theory in 1983 and 1984 based on the description of the magnetization. This theory takes into account a number of active correlation regions that are dispersed at random throughout the material. The microstructure of the substance, such as the size of the grains, is reflected in the time-averaged expression of the excess loss and serves to

identify these active regions as follows:

$$P_{ex} = \sqrt{\sigma G A V_0} \frac{1}{T} \int_0^T \left| \frac{dB(t)}{dt} \right|^{1.5} dt \quad (4.3)$$

where A is the core cross-section, V_0 is a parameter describing the material's microstructure, and G is the magnetic object friction coefficient. Due to the manufacturer's inadequate disclosure of information, obtaining these coefficients can be challenging.

- Total Core Losses: a material's internal magnetic field intensity can be described as:

$$H_{total} = H_{st-hyst} + H_{eddy} + H_{excess} \quad (4.4)$$

which means that the sum of the three fields—static hysteresis, eddy current, and the field due to excess losses—is the total field. When measuring the total core losses, the B-H curve is widened by the other two components because they depend on frequency while the first component is static and frequency-independent. The magnetic material's overall power loss density per loop is:

$$P_{total} = \frac{1}{T} \int_0^T \left(H_{st-hyst} \frac{dB(t)}{dt} + \frac{\sigma d^2}{12} \left(\frac{dB(t)}{dt} \right)^2 + \sqrt{\sigma G_0} \left| \frac{dB(t)}{dt} \right|^{1.5} \right) dt \quad (4.5)$$

It should be noted that the excess loss is highest in the mid-range of frequencies, whereas the static hysteresis loss is dominant at low frequencies. The classical eddy current loss dominates at higher frequencies.

4.1.3.2 Time Domain Model

According to the loss separation method in the frequency domain, the core loss density is obtained by.

$$P_v = P_e + P_h + P_{ex} = k_e f^2 B_m^2 + k_h f B_m^\beta + k_{ex} f^{1.5} B_m^{1.5} \quad (4.6)$$

In this case, P_v stands for the core loss per volume, P_e for eddy current loss, P_h for hysteresis loss, P_{ex} for excess loss, β for the power factor, which is typically equal to 2, f for the operating frequency, and B_m for the maximum magnetic flux density. The loss coefficients, denoted by k_e , k_h and k_{ex} , of the investigated magnetic material and other properties of the core material are to be determined from the P-B curves shown in Fig.4.2 and Fig.4.3. As previously mentioned, equation (4.7) below can be used to determine the time averaged value of the eddy current loss:

$$P_e = \frac{\sigma d^2}{12T} \int_0^T \left(\frac{dB(t)}{dt} \right)^2 dt \quad (4.7)$$

Since (4.6) is only applicable to sinusoidal waveforms, the coefficient k_e is obtained by equating P_e in (4.6) and (4.7) under sinusoidal excitation. As a result, the following methods can be used to assess the instantaneous value for the eddy current loss:

$$P_e(t) = \frac{k_e}{2\pi^2} \left(\frac{dB(t)}{dt} \right)^2, k_e = \frac{\sigma \pi^2 d^2}{6} \quad (4.8)$$

The time averaged value of the excess loss is calculated as follows, as was previously mentioned:

$$P_{ex} = \sqrt{\sigma G A V_0} \frac{1}{T} \int_0^T \left| \frac{dB(t)}{dt} \right|^{1.5} dt \quad (4.9)$$

Since manufacturers typically do not provide a complete material characterization, k_{ex} in (4.6) cannot be extracted directly. One can see that the magnitude of the coefficient, k_{ex} , is depen-

dent on G and V_0 by comparing (4.9) with the corresponding term in (4.6). The value of k_{ex} must therefore be determined through curve fitting. Assuming pure sinusoidal excitation and equating, one can write:

$$k_{ex} = \sqrt{2\pi\sigma G_0} \frac{2\pi}{T} \int_0^T |\sin(2\pi ft)|^{1.5} dt \quad (4.10)$$

The instantaneous value of excess loss can therefore be determined by:

$$P_{ex}(t) = \frac{k_{ex}}{8.76} \left| \frac{dB(t)}{dt} \right|^{1.5} \quad (4.11)$$

As shown in the following equation, the time-averaged hysteresis loss density can be determined.

$$P_h = \frac{1}{T} \int_0^T H(t) \frac{dB(t)}{dt} dt \quad (4.12)$$

The Equivalent Elliptical Loop (EEL) method, which is implemented in the finite element program Maxwell, is used to calculate hysteresis losses in the time domain. The irreversible component of the magnetic field H_{irr} is used to describe the magnetic hysteresis loss, and the ellipse parameters are represented as:

$$B = B_m \sin(\theta), H_{irr} = H_m \cos(\theta) \quad (4.13)$$

where $\theta = 2\pi ft$ and H_m is the maximum value of the magnetic field intensity. The resulting ellipse's area equals the hysteresis loss. Substituting (4.13) into (4.12), the time averaged value of P_h can be expressed mathematically as:

$$P_h = \frac{1}{T} \int_0^T H_m B_m 2\pi f \cos^2(\theta) dt = \pi f H_m B_m \quad (4.14)$$

By equating (4.14) and P_h in (4.6) and rearranging for k_h , the following result is obtained:

$$k_h = \frac{\pi H_m}{B_m^{\beta-1}} \quad (4.15)$$

By substituting H_m from (4.15) into (4.13), one can derive:

$$H_{irr} = \frac{k_h B_m^{\beta-1} \cos(\theta)}{\pi} \quad (4.16)$$

hence,

$$P_h = \frac{k_h}{C_\beta T} \int_0^T |B_m \cos(2\pi ft)|^{\beta-1} \frac{dB(t)}{dt} dt \quad (4.17)$$

where,

$$C_\beta = 4 \int_0^{\frac{\pi}{2}} \cos^\beta(\theta) d\theta \quad (4.18)$$

By utilizing the irreversible component of magnetic field intensity, the time averaged loss P_h is calculated. The instantaneous hysteresis loss can be expressed as follows:

$$P_h(t) = \frac{k_h}{C_\beta} |B_m \cos(2\pi ft)|^{\beta-1} \frac{dB(t)}{dt} \quad (4.19)$$

Consequently, the following are the three elements of the instantaneous magnetic loss in 3D cases for soft magnetic materials:

$$\begin{aligned} P_v(t) &= P_e(t) + P_h(t) + P_{ex}(t) \\ &= \frac{k_e}{2\pi^2} \left(\left(\frac{dB_x(t)}{dt} \right)^2 + \left(\frac{dB_y(t)}{dt} \right)^2 + \left(\frac{dB_z(t)}{dt} \right)^2 \right) + \\ &\quad \frac{k_h}{C_\beta} |B_m \cos(2\pi ft)|^{\beta-1} \left(\left| \frac{dB_x(t)}{dt} \right| + \left| \frac{dB_y(t)}{dt} \right| + \left| \frac{dB_z(t)}{dt} \right| \right) + \\ &\quad \frac{k_{ex}}{8.76} \left(\left(\frac{dB_x(t)}{dt} \right)^{1.5} + \left(\frac{dB_y(t)}{dt} \right)^{1.5} + \left(\frac{dB_z(t)}{dt} \right)^{1.5} \right) \end{aligned} \quad (4.20)$$

Here, the instantaneous values for the hysteresis, eddy current, and excess loss are denoted as $P_h(t)$, $P_e(t)$ and $P_{ex}(t)$, respectively. It should be noted that all calculations of core loss derived from FEM use the time dependent method. By using the least square method to compare the loss density calculated by (4.6) with the loss density determined from measurements supplied by the manufacturer (Fig.4.3), the loss coefficients, k_h and k_{ex} , are determined as follows:

$$Error(k_h, k_{ex}) = \sum_{i=1}^n (P_{vi} - (k_e f^2 B_m^2 + k_h f B_{mi}^\beta + k_{ex} f^{1.5} B_{mi}^{1.5}))^2 \quad (4.21)$$

the values for the i^{th} point on the P-B curve at any given frequency are B_{mi} and P_{vi} , respectively.

4.1.3.3 Empirical Methods

The core loss for any given waveform can be estimated using loss separation techniques. However, only the eddy current loss can be calculated; the other two components' factors and coefficients should be discovered through extensive testing and parameter fitting techniques. Due to this flaw, this model appears inadequate and unworkable for designers who favor simple techniques and sparse data sources for their materials. Steinmetz presented an equation in 1892 to calculate the magnetic loss within materials that was only reliant on the magnetic induction's peak value.

- Original Steinmetz Equation (OSE) essentially came from the curve fitting of a number of experiments under sinusoidal excitations at various frequencies and peak magnetic inductions, is the version of the Steinmetz equation that is currently used by designers of magnetic devices:

$$P_c = k f^\alpha B_m^\beta \quad (4.22)$$

where, f is the fundamental frequency of the excitation and B_m is the peak magnetic induction. Additionally, k , α , and β can be easily obtained using manufacturer datasheets without requiring in-depth knowledge of the materials as they are determined by material characteristics. For sinusoidal excitations, the accuracy of this expression is excellent. However, there is a pressing need to identify a technique with respectable accuracy for non-sinusoidal flux waveforms given the expanding use of power electronic conversion systems. The Fourier transform, which can be used to break down any waveform into a series of sinusoidal waves, was used to solve this issue. The total loss was then determined by applying (4.22) to each sinusoidal component and taking advantage of the harmonic superposition effect. Due to the nonlinear nature of magnetic materials, there is no orthogonality between the various harmonics, so this summation differs significantly from the measured values.

- Modified Steinmetz Equation (MSE): in recent years, the most practical and helpful tool for assessing magnetization losses has been the empirical Steinmetz equations. In order to extend them for non-sinusoidal waveforms, several modifications have been made. The initial upgrade was based on the physical understanding of the mechanics of hysteresis and relating the magnetic loss to the speed of changing magnetic flux density. Based on this concept, an equivalent frequency, f_{eq} , that depends on dB/dt , was introduced:

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^T \left(\frac{dB(t)}{dt} \right)^2 dt \quad (4.23)$$

where ΔB is the peak to peak flux amplitude and T is the period of the flux waveform. The MSE calculates the magnetic loss density as follows, taking into account this equivalent frequency:

$$P_c = (k f_{eq}^{\alpha-1} B_m^\beta) f \quad (4.24)$$

where f is the excitation fundamental frequency.

- GSE: another modification was suggested to fix the discrepancy between the MSE and OSE for sinusoidal waveforms. This concept is based on the physical supposition that the loss within the material depends on both the instantaneous flux density and the rate at which magnetic induction is changing. In light of this presumption, the Generalized Steinmetz Equation (GSE) was presented as:

$$P_c = \frac{1}{T} \int_0^T k k_i \left| \frac{dB(t)}{dt} \right|^\alpha |B(t)|^{\beta-\alpha} dt \quad (4.25)$$

where,

$$k_i = \frac{1}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos(\theta)|^\alpha |\sin(\theta)|^{\beta-\alpha} d\theta} \quad (4.26)$$

- iGSE: The improved Generalized Steinmetz Equation (iGSE) is another frequently employed expression for core loss calculations:

$$P_c = \frac{1}{T} \int_0^T k k_i \left| \frac{dB(t)}{dt} \right|^\alpha \Delta B^{\beta-\alpha} dt \quad (4.27)$$

where,

$$k_i = \frac{1}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos(\theta)|^\alpha 2^{\beta-\alpha} d\theta} \quad (4.28)$$

By using the peak-to-peak value ΔB instead of the instantaneous value B , the waveform could be divided into one major and several minor loops, with the derived expression being applied to each loop separately. Similar methodology, known as the natural Steinmetz equation and giving rise to the same expression as iGSE, was first presented in another research paper.

- WCSE: Shen created the most recent iteration of the Steinmetz equation, referred to as the Waveform Coefficient Steinmetz Equation (WCSE). To establish a relationship between

any arbitrary waveform and the sinusoidal one with the same peak flux density, he presented a coefficient for (4.22). This Flux Waveform Coefficient (FWC) can be calculated by multiplying the area of the flux waveform by the corresponding sinusoidal flux value:

$$FWC = \frac{\int_0^{\frac{T}{4}} \phi_{arb}(t) dt}{\int_0^{\frac{T}{4}} \phi_{sin}(t) dt} \quad (4.29)$$

where $\phi_{arb}(t)$ and $\phi_{sin}(t)$ are the instantaneous magnetic flux values inside the core connected to arbitrary and sinusoidal excitations, respectively. The core loss expression of OSE (4.22) directly multiplies this correction factor as shown below:

$$P_c = FWC \cdot k f^\alpha B_m^\beta \quad (4.30)$$

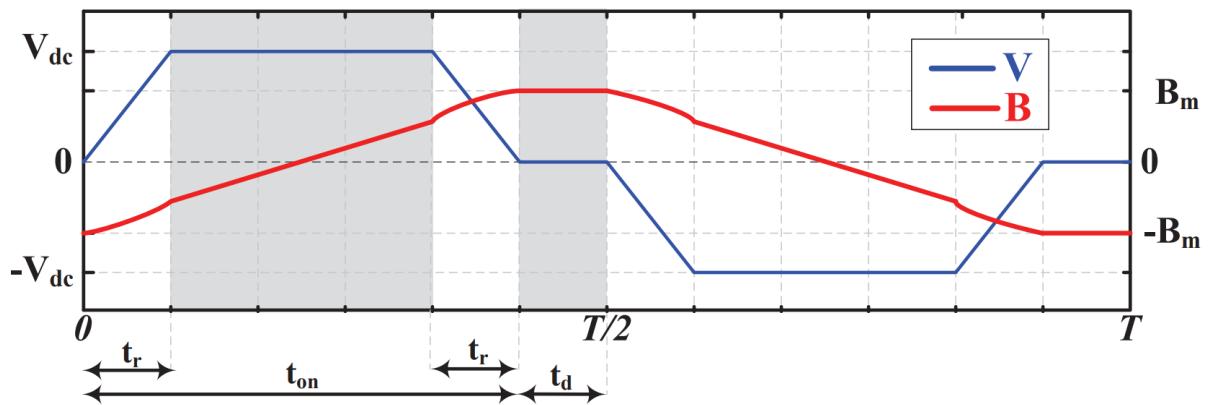


Fig. 4.7 Example of the excitation voltage and the corresponding instantaneous value of magnetic flux density

4.1.4 Modified Empirical Expressions

In this section, the aforementioned empirical loss calculation methods are modified to be applicable for rectangular waveforms, which are typical waveforms in switch-mode magnetics and have the corresponding duty cycles and rise times. The maximum applied voltage is regarded as a constant value for the purposes of comparing core losses while varying the waveform

characteristics. The peak induction, however, will not change. Therefore, the effective cross section of the core is varied to have a constant value of B_m by changing the shape of the voltage waveform, such as the rise time or duty cycle. The following Faraday's law equation shows the relationship between the necessary core cross section and the number of turns:

$$A_c * N_p = \frac{V_p}{k_f k_c B_m f} = \frac{13,000}{4 * 20,000 * 0.3} \Rightarrow A_c * N_p = \frac{13}{24} \quad (4.31)$$

where V_p is the peak value of the voltage shown in Fig. 4.7. k_c represents the core's filling factor, N_p represents the number of primary turns, and f represents the fundamental frequency.

The coefficient k_f is defined as:

$$k_f = \frac{2\sqrt{(2D - \frac{8}{3}R)}}{D - R} \quad (4.32)$$

where D stands for the duty cycle and R for the relative rise time in the rectangular waveform, with the rise and fall times being defined as:

$$D = \frac{t_{on}}{T} \leq \frac{1}{2}, R = \frac{t_r}{R} \leq \frac{1}{4} \quad (4.33)$$

In Fig. 4.7, where the time periods t_{on} and t_r are shown, the waveforms of the instantaneous voltage and the corresponding flux density are shown for one period. By integrating the voltage and dividing it by the number of corresponding winding turns and core cross section, one can quickly obtain the flux density waveform. As can be seen when the voltage is constant, the induction behaves linearly, but when the voltage is fluctuating during rise and fall times, the induction exhibits a second order pattern.

- Modified MSE: An accessible expression for magnetic core loss is derived as follows

using the previously described empirical equation of loss method for the MSE and (4.32) for the cross sections.

$$P_{c-MSE} = \left[\frac{2(2D - \frac{8}{3}R)}{\pi^2(D - R)^2} \right]^{\alpha-1} k f^\alpha B_m^\beta \quad (4.34)$$

- Modified IGSE: In a similar fashion, the derivation of the calculated expression for the IGSE method, suitable for loss assessment of the waveform shown in Fig.4.7, is as follows:

$$P_{c-IGSE} = \left[2D - \frac{4\alpha}{\alpha+1} R \right] \frac{2^\beta}{(D - R)^\alpha} k k_i f^\alpha B_m^\beta \quad (4.35)$$

- Modified WCSE: The modified WCSE expression is obtained as follows:

$$P_{c-WCSE} = \frac{4\pi}{D - R} \left[\frac{(D - 2R)^2}{8} + \frac{R^2}{3} + \frac{(1 - 2D)(D - R)}{8} \right] k f^\alpha B_m^\beta \quad (4.36)$$

In conclusion, thorough research has been done on a variety of core loss functions that are appropriate for arbitrary excitations. The OSE is the most popular empirical formula for estimating core loss, but it can only be used for sinusoidal excitation. Among the core loss functions that can be applied to any excitation waveform are MSE, GSE, and IGSE. Compared to OSE, these core loss functions are more accurate and general, but they are computationally intensive [8].

The following equation has been used in this study's use of IGSE to calculate the core power loss:

$$P_c = \frac{2^{\alpha+\beta} f^\alpha B_m^\beta D^{1-\alpha} K}{2^{\beta-1} \pi^{\alpha-1} (0.2761 + \frac{1.7061}{\alpha+1.354})} = 38.27 kW/m^3 \quad (4.37)$$

where α , β , and K are ferrite MnZn BFM8 material characteristics coefficients equal to 1.419, 2.884, and 3.53 coefficients, respectively, while D is the duty cycle equal to 0.5, and $B_m=0.3T$.

4.1.5 Windings and Transformer Geometry

Even though the most common materials for windings are copper or aluminum, the winding's internal structure has a bigger impact. Litz cables and foils are typical conductors used in medium frequency applications. For lower frequencies, however, continuously transposed cables can also be used. If higher losses and a liquid cooling system are not a concern, tubes are another option. The arrangement of the transformer's core and windings is referred to as its geometry. The most popular geometries for single-phase transformers are the core-type and shell-type, as shown in Fig.4.8. A toroidal core, coaxial windings, or matrix core configuration are some alternate geometries [46].

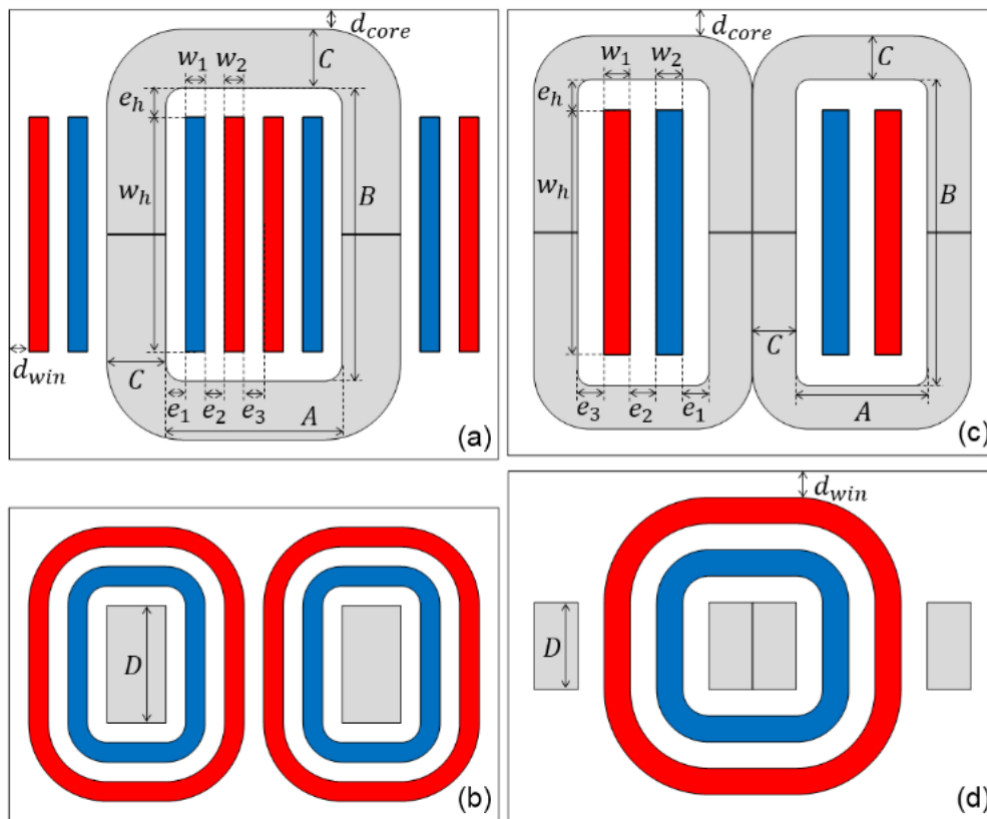


Fig. 4.8 Geometry schematics for (a) Core-Type front view, (b) Core-Type top view, (c) Shell-Type front view, and (d) Shell-Type top view in case of air insulation

The transformer's shape is crucial because it determines the energy density, core cross-

sectional area, volume, leakage inductance value, and overall size and compactness of the transformer. Avoiding core saturation and minimizing leakage inductance are two crucial constraints to be studied and taken into account when designing a challenging system like an MV MF high power transformer. On a 330kW 50kHz two-port transformer [82], the core-shape and shell-type configurations have been studied. The comparison of the two shapes' results demonstrated that the shell type configuration increases transformer efficiency and has a lower leakage inductance than the core-type one. Consequently, the system transformer core configuration has been decided upon as shell-type. As a result, the inner winding layers are the ones with lower voltage, and the outer layers would have higher operating voltage. The discussion of careful insulation and isolation distances is found in section 4.2 [83].

The largest available ferrite E-cores have been obtained (Fig. 4.9), and they have been built in shell configurations with various numbers of layers (depth). These models will be employed for the design and calculations compilation and optimization of all parameters in section 4.5.

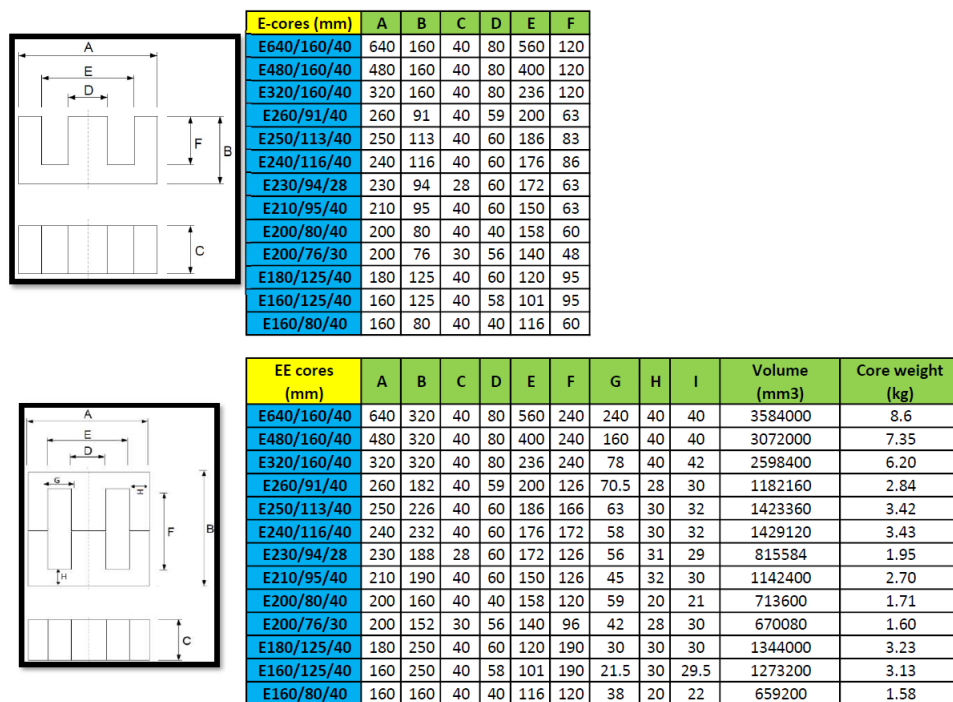


Fig. 4.9 Largest available ferrite E-cores used in design stage

4.1.6 Winding Loss

A winding conductor carrying alternating current is subject to magnetic fields as a result of both its own current and the alternating currents in nearby conductors. Eddy currents are produced inside the conductor as a result of the potential difference produced by these alternating magnetic fields. According to Lenz's law, the magnetic field produced by these eddy currents opposes the alternating field that initially caused them. As a result, unlike with direct current distribution, the distribution of alternating current inside the conductor is not uniform. When this occurs, the conductor's own alternating magnetic field has the result of increasing the charge concentration in the conductor's outer region, as indicated by the shaded area in Fig.4.10. As a result, the conductor's skin serves as the primary conduit for current flow, giving rise to the term "skin effect".

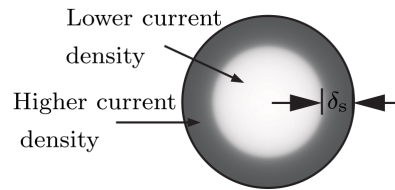


Fig. 4.10 Illustration of skin effect in a single current-carrying conductor

The skin depth, denoted by δ_s in Fig.4.10, is the depth below the conductor surface where the current density is reduced to about 37% of its value at the surface. This is expressed mathematically as follows:

$$\delta_s = \sqrt{\frac{p}{\pi \mu_0 \mu_r f}} \quad (4.38)$$

where p is the specific resistivity of the conductor material, μ_0 is the permeability of free space, μ_r is the relative permeability of the conductor material, and f is the frequency of the alternating current owing in the conductor. Similar to the skin effect, multiple current-carrying conductors placed close together will interact magnetically. As a result, the current density changes across

the conductors' cross-section depending on the direction of the current in the conductors, as shown in Fig.4.11. The proximity effect in current-carrying conductors is what causes this.

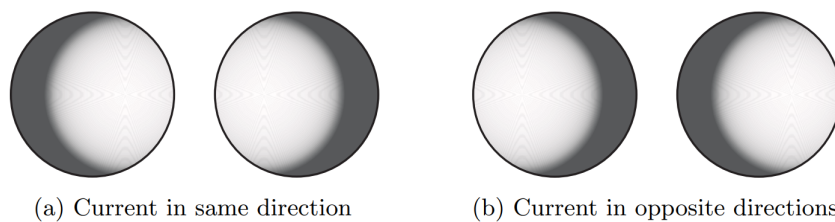


Fig. 4.11 Illustration of proximity effect between two neighboring current carrying conductors

It is crucial to take into account these two effects in order to analytically estimate the winding loss in a transformer winding in DAB because there are medium/high frequency currents in the windings and individual conductors are close together. Since the available cross-section for the current flow reduces as a consequence of skin and/or proximity effect, the resistance of the conductor(s) for AC, R_{ac} , is higher than for DC, R_{dc} , thus increasing the RI^2 loss. The R_{dc} is given by:

$$R_{dc} = \frac{p \cdot l_{con}}{A_{con}} \quad (4.39)$$

Litz wire, which consists of bundles of several thin, isolated strands, is typically used to lessen the skin effect. In order to analytically calculate the change in R_{ac} , a relation for litz wire was first presented and later improved. The approximate Bessel function served as the foundation for the concept. The proximity and skin effects were thought to be orthogonal to one another, allowing for the decoupling of the two effects, as shown by the following expression:

$$\begin{aligned} \frac{R_{ac}}{R_{dc}} = x_s(A) - x_p(A) = & \left[\frac{A}{2\sqrt{2}} \cdot \frac{ber(\frac{A}{\sqrt{2}})bei'(\frac{A}{\sqrt{2}}) - bei(\frac{A}{\sqrt{2}})ber'(\frac{A}{\sqrt{2}})}{(ber'(\frac{A}{\sqrt{2}}))^2 + (bei'(\frac{A}{\sqrt{2}}))^2} \right] \\ & - \left[\frac{A}{2\sqrt{2}} \cdot \frac{2\pi}{3} \cdot (4N_1^2 - 1) \cdot \frac{ber_2(\frac{A}{\sqrt{2}})ber'(\frac{A}{\sqrt{2}}) + bei_2(\frac{A}{\sqrt{2}})bei'(\frac{A}{\sqrt{2}})}{(ber(\frac{A}{\sqrt{2}}))^2 + (bei(\frac{A}{\sqrt{2}}))^2} \right] \end{aligned} \quad (4.40)$$

The Kelvin functions are denoted by the terms "ber" and "bei." The conductor diameter d_{con} in

relation to the frequency-dependent skin depth (4.38) is defined as the argument A as follows:

$$A = \frac{d_{con}}{\delta_s} \quad (4.41)$$

Another method for modeling the winding losses, also based on Bessel functions, takes into account a linear distribution of the leakage field across the winding for formulation of the following relation:

$$\begin{aligned} \frac{R_{ac}}{R_{dc}} = & \left[\frac{A}{2\sqrt{2}} \cdot \frac{ber(\frac{A}{\sqrt{2}})bei'(\frac{A}{\sqrt{2}}) - bei(\frac{A}{\sqrt{2}})ber'(\frac{A}{\sqrt{2}})}{(ber'(\frac{A}{\sqrt{2}}))^2 + (bei'(\frac{A}{\sqrt{2}}))^2} \right] - \\ & \left[\frac{A\pi^2\beta N_{str}}{48\sqrt{2}} \cdot (16N_1^2 - 1 + \frac{24}{\pi^2}) \frac{ber_2(\frac{A}{\sqrt{2}})ber'(\frac{A}{\sqrt{2}}) + bei_2(\frac{A}{\sqrt{2}})bei'(\frac{A}{\sqrt{2}})}{(ber(\frac{A}{\sqrt{2}}))^2 + (bei(\frac{A}{\sqrt{2}}))^2} \right] \end{aligned} \quad (4.42)$$

where N_{str} stands for litz strands per conductor turn, N_1 for "number of winding layers," and β for "winding packaging factor". When compared to (4.40), it can be seen that only the proximity effect term's coefficient has changed.

For round-wire winding, a relatively new method without Bessel function approximation was introduced, and later it was expanded to litz-wire winding. In light of this, the following expression can be used to determine R_{ac} :

$$\frac{R_{ac}}{R_{dc}} = A_s \left[\frac{\sinh(2A_s) + \sin(2A_s)}{\cosh(2A_s) - \cos(2A_s)} + \frac{2(N_{eff}^2 - 1)}{3} \cdot \frac{\sinh(A_s) - \sin(A_s)}{\cosh(A_s) + \cos(A_s)} \right] \quad (4.43)$$

where $N_{L,eff}$ is the effective number of winding layers given by:

$$N_{L,eff} = N_1 \sqrt{N_{str}} \quad (4.44)$$

The trigonometric and hyperbolic functions argument in (4.42) is changed from (4.40) in the

manner described below:

$$A_s = \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \frac{d_{str}}{\delta_s} \sqrt{\eta} \quad (4.45)$$

where d_{str} is the diameter of a single litz wire strand and η is the porosity factor, which is calculated as the ratio of the diameter of the conductor to the space between the centers of two adjacent conductors in the winding. The porosity factor for solid round-wire winding is assumed to be one.

Error rates for models based on the Bessel function typically range from 40% to 60%. In addition to analytical models, a more accurate FEM model can be used. Due to computational limitations, however, such a model is not preferred over analytical ones.

The winding power loss P_w can be calculated using the following relation given the frequency-dependent winding resistance (4.39, 4.41, or 4.42), and the decomposition of winding current in various sinusoidal harmonics:

$$P_w = R_{dc} \cdot \left[\sum_{h=1}^{\infty} I_h^2 \cdot \left(\frac{R_{ac}}{R_{dc}} \right)_h \right] \quad (4.46)$$

where I_h stands for the h^{th} harmonic of the winding current. In light of this, the two loss components can be analytically estimated using the core and winding characteristics as input [84].

To minimize skin and proximity effects at the system's 20kHz switching frequency, type-2 (Fig.4.12) litz wires have been chosen. Litz wires are conductors made of insulated strands that have been braided and twisted. As a result, the flux linkages between different strands will be balanced, resulting in a uniform distribution of current. A resistance ratio of $R_{ac}/R_{dc} = 1$ results from the reduction of skin and proximity effects, which lower AC losses in high frequency windings. Additionally, this will result in reduced eddy current losses, increased

efficiency, lower operating temperatures, a smaller final product footprint, significant weight reduction, and the avoidance of hot spots.

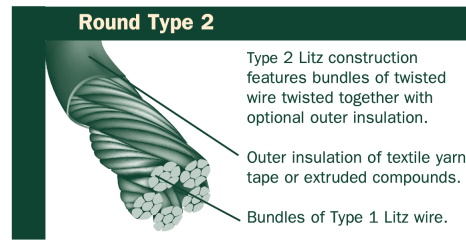


Fig. 4.12 Litz wire

36AWG individual strands are used for operating switching frequencies between 20 and 50kHz. With enough room for error, a current density of $1000 D_{cma}$ was used, resulting in the use of 1AWG secondary cables with 3360x36AWG strands and 4AWG primary cables with 1800x36AWG strands. Due to its outstanding dielectric strength of $\frac{2000Vac}{0.001''}$, maximum temperature of 250C, heat, water, and chemical resistances, exceptional flame retardancy, and low out-gassing, PFA cable jacket has been chosen. For the primary and secondary cables, 0.0101" and 0.0056" PFA thickness are calculated, respectively, using a 133 percent voltage margin for the cable voltage rating. Using Table 4.3 taken from the manufacture datasheet, the overall diameter of the cables is calculated. The primary and secondary cables have overall outer diameters of 0.342" and 0.559", respectively. Additionally, the primary cable weighs 156.42 pounds per 1000 feet, while the secondary cable weighs 318 pounds per 1000 feet. These numbers will be used in the compilation and optimization of all the parameters and transformer modeling.

Table 4.3 Litz cables characteristics

RECOMMENDED OPERATING FREQUENCY - 20 KHZ TO 50 KHZ										
30	100	4	36	S	1	-	.013	.318	110.100	4/36
28	175	7	36	S	1	-	.017	.557	62.900	7/36
26	250	10	36	S	1	SN	.023	.839	44.050	10/36
24	400	16	36	S	1	SN	.029	1.340	27.530	16/36
22	675	27	36	S	1	SN	.037	2.220	16.320	27/36
20	1025	41	36	S	1	SN	.044	3.350	10.740	41/36
18	1625	65	36	S	2	SN	.059	5.440	6.980	5X13/36
16	2625	105	36	S	2	SN	.074	8.740	4.320	3X35/36
14	4125	165	36	S	2	SN	.092	13.660	2.750	5X33/36
12	6625	265	36	S	2	SN	.116	21.830	1.710	5X53/36
10	10500	420	36	S	2	DN	.158	35.630	1.110	5X3X28/36
8	16500	660	36	S	2	DN	.197	59.010	.710	5X3X44/36
6	26250	1050	36	S	2	DN	.247	92.450	.450	5X5X42/36
4	45000	1800	36	S	2	DN	.322	156.420	.260	5X5X72/36
2	66500	2660	36	S	2	DN	.373	228.670	.180	7X5X76/36
1	84000	3360	36	S	5	SNB	.548	318.000	.140	6(5X4X28/36)
1/0	108000	4320	36	S	5	SNB	.655	420.000	.109	9(5X3X32/36)
2/0	135000	5400	36	S	5	SNB	.728	522.000	.087	9(5X3X40/36)
3/0	171000	6840	36	S	5	SNB	.870	682.000	.069	12(5X3X38/36)
4/0	211500	8460	36	S	5	SNB	.962	840.000	.055	12(5X3X47/36)

According to the above table, the primary and secondary cables' respective DC resistances are 0.26 and 0.14ohms per 1000 feet. The AC resistance is calculated using the equation below:

$$\frac{R_{ac}}{R_{dc}} = H + K\left(\frac{N * D1}{D0}\right)G \quad (4.47)$$

where, $H = 1$ is the resistance ratio of individual strands when isolated for 20-50kHz, $G = \left(\frac{D1\sqrt{F}}{10.44}\right)^4 = 2.1044 * 10^{-5}$ is the eddy current basis factor, $F = 20,000\text{Hz}$ is the operating frequency, $N_p = 1,800$ is the number of strands in the primary cable, $N_s = 3,360$ is the number of strands in the secondary cable, $D1 = 0.005''$ is the diameter of the individual strands over the copper, $D0p = 0.342''$ is the diameter of the finished primary cable over the strands, $D0s = 0.559''$ is the diameter of the finished secondary cable over the strands, and $K = 2$ is a constant depending on N . The primary and secondary litz wires' characteristics and parameter calculations are summarized in Table 4.4.

Table 4.4 Primary and Secondary Cables Parameters Summary

Parameters	Primary Cable	Secondary Cable
AWG	4	1
Current rating (A)	60	112
Strands	1800x36AWG	3360x36AWG
PFA jacket thickness (inch) (133% voltage rating)	0.0101	0.0056
Outer Diameter (inch)	0.342	0.559
Weight lbs/Mft	156.42	318
DC resistance (Ω /Mft)	0.26	0.14
AC resistance (Ω /Mft)	0.260245	0.14015
Total resistance (Ω /Mft)	0.520245	0.28015

4.1.7 Leakage Inductance

Fig.4.13 illustrates how leakage inductance affects DAB circuits. The voltage spikes, depicted in Fig.4.13, are brought on by the leakage flux's energy storage and will get worse as the load increases. These spikes will always be visible on the voltage switching waveform's leading edge. In order to reduce voltage spikes, transformers made for switching applications are typically made with a low leakage inductance, as shown in Fig.4.13. Additionally, the leading edge slope of the trapezoidal current waveform can be used to detect leakage inductance.

$$Energy = \frac{L_{lkg} I_{pk}^2}{2} \quad (4.48)$$

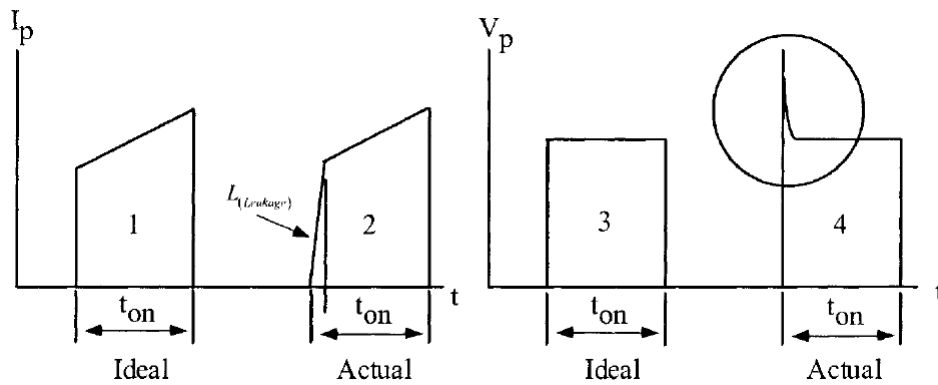


Fig. 4.13 Switching Voltage and Current Waveforms

Typically, a square wave with quick rise and fall times is used to drive transformers made for power conversion. Due to the parasitic capacitance in the transformer, this quick transition will cause high current spikes in the primary winding. These current spikes, depicted in Fig.4.14, are brought on by the capacitance in the transformer; regardless of the load, they always appear on the lead edge of the current waveform and have the same amplitude. Every half cycle, this parasitic capacitance will be charged and discharged. Transformer capacitance and leakage inductance are inversely correlated: increasing capacitance will increase leakage inductance, and decreasing capacitance will increase leakage inductance. To create the best transformer for the application, the power conversion engineer must make these trade-offs.

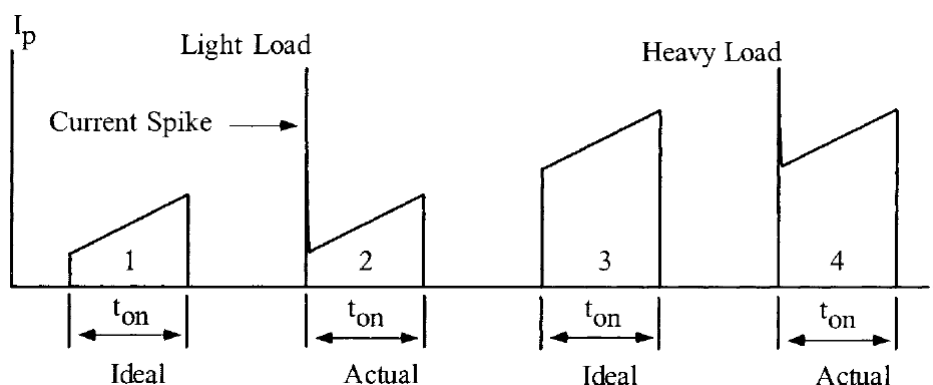


Fig. 4.14 Switching Voltage and Current Waveforms

Due to the flux created by the primary winding, which does not connect to the secondary

and instead creates leakage inductance in each winding without adding to the mutual flux, as shown in Fig.4.15, leakage inductance is actually distributed throughout the transformer's windings.

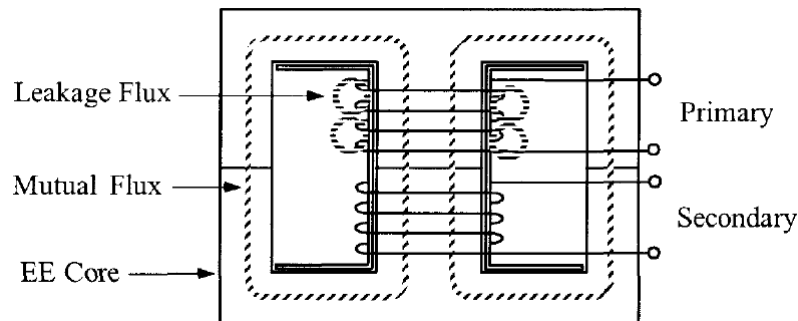


Fig. 4.15 Leakage Flux

Due to the flux created by the primary winding, which does not connect to the secondary and instead creates leakage inductance in each winding without adding to the mutual flux, as shown in Fig.4.15, leakage inductance is actually distributed throughout the transformer's windings. But in Fig.4.16, where the leakage inductance is denoted by L_p , leakage inductance is depicted as a lumped constant for the sake of simplicity.

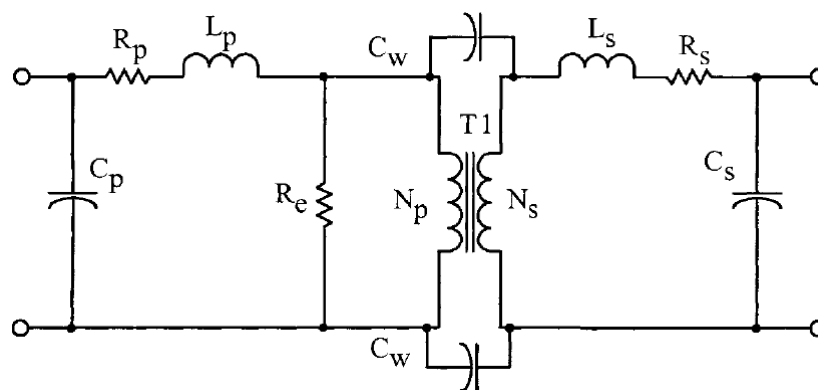


Fig. 4.16 Leakage Flux

The layer-wound coil's primary and secondary windings are intertwined to significantly reduce the leakage inductance, L_p and L_s . In Fig.4.17, the leakage inductance of the typical transformer with a single primary and secondary winding is displayed (4.49).

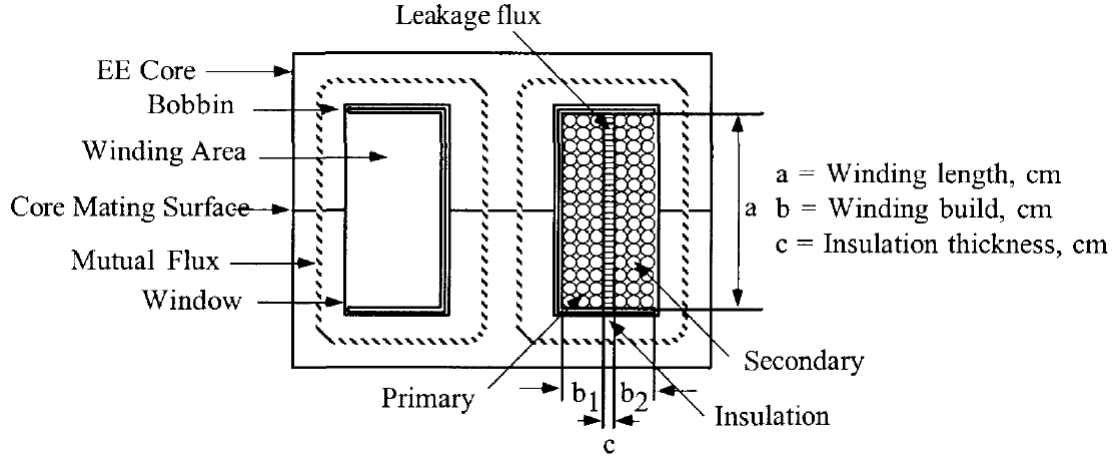


Fig. 4.17 Conventional Transformer Configuration

$$L_k = \frac{\mu_0(MLT)N_1^2}{a} \left(c + \frac{b_1 + b_2}{3} \right) \quad (4.49)$$

where the magnetic permeability $\mu_0 = 4\pi \times 10^{-7}$; MLT stands for the mean-length-turn of the core, a is the height of the windings, b_1 and b_2 for the thickness of the windings, c for the thickness of the insulation, and N_1 for the number of turns in the primary winding [85], [86]. Given the restriction on the maximum permissible leakage inductance for power flow, which is determined by the equation below at a phase shift of $\pi/3$, this equation will be incorporated into the overall optimization compilation process:

$$L_{lk_{max}} = \frac{nV_1V_2}{2\pi f_s P} \phi \left(1 - \frac{|\phi|}{\pi} \right) = \frac{0.55 * 13,000 * 7,200 * (\frac{\pi}{3})}{2 * \pi * 20,000 * 700,000} \left(1 - \frac{|\frac{\pi}{3}|}{\pi} \right) = 411 \mu H \quad (4.50)$$

The leakage inductance to be designed upon in terms of spacing and couplings between the primary and secondary windings is maintained to be a phase shift of approximately 25 degrees which corresponds to a ballpark of $200 \mu H$.

4.1.8 Area Product

Area product is a highly effective design tool that can be used to indicate a variety of transformer core properties. It makes the design process much simpler. The center pole area multiplied by the size of the winding window, or the space available for the copper wire and insulation, yields the area product of a core. The result, which is just a figure of merit when both areas are measured in square centimeters, is in centimeters to the fourth power. The area product has been shown to be a reliable predictor of the core's power rating for transformer applications, but it can also be used to determine the ideal core size for a transformer design. Its ability to predict additional important parameters, including surface area, temperature rise, turns, and inductance, makes it a flexible parameter. Many core manufacturers are currently quoting the area product. However, if not shown, it can be easily calculated using the following formula using the core dimensions:

$$A_{p,min} = W_a A_c = \frac{P_o D_{cma}}{K_t B_{max} f} SF = \frac{700,000 * 1,000}{0.0014 * 3,000 * 20,000} * 1.25 = 10,420 cm^4 \quad (4.51)$$

where $W_a A_c$ is the product of the window area and the core area, P_o is the transformer power level, D_{cma} is the current density in circular mil amps, f is the switching frequency, K_t is a topology constant, B_{max} is the maximum flux density, and SF is the stacking factor. $A_{p,min}$ is the minimum area product, reflecting the power handling capacity of a transformer core [87].

4.2 Insulation Analysis

The well coupled layout of the primary and secondary windings presents a challenge for achieving good electrical insulation for the parallel-concentric winding structure. In order to solve this problem, an insulation structure with flexible isolation boards of high dielectric strength was used to maintain adequate clearance between the inner and outer layer windings. The insulation structure between primary and secondary windings is depicted in Fig.4.18 and consists of an air gap (isolation board) and two layers of cable jackets.

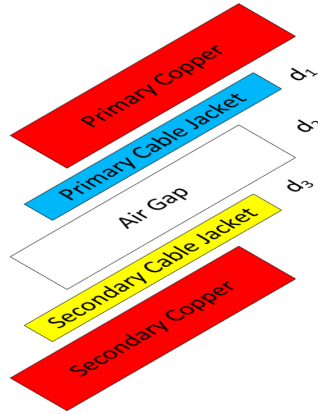


Fig. 4.18 Zoomed-in insulation structure between primary winding and secondary winding

One estimate for the distribution of electric fields is:

$$U = d_1 E_{pr-jacket} + d_2 E_{air} + d_3 E_{sec-jacket} \quad (4.52)$$

where U is the maximum voltage between primary and secondary windings = $13 - (-7.2) = 20.2\text{kV}$, $E_{pr-jacket}$ and $d_1 = 0.258\text{mm}$ are, respectively, the electric field and thickness of primary winding cable jacket, $E_{air} = 1.5\text{kV/mm}$ as safety margin and d_2 , respectively, the electric field and thickness of air gap, and $E_{sec-jacket}$ and $d_3 = 0.143\text{mm}$ are, respectively, the electric field and thickness of secondary winding cable jacket. The boundary condition for the nor-

mal field component across a medium interface is illustrated as follows under bipolar PWM excitation:

$$\epsilon_{pr-jacket} E_{pr-jacket} = \epsilon_{air} E_{air} = \epsilon_{sec-jacket} E_{sec-jacket} \quad (4.53)$$

where $\epsilon_{air} = 1.00059$, $\epsilon_{pr-jacket} = 2.06$, and $\epsilon_{sec-jacket} = 2.06$, respectively, are the dielectric constants of the air, primary and secondary winding cable jackets. The minimum isolation distance between the inner secondary winding layers and the outer primary winding layers is $d_2 = 12.8mm$ when (4.53) is plugged into (4.52). The primary and secondary windings isolation board for the transformer has been selected as the 12.8mm thick, 60kV high dielectric strength inorganic insulating board from 3M CeQUINBORD CGA (Fig.4.19).

3M™ CeQUINBORD CGA Inorganic Insulating Board

Typical Properties

Not for specifications. Values are typical, not to be considered minimum or maximum.

Properties measured at room temperature 73°F (~23°C) unless otherwise stated.

Property (Test Method)	Typical Value					
Nominal Thickness (ASTM D-645)	0.8 mm (1/32 inch)	1.6 mm (1/16 inch)	2.4 mm (3/32 inch)	3.2 mm (1/8 inch)	4.8 mm (3/16 inch)	6.4 mm (1/4 inch)
Basis Weight (ASTM D-202)	.88 kg/m ² 1.6 lb/yd ²	1.81 kg/m ² 3.3 lb/yd ²	2.6 kg/m ² 4.8 lb/yd ²	3.52 kg/m ² 6.5 lb/yd ²	5.18 kg/m ² 9.5 lb/yd ²	6.64 kg/m ² 12.2 lb/yd ²
Tensile Strength, MD (ASTM D-828)	55 lb/inch 96 N/cm	80 lb/inch 140 N/cm	130 lb/inch 228 N/cm	190 lb/inch 333 N/cm	215 lb/inch 376 N/cm	240 lb/inch 420 N/cm
Elongation, MD (ASTM D-828)	<2 %	<2 %	<2 %	<2 %	<2 %	<2 %
Dielectric Strength (ASTM D-149)	4.5 kV	12 kV	14 kV	20 kV	24 kV	28 kV
Moisture Absorption (ASTM D-644)	<1 %	<1 %	<1 %	<1 %	<1 %	<1 %

Fig. 4.19 3M™ CeQUINBORD CGA Inorganic Insulating Board

A 2D model is built based on the insulation design previously mentioned in order to simulate the distribution of the electric field in the MFT, as shown in Chapter 5. Excitation voltage is applied between the primary and secondary windings in the simulation in accordance with IEEE Std. C57.12.01 standard. According to the element geometry and Paschen's law, the air breakdown field (PD inception field) at ambient pressure is approximately 3kV/mm. The simulation results indicate that no significant PD is anticipated to be observed at this voltage level

because the electric field at working voltage is well below the air breakdown field. The electric field in the air and the dielectric are capacitively determined because the MFT is operating under bipolar PWM excitation in the DAB converter. Usually, the field strength in the gas-filled void or air gap is greater than it is in the solid dielectric. Consequently, the air gap is typically the most vulnerable link in the insulation chain. The field strength in the air gap needs to be less than a predetermined threshold, which is determined by the MFT configuration, in order to remove PDs from it. Fundamentally, Paschen's law allowed for a rough estimation of the threshold or PD inception field in the air gap. As a result, increasing the air gap's thickness is one way to raise the PD inception voltage (PDIV) of the MFT. Ideally, the MFT PDIV would be significantly increased by a large air gap between the primary and secondary windings. To achieve the desired power density as well as thermal and efficiency performance, the size of the MFT must be constrained. However, there is a clear space limitation due to the power density requirement of the MFT as well as the leakage inductance requirement [88].

The relationship between electrical insulation and PD is a novel topic for high-frequency transformer designs. Existing standards, FEA software, and theoretical calculations were applied in this situation. At this high voltage level, IEEE insulation standards have been used, and the clearance/creepage distances, insulation coordination, and E-field simulations have all been thoroughly examined in the same manner as described in section 3.4. According to IEEE C57.12.01/91 standards, four insulating testing requirements with their preferred testing sequences are as follows: Basic Impulse Lightning (BIL), low frequency applied voltage, induced voltage, and partial discharge test. BIL voltage level at each winding terminal while the other windings terminals and core are grounded. There should be no dielectric breakdown between any parts of the transformer (winding-winding or winding-core). According to Table-5 of the same standard (Table 4.5), 55kV is the calculated primary side BIL level and 39kV is

the secondary side one, and core insulation selected is 2x3M Tufquin 5-14 duplex electrical insulating sheets that provides 60kV dielectric strength (Table 4.6). The low frequency applied voltage test is 30kV and 17kV for primary and secondary, respectively. The applied voltage test shall be made by applying between each winding while all other windings connected to ground.

Table 4.5 Dielectric insulation levels for dry-type transformers used on systems with BIL ratings 350kV BIL and below

	Nominal L-L system voltages ^{d,e}	Low- frequency voltage insulation level	Basic lightning impulse insulation levels (BIL ratings) in common use kV crest ^{a,b} (1.2 × 50 μs)												
(kV rms)	(kV rms)	(kV rms)	10	20	30	45	60	95	110	125	150	200	250	300	350
1.5	1.2	4	S	1	1										
3.5	2.5	10		S	1	1									
6.9	5.0	12			S	1	1								
11	8.7	20				S	1	1							
17	15.0	34					S	1	1						
20	18.0	40						S	1	1					
27	25.0	50						2	S	1	1				
37	34.5	70								2	S	1			
49	46.0	95										S	1	1	
73	69.0	140											S	1	1
	Chopped wave ^c minimum time to flashover μs		1.0	1.0	1.0	1.25	1.5	1.6	1.8	2.0	2.25	2.7	3.0	3.0	3.0

Table 4.6 3M TufQUIN TF 5+14 Duplex Electrical Insulating Paper

Properties	Units	ASTM Test Method	Typical Values
Nominal Thickness	mm mil	D-645	0.48 19
Basis Weight	g/m ² lb/yd ²	D-202	645 0.84
Tensile Strength, MD	lb/inch N/cm	D-828	245 429
Tensile Strength, CD	lb/inch N/cm	D-828	314 550
Elongation to Break, MD	%	D-828	40
Elongation to Break, CD	%	D-828	132
Elmendorf Tear, MD	g N	D-689	740 7.3
Elmendorf Tear, CD	g N	D-689	1500 14.7
Dielectric Breakdown Voltage	kV	D-149	30
Moisture Absorption	%	D-644	<1

Induced voltage is intended to check the inter-turn and line-end insulation as well as main insulation to earth and between windings. Twice the rated voltage at secondary (in our case: 14.4kV) is applied and the primary windings terminals are kept open. Finally, PD is analyzed as a final step. PD is intended to verify that the internal insulation is free from damaging discharges. Each discrete partial discharge is the result of an electrical breakdown of an air pocket within the insulation. These discharges erode the insulation and eventually result in insulation failure. The general procedure for partial discharge testing is as follows: the voltage is raised to the pre-stress level of 1.8 times rated voltage (in our case: 23.4kV and 12.96kV), held for a minimum of 30s, and is then reduced to the voltage level equivalent to 1.3 times rated voltage (in our case: 16.9kV and 9.36kV) of the winding under test. After maintaining the 1.3 times rated voltage for 3 minutes, make the partial discharge measurement. This value shall be measured in picoCoulombs (pC) using techniques described in IEEE Std C57.124. The maximum acceptable level of partial discharge for solid cast windings is 10pC. The maximum acceptable level of partial discharge for resin-encapsulated windings is 50pC. Moving to the

insulation coordination studies which are at the SiC module termination points, IEC 61800-5-1 standard was employed.

Insulation coordination is the process of defining the dielectric strength, the insulation levels and distance considering the voltage levels of the system based on functional, basic, supplementary, double, and reinforced insulation level. According to the calculations conducted following the same procedure discussed in section 3.4, primary and secondary cable termination clearance and creepage distances are defined as 29mm/15mm for clearance and 65mm/37mm for creepage, respectively.

4.3 Thermal Analysis

4.3.1 Overview

The transformer is typically cooled using either natural or forced convection on its exterior surfaces (air or oil). To increase cooling effectiveness or decrease the volume of the transformer, more integrated solutions can also use cold plates on specific transformer faces. In addition, this solution needs an external liquid cooling system, which could increase the overall volume and solution losses [46].

A high-power transformer assembly is made up of many different materials, such as insulation, conductors, and cores, all of which have different thermal properties when combined. Different processes for heat transfer in various transformer assembly components are influenced by surface area, material properties, and coolant. As a result, estimating thermal behavior is necessary for an accurate characterization of the transformer's design. On the basis of conductor geometry and then the equivalent thermal network of the transformer, literature on analytical models to derive thermal resistances is presented. A bounded closed-form equation is used in another study to calculate the temperature gradient under unidirectional steady-state heat conduction. A more straightforward and general approach is discovered, which models various heat transfer mechanisms involved in various transformer parts and, in turn, characterizes various heat transfer coefficients.

The most significant and influential inputs are core and winding losses. Once the loss components are known, the core and winding geometry is used to calculate the thermal parameters, which are then precisely represented in each thermal branch. Finally, using Heun's method and PLECS, an equivalent thermal network of a concentrated winding transformer is derived and validated. Furthermore, FEM-CFD simulation results support the analytical findings. The

proposed thermal model is supported by strong agreement between analytical and simulation results, which demonstrates that it is simple to use, generally accurate, and computationally affordable.

To determine the thermal resistance for transformers of all sizes and shapes is the goal of thermal modeling. The ferrite material, core shape, conductor material, conductor size and type, winding process, insulation requirement (thickness and material of insulation layer), and cooling method all affect a transformer's thermal resistance. Theoretically creating a universal expression of thermal resistance for transformers of all sizes and shapes is too challenging. Experimental data is a useful tool for creating a thermal model for transformers. A transformer's hot spot is typically located at the bottom of the windings, or more specifically, where the winding meets the middle of the center leg of the bobbin. When a transformer is powered up, the measurement of the temperature increase in the hot spot can be used to determine the equivalent thermal resistance. Mulder measured these thermal resistances for transformers with various-sized EE cores under conditions allowing natural convection cooling. The measured thermal resistance, R_{th} , has been plotted as a function of the core volume, V_{core} , and is denoted by:

$$R_{th} = C_{th} V_{core}^{-0.54} \quad (4.54)$$

The following equation can be used to calculate the thermal resistance R_{th} expressed in terms of the area product A_p as shown below [67]:

$$R_{th} = K_{th} A_p^{-K_t} \quad (4.55)$$

where,

$$K_{th} = 12.22 \times 10^{-3}, K_t = 0.405 \quad (4.56)$$

These equations are used as a starting point for the temperature rise that will be compared in the compilation of transformer parameters for model optimization in section 4.5.

4.3.2 Thermal Resistance

Calculating the thermal resistance R_{ij}^{th} between two nodes (i,j) is carried out using (4.57). Based on the mechanism(s) involved, such as conduction, convection, radiation, or their combinations, the heat transfer coefficient h_{ij} is discovered.

$$R_{ij}^{th} = \frac{1}{h_{ij}A} \quad (4.57)$$

Expressions for the respective heat transfer coefficients are shown in Table 4.7 of the reference. Where l is the length of the material in the direction of heat transfer for the conduction heat transfer coefficient h_c .

Table 4.7 Heat Transfer Coefficients (h)

Conduction	Convection	Radiation
$h_c = \frac{\lambda}{l}$	$h_{cc} = Nu \frac{\lambda}{D}$	$h_r = \sigma \epsilon_i \frac{T_i^4 - T_j^4}{T_i - T_j}$

Surface orientation affects the equivalent conduction coefficient for convection, h_{cc} , D . According to some published works, D is equal to H for vertical surfaces and $\frac{WL}{W+L}$ for horizontal surfaces. Nusselt number is calculated using the formula $Nu = 0.55(GrPr)^{\frac{1}{4}}$. The Prandtl number $Pr = cp \frac{\mu}{\lambda}$ and the Grasshof number $Gr = \frac{p^2 g \beta D^3 \Delta T}{\mu^2}$ have no dimensions. Table 4.8 illustrates the temperature dependence of the properties of the coolant, such as density (p), volumetric expansion coefficient (β), dynamic viscosity (μ), thermal conductivity (λ), and specific heat capacity (c_p). ϵ_i and σ are the Stefan-Boltzmann constant and surface emissivity coefficient, respectively, for the radiative heat transfer coefficient (h_r).

Table 4.8 Coolant Properties of Oil (T = Temperature [C])

Parameter	Expression	Unit
ρ	$887 - 0.659 T$	$[kg.m^{-3}]$
β	8.6×10^{-4}	$[K^{-1}]$
μ	$0.13573 \times 10^{-5} \exp(\frac{2797.3}{T+273})$	$[kg.m^{-1}.s^{-1}]$
λ	$0.124 - 1.525 \times 10^{-4} T$	$[W.m^{-1}.K^{-1}]$
c_p	$1960 + 4.005 T$	$[J.kg^{-1}K^{-1}]$

4.3.3 Heat Capacity

The thermal capacitance (C^{th}) is calculated using formula (4.58) , where c_p , m , p , and V stand for the relevant material's specific heat capacity, mass, density, and volume, respectively. For the proposed lumped-winding thermal model, individual C^{th} for the insulation (enamel, Nomex) and conductor material (Cu) are added up to derive the equivalent thermal capacitance for a specific branch.

$$C^{th} = c_p m = c_p p V \quad (4.58)$$

4.3.4 Equivalent Thermal Network

A junction of a thermal branch is known as a node, where heat exchange occurs. The geometry of a typical shell-type transformer using an E-core (gray) is shown in Fig.4.20(a). With primary winding (red) inside and secondary winding (blue) outside, concentrated winding is positioned around the central limb. Each multi-layer winding is constructed of inter-layer cable jacket (green) and litz conductors. Each layer is a distributed source of heat. Individual turns in a layer are consolidated into a lumped layer, as shown in Fig.4.20(b) of reference. Individual lumped layers are combined with accumulated material (copper, insulation), which is symmetrically positioned around the mean radius of winding, as shown in Fig.4.20(c).

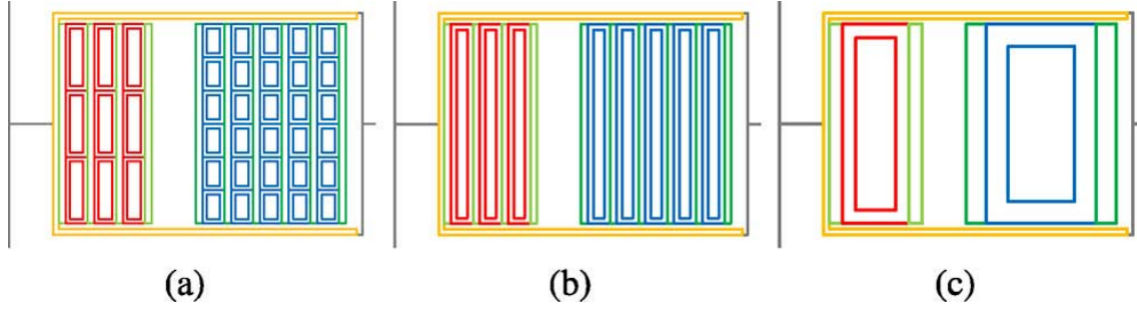


Fig. 4.20 Step-wise consolidation into an equivalent lumped model (a) Distributed turns and layers (b) Consolidation of turns into a lumped layer (c) Consolidation of layers into a lumped-winding

Additionally, the inner and outer sections of the winding's thermal resistances are calculated separately. When designing a high-power, high voltage system, the calculated value of $R_{wdg,o}^{th}$ is less than $R_{wdg,i}^{th}$ because the effective cross-sectional area is higher in the outer section of the winding for heat dissipation. Five thermal nodes are represented as total— T_{cc} , T_{ce} (core central, external limbs), T_p , T_s (primary, secondary) and T_{sp} (spacer). The ambient temperature, T_a , is represented as an infinite heat sink.

- Core: As shown in Fig.4.21(a), core loss is divided into central and external limbs and presented as separate thermal branches (a). Conduction is primarily used to transmit heat from the central core to the extremities. Between the core central limb and the primary winding through the bobbin, an alternate conduction path is created (insulation sheet). Due to exposure to coolant, convection heat transfer is more prevalent in the core external limbs.

- Winding: Fig.4.21(c) and Fig.4.21(d), respectively, show the thermal branches of the primary and secondary windings. Conduction is primarily used for heat transfer inside winding. Convection predominates between different winding sections because coolant is present in the spacer region. Convection also predominates at the secondary's outer surface.

- Spacer (isolation board): The thermal branch for a spacer is shown in Fig.4.21(b). Its temperature is higher than the surrounding air due to heat exchange between the winding and

coolant, which is confined in the spacer region. The order of the system matrix is increased by one while the spacer is modeled as an additional thermal node, but it aids in more precise calculation of thermal resistances resulting from convection mechanism. Convection mechanism at the surface where the coolant and winding meet in the spacer region ($R_{po,spacer}^{th}$, $R_{si,spacer}^{th}$). Calculations of the thermal resistances due to conduction of the coolant inside the spacer region ($R_{spacer,i}^{th}$, $R_{spacer,o}^{th}$) are done under the assumption that the coolant is a separate volumetric entity. Finally, the top and bottom exposed surfaces of the spacer region and the ambient temperature are taken into consideration for convection heat transfer, $R_{spacer,a}^{th}$.

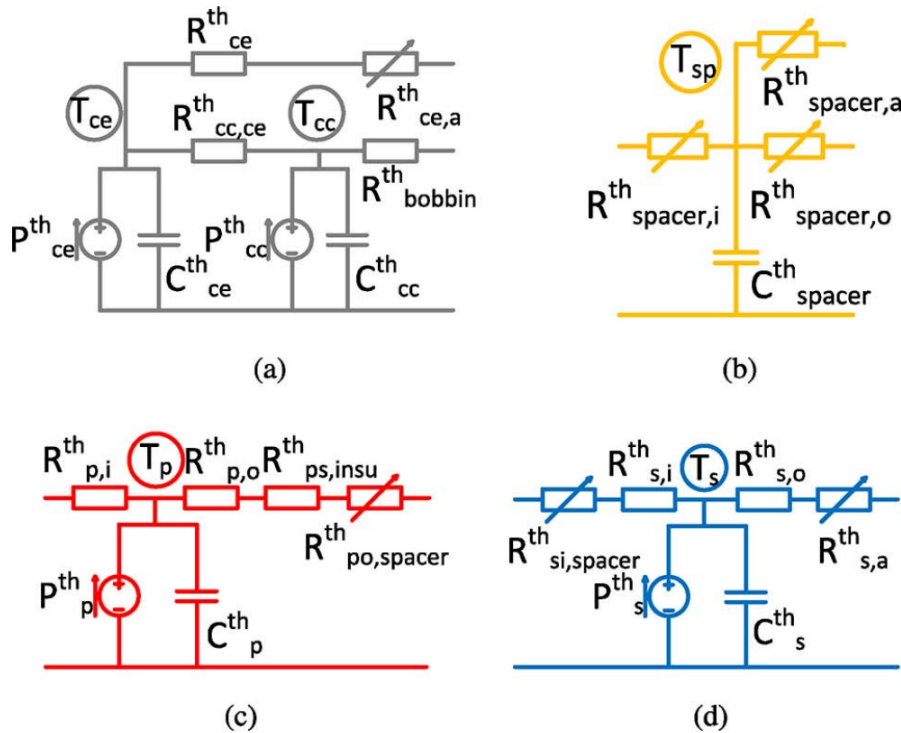


Fig. 4.21 Individual thermal branches (a) Core (T_{cc} , T_{ce}) (b) Spacer (T_{sp}) (c) Primary (T_p) (d) Secondary (T_s)

- Thermal Equivalence Model: to create the equivalent thermal network of the transformer as shown in Fig.4.22, the individual thermal branches of the core and windings are interconnected. Equivalent thermal resistance R_{eq}^{th} between nodes (i,j) is created by adding the individ-

ual thermal resistances of layers connected in cascade in the direction of heat transfer.

$$\begin{aligned}
 R_{ce,a}^{th} &= R_{ce}^{th} + R_{ce,a}^{th}(a) \\
 R_{p,cc}^{th} &= R_{bobbin}^{th} + R_{p,i}^{th}(b) \\
 R_{p,spacer}^{th} &= R_{p,o}^{th} + R_{ps,insu}^{th} + R_{po,spacer}^{th} + R_{spacer,i}^{th}(c) \\
 R_{s,spacer}^{th} &= R_{s,i}^{th} + R_{si,spacer}^{th} + R_{spacer,o}^{th}(d) \\
 R_{s,a}^{th} &= R_{s,o}^{th} + R_{s,a}^{th}(e)
 \end{aligned} \tag{4.59}$$

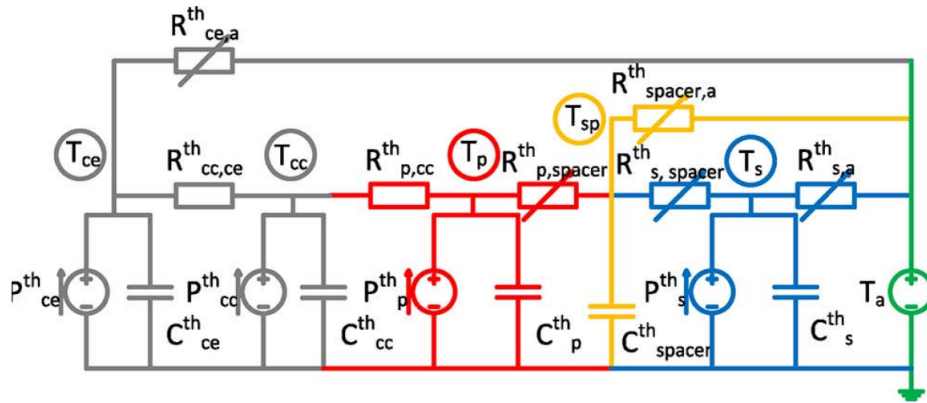


Fig. 4.22 Equivalent thermal network of transformer

4.3.5 Governing Equations

Every thermal node yields an energy balance equation. The system of equations in (4.60) shows how the derived thermal network is dynamic. In system of equations (4.60), time-varying components, such as $\frac{dT_j}{dt}$, can be set to zero to produce steady-state node temperatures. To estimate node temperatures at steady-state, a system of linear equations with the deduced form

(4.60) can be solved effectively, but transient behavior information will be lost.

$$\begin{aligned}
C_{cc}^{th} \frac{dT_{cc}}{dt} &= \frac{T_{ce} - T_{cc}}{R_{cc,ce}^{th}} + \frac{T_p - T_{cc}}{R_{p,cc}^{th}} + P_{cc}(a) \\
C_{ce}^{th} \frac{dT_{ce}}{dt} &= \frac{T_{cc} - T_{ce}}{R_{cc,ce}^{th}} + \frac{T_a - T_{ce}}{R_{ce,a}^{th}} + P_{ce}(b) \\
C_p^{th} \frac{dT_p}{dt} &= \frac{T_{cc} - T_p}{R_{p,cc}^{th}} + \frac{T_{sp} - T_p}{R_{p,sp}^{th}} + P_p(c) \\
C_{sp}^{th} \frac{dT_{sp}}{dt} &= \frac{T_p - T_{sp}}{R_{p,sp}^{th}} + \frac{T_s - T_{sp}}{R_{s,sp}^{th}} + P_{sp}(d) \\
C_s^{th} \frac{dT_s}{dt} &= \frac{T_{sp} - T_s}{R_{s,sp}^{th}} + \frac{T_a - T_s}{R_{s,a}^{th}} + P_s(e)
\end{aligned} \tag{4.60}$$

4.3.6 Numerical Solution

Equations in (4.60) are succinctly expressed in (4.61), where * denotes element-wise matrix multiplication.

$$\begin{aligned}
[C^{th}] * [T\cdot] &= [G^{th}][T] + [U] \\
\Rightarrow [T\cdot] &= [B] * [G^{th}][T] + [B] * [U] \\
\Rightarrow [T\cdot] &= [A][T] + [B] * [U]
\end{aligned} \tag{4.61}$$

Thermal capacitance and node temperature are denoted by $[C^{th}]$ and $[T]$, respectively. $[G^{th}]$ is the thermal conductance, which is calculated as $G_{ij}^{th} = \frac{1}{R_{ij}^{th}}$. The thermal susceptance $[B]$ is represented by the formula $B_{ij} = \frac{1}{C_{ij}^{th}}$. Core and winding losses are represented by $[U]$. Heun's (Modified Euler) method is used to numerically solve the equivalent thermal network.

4.3.7 Transient Behavior

The temperature of the windings (T_{wdg}) alters the wire's resistivity (p_{cu}), raising the DC resistance (R_{dc}). According to (4.62), when the switching frequency is fixed, the AC resistance

factor (F_R) decreases as the conductor resistivity (p_{cu}) increases.

$$F_{Rn} = \Delta[\zeta_1 + \frac{2}{3}(n^2 - 1)\zeta_2] \quad (4.62)$$

4.4 Transformer Six-capacitor Model

4.4.1 Overview

Continued efforts in developing Wide Band-gap (WBG) semiconductors have provided more efficient devices that lead to more power-dense power electronic converters. However, the higher voltages, faster edge rates, and increased switching frequency produce a problematic level of conducted emissions in the form of CM current [89]. The CM noise introduced can be a detriment not only to the converter itself but also to the surrounding systems. This CM noise can find its way through unexpected ground paths within the power distribution network and cause potential radiated emissions issues.

Frequency content in the high-frequency spectral range is introduced to the system as a byproduct of simultaneous higher voltage blocking capability and higher switching frequency (consequently reducing transformer size) that can be realized with WBG-based systems. Reducing the size of the transformer brings with it increased parasitic capacitance between primary to secondary sides of the transformer which, combined with the increased spectral content due to high dv/dt , lower loss switching of SiC MOSFETs results in high frequency circulating currents between primary and secondary circuits.

Electromagnetic (EMI) characterization methodologies have been emphasized in recent years as a means of gaining insight into root causes of self and system compatibility issues and as a means to EMI filter over-design. EMI characterization provides quantified insights into the Electromagnetic Compatibility (EMC) design challenge. Proper characterization is necessary to determine the correct amount of attenuation required to meet standards. If a method quantifies the EMI behavior with minimal computational burden, the iteration process is manageable to allow the implementation of automated EMI filter optimization algorithms. Various

EMI characterization methodologies have been explored by many researchers and generally fall under categories of direct circuit [90], FEA assisted [91], or empirically driven models [92]. These approaches can be categorized as either black-box methodologies [92], which lack high-frequency accuracy, or white-box methodologies [90], [91], which can be computationally burdensome and time consuming. To balance the analysis accuracy and simulation efficiency, a gray-box approach is applied in this work for EMI characterization. This modeling approach establishes a mathematical foundation by breaking up a Mixed-Mode (MM) circuit into its corresponding Differential-Mode (DM) and CM equivalent models (DEMs/CEMs), and captures the CM/DM cross-mode coupling caused by asymmetries. The approach enables accurate reproduction of waveforms up to 30MHz.

This chapter derives the CEM and associated DM cross-coupling for an Active Neutral Point Clamped (ANPC-FB), 2L-FB, and MF transformer. These CEMs are then combined to form the full NPC DAB CEM. The CEMs are derived in Section 4.4.2, validated through simulation and experimental results presented in Chapter 5. To the best of the author's knowledge, such derivation and validation for an NPC DAB have not been done in the literature.

4.4.2 Common-mode Derivation

The NPC DAB converter is a candidate topology for applications in power distribution systems due to its high power density, low device stresses, galvanic isolation, and bidirectional operation. With its high demand in power electronics, this chapter has been directed towards an accurate EMI characterization and reduction methodology to support the design of the DAB as a sub-module for much larger system applications. The NPC DAB topology and its corresponding test platform can be seen in Fig. 4.23. On the primary side of the transformer, there is a type-1 NPC full-bridge converter and can either be active (i.e. controlled as an ANPC con-

verter) or commutated through the diode depending on controls or voltage balance techniques. On the secondary side of the transformer, there is a 2L-FB. The CM modeling methodology establishes a mathematical equivalent circuit modeling technique. The dominant parasitic paths are parameterized and combined with CM voltage sources representing the impact of power electronic switching for an accurate prediction of conducted emissions. A systematic CM modeling approach is used where the objective is to define the CM voltage with respect to an arbitrary reference point, which is distinct from the ground. This floating reference makes it possible for the transformation of MM system components into CM equivalent components, which can then be systematically assembled to form CM equivalent circuits. These equivalent circuits accurately model the effects of mutual coupling between CM and DM voltages and currents due to circuit asymmetry. With this, there is a simple connection of these CM equivalent circuits that can be used to form the CM models for an entire system. The Line Impedance Stabilization Network (LISN)s connected to the lines on the inputs and outputs of the converter provide known CM impedances for the source and load side CM current paths and points to ground current measurement through each LISN resistor in order to provide hardware validation points for assumptions regarding internal parasitic capacitance paths to ground [93].

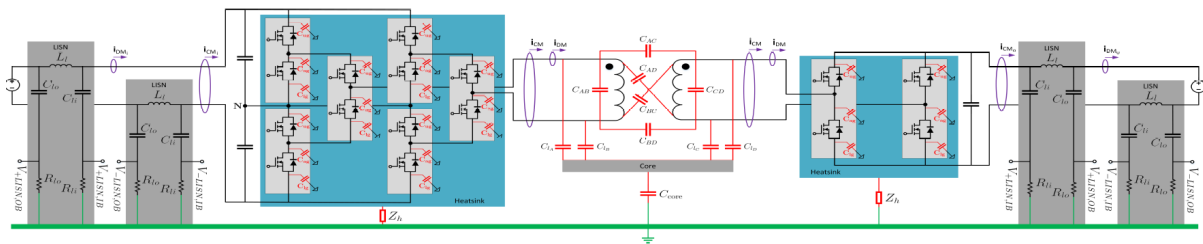


Fig. 4.23 EMI Characterization Platform, Dual Active Bridge MM Circuit with LISNs

The model validation approach is described in [94]. The full CM equivalent model will be comprised of three CM subsystems: the CM circuit of the Active Neutral Point Clamp full-bridge (ANPC-FB), the CM circuit of the MF transformer, and the CM circuit of the 2L-FB.

4.4.2.1 Converter CM Modeling

The first step in the proposed modeling methodology is to generate a CM equivalent circuit for each component of the power system. The general procedure for producing such an equivalent circuit from the component's DM model is broken into a few steps. First, parasitic couplings that provide paths for CM currents are identified and added to the DM model to form a MM model, shown in Fig. 4.23. The MM model is broken into its converter subsystems, and every interconnection point, or node, within the converter itself is labeled. When looking at these nodes, calculate the total paralleled capacitance to the heatsink for each node. Next, gather two or more nodes into "super-nodes", which need to be in proximity and make sense. Typically the super-nodes will be input nodes, output nodes, or symmetrical interconnection nodes. Once the super-nodes are assigned, construct a parasitic capacitance model.

When following this procedure, two-line and three-line parasitic capacitance models are typically encountered Fig. 4.24.

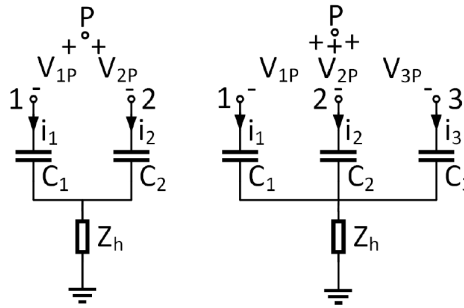


Fig. 4.24 Two-line (left) and three-line (right) capacitor models

By using KVL, line voltages for the model are determined with respect to an arbitrary reference point, P . The KVL for the two-line model in matrix form is,

$$\begin{bmatrix} V_{Pg} \\ V_{Pg} \end{bmatrix} = \begin{bmatrix} V_{1P} \\ V_{2P} \end{bmatrix} + \frac{1}{\hat{p}} \begin{bmatrix} \frac{1}{C_1} & 0 \\ 0 & \frac{1}{C_2} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} + \begin{bmatrix} R_h & R_h \\ R_h & R_h \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \quad (4.63)$$

where p is the Heaviside operator. Using the CM and DM definitions for currents and voltages:

$$\begin{aligned} V^{cm} &= \frac{(V_1 + V_2)}{2}, V^{dm} = V_1 - V_2 \\ i^{cm} &= i_1 + i_2, i^{dm} = \frac{(i_1 - i_2)}{2} \end{aligned} \quad (4.64)$$

and applying these definitions to transformation matrices:

$$T_2^v = \begin{bmatrix} 1 & -1 \\ 1/2 & 1/2 \end{bmatrix}, \quad T_2^i = \begin{bmatrix} 1/2 & -1/2 \\ 1 & 1 \end{bmatrix} \quad (4.65)$$

such that,

$$\begin{bmatrix} V^{dm} \\ V^{cm} \end{bmatrix} = T_2^v \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \quad \begin{bmatrix} i^{dm} \\ i^{cm} \end{bmatrix} = T_2^i \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \quad (4.66)$$

Applying these transformation matrices to the KVL equation decomposes the MM equation into its corresponding DM and CM equations. Then extracting the CM expression for a general two-line parasitic capacitor model results in:

$$V_{Pg} = -V^{cm} + \frac{C_2 - C_1}{2(C_1 + C_2)} V_{Cp,12}^{dm} + \frac{i^{cm}}{p(C_1 + C_2)} + Z_h i^{cm} \quad (4.67)$$

This expression is then extended to a single line circuit, which takes the form shown in Fig. 4.25. The total voltage from arbitrary point P to ground includes; the CM voltage source from P to the super-node, the DM coupling into the CM circuit (dependent voltage source), the total CM parasitic capacitance, and the heatsink impedance. When modeling a grounded system the heatsink impedance is simply a resistive connection to ground, and when a floated system is modeled there is a small capacitance in series with the resistive connection to ground.

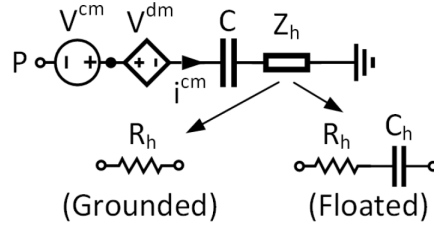
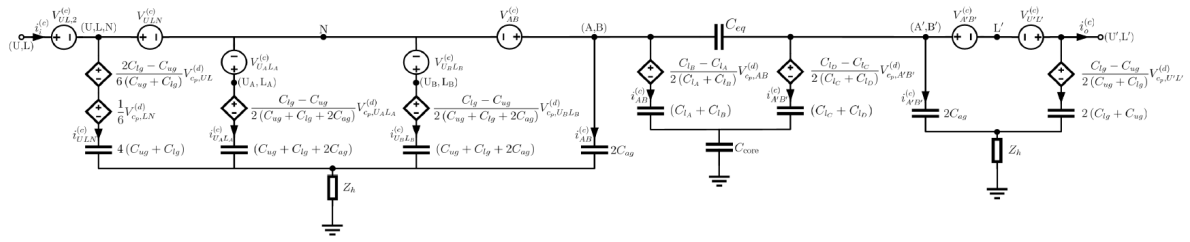


Fig. 4.25 CEM section example

Using this same procedure, the CEM for a three-line capacitor model can be derived with the CM expression shown in the below equation:

$$V_{Pg} = -V^{cm} + \frac{i^{cm}}{p(C_1 + C_2 + C_3)} + Z_h i^{cm} + \frac{C_2 + C_3 - 2C_1}{3(C_1 + C_2 + C_3)} V_{Cp,12}^{dm} + \frac{2C_3 - C_1 - C_2}{3(C_1 + C_2 + C_3)} V_{Cp,23}^{dm} \quad (4.68)$$

With (4.67) and (4.68), it is possible to construct the full system CEM. From inspection, as you increase the number of nodes in the super-node the more information it contains in each branch. By sticking with two- and three-line super-node models, it greatly reduces the complexity and the amount of DM coupling terms in each branch. Once this is applied to each component of the power system, the connection of each system is pieced together to form a CM equivalent circuit for the entire system. When piecing together each CM branch, the arbitrary reference point needs to be chosen. There is freedom in what is chosen for the arbitrary reference, but it makes sense to choose a point that is common within each converter separately (i.e. ANPC-FB, 2L-FB). For the CEMs produced in the paper, the arbitrary reference point for the ANPC-FB is chosen to be the neutral point (N), and for the 2L-FB it is chosen to be the lower DC bus connection (L). From there, it is a simple connection of similar reference points and super-nodes together to form the full system CEM as shown in Fig. 4.26.



4.4.2.2 Transformer Modeling

The CM modeling of the MF transformer has been derived from a simplified transformer parasitic model, Fig. 4.27. These lumped parasitic capacitance's seen are used to model conduction paths for the high-frequency currents. The inter- and intra-winding parasitics, labeled in blue, have originated from the basic six-capacitor model for winding parasitics. Each winding has a leakage capacitance due to the core and is labeled in red. The voltage stresses and winding capacitance are increased when grounding the core, for this reason, the core has been floated and this can be seen as some standoff capacitance, labeled in green.

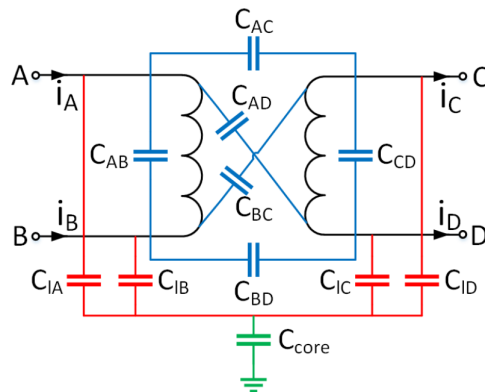


Fig. 4.27 Simplified transformer model

Since the transformer provides isolation, it makes sense to group up the input and output nodes separately. With the input and output super-nodes chosen, three main CM paths can be seen. First, a CM path from nodes (A,B) to ground through leakage paths containing C_{lA}

and C_{lB} . This creates a two-line parasitic capacitor model, therefore plugging the capacitance values into (4.69) provides a CM expression that can be constructed into a single line CM branch.

$$\begin{aligned}
C_{s,ortho} &= \frac{\epsilon_0 \cdot z \cdot l_{w,m}}{\alpha} \left[V + \frac{1}{8 \cdot \epsilon_D} \left(\frac{2\delta}{r_o} \right)^2 \frac{Z}{\alpha} \right] \\
&\quad \text{with} \\
\alpha &= 1 - \frac{\delta}{\epsilon_D \cdot r_o} \\
\beta &= \frac{1}{\alpha} \left(1 + \frac{h}{2 \cdot \epsilon_F \cdot r_o} \right) \\
V &= \frac{\beta}{\sqrt{\beta^2 - 1}} \cdot \arctan \left(\sqrt{\frac{\beta + 1}{\beta - 1}} \right) - \frac{\pi}{4} \\
Z &= \frac{\beta(\beta^2 - 2)}{(\beta^2 - 1)^{3/2}} \cdot \arctan \left(\sqrt{\frac{\beta + 1}{\beta - 1}} \right) - \frac{\beta}{2(\beta^2 - 1)} - \frac{\pi}{4}
\end{aligned} \tag{4.69}$$

where, $l_{w,m}$ is the mean turn length of the two considered layers, ϵ_0 is vacuum permittivity, ϵ_D is the dielectric constant of the wire insulation, and ϵ_F is the dielectric constant of the insulation between the layers.

Similarly, on the secondary side a CM path flows from nodes (C, D) to ground through leakage paths containing C_{lC} and C_{lD} . Resulting in another two-line parasitic capacitor model, where (4.69) is used again to construct another single line CM branch. The final CM path is the parasitic coupling path through the windings. Due to the nature of the modeling approach, the input nodes and output nodes are shorted, leaving an equivalent capacitance which consists of a parallel combination of the inter-winding capacitance. The intra-winding capacitance vanishes from the CM model, which makes sense as it primarily contributes to DM operation. The fully constructed CEM for the MF transformer is shown in Fig. 4.28.

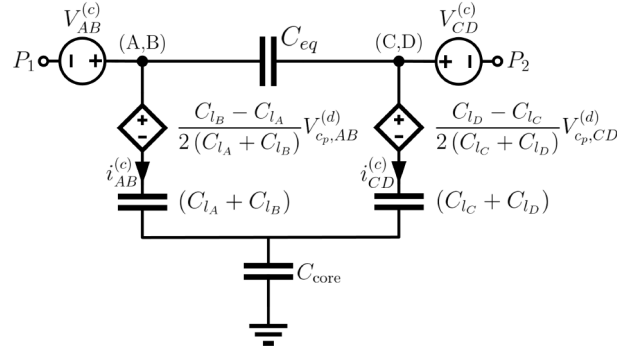


Fig. 4.28 Transformer CEM

With transformer isolation there is not a common reference point, therefore, the arbitrary reference points are influenced by its neighboring converter. So the primary reference point P_1 is shared with the ANPC-FB converter (N), and the secondary reference point P_2 is shared with the 2L-FB (L).

4.4.2.3 Transformer Parasitic Calculation

The cross-sectional view of the current design of the MF transformer can be seen in Fig. 4.29. The objective is to correlate the capacitance obtained from analytical calculations and Finite Element Analysis (FEA) simulations incorporated into the simplified six-capacitor transformer parasitic model.

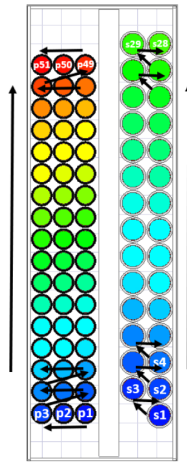


Fig. 4.29 Transformer cross-sectional view

Due to long computation time for FEA simulations, an analytical method of obtaining parasitic elements of the MF transformer needs to be established. This analytical method provides ways of determining winding parasitics which correlate to the equivalent six-capacitor model for multi-layer windings. This approach is used for windings consisting of solid or litz wire, but the calculations are carried out using solid wire approximations. For litz wires, the nominal radius can be calculated by subtracting the thickness of the litz wires outer insulation and the thickness of the insulation of a single strand from the total radius of the complete litz wire. The outer diameter of the litz wire can be taken from the data sheet of the wire. All calculations carried out for the equivalent winding capacitance are based on the static layer-to-layer capacitance. With this capacitance, the electrical energy which is stored between two successive winding layers is calculated and then used for calculating the equivalent capacitance for the whole winding arrangement. The winding capacitance of a transformer primarily depends on the winding arrangement, in which the windings can either be wrapped orthogonal or orthocyclic to each successive layer. In orthogonal windings the turns of successive layers are orthogonally on top of each other, whereas in orthocyclic windings the turns of the successive layers are in the gaps between the turns of the preceding layer. The current transformer design follows an orthogonal winding arrangement, in this arrangement the layer-to-layer capacitance is calculated by assuming the layers of the winding are equipotential surfaces that are used to approximate the electric flux lines as straight lines. With the considered path of the flux lines, a certain permittivity of the wire insulation and the insulation between the gaped layers with distance h , and the given layer-to-layer voltage, the electric field strength in different sections of the approximated flux line can be calculated. The electric field strength is used for calculating the electric energy which is stored between the two wires lying on top of each other. This energy is equated to the electric energy which is stored in the equivalent capacitor,

and then multiplying this capacitance by the number of turns per layer, z , results in the static capacitance of the two layers.

The static layer-to-layer capacitance does not take into account the voltage distribution between the layers, which is dependent on the winding method. There are two winding methods discussed in this chapter; standard and flyback winding methods, shown in Fig. 4.30.

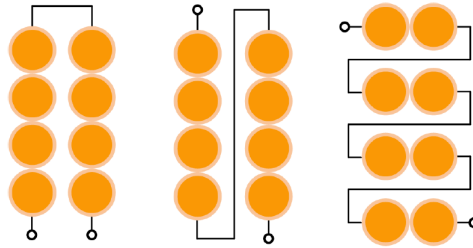


Fig. 4.30 (a) Standard winding; (b),(c) flyback winding

For the standard winding method, one side of the two layers is shortened and the voltage between the two layers at the unconnected end is doubled, which leads to a relatively high electric field strength and dielectric losses. With the flyback winding method all layers are wound in the same direction and the voltage between the two layers is consistently equal to one another. Therefore, the electric field strength and dielectric stress are uniformly distributed and thus lower compared to the standard winding method. Equating the stored electrical energy to the energy which is stored in the equivalent layer capacitor results in:

$$C_{layer,flyback} = \frac{C_{s,ortho}}{4} \quad (4.70)$$

The disadvantage of the flyback winding method is that at the end of one layer the wire of the winding has to cross all turns of this and its next layer, resulting in a larger overall winding length with more complexity for manufacturing and increased winding losses.

With the calculation of the equivalent layer capacitance for two layers defined, the equations

can now be extended for multi-layer windings. The equivalent capacitor for the complete winding is calculated by equating the energy stored in this capacitor to the energy which is stored in all the layer capacitors. If all layer capacitors are equal, the equation for the equivalent winding capacitor is greatly simplified to:

$$C_{winding} = 4 \cdot \frac{N_{layer} - 1}{N_{layer}^2} \cdot C_{layer} \quad (4.71)$$

Let us consider a multi-layer winding where all layers except the last layer have z turns and the last layer has k turns, where $k < z$. The equivalent winding capacitor is calculated by transforming all inter-layer capacitors to the connection of the winding by the impedance transformation rule of transformers. If it is assumed that all inter-layer capacitances are the same the equivalent winding capacitor is simply:

$$C_{winding} = \frac{4 \cdot C_{layer} (N_{layer} - 1) \cdot (z^2 + k^2)}{((N_{layer} - 1) \cdot z + k)^2} \quad (4.72)$$

Previously, an equivalent capacitance for two or more layers of the same winding has been calculated. This same technique can be used for calculating the equivalent capacitance for two layers from different windings (i.e. primary and secondary windings). The electrostatic behavior for two layers of different windings can be modeled by six independent capacitors. The values of the six capacitors are calculated using the energy approach, similar to the previous calculations. The six capacitors can be expressed in-terms of the static winding capacitance C_s , where it is assumed that $C_{AB} = C_{CD}$, $C_{AC} = C_{BD}$, $C_{AD} = C_{BC}$.

$$C_{AB} = -\frac{C_s}{6}, C_{AC} = \frac{C_s}{3}, C_{AD} = \frac{C_s}{6} \quad (4.73)$$

With all of this information, the calculation of the winding parasitic capacitance for the current transformer design can be done. The transformer employs the flyback winding method, similar to Fig. 4.30(c), with an orthogonal winding arrangement. The primary side has 17 layers, 3 turns per layer, and no distance between consecutive layers. The secondary side has 15 layers, 2 turns per layer, an incomplete layer containing a single turn, and no distance between layers. The wire constants are obtained from data sheets, and the mean turn length is determined by assuming a tight winding construction. The primary and secondary winding capacitance is calculated using (4.71) and (4.72), respectively. For the equivalent capacitance between the primary and secondary layers, only the static layer-to-layer capacitance (4.69) needs to be calculated, where the values used is the average between the primary and secondary winding values, and the insulation thickness between windings is accounted for. With this static capacitance, the equivalent capacitance is extended to the six-capacitor model following the assumptions made in (4.73). Finally, the primary winding capacitance which is in parallel with C_{AB} can be summed together, and likewise with the secondary winding capacitance and C_{CD} . This results in a calculated equivalent parasitic model for the windings of the MF transformer, shown in Fig. 4.31.

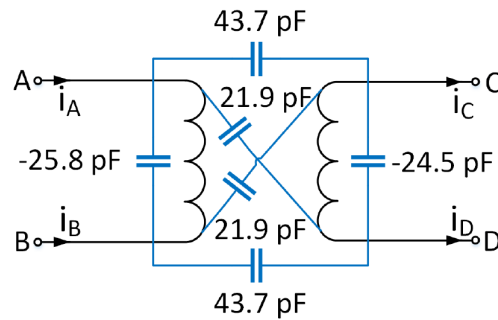


Fig. 4.31 Calculated Winding Parasitics

Simulation results and experimental validation will be presented in Chapter 5.

4.5 Transformer Parameters Compilation

Each parameter is calculated, and the optimized transformer model will be selected to be used and simulated in Ansys FEA simulations at the conclusion of the optimization algorithm. The parameters that were calculated and optimized for a variety of large E-core sizes and depths that are currently on the market are listed below:

- a) Window, cross-sectional, and power handling capability product areas: Eq. (4.51)
- b) Different core dimensions and shapes: Fig. (4.9)
- c) Number of primary and secondary turns: Eq. (4.31)
- d) Number of primary and secondary winding layers: Fig. (4.9)
- e) Length of primary and secondary winding cables: Fig. (4.9)
- f) Cable/core insulation: Table (4.6)
- g) Isolation distance: Eq. (4.52) + Eq. (4.53)
- h) Leakage inductance: Eq. (4.49)
- j) Core volume: Fig. (4.9)
- k) Core loss: Eq. (4.37)
- l) Primary and secondary windings copper losses (AC, DC): Eq. (4.47)
- m) Total losses and efficiency: Eq. (4.37) + Eq. (4.47)
- n) Temperature rise: Eq. (4.54) + Eq. (4.55) + Eq. (4.56)
- o) Transformer weight: (Fig.4.9) + Table (4.4)

CHAPTER 5

FEA Simulations and Experimental Results

5.1 Electromagnetic Ansys Simulation

After gathering all relevant data and comparing results from the previous chapter, we select the optimal theoretical model. An optimal transformer in terms of efficiency, temperature rise, weight, volume, and cost has been selected given a set of constraints including leakage inductance, isolation distance between primary and secondary layers, etc. Our ideal transformer layout requires a space of only about 320 millimeters on each side. Finite element analysis (FEA) software Ansys Maxwell-3D has been used to model electromagnetic fields with extreme precision. To achieve this, the materials are specified, litz wire is implemented, and actual cable jackets and insulation sheets are used in the simulation (Fig. 5.1).

As we delve deeper into the specifications of this transformer, we can see from this perspective of the cross-sectional area that the primary winding has 36 turns and two layers, while the secondary winding has 21 turns and two layers as well. The isolation distance is 12 millimeters, the layer thicknesses for the primary and secondary layers are 29 and 35 millimeters, respectively, and high dielectric strength insulation sheets with a thickness of 0.96 millimeters are used to isolate the core (Fig. 5.2).

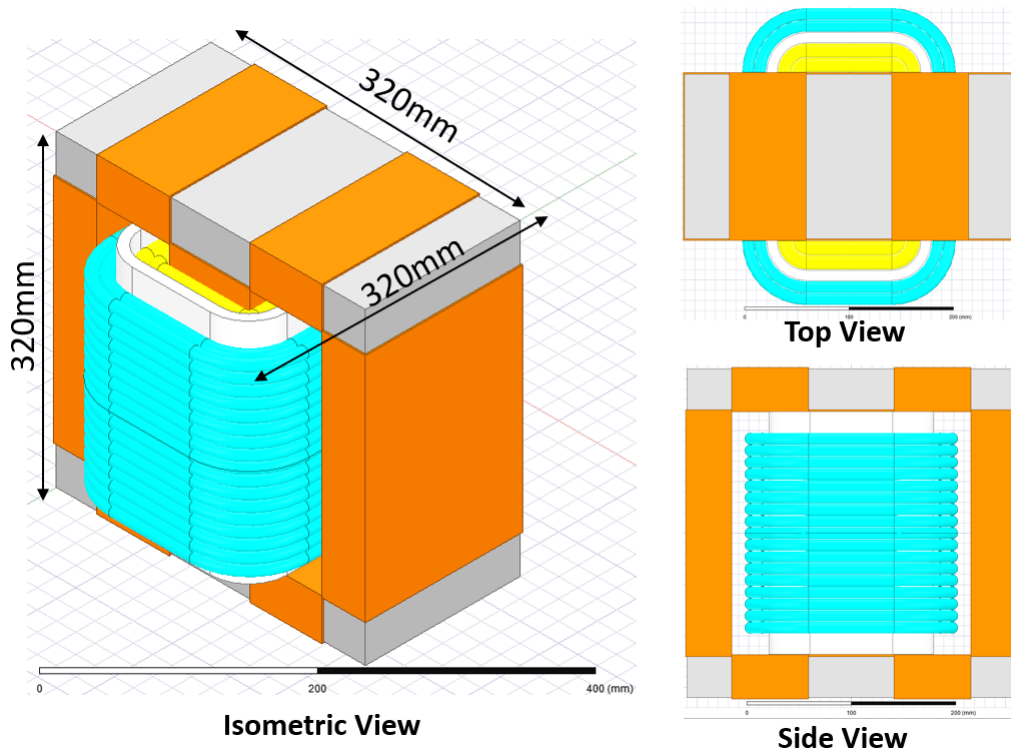


Fig. 5.1 Ansys Maxwell-3D Transformer Model

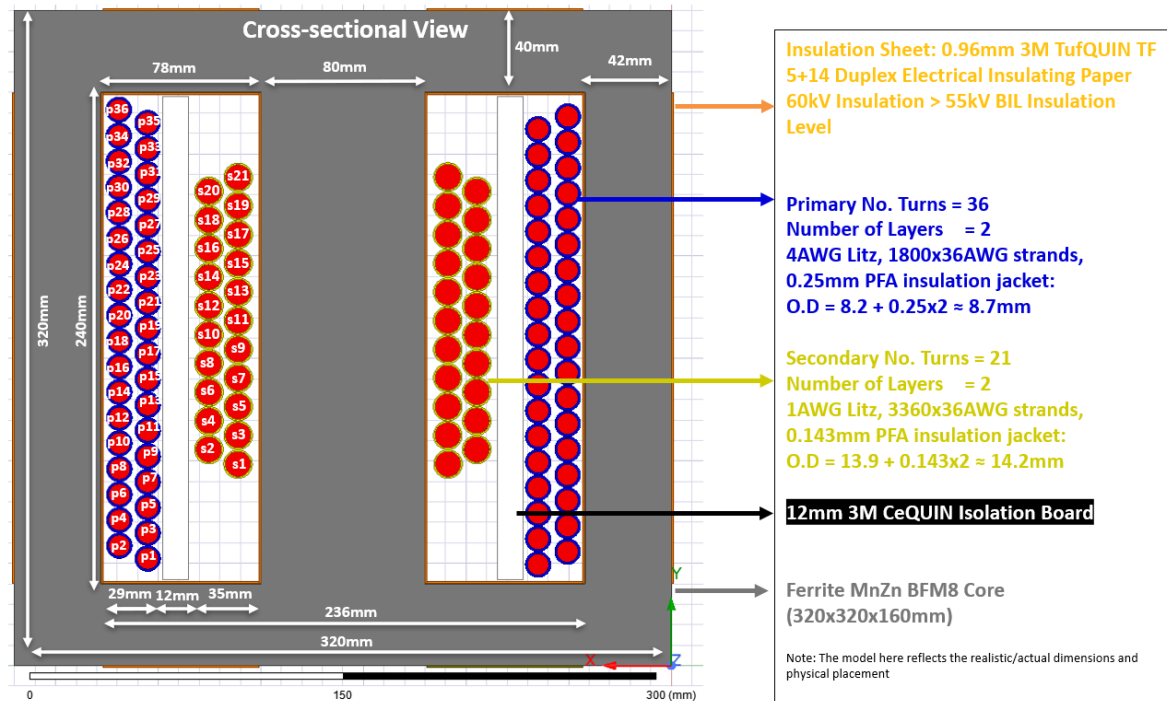


Fig. 5.2 Transformer cross-sectional view

Our circuit has been implemented using Ansys Simplorer for the purpose of simulating the

ANPC – 2level circuit, and the real Ansys Maxwell-3D transformer has been imported into this circuit for simulation purposes.

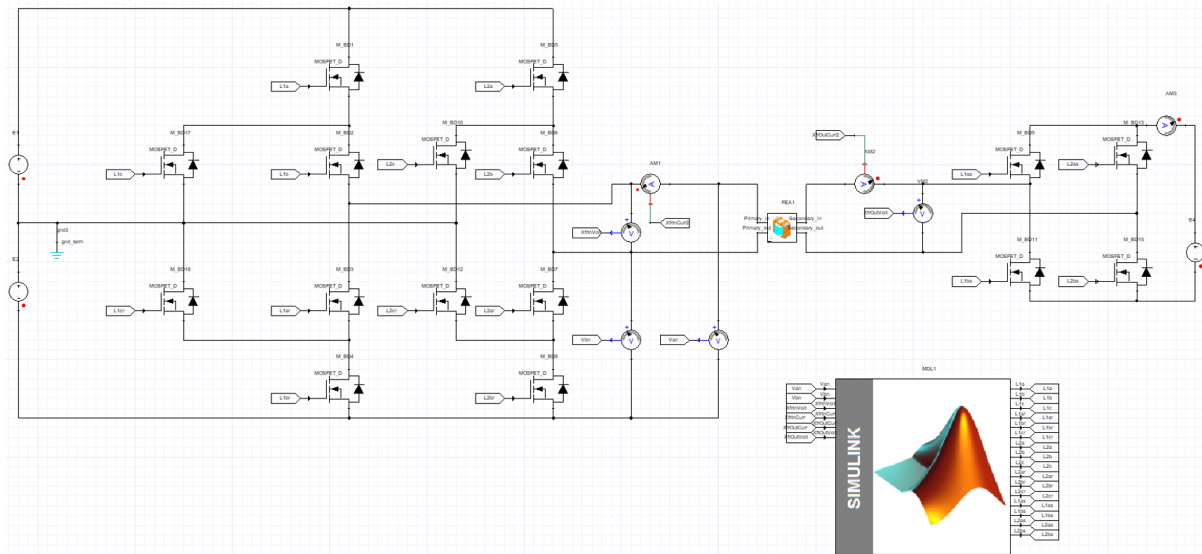


Fig. 5.3 Ansys Simplorer ANPC -2L circuit implementation

Simulink, which has been utilized throughout the process, is used to implement the algorithm that creates gate drive signals. This implementation generated the PWM signals that will be fed to Ansys Simplorer circuit in a real-time co-simulation between the two software programs (Fig. 5.4).

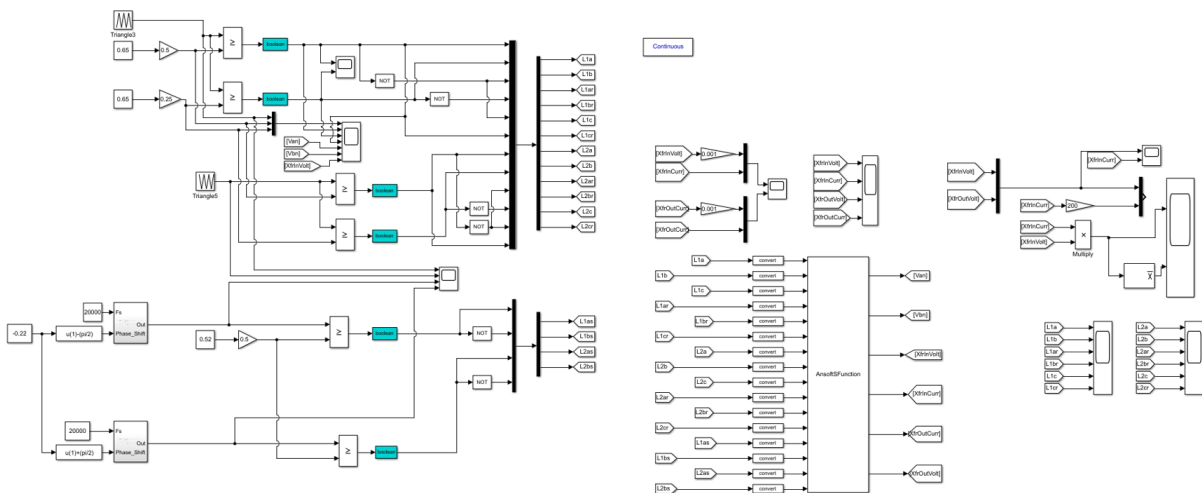


Fig. 5.4 Simulink PWM generation

To simulate the entire system, we combine Ansys Maxwell, Simplorer, and Simulink into a single simulation environment. By doing so, we are able to model not only the electromagnetics and transients of the system, but also the actual voltages and currents that occur at the 3- and 2-levels simultaneously with the transients. To the best of the author's knowledge, no other works in the literature offer such a novel and exhaustively detailed form of extensive simulation. The simulation accurately represents the real-world physical system and is extremely detailed (Fig. 5.5).

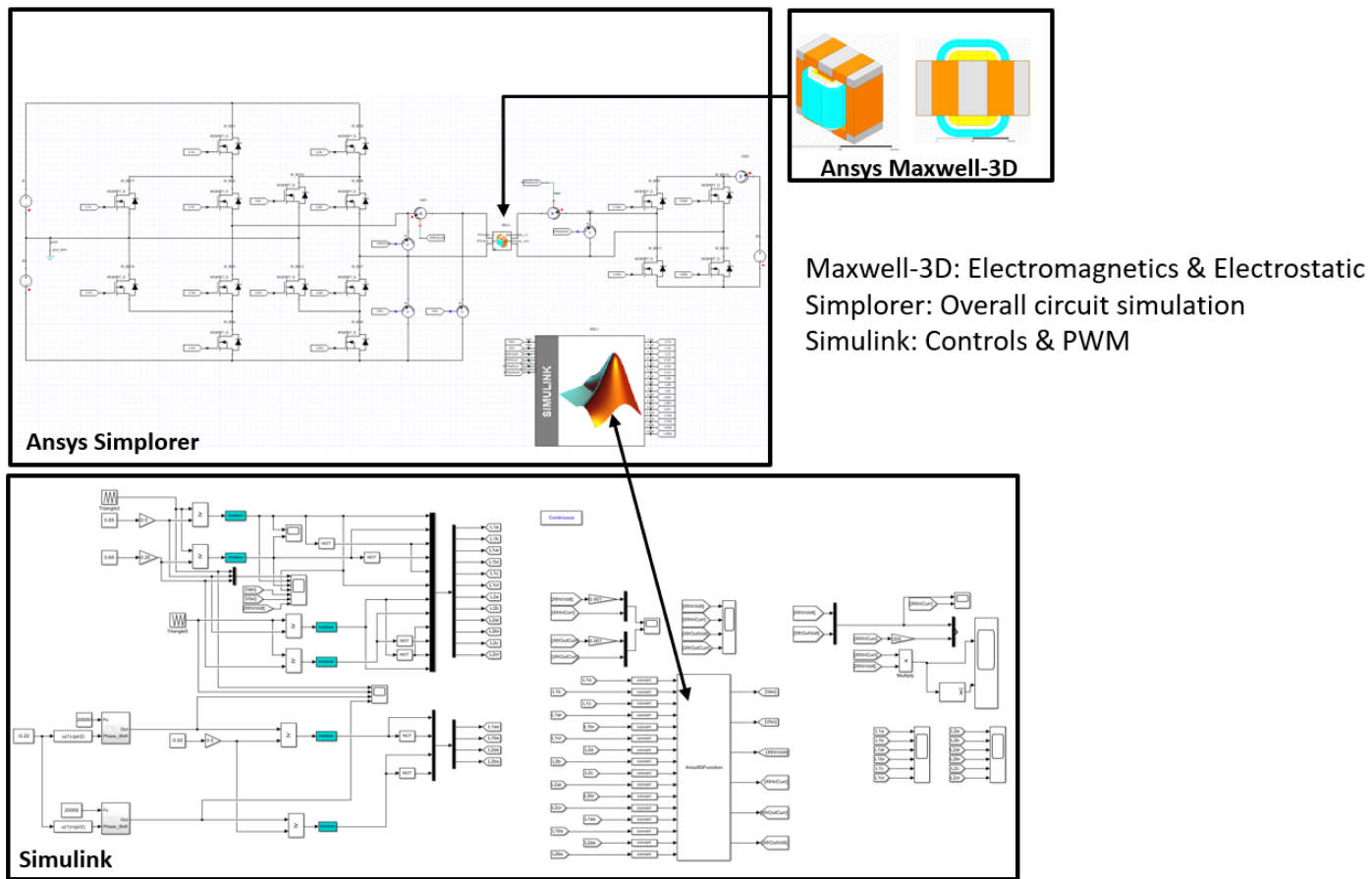


Fig. 5.5 System level transient co-simulation

The steady-state voltage and current results are as expected, with the primary voltage at 13kV 3-level (shown in green) and the secondary voltage at 7.2kV 2-level (shown in red), as well as the phase shift between them to which 700kW is pushed given the proper design of

leakage inductance around 200 to 250uH. The orange and blue lines in the diagram stand for the primary and secondary currents, respectively (Fig. 5.6).

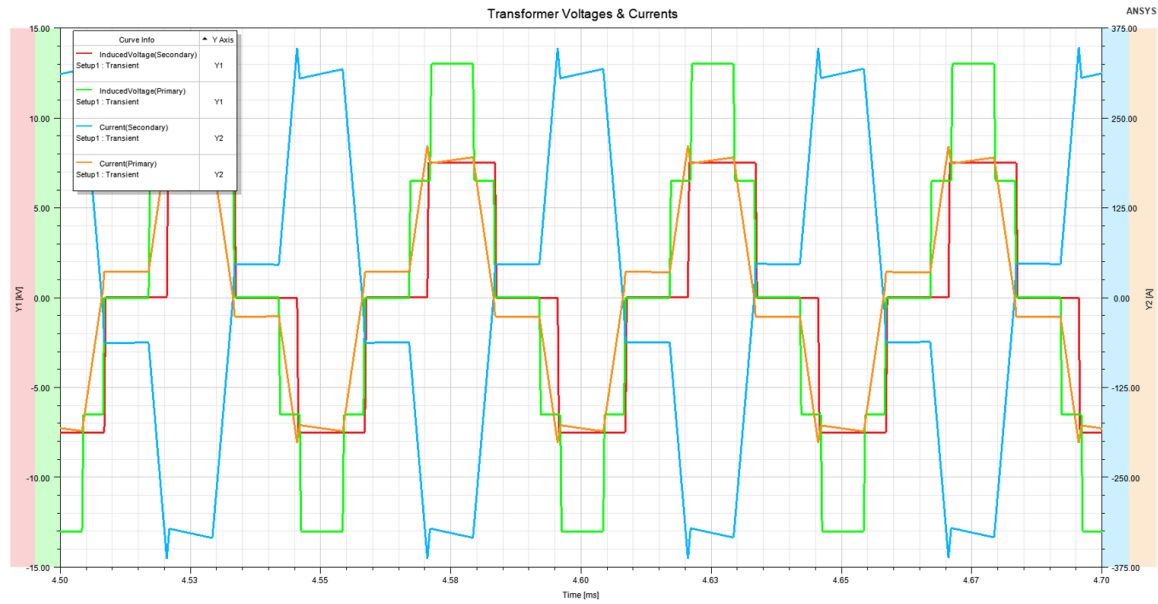


Fig. 5.6 Voltages and currents waveforms

The total losses calculated were as follows: 475 watts from the core (hysteresis and eddy currents) and 920 watts from the copper (DC and AC losses) (including proximity and skin effects due to the simulation of real litz wires with the specific number of strands and diameters). The total power loss was about 1.4 kilowatts. 99.8 percent efficiency has been achieved, which is quite high considering the type of application and the operating levels in hand (Fig. 5.7).

Satisfying the maximum flux density constraint, we can see that a maximum of around 0.3-0.35T is reached, avoiding core saturation given that the actual transients and voltage waveforms are simulated at 20kHz. This matched our initial constraint of around 0.3-0.35T operation region, on which we based our calculations (Fig.5.8).

Core loss (eddy + hysteresis) = 475W
 Copper AC (proximity + skin) + DC loss = 920W } Total loss \approx 1400W

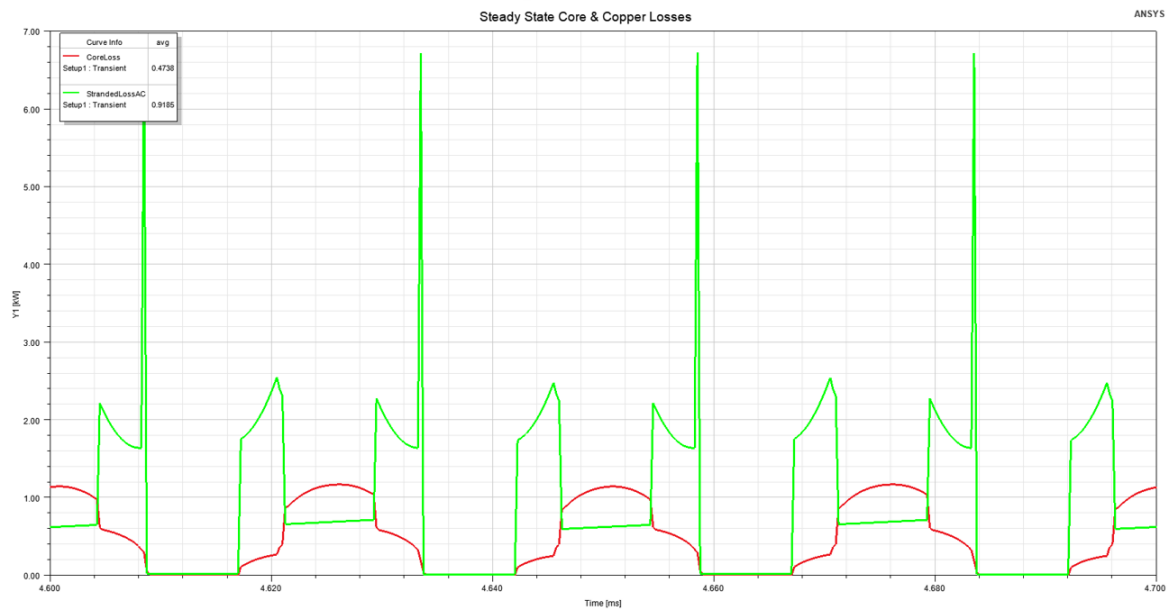


Fig. 5.7 Core and copper losses

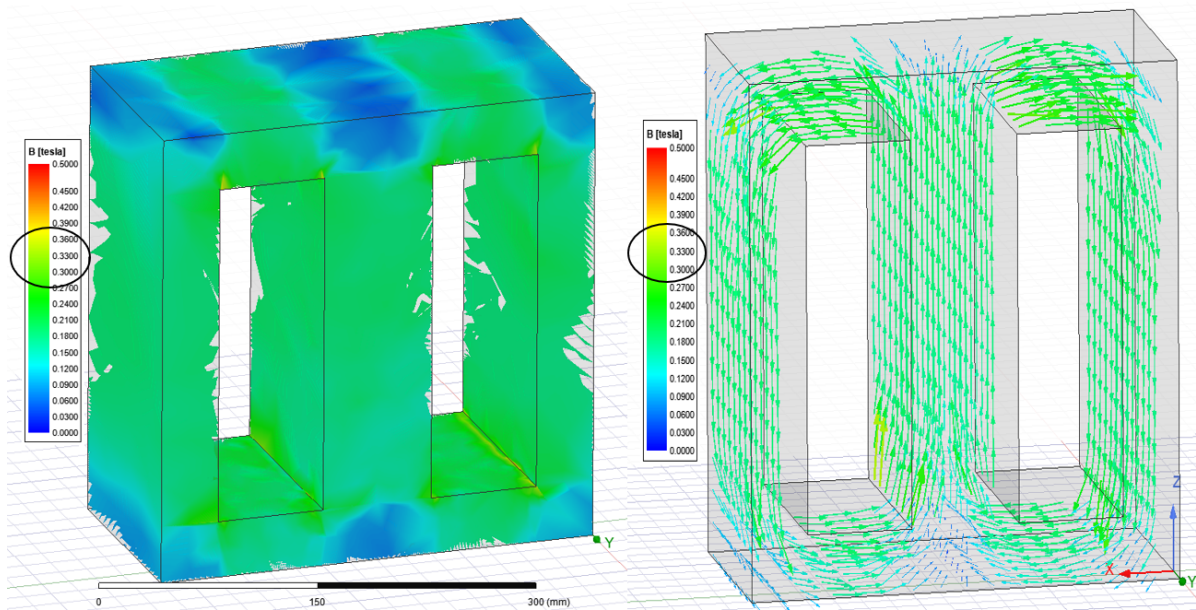


Fig. 5.8 Peak flux density

5.2 Electrostatic Ansys Simulation

Another type of FEA simulation that was carried out was electrostatic simulation. This will give us the e-field distribution across the transformer at different points. The designed and calculated 12mm isolation between the primary and secondary layers kept the kV/mm between the primary and secondary layers at a low level. The maximum e-field within the layers, as shown here, reached 5.4kV/mm, resulting in air breakdown. What is the reason for this? Because a standard layer-by-layer winding configuration is used here, the potential difference between p1 and p36 is greater than 12kV, and given the very short distance between, the E field at that point is very high (Fig.5.9).

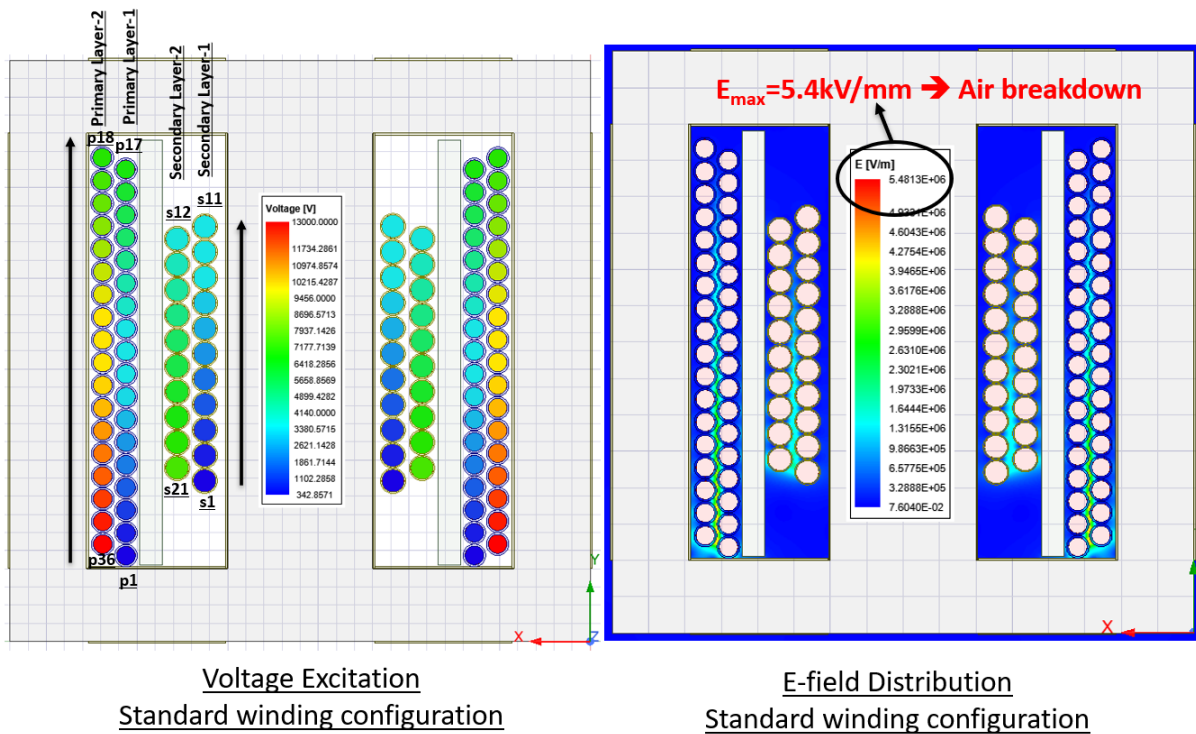


Fig. 5.9 Electrostatic simulation - 1st winding configuration

To address this, a flyback winding configuration has been modified, as shown on the left-hand side figure. This equates the potential difference between each consecutive adjacent turn, so for example, the potential difference between each consecutive turn for the primary is

13kV/36, which is minimal when compared to the previous configuration, which had a potential difference of more than 12kV between the first and last turn cable. Running the simulation confirms the benefit of this configuration, and the maximum e-field in the transformer is now around 1.5kV/mm, which is between the primary and secondary and was originally designed for in the insulation slides (Fig.5.10).

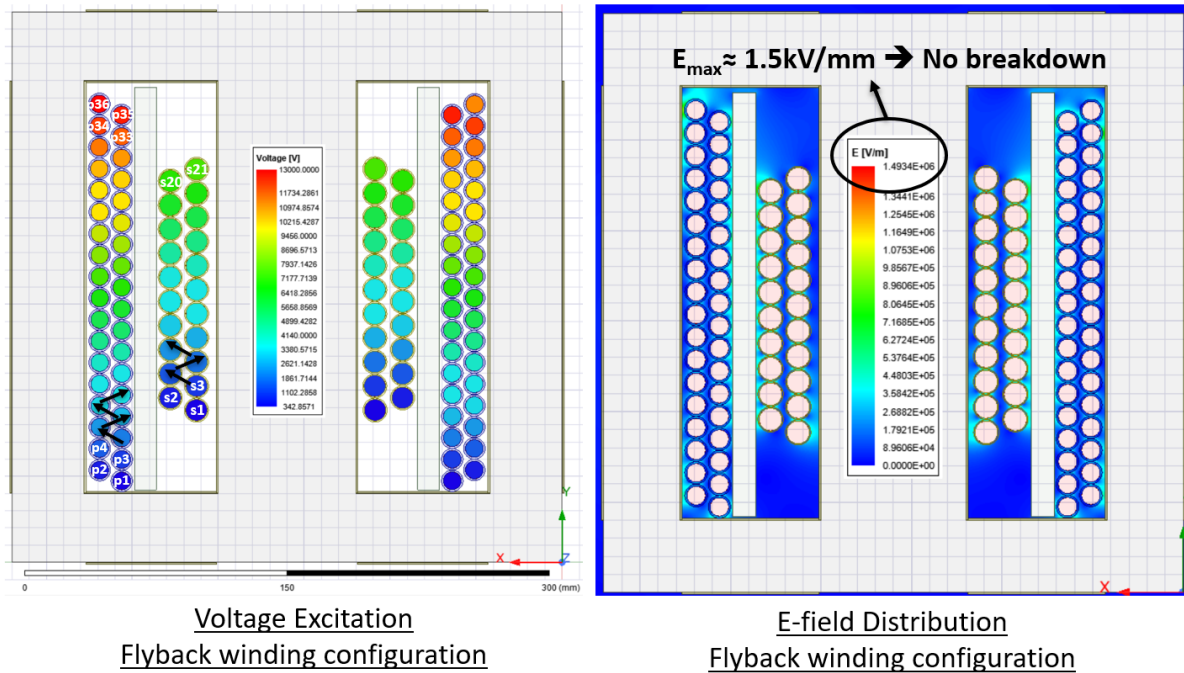


Fig. 5.10 Electrostatic simulation - 2nd winding configuration

5.3 Thermal Ansys Simulation

An identical transformer assembly is modeled in Maxwell 2D. The loss components derived from FEM are used as input for CFD analysis in Fluent. When each turn per layer is modeled as an individual heat source, configured model would represent actual heat transfer process most accurately but at the expense of heavy computational burden and simulation run-time. Temperature distribution of core and windings at steady-state under rated load is being worked on along Ansys Fluent FEA simulation and will be reported in a future publication.

5.4 EMI PLECS/Simulink Simulation

5.4.1 Simulation Validation

To validate the CM analysis, a time-domain simulation was performed for the detailed MM model of the power system [93]. A PLECS blockset integrated into MATLAB Simulink is used, where the controls are created in Simulink and the electrical circuits are modeled in PLECS. A single-phase shift modulation scheme has been developed, where the switching frequency and duty cycles are predetermined, and then closed-loop controls are applied to determine the phase shift needed to achieve the desired power level. All of the CM voltage inputs to the model were determined analytically from the steady-state DM operating point of the system. This steady-state DM operating point can be seen at the transformer interface, where the voltages and currents are shown in Fig. 5.11.

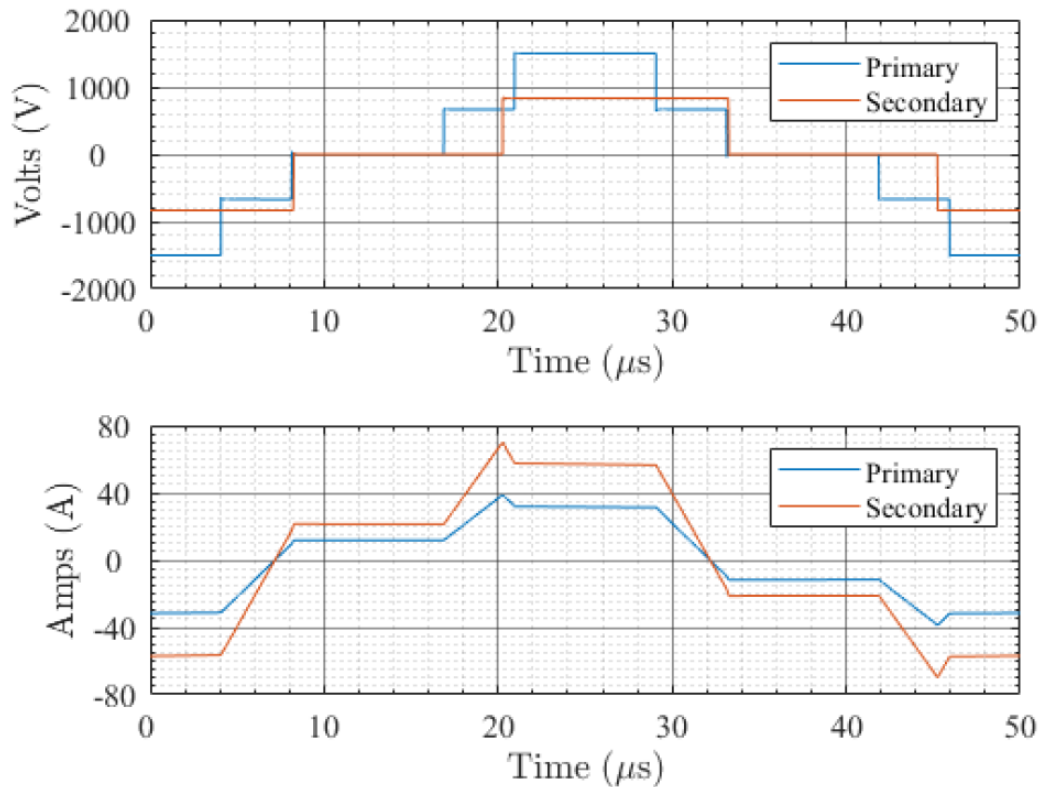


Fig. 5.11 Steady-state voltages (top), currents (bottom)

The CEM for the ANPC-FB and 2L-FB of the DAB have been validated, showing very accurate results of the displacement current through the heatsink for both the CM and MM models. The validation of the CEM is done for a system where every heatsink is grounded (Fig. 5.12) and floated (Fig. 5.13). In these figures, both the CEM and MM measurements line up exactly with no error between the two. From inspection, a grounded system produces the greatest amount of CM current with peak values at 0.8 Amps. CM current through the transistor base-plate can degrade power semiconductor module insulation, and by floating the heatsink we can limit the insulation stress on the devices. The CEM validation/measurements have verified this by reducing the peak currents and shortening the amount of time that the currents are flowing.

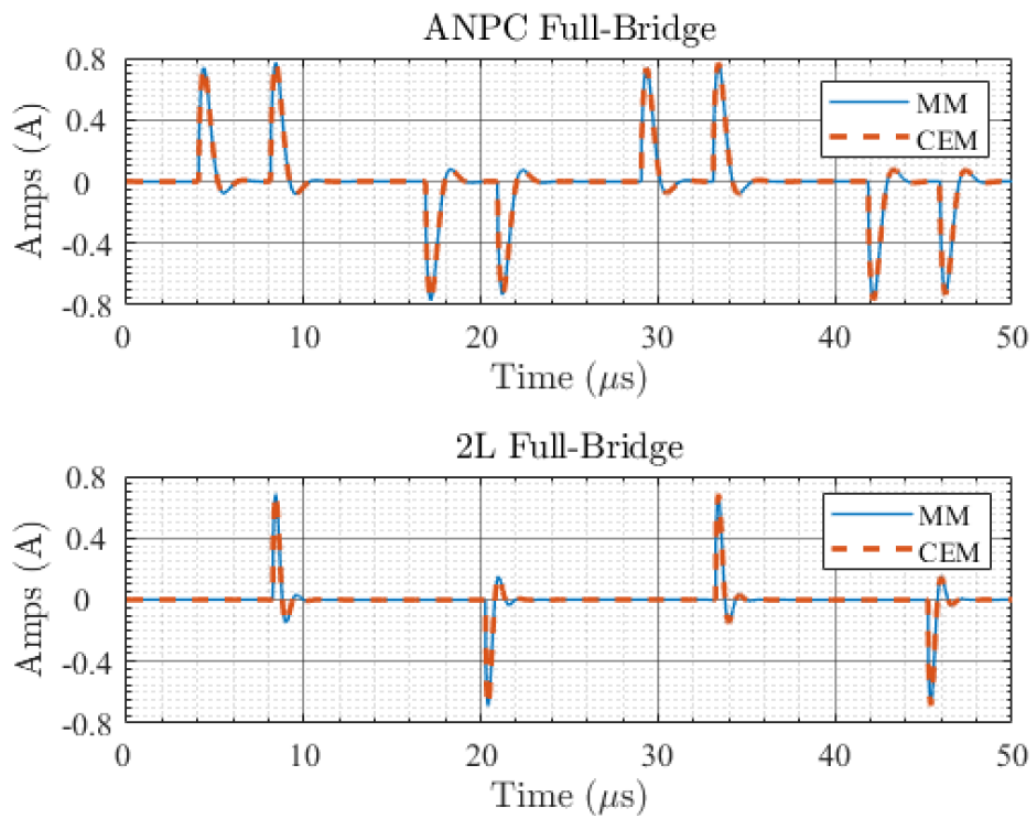


Fig. 5.12 CM validation, grounded heatsink

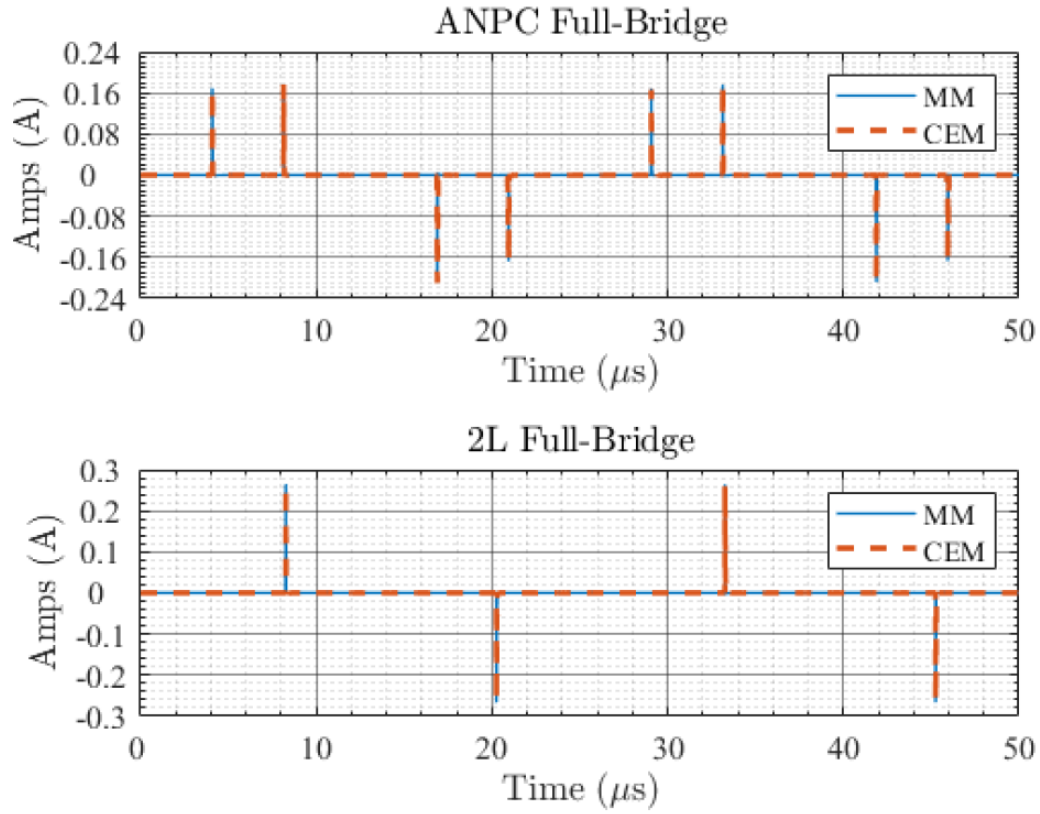


Fig. 5.13 CM validation, floated heatsink

While keeping the heatsink floated, a few CM mitigation efforts have been investigated for the ANPC-FB converter. The most significant method of decreasing the amount of CM displacement current through the heatsink into the ground potential was discovered by tying the neutral point of the ANPC-FB converter to the heatsink. This technique reduced the CM displacement current from amps down to a tens of micro amps, which resulted in a reduction with a few orders of magnitude. A plot of displacement current implementing this technique can be seen in Fig. 5.14. This method essentially shorts all parasitic capacitors seen by the neutral point of the ANPC, which makes up for about 25 percent of the total parasitic paths. Mathematically, this reduces the DM coupling into the CM circuit and reduces the total parasitic capacitance.

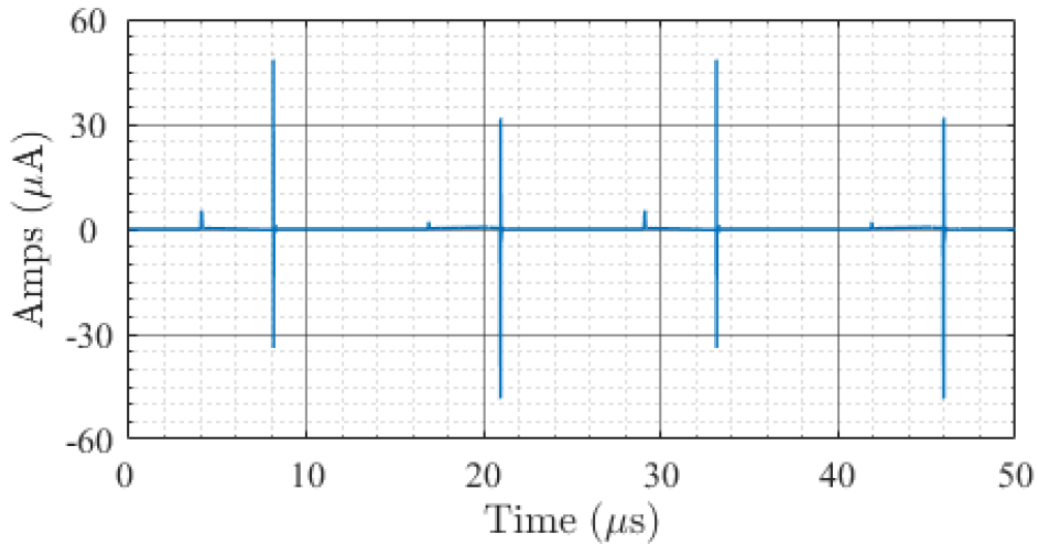


Fig. 5.14 ANPC CM current, neutral clamped heatsink

To the author's knowledge and the tools provided, it is difficult to float the transformer and provide parasitic paths for CM validation in simulation. This necessitates the need for validation of the transformer using hardware.

5.4.2 Hardware Validation/EMI Characterization

The HF characterization, transformer CEM, and impacts of heatsink grounding on CM currents will be validated and verified using all SiC MOSFET power modules. The 2L-FB and ANPC half-bridge (ANPC-HB) building blocks are used to construct the full system consisting of 1.7kV SiC MOSFET power modules (HT-3234-R-VB) from CREE. Both Double Pulse Test (DPT)s and pump-back tests have been performed to validate the effectiveness of the ANPC converter. DPT was performed at 2.4kVdc bus and 400A load current. In the DPT, the module under test withstood 1.2kVdc.

To successfully characterize the conducted emissions, a multi-step process needs to be followed. First, the parasitic capacitance of the switching module is extracted, this is required to accurately model the conducted emissions. Secondly, the full system is broken into multiple

stages, with each stage having a controlled CM path through LISNs. Finally, multiple tests are performed to measure the conducted emissions and validate the CEMs.

The custom-designed EMI characterization platform uses an unconventional configuration of LISNs on both the input and output of the system. This configuration allows observation of the conducted emissions generated, and by taking the difference of the input and output CM currents, the displacement current into the ground can be determined. The stages of testing are performed in this order: 2L-FB, ANPC-HB, ANPC-FB, some intermediate step using both full bridges, and the DAB. Each stage will allow for the converter to be placed on the ground plane of the test platform with the LISNs connected to the input and output. The impacts of grounding and floating the heatsink on conducted emissions are studied. For the ANPC converters the impact of a floating neutral clamped heatsink on conducted emissions will be characterized in future work. Once both the 2L-FB and ANPC-FB have been characterized separately, the penultimate stage utilizes both full-bridges as calibrated parts of the EMI test and characterization platform, without introducing any additional CM paths. The final stage, also to be performed in future work, will allow validation of all assumptions regarding the transformer CEM, including the model developed in this paper. Once this final step is completed, the future aim is to integrate a validated MF transformer CEM into full system design processes that provide insight into the impacts of conducted emissions compliance and assurance of robust self-compatibility. Fig. 5.15 shows the final EMI test and characterization environment.

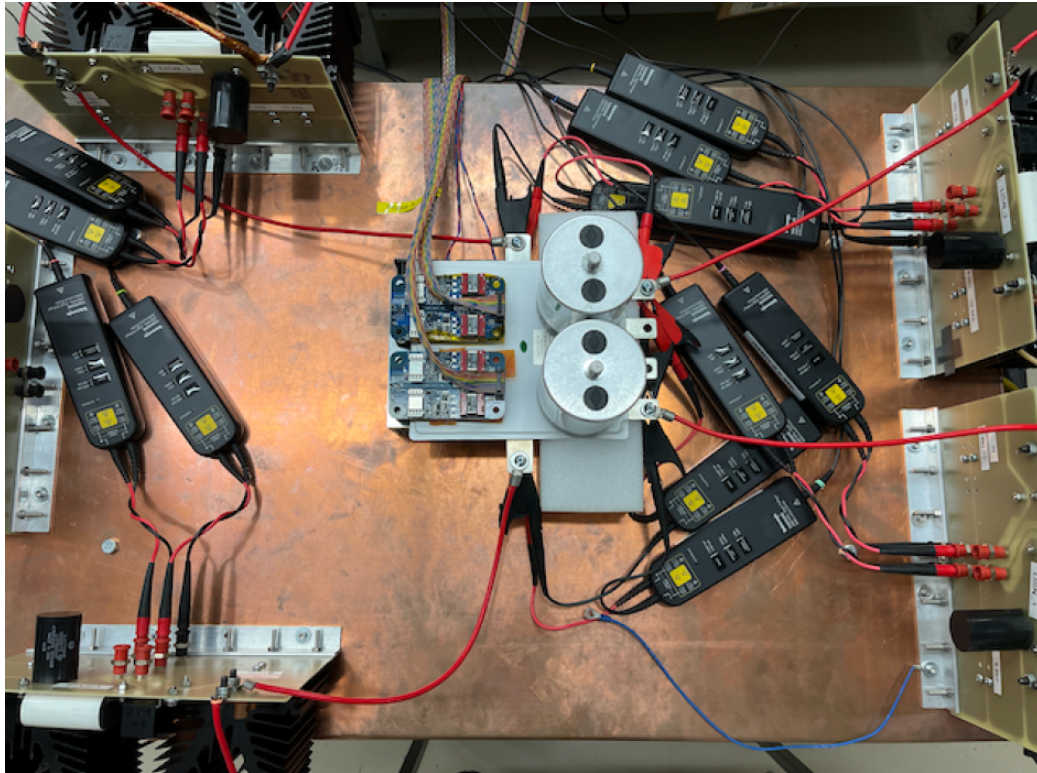


Fig. 5.15 Two-level full-bridge converter on EMI characterization platform

5.4.2.1 Two-Level Full-Bridge Converter Characterization

The EMI conducted emission of the 2L-FB is characterized by a methodology demonstrated in [95]. As shown in Fig. 5.15, the unfiltered full-bridge is configured as a 500V inverter, where the MOSFETs legs are switching at 20kHz, 50% duty cycle, with a bipolar scheme. It is terminated with a set of custom-made MIL-STD LISNs from the dc-side, and a set of artificial networks from the ac-side. Both the LISNs and the artificial networks have calibrated common-mode paths, therefore, ensuring an accurate common-mode measurement in frequency up to 30MHz. The in-situ voltage measurements on LISN measurement ports provide the waveforms necessary for EMI characterization of the full-bridge under test.

Fig. 5.16 and Fig. 5.17 present the EMI characterization results of the unfiltered full-bridge in time-domain and in frequency-domain. The results show that the common-mode EMI component is dominating the lower frequency between 10kHz to 1MHz and the differential mode

component is dominating the higher frequency. In this configuration, no obvious cross-mode coupling can be observed from the EMI spectrum. The estimated parasitics of the MOSFET modules shows close-to-symmetric pole-to-chassis parasitic capacitances, which explains the absence of the cross mode coupling effects.

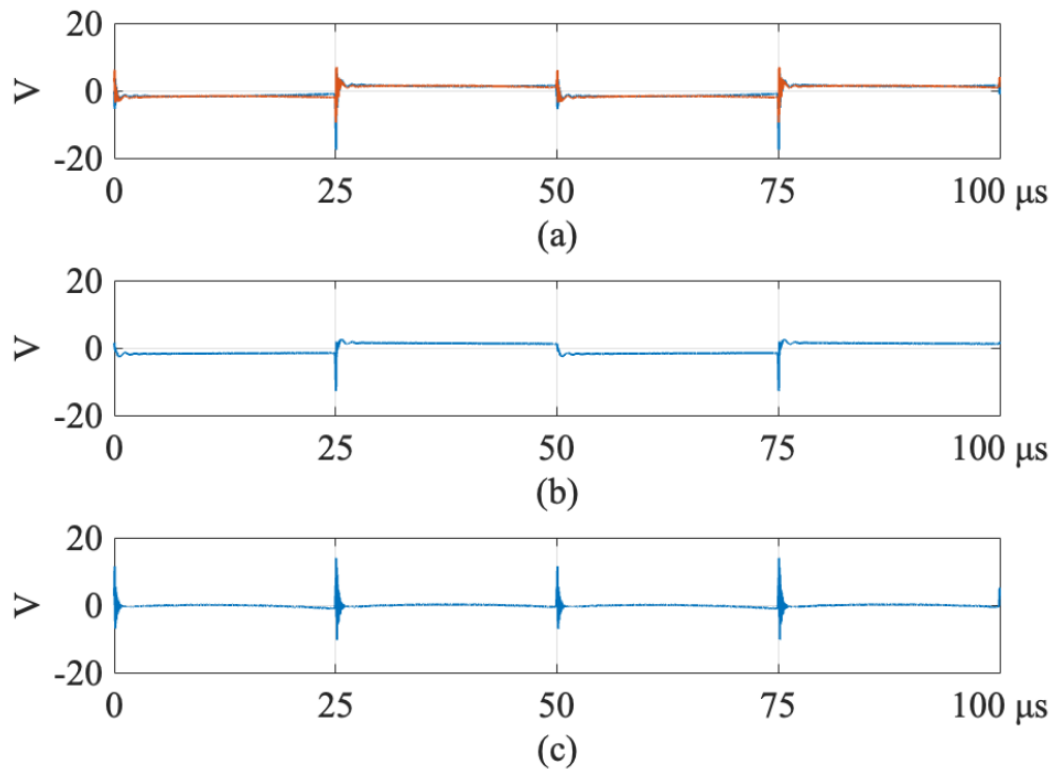


Fig. 5.16 Two-level full-bridge converter EMI characterization in time-domain. (a) mixed-mode (DC+ and DC-), (b) common-mode, (c) differential-mode.

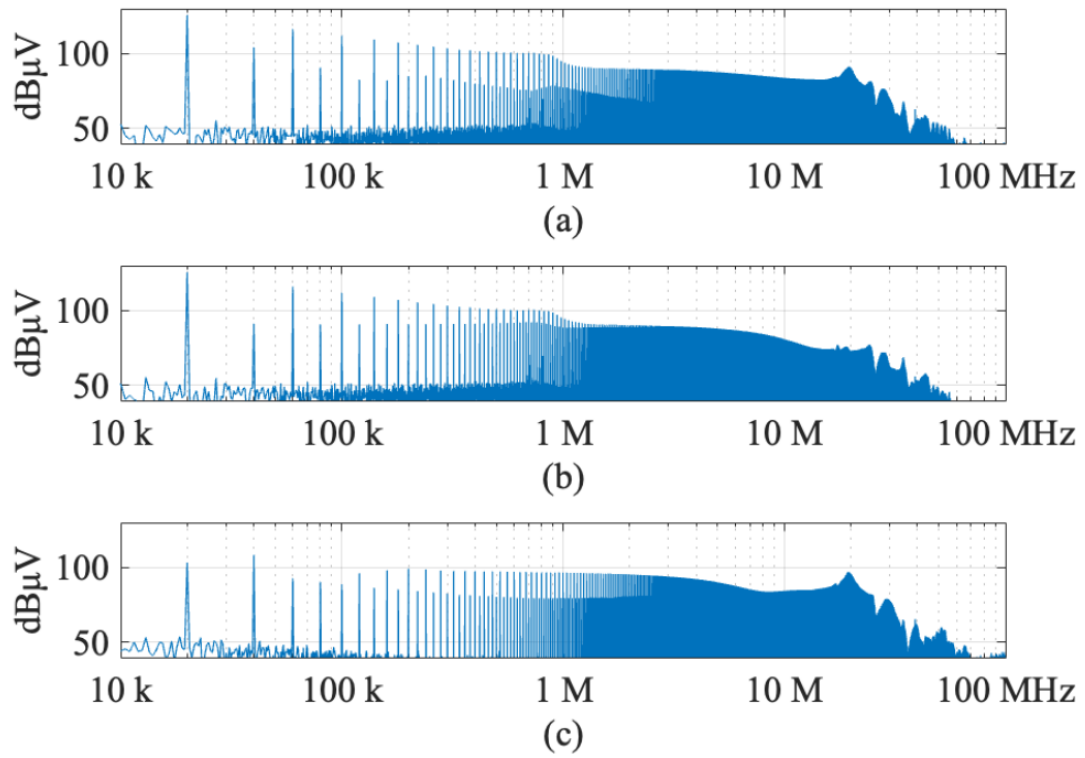


Fig. 5.17 Two-level full-bridge converter EMI characterization in frequency domain. (a) mixed-mode, (b) common-mode, (c) differential-mode.

5.5 Prototype Build and Testing

The flyback winding configuration necessitates extensive work during the transformer construction process. Because it is common practice to use lower voltage layers first and higher voltage layers at the outer layers, you can see that we begin with two secondary layers, then an isolation distance of 12 millimeters, and finally two layers of primary at the outer layer. The transformer measures 32 cm in width, 32 cm in height, and 38 cm in diameter. A 13/7.2kV 20kHz 700kW transformer has a power density of 18kW/L, whereas a 2.4/0.8kV 70kW 60Hz transformer has a power density of 0.252kW/L, demonstrating the benefits of high frequency transformer technology. In this case, high-frequency transformer technology clearly results in a much smaller transformer (Fig. 5.18).

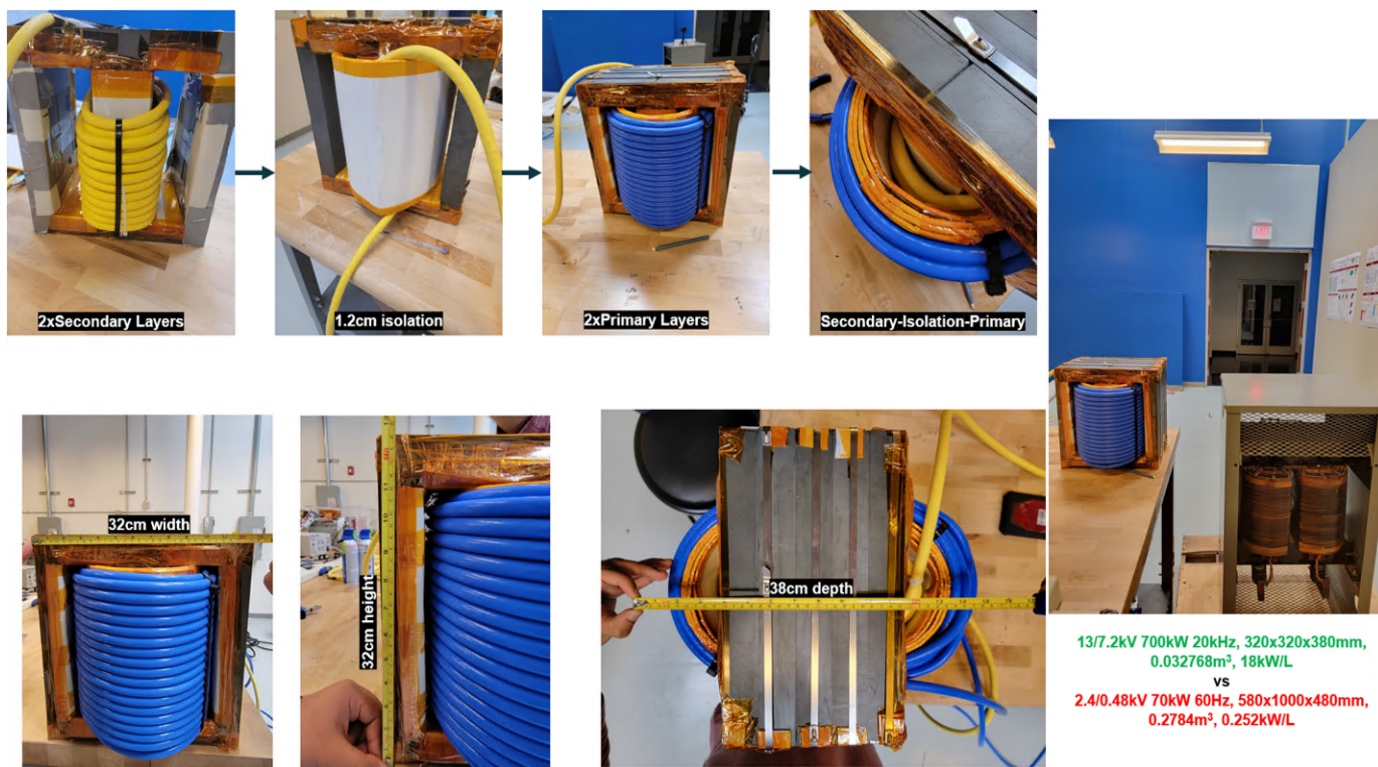


Fig. 5.18 Transformer Prototype

The following are the tests that must be performed at low frequency (60Hz) level:

a) 500 Vdc Insulation Resistance (IR)

b) DC HiPot test: 28 kV for the primary side (13 kV) and 16 kV for the secondary side (7.2 kV)

c) BIL test: 55kV for 13kV and 39kV for 7.2kV

d) 1 minute Applied Voltage Test: 30kV low frequency test

e) Partial Discharge

On the other hand, the high frequency tests to be conducted after building the converter:

a) dv/dt test will be performed using the following parameters: 1kV at 150kHz as opposed to 7.2kV at 20kHz

b) Full current test: 93A at 20kHz

c) Induced Voltage Evaluation (7200 cycles)

For the low frequency tests, insulation resistance tests, also known as IR tests for short, and DC Hipot tests were performed successfully. Furthermore, the transformer was transported to a high voltage testing facility to undergo BIL, applied voltage, and partial discharge tests. In terms of high frequency testing, prototypes of 10kV modules and gate drivers are currently being developed and tested. The plan is to begin purchasing and assembling the power converter stage until the high frequency testing is completed; this includes the busbar, DC link caps, cold plates, and other components.

To begin the IR tests, the transformer was connected to an 80kV HiPot tester (PTS-80) (Fig. 5.19). We began with a 500Vdc voltage applied between the various transformer components, namely the primary to the secondary and ground (Fig. 5.20), the primary to the secondary (Fig. 5.21), the primary to the ground (Fig. 5.22), the secondary to the primary and ground (Fig. 5.23), and the secondary to the ground (Fig. 5.24). The measured leakage current is extremely low, and the measured resistance is in the mega-ohm range. After concluding satisfying IR

testing results, a HiPot voltage was applied to the primary by gradually increasing the voltage by 5kV for ten seconds at a time until it reached 30kV, which was maintained for one minute (Fig. 5.25). The primary HiPot passed the test because there was no insulation breakdown or spark recorded, as well as because the measured leakage current recorded was $0.3\mu\text{A}$, which is lower than the mA passing range. Following the same procedure, a 16kV HiPot voltage test was performed on the secondary side (Fig. 5.26), with a $0.2\mu\text{A}$ leakage current recorded. This shows that the transformer passed the HiPot test without insulation breakdown, and it is now ready to go through the BIL test, as well as the stress applied voltage test and the partial discharge test. The testing results will be presented in future publications.

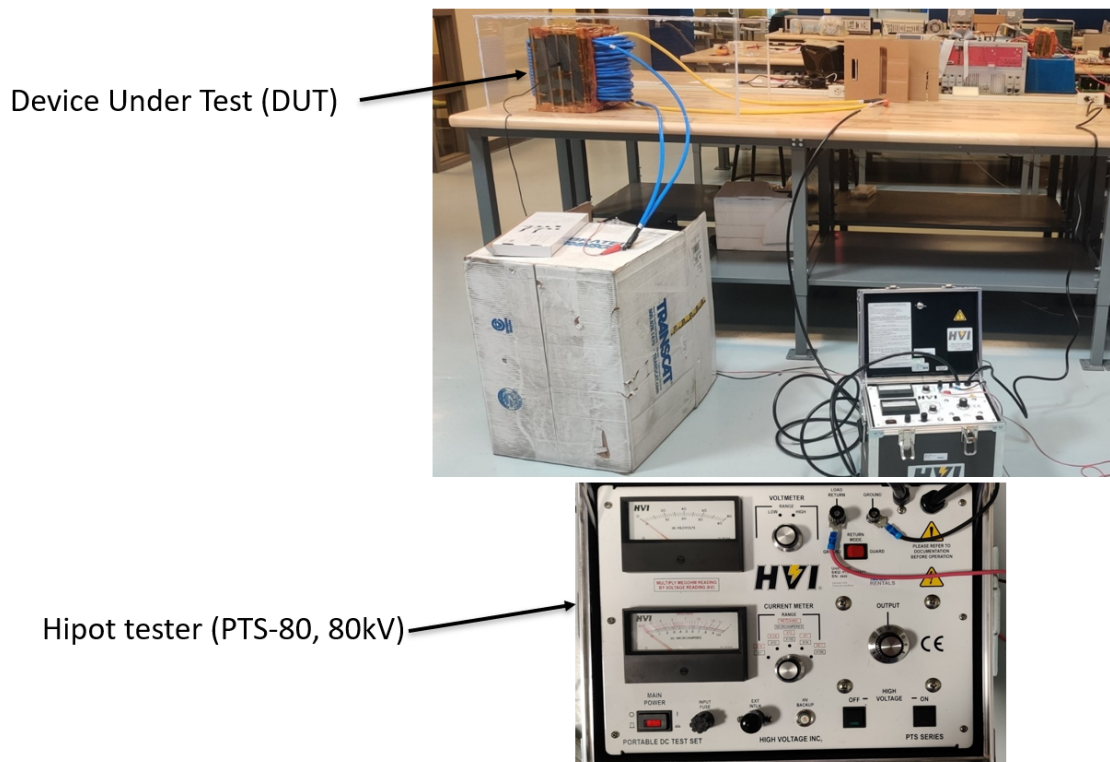


Fig. 5.19 Transformer connected to 80kV HiPot tester

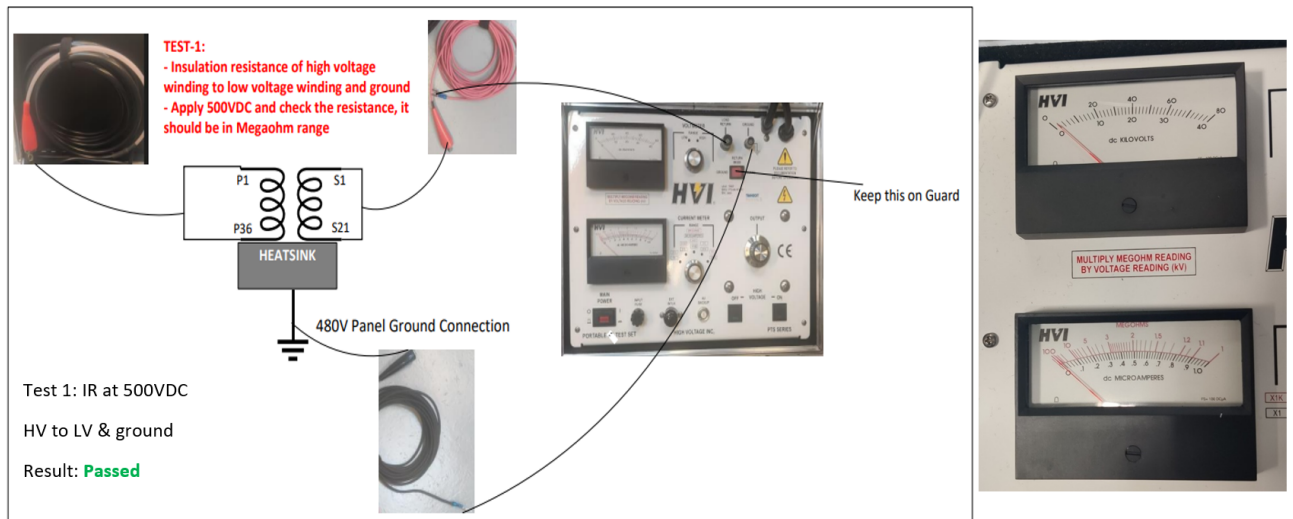


Fig. 5.20 IR: primary to secondary and ground

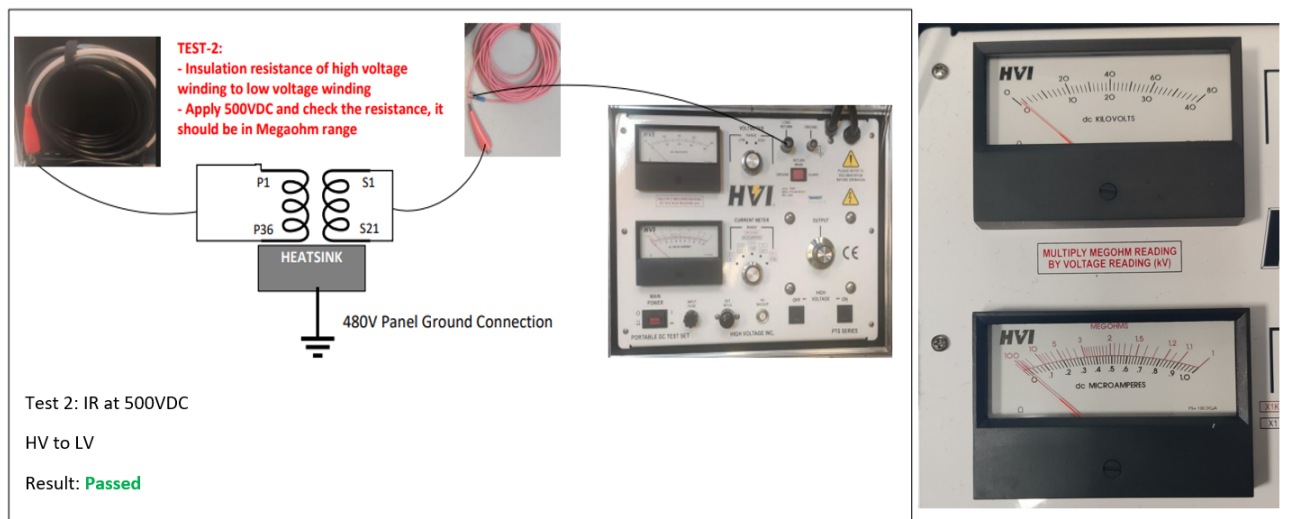


Fig. 5.21 IR: primary to secondary

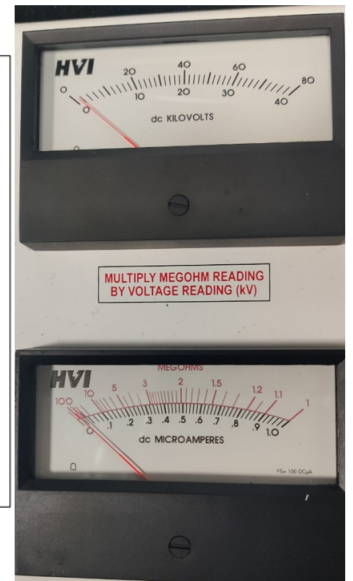
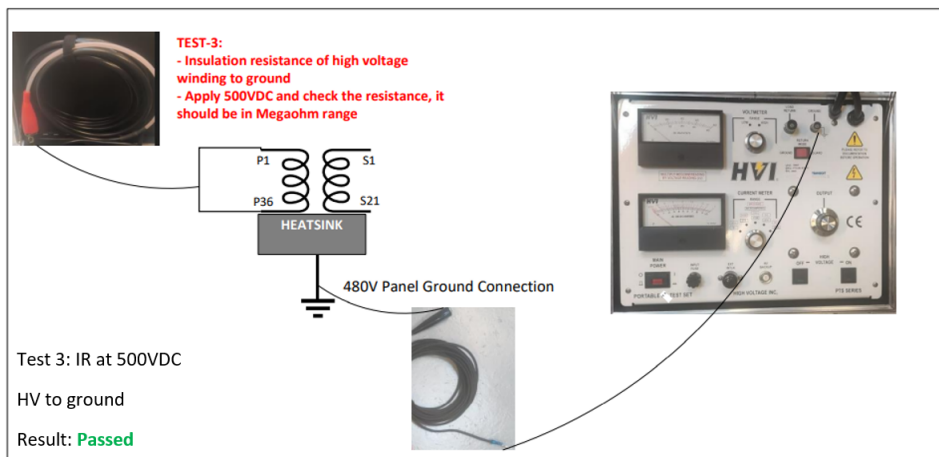


Fig. 5.22 IR: primary to ground

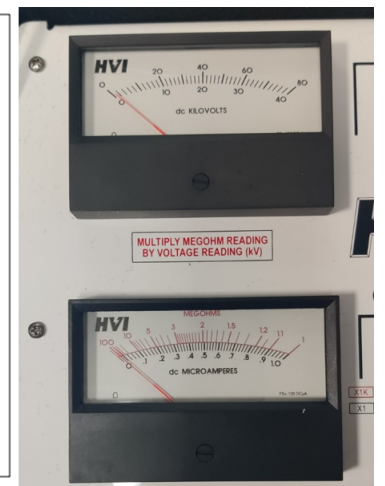
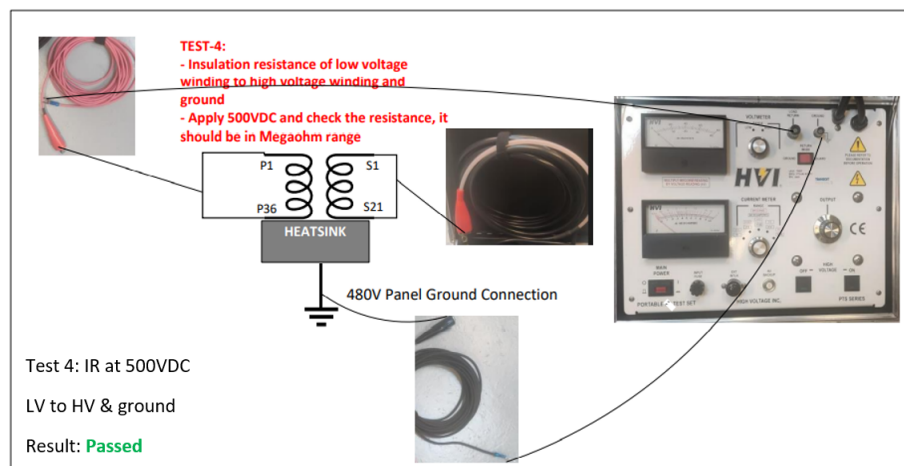


Fig. 5.23 IR: secondary to primary and ground

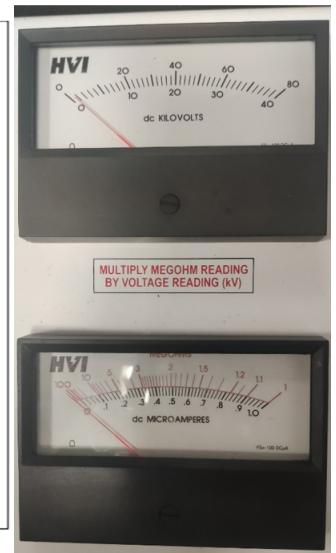
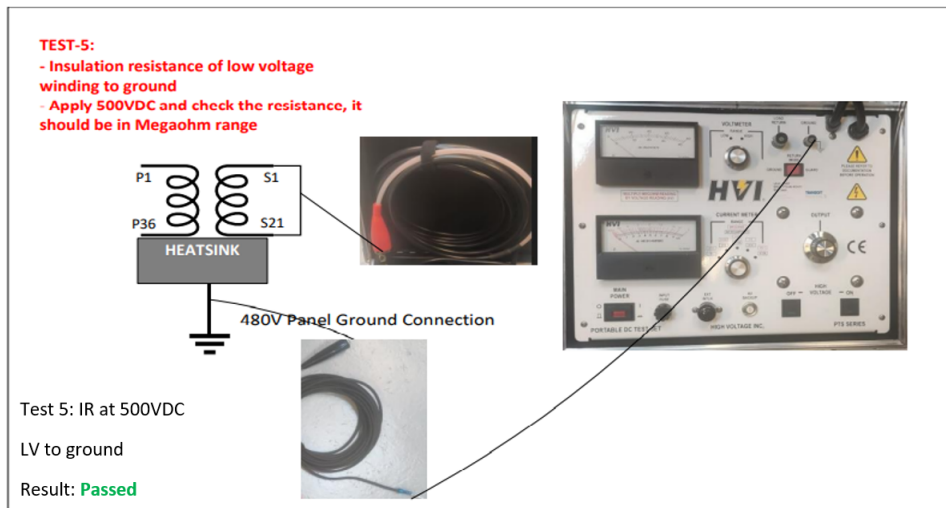


Fig. 5.24 IR: secondary to ground

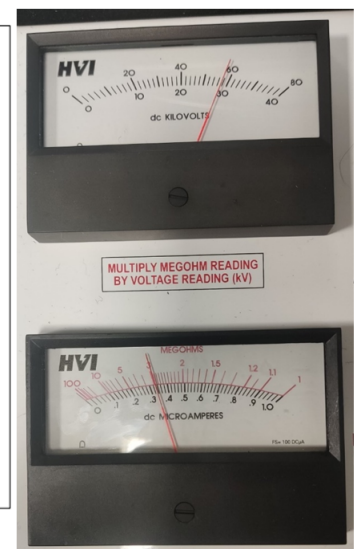
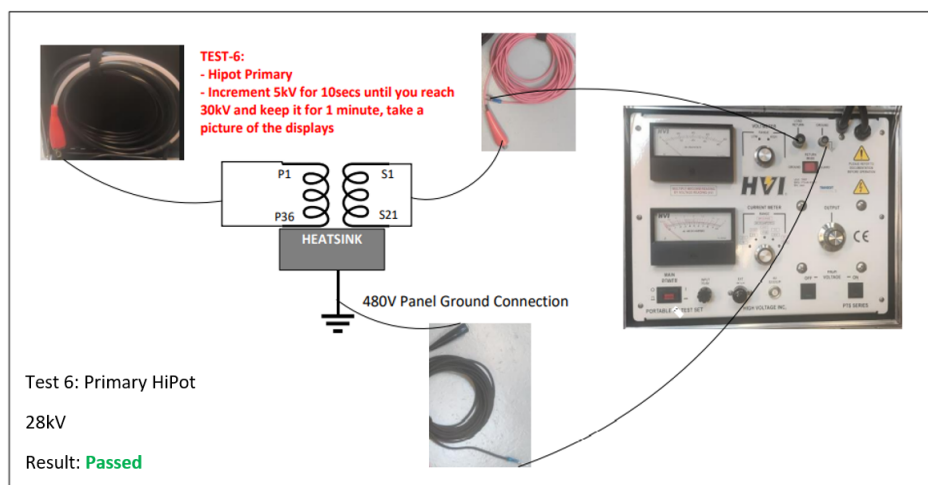


Fig. 5.25 Primary HiPot test

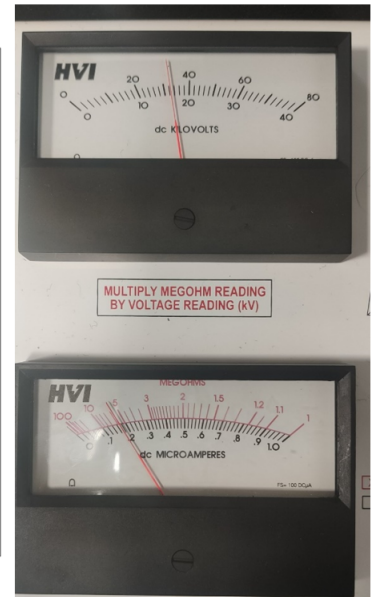
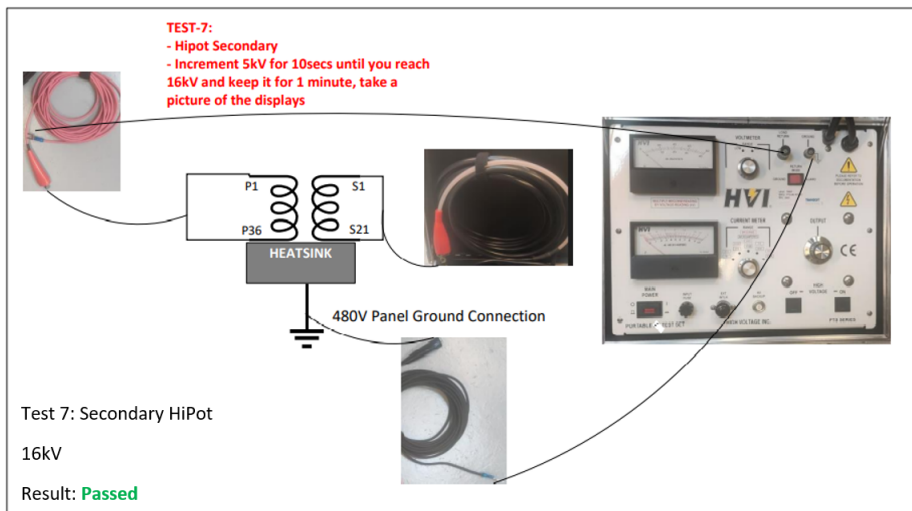


Fig. 5.26 Secondary HiPot test

CHAPTER 6

Conclusion and Future Work

The proposed work is centered on the creation of a dual active bridge with high power, medium voltage, and medium frequency control. By providing a more power dense, cost-effective, and efficient solution, this architecture addresses the shortcomings of existing modular systems. This topology is investigated for the first time on a 700kW system connected to a 13kVdc input to generate 7.2kVdc at the output with a 20kHz switching frequency. It investigated the use of 10kV SiC modules and gate drivers in an active neutral point clamped to two level dual active bridge converter. A comprehensive transformer design that employs a multi-physics approach that addresses all magnetic, electrical, insulation, and thermal aspects were prioritized. The transformer is designed and tested to ensure the viability of the system.

As for the future recommended work, we need to build the power converter and do system level testing in which we can find potential customers. We would like to investigate the effect of field grading and apply the proper mitigation solutions to our transformer so the transformer can go into production phase and not just a lab prototype. Finally, carrying out a detailed transformer thermal modeling and buying the proper epoxy with liquid cooled plates to cover all the transformer sides, and then test at the rated system current and voltage levels once the 10kV SiC modules are tested and ready for utilization.

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1. A. E. Shafei, S. Ozdemir, N. Altin, G. Jean-Pierre and A. Nasiri, "A High Power High Frequency Transformer Design for Solid State Transformer Applications," 2019 8th International Conference on Renewable Energy Research and Applications (ICRERA), 2019, pp. 904-909, doi: 10.1109/ICRERA47325.2019.8996515.
2. G. Jean-Pierre, N. Altin, A. El Shafei and A. Nasiri, "Efficiency Optimization of Dual Active Bridge DC– DC Converter with Triple Phase-Shift Control," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), 2020, pp. 1217-1222
3. G. Jean-Pierre, M. Khayamy, N. Altin, A. E. Shafei and A. Nasiri, "A Triple Phase-Shift Based Control Method for RMS Current Minimization and Power Sharing Control of Input-Series Output-Parallel Dual Active Bridge Converter," 2020 IEEE Transportation Electrification Conference and Expo (ITEC), 2020, pp. 550-555
4. A. El Shafei, S. Ozdemir, N. Altin, G. Jean-Pierre and A. Nasiri, "Design and Implementation of a Medium Voltage, High Power, High Frequency Four-Port Transformer," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), 2020, pp. 2352-2357, doi: 10.1109/APEC39645.2020.9124337.
5. G. Jean-Pierre, A. El Shafei, N. Altin and A. Nasiri, "A Multiport Bidirectional LLC Resonant Converter for Grid-Tied Photovoltaic-Battery Hybrid System," 2019 8th International Conference on Renewable Energy Research and Applications (ICRERA), 2019,

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6. A. El Shafei, S. Ozdemir, N. Altin, G. Jean-Pierre and A. Nasiri, "A Complete Design of a High Frequency Medium Voltage Multi-Port Transformer," 2019 8th International Conference on Renewable Energy Research and Applications (ICRERA), 2019, pp. 761-766, doi: 10.1109/ICRERA47325.2019.8997088.
 7. G. Jean-Pierre, N. Altin, A. E. Shafei and A. Nasiri, "A Control Scheme Based on Lyapunov Function for Cascaded H-Bridge Multilevel Active Rectifiers," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), 2020, pp. 2021-2026, doi: 10.1109/APEC39645.2020.9124234.
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 9. A Multiport Bidirectional LLC Resonant Converter for Grid-Tied Photovoltaic-Battery Hybrid System. A Nasiri, G Jean-Pierre - International Journal of Renewable Energy Research, 2020.
 10. S. Beheshtaein et al., "An Optimal Design of a Hybrid Liquid/Air Cooling System for High Power, Medium Frequency, and Medium Voltage Solid-State Transformer," 2021 IEEE 12th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2021, pp. 1-8, doi: 10.1109/PEDG51384.2021.9494251.
 11. Jean-Pierre, G.; Altin, N.; El Shafei, A.; Nasiri, A. Overall Efficiency Improvement of a Dual Active Bridge Converter Based on Triple Phase-Shift Control. *Energies* 2022, 15, 6933. <https://doi.org/10.3390/en15196933>
 12. S. Ozdemir, N. Altin, A. E. Shafei and A. Nasiri, "Parameter Selection of an LLC Res-

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13. A. El Shafei, S. Ozdemir, N. Altin, G. Jean-Pierre and A. Nasiri, ”Development of a Medium Voltage, High Power, High Frequency Four-Port Solid State Transformer,” in CES Transactions on Electrical Machines and Systems, vol. 6, no. 1, pp. 95-104, March 2022, doi: 10.30941/CESTEMS.2022.00013.

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Curriculum Vitae

Education

PhD in Electrical Engineering: University of Wisconsin – Milwaukee

- Advisor: Prof. Adel Nasiri
- Degree Focus: Power Electronics
- Minor: Control Systems
- January 2017 - December 2022

BE. Electrical and Computer Engineering, American University of Beirut

- Honors
- September 2009 - June 2013

Work Experience

Eaton Research Lab (ERL), (Menomonee Falls, WI): July 2022 - Current

- Full-time Lead Electrical Engineer – Power Electronics and Solid-State Transformers

Imagen Energy LLC (Milwaukee, WI): 2021

- 100kW AC/DC Compact Power Converter
- 100kW Resonant DC/DC EV Fast Charging Converter
- 250kW AC/DC Compact Power Converter
- Compact High Power Direct Medium Voltage Solar PV Inverter

Eaton Research Lab (ERL), (Menomonee Falls, WI): 2019-2020

- Medium Voltage Extreme EV Fast Charging Converter

Imagen Energy LLC, (Milwaukee, WI): 2018

- 150kW Inverter for Grid-Tie Application
- 500kW, 2000Hz Inverter for High Speed PMSM Applications

Power Electronics Lab, UWM (Milwaukee, WI): 2017-Current

- 13/7.2kV, 700kW, 20kHz Solid State Transformer
- 7.4/0.4/0.4/0.4kV, 100kW, 50kHz Four-ports Solid State Transformer
- 0.4/3.4kV, 25kW, 30kHz Solid State Transformer
- 1/1kV, 330kW, 50kHz Solid State Transformer
- 170/400V, 3kW, 50kHz Solid State Transformer

Consolidated Contractors Company Ltd (CCC), Sultanate of Oman: 2013-2016

- Oil and Gas field electrical design and electrical construction work
- RHOP Gas Plant Electrical and Instrumentation Material Focal Point
- South Oman Oil and Gas 132kV Substation work

Consolidated Contractors Company Ltd (CCC), Doha, Qatar: Summer 2012

- Electrical Work at New Doha International Airport

Teaching Experience

- Teacher Assistant (TA) for Electro-mechanical Energy Conversion (UWM)
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- Teacher Assistant (TA) for Signals and Systems (AUB)