A Circuit-Level SPICE Modeling Strategy for the Simulation of Behavioral Variability in ReRAM

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***Abstract*— The intrinsic behavioral variability in resistive switching devices (also known as "memristors" or "ReRAM devices") can be a reliability limiting factor or an opportunity for applications where randomness of resistance switching is essential, such as hardware security and stochastic computing. The realistic assessment of ReRAM-based circuits & systems towards practical exploitation requires variability-aware ReRAM modeling. In this context, here we present a versatile, circuit-level implementation strategy to incorporate cycle-to-cycle (C2C) variability to the ReRAM model parameters in SPICE simulations. We evaluated the proposed approach with threshold-based models of a voltage-controlled bipolar ReRAM device and managed to reproduce the main features observed in experimental curves for different pulsed voltage inputs. With key upgrades, compared to previous approaches found in the literature, our strategy enables the enhancement of any ReRAM device model towards the exploration of new ways to make the most of the C2C ReRAM variability, and to test the robustness of any designed circuits & systems against ReRAM variability.**

Keywords— memristor; resistive switching device; ReRAM; modeling; simulation; cycle-to-cycle variability; LTSpice.

I. Introduction

Technology of resistive switching devices (also referred to as "memristors" or "ReRAM devices") is continuously maturing. Some companies have already released commercially available discrete and crossbar-organized devices [1]. Likewise, ReRAM products continuously attract important investments [2], [3] as ReRAM technology is becoming a strong candidate for high-density storage arrays and novel in-memory computing systems [4]. The data stored in resistive memory cells are represented by their resistance; logic '0' by a high resistive state (HRS) and logic '1' by a low resistive state (LRS), or vice versa. In bipolar ReRAM devices, one voltage polarity is required to switch the device from HRS to LRS (SET process), and the opposite polarity is required to get the cell from LRS to HRS (RESET process). Robust ReRAM devices with high resistive switching uniformity, along with good cycling (SET-RESET) endurance and fast switching are much desired properties for large-scale commercial exploitation. The development of compact device models contributed significantly to the progress of research in this field so far, being adequate to capture the experimentally observed behavior and demonstrate functionality and potential usefulness in applications [5], [6].

Nevertheless, one barrier still preventing their widespread practical use is variability. Using the same pulsing procedure to program a device several times from/to its HRS and LRS state, typically gives significantly different results due to cycle-to-cycle (temporal) variations. Temporal variations are attributed to the stochastic nature of resistive switching, which is very hard to tackle at the material level and causes constraints on operation, reliability and scalability of the circuits. Variability characteristics show significant dependence on the oxide material according to [7]. With inherent variability at the heart of ReRAM switching performance, inclusion of this characteristic in any compact model has gained considerable interest lately to obtain realistic simulation curves in circuit simulation environments which will allow a realistic assessment of ReRAM-based circuits. A time series analysis technique was presented in [8] to describe temporal variability in long cycling sequences using an autoregressive model. Many more relevant works can be found presenting different approaches to this challenging problem [9]-[12]. Designing simple subcircuit components to enrich results of SPICE simulations are a key issue, given the existing tradeoff between accuracy and simulation length when a large number of devices are involved. In this context, a versatile approach to incorporate stochasticity in model parameters was introduced in [13] where a Verilog-A description was presented and applied to the threshold-type switching ReRAM model proposed in [5].

In this context, here we build upon such work to present a compact circuit-level implementation strategy to incorporate temporal variability to any ReRAM model parameters of interest in SPICE simulations. We verified the proposed approach using different threshold-based ReRAM models of the literature and managed to reproduce the features observed in experimental curves for different pulsed voltage inputs in LTSpice simulations, while also presenting key upgrades to the original description of [13]. Our solution enables the enhancement of any compact ReRAM device model towards the exploration of new ways to embrace and make the most of the temporal ReRAM variability, and to test the robustness of any designed circuits & systems against ReRAM variability.

II. Variability Modeling and Simulation Setup

Based on the work presented in [13], in this section we provide a simple *circuit-level strategy* on how variability can be included in certain ReRAM model parameters. We focus on threshold-type ReRAM models as this type of switching is an extremely important and common feature of such devices. One such behavioral model was proposed in [5] and has been widely used ever since, even with further enhancements [6]. It accepts the definition of asymmetric switching thresholds V_{SET} * V_{RESET} and different switching rates for the SET and RESET ($\beta_{SET} \neq \beta_{RESET}$) processes. Figure 1 shows the internal dynamics of the model and curves with the resistance

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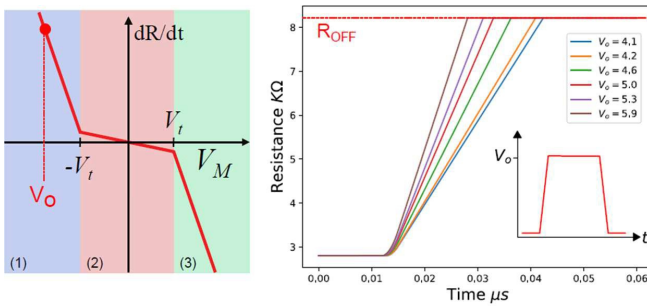

Fig. 1 (a) Graph indicating the dependence of the ReRAM device switching rate on the applied voltage V_M. (b) *R-t* curves showing state evolution towards the HRS (R_{OFF}) boundary by applying voltage pulses of different amplitude V_o. Model parameter values [5]: R_{ON} = 2800Ω, R_{OFF} = 8200Ω, SET/RESET threshold v_t = 2.2V, α = 0 and β = 1e11.

evolution during RESET, for voltage pulses of different amplitude. Higher pulse amplitudes result in faster switching (likewise in the SET process) because the resistance change-rate is proportional to the difference between the instantaneous applied voltage V_M and the switching threshold (V_{SET} or V_{RESET}).

In threshold-type voltage-controlled models, the resistance change is initiated once the SET/RESET threshold has been reached. Thus, the simplistic approach presented in [13] to induce stochasticity in simulations consisted in a Verilog-A model for the variability of the switching point, able to be integrated within any of the established threshold-type models. The central idea of their approach relied upon modifying the SET/RESET threshold voltage value(s) depending on a certain probability calculated at every time step of simulation. More specifically, the method required picking a sample from a uniform random distribution U and comparing it with the probability of switching P (Poisson distribution), calculated at every time step. Whenever it is P>U the threshold voltage variable takes the value of the instantaneously applied voltage. Otherwise, it takes the default value. Such switching probability can be adjusted to experimental data after extracting the statistical information.

The Verilog-A implementation in [13] used internally available distribution functions which accessed the simulation timestep value. The latter is not accessible in LTSpice netlists and it is not fixed during simulation, given that the internal engine modifies the simulation timestep depending on the complexity of the simulated circuit. Moreover, LTSpice has limited capacity to generate pseudorandom numbers given that all readily available methods use the same seed value. These are some of the reasons that limit universality of the originally proposed implementation and applicability in SPICE-like simulation environments. Some further observations concern the fact that there were not any limiting values defined for the threshold voltage variable, meaning that it could instantaneously take any value depending exclusively on the applied input voltage.

For these reasons, we used a Python script to generate externally the numbers of the required distributions, based on specific user-defined parameters. Fig. 2 shows the block diagram resuming the interaction between user and the simulation flow. The user defines the circuit netlist including the ReRAM model parameters and the distribution parameters for the Python scripts which generate the input text files to be used in the LTSpice environment, the time interval between every pair of picked numbers stored in the text files, the total

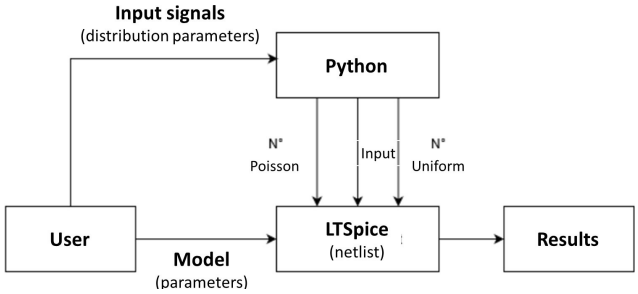

Fig. 2 Block diagram describing the user interaction with the simulation flow.

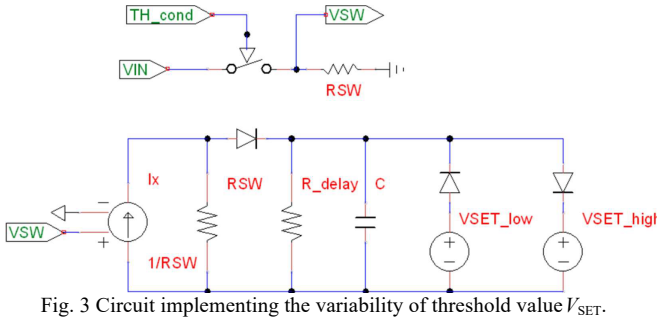

Fig. 3 Circuit implementing the variability of threshold value V_{SET}.

simulation time, the waveform for the voltage to be applied to the ReRAM devices(s), etc. The values in the input text files are used in LTSpice as data for controlled voltage sources.

Here we show how we successfully applied circuit-level strategies to model the variable threshold value for the same ReRAM model proposed in [5]. Unlike in Verilog-A implementations where different variables can be defined, in circuit-level modeling approaches we alternatively use signals to store the related information. Thus, we represented the threshold value as the voltage over a capacitor. We used the circuit shown in Fig. 3 to control its value over time during the simulation. This circuit corresponds to the SET threshold, whereas another instance should be used for the RESET threshold, if asymmetric thresholds are required.

The value range for the threshold voltage is defined by *VSET_low* and *VSET_high* with a diode clipping topology. We use a voltage-controlled switch where the control signal *TH_cond* (meaning *threshold condition*) allows applying the instantaneous voltage value applied to the ReRAM device (V_{IN}) at a certain moment to a resistor *RSW*. The *TH_cond* signal becomes logic "1" (causing a closed switch) whenever it is P>U. We use the Norton equivalent of the circuit composed by the *VSW* and the resistor *RSW*, thus having a voltage controlled current source circuit to charge the capacitor to the corresponding threshold voltage value. Moreover, the circuit includes a resistor *R_delay*, such that, when no external action is taken to modify the threshold voltage, its value decreases (discharge of the capacitor) towards the minimum value, which is also the default value for this parameter. With this we make sure that the threshold value will not be kept for too long at values near the high boundary when high voltages are applied, which could affect the behavioral characteristics of the device model. We use a diode for this reason and select *RSW* << *R_delay*, such that the capacitor can discharge through *R_delay* when the current source is not active, able to reach a minimum of *VSET_low*. For the reset threshold V_{RESET}, which has a negative value in bipolar devices, a similar circuit is used where the polarity of

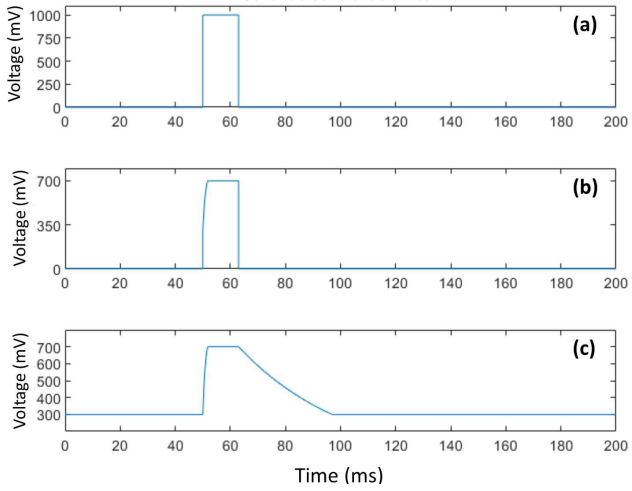

Fig. 4 Simulation results showing (a) the *TH_cond* signal, (b) the the *VSW* signal, and (c) the voltage across the capacitor.

the diodes and the current source has to be the opposite. It is worth mentioning that, even though here this modeling approach is applied to inject variability to the threshold voltage parameter, in fact the same principles can be used to incorporate variability to any of the model´s parameters.

III. Simulation Results

First, simulation results are shown to verify functionality of the circuit-level modeling approach. Circuit parameters were *RSW*= 1kOhm, *R_delay* = 40kOhm, *C*= 1uF, *VSET_low* = 0.3V, *VSET_high* = 0.7V, and input voltage pulse amplitude V_{IN} = 0.8V. The threshold parameter is initially set at the *VSET_low* value. We used ideal models for the diode components. In Fig. 4 we observe that whenever a stochastic event occurs, the *TH_cond* signal takes value "1" and *VSW* becomes equal to V_{IN} as the capacitor charges, whereas once the *TH_cond* signal returns to logic "0", the capacitor discharges towards *VSET_low* value. Using a small capacitance will result in small *RC* delay and fast charging times, which is desirable in this case.

Once circuit behavior was verified, we next simulated the SET process based on the ReRAM model of [5] while applying a positive voltage ramp to the device reaching from 0V to 0.8V in 40ms. We particularly used the Poisson and the Uniform distributions and fixed the script parameters to obtain a success probability (i.e., the probability to have P>U) of 2.25%. We initialized the ReRAM device at R_{OFF} = 100kOhm. Fig. 5a shows the simulation results. We purposely left a 2-ms range at the beginning with 0V input to verify that the device was properly initialized. Finally, the input voltage is kept at 0.8V during aprox. 10ms, being higher than the maximum SET threshold value by 100mV. We observe that once the device reaches the minimum resistance value at aprox. 35ms, then no further switching occurs in its resistance, thus the current follows the applied voltage. Compared with previous simulation in Fig. 4, here we used *C* = 10 pF, *R_delay*= 100 MOhm, and the ReRAM model parameter β_{SET} =1e8. Moreover, we observe that the switching rate of the device is variable and the results qualitatively resemble experimental results commonly seen in relevant published works, such as in [6] and [14] for commercial memristors by *Knowm Inc*. For clarity, we included in the simulation results the response of the device when the effect of variability was ignored. Fig. 5b shows the time evolution of the threshold value during the

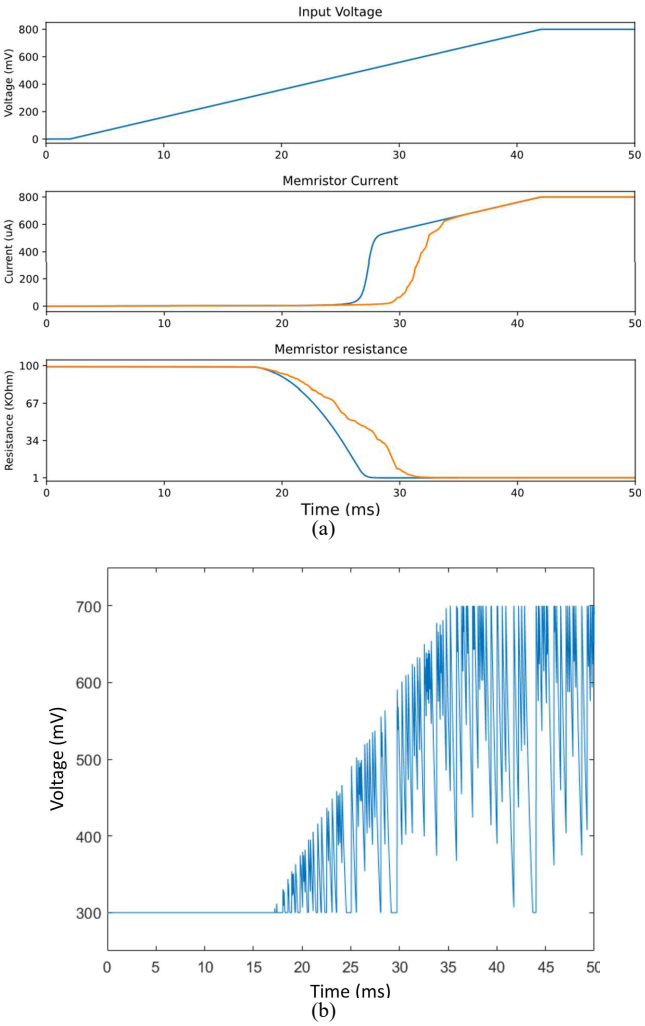

Fig. 5 Simulation results for the SET process based on the ReRAM model of [5]. (a) From top to bottom, the plots show the applied ramp voltage, the current through the device and its resistance, either with (orange) or without (blue) variability, distinguished with different line colors. (b) The time evolution of the value of the SET threshold parameter of the model.

simulation. We observe that whenever a switching event occurs (P>U), the threshold parameter is assigned the value of the applied voltage, which explains why the form of the threshold curve follows the input voltage ramp. It is worth mentioning that the resistance change rate is proportional to the difference V_{IN}-$V_{SET/RESET}$, so the larger this difference, the larger the change in the resistance and thus in the current curve of Fig. 5a.

Moreover, we successfully applied the same technique to other memristor models of the literature. In Fig. 6 we show simulation results for the model presented in [15] by Yakopcic *et al*., which is also a threshold-type model but it belongs to the category of hyperbolic sine models. Compared to the model in [5], it supports nonlinear LRS and HRS boundary states and can certainly capture richer switching dynamics. Parameter values for the model were as follows: *a1*=0.013, *a2*=0.0129, *b*=0.068, *Vp*=0.17, *Vn*=0.12, *Ap*=2500, *xo*=0.5, *An*=4000, *xp*=0.3, *xn*=0.6, *alphap*=1, *alphan*=5, and *eta*=1. Here variability was applied to both SET/RESET thresholds *Vp* and *Vn*. The aforementioned values for these parameters were the default values and the minimum values at the same time. Circuit parameters were selected as follows: *Vp_high*=0.50, *Vn_high*= 0.3, and *R_delay*= 50MOhm.

The simulation scenario consisted of consecutive SET-RESET cycles with pulsed input voltage. The applied SET/RESET pulses were 10/1-ms wide and their amplitude was 500mv (700mV) for SET (RESET). The time separation between consecutive pairs of numbers picked from U and P distributions was here set at 2us, to improve the quality of simulation results with much more events per second. For comparison reasons, we show in the same plots the results obtained with and without variability. SET threshold values range between *Vp* and *Vp_high*, as expected. We observe that when ignoring variability, the current evolution follows the expected trajectory based on the model´s equations. However, with variability applied, the device response in every consecutive SET pulse follows a different and less predictive trajectory with stochastic events, which is typically observed in experimental measurements on real ReRAM devices.

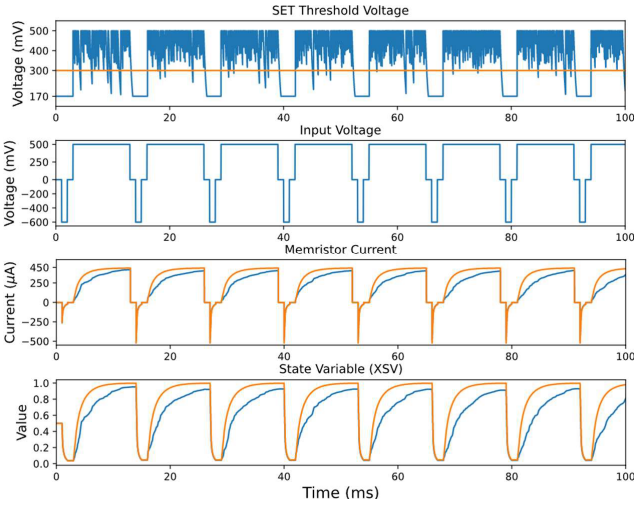

Fig. 6 Simulation results for the SET-RESET process based on the ReRAM model of [15]. From top to bottom, the plots include the situation with (blue) and without (orange) variability, distinguished with different color. They show the SET threshold value, the applied input voltage, the current through the memristor and the value of the state variable of the model, ranging between 0 and 1. SET threshold value was set to 0.3V when no variability was concerned.

IV. Conclusions and Future Work

In this work, the netlist of two voltage-controlled threshold-type ReRAM device models was enhanced by variability through a *circuit-level* implementation technique that compares two numbers of different probability distributions, generated externally to define whether a switching event will occur. Simplicity and applicability are the main advantages of this implementation approach. Validity was obtained for the variability applied to the models, since for a sequence of applied SET-RESET pulses the observed variation (rate of resistance change) in each cycle presents a certain degree of stochasticity; i.e. the resistance does not vary in a constant way as observed in simulations without variability. The presented approach makes possible the incorporation of variability in any model parameter in SPICE-like environments and the simulation results underline the rich and realistic simulated curves which can be used to test the robustness of the designed circuits against variability, or assess the exploitation possibilities in applications where randomness of resistance switching behavior is essential. ReRAM devices are particularly interesting for stochastic computing systems [16] where numbers are represented as bitstreams and each bit takes its logic value with certain probability.

Future work in this context concerns statistical parameter extraction from switching performance of real ReRAM devices for the direct injection of random patterns extracted from physical measurements [17], direct comparison of simulation results with experimental data, as well as performance characterization of simulation models in terms of simulation time overhead because of variability injection.

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