Effect of post annealing thermal heating on $Cu2ZnSnS_4$ solar cells processed by sputtering technique

M.F Sanchez[1], T.G Sanchez[1],Maykel Courel[2],Odin Reyes[1], Y. Sanchez[2], E. Saucedo[2]*, P.J. Sebastian[1]*,

[1]Instituto de Energías Renovables, Universidad Nacional Autónoma de México, Temixco, Morelos, 62580, México

[2]Centro Universitario de los Valles (CUValles), Universidad de Guadalajara, Carretera Guadalajara-Ameca Km. 45.5, C.P. 46600, Ameca, Jalisco, Mexico

[2]Catalonia Institute for Energy Research (IREC), Jardins de les Dones de Negre 1, Sant Adrià de Besòs, 08930, Barcelona, Spain.

* Corresponding authors:

P.J. Sebastian; e-mail: sjp@ier.unam.mx

E. Saucedo; e-mail: esaucedo@irec.cat

Abstract

Recently, to improve solar conversion efficiency of Cu_2ZnSnS_4 (CZTS) solar cells it is incorporated dopants like Ge and Cd in the crystal lattice of the absorber layer to reach an energy gap of 1.1 eV. According to Shockley-Queisser photon balance calculations the maximum efficiency is found to be 30% for an energy gap of 1.1 eV. Using Cd one can adjust the energy gap of CZTS from 1.55 to 1.09 eV. Therefore, in this work, a detailed study of

the diffusion of Cd contained in CdS window layer towards the CZTS absorber was carried out by means of a thermal treatment (hotplate) of the solar cell.

The thermal treatment of the Mo/CZTS/CdS/i-ZnO-ITO solar cell was carried out at temperatures ranging from 100°C to 400°C and times varying from 3 to 15 minutes in air atmosphere. The CZTS was grown from deposits of metallic precursors (Cu / Sn / Cu / Zn) by sputtering and annealing at two ramps: 200 ° C for 45 min with an argon flow of 1 mbar and 550 °C for 5 min at 1 bar in an atmosphere of S + Sn. For the complete solar cells with a hotplate treatment of 280 °C for 6 minutes, an increase of 2.7% to 5.2% of conversion efficiency was observed compared to the solar cell without hotplate treatment. The solar cells with hotplate treatment present an XRD peak shift from 28.5° to 28.24°, with lattice parameters a = b = 5.431 Á and c = 10.929 Á, while 338 cm^{-1} Raman peak displacement to the left was observed. The band gap decreased from 1.56 to 1.43 eV and Jsc increased from 12.0 mA/cm^2 to 15.4 mA/cm^2.

1. Introduction

Kesterite semiconductors such as Cu_2ZnSnS_4 (CZTS), $Cu_2ZnSnSe_4$ (CZTSe) and $Cu_2ZnSn(SSe)_4$ (CZTS,Se) constitute potential absorbers for thin film solar cell applications due to their adequate physical properties such as direct band-gap transitions in the range of 1.0-1.5 eV [1,2] and an absorption coefficient higher than10^4 cm^{-1} [3-5]. In addition, these compounds are based on low-toxic and high abundance elements in the earth's crust, which would reduce the processing cost of solar cells [6]. According to theoretical calculations, a conversion efficiency higher than 30% is expected, which is comparable with the ones obtained for CdTe and CIGS [7]. However, current efficiencies reported for CZTS, CZTSe and CZTSSe solar cells are far behind those achieved by CIGS technology (22.6%) [8]. A high open-circuit voltage deficit has been identified as the main reason for low solar cell efficiencies, which is a result of low minority carrier lifetime [9] and high recombination rates

at buffer/absorber interface [10]. Therefore, more studies focused on the reduction of defects in Kesterite materials are in progress by the scientific community.

The doping of Kesterite with other elements has been proposed as a route to reduce the effect of defects that promotes the solar cell efficiency. In particular, the use of Cd as doping element in Kesterite compound has been reported in the literature, with the advantages of band-gap tailoring in the range of 1.09-1.55 eV as a function of Cd concentration, the reduction of Cu_{Zn} and Zn_{Cu} antisite defects [11-13] and the decrease of ZnS secondary phases due to the partial substitution of Zn element by Cd element [14]. In particular, Xiao et. al. doped Kesterite with different Cd concentrations to obtain the total replacement of Zn by Cd and observed a reduction of band-gap with the increase of Cd doping from 1.55 eV (CZTS) to 1.09 eV (CCTS)[15]. On the other hand, there are other reports on Cd diffusion from the buffer layer to the Kesterite material as reported by J. Huang et. al. [16]. In this work, authors deposited CZTS thin films by sputtering technique followed by a thermal treatment with a laser for few microseconds, obtaining a Cd diffusion at CdS/CZTS interface, which resulted in the reduction of band-gap energy from 1.52 to 1.3 eV, Voc increase from 491.41 to 535.50 mV as well as the reduction of carrier recombination at depletion zone, increasing thereby solar cell efficiency from 3.83 to 5.60%. In another work, K. Sun et al.[9] dipped CZTS simples in a mixture of cadmium sulfate and ammonium hydroxide and later submitted to a thermal treatment, favoring Cd diffusion at CZTS/CdS interface, demonstrating the reduction of carrier recombination at the depletion zone, which was translated into a Voc increase from 616.9 to 689.1mV and an efficiency increase from 5.94 to 7.62%. In addition, it was reported the enhancement of minority carrier lifetime from 10 ns to 28 ns, resulting in improved EQE in the range of 500-550nm. Taking into account the advantages of CZTS doped with Cd reported by previous works, in this experimental work

we present results on the improvement of CZTS solar cell efficiency as a result of Cd diffusion from CdS layer after a thermal treatment.

2. Experimental Details

2.1. Solar cell processing

Solar cells were fabricated under Glass/Mo/CZTS/CdS/i-ZnO/ITO configuration. A back contact of Mo with thickness of 1 μm and sheet resistance of 0.205 Ω/sq was deposited by DC-magnetron sputtering technique on corning glass substrate. After this, CZTS absorber layer was grown starting from Cu/Sn/Cu/Zn stack deposited by sputtering technique under Zn-rich and Cu-poor conditions (Cu/(Zn+Sn)= 0.8 and Zn/Sn=1.25) and later subjected to a thermal annealing under two steps in a tubular oven by using a partially lock graphite box of 69 cm^3 with 100 mg of S (99.999%) and 5 mg of Sn (99.995%). The thermal annealing consisted of two steps; in the first step samples were heated up starting from room temperature under a heating rate of 20°C/min until 200°C was achieved, which was kept for 30 min under an argon flux of 1 mbar. In the second step, a heating rate of 20°C/min was also considered but now the temperature was raised up to 550°C and a static pressure of 1 bar in air atmosphere. In this case the samples are thermally treated for 15 min. Later on the, samples were naturally cooled down to room temperature. The final thickness of the absorber layer after thermal annealing was 1.5 μm. Before depositing CdS layer, the absorber material was subjected to a chemical etching consisting of a solution of $(NH_4)_2S$ during 2 minutes to eliminate secondary phases from the surface and to passivate it. After this, CdS layers of 50 nm width were deposited on the absorber material by chemical bath deposition, followed by ZnO (50 nm) and ITO (300 nm) layers by DC-magnetron sputtering during 10 min and 20 min, respectively. Finally, solar cells were subjected to a thermal annealing in a hotplate in air atmosphere to improve the quality of the junction. For this, it

was first studied the effect of temperature by setting the hotplate at 100, 200, 300 and 400°C for 10 min. Then, conditions that favor the optimization of solar cell efficiency was studied but now considering temperatures of 250, 260, 270, 280, 290, 300 and 325°C. Once an optimum temperature is found, the effect of different annealing times of 3, 6, 10, 12 and 15 min in the hotplate was evaluated. For electrical characterization, solar cells were mechanically scribed using a scriber (MR200 OEG), resulting in areas of 0.087 cm^2.

2.2. Characterization

For structural characterization of CZTS thin film solar cells, XRD measurements were performed using a Rigaku diffractometer with CuKα radiation (k=1.54056 Å). XRD measurements were carried out in the 2θ-θ mode, considering the range of 20-80° with a grazing angle of 1.5°. The transmittance and reflectance spectra of the thin films were measured using Shimadzu 3101 PC UV-vis spectrophotometer in the wavelength range of 250-2500 nm. The SEM cross-section images were obtained by using a ZEISS Auriga Serie Microscope under an accelerating voltage of 5 kV. For I-V measurements of the thin film solar cells, a Sun 3000 class AAA solar cell simulator was used. Standard conditions of 25ºC and AM1.5G with an irradiance of 100mW/cm^2 were used for electrical measurements of the solar cells. External Quantum Efficiency (EQE) measurements were performed using a Bentham PVE300 system calibrated with photodiodes of Si and Ge. For C-V measurements in dark, a Keithley CV590 with 100 kHz was used with a voltage modulation of 10 mV. Furthermore, Raman spectroscopy measurements were carried out using an iHr550 Horiba-JobinYvon system with He-Ne laser characterized by an excitation source of 633 nm. For this, Si was used as the reference and Raman spectra of samples were corrected with respect to Si line at 520 cm^{-1}.

3. Results and Discussion

3.1. Study on the impact of hotplate annealing temperature on CZTS solar cells

The influence of different hotplate annealing temperatures on the CZTS solar cell properties was studied first. Figure 1 shows the short-circuit current density as a function of thermal annealing temperature of the hotplate on solar cell CZTS 1. In particular, the effect of temperatures of 100, 200, 250, 300 and 400°C were evaluated on CZTS solar cells during 10 min. Result for reference solar cell without hotplate annealing was included for comparison. This figure shows that Jsc has a tendency to decrease at 200 ° C and then to increase and reaching a maximum at 300 ° C. However, as an interesting result, a maximum value of 13.9 mA/cm^2 at 300 ^{o}C was found, which is higher than the value obtained for the reference solar cell which is 12.0 mA/cm^2. This improvement in Jsc is presumably due to Cd diffusion from CdS to CZTS layer during the hotplate annealing, which would reduce CZTS bandgap, thereby increasing the Jsc value. For a relatively high temperature of hotplate annealing (400^{o}C), degradation in Jsc to values of 0 mA/cm^2 is observed. As a result, a hotplate annealing temperature of 300 ^{o}C allows better Jsc values for the solar cells, while a clear degradation in the p-n junction of the devices is observed for higher temperatures.

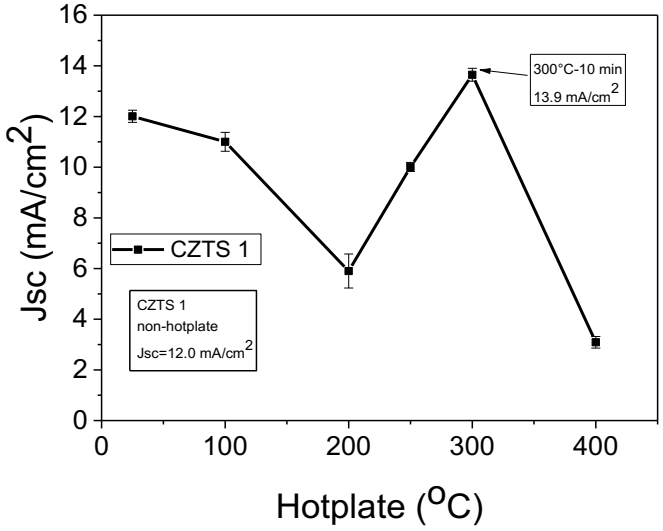

Figure 1. Effect of hotplate annealing process tested in the range of 100 to 400ºC on Jsc of the CZTS solar cells

¡Error! No se encuentra el origen de la referencia. shows the influence of hotplate annealing temperature on the CZTS devices in the range of 250 to 325 °C. The influence of temperatures of 250, 260, 270, 280, 290, 300 and 325°C for 10 min was tested. The device without hotplate showed values of η = 2.7% and Jsc = 12.0 mA/cm^2. The hotplate annealing temperature of 280°C showed a maximum Jsc value of 15.0 mA / cm^2

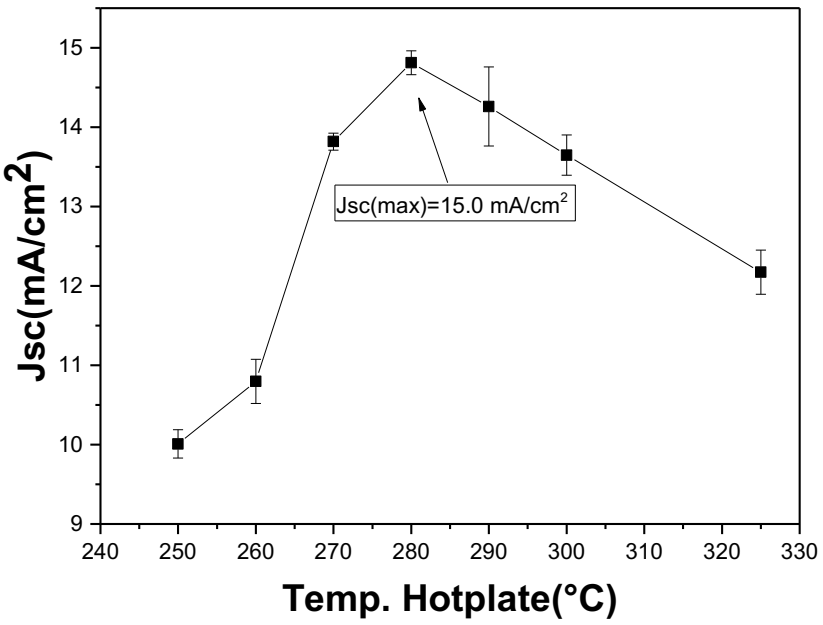

Figure 2. Jsc vs temperature graph showing the influence of hotplate annealing temperature on the CZTS device

4.2 Study on the influence of hotplate annealing time on CZTS solar cells

Fig. 3 shows the optimization of hotplate annealing time on CZTS devices. With the hotplate annealing temperature kept at 280°C, hotplate annealing times of 3, 6, 10, 12, and 15 minutes were investigated. In the same way as in the case of hotplate annealing temperature study, the curves of efficiency versus time and Jsc versus time do not show a linear increase or decrease with increasing time. For 6 minutes of hotplate annealing, a maximum conversion efficiency of 5.2% and Jsc of 15.4 mA/cm^2 were obtained. For times higher than 6 minutes, efficiency and Jsc values showed a decrease (**Table 1**)

Table 1. Electrical properties of the CZTS device in the hotplate annealing time study

Hotplate-time (min)	η (%)	FF (%)	Voc (mV)	Jsc(mA/cm^2)
3	3.3	44.2	495.4	14.8
6	5.2	52.7	638.6	15.4
10	4.1	37.8	608.8	15.0
12	3.2	35.6	609.4	14.1
15	3.0	37.0	627.3	13.0

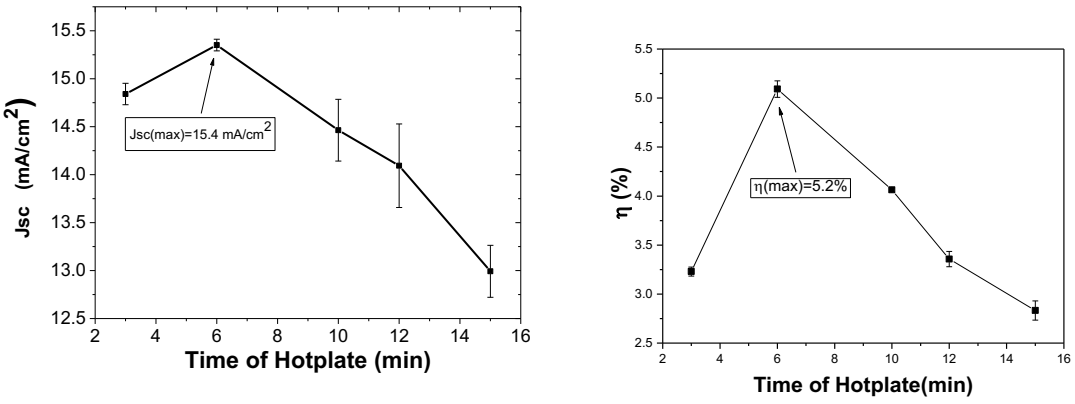

Figure 3. Rresults of the hotplate-time optimization a) Jsc vs hotplate-time b) η vs hotplate-time

4.3 Characterization of non-hotplate, optimized hotplate and excess-time hotplate devices

Fig. 4 shows the XRD diffractograms of non-hotplate, hotplate (280°C-6 min.) and excess-Hotplate (excess hotplate time) devices. In all the three devices, the 28.4° peak (112)

characteristic of kesterite phase is present and doesn´t overlap with secondary phases. However, devices with hotplate the 28.4° peak shifted slightly to the left (Fig. 4b). In the literature, it is mentioned that this shift is due to partial substitution of zinc by cadmium in CZTS structure [2] [1] and lattice parameters *a* and *b* increased from 5.427Å to 5.431Å and *c* from 10.903Å to 10.929Å due to the larger size of Cd atom [17-19]. The crystal size increased from 33 nm to 37.47 nm with Hotplate compared to non-Hotplate device (**Table 3**).

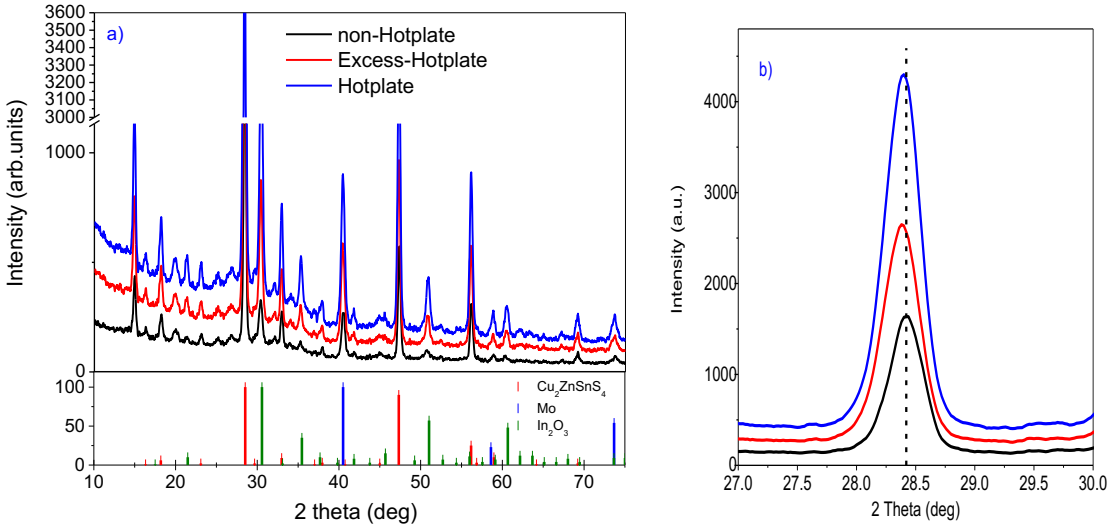

Figure 4. a) X-ray diffractograms of non-hotplate, hotplate and excess-hotplate devices. **b)** position of the main peak of CZTS at 2θ = 28.5°

Table 2. The lattice parameters and crystal size of non-hotplate, hotplate and excess-hotplate devices.

CZTS Devices	Lattice parameters (Å)		Cell Volume ($Å^3$)	Crystal size corrected for strain (nm)	Micro-Strain (Williamson–Hall)
	a=b	c			
non-Hotplate	5.427	10.903	321.10	33	0.0042
Hotplate	5.431	10.929	322.36	37.47	0.0043
Excess-hotplate	5.440	10.964	324.46	32.25	0.0037

Fig. 5 shows the Raman spectra of the non-hotplate, hotplate and excess-hotplate devices. Main peaks of CZTS at 337cm^{-1} (mode A) and 366 cm^{-1} (mode E), as well as other peaks with vibrational mode A at positions 263 cm^{-1} and 287cm^{-1}[20] were observed. For the Peak at 313 cm^{-1} (mode A) an increase in intensity is observed when applying the hotplate treatment, which can be attributed to SnS_2 secondary phase[21]. It is observed that in devices with hotplate there is a displacement of the main peak at 338cm^{-1} towards the left to 334cm^{-1} (Fig. 5b), which is due to the presence of cadmium by diffusion during hotplate annealing of CZTS structure, which comes from the CdS window layer. It has been reported in the literature that the presence of cadmium in the $Cu_2Zn_{x-1}Cd_xSnS_4$ structure has a main peak at 332cm^{-1}[17,18,22]].

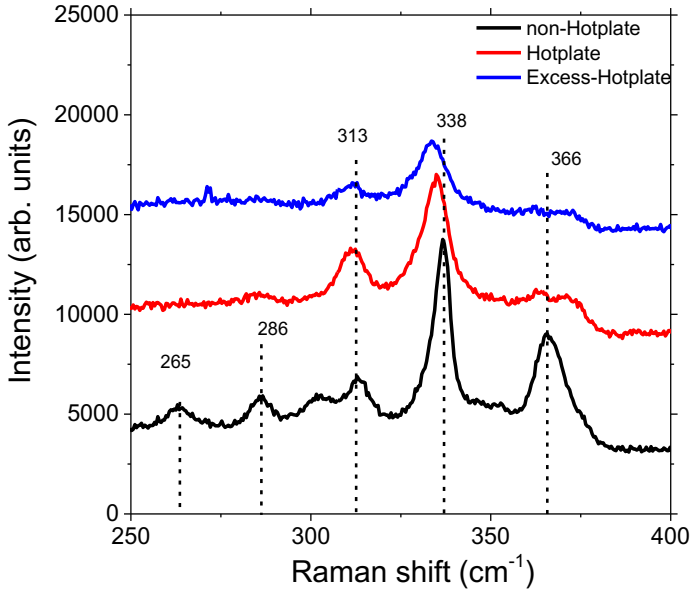

Figure 5. Raman spectra of the non-Hotplate, hotplate and excess-hotplate devices

The external quantum efficiency curves of the non-hotplate, hotplate and excess-hotplate devices are presented in fig 6 (a) [16]. In the device with hotplate at 280°C for 6 minutes EQE increased from ~70% to ~80% in the range of 500 to 800 nm compared to the non-hotplate device, which increased Jsc. This can be attributed to an increase in carrier lifetime and / or a decrease in carrier recombination within the depletion zone [9]. Absorption above 800 nm results in a smaller band gap compared to non-hotplate device, which is related to the diffusion of cadmium on absorber surface [16]. For Excess-hotplate device, steep drop in EQE can be observed. Band gaps for non-hotplate and hotplate devices are presented in figure 6 b. The curve corresponding to the device with hotplate has a wavelength range of 800 to 900 nm, while the band gap shows a decrease that goes from 1.56 to 1.43 eV. Reduction of band gap is a consequence of partial replacement of zinc by cadmium in CZTS structure, due to diffusion of cadmium from n-type semiconductor to the absorber, a consequence of applying temperature to the device.

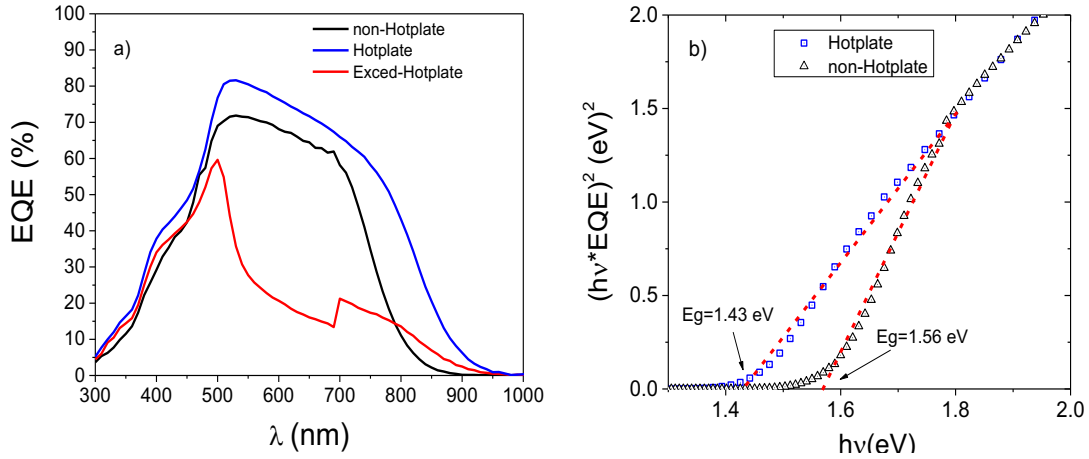

Figure 6. a) EQE of non-hotplate, hotplate (280°C-6 min) and excess-hotplate (280°C) devices with long time and **b)** band gap for hotplate and non-hotplate devices

Fig. 7 shows the curves of Isc vs. Voc for hotplate and non-hotplate devices. An increase in the values of Jsc (3.6 mA), Voc (55 mV) and FF (8%) can be observed for the hotplate device (table 3). The increase in Jsc was due to better electron collection in long wavelength region (500 to 800nm) as mentioned above, showing an improvement in conversion efficiency from 2.7 to 5.2%.

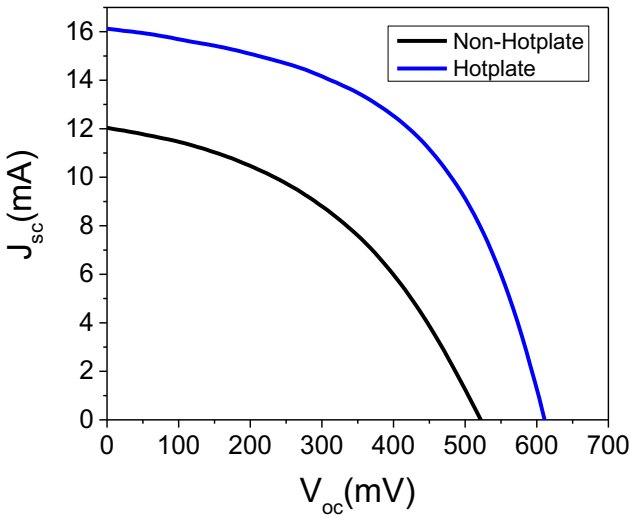

Figure 7. Jsc vs. Voc curves for hotplate and non-hotplate devices

Table 3 Comparison of electrical properties of non-hotplate and hotplate devices

Device	η (%)	FF (%)	Voc (mV)	Jsc (mA/cm^2)
Non-Hotplate	2.5±0.15	43.93±0.378	579.33±12.19	11.74±0.26
Hotplate	5.1±0.085	52.15±0.53	634.32±2.30	15.35±0.06

To characterize the electronic properties of photovoltaic devices, capacitance-voltage (C-V) measurements were carried out. Estimated values of charge carrier concentration, concentration profile of charge carriers and the width of depletion zone were included. Capacitance (C) per unit area (A) as a function of applied voltage (V) is given by:

$$\left(\frac{C}{A}\right)^2 = \frac{q\varepsilon_0\varepsilon_r|N_A - N_D|}{2(V_{bi} - V)} \qquad (1)$$

where, $|N_A - N_D|$ is the net doping density, V_{bi} (=ϕ_{bi}/q) is the built-in potential, q is the elementary charge (1.602x10^{-19}C), ε_0 is the permittivity of free space (8.85x10^{-12} F / m), and ε_r is the relative permittivity (7 for CZTS).

From the linear extrapolation of data from the *Mott-Schottky* 1/(C)^2 vs. V (Fig.8a) plot for 1/(C/A)^2 → 0 (or C → ∞) with low forward bias led to a built-in potential around Vbi = 950 mV for hotplate device and Vbi = 1850 mV for the non-hotplate device. It is well known that the built-in potential is directly proportional to the value of band bending in CZTS layer near the interface, and generally estimation of Vbi is not very accurate when doping is low in thin films [23,24]. It is observed that for the non-hotplate solar cell, CV data shows that

capacitance is practically unchanged when reverse bias is greater than 1V (see inset), suggesting that the CZTS film is completely depleted due to the thin nature of the layer.

The width of the depletion zone W was determined by measuring the capacitance and net doping density $N_A - N_D$ obtained from the derivative through the following equation:

$$\frac{d}{dV}\left[\frac{1}{(C/A)^2}\right] = -\frac{2}{q\varepsilon_0\varepsilon_r|N_A - N_D|}, \qquad \left(W = \frac{A\varepsilon_0\varepsilon_r}{C}\right) \qquad (2)$$

Hotplate device showed a decrease in space charge region from ~ 229 nm to ~ 136nm. A depletion zone width in the range of 95-200 nm has been reported in the literature for CZTS solar cells [25.27].

For low forward bias, capacitance of CZTS/CdS junction dominates and therefore $|N_A - N_D|$ corresponds to a region close to CdS, so built-in potencial is V_{bi} =1.85V and 0.95V for hotplate and non-hotplate devices, respectively. Values of $|N_A - N_D|$ = 5x10^{16}cm^{-3} and 2x10^{17}cm^{-3} were obtained for hotplate and non-hotplate devices, respectively. These values are close to N_A-N_D values reported for CZTS solar cells [28,29].

Table 4. Depletion zone, Na and Vbi for hotplate and non-hotplate devices

Device	N_A (cm^{-3})	W_d (nm)	V_{bi} (V)
Hotplate	2x10^{17}	229	1.85
Non-Hotplate	5x10^{16}	136	0.95

Profiles of net acceptor concentration through hotplate and non-hotplate devices are presented in Fig. 8b. The branch on the left side (direct bias) indicates the doping density at CZTS/CdS interface; tail extending towards Mo substrate (reverse bias) corresponds to

doping density in most of the absorber layer. As can be seen in the C-V profile, non-hotplate device has a doping of $5x10^{16}$ cm^{-3} in the region of CZTS/CdS interface and hotplate device has a higher doping value of $2x10^{17}cm^{-3}$ in this zone.

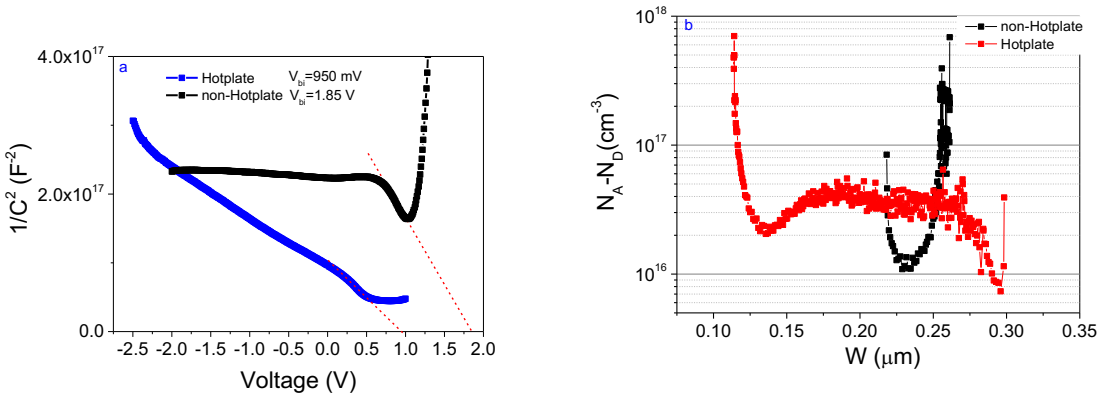

Figure 8. a) $1/C^2$ vs. V graph for the hotplate and non-hotplate devices for calculating Vbi and **b)** Doping profiles estimated from C–V data measured at 100 kHz

SEM Analysis

Fig. 9 shows the cross-sectional SEM images (A, B) of the non-hotplate device (Mo / CZTS / CdS / ZnO-i / ITO). According to the micrograph for the solar cell without hotplate, the grain size is not homogeneous; near the interface with the window layer it presents an average size of 368.44nm and 160.39nm at the interface with the posterior molybdenum contact. This variation in grain size along the thickness of the absorber may be due to an excess of Zinc in the lower part of the film [23]. The total thickness of the absorber is 1.5 μm.

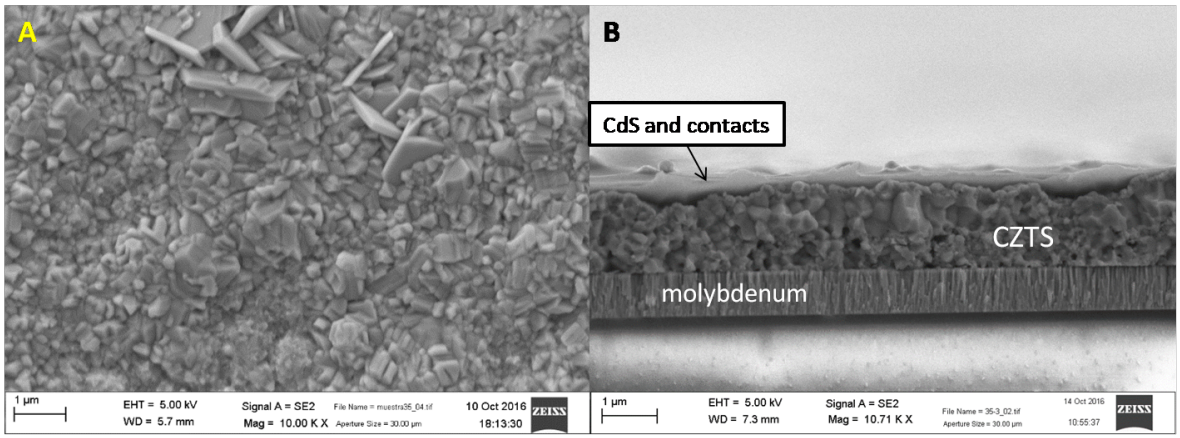

Figure 9 SEM micrographs for the non-hotplate device: **A)** superficial magnificación of 10K **B)** transversal magnificación of 10.7K

For the device with hotplate (Fig 10) the grain size is observed uniform throughout the thickness of the absorber with an average size of 418.87 nm. The increase in grain size can be attributed to the incorporation of cadmium in the crystalline lattice of the absorber [2].

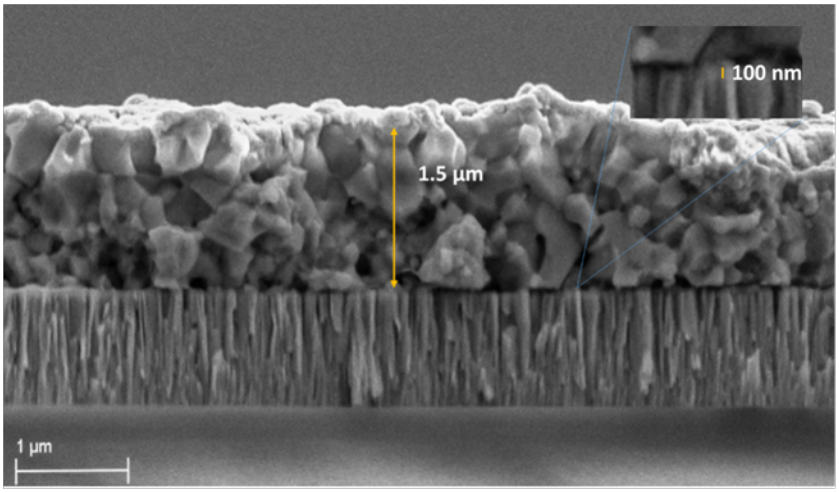

Figure 10 SEM for the hotplate device (280°C-6 min)

Conclusions

CZTS solar cells were subjected to a thermal treatment under air atmosphere by using a hot plate and the impact of different temperatures and annealing times on solar cell characteristics were studied. It was found that the thermal treatment decreased the absorber bandgap from 1.56 to 1.43 eV and increased the J_{sc} from 12.0 to 15.4 mA/cm^2, which is due to the result of 20 % increase of EQE. We suggest applying about 280 ° C hotplate heat treatment for 6 min for the solar cell structure, to promote cadmium diffusion from the n-type semiconductor to the absorber structure, resulting in an increase of up to 1% in efficiency of the cell, as well as an improvement in Jsc and EQE. These changes are due to a partial replacement of Zn by Cd in the structure of Cu2ZnSnS4, this phenomenon decreases band gap from 1.63 to 1.5 in the CZTS.

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