# Beneficial Role of Noise in Hf-based Memristors

Rosana Rodriguez, Javier Martin-Martinez, Emili Salvador, Albert Crespo-Yepes, Enrique Miranda, Montserrat Nafria
Electronic Engineering Dept., REDEC Group
Universitat Autònoma de Barcelona (UAB)
Bellaterra, Barcelona, Spain
rosana.rodriguez@uab.es

Antonio Rubio, Vasileios Ntinas
Electronic Engineering Department
Universitat Politècnica de Catalunya (UPC)
Barcelona, Spain
antonio.rubio@upc.edu
vasileios.ntinas@upc.edu

Georgios Ch. Sirakoulis
Dept. of Electrical & Computer Engineering
Democritus University of Thrace (DUTh)
Xanthi, Greece
gsirak@ee.duth.gr

***Abstract*— The beneficial role of noise in the performance of Hf-based memristors has been experimentally studied. The addition of an external gaussian noise to the bias circuitry positively impacts the memristors characteristics by increasing the OFF/ON resistances ratio. The known stochastic resonance effect has been observed, when changing the standard deviation of the noise. The influence of the additive noise on the memristor current-voltage characteristic and on the set and reset related parameters are also presented.**

***Keywords— Stochastic resonance, memristors, RRAM devices, resistive switching***

## I. INTRODUCTION

Emerging devices as memristors are nowadays of great interest in the scientific community due to their properties, as low power consumption and large integration density [1]. The reversible change in memristor conductivity when subjected to a proper biasing opens the possibility of their use in a wide range of applications, such as non-volatile memory, alternative computing architectures, neuromorphic systems, security schemes, etc [2-6]. Memristors show a non-linear current-voltage characteristic, so the properties associated to nonlinear systems can be explored in these devices. In this sense, although noise in electronics should usually be avoided, in non-linear systems it can have a beneficial role, improving the performance of devices. This phenomenon is known as Stochastic Resonance (SR) and it is present in nature in several fields as biology, engineering, etc [7-10]. SR takes place in non-linear devices with thresholds in their characteristic curves, as it is the case of memristors.

Several previous works have analyzed the constructive role of noise in memristors. [11] analyzes theoretically the beneficial role of an additive noise in memristors through a memristor model. An alternative SR model in memristors can be found in [12], with a good agreement with experimental measurements in manganite samples. In [13] SR is experimentally studied in memristors subjected to sinusoidal signals with noise added. The SR was also shown to reduce the Bit Error Rate (BER) in Resistive Random Access Memory (RRAM) devices [14]. In [15], the addition of noise in metal-oxide memristors fabricated with zirconium dioxide and tantalum pentoxide is analyzed both experimentally and theoretically, observing the constructive role of noise in these samples.

In this work, we demonstrate experimentally the beneficial role of noise in CMOS compatible hafnium oxide-based memristors. Differently to other works where the noise signal is needed to observe the regular memristor hysteretic current-voltage characteristic (I-V, Figure 1), in this work we start from samples where the initial I-V curves (without noise) show a clear differentiation between the memristor low resistance state (LRS, ON state) and the high resistance state (HRS, OFF state), and study the impact of a noise added to the bias of the device on these I-V characteristic curves. In this case, noise is not used to initiate/achieve memristor state's switching, but to further improve/widen the existing resistance window. Statistical characterizations of the resistance ratio between the ON and OFF states ($R_{OFF}/R_{ON}$) and of the currents and voltages in the set and reset processes in the presence of noise are analyzed.

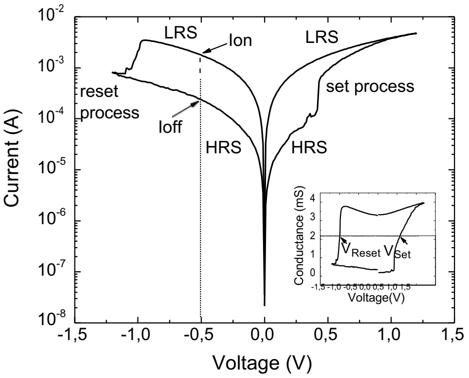

Figure1: Typical current-voltage characteristic of the memristors used in this work. Inset: The set/reset voltages were defined as the positive (Vset) /negative (Vreset) voltages for which the mean value between the maximum and minimum conductance values in the I-V curve characteristic were measured. Iset and Ireset currents correspond to the currents associated to Vset and Vreset respectively.

## II. SAMPLES AND MEASUREMENT PROCEDURE

The tested samples consist in TiN−Ti−$HfO_2$−W Metal-Insulator-Metal (MIM) structures. A cross-sectional view is shown in Figure 2. The devices were fabricated on Si wafers with a thermally grown 200nm-thick $SiO_2$ layer. The 10nm-thick $HfO_2$ layer was deposited by atomic layer deposition

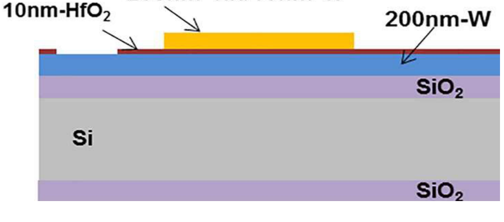

Figure 2: Schematic of the MIM structures used in this work.

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(ALD) at 225°C using TDMAH and $H_2O$ as precursors, and $N_2$ as carrier and purge gas. The bottom electrode consists of a 200nm−W layer and the top electrode of a 200nm−TiN on top of a10nm−Ti layer acting as oxygen getter material. The resulting device structures are square cells with an area of 5x5μm$^2$. Further details of their fabrication process can be found in [16].

The measurements were performed using a Semiconductor Parameter Analyzer (SPA) Agilent 4156C. The equipment was controlled via GPIB bus, and the measurements programmed with Matlab software. Firstly, fresh (i.e. as-grown) memristors were subjected to a 1mA current-limited forming process that takes place at voltages ≅ 4V. After forming, the memristor I-V characteristics (Figure 1) were registered during 200 consecutive cycles. To measure the I-V curves, the samples were subjected successively to voltage ramps, sweeping the voltage from 0V to 1.2V, from 1.2V to -1.2V and from -1.2V to 0V and the current was registered during the application of voltage.

The memristors used in this work present a bipolar behavior. The set process (the change from HRS to LRS) is produced for positive voltages and the reset process (the change from LRS to HRS) takes place at negative voltages (Figure 1). The variation in the memristor conductivity is related to the formation/destruction of a conductive filament through the dielectric where oxygen-related species are responsible of this conductive variation[17].

Registration of each I-V curve takes several seconds, so that each voltage ramp can be considered as a series of DC measurements with increasing voltage. To analyze the noise impact, Gaussian noise, whose standard deviation (σ) ranged between 50 mV and 150 mV, was added to the ramp voltage by smart instrument control. Noise was generated by the SPA, programmed with a Matlab script to add point to point to the voltage ramp bias a gaussian signal of a determinate sigma. Different devices were used to analyze each of the considered noise conditions. Noise impact on the difference between ON and OFF memristor resistance ratio ($R_{OFF}/R_{ON}$), I-V curves, set and reset voltages and currents (Vreset and Ireset) were studied.

Memristors were also subjected to pulsed voltages of 50 Hz and 1KHz frequency using the Keithley 4200A-SCS. For these measurements, Gaussian noise was added to the system by hardware, using the Keysight 81150A pulse function arbitrary noise generator.

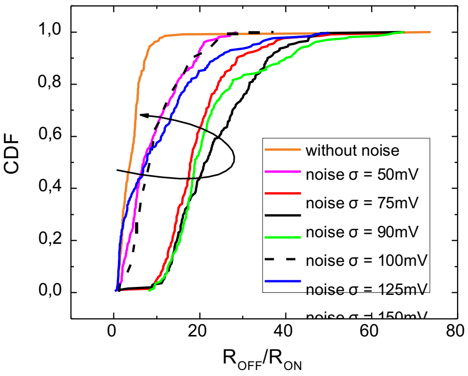

Figure 3: CDFs of the memristor $R_{OFF}/R_{ON}$ ratio for different noise σ. The curves are ordered following the stochastic resonance behavior. Noise σ of 90 mV offers best $R_{OFF}/R_{ON}$ ratio.

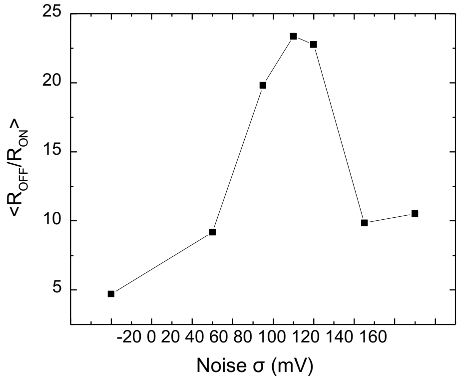

Figure 4: Mean values of the memristor ratio $R_{OFF}/R_{ON}$ as a function of the noise σ. The stochastic resonance curve is observed.

## III. RESULTS

### A. *Impact of noise on memristor $R_{OFF}/R_{ON}$ resistance ratio*

From the values of currents at a voltage of -0.5V in the I-V memristor characteristics ($I_{OFF}$ and $I_{ON}$ in Figure1) the resistance ratio $R_{OFF}/R_{ON}$ was directly obtained through Ohm's law. The reading voltage of -0.5V was chosen because the probability to change the memristor state at this voltage value is very low. $R_{OFF}/R_{ON}$ was evaluated from the I-V's measured with and without additive noise. Figure 3 shows the cumulative distribution functions (CDFs) of the $R_{OFF}/R_{ON}$ ratio measured for the 200 cycles at each noise condition. Note that the smallest $R_{OFF}/R_{ON}$ ratio is measured when noise is not added and that the presence of noise always leads to larger values of this parameter. However, the improvement depends on the value of σ. Initially, as σ increases, the CDF curves are shifted to the right (i.e, to larger $R_{OFF}/R_{ON}$ values), with a maximum shift for the case of σ= 90 mV. But, for larger noise σ values, the CDFs curves shift towards smaller values of $R_{OFF}/R_{ON}$. This result suggests that the phenomenon of the stochastic resonance is observed in memristors in the presence of noise. Figure 4 shows the mean value of the $R_{OFF}/R_{ON}$ ratio as a function of the noise standard deviation. Each point in this graph is the mean value of the ratios measured in the 200 cycles applied

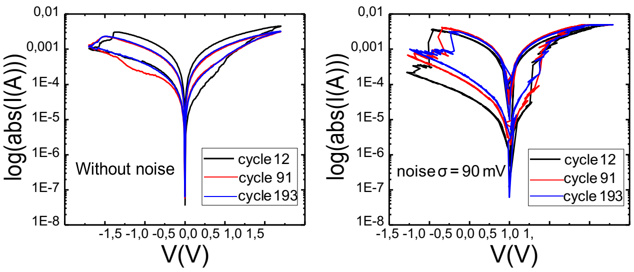

Figure 5: Memristor current-voltage characteristics at cycles 12, 91 and 193 without (left) and with 90 mV noise σ.

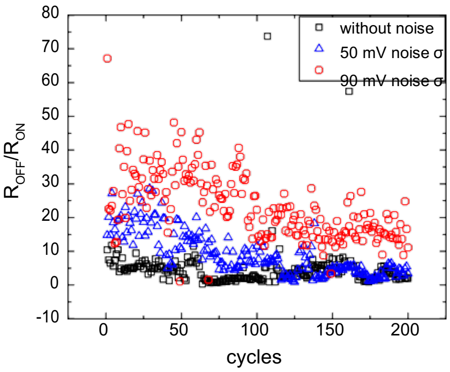

Figure 6: Memristor $R_{OFF}/R_{ON}$ ratio as a function of the number of cycles for the without noise case and for additive noise σs of 50 mV and 90 mV.

for each noise condition. Clearly, an increment of the $R_{OFF}/R_{ON}$ ratio is observed when noise is added, and the maximum improvement is observed for noise σ around 90 mV. The addition of noise has a clear beneficial role, and the typical stochastic resonance curve with a peak for intermediate noise levels is observed.

To further analyze the impact of noise in the memristor I-V characteristic, Figure 5 shows the memristor I-V curves without adding noise (left) and with a noise of 90 mV σ summed to the bias (right). Differences in the currents and voltages associated to set and reset processes are also observed in the presence of noise. These differences are analyzed in more detail in the next section. From the 200 cycles, cycles 12, 91 and 193 were selected as examples of initial, intermediate, and final cycles. The memristor I-V characteristic is clearly more open when noise is added, leading to the larger $R_{OFF}/R_{ON}$ resistance ratios. In both cases, as the number of cycles increases, the difference between ON and OFF state currents decreases, and the hysteretic behavior of the I-V curves tends to decrease. This is a general trend for all the noise σ studied and can be attributed to a memristor degradation as the number of I-V cycles increases, that provokes a decrease of the memristor resistance ratio. As an example, Figure 6 shows the evolution of the $R_{OFF}/R_{ON}$ ratio along the 200 I-V cycles, for the w.o.-noise case and when a noise of 50 mV or 90 mV σ is added. A clear difference in the evolution of the $R_{OFF}/R_{ON}$ ratio with cycling is observed, depending on the presence or absence of noise. Again, a notable increment of the ratio for σ=90 mV is observed in the first cycles. However, as the number of cycles increases, the $R_{OFF}/R_{ON}$ ratio tends to decrease, for the three cases represented, which is related to the reduction of the difference between the ON and OFF state currents observed in Figure 5, attributed to the memristor degradation.

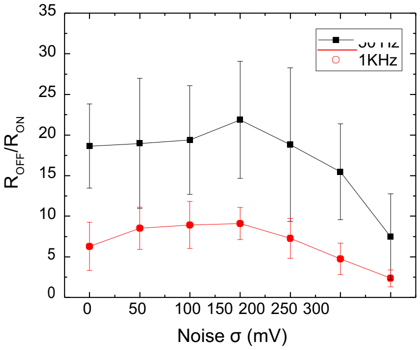

Figure 7: $R_{OFF}/R_{ON}$ resistance ratio for memristors subjected to pulsed measurements. Error bars indicate the standard deviation.

The previous results have been obtained through the application of slow ramp voltages that can be considered a sequence of increasing voltage DC measurements. $R_{OFF}/R_{ON}$ ratio was also investigated when memristors were subjected to bipolar pulsed voltages (with top and bottom voltages of 1.1V to -1.1V respectively) with frequencies of 50 Hz and 1KHz. For each frequency and noise σ, 200 pulse periods were applied. Memristor I-V curves are obtained from the rise and fall edges of the pulsed signal, and the $R_{OFF}/R_{ON}$ ratio was calculated from the $I_{ON}$ and $I_{OFF}$ currents at -0.5V as in the DC case. Figure 7 shows the mean value of the $R_{OFF}/R_{ON}$ and the standard deviation for each frequency/noise condition. As frequency increases, both the resistance ratio mean value $<R_{OFF}/R_{ON}>$ and its standard deviation decrease, as expected [18]. A dependence of the $R_{OFF}/R_{ON}$ ratio on the noise standard deviation is also observed, with larger $R_{OFF}/R_{ON}$ values for noise σ ranged between 50 and 200 mV. However, the impact of noise in these pulsed conditions is lower than for the DC case.

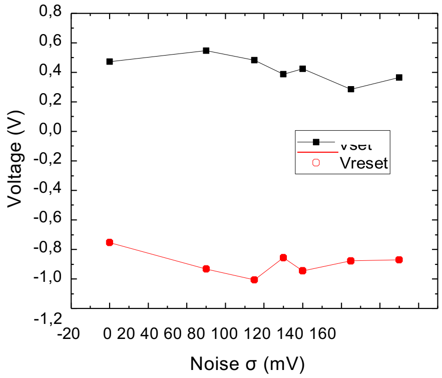

Figure 8: Mean values of Vset and Vreset as a function of noise σ.

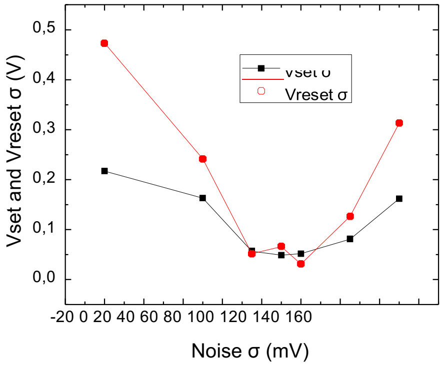

Figure 9: Vset and Vreset standard deviations as a function of noise σ.

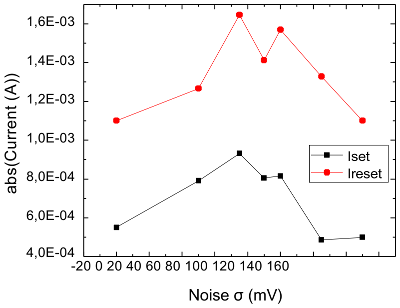

Figure 10: Mean values of Iset and Ireset currents as a function of noise σ

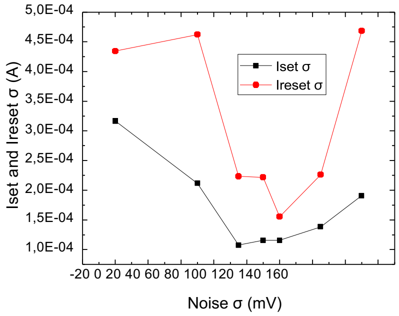

Figure 11: Iset and Ireset standard deviations as a function of noise σ.

### B. *Impact of noise on memristor set and reset parameters*

The effect of noise on the voltages and currents associated to the set and reset processes (Vset, Vreset and Iset, Ireset) was also analyzed for the DC case.

Figures 8 and 9 show the Vset and Vreset voltages and their standard deviations, respectively, as a function of the noise σ. The results suggest that the addition of noise tends to decrease Vset. In the case of Vreset, the influence of noise is not so clear. Although, in general, larger values of Vreset (in absolute values) are measured in the presence of noise, for σ=90 mV, a change of tendency to lower reset values is observed. The effect of noise in the Vreset and Vset dispersion is more noticeable (Figure 9). For the noise σ where SR is more clearly observed (from 75mV to 100 mV), a lower dispersion of the Vset and Vreset values is obtained. Similar trends have been observed for the Iset and Ireset currents (Figure 10). For the noise cases where the SR is more visible, Iset and Ireset currents tend to increase (in absolute value), leading to a major difference between LRS and HRS conduction levels, that is, the ROFF/RON ratio. Again, the impact of noise is more appreciable in the Iset and Ireset standard deviations, with lower current dispersions for noise σ between 75 mV and 100 mV (Figure 11).

## IV. CONCLUSIONS

The potential beneficial role of external noise has been demonstrated in Hf-based memristors. The addition to the bias of Gaussian noise of a determined standard deviation increases the resistance difference between the memristor LRS and HRS by opening the resistance window between ON and OFF states. The typical stochastic resonance curve has been observed with a peak at a certain optimum noise level: the OFF/ON resistance ratio is the lowest for the case without noise, and in the presence of noise, it increases until the optimum noise standard deviation and decreases again for larger noise amplitudes. Clear differences in the memristor current-voltage characteristics have been observed when noise is added, affecting the hysteretic memristor behavior. The impact of noise on the set and reset voltages and currents has also been studied, observing that the addition of the external noise provokes a lower dispersion of set and reset voltages and currents. Though more investigation about the constructive role of noise on memristors should be performed, this work paves the way for a promising scenario where characteristics and reliability of memristive circuits can be enhanced, taking advantage of the SR phenomenon.

## ACKNOWLEDGMENT

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