Design Optimization of Switching-Cell-Array-Based Power Converters

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***Abstract*— With the aim to increase standardization, reduce the cost, and obtain advanced performance features, the design of voltage-source power converter legs can be undertaken by combining several instances of a standard switching cell, properly connected in active neutral-point-clamped structures to reach the desired voltage and current ratings. These switching cells can be organized into switching-cell arrays. This design approach introduces several degrees of freedom into the design. Namely, the different options to interconnect the cells and the distribution of switching losses among these cells. This article aims to define an optimization problem to explore this design space. The design problem is formulated in different scenarios, involving different conversion configurations (dc-dc and dc-ac), different leg number of levels (two and three), and different types of available cells (standard and conduction-optimized in combination with switching-optimized). A weighted objective function is then defined in terms of leg simplicity, efficiency, and reliability. The value of the design variables that minimize the objective function with different sets of weighting factors are obtained under selected scenarios and operating conditions, to illustrate the flexibility of the converter design approach under study. The solution of the optimization problem is obtained using a surrogate optimization algorithm in MATLAB, well suited to quickly solve optimization problems involving a combination of integer design variables (the number of parallel switching cells in each converter leg position) and continuous design variables (the proportion of switching losses taken by each cell), together with linear and nonlinear constraints.**

Keywords*— *Active neutral-point clamped (ANPC), design optimization, switching-cell array (SCA), standardized design, surrogate optimization.

I. INTRODUCTION

Nowadays, engineering designs focus on increasing the standardization of the design process in order to achieve the optimal or near-optimal compatible design in a reasonable amount of time. Besides, to maintain the competitive edge in the growing industry, the designers have to make the best utilization of existent resources to satisfy the most critical consumer demands.

Amongst power electronics systems, an inevitable increase in the adoption of power electronics converters has taken place in recent years leading to dispersion in power electronics converter design.

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Essentially, power converter design is complex due to its heterogeneous and multidisciplinary nature and its wide range of specifications and applications. This complexity has been tackled by experienced design engineers through educated initial choices and partial semi-automated design procedures, often involving some stages of trial and error. Each designer tends to lean towards the specific design strategies they are more confident with. However, the ability and professional expertise of the designer usually lead to good but not optimum designs. Overall, this has traditionally led to a wide range of design approaches and a lack of standardization in power converter design, which has also contributed to a lack of standardization and optimization in components and manufacturing processes.

The search for standardization in power converter design is motivated by the potential of a significant decrease in design time, a significant decrease in converter cost, and an increase in converter performance features. In the literature, one can only find a few attempts to pursue such standardization. However, they are recently receiving more attention due to the potential benefits they can bring. In summary, two main approaches are found in the literature to standardize the design of power converters:

1) Series and/or parallel combination of a basic power converter module, which consists of a power electronic block forcing either a dc or ac voltage/current at the block interfaces [1].
2) Use of multilevel converter topologies, which produce voltage/current waveforms with multiple possible values [2], [3].

The approach presented in [3] is based on the use of multilevel active neutral-point-clamped (ANPC) topologies. The ANPC topology can be used to produce power converter legs with scalable voltage and current ratings from standard components. Subsequently, these converter legs can be used to implement both dc-dc and dc-ac converters, with and without galvanic isolation. An array of switching cells, shown in Fig. 1(a), can be employed for this purpose. Each switching cell (SC), shown in Fig. 1(b) is formed by an active switch with an antiparallel diode, a gate driver (GD), and a gate-driver power supply (GDPS) so that the SC is self-powered. By an appropriate interconnection of the SCs, ANPC legs with a different number of levels can be formed. The configuration of the legs will define the leg voltage and current ratings.

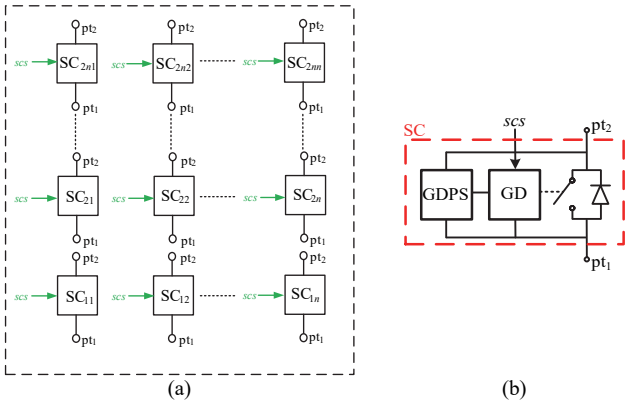

Fig. 1. Switching cell array (SCA) device. (a) A $2n \times n$ SCA. (b) Basic block diagram of a switching cell.

For instance, as shown in Fig. 2, a 6x3 SCA could be used to implement ANPC legs with two, three, and four levels. The spare SCs in blue can then be connected in parallel in strategic SC positions within the leg increasing the redundancy of these positions. Overall, by increasing the number of levels, the leg voltage rating increases while the leg current rating decreases.

Reference [4] illustrates in selected examples the benefits in terms of efficiency and reliability that the finer granularity of SCA-based power converter design can bring.

SCA-based power converter legs present degrees of freedom (DoF) in their configuration and operation to reduce the total losses and properly distribute the losses among the SCs. An additional DoF might be the selection of the type of SCs used to form the SCA. One can envision three types of SCs: standard SCs (balanced conduction and switching performance), SCs optimized for switching (better switching performance than conduction performance), and SCs optimized for conduction (better conduction performance than switching performance).

To obtain the best possible performance, it is key to properly exploit these DoFs, while this has not yet been explored in the literature. This article proposes an automatic design optimization approach to do so and discover the optimal design configuration and operation in different scenarios.

The article is organized as follows. Section II defines the optimization problem. Section III presents and discusses the optimization results under different scenarios. Finally, Section IV outlines the conclusions.

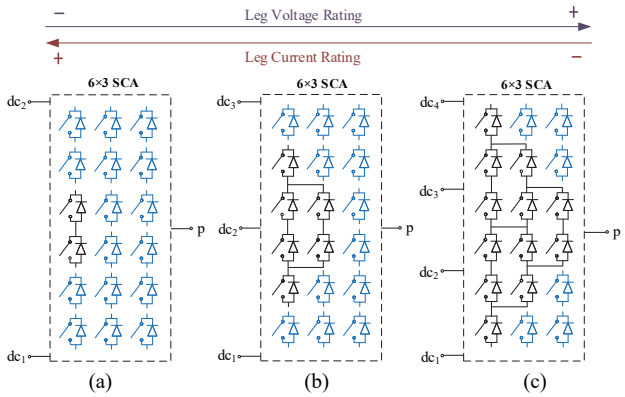

Fig. 2. Examples of 6x3 SCA leg configurations. (a) Two-level. (b) Three-level. (c) Four-level.

II. Definition of the Optimization Problem

A. Conversion Systems under Design

Two types of conversion systems are considered in order to illustrate the design optimization approach: a synchronous buck dc-dc converter and a three-phase dc-ac converter. The optimization problem is formulated in order to design the converter legs required in each case. Both two-level and three-level legs are considered, while the extension to a higher number of levels would be fairly straightforward.

1) Synchronous Buck Dc-Dc Converter: The conversion system is shown in Fig. 3. The load is modeled as a current source. The topology is bidirectional in power flow, but due to its inherent symmetry, without loss of generality, it will be assumed that the load current has a positive constant value $I_L > 0$. The value of the inductance L is also assumed to be large enough to neglect the inductor current ripple so that $i_p \approx I_L$.

a) Two Levels: As shown in Fig. 3(a), the converter leg is formed by two switch positions: S_1 and S_2, that can be configured with one or more parallel SCs. Both switch positions are operated in a complementary manner.

For $i_p > 0$, switching losses occur in S_2 while for $i_p < 0$, they concentrate in S_1.

The average value of the output voltage can be approximated by

$$V_o = d_2 \cdot V_i \tag{1}$$

where d_2 is the duty cycle of the connection to point 2.

b) Three Levels: As shown in Fig. 3(b), the converter ANPC leg is formed by six switch positions: S_1, S_2, …, and S_6 that can be configured with one or more parallel SCs.

The ANPC leg in Fig. 3(b) can be operated as described in [5] with three switching states to connect to the three dc-link points that minimize the conduction loss. For $i_p > 0$, switching losses occur in blue devices, while for $i_p < 0$, they concentrate in orange devices. The topology and operating principle offer the possibility of distributing the switching loss between the blue devices S_2 and S_6 and between the orange devices S_3 and S_5.

The blocking voltage of all switches in Fig. 3(b) is half the blocking voltage in Fig. 3(a). Thus, the voltage rating of the switches can be halved.

The average value of the output voltage can be obtained as

$$V_o = d_2 \cdot (V_i/2) + d_3 \cdot V_i \tag{2}$$

where d_2 and d_3 are the duty cycle of the connection to points 2 and 3, respectively.

2) Three-Phase Dc-Ac Converter: The conversion system is shown in Fig. 4. The load is modeled as a balanced three-phase sinusoidal current source with isolated neutral. The value of filter inductance L and capacitance C is also assumed to be large enough to neglect the inductor current ripple.

The converter synthesizes a fundamental three-phase voltage v_a, v_b, and v_c, which can be expressed in normalized terms as

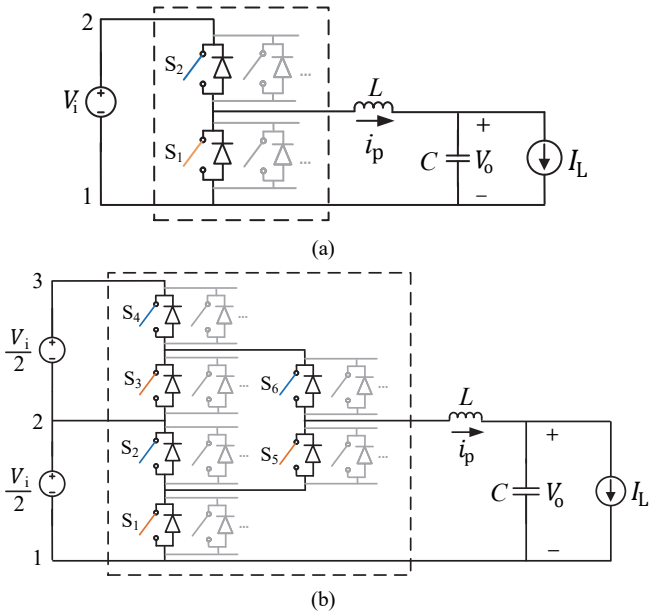

Fig. 3. Synchronous buck dc-dc converter. (a) Two levels. (b) Three levels.

$$
\begin{aligned}
d_a &= \frac{m}{\sqrt{3}} \cdot \cos(\theta) \\
d_b &= \frac{m}{\sqrt{3}} \cdot \cos\left(\theta - \frac{2\pi}{3}\right) \\
d_c &= \frac{m}{\sqrt{3}} \cdot \cos\left(\theta + \frac{2\pi}{3}\right)
\end{aligned} \tag{3}
$$

where θ is the ac-side line-cycle angle, and m is the modulation index ($m \in [0,1]$ in the linear modulation range).

The PWM approach presented in [6] is assumed to determine the duty cycles of connection of each leg ac terminal x to each dc-link terminal y, designated as d_{xy}.

a) Two Levels: As shown in Fig. 4(a), each converter leg is analogous to the one in Fig. 3(a) and they share the same operating principle and basic features.

According to (3) and a typical modulation approach, the duty cycles of connection of each leg ac terminal to each dc-link terminal can be calculated as

$$
\begin{aligned}
d_{off} &= \frac{\max[d_a,d_b,d_c] + \min[d_a,d_b,d_c]}{2} \\
d_{a1} &= 0.5 - d_a + d_{off} \\
d_{b1} &= 0.5 - d_b + d_{off} \\
d_{c1} &= 0.5 - d_c + d_{off} \\
d_{a2} &= 1 - d_{a1} \\
d_{b2} &= 1 - d_{b1} \\
d_{c2} &= 1 - d_{c1}.
\end{aligned} \tag{4}
$$

b) Three Levels: As shown in Fig. 4(b), each converter leg is analogous to the one in Fig. 3(b) and they share the same operating principle and basic features.

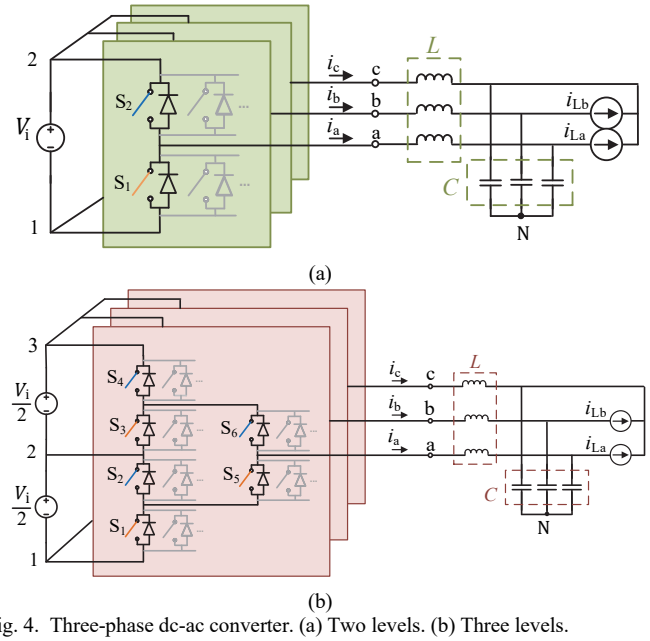

Fig. 4. Three-phase dc-ac converter. (a) Two levels. (b) Three levels.

According to (3) and the modulation approach presented in [6], the duty cycles d_{xy} can be calculated as

$$
\begin{aligned}
d_{a1} &= \max[d_a,d_b,d_c] - d_a \\
d_{b1} &= \max[d_a,d_b,d_c] - d_b \\
d_{c1} &= \max[d_a,d_b,d_c] - d_c \\
d_{a3} &= d_a - \min[d_a,d_b,d_c] \\
d_{b3} &= d_b - \min[d_a,d_b,d_c] \\
d_{c3} &= d_c - \min[d_a,d_b,d_c] \\
d_{a2} &= 1 - d_{a1} - d_{a3} \\
d_{b2} &= 1 - d_{b1} - d_{b3} \\
d_{c2} &= 1 - d_{c1} - d_{c3}.
\end{aligned} \tag{5}
$$

B. System Specifications and Fixed Design Variables

Table I presents the system specifications and fixed design variables considered in the formulation of the optimization problem. It outlines the variable names, their description, and the values applied in the optimization runs of Section III. To present the study in a generic case, all variables and parameters are treated in per-unit values. In addition, the power switch in the SC is assumed to be a metal-oxide-semiconductor field-effect transistor (MOSFET) and it is also assumed that all SCs forming a converter leg are mounted on a common heat sink.

C. Design Variables

Two sets of design variables are considered in the optimization problem. The first set consists of the number of parallel SCs in each leg position i and for each SC type, designated as $nc_{i,\text{std}}$, $nc_{i,\text{condop}}$, and $nc_{i,\text{swop}}$. In two-level legs, this accounts for 2 design variables for *hybrid* = 0 and 4 for *hybrid* = 1, while in three-level legs, this accounts for 6 design variables for *hybrid* = 0 and 12 for *hybrid* = 1. They are integer, and thus discrete, design variables.

TABLE I. SYSTEM SPECIFICATIONS AND FIXED DESIGN VARIABLES

Variable Name	Description	Applied Value
mode	Conversion mode 1: dc-dc conversion 2: dc-ac conversion	1or 2
n	Number of leg levels	2 or 3
d_i	Duty cycle of the leg connection to the dc-link point *i* (only for *mode* = 1)	1/*n*
m	Modulation index (only for *mode* = 2)	0.75
φ	Leg current phase-shift with reference to the fundamental component of the leg ac terminal voltage (only for *mode* = 2)	30 degrees
hybrid	Binary variable indicating the type of SCs used 0: Only standard SCs 1: A combination of conduction-optimized SCs and switching-optimized SCs	0 or 1
$P_{\text{cond,std}}$	Normalized conduction power loss of a standard SC at a normalized leg current equal to 1	1
$P_{\text{cond,condop}}$	Normalized conduction power loss of a conduction-optimized SC at a normalized leg current equal to 1	0.5
$P_{\text{cond,swop}}$	Normalized conduction power loss of a switching-optimized SC at a normalized leg current equal to 1	2
$P_{\text{sw,std}}$	Normalized switching power loss of a standard SC at a normalized leg current equal to 1 and at the carrier frequency	1
$P_{\text{sw,condop}}$	Normalized switching power loss of a conduction-optimized SC at a normalized leg current equal to 1 and at the carrier frequency	2
$P_{\text{sw,swop}}$	Normalized switching power loss of a switching-optimized SC at a normalized leg current equal to 1 and at the carrier frequency	0.5
T_{hs}	Normalized value of the heat sink temperature	0.75
T_{jmax}	Normalized maximum value of the junction temperature of the SC power switch	1
$R_{\text{th,j-h}}$	Normalized thermal resistance from the junction of the SC power switch to the heatsink	0.25
λ_0	Normalized SC failure rate at the maximum junction temperature	1
minlev	Minimum number of available leg levels to continue operation	2

On the other hand, since in the ANPC topology the switching losses can be distributed among the different SC types connected in parallel, and among certain leg positions, a second set of design variables is introduced consisting on a weight assigned to each position and SC type to determine the proportion of the switching losses that this SC will be withstanding, designated as $sw_{i,\text{std}}$, $sw_{i,\text{condop}}$, and $sw_{i,\text{swop}}$. In two-level legs, this accounts for 0 design variables for *hybrid* = 0 and 4 for *hybrid* = 1, while in three-level legs, this accounts for 4 design variables for *hybrid* = 0 and 12 for *hybrid* = 1. They are continuous design variables.

The two sets of design variables are summarized in Table II.

TABLE II. DESIGN VARIABLES

Number of parallel switching cells in leg position *i*	Switching weights in leg position *i*
$nc_{i,\text{std}}$	$sw_{i,\text{std}}$
$nc_{i,\text{condop}}$	$sw_{i,\text{condop}}$
$nc_{i,\text{swop}}$	$sw_{i,\text{swop}}$

D. Objective Function

The goal of an optimization is to find the value of the design variables that minimize a given objective or cost function. In this work, the selected objective function to be minimized incorporates three paramount aspects: leg efficiency, leg reliability, and leg simplicity. It is formulated as

$$Obj = W_{\text{L}} \cdot \frac{P_{\text{LT}}}{P_{\text{LT,max}}} + W_{\text{F}} \cdot \frac{\lambda_{\text{leg}}}{\lambda_{\text{leg,max}}} + W_{\text{C}} \cdot \frac{CP}{CP_{\text{max}}}. \quad (6)$$

The efficiency is accounted for through the first term, which includes the total leg losses P_{LT}. The reliability is accounted for through the second term, involving the leg failure rate λ_{leg}. Finally, the third term introduces the leg complexity *CP*, computed as a function of the number of leg SCs and the diversity of SC types, as will be shown in the next subsection. In order to properly combine aspects of different nature and with different units, P_{LT}, λ_{leg}, and *CP* are normalized dividing by their maximum values ($P_{\text{LT,max}}$, $\lambda_{\text{leg,max}}$, and CP_{max}, respectively). The value of the design variables that produce these maximum values is usually obvious and thus, these maximum values are easily obtained. In addition, each of the three terms contains a weighting factor (W_{L}, W_{F}, and W_{C}) to allow the designer to assert priorities. The value of each of these weighting factors can be selected between 0 and 1 according to the design priorities to obtain the desired tradeoff solution. Moreover, if it is forced that $W_{\text{L}} + W_{\text{F}} + W_{\text{C}} = 1$, then the objective function provides the cost of the design in the per-unit value of the cost of the worst possible design.

E. Models

To be able to compute the objective function as a function of the design variables, proper models need to be introduced. These models need to be computationally efficient, as a large number of function evaluations will need to be performed in each optimization run, while also being accurate enough to capture the main performance features of the system.

The selected models are described in detail in [4] and [7]. In the following, their main characteristics are summarized. In order to perform a generic study, the models operate with all variables in per-unit values.

1) Thermo-Electrical Model: A steady-state average thermo-electrical model is used, which allows estimating the losses and temperature of all SCs within the leg. The model is based on the following assumptions:

- The power switch in each SC is a MOSFET.
- For simplicity, diode reverse-recovery losses are assumed to be negligible.
- If several identical SCs are connected in parallel, it is assumed that they all concurrently conduct the same share of the current in the ON-state. It is also assumed that, in each switching cycle, one of them is turned on first and turned off last in order to take all the switching losses of the group. The selected SC for taking the switching losses is alternated through the subsequent switching cycles so that, on average, all parallel SCs withstand the same switching loss.

The total power loss of a MOSFET can be computed as

$$P_T = P_{cond} + P_{sw} \tag{7}$$

where P_{cond} is the conduction loss and P_{sw} is the switching loss.

The conduction loss of a MOSFET can be estimated as

$$P_{cond} = R_{DS(on)} \cdot I_{rms}^2 \tag{8}$$

where $R_{DS(on)}$ is the ON-state resistance of the MOSFET and I_{rms} is the rms value of the MOSFET current.

The switching loss of a MOSFET can be calculated as

$$P_{sw} = E_{sw} \cdot f_s \tag{9}$$

where $E_{sw} = E_{on} + E_{off}$, E_{on} is the turn-on energy loss, E_{off} is the turn-off energy loss, and f_s is the switching frequency.

From the value of the normalized SC total loss, P_T, the normalized value of the SC temperature can be calculated as [8]

$$T_j = P_T \cdot R_{th,j\text{-}h} + T_{hs} \tag{10}$$

where T_{hs} is the normalized heat sink temperature, $R_{th,j\text{-}h}$ is the normalized thermal resistance from the junction of the MOSFET to the heat sink, and T_j is the normalized value of the MOSFET junction temperature.

2) Reliability Model: The leg failure rate is computed with a Markov chain model based on the following assumptions:

- SCs always fail in open circuit. This can be guaranteed through the inclusion of an intelligent electronic fuse, as proposed in [9].
- For the sake of simplicity in the calculations, it will be assumed that the failure rate of a SC does not change as the parallel SCs fail in open circuit. This can be ensured by decreasing the load current as SCs fail.

From the normalized value of the SC temperature, the normalized value of the SC failure rate can be obtained as [10]

$$\lambda = \lambda_0 \cdot \pi_T \tag{11}$$

where λ_0 is the normalized failure rate at $T_j = 1$ and π_T is the correction factor according to the actual temperature value. Factor π_T can be calculated as [10]

$$\pi_T = e^{4640 \cdot \left(\frac{1}{373} - \frac{1}{T_j \cdot 100 + 273}\right)}. \tag{12}$$

Once the failure rate of each SC has been calculated, the failure rate of a subsystem of *pr* SCs connected in parallel can be calculated from the Markov model of this subsystem [7]. Finally, according to the corresponding leg Markov model [7], the overall leg failure rate can be obtained.

3) Complexity Model: The leg complexity is quantified taking into account the total number of SCs to configure the leg and the diversity of SCs used, as

$$\begin{aligned} CP &= \textstyle\sum_{i=1}^{N} nc_{i,std} && \text{for } hybrid = 0 \\ CP &= 2 \cdot \textstyle\sum_{i=1}^{N} (nc_{i,condop} + nc_{i,swop}) && \text{for } hybrid = 1 \end{aligned} \tag{13}$$

where N is the number of power converter leg positions. As can be observed, a factor of 2 is introduced in the case of *hybrid* = 1 to increase the complexity due to the need for two different SC types, with reference to the case *hybrid* = 0, where only one type of SC is needed.

F. Constraints

The value of the design variables that minimize the objective function must be found subject to some constraints that limit the design space to guarantee that the solutions are physically meaningful and feasible, and to reduce the optimization algorithm search effort. In this case, the following constraints are introduced.

In the case of using only standard SCs (*hybrid* = 0), the number of cells are limited according to

$$1 \le nc_{i,std} \le 5. \tag{14}$$

In the case of *hybrid* = 1, the number of cells are limited according to

$$\begin{aligned} 0 \le nc_{i,condop} \le 5 \\ 0 \le nc_{i,swop} \le 5 \\ nc_{i,condop} + nc_{i,swop} \ge 1. \end{aligned} \tag{15}$$

Constraints (14) and (15) force the minimum number of SCs in each leg position to 1. They also limit the maximum number of SCs in parallel of the same type to 5, in order to limit the design space and also because it has already been shown in previous works that as the paralleling increases, the incremental benefits in terms of efficiency and reliability decrease [4].

Another set of constraints specify that the values of the switching weights must be bound between 0 and 1, as

$$\begin{aligned} 0 \le sw_{i,std} \le 1 \\ 0 \le sw_{i,condop} \le 1 \\ 0 \le sw_{i,swop} \le 1. \end{aligned} \tag{16}$$

Finally, an additional set of constraints is also established to limit the junction temperature of each SC power switch to its maximum allowed value, as

$$T_{jk} \le T_{jmax} \tag{17}$$

where k is the number of SCs used.

G. Optimization Algorithm

The surrogate optimization algorithm from the MATLAB global optimization toolbox is selected to solve the optimization problem. It is well suited for problems with both continuous and discrete design variables and linear and nonlinear constraints. This solver has proven to exhibit a great performance while it is reliable and easy to handle.

III. Optimization Results

The search for the optimum design has been carried out under different scenarios and several sets of objective function weights. Both the dc-dc (*mode* = 1) and the three-phase dc-ac (*mode* = 2) conversion configurations have been considered, with two-level (n = 2) and three-level (n = 3) converter legs. In each of these cases, the use of only standard SCs (*hybrid* = 0) and the use of a combination of conduction-optimized SCs and switching-optimized SCs (*hybrid* = 1) has been studied. The remaining system specifications are detailed in Table I.

Table III presents the objective function normalization factors employed in each case.

TABLE III. OBJECTIVE FUNCTION NORMALIZATION FACTORS

mode	*n*	$P_{LT,max}$ [p.u.]	$\lambda_{leg,max}$ [p.u.]	CP_{max} [p.u.]
1	2	3.25	3.62	40
	3	6.7	2.1	120
2	2	2.5	2.4	40
	3	4.4	1.6	120

To obtain the global optimum result in each scenario, the surrogate algorithm requires less than 500 function evaluations. Fig. 5 illustrates the optimization progress in one of these cases. The evaluation of one design in each iteration takes less than 0.25 seconds in a personal computer with an Intel Core i5 processor and 16 GB of RAM.

Fig. 6 presents the optimal designs in the dc-dc power conversion case with $I_L > 0$. For four different combinations of the objective function weights (W_L, W_F, and W_C), the number of parallel SCs in each leg position is indicated, together with the corresponding optimal value of the switching weight within brackets, wherever relevant.

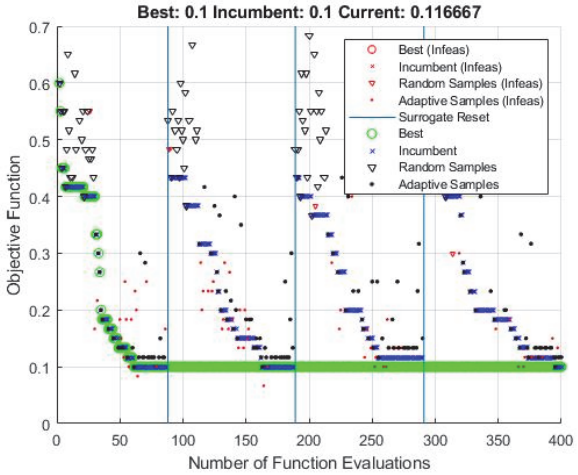

Fig. 5. Surrogate optimization progress window.

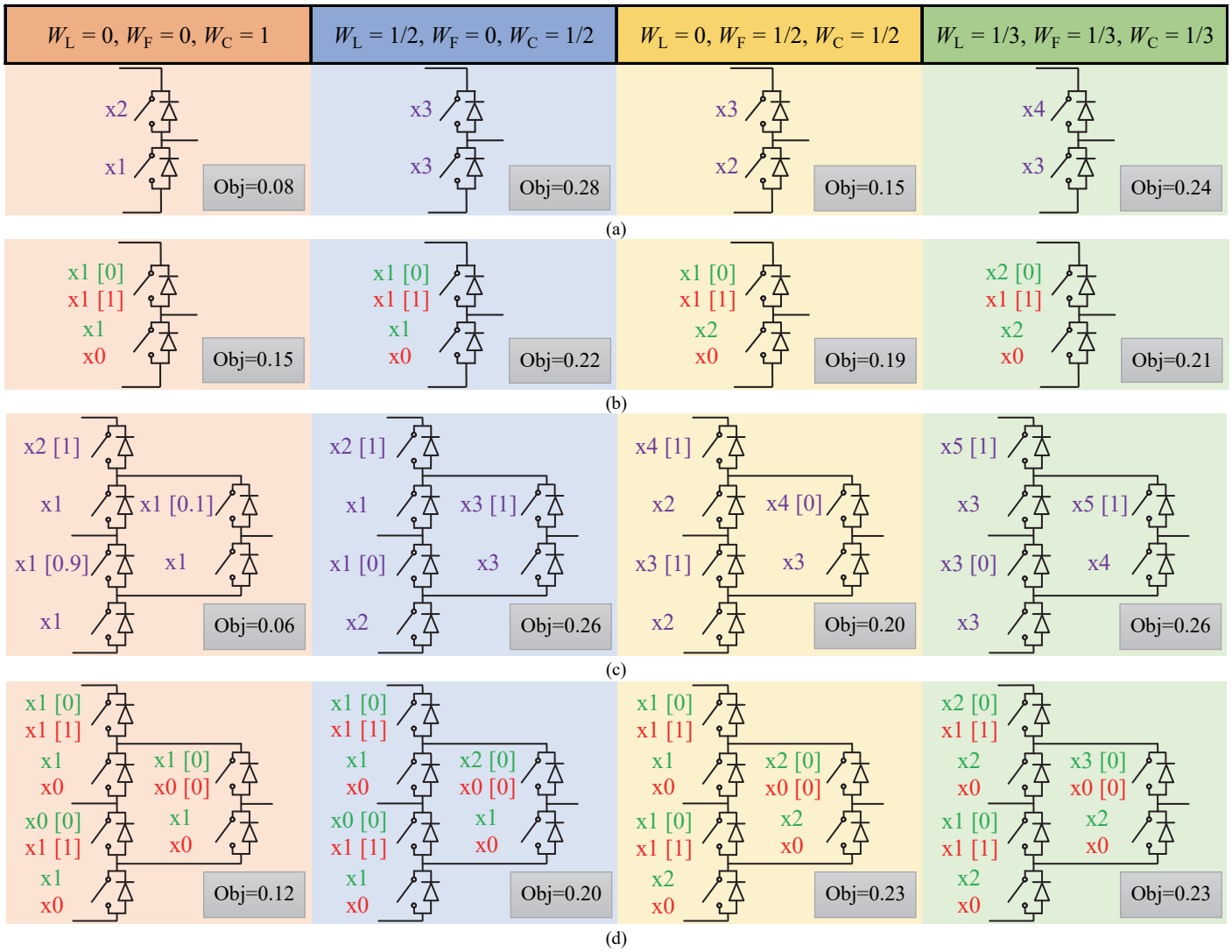

Fig. 6. Optimal designs in the dc-dc power conversion case with $I_L > 0$. Standard SCs are shown in purple, conduction-optimized SCs are shown in green, and switching-optimized SCs are shown in red. The number of cells z is indicated as xz. Switching weights for each group of SCs that can take switching losses are shown within brackets. (a) $n = 2$ and *hybrid* = 0. (b) $n = 2$ and *hybrid* = 1. (c) $n = 3$ and *hybrid* = 0. (d) $n = 3$ and *hybrid* = 1.

Fig. 6(a) and Fig. 6(b) present the results under the two-level case with *hybrid* = 0 and *hybrid* = 1, respectively. It can be observed that in the first column, where the only goal is to minimize complexity, two SCs are necessary in the top position to meet the maximum temperature constraint. In the second column, which combines the power loss and complexity goals, a larger number of SCs is selected. Adding more SCs reduces the leg losses, but as the number of parallel SCs increases, the reduction in losses decreases, and at some point, this reduction in losses does not compensate for the increased complexity. In the third column, combining failure rate and complexity, the resulting optimum configuration is similar to the previous case but slightly different. In the fourth column, where the three goals are combined, the optimum number of SCs rises slightly compared to previous cases. Since $I_L > 0$, switching losses always take place in the top leg position, not in the bottom. This explains the asymmetry of the optimum solutions. Please, also note that the switching weights indicate that the SCs optimized for switching withstand all switching losses, as expected. The objective function value indicated for each optimum design represents its cost as a per-unit value of the cost of the worst design. Please, note that, in some cases, the solution using standard SCs presents a lower cost, while in some others, the combination of conduction-optimized and switching-optimized SCs produces a lower cost. Thus, each type of solution can be optimal depending on the design specifications and goals.

Fig. 6(c) and Fig. 6(d) present the results under the three-level case with *hybrid* = 0 and *hybrid* = 1, respectively. The conclusions drawn are similar as in the two-level case. In the first column, it is interesting to note how the switching weights determine a sharing of the switching losses among two standard SCs to be able to meet the maximum SC temperature constraint. In general, though, the optimal switching weights indicate that it is better to focus switching losses in a specific group of SCs.

Fig. 7 presents the optimal designs in the three-phase dc-ac power conversion case. Fig. 7(a) and Fig. 7(b) present the results under the two-level case and Fig. 7(c) and Fig. 7(d) present the results under the three-level case. In this conversion scenario,

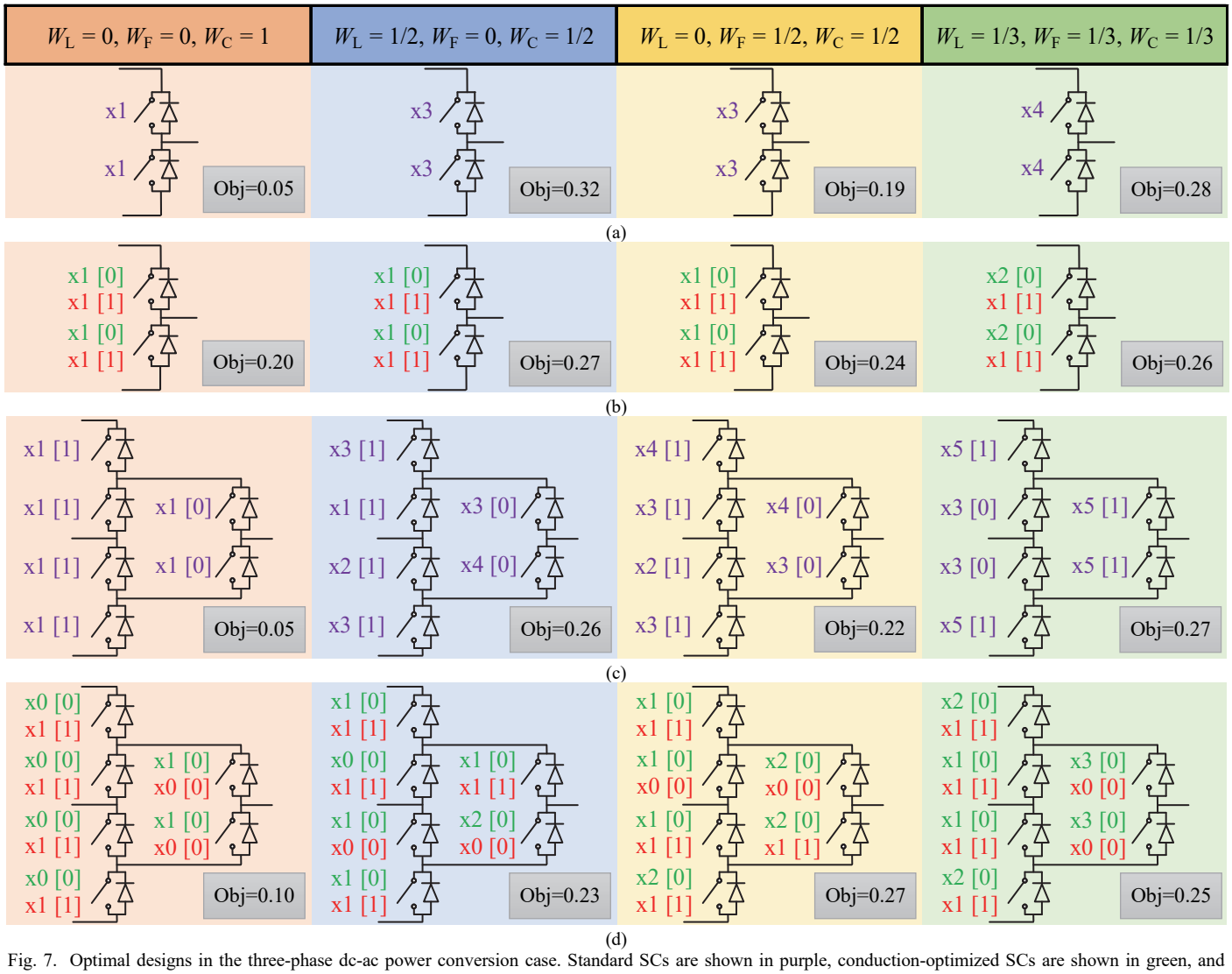

Fig. 7. Optimal designs in the three-phase dc-ac power conversion case. Standard SCs are shown in purple, conduction-optimized SCs are shown in green, and switching-optimized SCs are shown in red. The number of cells *z* is indicated as x*z*. Switching weights for each group of SCs that can take switching losses are shown within brackets. (a) *n* = 2 and *hybrid* = 0. (b) *n* = 2 and *hybrid* = 1. (c) *n* = 3 and *hybrid* = 0. (d) *n* = 3 and *hybrid* = 1.

the operation of the leg is fully symmetrical. In general, this leads to a symmetrical optimal configuration of the leg. However, it is interesting to note that in the second and third columns of the three-level case, the optimal configuration of the legs is asymmetrical. The superiority of this asymmetrical configuration compared to other close symmetrical configurations has been confirmed.

IV. Conclusion

An automated design optimization approach based on a surrogate algorithm has been presented to determine the optimal design configuration of SCA-based power converter legs. The number of parallel SCs in each converter leg position and the distribution of switching losses among SCs have been selected as the system design variables, and the optimization process is in charge of finding the value of them that minimizes a weighted objective function incorporating three distinct aspects: efficiency, reliability, and simplicity. The design optimization results, although highly dependent on the competing objectives, weighting factors, and the proposed analytical models, highlight important features of the standardized design of power converters based on SCA devices, such its inherent flexibility to accommodate different conversion scenarios and operating conditions.

The presented surrogate-based optimization has proven to be a very effective and powerful tool for obtaining global optimal design configurations compared to traditional design optimization procedures.

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