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An Intelligent Electronic Fuse for Selective Isolation of Faulty Switching Cells in Power Electronic Converter Legs to Guarantee Continuous Operation

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***Abstract*- This paper proposes a novel device designated as an intelligent electronic fuse (iFuse) intended to be connected in series with any current-bidirectional voltage-unidirectional active switch present in a power converter. The iFuse duty is to selectively isolate its series-associated switch from the rest of the converter circuit immediately after detecting that this switch has failed in short circuit. Nonetheless, it maintains the reverse (free-wheeling) current path originally offered by the failed switch. The failure detection is typically performed when the failed switch causes a shoot-through event. Therefore, the iFuse is able to block large currents. The iFuse allows increasing the power-converter fault tolerance and reliability with regard to switch short-circuit failures, as in converters featuring switches in parallel, redundant legs, and multilevel neutral-point-clamped topologies. The reliability model analysis of a two-level converter leg with two parallel switches per position, reveals that its reliability can be increased up to four times when an iFuse is implemented in series with each switch. The iFuse device feasibility and good performance is verified through experimental tests, proving that it can detect and isolate the associated-switch failure in 6 μs, while stopping short-circuit currents of up to 1 kA without incurring in harmful *di*/*dt* values.**

I. Introduction

At present day, power electronics is an essential subsystem in an extensive range of applications and power ratings [1]. Some of these applications are categorized as critical, that is, the continuity of the service must be assured at all time, mainly because of safety or economic reasons [2], not allowing an unexpected system shutdown, although a degraded operation can be eventually accepted [3]. Therefore, fault-tolerant operation of the system, and specifically of the power electronics converter, is required [3]. For example, in electric vehicles, a motor drive failure may risk the passenger safety [2]–[4], and a limp-home mode is desirable.

It is estimated that typically 50% of faults in power converters are due to power switch failures [5], [6], which are typically caused by power-semiconductor damage or switch-gate-driver damage or malfunction [7]. Moreover, these failures typically cause the power switch to remain in a permanent OFF state; i.e., a switch open-circuit failure (OCF) , or to remain in a permanent low-ohmic ON state; i.e., a switch short-circuit failure (SCF) [8].

The ease in achieving fault tolerance depends on the type of switch fault. In a voltage-source converter topology, a switch OCF provides inherent fault isolation. In contrast, a switch SCF implies the short-circuit of a voltage source; i.e., a shoot-through event, when the switch complementary to the failed switch is turned on.

A simple example is power converters employing parallel switches for reduced conduction losses, as in the two-level three-phase traction inverter of Tesla Model S, with six parallel discrete IGBTs per switch position [9]. Thanks to the inherent redundancy provided by the parallel switches, these converters can sustain multiple switch OCFs. However, a SCF of one of the switches forces disabling the whole converter leg in order to avoid a shoot-through event, and converter operation must stop.

Another example are converters employing active neutral-point-clamped (ANPC) topologies, which also feature inherent redundancy thanks to the multiple leg switching states available. As shown in [10], when SCFs occur in an ANPC leg, the resulting switching states feature, on average, less available connections to the dc-link points than in the switch OCF case.

There are solutions in the literature to reduce the impact caused by switch SCFs on converters fault tolerance. These solutions consist on introducing additional hardware in order to isolate the switch in SCF, or the part of the circuit affected by the switch SCF, from the rest of the circuit. For instance, [11]–[13] present dc-ac fault-tolerant power converters with leg redundancy. In [11] a fast fuse in series with each active switch

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is employed, such that when a shoot-through event occurs due to a switch SCF, the fuses are blown, isolating the short-circuit failed switches from the switching-leg output. However, there is no guarantee that the fuse in series with the short-circuited switch will blow, since the fuse of the complementary switch could blow first. A more advanced solution is proposed in [12] for the same topology, where again a fast fuse is placed in series with each active switch but the fuses are selectively blown with a robust active switch (thyristor) and the energy stored in the dc link. In contrast, [13] presents a two-level three-phase dc-ac converter employing two switches in series per position (one of them in permanent ON state) and two legs per phase (one of them in stand-by). When a switch SCF or OCF occurs on the active leg, all switches in this leg are turned off and the redundant leg is enabled and operated with the same switching strategy as the faulty leg previous to the fault. In [10], the connection of the active switches to the dc-link capacitors in an ANPC leg can be opened through four-quadrant (4Q) switches, in order to cut the short-circuit current path. Similarly, in [14], the connection of a three-level ANPC leg to the dc-link neutral point can be opened through a fast fuse placed in the connection path. As in [11], these fuses are deliberately blown with thyristors and the energy stored in the dc-link capacitors. After opening the dc-link-neutral-point connection, an alternative modulation strategy is employed to operate the converter with the remaining switching states. A similar approach is proposed in [15] for a multilevel converter employing a flying-capacitor topology, where 4Q switches are employed to disconnect the necessary flying capacitors to avoid the shoot-through event caused by a switch SCF.

The presented solutions mitigate the consequences of switch SCFs, but present some drawbacks. For instance, fuses are bulky [16] and its typical melting profile requires a short-circuit current much higher than the nominal current to have reduced melting times [16], which could lead the healthy devices in the short-circuit current path to fail. Also, the fuse resistance and stray inductance increase the conduction losses and voltage spikes during switching transitions in normal operation [2]. Replacing fuses with switches allows performing the isolation action in less time and yields less conduction losses during normal operation [13]. Nonetheless, all the solutions employing switches to open the short-circuit current path caused by a switch SCF [10], [13], [15] rely on a centralized control that first has to detect the failure and then commands the turn off of the corresponding protection switch.

Typical solutions to open the short-circuit current path caused by a switch SCF without relying on a centralized control employ either switch gate drivers with short-circuit protection (GDSCP), solid-state circuit breakers (SSCB) [17], or electronic fuses (eFuses) [18]–[20]. It should be noted that eFuses and SSCBs are equivalent in their basic functionality when protecting against a short-circuit current and, from now on, both will be referred as eFuses. For instance, eFuses could replace the fast fuses employed in the fault-tolerant converters from [11], [12], and [14].

A general solution would be employing a GDSCP for each switching device or placing an eFuse in series with each device. Nonetheless, this general solution is not satisfactory since it cannot provide selective isolation of the short-circuit-failed switch. This is illustrated in Fig. 1, which assumes an initial switch SCF on a two-level leg with two parallel devices per position.

As shown in Fig. 1(a), when the GDSCP is employed as a protection mechanism, the short-circuit current flowing through switches S_{1a} and S_{1b} is detected by their corresponding GDSCP and both switches are subsequently turned off. This scenario ends up in a state where the leg output terminal can no longer be connected to dc-link point 1 (it is permanently connected to point 2), and the leg must stop its operation.

As shown in Fig. 1(b), when eFuses are employed as protection devices, and assuming that they are configured to trip as soon as a short-circuit current is detected, all three eFuses in the short-circuit path will trip, leaving the leg output terminal floating. The leg output terminal can no longer be connected to point 1 and the leg must stop operating.

Therefore, currently existing standalone protection devices do not allow the selective isolation of the switches in SCF, which is necessary to take full advantage of the switch-level redundancy offered by many topologies. Consequently, it is desirable to conceive a device with such selective isolation capability, able to transform all switch failures into an equivalent OCF.

This paper proposes a new device to accomplish the above purpose, designated as intelligent electronic fuse (iFuse). The iFuse is conceived to be connected in series with a CBVU active switch, performing an automatic continuous monitoring at component level of its associated active switch in order to detect its failure. In case the failure of the associated active switch is detected, the iFuse proceeds to block the forward current path, stopping the eventual short-circuit current and preventing future shoot-through events. Moreover, it also maintains the free-wheeling path that was offered by the active switch previous to the failure. This principle of operation is illustrated in Fig. 1(c), where the iFuse in series with the short-circuit-failed switch opens the short-circuit current path, while the rest of iFuses in the same path remain ON. Thanks to this, the switch SCF isolation process is performed in a stand-alone manner, and the converter leg can reliably continue its operation without any break or change in the operating strategy. Thus, the proposed iFuse allows the fault-tolerant operation of power converters under switch SCFs taking full advantage of the converter switch-level redundancy, and significantly improving the reliability of the converter itself and the system where it is employed.

The manuscript is organized as follows. Section II describes the functional blocks constituting the iFuse and its working principle. Section III describes which kind of power converters would be most benefited in terms of fault-tolerance by incorporating iFuses. Section IV demonstrates the reliability increase thanks to the use of the iFuse in a two-level inverter leg with two parallel switches per position. Section V presents

experimental results to demonstrate the feasibility and good performance of the proposed iFuse device. Finally, Section VI outlines the conclusions.

II. iFuse Configuration and Operating Principle

Fig. 2 presents a diagram of the series connection of an iFuse with a CBVU active switch (S_m). This series connection can be regarded as a new compound device; i.e., a switching cell (SC), featuring power terminals pt1 and pt2, input binary signal *S* for the control of S_m, and output binary signal *st* to report the health status of S_m. The iFuse is composed of an active switch (S_{iF}) together with its driving circuitry, the circuitry to quickly diagnose S_m fault, and the iFuse power supply. S_{iF} is a CBVU switch. This allows maintaining the freewheeling path after the S_m SCF, which in pre-fault condition is offered by S_m antiparallel diode. The diode shown in the iFuse symbol of Fig. 2(a) denotes the availability of the abovementioned free-wheeling path.

Isolated drivers are required to transfer digital signals between the converter control and the converter power circuit. The self-powered-supply circuit conceived in [21] can be used to power the gate driver of S_m (GDPS) and the iFuse circuitry (iFPS) by recycling S_m turn-off switching losses.

Fig. 3 and Fig. 4 show in full detail the circuit of the four main functional blocks making up the proposed iFuse. An n-channel metal-oxide-semiconductor field-effect transistor (MOSFET) is here selected to implement the S_{iF} switch. The S_m-fault automatic-detection circuitry is composed of the forward-current detection circuit (FCDC) and the fault detection logic (FDL). Fig. 4 shows the circuit of the iFPS, following the design of [21] but modified to deliver two voltage supplies, V_{fuse} and V_{cc}, the latter stabilized with linear voltage regulator U_5. The iFPS is isolated from the power converter control and does not require or involve any inductive, capacitive or optical coupling with any circuit outside the SC. Thus, it is not affected by the floating nature and switching voltage of nodes pt1 and pt2. Fig. 5 shows the evolution of the main iFuse analog and digital signals described in this section.

The compound device shown in Fig. 2(a) is to be integrated in a power converter. A SCF of S_m will be typically followed by a switching state where S_m control signal is low ($S = 0$) and a positive current i_S flows through S_m, with reference to Fig. 2(b). The proposed iFuse solution will stand-alone detect this situation to diagnose the SCF of S_m, to then immediately isolate it from the rest of the circuit by blocking its forward current path.

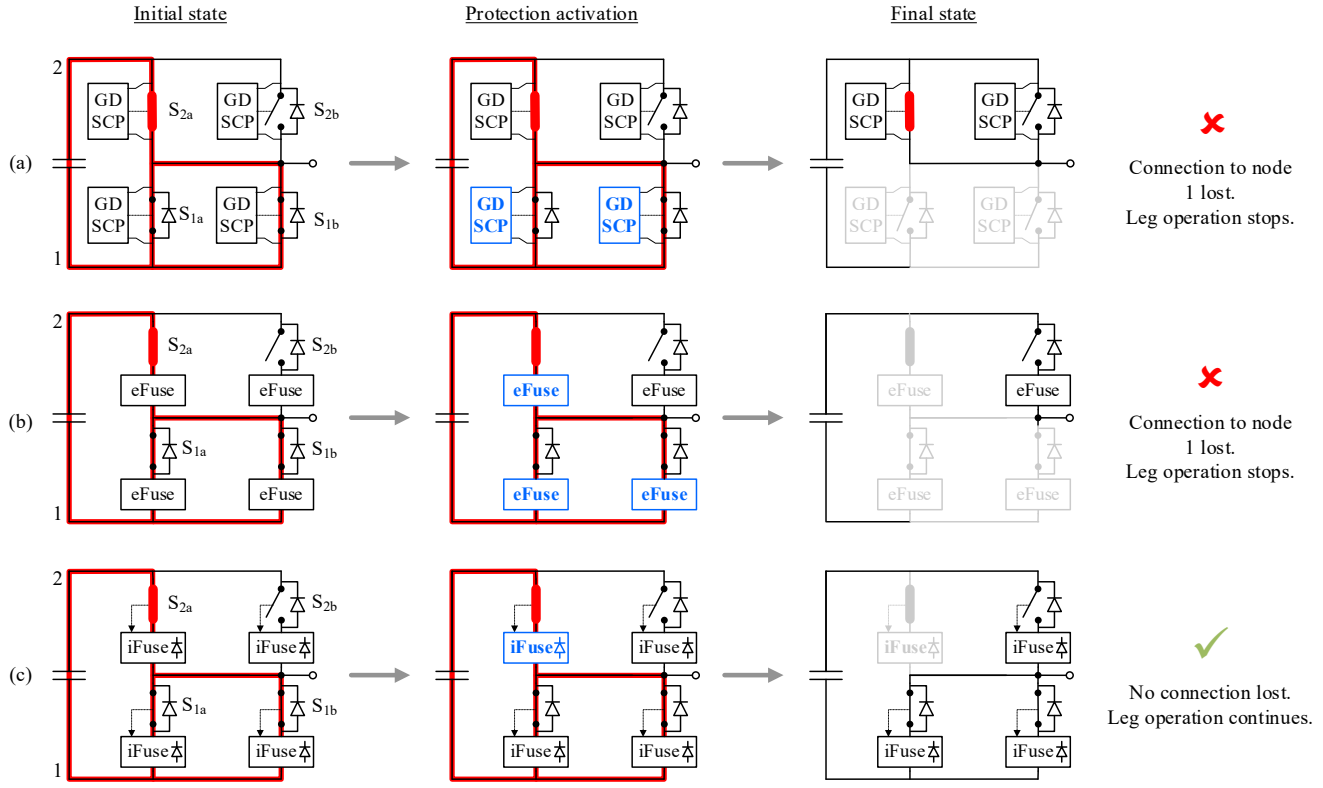

Fig. 1. Chronological evolution (from left to right) of a switch SCF event on a two-level switching leg with two parallel devices per position. The chronogram starts with S_{2a} failing in short circuit and the switching-leg output connected to dc-link point 1, leading to a short circuit of the dc-link capacitor (short-circuit current path marked in red). After the initial state, some of the protective devices are activated (highlighted in blue), leading to the final state where the short-circuit current is interrupted. Three configurations are considered, depending on the device in charge of opening the short-circuit current path: (a) GDSCP. (b) eFuse. (c) iFuse.

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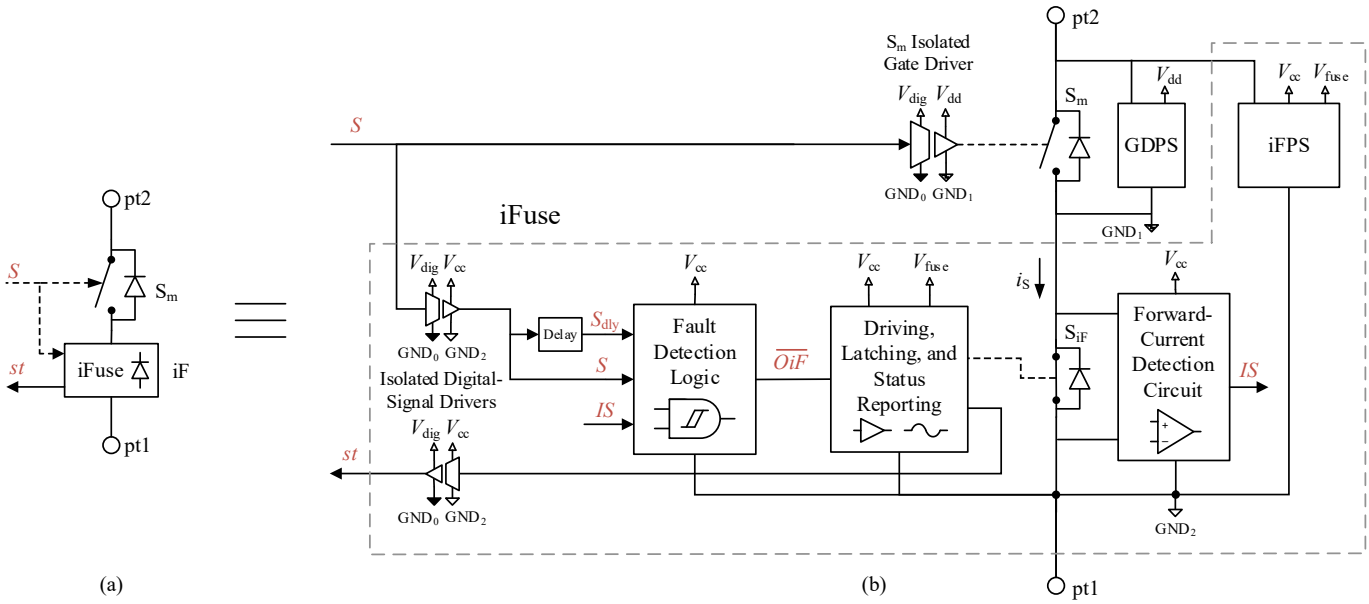


Fig. 2. Diagram of the compound device constituted by switch S_m and the proposed iFuse; i.e. the switching cell. (a) Compact representation of the compound device, showing the iFuse symbol. (b) Expanded view of the iFuse device, showing its internal functional blocks. Relevant digital signals appear in red.

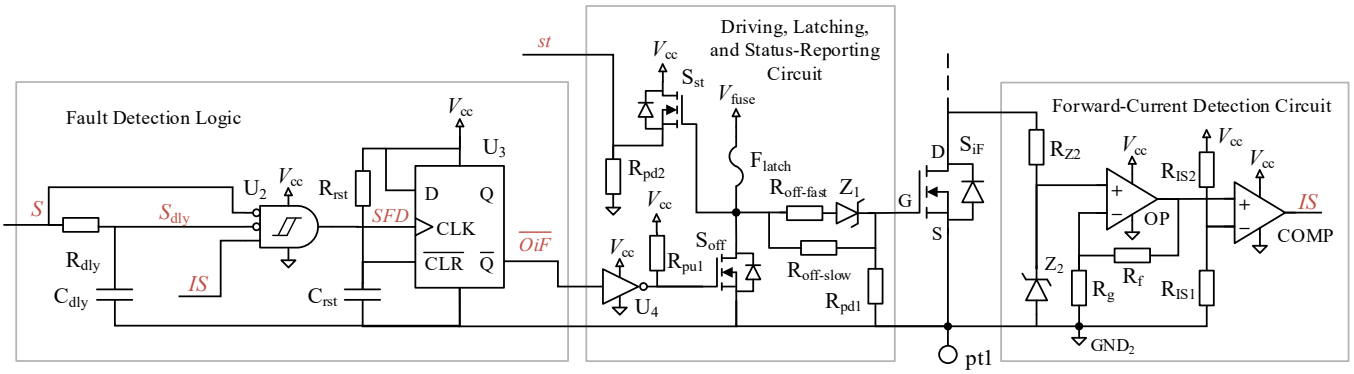


Fig. 3. Schematic of the fault detection logic, the driving, latching, and status-reporting circuit, and the forward-current detection circuit. Relevant digital signals appear in red. All ground symbols are connected to GND_2.

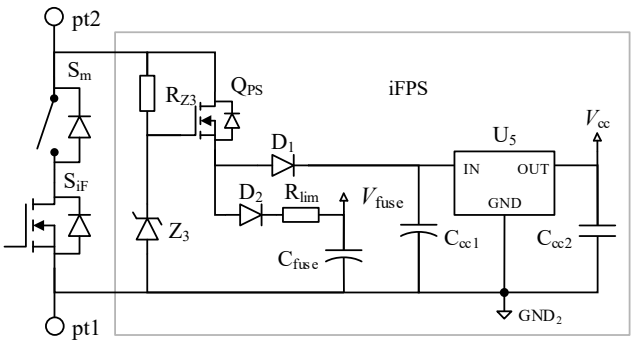


Fig. 4. Schematic of the iFPS circuit.

In normal operation, S_{iF} is kept permanently ON thanks to voltage V_{fuse} feeding S_{iF} gate through fuse F_{latch} (see Fig. 3). During this condition, and since MOSFET S_{iF} acts as a shunt when ON, the FCDC senses the current i_S by amplifying the voltage across S_{iF} with the circuit formed by operational amplifier OP and resistors R_f-R_g. The sensed current is then compared through comparator COMP and resistors R_{IS1}-R_{IS2} to the threshold value $I_{S,th}$, in order to determine if a positive current is flowing through S_m. This is indicated by Boolean variable *IS*, such that

$$IS = 0 \text{ when } i_S < I_{S,th}$$
$$IS = 1 \text{ when } i_S \geq I_{S,th}. \quad (1)$$

It seems then straightforward that the FDL just needs to look for a concurrent $S = 0$ and $IS = 1$ to determine the SCF of S_m.

However, it must be taken into account that the described conditions can also be met during the S_m turn-off transient in normal operation. Therefore, to avoid a false S_m-failure detection, the fault detection must be disabled during this time interval. To do so, a disable signal

$$D = \overline{S} \cdot S_{\text{dly}} \tag{2}$$

is defined, where S_{dly} is a replica of S delayed T_{dis} seconds and generated with R_{dly} and C_{dly} RC network. T_{dis} should be selected to be larger by some margin than the maximum turn-off transient time of S_m.

Finally, the switch fault detection signal

$$SFD = \overline{D} \cdot \overline{S} \cdot IS = \overline{S} \cdot \overline{S_{\text{dly}}} \cdot IS \tag{3}$$

is generated, where $SFD = 1$ indicates the detection of S_m SCF. When signal SFD transitions from 0 to 1, it latches signal $\overline{OiF}$ to zero with the D bistable U_3. Therefore, when a fault is detected $\overline{OiF} = 0$ permanently, causing MOSFET S_{off} to turn on, which performs two actions: turning S_{iF} off by discharging its gate and fusing F_{latch}. Moreover, pull-up resistance R_{pu1} ensures that, in case of failure of the FDL block, the iFuse is engaged, turning S_{iF} off. The D bistable is reset to $\overline{OiF} = 1$ during the iFuse device power up with R_{rst} and C_{rst} RC network.

S_m SCF may result in a short-circuit current flowing through the failed switch as well as other switches. Such event will trigger the gate-driver overcurrent protection of the healthy switches in the short-circuit current path. The FDC must be fast enough to assert S_m SCF before the triggering of the healthy switches overcurrent protection. Otherwise, once the overcurrent protection is engaged, current would be mitigated and the FDC would be unable to detect any fault.

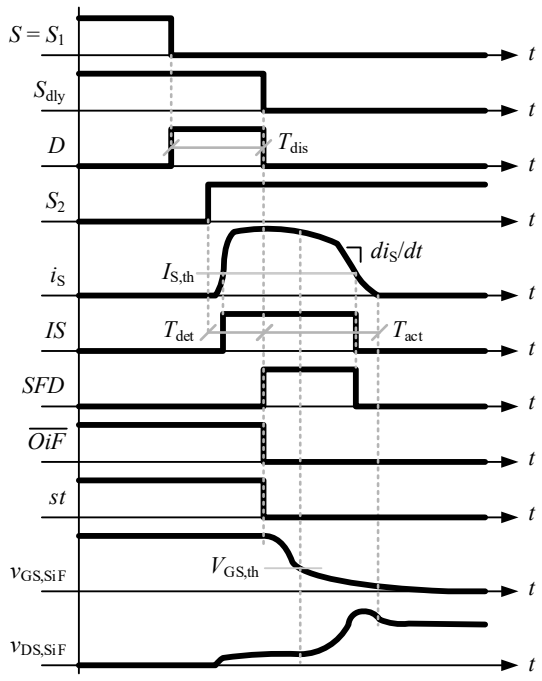


Fig. 5. Typical evolution of the main analog and digital signals from the iFuse circuitry during a shoot-through event due to a SCF of the switch associated to the iFuse, as in the circuit shown in Fig. 11(a). The event $i_s > I_{s,\text{th}}$ does not need to take place before any predefined time such as T_{dis}.

Moreover, the short-circuit current scenario also imposes that S_{iF} turn off must be performed taking into account two considerations. First, S_{iF} turn off must be quick enough to avoid damaging S_{iF} and other healthy switches located in the short-circuit current path. The maximum energy absorption capability of MOSFET and IGBT chips is around 4 to 5 J per cm^2 of die surface, resulting in a maximum permissible short-circuit event duration around 10 µs [8], [22]. However, on a second consideration, S_{iF} turn off must be slow enough to avoid high di_S/dt values that could cause voltage spikes in the parasitic inductances present in the short-circuit current path, damaging S_{iF} and other healthy devices due to overvoltage. For this reason, the turn off of S_{iF} is performed in two stages. In the first stage, S_{iF} gate is discharged until its gate-to-source voltage $v_{\text{GS,SiF}}$ reaches the threshold value $V_{\text{GS,th}}$. In this interval, S_{iF} remains ON since $v_{\text{GS,SiF}} > V_{\text{GS,th}}$ and S_{iF} gate discharge is performed quickly to account for the first consideration. In the second stage, $v_{\text{GS,SiF}}$ is discharged from $V_{\text{GS,th}}$ to zero volts. This is the interval where the true turn off takes place. To account for the second consideration, the gate discharge is performed slower than in the first stage. The abovementioned discharge process is accomplished through the network composed of $R_{\text{off-slow}}$, $R_{\text{off-fast}}$, and zener diode Z_1, with $R_{\text{off-slow}} >> R_{\text{off-fast}}$ and zener voltage $V_Z \approx V_{\text{GS,th}}$. This way, S_{iF} gate is initially discharged fast thanks to the low-impedance path offered by the series connection of $R_{\text{off-fast}}$ and Z_1 until $v_{\text{GS,SiF}} \approx V_Z$, when Z_1 turns off. Afterwards, S_{iF} gate is discharged slowly through $R_{\text{off-slow}}$, to ensure a low-di/dt turn-off transition.

The purpose of F_{latch} is to serve as a one-time latch. When S_{off} is turned on, V_{fuse} voltage supply is short-circuited through S_{off} and F_{latch}, effectively fusing F_{latch}. Once F_{latch} is fused, S_{iF} is guaranteed to remain OFF through pull-down resistor R_{pd1}, thus permanently blocking any forward current through S_m, regardless of any possible malfunction in the circuit due to the failure event. It is therefore only used to prevent a subsequent undesired turn-on of S_{iF} due to the loss of power or damage in the S_{iF} control circuitry. F_{latch} current rating can be quite small since the fuse does not have a current limiting function, which allows a low capacitance value for C_{fuse} in Fig. 4.

The steady-state drain-to-source voltage of S_{off} ($V_{\text{DS,Soff}}$) reflects the state of F_{latch} and hence, the health status of S_m. For convenience, the output health-status reporting binary variable st is defined from this voltage. The value of this variable is $st = 1$ when $V_{\text{DS,Soff}} = V_{\text{fuse}}$ (F_{latch} is unfused and S_m is in healthy condition) and it is $st = 0$ when $V_{\text{DS,Soff}} = 0$ V (F_{latch} is fused and S_m has failed). Variable st can be fed back to the power converter control such that the switching strategy and/or converter structure can be reconfigured after the failure, if necessary.

The advantage of the iFuse local control is that it is faster than a centralized control, as the iFuse does not need to establish a communication with such centralized control, and it enables a quick reaction to clear the short-circuit currents that

may occur after the short-circuit failure of the main switch. Still, a centralized control of the iFuse tripping is also possible, for redundancy or for other purposes, though the inclusion of an input signal to the iFuse circuitry to be able to externally command the tripping of the iFuse.

Referring to Fig. 5, the detection time T_{det} is the time the automatic-diagnosis circuit takes to identify S_m SCF, and the actuation time T_{act} is the time it takes for the driving circuit to turn off S_{iF}.

S_{iF} CBVU switch is not a standard switch, as it is not required to switch frequently. Its main requirements are:

- ON-state voltage drop should be as small as possible in order to minimize the increment of converter conduction losses incurred when adding the iFuse.
- It should be able to withstand short-circuit currents for a few µs.
- Drain-to-source breakdown voltage should match the associated switch S_m breakdown voltage.

A low conduction voltage drop generally implies high switching losses. However, S_{iF} switching losses can be neglected, since it will only turn on at zero current during the converter power up and it will turn off only once, when the fault of its associated switch is detected. Moreover, low-conduction-loss devices are also more robust under short-circuit currents since they feature a higher current rating than low-switching-loss devices for the same voltage rating and semiconductor technology.

III. Applications

The proposed iFuse device is meant to be employed in power converters where the forward current path of the short-circuit-failed switches must be cleared to prevent the short circuit of any voltage source involved in the converter operation. When these converters feature some sort of redundancy, such action allows continuing the operation.

In the following, some cases of interest are discussed.

A. Power Converters Employing Parallel Switches

As explained in Section I, power converters employing parallel switches allow easily demonstrating the impairment caused by a switch SCF on the converter inherent fault-tolerance capabilities. Fig. 6(a) presents the same leg topology and switch SCF scenario shown in Fig. 1(c) but also depicting the two leg switching states with their corresponding current paths after the switch S_{2a} SCF and the engagement of switch S_{2a} iFuse. Compared to the case employing eFuses (Fig. 1(b)), employing iFuses allows selectively isolating the switch failed in short circuit. Moreover, when the leg output terminal is connected to dc-link node 2 and $i_o < 0$, current will partially flow through the S_{2a} iFuse free-wheeling diode, allowing similar conduction-loss values to the pre-fault case.

B. ANPC Topologies

As explained in Section I, these topologies are more vulnerable to switch SCF than to switch OCF. As an example, Fig. 6(b)-(c) shows a three-level ANPC converter leg [10] where two switches have failed in short circuit: S_{p12} and S_{n22}. The same switching states employed in [10] to connect to the three dc-link points are assumed. In Fig. 6(b), without iFuses, a short circuit of a dc-link capacitor occurs when the leg is connected to dc-link nodes 1 and 3. Therefore, the leg is inoperative since only the connection to one of the dc-link nodes remains. In Fig. 6(c), with iFuses, the short circuit of a dc-link capacitor is avoided, and the connection of the output terminal to the three dc-link points is preserved, without the need to modify the switching states. This is a general interesting advantage of the introduction of the iFuse. Failures

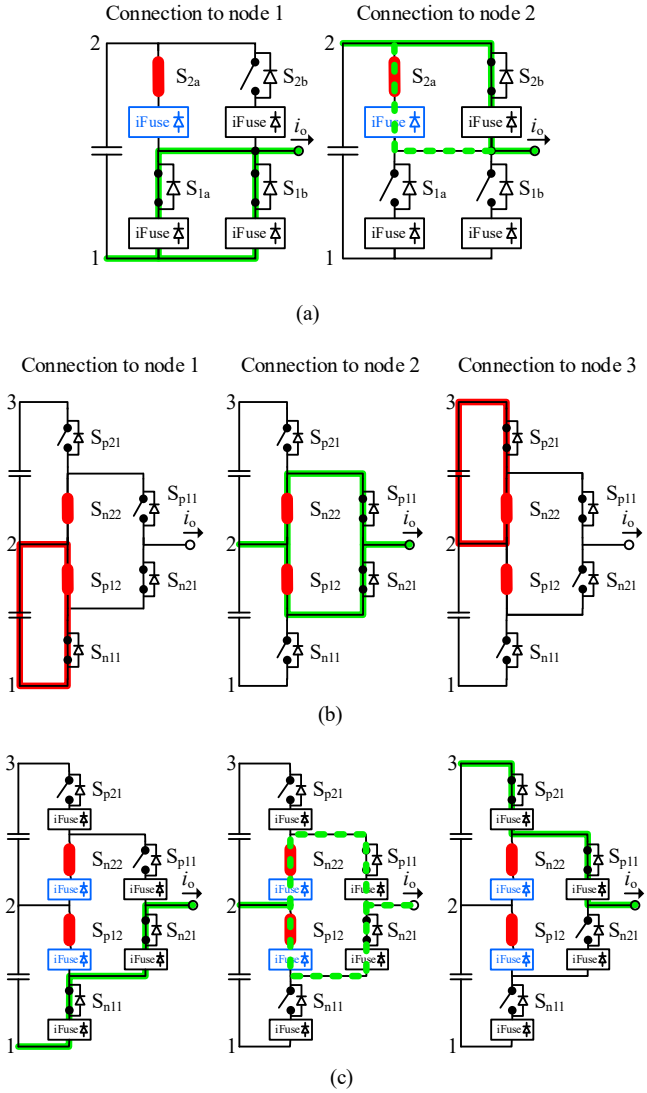


Fig. 6. Examples of converter legs where the iFuse device can be employed to take advantage of switch-level redundancy. Switches failed in short circuit and the short-circuit current paths are marked in red. The iFuses that have been engaged (OFF state) are marked in blue. Current paths for any polarity of i_o are marked in green solid lines. Current paths for only $i_o < 0$ or only $i_o > 0$ are marked in green dashed lines. (a) Two-level leg with two parallel switches per position. (b) Three-level ANPC leg without iFuses. (c) Three-level ANPC leg with iFuses.

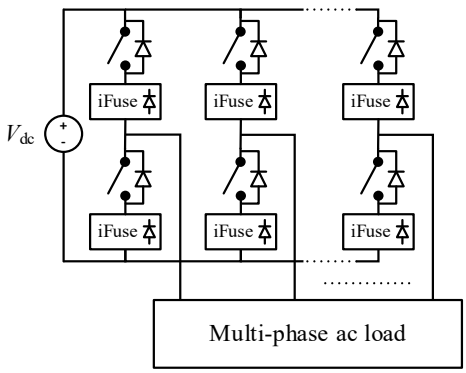


Fig. 7. Multiphase dc-ac converter that can continue operating after the failure of one or more legs, feeding, for instance, a multiphase motor with five or more phases.

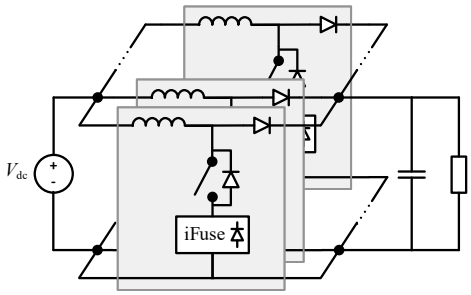


Fig. 8. Interleaved multiphase boost dc-dc converter.

under the iFuse protection do not need a change of the converter switching states. The converter can continue operating with the same switching states used before the failure. It is worth noting that connection to dc-link-point 2 is preserved thanks to the iFuse reverse-conduction feature.

C. Multiphase Dc-Ac Converters Featuring Leg Redundancy [2], [3], [7], [11]–[13]

This case is illustrated in Fig. 7. As explained in Section I, conventional solutions employ different strategies involving additional hardware (fast fuses, thyristors, capacitors, redundant series switches) and a centralized control to isolate the faulty leg. The proposed iFuse can replace these conventional solutions, allowing for a simpler implementation thanks to its standalone operation, and substantially improving the performance of the fault-tolerance mechanism, especially when substituting fault-isolation mechanisms employing fast fuses.

D. Interleaved Dc-Dc Converters

This last case corresponds to interleaved dc-dc converters, as for example two-level multiple-phase boost converters [3], [23], illustrated in Fig. 8. In such converters, a SCF of an active switch leads to the saturation of the inductor and eventually the short circuit of the input power supply. Employing an iFuse in series with each switch avoids this situation and allows reporting the failure to the converter closed-loop control, through signal *st*, such that proper action can be taken to continue the operation with the remaining phases.

E. Converters featuring 4Q switches

Combining two SCs (main switch + iFuse) in anti-series results in a 4Q SC with switch SCF protection; i.e., in case one of the two main switches in the 4Q SC fails in short circuit, its associated iFuse will open. Thus, after a switch SCF the 4Q SC will still maintain the bidirectional voltage-blocking capability, while thanks to the reverse current conduction path offered by the iFuse, the SC will allow current flow in one of the two directions. The proposed SC anti-series association would be useful in power converters employing 4Q switches, such as matrix converters and converters featuring t-type and π-type ANPC switching legs, among others.

IV. Reliability Improvement

A two-level converter leg with two switches in parallel per position (Fig. 6(a)) serves as a good and simple example to study and quantify the reliability improvement offered by the iFuse.

First, let us consider the converter leg in Fig. 6(a) but without iFuses. In this case, when any switch SCF occurs, the converter must be shut down. Instead, if a switch OCF occurs, the converter can still operate as long as there remains at least one switch per position. Moreover, it will be assumed that whenever the first OCF occurs, the leg output current is halved. This way, the failure rate of the switch in parallel with the failed switch does not increase above its nominal value.

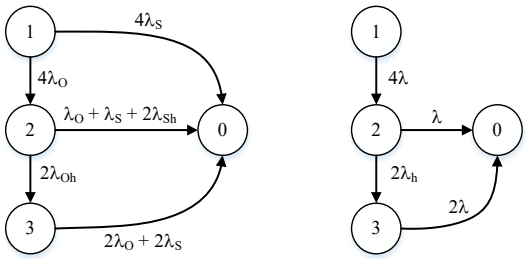
Next, let us consider the converter leg shown in Fig. 6(a) with the iFuses. Thanks to these iFuses, the converter can continue in operation regardless of the type of failure as long as there remains at least one operating switch per position. As in the previous case, it will be assumed that whenever the first switch failure occurs, the leg output current is halved.

The reliability of both cases can be easily evaluated deriving their Markov chain model and then computing the system mean-time to failure (MTTF), as presented in [24]. Fig. 9 shows the Markov chain model for both cases, where the states are defined in Table I. The transition rate between states is defined by the addition of the relevant main switch failure rates. λ_O is the switch OCF rate and λ_S is the switch SCF rate, both at the nominal switch current, with the total failure rate being $\lambda = \lambda_O + \lambda_S$. λ_{Oh} and λ_{Sh} are the corresponding failure rates at half the nominal switch current, with $\lambda_h = \lambda_{Oh} + \lambda_{Sh}$. For the sake of simplicity, it will be set that $\lambda_h = \lambda /2$. Let us also define $\alpha = \lambda_O / \lambda = \lambda_{Oh} / \lambda_h$ as the probability of OCF occurrence, while $1 - \alpha$ represents the probability of SCF occurrence.

Note that the Markov chain model of Fig. 9(b) assumes that the iFuse failure rate is much smaller than λ and λ_h, since the iFuse is permanently in the ON state with only conduction loss, zero switching loss, and no switching stress, as opposed to the main switch, where much more conduction loss, substantial switching loss, and substantial switching stress takes place. In addition, a robust design of the iFuse auxiliary circuitry is also

TABLE I
MARKOV CHAIN DIAGRAM STATES DEFINITION

State	Fig. 9(a)	Fig. 9(b)
1	All switches are healthy.	All switches are healthy.
2	One switch OCF has occurred.	One switch has failed.
3	Two switch OCFs, one in each leg position, have occurred.	Two switches, one from each leg position, have failed.
0	One switch SCF or two switch OCFs from the same leg position have occurred. The leg is shut down.	Two switches from the same leg position have failed. The leg is shut down.



(a) (b)

Fig. 9. Markov chain diagrams of a two-level converter leg with two switches in parallel per position. (a) Without employing the iFuse. (b) With one iFuse in series with each switch (Fig. 6(a)).

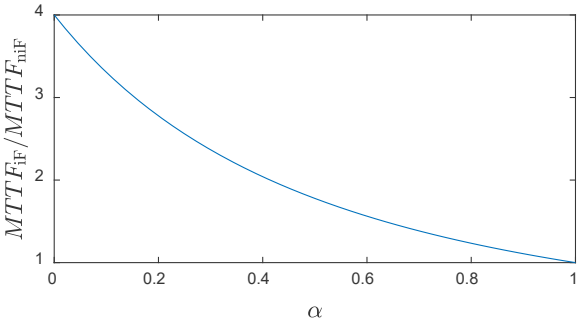


Fig. 10. Ratio of the MTTF of the converter leg in Fig. 6(a) to the MTTF of the same leg without employing iFuses.

assumed. Thus, under these assumptions, the iFuse failure rate can be neglected.

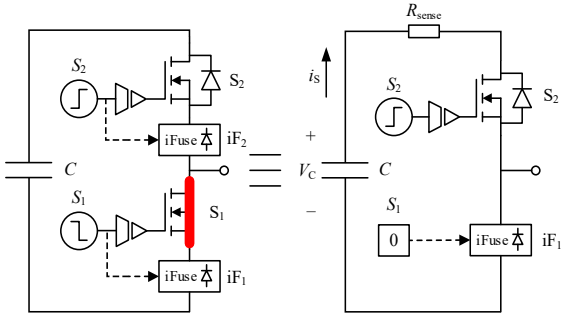
The resulting MTTF in both cases (without and with iFuses, respectively) is

$$MTTF_{niF} = \frac{1}{\lambda} \cdot \frac{\alpha^2 + 2\alpha + 1}{4}$$
$$MTTF_{iF} = \frac{1}{\lambda}. \quad (4)$$

The ratio between both is plotted in Fig. 10 as a function of α. As expected, when all failures are OCF ($\alpha = 1$), then both MTTF are equal. However, when the probability of SCF increases (α decreases), $MTTF_{niF}$ decreases. With an equal probability of switch OCF and SCF ($\alpha = 0.5$), the MTTF of the converter leg employing iFuses is 1.7 greater than the leg not employing iFuses. When all failures are SCF ($\alpha = 0$), the MTTF of the leg employing iFuses is 4 times greater.

TABLE II
EXPERIMENTAL TEST PARAMETER VALUES

Parameter	Value
$V_{C,init}$	50 V
C	440 µF (electrolytic cap.) + 13.2 µF (PET film cap.)
R_{sense}	2.5 mΩ ± 1%
$R_{off\text{-}fast}$	10 Ω
$R_{off\text{-}slow}$	330 Ω
V_{Z1}	5.1 V
V_{fuse}	15 V
$I_{S,th}$	200 A
$R_{DS,on}$ (S_2)	11.1 mΩ
$R_{DS,on}$ (S_{iF})	1.3 mΩ



(a) (b)

Fig. 11. First experimental test schematic. (a) Reproduced scenario. (b) Simplified circuit configuration used for the experimental test.

V. EXPERIMENTAL RESULTS

Experimental tests have been carried out to demonstrate the feasibility and effectiveness of the proposed solution. In the first test, a SCF is forced in the bottom switch S_1 of the two-level converter leg shown in Fig. 11(a). A shoot-through event will subsequently occur when the leg output transitions from the connection to the negative dc-link rail to the connection to the positive dc-link rail; i.e., when S_1 transitions from high to low and then S_2 transitions from low to high. At S_2 turn on, the dc-link capacitor will be short circuited and then iFuse iF_1 should turn off after a short time interval.

This scenario has been reproduced with the simplified circuit configuration of Fig. 11(b). In this circuit, both S_1 and iF_2 have been replaced by a short, since they behave as a low-ohmic contact. Signal S in iF_1 is set low. In the experiment, the dc-link capacitors, formed by a parallel connection of electrolytic and PET film capacitors, are first pre-charged to voltage $V_{S,init}$. Then, shortly after, S_2 is turned on. Resistor R_{sense} is employed to measure current i_S.

Switches S_2 and S_{iF} are implemented with MOSFETs IRFR4510 and IPT015N10N5, respectively, both rated at 100

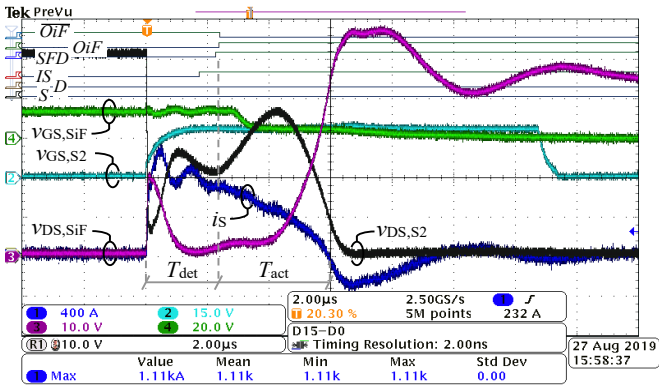


Fig. 12. Experimental results showing digital (top) and analog (channels 1 to 4 and R1) signals.

V. The device selection has been performed to emulate the typical characteristics of both devices: the main switch S_2 featuring a good switching performance with moderate conduction performance, while S_{iF} features an optimal conduction performance. Table II shows the main component parameter values of Fig. 11(b). As it can be seen, IPT015N10N5 $R_{DS,on}$ is very low. In fact, it was the commercial 100 V-rated Si MOSFET with the lowest ON-state channel resistance at the time of the experimental tests. With the abovementioned S_2 and S_{iF} MOSFET selection, a power converter incorporating an iFuse in series with each switch, would only experience a 12% increase in its conduction losses. Nonetheless, due to the novelty of the concept and the intended switch functionality, it is reasonable to expect some room for optimizing the design of switches to be used in iFuses and further reduce the conduction losses.

Fig. 12 shows the results of the described experimental test. As it can be observed, once S_2 gate-to-source voltage $v_{GS,S2}$ begins to rise, shoot-through current i_S rises abruptly, reaching a peak value of 1.1 kA. After 1.7 µs, digital signal *IS* goes high indicating that current $i_S > I_{S,th}$ (a certain delay is introduced by the detection circuit), followed by the activation of *SFD* and *OiF* signals. Once $\overline{OiF} = 0$, the S_{iF} turn-off procedure begins by discharging its gate in two stages, as can be observed in $v_{GS,SiF}$ and as explained in Section II. S_{iF} true turn off starts when $v_{GS,SiF}$ reaches $V_{GS,th}$ (around 4 V) with its drain-to-source voltage ($v_{DS,SiF}$) and current (i_S) presenting slopes of approximately 30 V/µs and –340 A/µs, respectively. Thanks to the moderate di_S/dt value, the peak value of $v_{DS,SiF}$ during the turn off process is limited to 57 V, corresponding to an overshoot of only 14%.

The time intervals for T_{det} and T_{act} are 2.4 µs and 3.6 µs, respectively. Therefore, the iFuse is capable of detecting the switch in SCF and blocking the forward current path of its associated switch in 6 µs. Time interval $T_{det} = 2.4$ µs is shorter than the typical response time of the overcurrent protection of the healthy-switches gate driver, which typically is between 8 to 10 µs. Therefore, the iFuse is able to engage successfully without the negative interference of the healthy-switch driver overcurrent protection.

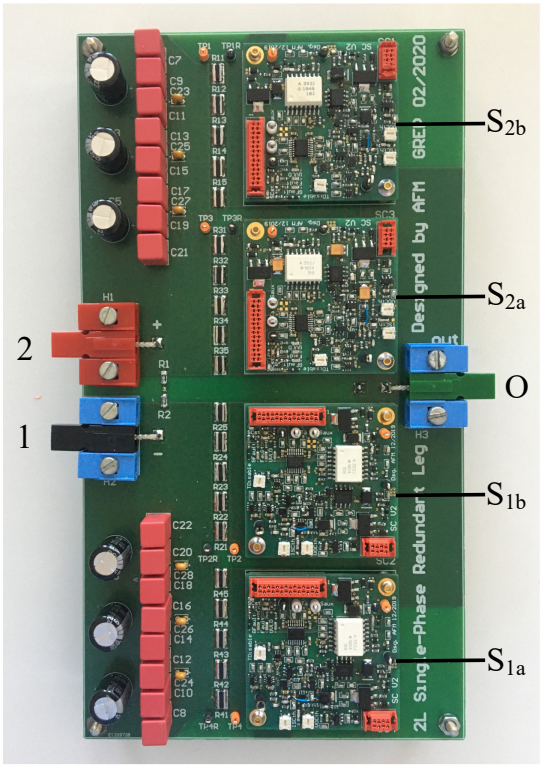


Fig. 13. Prototype of a two-level leg with two parallel switches per position according to Fig. 6(a). All switches are equipped

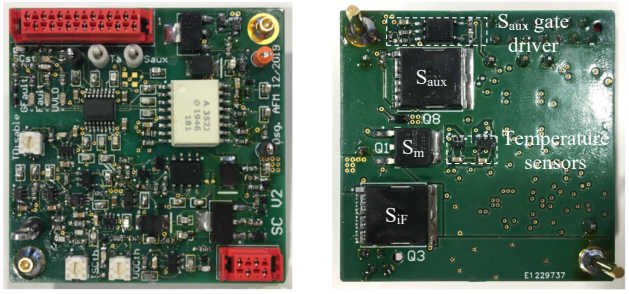


Fig. 14. Detail of the SC implementation. S_{aux} is an auxiliary switch in parallel with S_m used to emulate short-circuit faults of the main switch S_m.(a) Top. (b) Bottom.

During the shoot-through, S_2 drain-to-source voltage $v_{DS,S2}$ reaches an average value of approximately 25 V, indicating that the device is working in the saturation region. During this interval, S_2 junction temperature increases rapidly due to the high power loss, which in turn decreases the saturation current. This phenomenon is consistent with the findings in [22] and explains why i_S current starts decreasing before S_{iF} starts turning off.

The capacitor voltage (V_C) decreases 8 V after the shoot-through event, indicating that approximately 15 mJ have been dissipated in R_{sense}, S_2, S_{iF}, and the parasitic elements of the circuit. This energy value is far below the maximum short-circuit energy that S_2 and S_{iF} can withstand, which is around 750 mJ and 2.5 J, respectively, considering a die surface of

approximately 0.15 cm^2 for IRFR4510 and 0.5 cm^2 for IPT015N10N5.

Additional experimental tests have been performed in a two-level leg with two parallel switches per position according to Fig. 6(a) and feeding a series resistive-inductive load. Fig. 13 presents the leg prototype. Each main switch is paired with an iFuse, forming a SC. Fig. 14 shows a detail of the SC implementation. Note that the SC incorporates an auxiliary switch (S_{aux}) in parallel with the main switch, in order to be able to emulate short-circuit faults of the main switch in a controlled manner, by simply turning on S_{aux} at the desired point in time of the fault.

Fig. 15 presents the results under different fault scenarios. S_1 and S_2 are the switch control signals of the bottom and top switches, respectively. Voltage v_o is the leg output terminal voltage with respect to dc-link point 1 and current i_o is the leg output current. In Fig. 15(a) a short-circuit fault of switch S_{1a} is emulated during the conduction interval of S_{2a} and S_{2b}. The activation of the auxiliary switch to emulate the fault is commanded by signal S_{1a_SC}. The fault is emulated during the conduction interval of the complementary switches to produce the maximum distortion in the output leg voltage. Right after the fault, a shoot-through event brings the current of switch S_{1a} (i_{S1a}) above 1 kA, current that is also flowing through S_{2a} and S_{2b}. The iFuse in S_{1a} SC opens immediately, while all other iFuses are not triggered, and the leg can continue operating as normal, thanks to the availability of healthy redundant switch S_{1b}. Fig. 15(b) demonstrates the good performance of the redundant leg under the short-circuit fault of S_{2a} during the conduction interval of switches S_{1a} and S_{1b}. Finally, Fig. 15(c) demonstrates the good performance under again the short-circuit fault of S_{2a}, but now the fault takes place during the conduction interval of switches S_{2a} and S_{2b}, which is the most typical case. The fault does not cause a shoot-through event until the complementary switches S_{1a} and S_{2b} are turned on. Again, the fault is quickly cleared by the corresponding iFuse and the leg continues operating as normal.

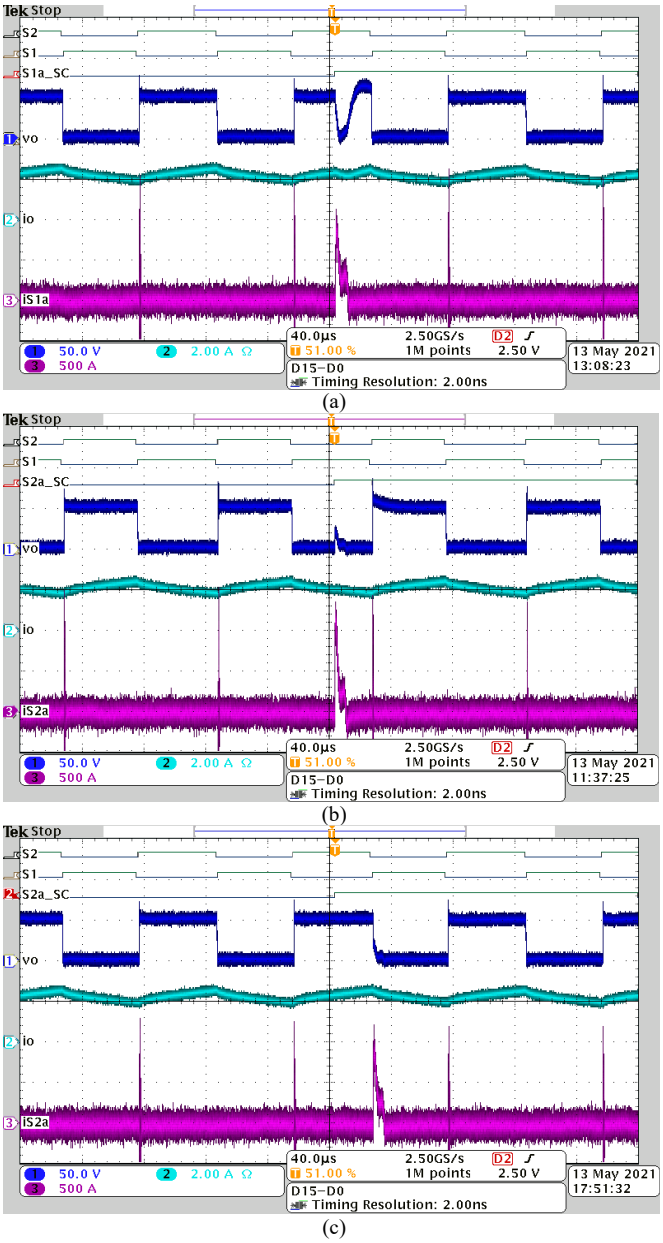


Fig. 15. Experimental results with the two-level leg of Fig. 13 fed by a 50 V dc power supply and feeding a series resistance-inductance load. (a) Short-circuit of S_{1a} occurring in the middle of the conduction interval of S_2. (b) Short-circuit of S_{2a} occurring in the middle of the conduction interval of S_1. (c) Short-circuit of S_{2a} occurring in the middle of the conduction interval of S_2.

VI. Conclusion

A novel protection device has been presented to improve the fault tolerance and reliability of power converters where switch SCFs are especially detrimental. Table III highlights the main differences of the proposed iFuse compared to alternative technologies. The iFuse transforms very quickly an original switch SCF into an OCF, and at the same time enables a free-wheeling current path through the failed device. The converter fault tolerance and reliability can be improved by connecting an iFuse in series with each CBVU switch, or at least with those more critical in terms of fault tolerance. A selective turn off of only the iFuse whose associated switch has failed in short circuit is then guaranteed, all performed in a standalone fashion. Since the switch-failure detection will be usually performed during a shoot-through event, special care has been taken in the design of the iFuse turn-off procedure so that it is fast enough to avoid the damage of healthy devices due to sustained overcurrent, and at the same time it does not incur in high di/dt that could damage healthy devices due to overvoltage. A signal reporting the health-status of the associated switch has been added. The iFuse does not require an additional power supply, because the power required for the iFuse operation is provided by recycling the turn-off losses of the associated converter switch. Therefore, the proposed design for the iFuse makes it suitable for its application in all types of converters and simplifies to a great extent the integration of the iFuse into a compact assembly, being a significant advantage in comparison to other existing solutions based on bulky fuses

and redundant converter branches. The health-status reporting functionality can be easily complemented with the OCF detection, by simply monitoring the associated switch voltage across the power terminals. Since the detection of the switch SCF is almost instantaneous, the iFuse will perform successfully regardless if the power converter is in steady-state or transient operation.

The iFuse enables in a simple manner substantial fault-tolerance and reliability improvements in converters with parallel power devices, employing multilevel neutral-point-clamped topologies, with redundant legs and/or with multiple phases. If incorporated in multiple power switches, the converter will be able to withstand multiple switch faults. As a matter of fact, in cases such as in a two-level switch-level-redundant leg equipped with iFuses (Fig. 6(a)), the number of tolerated switch SCFs is greater than in the case of two redundant legs featuring the same total number of power switches. This advantage is certainly obtained at the expense of increased conduction losses, stray inductance in the commutation loops, circuit space and complexity, and cost. However, an optimal design of S_{iF} producing very small conduction losses, the integration of S_m and S_{iF} into the same package, the integration of the auxiliary circuitry, together with the benefits of economies of scale under the scenario of a massive use of these SCs for multiple applications, could minimize these disadvantages to a level where the use of the iFuse is competitive. Moreover, an integrated design of the SC would free the converter manufacturer from the task of properly selecting the iFuse-components and a combined S_m-S_{iF} chipset could be made available to configure power modules with device paralleling.

Experimental results demonstrate that the designed circuit allows a fast detection and isolation of a short-circuit-failed switch, clearing short-circuit currents up to 1 kA without damaging healthy devices.

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TABLE III
COMPARISON OF ALTERNATIVE TECHNOLOGIES

Feature	Smart/Intelligent Switch	Solid-State Circuit Breakers and Electronic Fuses	Proposed iFuse
Function	Provides overcurrent and short-circuit protection in a given circuit branch through a power semiconductor device that also performs a permanent switching function. As soon as a branch overcurrent is detected, the protection is activated leaving open the forward conduction path of the branch.	Provides overcurrent and short-circuit protection in a given circuit branch through a dedicated power semiconductor device introduced to only perform this function. As soon as a branch overcurrent is detected, the protection is activated, leaving open the branch.	Provides selective protection leaving open the forward conduction path of an associated power switch which has failed. The protection is activated as soon as the short-circuit failure of the associated power switch is detected, even at low current values. If the associated main power switch has not failed, the protection is not activated, even in the presence of overcurrents and short circuits.
Selective isolation of faulty power switches in voltage-source power converters	No	No	Yes
Enables reverse current direction after tripping	Yes	No (typically)	Yes
Bipolar voltage blocking after tripping	No	Yes (typically)	No
Includes voltage clamping circuit	No	Yes	No
Self powered	No (typically)	No (typically)	Yes