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Dissertation

Tailored Electrical Characteristics in Multilayer Metal-oxide-based-memristive Devices

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Abstract

Multilayer metal-oxide-based-memristive devices are one of the most promising candidates for neuromorphic computing. However, specific applications of neuromorphic computing call for different requirements for memristive devices. Therefore, an open challenge in technological development is the tailored design of memristive devices for specific applications. In particular, multilayer stacks complicate fabrication processes due to a large number of device parameters such as staking sequences and thicknesses, quality, and property of each layer. Therefore, systematic investigations of the individual device parameters are particularly decisive. Moreover, they need to be combined with a profound understanding of the underlying physical processes to bridge the gap between material design and electrical characteristics of the resulting memristive devices.

To obtain memristive devices with different resistance switching characteristics, various sequences and combinations of three metal oxide layers (TiO_x, HfO_x, and AlO_x) are fabricated and studied. First, single-layer oxide devices are investigated to find desirable multilayer stacks for memristive devices. Second, TiO_x/HfO_x-based bilayer oxide devices are fabricated. Via systematic experiments and statistical analysis, it is shown that the stoichiometry, thickness, and device area influence operating voltages, non-linearity in resistive switching, and variability. Third, TiO_x/AlO_x/HfO_x-based devices are fabricated. By adding AlO_x into the bilayer oxide stacks, these trilayer devices present favorable electrical features for use in neuromorphic hardware, such as electroforming-free and compliance-free switching as well as long retention. The developed memristive devices are integrated into systems such as crossbar structures and one-transistor-one-memristor configurations. Here, suitability for efficient neuromorphic computing is assessed. Also, methods to tune the device resistance gradually in an analog fashion are demonstrated. This feature allows for efficient neuromorphic computation.

This comprehensive study highlights the relationship between device parameters and electrical properties of multilayer metal-oxide-based memristive devices. On this basis, tailoring methodologies are established for specific neuromorphic applications.

Kurzdarstellung

Auf Mehrlagen-Metalloxiden basierende memristive Bauelemente sind einer der vielversprechendsten Kandidaten für neuromorphes Computing. Allerdings stellen spezifische Anwendungen des neuromorphen Computings unterschiedliche Anforderungen an die memristiven Bauelemente. Eine ungelöste Herausforderung in der technologischen Entwicklung ist daher das maßgeschneiderte Design von memristiven Bauelementen für spezifische Anwendungen. Insbesondere die unterschiedlichen Materialien des Schichtstapels erschweren die Herstellungsprozesse aufgrund einer großen Anzahl von Parametern, wie z. B. der Stapelsequenzen und -dicken und der Qualität sowie der Eigenschaften der einzelnen Schichten. Daher sind systematische Untersuchungen der einzelnen Bauelementparameter besonders entscheidend. Darüber hinaus müssen sie mit einem tiefgreifenden Verständnis der zugrundeliegenden physikalischen Prozesse kombiniert werden, um die Lücke zwischen Materialdesign und elektrischen Eigenschaften der resultierenden memristiven Bauelemente zuschließen.

Um memristive Bauelemente mit unterschiedlichen resistiven Schalteigenschaften zu erhalten, werden verschiedene Abfolgen und Kombinationen von drei Metalloxidschichten (TiO_x, HfO_x und AlO_x) hergestellt und untersucht. Zunächst werden einschichtige Oxidbauelemente untersucht, um Kandidaten für mehrschichtige Stapel zu identifizieren. Zweitens werden zweischichtige TiO_x/HfO_x Oxidbauelemente hergestellt. Anhand von systematischen Experimenten und statistischen Analysen wird gezeigt, dass die Stöchiometrie, die Dicke, und die Fläche des Bauelements die Betriebsspannungen, die Nichtlinearität beim resistiven Schalten und die Variabilität beeinflussen. Drittens werden TiO_x/AlO_x/HfO_x-basierte Bauelemente hergestellt. Durch das Hinzufügen von AlO_x in die zweischichtigen Oxidstapel weisen diese dreischichtigen Bauelemente optimale elektrische Eigenschaften für den Einsatz in neuromorpher Hardware auf, wie z. B. elektroformierungsfreies und strombegrenzungsloses Schalten sowie eine lange Lebensdauer. Die entwickelten memristiven Bauelemente werden in Systeme, wie Kreuzpunkt-Strukturen und Ein-Transistor-ein-Memristor-Konfigurationen integriert. Hier wird die Eignung für effizientes neuromorphes Computing bewertet. Außerdem werden Methoden zur stufenlosen analogen Einstellung des Widerstands der Bauelemente demonstriert. Diese Eigenschaft ermöglicht effiziente neuromorphe Rechenschemata.

Diese umfassende Studie beleuchtet die Beziehung zwischen den Bauelementparametern und den elektrischen Eigenschaften von mehrschichtigen memristiven Bauelementen auf Metalloxidbasis. Auf dieser Grundlage werden maßgeschneiderte Methoden für spezifische neuromorphe Anwendungen entwickelt.

초록

금속산화물 다층 구조로 이루어진 멤리스터 소자는 뉴로모픽 컴퓨팅의 가장 유망한 후보로 꼽히고 있다. 그러나 뉴로모픽 컴퓨팅이 적용되는 응용 분야는 다양하며, 각 분야에 따라 멤리스터 소자 성능에 대한 요구사항이 달라진다. 따라서 특정 응용 분야에 따른 멤리스터 소자의 맞춤형 설계가 필요하다. 특히, 다층 구조에서는 각 박막의 적층 순서, 두께, 품질 및물성과 같은 많은 매개변수를 고려해야 하므로, 공정 과정이 복잡해진다. 그러므로 각 매개 변수에 관한 체계적인 연구가 특히 중요하다. 또한, 멤리스터 소자에 사용되는 재료와 소자의 전기적 특성을 연관 짓기 위해서는 소자 작동의 물리적 원리에 대한 깊은 이해가 연구에 포함되어야 한다.

다양한 전기적 특성을 보인 멤리스터 소자를 제작하기 위해 3종류의 금속 산화물층 (TiOx, HfOx, AlOx)이 다양한 순서로 적층하고 결합한다. 첫째, 단일 층 산화물 소자를 제작 및 분석하여 멤리스터 소자에 적합한 다층 구조를 찾아낸다. 둘째, TiOx/HfOx 기반 이중 층 산화물소자를 연구한다. 체계적인 실험설계와 통계적 분석을 통해 박막의 물성, 두께 및 소자 면적이 어떻게 작동 전압, 저항 변화의 비선형성 및 성능 가변성에 영향을 미치는지 연구한다. 셋째, AlOx 박막을 이중 층 산화물 구조에 추가함으로써 TiOx/AlOx/HfOx 기반 삼중 층 구조소자가 제작되고 연구된다. 이러한 삼중 층 소자는 별도의 전자 형성과 전류 제한 회로를 더는 필요로 하지 않으며 향상된 기억 능력을 보인다. 이러한 특성은 뉴로모픽 컴퓨팅을 위한 부품소자로써 사용하기에 적합한 전기적 기능을 제공한다. 개발된 멤리스터 소자는 크로스바 구조 및 1-트랜지스터-1-멤리스터 구성과 같은 시스템에 집적된다. 제작된 시스템에서 효율적인 뉴로모픽 컴퓨팅 가능성 대한 멤리스터 소자의 적합성이 평가된다. 또한, 아날로그 방식으로 소자의 저항을 점진적으로 조정하는 방법을 시연한다. 이 기능은 효율적인 뉴로모픽 컴퓨팅을 가능하게 한다.

이 포괄적인 연구는 금속산화물 다층 구조 기반 멤리스터 소자의 소자 적 매개변수와 전기적 특성 간의 관계를 밝혀낸다. 이를 기반으로 특정 뉴로모픽 응용 분야에 대한 맞춤 설계 방법 론을 제공한다.

Publication

- S. Park, B. Spetzler, T. Ivanov, and M. Ziegler, "Multilayer redox-based HfO_x/Al2O3/TiO2 memristive structures for neuromorphic computing", Sci Rep 12, 18266 (2022)
- <u>S. Park</u>, S. Klett, T. Ivanov, A. Knauer, J. Doell, and M. Ziegler, "Engineering Method for Tailoring Electrical Characteristics in TiN/TiOx/HfOx/Au Bi-Layer Oxide Memristive Devices", Frontiers in Nanotechgnology 3 (2021)

Conference

- <u>S. Park</u>, C. Ziebold, S. Klett, T. Ivanov, and M. Ziegler, "Statistical Evaluation of Tailored Memristive Characteristics in TiOx-HfOx Bilayer System", 4th International Conference Emerging Materials, Technologies and Applications for Non-volatile Memory Devices, CIMTEC, June (2022), talk (presented by C. Ziebold)
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- <u>S. Park</u>, T. Ivanov, S. Klett, A. Knauer, J. Doell, and M. Ziegler, "Tailored electrical characteristics in TiOx/HfOx-based memristive device for targeting neurmomorphic computing", Thin Film, 2021 SKM21-DPG Spring Meeting, Virtual, Sep (2021), talk
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1 Introduction

Artificial intelligence is becoming an integral part of our everyday lives. For computers to learn and evolve to simulate human intelligence, however, it requires handling a tremendous amount of data. In this respect, conventional CMOS technologies and conventional computing architectures exhibit inefficiency resulting in immense energy consumption. As an alternative, neuromorphic computing has been spotlighted in recent years [SPP+17], in particular, with the development of memristive devices [Iel18]. Neuromorphic computing aims at emulating key features of the human brain, where data are stored and processed in the same place simultaneously with high energy efficiency and parallelism. This concept can be realized with memristive devices. Figures 1.1(a) and (b) illustrate an analogy of their physical system. Memristive devices have at least two resistance states. The two states are switchable from a low resistance state to a high resistance state and vice versa, once a sufficiently strong electric field is applied. This electrical characteristic of memristive devices is referred to as resistive switching (RS) which is illustrated in Figure 1.1(c). In addition, their simple two-terminal device architectures allow the realization of massive memristive networks similar to neuro-biological architecture.

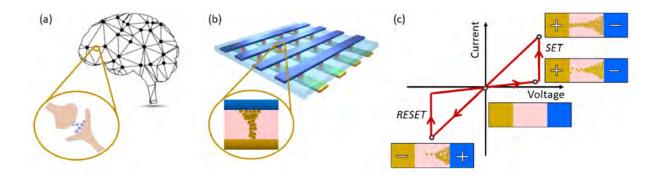


Figure 1.1: (a) A schematic of human brains. Neural cells are connected with high parallelism. (b) Artificial neural network based on memristive devices. They have simple two-terminal architectures. (c) RS behavior in memristive devices. By applied electric fields, the resistance states are switched from a low resistance state to a high resistance state and vice versa. (Figure (a)-(c) taken from [Cal29])

Among various types of memristive devices, redox-based RS devices consisting of multilayer metal oxide systems gained considerable interest due to their outstanding performance such as high endurance, fast speed, low power consumption, long data retention, as well as compatibility with the complementary metal-oxide-semiconductor technology [LLF+18]. Moreover, the integration of such memristive devices in crossbar structures has proved their suitability for neuromorphic hardware in terms of density, speed, and energy efficiency, whereby efficient machine learning algorithms were implemented [LA21, KJT+19, YWG+20]. For this, the mem-

ristive devices must satisfy the two steps of machine learning algorithms: [AMD11]: training and inference algorithms. In the training phase, data are fed into a mathematical model, and the algorithm modifies the parameters of the training model. This process continues over many cycles until the training model gives the desired outputs. After that, the training model can be used to produce practical results, which is the inference phase. In the inference algorithm, the well-trained model can create predictions. Depending on the algorithms assigned on memristive networks, different requirements for memristive devices are prioritized [TAN+18, SWW+21]. Therefore, a common challenge in the development of memristive devices is a tailored design of memristive devices for respective applications. For technological developments of multilayer metal-oxide-based-memristive devices, however, many device parameters must be taken into account. The device parameters include material properties of active layers and interface layers and geometrical parameters such as layer stacking sequences, thicknesses of each layer, device area, and so on. Apart from that, the physical fundamentals of functional layers in stacking structures are not well understood due to the complex coupling of chemical and physical processes [HCH⁺14]. To obtain insight into the impact of those device parameters on the RS characteristics in memristive devices, systematic investigations of the individual parameters are particularly decisive. Moreover, suitable manufacturing technologies combined with a profound understanding of the underlying physical processes can help bridge the gap between material design and RS characteristics in memristive devices.

The aim of this thesis is to find methodologies to tailor RS characteristics in metal-oxide-based-memristive devices toward specific applications for neuromorphic computing. This thesis includes seven chapters as follows.

The succeeding chapter (ch.2) introduces theoretical backgrounds, split into three parts.; Firstly, the fundamentals of redox-based memristive devices are explained, including the phenomenological description of RS characteristics of memristive devices and RS mechanisms. Secondly, the fundamentals of neuromorphic computing are described. Here, architectures of neural networks and requirements for memristive devices as neuromorphic hardware are introduced. The third part explains the analysis methods that are used to investigate RS characteristics in the following chapters.

In the next chapter (ch.3), the experimental methods to manufacture the investigated devices in this thesis are detailed as well as the methods to characterize those devices.

In the following, ch.4 starts by reporting the current status of the development of metal oxide materials for memristive devices. After that, the technological development processes of three metal oxide films (TiO_x , HfO_x , and AlO_x) are presented. Varying sequences and combinations of the three metal oxide layers, memristive devices with different RS characteristics are fabricated. They are demonstrated from ch.5 to ch.7.

Ch.5 consists of three parts in which RS characteristics of fabricated memristive devices are presented and discussed. In the first part, major considerations when selecting oxide layers and interface layers are discussed. For this, the electrical characteristics of single-layer metal-oxide-based memristive devices are investigated. Based on the investigation, TiO_x/HfO_x bilayer systems are designed, whose RS characteristics are presented in the second part of ch.5. Here, a systematic investigation of the relationship between device parameters and RS characteristics is conducted. Those device parameters include the stoichiometry and thickness of HfO_x and device area. As a result of the investigation, pathways to optimize the properties of the TiO_x/HfO_x-based memristive devices are discussed in respect of specific neuromorphic applications. To improve the performance of the TiO_x/HfO_x-based memristive device, an AlO_x layer is inserted in the memristive layer stack. The resulting RS characteristics of the TiO_x/AlO_x/HfO_x-based

memristive devices are presented in the last part of ch.5. The RS characteristics are investigated in terms of the requirement of current compliance and operating voltage range. For a precise adjustment of the RS characteristics, the stoichiometry of the HfO_x layer is further modified in the trilayer oxide stack. The impact of the device parameters such as oxide properties and the layer sequence on the RS characteristics are studied using a numerical simulation. A physics-based device model is developed for the simulation to deepen the understanding of the RS mechanisms. It encompasses essential interfacial interaction in the trilayer oxide systems that can be applied for tailoring the RS characteristics further.

In the next chapter (ch.6), the developed single memristive devices are integrated into crossbar structures and one-transistor-one-memristor systems for neuromorphic computing. Here, several concerns regarding final applications of the systems such as sneak-path problems, device reliability, or compatible electronic properties with connecting devices are thoroughly investigated.

Finally, ch.7 demonstrates methods to tailor non-linearity in RS which is an essential feature for efficient neuromorphic computing. The chapter is split into two parts. The first part presents tailoring methods by designing physical device structures with appropriate materials and the sequence of the oxide materials. Finally, the last part shows tailoring methods by controlling supply voltage signals on memristive devices. Moreover, a method to analyze the non-linearity in RS via machine learning is demonstrated.

2 Theoretical Background

Neuromorphic computing has been under the spotlight for energy-efficient memory-centric applications such as real-time visual information processing and natural language processing [MMQG20, Fur16, SPP+17, SKS+21]. As a candidate for neuromorphic hardware, memristive devices have been studied intensively [IA19b, BSS+17]. They are characterized by reversible resistive switching (RS) characteristics and simple architectures, which allow for memory and resistance plasticity with high scalability. This chapter provides the fundamentals of the RS characteristics and their application in neuromorphic computing, divided into three sections. Firstly, RS characteristics of memristive devices and the physical mechanisms are introduced. The RS characteristics enable emulating cognitive computing of human brains when memristive devices comprise highly connected networks, so-called artificial neural networks. Architectures of the neural networks and the required device performances for neuromorphic computing are summarized in the second part of the chapter. Lastly, analysis methods are described that are used to investigate RS characteristics of memristive devices in the following chapters.

2.1 Resistive Switching

Memristive devices comprise a switching layer sandwiched in between conducting electrodes as shown in Figure 1.1(b). Memristive devices feature RS behaviors which refer to reversible electrical resistance changes of devices by applied electric fields. RS can be caused by structural phase changes of the switching layers or by internal redox reactions that denote a coupled reduction and oxidation reaction in the switching layers [Was12]. In this thesis, the latter, i.e., redox-based memristive devices are focused on. This section introduces the basic terminologies and the general features of the RS operations. Additionally, materials used for redox-based memristive devices and the physical mechanisms of the RS are presented.

2.1.1 Resistive Switching Characteristics

RS behaviors of memristive devices can be observed in Current-Voltage (I-V) characteristics via DC voltage sweep measurements. In the measurements, voltage is swept following a triangular waveform as shown in Figure 2.1(a). A typical I-V characteristic of redox-based memristive devices is plotted in Figure 2.1(b). The memristive device shows initially high resistance. When a larger voltage than a V_{EF} is applied, the resistance changes to a lower resistance termed a low resistance state (LRS), or ON-state. The transition from the pristine high resistance to the LRS is referred to as an electroforming (EF) process, and the V_{EF} as the EF voltage. In the EF process, a full electrical breakdown of the memristive device is prevented by imposing current

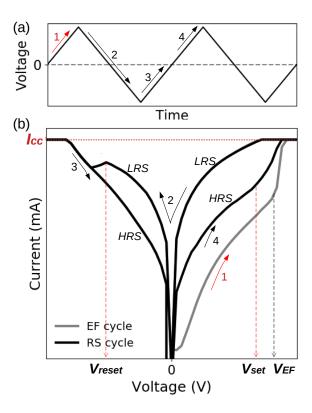


Figure 2.1: (a) A sequence of voltage sweeps in a triangular waveform. (b) A typical I-V characteristic of redox-based memristive devices. EF cycle and RS cycle in the plot denote voltage sweep cycles where an electroforming process and a stable RS operation are observed, respectively.

compliance, I_{cc} , through the memristive device. When the sweep voltage is decreasing, the resistance of the device is retained in the LRS, until a large negative voltage, V_{reset} , is applied. The V_{reset} is strong enough to cause the change in the resistance state of the memristive device from the LRS to a high resistance state (HRS), or OFF-state. This process is called a RESET process, and the V_{reset} is the RESET voltage. With increasing sweep voltages, the HRS is retained. The resistance in the HRS is most likely lower than the pristine resistance of the device, which is observed in the consecutive sweep cycle. The HRS is switched to the LRS when a strong electric field is applied to the device. This process is called a SET process, and the voltage is defined as the SET voltage, V_{set} . The V_{set} is smaller than the V_{EF} . Additionally, the resistance ratio of HRS (R_{HRS}) to LRS (R_{LRS}) is defined as a switching window, i.e., R_{HRS}/R_{LRS} , which is also called an on/off ratio.

As seen in the example in Figure 2.1(b), RS behaviors are commonly observed in a form of pinched I-V loops. Additionally, the switching voltages are opposite polarities, i.e. a positive V_{SET} and a negative V_{RESET} . It is defined as a bipolar RS. However, for some memristive devices, RS behaviors are unipolar in which the switching voltages are the same polarity. These distinctive RS types result from different working mechanisms that are affected by the material systems in memristive devices.

2.1.2 Resistive Switching Mechanisms

RS in redox-based memristive devices can be categorized into three types by details of the working mechanisms: valence change memory effect, thermochemical memory effect, and electrochemical metallization memory effect [Was12]. However, the three types of RS have in common that charged ions in the switching layers migrate driven by an applied electric field, resulting in ionic partial current. The charged ions can stem from oxygen anions or metal cations. The ionic currents lead to redox processes. These electrochemical reactions result in the resistance change in the memristive devices. The details in the processes of ion migrations and redox reactions depend on the material systems that consist of memristive devices. In this section, the three types of RS mechanisms and material systems that are often used for each RS type are listed.

Valence Change Memory Effect

valence Change Memory (VCM)-type RS are often observed in Transition Metal Oxide (TMO)s such as Ti and Hf [CLW+17, WDSS09]. VCM effects are based on the migration of oxygen-related ions in the oxide layers. Here, the oxygen-related ions are described as oxygen anions or oxygen vacancies which are the corresponding vacancies [Was12, CLC+16]. The migration of such ions leads to changes of valence state of the transition metal cations, which results in a considerable change in the electrical resistance of the devices [LI15]. The ion transport properties and the redox reaction rate depend on used material's properties such as oxygen concentration and crystal structure [MS09, CRS12, MGHEDS21]. Moreover, TMOs have a wide variety of oxidation states, and a wide range of stable phases exists [GPHS07]. These characteristics of TMOs enable causing distinctive RS characteristics. For example, the VCM-based devices can be split into two variants: interface-type and filamentary-type. The interface-type RS is caused by a homogeneous and uniform change across the entire active area. On the other hand, the filamentary-type RS is based on a single and a strong conductive filament (CF) that grows from one electrode to the counter electrode.

Interface-type RS is often observed in TMOs with a few oxygen vacancies and asymmetric work functions of electrodes [RK20, JKR+21, WLX+20]. In the devices, at least one electrode (SE) forms a high Schottky barrier. For the SE, metals with high work functions with low oxygen affinities such as Pt, Au, and TiN can be used. When a positive voltage is applied to the SE, oxygen anions migrate toward the SE across the switching layer, as shown in Figure 2.2(a). Here, the migration of the ions occurs homogeneously over the entire device area. When the ions are close to the SE/switching-layer interface, the Schottky barrier height is reduced due to the increased number of negatively charged oxygen ions [PKI+21]. It results in a SET process in the device. When a negative voltage is applied to the SE, the ions drift away from the SE, which causes a RESET process. As shown in Figure 2.2(e), in most cases, the interface-type devices feature gradual RS and current rectification in the I-V curves [YYS+16, Saw08, RK20]. The interface-type devices show good uniformity (low variance) in the RS and scaling effect of resistance due to the homogeneously distributed current across the device area. However, they often suffer from poor retention which is the time until the device resistance remains constant [SDH+17, Saw08].

Filamentary-type devices typically consist of a switching layer and asymmetric electrodes with significantly different work functions and oxygen affinities [YSM+11, MAJK+16]. One of the electrodes has a high oxygen affinity such as Al, and Ti, which is referred to as an ohmic

electrode (OE) in the following. The counter electrode (CE) has a high work function as well as a low oxygen affinity such as Pt, Ir, and TiN, which builds a high potential barrier at the switching layer/CE interface. The RS is mostly observed after an EF process [RHM+20] during which oxygen vacancies are generated in the switching layers. A schematic of the RS operation is shown in Figure 2.2(b). When a positive voltage is applied to the OE, oxygen vacancies drift towards the CE due to their positive charges. Here, the mobile oxygen vacancies are doublepositive charged (V_O^{++}) . When they are close to each other, the V_O^{++} s are reduced to single charged oxygen vacancies (V_Q^+) , forming a localized CF in the direction of CE (see Figure 2.2(b)) [KYN⁺13]. The CF results in a significant decrease of the barrier height at the switching layer/CE interface, turning the device into an LRS (SET process). Moreover, since the CF consists of V_O^+ that has a significantly higher energy barrier for diffusion than V_O^{++} , long retention time is observed in the filamentary-type devices [DMKN16]. During a RESET process (see Figure 2.2(b)), a negative voltage attracts the oxygen vacancies toward the OE. Therefore, the CF partly ruptures, which switches the device back to the HRS. In the I-V curves, as shown in Figure 2.2(f), the filamentary-type devices typically present abrupt switching and symmetry in the RS operations compared to the interface-type devices. They are also characterized by resistance independent of device areas due to the localized CF structures [FCW+10]. However, the randomness of the formation and rupture of the CF structures causes intrinsic variability in filamentary-type devices [BSS⁺17].

Thermochemical Memory Effect

Thermochemical Memory (TCM) effects are based on ionic transport and redox reaction facilitated dominantly by a temperature gradient (than by an applied electric field). A schematic of the RS mechanisms is shown in Figure 2.2(c). In TCM devices, a CF consisting of oxygen vacancies is formed during an EF process, which turns the device into an LRS. When a voltage is applied to the device and the corresponding current is sufficiently high, Joule heating is induced with an increase in temperature in the CF. The CF ruptures, resulting in an HRS in the device (*RESET process*). A subsequent SET process is similar to the EF process, although the required voltage for the SET process is typically lower than that for the EF process [Was12]. A typical I-V relation of TCM devices is shown in Figure 2.2(g). The SET voltage is lower than the EF voltage since the CF is not completely dissolved but only ruptured during the RESET process. In the RESET process, the corresponding current at the RESET voltage is larger than the SET current. The high current induces Joule heating and temperature increase, which results in the RS operations that are barely influenced by the polarity of applied voltages. TCM effects are observed in all metal oxides which show a large difference between the HRS and the LRS, such as ZrO_x, TiO_x, Al₂O₃, and SiO₂[Was12].

Electrochemical Metallization Memory Effect

Electrochemical metallization memory (ECM) effects are observed in memristive devices in which electrochemically active electrodes (AE) provide mobile metallic cations into the switching layers, while the counter electrodes (CE) are electrochemically inert. The ECM process is illustrated in Figure 2.2(d). The consecutive steps of the ECM are as follow: for a SET process,

positive voltages are applied to the AE, and the metallic cations are discharged. The cations drift driven by the electric field toward the CE. On the surface of the CE, the cations are electrochemically reduced and form a highly CF. The CF grows in the direction of the CE until electrical contact is established, which drops the voltage immediately. By applying the opposite polarity of voltages, electrochemical dissolution of the CF takes place. The rupture of the CF switches the resistance state back to the HRS. A representative I-V curve is shown in Figure 2.2(h). The ECM devices show bipolar RS due to the charged metallic cations. They show a high switching window (on/off ratio) and fast and abrupt switching [VWJK11]. Because of those characteristics, they have been intensely developed for selector applications as volatile memory hardware [WCL+21].

The AE can be made of Ag or Cu, and the CE can be Pt, Ir, Au, or W. For the switching layers, ionic conductive materials are recommended that can facilitate the migration of metallic cations. The examples are Au_2S , Cu_2S that contains a host cation, or insulators such as SiO_2 , WO_3 that are doped with cations of AEs.

2.2 Neuromorphic Computing

Neuromorphic computing aims at computing as human brains with high energy efficiency and parallelism. It mimics the neural network architecture, where data is processed and stored in the same place simultaneously and travels from one neuron to other neurons through a highly parallel network. As hardware for neuromorphic computing, memristive devices have attracted a lot of attention [IA19a]. Memristive devices have shown the capability to emulate synaptic functionalities of human brains [HWW+20]. For instance, during the learning process, biological synapses change the strength of the synaptic connections [CFB+16]. Similarly, the gradual change in conductance of memristive devices can mimic the learning process of biological synapses. Moreover, the simple two-terminal structures allow for realizing highly parallel networks.

In this section, neural network architectures are first introduced. In the following, the performance requirements of memristive devices for applications for neuromorphic computing are described.

2.2.1 Neural Networks

Human brains contain about 100 billion neurons, and each neuron is connected to up to 10,000 other neurons. The signals travel from neuron to neuron through synapses that are approximated as many as 1,000 trillion [Zha19, Chu16]. Neuromorphic computing systems mimic the structure of human brains. The most known structure is Artificial Neural Network. There are several models, but the Deep Neural Network (DNN) is the most widely used [JC17]. DNN consists of several layers in which there are a collection of artificial neurons, as shown in Figure 2.3(a). Input enters into the neurons in the *input layer*, and the output is sent out of the neurons in the *output layer*. Computing is conducted in the intermediate layers called *hidden layers*. In the DNN, each neuron is connected to all neurons in the previous layer via synapses. Each synapse has different strengths of the connection called synaptic weight. Increasing synaptic weight indicates that the synapse transmission is strengthened persistently, called long-term

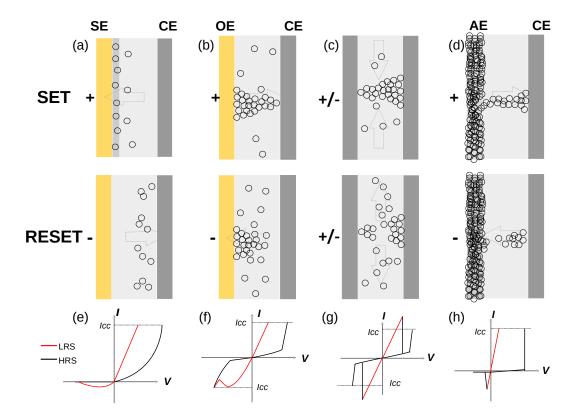


Figure 2.2: (a)-(d) Schematics of RS mechanisms for SET processes (upper) and RESET processes (lower) in memristive devices. Memristive devices consist of two electrodes and one switching layer. In the switching layers, the respective ion species for each type of RS are depicted using circle markers. (e)-(h) RS operations in DC voltage sweep measurements. (a) Interface-type devices in the VCM mechanisms. At the SE/switching-layer interface, a high potential barrier is built. Upper: when positive voltages are applied to the SE, the barrier height is reduced, resulting in an LRS. Lower: when negative voltages are applied to the SE, oxygen ions drift toward the CE, switching the device to an HRS. (e) Gradual changes in device resistnace and current rectifying features are observed. The RS operation is controlled by current compliance (I_{cc}). (b) Filamentary-type devices in the VCM mechanisms. Upper: when positive voltages are applied to the OE, oxygen vacancies drift toward the CE, forming a CF through the switching layer. The device switches to an LRS. Lower: when negative voltages are applied to the OE, the CF ruptures, which results in an HRS. (f) An abrupt switching and symmetry in RS operations are observed. (c) TCM-type devices. Regardless of the polarity of applied voltages, RS operations are observed. The RS is caused by forming (upper)/rupturing (lower) of a CF due to a thermal gradient induced by Joule heating. (g) Unipolar RS operation is observed. The current at the RESET process (LRS \rightarrow HRS in the plot) is significantly higher than the SET current (which is limited by I_{cc}). (d) ECM-type devices. Upper: when positive voltages are applied to the AE, metallic cations are discharged and migrate toward the CF. A CF is formed, which results in an LRS. Lower: when negative voltages are applied to the AE, cations migrate back to AE, rupturing the CF. It results in an HRS. (h) A large switching window (on/off ratio) and abrupt switching are observed.

potentiation, while synapse transmission that is continuously weakened by decreasing synaptic weight is called long-term depression. Computing in the DNN is based on parallel matrix-vector multiplication algorithms [ILC+19], as shown in Figure 2.3(b). The data sent out of previous neurons is weighted by the corresponding synaptic weights and summed up. The weighted sum is classified by an activation function.[MNAB+21]. This algorithm continues until the data reach the output layer, modulating the change of synaptic weight in the neural network [KAJ+18]. Many researchers realized the DNN via crossbar arrays consisting of memristive devices [HWW+20, WJS+18]. In the crossbar arrays, two electrode lines are perpendicularly arranged in rows and columns as shown in Figure 2.4. At each cross point, memristive devices are located, and they serve as synapses. The synaptic weights are stored in the conductance of the devices. When voltage signals enter memristive devices, the signals (inputs) are weighted by multiplying the stored synaptic weights (conductance). The results are the induced currents. The induced currents are summed up in each column, as the following equation:

$$I_j = \sum_{k=1}^m W_{jk} \cdot V_k \tag{2.1}$$

, where the m is the number of electrode lines in the rows, the j is the number of corresponding electrode lines in the columns (i.e., j = 1, 2, ..., n), and the n is the number of electrode lines in the columns. The summed currents (I_j) are processed by using activation functions to be sent to the neurons in the succeeding layers. This process takes place in parallel in all memristive devices in the crossbar array.

2.2.2 Requirements for Neuromorphic Hardware

For neuromorphic computing with high energy efficiency and high throughput, memristive devices should have i) compatibility with Complementary metal-oxide-semiconductor (CMOS), ii) large memory capacity, iii) analog resistive switching, iv) reliability (retention, endurance, variability), and v) low power consumption [IA19a, CSS+19, JT15, IKJ20]. In the following, those requirements of memristive devices are described, comparing the current status of memristive device technologies.

Compatibility with CMOS

The operating voltages should be compatible with scaled CMOS, which ranges from a few hundred millivolts (> 100 mV) to a few volts. Also, the materials should be compatible with CMOS fabrication. Among CMOS compatible materials, HfO₂ has shown promising results as a memristive material. For example, HfO₂-based memristive devices with an operating voltage of < 2V [LCC⁺09, SBK⁺14, BCS⁺16], HfO₂/TiO_x-based devices with < 1V [CMB⁺19], and HfO₂/WO₃-based devices with a switching voltage of 4 V [KTO⁺19] have been demonstrated.

Memory Capacity and Analog Resistive Switching

Memory capacity is the amount of memory that can be used which is commonly expressed in bytes. State-of-the-art computing such as the DNNs needs large memory capacities to store

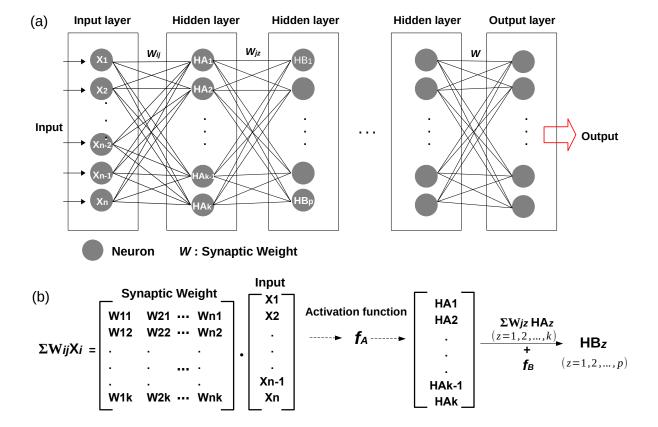


Figure 2.3: (a) A schematic of the DNN architectures. The DNN consists of an input layer, more than one hidden layers, and one output layer. Each layer has neurons. Each neuron is connected to all neurons in the previous layer via synapses. The synapses have different synaptic weights (W). (b) An example of computation algorithms in neurons. Inputs (X_i) are weighted by synaptic weights (W_{ij}) and summed up (*vector-matrix multiplication*). The weighted sums are further processed by activation functions (f_A) . The results are sent to the neurons (HAj) in the first hidden layer (i = 1, 2, ..., n, and <math>j = 1, 2, ..., k). This computing algorithm continues until the final output is obtained.

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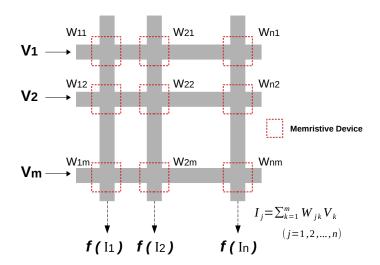


Figure 2.4: An illustration of realization of the DNN via crossbar arrays. Two electrode lines are perpendicularly arranged. At each cross point, memristive devices are located. Conductances of the devices serve as synaptic weights. When voltage signals (V) enter memristive devices, the voltage signals induce the corresponding currents (I) according to the conductance values (W) of the devices. The currents are summed up in each column and further processed by activation functions (f). The outputs are sent to the neurons (memristive devices) in the succeeding layer (crossbar array).

weight information. The average memory requirement is 16 GB [Sab01]. It means a total of around 10^{11} weights (conductance states) are required. To achieve high memory capacity, large switching windows (on/off ratio) and analog switching features can be considered. Here, analog switching features are related to multiple conductance levels. And, each level can be used as a storage. HfO_x-base memristive devices [HSZ⁺17] and multilayer metal oxide systems such as TiO_x/AlO_x [SKT⁺17] and HfO₂/ TiO_x [CMB⁺19]-based memristive devices have demonstrated analog switching with more than ten conductance levels.

Retention

Retention is defined as the time until data is stored in the memory device. It is a critical performance parameter of nonvolatile memory. If memory devices have short retention time, the data should be programmed repeatedly. Thus, retention is linked to power consumption. A typical requirement for non-volatile memories is 10 years at 85°C [JT15]. Among memristive devices, the comparable retention time of >108 s (over 10 years) has been reported in filamentary-type devices based on HfO₂-based [CGC+13, JHL+16] and TaO₂-based devices [HHY+15]. Retention time for interface-type devices is typically shorter than filamentary-type devices [SDH+17]. A long retention time reported for interface-type memristive devices is > 10^4 s (over several months) in the HfO_x/SiO₂-base [HCZ+16], TaO_x/TiO₂-based [CHH+15], and Hf_{0.8}Si_{0.2}O₂/Al₂O₃/Hf_{0.5}Si_{0.5}O₂-based devices [JKR+21].

Endurance

Endurance is how many cycles memory devices can operate switch-on and -off. The higher endurance memristive devices have, the more frequently the devices can be operated for programming. At least endurance cycles of 10^3 are required [JT15], and, for efficient training, endurance cycles of 10^6 are desired [ILC+19]. To compete with the DRAM (Dynamic Random Access Memory) or the SRAM (Static Random Access Memory), an endurance of 10^{12} is needed. Satisfactory endurance has been reported in TiO_2 -based [YTNS07], TiO_x/HfO_x -based [LCW+08], and HfO_2 -based [JHL+16] memristive devices that showed endurance cycles of 10^6 , 10^6 , and 10^{11} , respectively.

Variability

Variability is defined as the deviation of the main chosen performance parameters. For instance, in memristive devices, conductance states in the LRS/HRS or switching voltages are performance parameters. Variability can be divided into two categories: i) device-to-device variability which is a deviation from different devices, and ii) cycle-to-cycle variability which is a deviation at every switching cycle in one device. For efficient programming and high performance, variability is an important factor [CAA $^+$ 20, KNK $^+$ 20]. Many researchers have improved variability (uniformity) in RS of memristive devices by using multilayer metal-oxide systems such as HfO $_x$ /TiO $_x$ [JHD16, YDZ $^+$ 16], Al/HfO $_z$ [YGD $^+$ 09], and Ta/HfO $_z$ [KPK $^+$ 18].

Low Power Consumption

Power consumption is the amount of energy that memory devices require for their operation. To be comparable to the DRAM, a memory device should consume a few nanowatts. Low power consumption (a few tens of nW) of memrsitive devices has been reported in multilayer metal oxide systems such as TiO₂/TiO_x [XMDZ17], HfO_x/TaO_y/HfO_x [SBN⁺20], and Hf_{0.8}Si_{0.2}O₂/Al₂O₃/Hf_{0.5}Si_{0.5}O₂ layer stacks [JKR⁺21].

Self-rectifying Behaviors

Highly dense crossbar arrays suffer from unintentional currents flowing through the neighboring devices, the so-called sneak path current [BK19, SZT⁺20]. It results in errors in the programming/reading of device states and unnecessary power consumption. To tackle the sneak path problems, memristive devices that show current rectification, the so-called self-rectifying feature, can be used. It is a highly nonlinear and asymmetric I-V behavior, which enables to distinguish between a chosen device and unchosen devices in crossbar arrays.

Prioritized Requirements for Applications

A priority in the device parameters depends on the assigned task in neuromorphic computing such as training and inference algorithms [TAN+18, SWW+21]. In the training algorithms, data are fed into a mathematical model, and the algorithm modifies the weights of the training model. Here, the weights are stored in conductance states in memristive networks. This training algorithm continues over many cycles during which the conductance states in memristive networks are tuned to have the right weight matrices [KSJ18]. For the training algorithms, analog behaviors of memristive devices allow for efficient computing. This is because linear adjustment of conductance is possible by modulating programming pulses proportionally [JC22]. Apart from that, the higher the endurance is, the more training cycles. Therefore, for the training algorithms, analog switching and high endurance are important, whereas retention is less significant [CSS+19, TAN+18, SWW+21]. In the inference algorithms, the well-trained models can create predictions based on the weights obtained after the training algorithms. Those weights are stored in memristive networks [CDL+19]. Therefore, long retention and high energy efficiency are critical parameters for memristive devices, whereas analog switching and endurance are less important[TAN+18, SWW+21].

2.3 Analysis Methods for RS Characterization

This section first introduces statistical measures used to analyze RS characteristics in memristive devices. Statistical analysis allows formalizing representative RS characteristics of a great number of memristive devices. Secondly, machine learning algorithms are introduced as an analysis method. In the algorithms, mathematical models are used to train the impact of variables of interest on RS behaviors. Based on the well-trained model, a prediction is made, which can be used to adjust RS characteristics. Using the mathematical methods described in the last part of this section, machine learning analysis to predict RS operations is demonstrated in ch.7.2.

2.3.1 Statistical Measures

In the following, statistical measures that were used in this thesis are described: mean, median, quartile, standard deviation, probability density function, cumulative distribution function.

Boxplots

Boxplots used in this thesis display distributions of datasets using six statistics: minimum, first quartile (Q_1) , mean, median, third quartile (Q_3) , and maximum. Figure 2.5(a) shows an example of the boxplots. The median is the middle value in a dataset which is marked with a line in red color inside the box. The mean is the arithmetic average, which is the sum of the values divided by the number of values. The mean value is marked with a circle marker on the boxplot. In the example, the mean value cannot represent the center value of the data (median), which indicates skewed distribution. Quartile divides the values in the dataset into four parts. The Q_1 cuts off the lowest 25 % of the data, and the second quartile (Q_2) cuts the data in half (50 %), which is the median of the data. The Q_3 splits off 75 % data point from the smallest value. On the

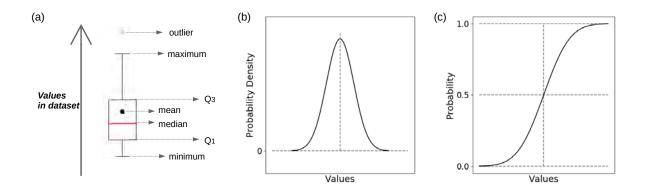


Figure 2.5: (a) Distribution in a boxplot. (b) Normally distributed data in a PDF curve. (c) Normally distributed data in a CDF curve.

boxplot (see Figure 2.5(a)), the bottom and the upper edges of the box indicate the Q_1 and the Q_3 , respectively. The area inside the box represents the range between Q_1 and Q_3 , which is called the interquartile range (IQR). The IQR shows the spread of the values. In addition to the box on the boxplot, there are lines, the so-called whiskers, extending from the box. The bottom and the upper whiskers indicate the minimum and the maximum of the dataset, which are Q_1 - 1.5·IQR (lowest 49.65%) and Q_3 + 1.5·IQR (99.65%), respectively. Thus, the data points outside the boundary of the whiskers, so-called outliers, are the remaining 0.7% of the values in the dataset.

Aside from the IQR, the standard deviation (σ) is another method to measure spread of dataset. The σ is calculated using the following equation:

$$\sigma = \sqrt{\frac{1}{N} \sum_{i=1}^{N} (X - \mu)^2}$$
 (2.2)

, where the X, the N, and the μ are individual values in the dataset, the number of values, and the mean in the dataset. The larger the σ is, the wider spread of X. However, the larger the μ is, the larger the σ . Thus, it is difficult to compare how much two datasets are spread out using σ alone if the two datasets have several orders of difference in the μ values. For this case, relative standard deviation (RSD), also known as the coefficient of variation (CV), can be useful. The RSD is calculated as the ratio of σ to μ (σ/μ). It allows for a relative comparison of the two datasets. However, the RSD is sensitive when the examined datasets contain outliers. In that case, the quartile coefficient of dispersion (QCD) is an alternative method. The QCD is computed as the following equation:

$$QCD = \frac{Q_3 - Q_1}{Q_3 + Q_1} \tag{2.3}$$

Probability Distribution Function

The probability density function (PDF) is used to specify how likely a random value falls in a particular range of values in a dataset. The PDF can be interpreted as the continuous version of

the histogram. On the x-axis, values of interest are shown, and the y-axis presents the density of the values, as shown in Figure 2.5(b). The peak value represents the median of the dataset. The width of the PDF curve indicates the spread of the dataset. When the distribution of values in datasets shows a bell-shaped curve with symmetry about the peak, it is said that the dataset is normally distributed. The general form of normal distributions is as the following equation:

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} \exp[-\frac{1}{2}(\frac{x-\mu}{\sigma})^2]$$
 (2.4)

, where the μ is the expectation of the distribution (which can be the mean or the median), and the σ is its standard deviation.

The cumulative distribution function (CDF) is obtained by integrating the PDF. The CDF is the probability that a random value will take a certain value. In the CDF plots, values of interest are shown on the x-axis, and the probability from zero to one is on the y-axis. In the CDF curves, normally distributed datasets are visualized in an S-shaped form as shown in Figure 2.5(c). The probability is between 0 to 1. The value at the probability of 0.5 represents the median of the dataset. The steeper rise the S-shaped form is, the smaller the spread of the dataset.

2.3.2 Mathematical Functions used in Machine Learning Algorithms

In the following, mathematical functions that are used in the machine learning algorithm in ch.7.2 are introduced. As described above (see ch.2.2.1), weighted inputs are summed and processed through activation functions in neurons. Afterward, this processed information is sent to neurons in the succeeding layers. As an activation function, the rectified linear activation function (ReLU) is the most commonly used [Dan23]. The ReLU function can be written as follows:

$$f(x) = \max(0, x) \tag{2.5}$$

As shown in the equation, the function returns the input value back directly, if the input is positive. Otherwise, the function will output zero. Its rectifying feature and linear behavior allow for a fast learning and efficient training [Bro03].

The linear activation function returns the input back as the following equation:

$$f(x) = x \tag{2.6}$$

The function does not do anything, which is used in the output layer [Tiw18].

The adaptive Moment Estimation (Adam) is an optimization algorithm that tunes weights and learning rates. It minimizes the loss function which is the difference between predicted values and actual values. The Adam is based on the stochastic gradient descent that can be expressed as the following equation:

$$w_{updated} = w - \eta \nabla Q(w) \tag{2.7}$$

, where the w, the η , and the Q are randomly chosen a set of values from the dataset, the learning rate, and the loss function, respectively. The Adam offers fast computation time. Furthermore, it requires low memory and less tuning than any other optimization algorithm [Gup07].

Loss functions are used to calculate the difference between the predicted values obtained by

trained models, and the actual values used in training. Outputs of loss functions, the so-called *loss*, are a measure to evaluate how well the trained models perform. A large value for the *loss* indicates the poor performance of the trained models. Among loss functions, mean squared error (mse) is the simplest and the most commonly used [Sei21]. The mse is calculated as the following equation:

$$mse = \frac{1}{N} \sum_{i=1}^{N} (y_i - \hat{y}_i)^2$$
 (2.8)

, where the N, the y_i , and the \hat{y}_i are the number of values in the dataset, actual values, and predicted values. In the mse, outlier predictions are detected easily, since the function outputs the square of the difference between y_i and \hat{y}_i .

In the DNN, overfit models are trained algorithms that perform well on training datasets but not on values that are not used in training. To prevent overfitting, the Dropout function can be used that randomly drops out neurons during training. It has advantages in that it is a simple and compatible method with many types of training procedures [GBC16].

3 Experimental Methods

This chapter describes the fabrication processes of memristive devices that are investigated in this thesis. Also, the characterization methods to study materials properties and electrical properties of memristive devices are detailed.

3.1 Device Fabrication

A basic structure of memristive devices in this thesis is seen in Figure 3.1(a). A relevant layer stack (memristive layer) of the devices is marked in the figure. It comprises a resistive switching layer sandwiched between two metal electrodes. The switching layer is either a single or multilayer of metal oxides in this thesis. The surface of single devices is passivated by a SiO₂ layer. The two electrodes of the memristive devices are connected to *contact pad* layer for electrical measurements. A standardized procedure is used to build memristive devices in this thesis, which includes i) deposition of the memristive layer, ii) etch of the unnecessary parts, iii) passivation of single devices, and iv) deposition of contact metal films. The process i) is important, because memristive layers strongly affect the electrical properties of memristive devices. The structure of devices is determined by photomask designs used in the process ii) - iv). In the following, the used mask layouts are presented, and the four fabrication processes are described in detail.

3.1.1 Mask Layout

5-inch photomasks consist of soda-lime glass and chrome (Compugraphics GmbH, Jena, Germany). Light can pass through only the glass part of the masks. Two sets of mask layouts used in this thesis are shown in Figure 3.1(b) and (c).

To develop material systems for memristive devices, a set of mask layouts was used designed by Hansen [Han17] as shown in Figure 3.1(b). It contains six different device areas, allowing for studying the resistance-area relation in RS operations of memristive devices. The set is a basic design unit cell, which is arranged repeatedly over a 4-inch wafer. Therefore, a total of around 40,000 devices can be fabricated at one process run on a wafer, which allowed for investigating the statistical RS operation of memristive devices.

The second set of mask layouts is designed to investigate memristive devices interconnected in a form of crossbar arrays. In Figure 3.1(c), a basic design unit cell is shown. The basic unit cell is arranged repeatedly over a 4-inch wafer. Therefore, a total of around 200 crossbar arrays are fabricated at one process run. More details of the crossbar arrays are described in ch.6.1.

Both sets comprise four different mask layouts. A region where the four masks are overlapped is marked with dashed lines in Figure 3.1(b) and (c) accordingly. The difference between the two

sets is the arrangement of the patterns for electrodes. In the first set (see Figure 3.1(b)), memristive devices have independent electrodes, ensuring that a supply voltage is applied to only one single device. In the other set (see Figure 3.1(c)) electrodes are shared with neighboring cells. Except for the arrangement for the electrodes, both sets of mask layouts result in the same architecture of memristive devices at a single device level. The four individual mask designs are presented in Figure 3.1(e-h) along with the resulting structures of the layers. Figure 3.1(d) shows a memristive layer without any structures after the process i). Figure 3.1(e) and (f) show the memristive layer structured by using the first and the second mask layouts, respectively. The former and the latter determine bottom electrodes and device areas, respectively, which corresponds to the process ii). Figure 3.1(g) presents a structured passivation layer by using the third mask layout. It represents the process iii). Figure 3.1(h) shows structured contact pads by using the fourth mask layout, which corresponds to the process iv).

3.1.2 Deposition of Memristive Layers

In this thesis, deposition of memristive layers was conducted via a cluster system (CS 400 ES; Von Ardenne, Dresden, Germany). The cluster system consists of three process chambers: one e-beam evaporator and two DC magnetron sputter chambers. Substrates can be moved from one to other process chambers through a transfer chamber in the cluster system. Among the deposition processes, DC magnetron sputter is used (PC 5 chamber) to deposit memristive layers that are presented in this thesis. In the process chamber, three source targets (Ti, Al, Hf) are coaxially equipped on the top (see Figure 4.3(a)). The substrate holder is situated on the bottom, and it can be rotated or lifted up and down. The distance between the target materials to the substrate holder is 55 cm. A gas mixture of inert gas of Ar and reactive gas of O₂ is injected into the chamber during sputtering. The ratio of a gas mixture is written in detail in ch.4. Working pressure of 5e-3 mbar and dc power of 200 W are kept constant for all memristive layers. During deposition processes, the chamber pressure is regulated through a feedback loop involving a butterfly valve and two pressure gauges. There are shutters in front of the source targets and the substrate holder with which the duration of the deposition is controlled.

3.1.3 Etch of Memristive Layers

After deposition of memristive layers, structuring of memristive devices is realized by lithography processes followed by etching processes.

Photolithography

The process begins with a preparation step. In this step, a clean Si/SiO₂ substrate is baked at 95 °C for the desorption of water molecules on the surface. Afterward, vaporized HMDS (Hexamethyldisilazane) is applied to the substrate to enhance the adhesion between a photoresist and the substrate. After the substrate preparation, a photoresist is spin-coated on the substrate. The used photoresists are AZ 1518 (MicroChemicals GmbH, Ulm, Germany) and AZ nLOF 2020 (MicroChemicals GmbH) which are referred to as positive PR and negative PR, respectively,

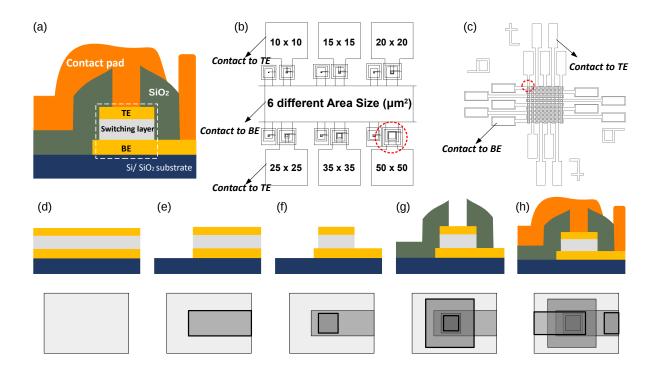


Figure 3.1: (a) A representative structure of memristive devices. On a Si/SiO₂ substrate, a memristive layer including a bottom electrode (BE), a switching layer, and a top electrode (TE) is shown. The surface of the memristive layer is passivated by a SiO₂ layer. Contact pads are connected to the two electrodes for electrical measurements. (b) A set of mask layouts for investigating single memristive devices with six different device areas. It consists of four different mask layouts. A region where the four masks are overlapped is marked with a dashed line. (c) A set of mask layouts for investigating memristive devices in crossbar arrays. It consists of four different mask layouts. A region where the four masks are overlapped is marked with a dashed line. (d-h) The cross-sections of the deposited layers. The layers are structured by using the mask layouts shown below accordingly. Among the four processes in the standardized fabrication procedure, (d) shows the deposited layers in the process i). (e) and (f) present the structured layers after the process ii). In this step, the structure of BE and device areas are determined. (g) presents the structured SiO₂ layer after the process iii). (h) shows the final architecture of memristive devices after the process iv).

in the following. The rate of the spin-coating is 4,000 rpm, which forms a 2 μ m photoresist. The substrate covered with the photoresist is baked at 100 °C for 1 min for the positive PR, or at 120 °C for 1 min for the negative PR. Afterward, the photolithography processes are conducted using a UV-lithography process (Mask Aligner MA8e; SÜSS MicroTec SE, Garching, Germany) at a wavelength of 365 nm (i-line). A photomask and the substrate are brought into contact in the mask aligner, in which the photomask is placed between the substrate and the light source. The substrate is moved to be aligned to the photomask. They are pressed close together in a vacuum mode. The substrate is exposed to a UV light through the photomask. The light reaches the photoresist only through the glass part of the photomask, which causes a chemical reaction in the region. The dose of the light is $186 \,\mathrm{mJ/m^2}$ for the positive PR or $120 \,\mathrm{mJ/m^2}$ for the negative PR. After the exposure step, the positive PR is immersed in a developer solution for 35 s which is a dilution of AZ developer (MicroChemicals GmbH): $H_2O = 1$: 1. The photoresist exposed to the light is removed by the developer solution. For the negative PR, the substrate is baked at 120 °C for 1 min after the exposure step, then dipped into a developer solution (AZ 726 MIF; MicroChemicals GmbH) for 50 s. The unexposed region of the negative photoresist is removed.

Device Structuring Methods

The structuring is done via etching processes or lift-off processes in this thesis. Etching is a subtractive process. The deposited layer in the region that is not protected by photomasks is eroded by etching processes. As opposed to it, liftoff is an additive process. The deposited layers in the region that is not protected by photomasks remain.

The used etching process can be divided into two categories: wet etching and plasma etching. Wet etching is used for Au layers (dilution of Au etchant: $H_2O = 1$: 5, rate: 30 nm/min), and SiO₂ layer (Buffered oxide etch, 5-6 s for 120 nm). For wet etching, the positive PR is used for photomasks. Before the wet etching, baking the substrate can help to enhance the adhesion between the photomask and the deposited layer underneath. Additionally, O2 plasma treatment is necessary for small features (< 10 nm), which removes residuals of the photoresist on the surface of the substrate. Plasma etching (Inductively Coupled Plasma Reactive-ion Etching) was used for TiN layers and metal oxide layers (PlasmaPro 100 Cobra ICP RIE Etch; Oxford Instruments, Abingdon, United Kingdom). The etching is conducted at 20 °C with ICP power of 500 W and RF power of 15 W. The working pressure and the etching gases were varied depending on the etched materials. For TiN and TiO₂ films, working pressure of 15 mTorr and CF₄ gas flow of 40 sccm are used. The etching rates are 18 nm/min and 25 nm/min for TiN and TiO₂ films, respectively. For HfO₂ layers, working pressure of 4 mTorr and a gas mixture of CF₄: Ar = 40: 15 are used. The etching rate of HfO₂ films is 10 nm/min. Using the same etching condition, however, the TiO2 and the SiO2 layers are also etched. Therefore, it is required to set an etching duration carefully. A passivation SiO₂ layer is etched using plasma etching (PlasmaPro 100 RIE; Oxford Instrument), in case an Al layer is placed under a SiO₂ layer. The etching rate is 35 nm/min when using a gas mixture of CHF₃: Ar = 12: 38 at working pressure of 30 mTorr and working power of 200W. After the plasma etching processes, the best way to remove the photoresist is to immerse the substrate in Aceton solution for 30 min at room temperature, followed by O₂ plasma treatment.

In the liftoff processes, negative PR is used in this thesis. Firstly, photomasks are prepared on the substrate. Afterward, materials are deposited. The photoresist is lifted off using a DMSO-

based stripper (TechniStrip Micro D350; MicroChemicals GmbH) with 10 % cyclopentanone at 80 °C overnight. However, the Al layers can be damaged by the DMSO-based stripper, especially when the Al layers are in contact with Au layers. In that case, a photoresist-stripper P53 (MicroChemicals GmbH) is recommended to be used at 50 °C for 1 h. The P53 solution is based on a gentle physical detaching of the photoresist, which minimizes the chemical corrosion in Al layers.

3.1.4 Passivation Layers and Contact Pads

Structured memristive devices are passivated with a SiO_2 layer as shown in Figure 3.1(a). At first, a SiO_2 layer was deposited using an Inductively Coupled Plasma Enhanced Chemical Vapour Deposition (ICP-PECVD) system (Plasmalab 100; Oxford, Abingdon, United Kingdom) all over the substrate. ICP power of 500 W, working pressure of 8 mTorr, and a gas mixture of SiH_4 : $N_2O = 9$ sccm : 20 sccm are used. The deposition is conducted at $100\,^{\circ}C$ with a rate of 18 nm/min. A photolithography process is conducted on the surface of the SiO_2 layer. Afterward, the deposited SiO_2 layer is etched, which results in contact windows (see Figure 3.1(g)). Finally, an Al contact layer is deposited using an e-beam evaporator, and a liftoff processe is conducted for structuring as seen in Figure 3.1(h). The details of the etching/liftoff processes are described above.

3.2 Device Characterization

Characterization is performed in terms of material properties of memristive layers and electronic properties of memristive devices. Studying material properties helps to understand the electrical characteristics of memristive devices.

3.2.1 Material Characterization

Spectroscopic ellipsometry (SE) is used to determine refractive indices and thicknesses of metal oxide layers in this thesis. Two SE tools are used: SE500 (Sentech GmbH, Berlin, Germany), and SenResearch 4.0 (Sentech GmbH, Berlin, Germany). Both conduct multi-angle measurements. Spectral ranges used are 623.8 nm and 380 nm - 850 nm for the former and the latter setups, respectively. The former is conducted by manually changing the angles of the incident light, while the latter is by automatically changing the angles. Because of the automatic control system, the latter is used to investigate the uniformity of deposited layers over a 4-inch wafer, which requires repetitive measurements at many different positions.

Using the two ellipsometers, the change in polarization of a light beam upon reflection from the surface of examined samples is measured. Afterward, refractive indices and thickness are calculated using ellipsometry software (Sentech GmbH, Berlin, Germany). In particular, the latter tool (SenResearch 4.0) allowed for studying multilayer systems. Thus, it is used to investigate thin Al layers (< 5 nm) in which interfacial layers considerably influence the measurement results. Along with the SE measurements, a surface profilometer (Dektak 150; Veeco, Plainview (NY), USA) is used to confirm the thickness of layers in which a stylus with a radius of $12.5 \,\mu m$,

a force of 10 mg, and a resolution of 0.033 μ m/sample are used.

X-ray photoelectron spectroscopy (XPS) is used to determine the quantitative chemical composition of metal oxide layers in this thesis. In the XPS setup (SPECS Surface Nano Analysis GmbH, Berlin, Germany), monochromatic $AlK - \alpha$ radiation (excitation energy $h\nu = 1,486.68$ eV) is used. A SPECS SAGE HR 150 XPS system is equipped with a 1D delay-line detector and a Phoibos 150 analyzer for charge neutralization. The calibration of the energy scale is ensured by reference measurements on a polycrystalline silver sample. The analyzed area size is a diameter of 1 mm.

X-ray diffraction (XRD) analysis (Bruker D8 Discover; Bruker Corporation, Billerica (MA), USA) is used to determine the structural properties of metal oxide layers in this thesis. The used XRD system consists of a copper $K\alpha$ radiation source and a Lynxeye XE-T detector (energy resolution: < 380 eV at 8 KeV). The measured data is filtered to remove $K\alpha$ -contributions and the collected data is corrected by subtracting background noise.

Atomic force microscopy (AFM) (AIST-NT Combiscope1000; AIST-NT, Novato (CA), USA) is used to investigate the roughness and the morphologies of metal oxide layers. The tip (PPPNC-HR probe; nanosensors, Neuchaetel, Switzerland) has a radius of curvature < 10nm and resonance frequency of 330 kHz. Measurements are performed in a non-contact AC mode with an amplitude of 50 nm and a scanning speed of 0.1 /s. The resolution of rooted mean surface roughness is 0.1 nm. Surface roughness is investigated using two different parameters of R_a and RMS in this thesis. R_a is the roughness average of examined surface profiles. It is calculated as the following equation:

$$R_a = \frac{1}{\ell} \int_0^\ell |y| dx \tag{3.1}$$

, where the ℓ and the y are a total scanned length in the x-direction and the measured height. RMS is the root mean square roughness of surface profiles. It is calculated as the following equation:

$$RMS = \sqrt{\frac{1}{\ell} \int_0^\ell |y|^2 dx}$$
 (3.2)

According to the equation of 3.1 and 3.2, a single large peak within the surface profiles will affect the RMS value stronger than the R_a value. Therefore, a detailed surface topology can be understood by comparing the difference between R_a and RMS values [Saw20]. Furthermore, surface topology is further investigated using R_{SK} [RFR07]. R_{SK} is calculated using the following equation:

$$R_{SK} = \frac{1}{RMS^3} \left[\frac{1}{\ell} \int_0^\ell (y - R_a)^3 dx \right]$$
 (3.3)

It is used to measure the symmetry of the surface profile about the average roughness. When the distribution of surface profile about the average is symmetric, a R_{SK} value is close to zero, which means a flat and homogeneous surface. A positive R_{SK} indicates more peaks than valleys about the average roughness on the surface. On the contrary, the surface in which valleys are more dominant shows a negative value of the R_{SK} .

3.2.2 Electrical Characterization

In this thesis, electrical characterizations are performed via direct current (DC) voltage and pulsed voltage signals using a source-measurement unit (B2901A; Keysight, Santa Rosa(CA),

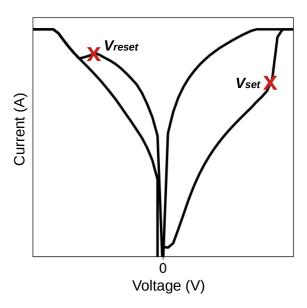


Figure 3.2: Determination of switching voltages. The SET (V_{set}) and the RESET voltage (V_{reset}) are marked with X.

United States). DC voltage measurements allow for examining resistive switching behaviors that are visualized as a hysteretic I-V loop (see Figure 2.1(b)). Additionally, they help to determine critical bias points that can be used for pulsed voltage measurement. Pulse measurements are used to investigate the memory performance for applications such as retention and linearity trend in the conductance update of memristive devices.

As for the DC voltage measurement, DC voltages are swept incrementally starting from zero to selected peak voltages in a triangular waveform (see Figure 2.1(a)). Voltages are applied to the top electrodes of memristive devices, while the bottom electrodes are grounded. Aperture time is set to 4e-2 s, which is the integration time for one-point measurement. During the DC voltage measurement, current compliance is imposed to prevent devices from permanent damage, if it is necessary. As a result of DC voltage sweep measurements, I-V characteristics are obtained. Based on the DC sweep measurements, the amplitude of switching voltages and reading voltages are determined that are used for pulse measurements. As seen in Figure 3.2, when the voltage increases, at the marked bias point V_{set} , the resistance starts decreasing at a higher rate than during the previous voltage sweep. The marked voltage point is defined for the SET voltage in this thesis (see the definition of the SET and RESET processes in ch.2.1). Similarly, the RESET voltage is defined as where the resistance starts increasing at a higher rate. The bias point V_{reset} is marked in Figure 3.2. To automize the procedure of switching voltage extraction, SET and RESET voltages are defined where the second derivative of current values $(\Delta(\frac{\Delta I}{\Delta V}))$ are the maximum and minimum, respectively [YTM+19]. It is because the magnitude of the second derivative shows the instantaneous acceleration of the current, and the sign indicates the direction of the acceleration. Reading voltages for the respective memristive devices are chosen through trial and error. Here, the reading voltage is small enough not to influence the device states but large enough to sense the current in our measurement setup.

4 Technological Development of Oxide Materials

Most outstanding RS characteristics have been demonstrated in memristive devices based on transition metal oxides [Saw08, DVRRS18, CBM+21]. RS characteristics are closely linked to the oxide properties in metal-oxide-based memristive devices [WWNX10, SAR+18, SJV+16, MSJ+11]. The oxide properties are, in turn, strongly dependent on the fabrication process [SVML+17, PKI+21]. Among the processes, sputter deposition is an attractive method for the deposition of metal oxides, in that the material properties can be tailored by adjusting the process parameters [ZSS+19]. For example, the deposition rate is a critical factor in the reactive deposition mode to determine the composition of the oxide materials and their properties [Pan13]. Additionally, Zahari et al. reported that plasma condition affects the oxidation state in the metal oxide films [ZSS+19]. Hence, investigating the relationship between the process parameters and the deposited oxide properties is important to find methodologies to adjust oxide properties. This investigation, furthermore, allows for realizing metal-oxide-base memristive devices with desired performance.

In this chapter, the recent achievements in memristive devices based on two transition metal oxides (TiO₂ and HfO₂) are outlined first. It provides a link between RS characteristics and the materials used for the memristive devices. Based on that, a strategy of material system designs for memristive devices is proposed. In the following, we present a development of the deposition process of three memristive materials (TiO₂, HfO₂, and Al₂O₃). As a deposition method, reactive sputtering is used via DC magnetron sputtering. The relevant parameters of the deposition are introduced which include deposition rate, the ratio of the reactive gas mixture, and the rotation function of the substrate holder in the sputtering chamber. Afterward, the effect of the process parameters on the material properties is investigated. The material properties are examined using SE, XPS, XRD, and AFM techniques. The details of the process parameters of sputtering and characterization methods are described in ch.3.

4.1 Material Systems for Memristive Devices

Among all kinds of redox-based memristive devices that have been reported, TMOs-based systems such as TiO₂ and HfO₂ are the most extensively studied [Saw08, CLW⁺17]. Since the 1960s, the RS phenomena of TiO₂ have been widely analyzed [SRS⁺11]. What is more, the firstly realized memristive device was based on TiO₂ [SSSW08]. TiO₂-based memristive devices have demonstrated good endurance [YTNS07] and low power consumption [XMDZ17] as filamentary-type devices (see VCM-type in ch.2.1). In particular, when TiO₂ layers are used combined with HfO₂ layers, the memristive devices have shown remarkable RS performance in terms of endurance [JHL⁺16] and variability [JHD16, YDZ⁺16]. HfO₂ is a CMOS compatible material. Along with this technological advantage, HfO₂-based memristive devices

(filamentary-type) have attracted a lot of attention. Those devices in a form of single or multilayer oxide systems have shown outstanding performance which fulfills the most aspects of requirements (see ch.2.2) including endurance [JHL+16], analog switching [HSZ+17], retention [CGC+13, JHL+16], variability [YGD+09, KPK+18], and low power consumption [SBN+20]. Moreover, interface-type switchings (see VCM-type in ch.2.1) have been observed in many HfO₂-based devices [RK20, JKR+21, MFL+17, YYS+16]. Among them, good retention has been demonstrated in which Al₂O₃ or Al are embedded in the memristive layers [HCZ+16, JKR+21]. Enhanced retention by using Al₂O₃ layers has been reported in many filamentary-type devices as well [WQC+15, VWJ18]. Moreover, analog switching [SKT+17] and good variability [YGD+09] have been demonstrated by adding Al₂O₃ layers in filamentary-type devices.

In summary, remarkable performance was observed in memristive devices in which several metal oxide layers are stacked creating multilayer metal oxide systems. In those multilayer systems, HfO_2 layers served as active RS layers that determine major RS characteristics. Adding TiO_2 layers enhanced endurance and variability. Inserting Al_2O_3 layers into the multilayer systems improved retention, analog switching, and RS uniformity. Based on the survey of memristive devices that could be utilized in neuromorphic computing applications, three metal oxide materials (HfO_2 , TiO_2 , and Al_2O_3) were chosen for building blocks of multilayer systems for memristive devices in this thesis.

4.2 Titanium Dioxide

In this section, the general material properties of titanium dioxide (TiO₂) are first briefly described. In the following, impacts of the ratio of the reactive gas mixture on material properties of deposited TiO₂ layers are introduced. Finally, a calibration method to obtain desired material properties is proposed.

4.2.1 General Material Characteristics

Ti is a transition metal that can have various valence states. Thus, titanium oxide shows various phase transitions depending on oxygen partial pressure and temperature. Among them, thin TiO_2 films are widely used in a variety of applications, not to mention in memristive devices [Ste20, SRS+11]. TiO_2 has advantages in manufacturing due to its simple composition, easy fabrication, and low production cost [IMC+20, JLC10]. The electrical and chemical properties of TiO_2 depend on the amorphous or crystalline phase and the concentrations of oxygen vacancies (which is the respective positions of a loss of oxygen atoms in the crystal lattice). Deposition of TiO_2 layers at room temperature generally results in amorphous TiO_2 [Ste20]. However, for some cases, locally crystallized TiO_2 grains embedded in amorphous TiO_2 are observed as well [Jeo09]. Amorphous TiO_2 layers show refractive indices of around 2.4 [BF17]. It has a high bandgap of 3.5 eV with a high electrical resistivity of $10^{11}\Omega \cdot \text{cm}$ [Sta03]. It is regarded as an n-type semiconductor. The electrical conductivity of TiO_2 depends on the concentration of oxygen vacancies, i.e., the more the oxygen vacancies are, the larger the conductivity in TiO_2 layers [HALL+18]. The described material properties are summarized in Table 4.1.

4.2.2 Process Parameters for Sputter Deposition

Gas partial pressure can influence deposition rate in sputtering [SPM+07]. Moreover, the deposition rate is a critical factor that determines the composition of the oxide materials and their properties [Pan13]. Therefore, careful observation of the gas partial pressure is needed to obtain desired oxide materials with high yield. In this section, we present the impacts of gas partial pressure on the material properties of sputtered TiO₂ layers. In our sputtering systems, gas partial pressure is monitored via the gas flow rate which is directly related to pressure differential, i.e., the greater the gas pressure is, the greater the gas flow rate. Afterward, a method to calibrate the sputtering process is proposed.

Deposition Rate

Three different TiO_2 layers were prepared by using a reactive gas mixture of O_2/Ar with three different volumetric (*sccm*) ratios: 10/90, 10/61, and 10/40. Except for the gas mixture ratio, other process parameters were kept constant. The thicknesses and the refractive indices were obtained using an ellipsometer. Figure 4.1(a) shows the results for the individual O_2/Ar ratio. The highest refractive index was found for the gas mixture of $O_2/Ar = 10/40$. We assume that the film has the most compact microstructure among the three films [MCLDS14, EPP+07]. A densely packed structure contains a low density of defects [RLZ11]. Also, it suppresses the formation of oxygen vacancies that decreases the resistivity of the TiO_2 film [RTSK19]. Oxide films with low pristine resistivity can make RS hard to be triggered [SPLT17].

Deposition rates were calculated by dividing the measured thickness by the duration of deposition. The deposition rate increases with increasing partial pressure of Ar as shown in Figure 4.1(a). Increasing Ar pressure may increase the number of Ti ions [KFS⁺99]. However, stoichiometric TiO_2 films are only obtained at sufficient O_2 partial pressure [KFS⁺99]. It is because more O_2 is present for the oxidation reaction. Further increasing the O_2 partial pressure (or decreasing Ar pressure), however, can yield a higher oxygen deficiency due to the negative oxygen ion bombardment of the substrate, which can be recognized by a saturated deposition rate [TPD⁺02]. Here, the film deposited under the $O_2/Ar = 10/40$ shows the lowest but not yet saturated deposition rate. Moreover, the refractive index is the highest among the three and comparable to the value that is reported by Butt et al. [BF17]. Therefore, we assume that the film is close to the stoichiometric ratio of TiO_2 .

Holding the gas mixture of $O_2/Ar = 10/40$, the sputtering duration was varied. The deposition rate and the refractive indices are shown in Figure 4.1(b). The deposition rate decreases with increasing sputter time assumingly due to the oxidation of the Ti source target [PPD+01]. The refractive indices decrease with increasing duration of deposition. The reason could be a different structure within the TiO_2 film, or the influence of the reflected light at the film-air interface in ellipsometry measurement as reported by Kasikov et al. [KAM+05].

Calibration of Deposition Rate

As shown above (see Figure 4.1(a)), the deposition rate of the TiO_2 layers is determined by the reactive gas flow. To keep track of the reactive gas flow, the angle of the butterfly valve

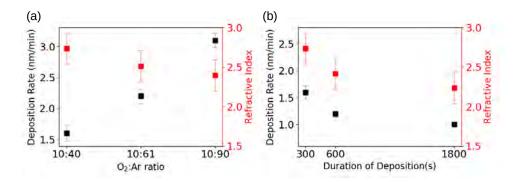


Figure 4.1: Refractive indices and deposition rates of TiO₂ films for (a) the variation of reactive gas mixtures and (b) duration of deposition.

Oxide	TiO_2	HfO_2	Al_2O_3
Bandgap energy (eV)	3.5	5.6	6.67
Electrical resistivity (Ω ·cm)	10^{11}	10^{14}	10^{14}
Oxygen diffusion coefficient (cm ² /s)	10^{-13} [BCK21]	10 ⁻¹⁴ [ZJEG 11]	10^{-19}

Table 4.1: General material properties of oxide materials (see the reference in texts)

was recorded in our sputter system, which indicates the amount of gas that enters the sputter chamber. For example, the change of the angle from 30.3° (for experiments shown in Figure 4.1) to 30.6° reduced the deposition rate from 1 nm/min to 0.5 nm/min, in which the same sputtering condition (working pressure, working power, source-target distance, and $O_2/Ar = 10/40$) was used. An increase in the valve angle means that an increased gas mixture was introduced into the chamber. We assume that the O_2 partial pressure in the gas mixture was increased since a higher O_2 partial pressure is more likely to reduce the deposition rate. In the calibrated sputtering parameters (30.6°), the TiO_2 film showed a thickness of 15 nm for the sputtering time of 30 min, a refractive index of 2.2, oxygen stoichiometry of Ti: O = 1: 2, and amorphous or nanocrystalline phase.

4.3 Hafnium Dioxide

In this section, the general material properties of HfO_2 are first briefly described. In the following, the development of the deposition process of HfO_2 layers is presented. Investigated process parameters include the ratio of the reactive gas mixture, the rotation of the substrate holder, and the distance between source target to wafer.

4.3.1 General Material Characteristics

HfO₂ shows various phase transitions depending on oxygen partial pressure and temperature [GGS⁺17]. The structure of HfO₂ deposited at a low temperature (<500 °C) is often observed as amorphous phases [CMR⁺18]. However, for some cases, locally crystallized HfO₂ grains embedded in amorphous HfO₂ are observed as well [MSPD⁺06, LBH⁺13, KMS03]. The amorphous structures show refractive indices of around 2 [PYK16, WOM⁺19]. They have generally

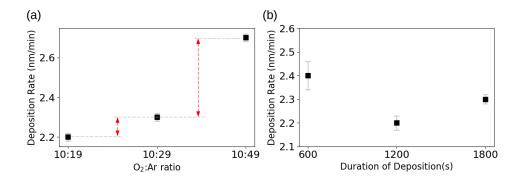


Figure 4.2: Deposition rates of HfO₂ films for (a) the variation of reactive gas mixtures and (b) duration of deposition.

a higher resistance than the crystalline structures such as monoclinic and tetragonal phases [ZMT+01, ZTG+02]. Therefore, amorphous HfO₂ has played an important role as an insulating layer in Si-based semiconductor devices [GCJC+03, GJ18]. Therefore, the compatibility with the silicon electronic manufacturing processes has offered an advantage as a material for memristive devices [RK21]. It has a wide bandgap of 5.6 eV [KVZ+21] and a high electrical resistivity of $10^{14} \,\Omega \cdot \text{cm}$ [LBH+11]. Moreover, the electrical properties of HfO₂ layers depend on their defect structures, which is expressed as a deviation from the ideal oxygen stoichiometry [KVZ+21]. For example, the larger the deviation is in HfO_x layers is, where x <2, the lower the resistivity of the films is observed [HKM+11]. The described material properties are summarized in Table 4.1.

4.3.2 Influence of Ratio of Reactive Gas Mixture

We prepared three different HfO₂ films varying the ratio of the reactive gas mixture of O₂/Ar with three different volumetric (sccm) ratios: 10/19, 10/29, and 10/40. All three samples showed the refractive indices of 2.0 ± 0.1 in ellipsometry measurements. The thicknesses of the films were measured using an ellipsometer and confirmed via a profilometer measurement. The deposition rate was calculated in the same manner as in the previous section. In Figure 4.2(a), the highest rate is observed in the gas mixture of O₂/Ar = 10/49. For the other two conditions, a much smaller difference in the rate is found. We assume that the ratio of O₂/Ar = 10/29 is a condition near the saturation point at which the maximum amount of O₂ can contribute to the film composition. Holding the deposition condition of O₂/Ar = 10/29, the duration of sputtering was varied. The fastest deposition rate was observed for the sputtering duration of 600 s as seen in Figure 4.2(b).

4.3.3 Influence of Substrate Rotation

During reactive sputtering, a rotation of the substrate may change the plasma parameters on the surface of the substrate [ZSS+19, Pan13]. It affects the ratio between the reactive gas and the sputtered materials. Thus, the rotation can give an impact on the composition of the deposited film.

In our sputtering system, three source targets are equipped co-axially on the top of the chamber as seen in Figure 4.3(a). This configuration results in the variation in the target-substrate distance. For example, for a 4-inch wafer, the variation is 31 mm between the minimum and the maximum distance, as shown in Figure 4.3(b). If the substrate holder is not rotated during the deposition, the distance variation is held constant. Thus, it can lead to different deposition rates at different positions on the substrate [ZSS12]. We

deposited HfO_2 films in an $O_2/Ar = 10/29$ gas mixture, controlling the rotation function of the substrate holder: rotation mode or stationary mode. During the deposition, the other process parameters were kept the same. The fabrication process is detailed in chapter 3. The material properties of the HfO_2 films were analyzed using ellipsometry, profilometer, XPS, XRD, and AFM methods. The methods of analysis are detailed in chapter 3.2.

Deposition Rate

Rotation Mode: A HfO_2 film was sputtered for 900 s using rotation mode on a 4-inch wafer. The thickness of the HfO_2 film was estimated using ellipsometry measurements (SenResearch 4.0, see details in ch. 3.2) at 8 randomly chosen spots over the 4-inch wafer. Over the 4-inch wafer, the average thickness was 37.3 nm with a variation of 1.5 nm. The deposited film showed good uniformity in the thickness.

Stationary Mode: In the previous section, the deposition rate was slightly faster for a shorter sputtering time as shown in Figure 4.2(b). To check the deposition rate for a thin HfO₂ layer, we deposited a HfO₂ film as thin as possible, while still being able to measure the thickness using our ellipsometer and profilometer. If films are too thin, it is hard to obtain reliable results. A HfO₂ film was deposited for 230 s on a 4-inch wafer without rotating the substrate. Its thickness and the refractive index were measured at five spots over the wafer. The results are summarized in Table 4.2. The positions on the wafer were numbered in the order of increasing source-substrate distance, as seen in Figure 4.2(b) and (c). For example, pos.1 and pos.5 refer to the furthest and the closest position from the source target, respectively. Pos.3 is located at the center of the substrate. The thickness in pos.3 was approximately 10 nm both in ellipsometry and profilometer measurements. The thickness in the direction toward pos.1 was thinner, whereas that in the direction of pos.5 was thicker than in pos.3. A schematic of the deposited film is shown in Figure 4.3(c). Along an imaginary line from pos.1 to pos.5, a gradient of the thickness was observed in the HfO₂ film. Based on the thickness gradient, we extrapolated a thickness for a thinner HfO₂ film. At first, we assume the HfO2 grows at each position proportionally to sputter time. Following, we calculated the deposition rate at each position, dividing the thickness of the film by the sputtering time of 230 s. For example, for the sputtering time of 115 s, the center of the HfO₂ film will be approximately 5 nm. The thinnest is expected to be 2 nm, and the thickest is to be 8 nm on a 4-inch wafer. These values are used for analysis in chapter 5.2. In terms of refractive index, higher values were observed in general than the refractive index of the uniform HfO₂ film of 2.0. In the following, a uniform HfO₂ and a wedge HfO_x films stand for the film sputtered using a rotation mode and a stationary mode, respectively.

It is worth mentioning a large thickness variation between the results of the ellipsometer and profilometer in pos.1 and pos.5. For pos.1, the reason could be the influence of the reflected light at the film-air interface in ellipsometry measurement [KAM $^+$ 05] due to its thin thickness. Also, the variation may be caused by irregular surface roughness of the film. In our setup, the scanned area size in the ellipsometer is larger than that in the profilometer. The thickness from the ellipsometer is averaged over the area in a mm² range, while the profilometer scans the height of a structured step with a spatial resolution of several tens of μ m. Therefore, we averaged the thicknesses of the thin HfO_x film in the analysis to compensate for the limitation of the two measurement methods.

Oxygen Stoichiometry

Rotation Mode: A uniform HfO_2 film was sputtered for 900 s on a 4-inch wafer. The oxygen stoichiometry in the HfO_2 was investigated using XPS. Deposition in rotation mode resulted in a Hf/O ratio of 1/1.98 [PKI+21], which fits almost the stoichiometric ratio of HfO_2 .

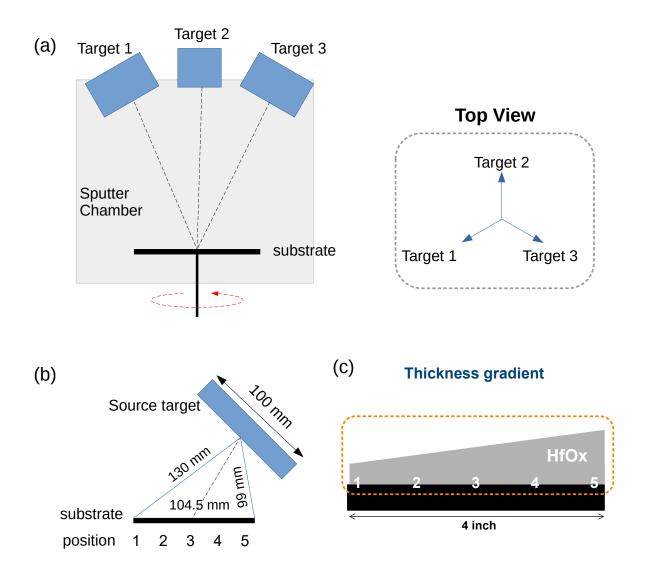


Figure 4.3: (a) Left: cross-section of the used sputter system. Three source targets are equipped co-axially on the top of the chamber. The substrate holder can be rotated during the deposition process. Right: top-view of the arrangement of three source targets. (b) Distance from the source target and substrates are shown. The labeling method used for analysis is also illustrated: pos.1 is the closest and pos.5 is the furthest from the source target. (c) A thickness gradient of the deposited HfO_x film when using a stationary mode.

position	pos.1	pos.2	pos.3	pos.4	pos.5
Thickness in profilometer (nm)	3	6	9.5	9.5	14
Thickness in ellipsometer (nm)	6.71	8.14	10.66	14.48	18.55
Refractive index	2.471	2.407	2.103	2.109	1.747

Table 4.2: Distribution of thickness and refractive index of the HfO₂ film that is sputtered using a stationary mode.

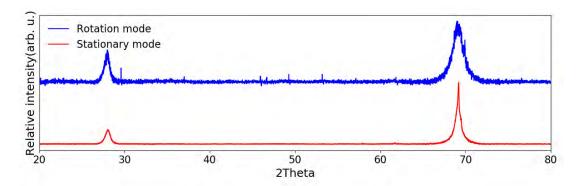


Figure 4.4: XRD spectra of the HfO₂ film and the HfO_x sputtered in a rotation mode and a stationary mode, respectively.

Stationary Mode: We further studied the oxygen stoichiometry in the wedge HfO_x using XPS measurement. We prepared three 1×1 cm² SiO₂ substrates and placed them in pos.1, pos.3, and pos.5 on the substrate holder in the sputtering chamber (see Figure 4.3(b)). The pos.1, 3, and 5 are named in the order of increasing film thickness on the 4-inch wafer, respectively. The HfO_x films showed a Hf/O_x ratio of 1/1.95, 1/1.80, and 1/1.81 in pos.1, pos.3, and pos.5, respectively. In pos.5, the largest deviation from the ideal oxygen stoichiometry was observed. We assume that a position closer to the target source contains more sputtered Hf ions. It might result in an insufficient amount of oxygen ions that can react to the Hf ions. Thus, it causes a higher deviation from the ideal stoichiometry of HfO_2 . The impact of oxygen stoichiometry in HfO_2 films on electrical properties is discussed in ch. 5.2.1.

Structural Property

A HfO $_2$ film and a HfO $_x$ film were sputtered for 900 s on 4-inch Si wafers. The structural properties of the two films were investigated via XRD measurements. Figure 4.4 shows an XRD spectrum of a uniform HfO $_2$ and a wedge HfO $_x$ films in a full scanned range from $2\theta = 20$ ° to 80°. Examined XRD results were normalized with respect to the Si(100) peak at 69°. Both showed the major characteristic peaks near a 2θ of 28° which corresponds to the ($\overline{1}11$) plane of a nanocrystalline monoclinic-HfO $_2$ (m-HfO $_2$) [BMSB $^+21$]. However, a stronger intensity was observed in the HfO $_2$ film, as seen in Figure 4.5, which indicates a larger average grain size and a better-oriented structure along ($\overline{1}11$) plane than the HfO $_x$ film [MSPD $^+06$]. In the following, the major characteristic peaks of the individual films were focused on for a more in-depth investigation.

Rotation Mode: An XRD spectrum of the HfO_2 film is shown in Figure 4.5. The major characteristic peak was found at 28° on the 2theta (2θ) scale. It corresponds to the $(\bar{1}11)$ plane of a nanocrystalline monoclinic- HfO_2 (m- HfO_2) [BMSB+21]. HfO_2 films deposited at a low temperature ($<500^{\circ}$) are often amorphous [CMR+18]. Considering that, we assume that the film has crystalline structures embedded in an amorphous matrix as demonstrated by many other works in literature [MSPD+06, LBH+13, KMS03].

Stationary Mode: The structural properties of the HfO_x films were examined in detail at five different positions on the wafer using the XRD method. The positions are named as pos.1, 2, 3, 4, and 5 in the order of increasing film thickness, respectively (see Figure 4.3(c)). The spectra peaks are shown in

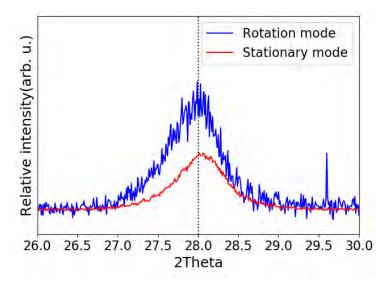


Figure 4.5: XRD spectra of the HfO_2 films sputtered in a rotation mode and a stationary mode. The peaks corresponding to ($\overline{1}11$) planes of m-HfO₂ are observed in both films.

Figure 4.6(a). The major characteristic peak in pos.3 was found at 28.1 ° on the 2θ scale that corresponds to the ($\overline{1}11$) planes of m-HfO₂ [RBGC12, BMSB⁺21]. The ($\overline{1}11$) peak in pos.1 was seen at $2\theta = 28.12^{\circ}$, and in pos.5 at $2\theta = 28.06^{\circ}$. A shift of the diffraction peaks toward a lower 2θ angle was observed with increasing film thickness. However, the thicker the film is, the greater intensity is obtained [ACST11]. Therefore, it is difficult to compare the crystalline structures of the five positions with the intensity alone. Each diffraction spectrum was normalized by respective intensity at the major characteristic peak for each position. Figure 4.6(b) shows different widths for each position on the 4-inch wafer. To compare the widths, the full width at half maximum (FWHM) was measured from the spectra which are defined as the broadening of the diffraction line measured at half its maximum intensity. The widest FWHM (2θ) of 0.79° was observed in pos.1, while the narrowest of 0.68° in pos.5. The FWHM decreased with increasing thickness. The crystalline sizes (D) were estimated for the respective positions using the Scherrer's equation as the following [KBKR10]:

$$D = \frac{0.9\lambda}{\beta cos\theta} \tag{4.1}$$

where the λ , the β , and the θ are the X-ray wavelength, the FWHM, and the angle of the peak. According to the equation, pos.1 showed the smallest D, while pos.5 has the greatest D, i.e. the D increases with the increasing thickness of the HfO_x film. The larger the crystalline size is, the larger electrical conductivity is obtained in HfO_x films [KBKR10]. Therefore, pos.5 is likely to exhibit a higher leakage current than the other positions.

Surface Roughness and Morphology

A HfO₂ film and a HfO_x film were sputtered for 900 s on 4-inch Si wafers. The surface roughness and morphologies of the two films were investigated via AFM measurements. The details of roughness parameters used in the following analysis (R_a , RSM, R_{SK}) are explained in ch.3.

Rotation Mode: Figure 4.7 shows the obtained morphology image and the surface profile. The size of the examined area was $15 \times 15 \ \mu\text{m}^2$. The HfO₂ film shows almost homogenous and uniform surface

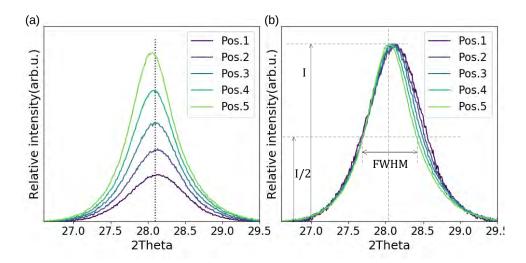


Figure 4.6: XRD spectra for the wedge HfO_x film. (a) Normalized diffraction spectra by the intensity of the Si(100) peak. (b) Normalized diffraction spectra by respective intensities of $(\overline{1}11)$ planes of m-HfO₂.

morphologies. The roughness average (R_a) of 1 nm and the root mean square roughness of surface (RMS) of 2 nm were obtained over 15 × 15 μ m². To describe the details of the surface topography skewness of the profile (R_{SK}) were calculated [RFR07] which was 2.8. The larger value of the RMS than the R_a and the positive R_{SK} value implied that large peak structures exhibit over the film (see roughness parameters in ch.3.2). The surface profile is visualized in Figure 4.7(lower) which was scanned along the marked path (see Figure 4.7(upper)). Although peak structures are observed, they are distributed homogeneously with a distance of around 5 μ m to each other. As a memristive layer, the peak structures of the HfO₂ film can be used to enhance the electric field [PJSM13], resulting in low operating voltages in memristive devices. Furthermore, the peak structures can serve as interface traps at Schottky junctions [SMK+09] in which electric charges are captured and released. Those interface traps can cause interface-type RS operations (see VCM-type in ch.2.1) [BKK14]. Therefore, the deposited HfO₂ film seems to be a promising candidate for memristive layers. Memristive devices consisting of the HfO₂ layer is presented in ch.5.2 and ch.5.3.

Stationary Mode: After depositing a HfO_x film on a 4-inch wafer, the wafer was cleaved into four pieces. Pos.1, 2, 3, and 4 were named in the order of increasing thickness in the HfO_x film similarly to the labeling method shown in Figure 4.3(c). The scanned area was $15 \times 15 \ \mu \text{m}^2$ for each position. Figure 4.8 shows surface morphology images and surface profiles of the examined four spots. In pos.1, an extremely smooth surface is shown in Figure 4.8(a). The R_a and the RSM were both 0.1 nm over the examined area. It is close to the measurement limit of the used AFM setup. In pos.2, the R_a and RMS over the examined area were 0.8 nm and 1 nm, respectively. The two roughness parameters are almost the same, indicating a homogenous and smooth surface profile. The roughness parameters are summarized in Table 4.3. Moreover, a textured morphology was observed, as seen in Figure 4.8(b). The morphology exhibits certain orientations. The periodic ripple patterns were scanned along a line drawn perpendicularly to the orientation, as marked in the AFM image (see Figure 4.8(b) (upper)). The distance between adjacent peaks (S_m) was around 2.3 μm on average. In Figure 4.8(c), the surface in pos.3 seems homogenous and smooth. The Ra and the RMS over the examined area were 0.8 nm and 1 nm, respectively. Similarly to pos.2, a textured morphology was observed. The S_m was 2.7 μm on average. When comparing the roughness parameters of the pos.2 and the pos3, both have very smooth and homogenous surfaces. However, the S_m value of the pos.3 is greater than that of the pos.2, which

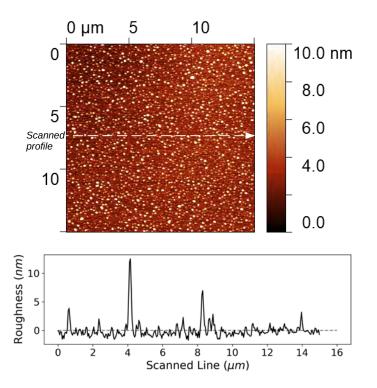


Figure 4.7: Upper: AFM topography with area window $50 \times 50 \ \mu m^2$ of a uniform HfO $_2$ film. Lower: the surface profile along the marked path. In the surface profile, the baseline was corrected by the average roughness.

position	pos.1	pos.2	pos.3	pos.4
R_a (nm)	0.1	0.8	0.8	15.2
RMS (nm)	0.1	1.0	1.0	22.4
$S_m(\mu m)$	∞ (smooth)	2.3	2.7	1.8

Table 4.3: Roughness and the mean spacing(S_m) in the respective position in the wedge HfO₂ film obtained by AFM measurements.

indicates a growth of the ripple texture in the lateral direction to the substrate with increasing HfO_x thickness. Figure 4.8(d) shows surface morphologies in pos.4. It shows a textured structure with large spheroidal islands. In pos.4, R_a and RMS over the examined area were 15.2 nm and 22.4 nm, respectively. The discrepancy between the two roughness parameters and an R_{SK} of 2.3 indicate large odd peak structures on the surface. The surface profile is visualized in Figure 4.8(d) (lower) which is scanned along the marked path in the AFM image (see Figure 4.8(d)(upper)). The scanned path is perpendicular to the orientation of the ripple pattern. The S_m value on average was smaller than those in pos.2 and pos.3, and the textured pattern is more irregular. The islands appeared as sharp peak structures that were greater than the film thickness of 37.5 nm.

The measured parameters in the four spots are summarized in Table 4.3. In summary, the HfO_x film showed extremely smooth and uniform surface profiles except for pos.4. In pos.2 and pos.3, textured morphologies were observed as shown in Figure 4.8(b) and (c). The ripple patterns might be caused by a directional bombardment of oxygen ions on the surface of growing films [CDB09, LCT⁺13]. The ripple texture can increase the electric breakdown voltage, and decrease the leakage current[NSS07]. The profile in pos.4 displayed significantly rougher surfaces than the other spots. Additionally, spheroidal islands were grown on the surface. The significantly high island structures might reduce the production yield of memristive layers and increase the leakage currents.

Summary of Material Properties of sputtered HfO₂ Film

The influence of substrate rotation on the material properties was investigated. Using the rotation mode, uniform HfO_2 films were obtained, while wedge HfO_x films were deposited using the stationary mode. The refractive index was smaller in the HfO_2 films than in the HfO_x films, which might be attributed to a relatively smaller metallic content of the HfO_2 films [LBH+13]. The Hf/O ratios were examined via XPS measurements. The uniform HfO_2 film showed a nearly stoichiometric ratio of HfO_2 , whereas the HfO_x film showed a larger deviation from the ideal oxygen stoichiometry. In XRD measurements, monoclinic crystalline structures were observed in both the HfO_2 and the HfO_x films. We assume that the crystalline structures are embedded in an amorphous phase. The surface morphologies were investigated using AFM measurements. The uniform HfO_2 film showed a homogenous surface with a roughness of 1 nm, in which uniformly distributed peak structures were observed. A smoother surface was observed in the HfO_x film except for in the thickest region in which significantly large island structures were observed.

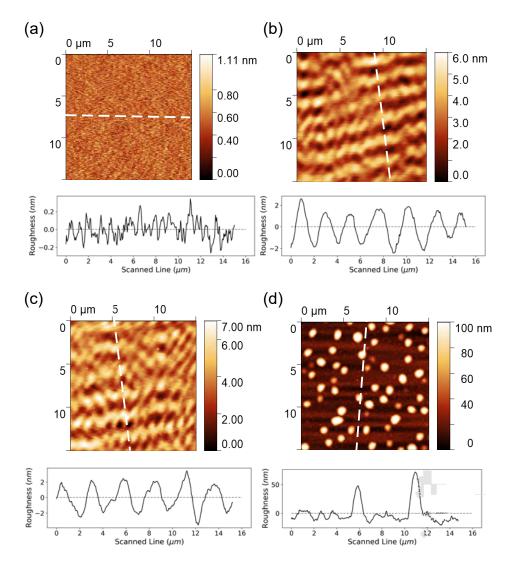


Figure 4.8: AFM morphology images and the roughness profiles at (a) pos.1, (b) pos.2, (c) pos.3, and (d) pos.4 in the order of increasing thickness. In the surface profile, the baseline was corrected by the average roughness.

4.4 Aluminum Oxide

In this section, the general material properties of aluminum oxide are first briefly described. In the following, the development of the deposition process of AlO_x layers is introduced.

4.4.1 General Material Characteristics

Thin aluminum oxide (AlO_x) layers thermally oxidized at room temperatures have long been employed to achieve high-performance metal-insulator-metal tunnel junctions [TMP⁺05]. Those AlO_x films are often amorphous structure [JSTM00]. The bandgap energy is 6.67 eV [LMR⁺15] and an electrical resistivity is about $10^{14} \Omega \cdot \text{cm}$ [bGEWbhs19]. Amorphous aluminum oxides attracted attention for non-volatile memory application as well [WQC⁺15, VWJ18, YGD⁺09]. AlO_x are often used as charge trapping and blocking layer in memristive layers, which can improve retention [JKR⁺21]. This is because of a low oxygen diffusion coefficient of about $10^{-19} \text{ cm}^2/\text{sec}$ [JKR⁺21], which means oxygen ions hardly move in AlO_x. Moreover, non-stoichiometric AlO_x layers or Al/AlO_x stacks have improved reliability of RS operations in memristive devices [MGC⁺21, AKKL17]. The described material properties are summarized in Table 4.1.

4.4.2 Process Parameters for Sputter Deposition

For AlO_x films, native silicon oxide on the Si substrates was etched using an HF solution. On each of the Si substrates, Al layers (2nm) were sputtered with a deposition rate of 0.3 nm/s. Afterward, the gas mixture of Ar and O_2 into the sputter chamber was introduced. The working pressure was 5e-2 mbar during oxidization of the Al layers, in which the gas mixture of Ar/O_2 with a volumetric (*sccm*) ratio of 30/10 was used. The Al layers were oxidized for 15 mins or 30 min. Therefore, two different types of AlO_x layers were realized.

The thicknesses of oxidized Al layers were investigated using an ellipsometer. For analysis, a fitting model consisting of substrate/Al/Al-interfacial layer/Al $_2$ O $_3$ was used, considering the oxidization mechanisms of Al layers [HMS09]. For the fitting, the thickness of all three layers was fitted, while the refractive indices were kept constant. This technique significantly reduces the number of fitting parameters, easing obtaining the thickness of transparent and thin films [MJW93]. The refractive indices were 1.604, 1.381, and 1.351 for the Al $_2$ O $_3$, the Al-interfacial layer, and the Al layer, respectively. Those refractive indices were referred to from the material library provided by SENTECH Instruments GmbH (Berlin, Germany). The Al film oxidized for 15 mins (which is referred to as Al-O-15 in the following) showed an Al $_2$ O $_3$ layer of 1.8 nm and an interfacial layer of 1.2 nm. The film oxidized for 30 mins (which is referred to as Al-O-30 in the following) showed an Al $_2$ O $_3$ layer of 3.83 nm and an interfacial layer of 0.5 nm. The Al-O-30 film presented a thicker oxide product than the Al-O-15 film. Both films showed no Al layer in the fitting.

Stoichiometry of the two films was investigated via XPS measurements. For the Al-O-15 film, $80.95\,\%$ oxide product (Al₂O₃) and 19.05% metallic Al were observed. For the Al-O-30 film, $86.94\,\%$ of oxide product and 13.06% metallic Al were examined. The XPS results showed the presence of Al within the films, while the results from ellipsometry measurements above showed no Al layer. However, both results clearly indicate the presence of more oxide products in the Al-O-30 film than in the Al-O-15 film in a substrate/Al/Al-interfacial layer/Al₂O₃ structure. For AlO_x layers to serve as oxygen barriers in memristive devices, a sufficient amount of oxidized products is needed. Therefore, the Al-O-30 film seems a better choice [DSCS03, GGC+02].

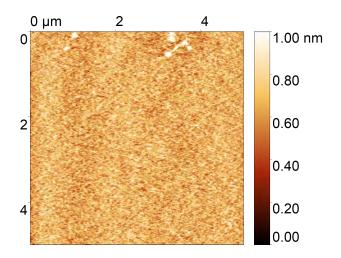


Figure 4.9: An AFM image of an AlO_x layer oxidized for 30 mins.

The roughness of the Al-O-30 layer was investigated via AFM measurements. Examined area size was $5\times 5~\mu m^2$, as shown in Figure 4.9. The R_a and the RMS were both 0.1 nm, indicating an extremely smooth surface. A smooth surface of the Al-O-30 layer can improve the uniformity of memristive devices.

5 Tailored Resistive Switching Characteristics: Metal-oxide-based Memristive Devices

In recent years, there has been significant technological progress in memristive devices. A common goal is to realize memory performance that fulfills requirements for respective neuromorphic applications (see chapter 2.2.2) [TAN+18, SWW+21]. In this respect, it would be convenient to have a handbook with which one can design memristive devices that contain desired electrical properties. In this chapter, it is shown how to select materials for metal-oxide-based memristive devices and how to engineer memristive characteristics by modifying the structure of memristive layers. This chapter consists of three sections. In the first section, various metal-oxide-based memristive devices are introduced. Their electrical properties are compared to one another to deduce the effect of the material properties on the RS characteristics. Based on the investigation, we design bilayer memristive devices consisting of TiN/TiO_x/HfO_x/Au which are introduced in the second section. Two types of bilayer memristive devices are fabricated using different oxygen stoichiometry in the HfO_x layer. They exhibit distinct RS mechanisms, i.e., filamentary-type and interface-type RS (see VCM-type in ch.2.1). The electrical characteristics of each type are tuned by adjusting the layer thickness and the active device area. The relationship between the electrical properties and device structures is analyzed using statistical methods. The last section presents trilayer memristive devices consisting of TiN/TiO_x/AlO_x/HfO_x/Au stack. The RS characteristics are investigated in terms of the requirement of an electroforming process, current compliance, and operating voltage range. The retention times are examined by controlling maximum applied voltages. Furthermore, the RS mechanisms in the device are discussed based on the experimental observation combined with a numerical simulation. Basic terminologies and RS mechanisms of memristive devices are described in ch.2.1. The material properties of the used memristive layers are found in ch.4. Details of the fabrication and the electrical measurements are described in ch.3.

5.1 Material Selection for Metal-oxide-based Memristive Devices

In metal-oxide-based memristive devices, the RS behaviors are caused by the transport of ionic and electric carriers in the metal oxide (MO) layers [Iel16]. The mobility and the density of the mobile electric/ionic carriers are determined by the material properties of the MOs. Thus, choosing the right MO is important to realize desired RS properties. Additionally, the material properties of MOs can be modified by the materials chosen as electrodes. For example, metal electrodes with a high oxygen affinity induce oxygen vacancies in the MO, which affects the RS characteristics [SK19]. In this section, a variety of memristive devices are fabricated to study the impact of oxide/electrode materials for memristive devices on their RS properties. Firstly, two types of memristive devices are presented that consist of different MOs: HfO₂ or TiO₂. Their RS characteristics are investigated individually. Afterward, the influence of

the MO materials on RS properties is discussed. In the second part, various TiO₂-based memristive devices are fabricated that utilize different electrode materials and configurations. The electrode materials used here are Al, TiN, and Au, which have distinct work functions and oxide formation energies. They are employed as bottom electrodes or top electrodes. The RS characteristics of individual memristive devices are analyzed. Finally, the impact of electrodes on the RS properties is discussed.

5.1.1 Metal Oxide Material and Resistive Switching Characteristics

We fabricated two types of metal-oxide-based memristive devices: Al/HfO₂/TiN device and Al/TiO₂/TiN device. The relevant layer stacks of the devices are depicted in Figure 5.1. Both had a 50 nm Al layer as the bottom electrodes (BEs) and a 50 nm TiN layer as the top electrodes (TEs), but different MOs (HfO₂ or TiO₂) for the switching layer. The detailed architecture of the memristive devices is found in Figure 3.1(a).

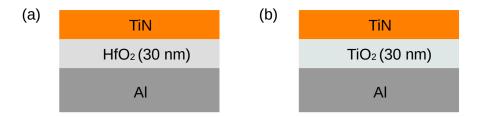


Figure 5.1: The relevant layer stacks of (a) an Al/HfO₂/TiN and (b) an Al/TiO₂/TiN.

The I-V curves of the two types of devices were investigated via DC voltage sweep measurements. During the measurements, consecutive sweep cycles were performed and adequate current compliance was imposed to prevent an electrical breakdown of the memristive devices. In the measurements, two schemes of voltage sweep were used as following: i) $0 \text{ V} \rightarrow \text{peak positive voltage} \rightarrow \text{peak negative voltage} \rightarrow 0 \text{ V}$, or ii) $0 \text{ V} \rightarrow \text{peak negative voltage} \rightarrow 0 \text{ V}$, as depicted in Figure 5.2. In the following, the former scheme is referred to as *positive-first*, and the latter *negative-first*.

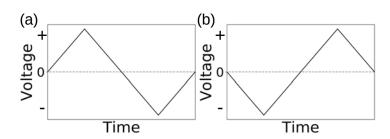


Figure 5.2: Voltage sweep schemes: (a) positive-first and (b) negative-first.

Unipolar Switching: HfO₂-based memristive devices (Al/HfO₂/TiN)

On memristive devices based on an Al/HfO $_2$ (30 nm)/TiN stack, DC voltage sweep measurements were performed using the positive-first scheme, in which two consecutive sweep cycles were conducted. The resulting I-V relation is presented in Figure 5.3(a). The pristine resistance of the device was in a HRS. In the first cycle, the resistance decreased, with increasing sweep voltage. At 4 V, the decrease in the resistance was stopped by the current compliance. While decreasing voltage to 0 V, a low resistance was

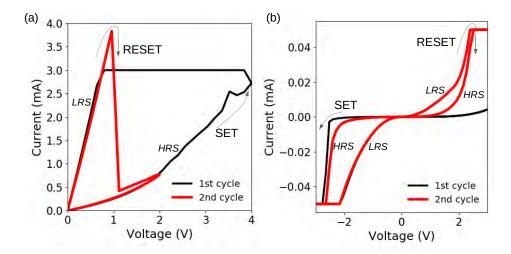


Figure 5.3: RS behaviors of (a) Al/HfO/TiN devices and (b) Al/TiO₂/TiN in DC voltage sweep measurements.

observed, which implies a transition from the HRS to a LRS (*SET process*). The LRS followed a highly ohmic (linear) I-V relation. In the second sweep cycle, the current compliance was turned off. The LRS was switched to the HRS at 0.95 V (*RESET process*), at which a higher current of 3.8 mA was observed. The device showed reversible RS between an HRS and an LRS. The obtained switching window (see ch.2.1) was 16 at 0.12 V.

Based on a highly ohmic I-V relation in the LRS, we assume that a metal-rich CF was formed through the HfO₂ layer during the SET process. The RESET process occurred with the same polarity as the SET process (*unipolar RS*). The RESET current was higher than the SET current. The I-V relations resemble typical characteristics of TCM-type devices [WDSS09] (see Figure 2.2(c) and (g)).

Bipolar Resistive Switching: TiO₂-based memristive devices (AI/TiO₂/TiN)

The RS characteristics of an Al/TiO₂(30 nm)/TiN device were investigated via DC voltage sweep measurements using the positive-first scheme, in which two consecutive sweep cycles were performed. The resulting I-V curves are shown in Figure 5.3(b). In the first cycle, the sweep voltage up to 3 V did not affect the device resistance. The first resistance drop was observed at -2.52 V. A further decrease in the resistance was limited by the current compliance. During the voltage sweep back to 0 V, the device showed an LRS. In the second consecutive sweep cycle, a resistance change in the LRS was observed at 1.8 V, which was limited by the current compliance. When the sweep voltage was decreased, an HRS was observed, which indicates a transition from the LRS to the HRS (*RESET process*). The resistance in the HRS was lower than the pristine resistance of the device. At -2.4 V the device resistance decreased, which was limited by the current compliance. During the voltage sweep back to 0 V, the LRS was observed, which indicates a transition from the HRS to the LRS (*SET process*). In the following sweep cycles, the RS behaviors were observed the same as in the second sweep cycle. Therefore, we could recognize the first sweep cycle as an EF cycle which initiated a stable RS operation. After the EF, the device showed a bipolar RS behavior (see the definition in ch.2.1).

Jeong et al. demonstrated [JLCK09] that the aluminum oxide layer formed at the Al/TiO₂ interface plays an important role in the RS operation. Considering the low energy for the oxide formation in Al, we assume that the Al BE formed aluminum oxide at the interface, taking oxygen atoms from the TiO₂ layer. A possible scenario for the RS mechanism is as follows: during the EF process, the negative EF voltage repelled oxygen ions in the TiO₂ layer toward the BE [JLRC10]. Thus, a large number of oxygen

vacancies were formed in the TiO_2 layer. Consequently, a CF was established, which dropped the device resistance. Under a positive voltage, the oxygen vacancies drifted toward the bottom electrode, which ruptured the CF in the TiO_2 layer. Therefore, the resistance switched back to the HRS.

Table 5.1: Comparison of the Al/HfO₂/TiN and the Al/TiO₂/TiN memristive devices. The V_{SET} , the V_{RESET} , the Swtiching Window_{@0.12V}, the E_{ox} , and the E_a are voltage at a SET process, voltage at a RESET process, switching window measured at 0.12 V, formation energy for oxygen vacancies, and activation energy for migration of oxygen vacancies, respectively.

Comparison of TiO₂ and HfO₂ as Switching Layer

The parameters of RS operations are summarized in Table 5.1. The Al/HfO₂/TiN device showed a unipolar RS behavior. The RS operation was an abrupt transition in the I-V curve in Figure 5.3(a), especially for the RESET process. Based on the main characteristics of the I-V curve, the RS mechanism is assumed to be a TCM effect (see ch.2.1). On the contrary, the Al/TiO₂/TiN device required the opposite polarity of switching voltages, indicating a bipolar RS behavior. Also, the RS operation was fairly gradual as seen in Figure 5.3(b), which implies a VCM effect (see ch. 2.1). Although the switching window was slightly smaller than the Al/HfO₂/TiN device as shown in Table 5.1, the Al/TiO₂/TiN exhibited a more stable RS behavior. For a stable RS operation, a sufficient amount of oxygen vacancies are required [SSL⁺17]. Al requires less energy for oxide formation than Ti and Hf [CYH+11]. Thus, an Al layer can induce oxygen vacancies in both oxides once in contact, forming the aluminum oxide. However, HfO2 requires 4.04 eV [CSB+14] to form an oxygen vacancy, while TiO2 needs 1.35 eV [PW15]. Thus, the amount of generated oxygen vacancies in the HfO2 layer is lower than in the TiO2 layer. Therefore, it might be insufficient for a stable RS. Moreover, the activation energy for migration of oxygen vacancies is 1.1 eV for TiO₂ [LLZ⁺12], while 2.4 eV for HfO₂ [GSMS19]. We assume that a high diffusion barrier in the HfO₂ layer makes oxygen vacancies hard to move within the film. Instead, a sudden current increase may occur due to a thermoelectric breakdown in the HfO₂ layer, which creates a CF. The current overshoot during the RESET process indicated that a TCM effect was dominant in the RS operation. However, a sufficient amount of oxygen vacancies in the TiO₂ layer can migrate with lower energy than in the HfO₂ layer. Thus, the TiO₂-base devices might show a VCM-type RS.

5.1.2 Electrode Material and Switching Characteristics

Electrode materials create an electronic barrier or interface state at the interface contacting MOs, which affects the RS mechanism in memristive devices [KR10, YR07]. The decisive factor for the interface condition is the work function and the oxygen affinity of electrodes [YSM+11, MAJK+16]. A high metal work function (Φ_M) and a low oxygen affinity may form a Schottky barrier (Φ_B) at the interface that defines an effective electric field across the MOs, as the following equation:

$$\Phi_B = \Phi_M - \chi \tag{5.1}$$

, where the χ is the electron affinity of MOs. An electrode material with a high oxygen affinity might react to MOs, leaving oxygen vacancies in the MOs behind. Many researchers have reported that se-

lecting the right material for the electrodes can reduce the EF voltage or even eliminate the EF process [SLK $^+$ 05, KMM $^+$ 19, PLP $^+$ 12]. In this section, TiO $_2$ -based memristive devices with various electrode configurations are demonstrated. The used materials for electrodes are Al, TiN, and Au. The Φ_M and the oxygen affinity (Enthalpy of Oxide formation) of the metals are summarized in Table 5.2. The effect of using Al and TiN as electrode materials on the RS operation is analyzed in terms of the oxygen affinity. Additionally, the effect of using TiN and Au as electrode materials are investigated in respect of the Φ_M . In the first part, the RS characteristics of a TiN/TiO $_2$ /TiN device and an Al/TiO $_2$ /TiN device are compared. As seen in Figure 5.4(a) and (b), the BEs consist of different materials in the two devices. We analyze the effect of using TiN and Al as the BE materials on the RS operations. Secondly, we study the impact of employing Al, TiN, and Au as the TE materials on the RS characteristics. The relevant layer stacks of the investigated devices are depicted in Figure 5.4 (a, d) and (b, c). The electrical characterization is based on DC voltage sweep measurements. In the measurements, two schemes of voltage sweep were used, as depicted in Figure 5.2.

Material	Work function(eV)	Enthalpy of Oxide Formation (kJ/mol)
Ti	4.33	-994 [CYH ⁺ 11]
Al	4.25 [YR07]	-1676
TiN	4.68 [YR07]	-578.8 [PGCV16]
Au	5.1 [YSM ⁺ 11]	-13 [AS72]

Table 5.2: Work function and enthalpy of oxide formation for metal materials of Ti, Al, TiN and Au.

Bottom Electrode

This section presents the RS properties of a $TiN/TiO_2/TiN$ device and compares them with those of an $Al/TiO_2/TiN$ device. The relevant layer stacks of two types of devices are depicted in Figure 5.4(a) and (b). They have the same thickness of TiO_2 (30 nm) as the switching layer and TiN (50 nm) as the TE. However, one device uses Al (50 nm) and the other TiN (50 nm) as the material for the BE. In the following, the $Al/TiO_2/TiN$ and $TiN/TiO_2/TiN$ are called Al-TiN, and TiN-TiN, respectively.

The I-V characteristics of a TiN-TiN device were investigated via DC voltage sweep measurements, in which two consecutive sweep cycles were performed. During the measurement, current compliance was imposed. The voltage was swept in the negative-first scheme. As seen in Figure 5.4(a), at -4 V a significant drop in the pristine resistance of the device was observed in the first sweep cycle. A further decrease in the resistance was limited by the current compliance. When the voltage was swept back to 0 V, the device showed a lowered resistance that is referred to as HRS in the following. The HRS was retained until the voltage was increased to 1.56 V. With decreasing the voltage, a transition in the resistance to an LRS was observed. In the second consecutive sweep cycle, the LRS was observed until the voltage was decreased to -1.56 V. When the voltage was swept back to 0 V, an increase in the resistance was observed which was identical to the HRS in the first sweep cycle. The HRS switched again to the LRS at 1.56 V. The TiN-TiN device showed a bipolar RS operation after the irreversible resistance drop in the first sweep cycle. Therefore, we assume that the first resistance drop was an EF process.

The symmetry in the I-V hysteresis as well as in the switching voltages indicates the symmetric configuration in the bottom and the top interfaces. TiN requires larger energy than Ti to form an oxide as seen in Table 5.2. Therefore, the TiN could not induce oxygen vacancies in the TiO_2 . After the EF cycle, RS operation was observed in the TiN-TiN device. We assume that a large number of oxygen vacancies were generated in the TiO_2 layer since the device resistance was significantly decreased. However, a small I-V hysteresis was observed, implying only a few oxygen vacancies are able to contribute to the RS operation.

	$V_{SET}(V)$	$V_{RESET}(V)$	$V_{EF}(V)$	$SW_{@0.12V}$	$R_{@0.12V}(G\Omega)$
Al/TiO ₂ /TiN	-2.4	2.28	-2.52	12	0.4
TiN/TiO ₂ /TiN	-1.56	1.56	-4	3	1.8

Table 5.3: RS operating parameters for the Al/TiO₂/TiN (Al-TiN), and the TiN/TiO₂/TiN (TiN-TiN) devices. The V_{SET} , the V_{RESET} , the V_{EF} , the $SW_{@0.12V}$, and the $R_{@0.12V}$ are voltage at the SET process, voltage at the RESET process, voltage at the EF process, the switching window at 0.12 V, and the pristine resistance at 0.12 V, respectively.

Comparison of Al and TiN as Bottom Electrode Both Al-TiN and TiN-TiN devices required an EF process for the RS operation and exhibited bipolar RS behaviors. The parameters of RS operation of the Al-TiN and the TiN-TiN devices are compared in Table 5.3 and Figure 5.4(a) and (b). The TiN-TiN showed symmetry in the I-V relation, implying a negligible impact of an interfacial layer. The Al-TiN device showed a smaller EF voltage and a more pronounced I-V hysteresis than the TiN-TiN device. As shown in Table 5.2, Al has smaller enthalpy for oxide formation than Ti, while TiN has larger enthalpy than Ti. Therefore, we assume that the Al BE reduced TiO₂, generating oxygen vacancies in the TiO₂. Less than 0.05% change in the number of oxygen vacancies can decrease the resistivity of TiO₂ by orders of magnitude [YSM+11]. When the resistances of the two devices are compared as shown in Table 5.3, a lower resistance was observed in the pristine Al-TiN device, implying a larger amount of oxygen vacancies. Furthermore, a larger density of oxygen vacancies in the TiO₂ induces larger mobility of ions in the TiO₂ [WVS+04]. More mobile oxygen vacancies can form a bigger CF, which enhances the local electric field across the CF. Thus, selective and controlled growth of the CF could reduce the EF voltage and increases the RS hysteresis (switching window) in the Al-TiN device [SBT19].

Top Electrode

In this section, the impact of the TE on the RS operation is investigated. The relevant layer stacks of the examined devices are depicted in Figure 5.4. Firstly, the RS characteristics of an Al/TiO $_2$ /Al device are investigated. They are compared to that of the Al/TiO $_2$ /TiN device that is presented in the previous section. The two devices have the same thickness of TiO $_2$ layer (30 nm) and the Al BE (50 nm) but different TE (50 nm). In the following, the Al/TiO $_2$ /TiN and the Al/TiO $_2$ /Al devices are referred to as Al-TiN and Al-Al devices, respectively. Secondly, the RS characteristics of a TiN/TiO $_2$ /Au device are presented and compared to the TiN/TiO $_2$ /TiN device in the previous section. The TiN/TiO $_2$ /Au and the TiN/TiO $_2$ /TiN devices are referred to as TiN-Au and TiN-TiN devices, respectively.

Al as Top Electrode (Al/TiO₂/Al) On an Al-Al device, DC voltage sweep measurements were conducted, in which two consecutive cycles of measurements were performed. The sequence of the voltage sweep followed the negative-first scheme, in which current compliance was imposed. The resulting I-V curves are presented in Figure 5.4(c). In the first cycle, an abrupt resistance drop was observed at -2.52 V. A further decrease in resistance was limited by the current compliance. With increasing applied voltage, an LRS was shown, which indicates a SET process. At 1.56 V, a change in the resistance was observed. While decreasing voltage to 0 V, an increase in the resistance was observed, which indicates a transition to an HRS (*RESET process*). In the second sweep cycle, the resistance in the HRS was relatively lower than the pristine resistance of the device. A SET was observed at -2.52 V, which was limited by the current compliance. With decreasing voltage, the LRS was observed, until the RESET occurred at 1.56 V. For the voltage sweep back to 0 V, the HRS was shown. The Al-Al device showed a bipolar RS

behavior. The difference between the first cycle and the second cycle was negligible. It can be interpreted that the RS did not require an EF process. The switching window at 0.12 V was 16. Notably, the RS operation was rather asymmetric despite the symmetric device configuration. A similar RS behavior was reported by Jeong et al. [JLCK09, DKH+08]. As they observed in their Al/TiO₂/Al device, we assume that aluminum oxide was formed at the interface between the TiO₂ and the Al BE, leaving oxygen vacancies in the TiO₂ behind. Given that the I-V relation was asymmetric (see Figure 5.4(c)), the aluminum oxide layer plays an important role in the RS operation[JLRC10].

	$V_{SET}(V)$	$V_{RESET}(V)$	$V_{EF}(V)$	$RW_{@0.12V}$
Al/TiO ₂ /TiN	-2.4	2.28	-2.52	12
Al/TiO ₂ /Al	-2.52	1.56	-2.52	16

Table 5.4: Parameters of RS operations in an Al-TiN and an Al-Al device.

Comparison of Al and TiN as Top Electrode The Al-Al device and Al-TiN device had the same BE and TiO₂ layer but different TE materials. They showed similarities in the RS characteristics as shown in Table 5.4 and Figure 5.4(b) and (c). Both types of devices showed bipolar RS behaviors, almost the same EF voltages, and similar SET voltages. We assume that their similar RS behaviors were associated with the aluminum oxide layer at the Al/TiO2 interface. However, the RESET voltage was larger for the Al-TiN device than for the Al-Al device. As shown in Table 5.2, TiN has a higher work function than Al. Therefore, contact of the TiO₂ with the TiN can result in a higher Schottky barrier at the interface. The Schottky barrier at the interface assumingly reduced the internal effective electric field in the TiO₂ [YR07]. It could result in a higher voltage drop at the interface for the RESET in the Al-TiN device. However, Al TE can reduce TiO2, which might cause a change in the Schottky barrier height [KR10]. Hence, we needed to exclude a probable impact of the interfacial layer formed at the interface. To investigate the interface influence in the RS operation further, a TiN/TiO₂/Au device was fabricated, in which Au (50 nm) cannot reduce TiO2. We compared the RS characteristics of the TiN/TiO2/Au device to the TiN/TiO₂/TiN device that had TiN TE (50 nm) that hardly reduces the TiO₂. Thus, we study the impact of the TE on the RS operation concerning the work function of the electrode materials. In the following, the devices of TiN/TiO₂/TiN and TiN/TiO₂/Au types are called TiN-TiN, and TiN-Au, respectively.

Au as Top Electrode (TiN/TiO₂/Au) On a TiN-Au device, we conducted the DC voltage sweep measurements in the positive-first scheme, in which current compliance was used. The resulting I-V curves are shown in Figure 5.4(d). With increasing voltage, the current increased, which was limited by the current compliance. For decreasing voltage applied, a lowered resistance was shown. At -1 V, the current reached current compliance again. When the voltage swept back to 0 V, a more lowered resistance was observed. In the second sweep cycle, a slightly increased current was seen compared to the current in the first cycle. Still, a RESET process is not observed, similar to the first cycle. The TiN-Au device did not show RS behavior. We assume that the device had a high Schottky barrier formed at the top interface due to the high work function of the Au layer. At a negative bias, an effective internal electric field inside the TiO₂ was assumingly too small to induce resistance switching, which might hinder a RESET process.

Comparison of TiN and Au as Top Electrode: The TiN-TiN device showed symmetric I-V hysteresis after an EF process in Figure 5.4(a), which is an indication of a filamentary-type RS. However, the TiN-Au exhibited neither an EF process nor RS operation. A TiO₂ containing oxygen vacancies is

regarded as an n-type wide-band-gap semiconductor [KR10]. Therefore, contact with metals that have a higher work function than TiO_2 forms a Schottky barrier. Au has a higher work function than TiN as shown in Table 5.2. Thus, a higher Schottky barrier height could be formed at the interface in the TiN-Au device than in the TiN-TiN device. Since a high Schottky barrier height makes the electron transfer between the metal and the TiO_2 difficult, we compared the resistance of the two devices. The resistance was measured in the pristine devices at a low forward voltage at which ion currents are negligible. The resistance of $12~G\Omega$ in the TiN-Au was higher than $1.8~G\Omega$ in the TiN-TiN device. The result suggests that the impact of the Schottky barrier can be a dominant factor in I-V characteristics. However, the rectifying effect was insignificant despite the presence of the Schottky barrier in the TiN-Au device. It could result from a small asymmetry in work functions of the two electrodes [KVP+22]. If a metal oxide with a smaller electron affinity (work function) than TiO_2 such as HfO_2 is employed, the effective Schottky barrier height could be increased, which may result in rectifying behavior. This will be demonstrated in the following section 5.2.1.

Summary

We fabricated memristive devices using two metal oxides (TiO₂ and HfO₂) and several electrode configurations including Al, TiN, and Au. Comparing these devices to one another, we deduced how the materials for the MO layer, the BE, and the TE affect the RS characteristics. The Al/HfO₂/TiN device showed a TCM-type RS behavior. It implies that HfO₂ as a switching layer could lead to a large I-V hysteresis at a small switching voltage. However, the HfO₂-based device showed low reliability in the RS operation. On the contrary, the Al/TiO₂/TiN devices showed stable bipolar RS behavior. We assume that the oxygen vacancies migrate easier in the TiO₂ layer than in the HfO₂ layer due to a lower diffusion barrier, which may improve the reliability. Secondly, the impact of the BE was investigated using Al-TiN and TiN-TiN devices. The Al-TiN device showed more pronounced RS behavior. We assume that a sufficient amount of oxygen vacancies were induced due to low energy for oxide formation in the Al BE, which helped to form a stable CF in the TiO₂ layer. In the following, we studied the role of the TE in RS operations. Comparing the Al-Al and the Al-TiN devices, we found that the Al-TiN device required a higher RESET voltage than the Al-Al device. The TiN TE assumingly formed a higher Schottky barrier than Al due to a high work function. Therefore, a higher voltage was required to lower the Schottky barrier for the Al-TiN devices. Finally, the TiN-TiN and the TiN-Au devices were compared to study the impact of the TE on RS operation in detail. In those devices, inactive materials were used for all electrodes, which allowed to minimize the impact of an interfacial layer at the interfaces on the RS operation. Comparing the two types of devices, we found that employing a metal with a high work function such as Au for the TE may eliminate an EF process due to the homogeneous interface change by a high Schottky barrier. The TiN-Au device showed a possibility of an application for the interface-type RS.

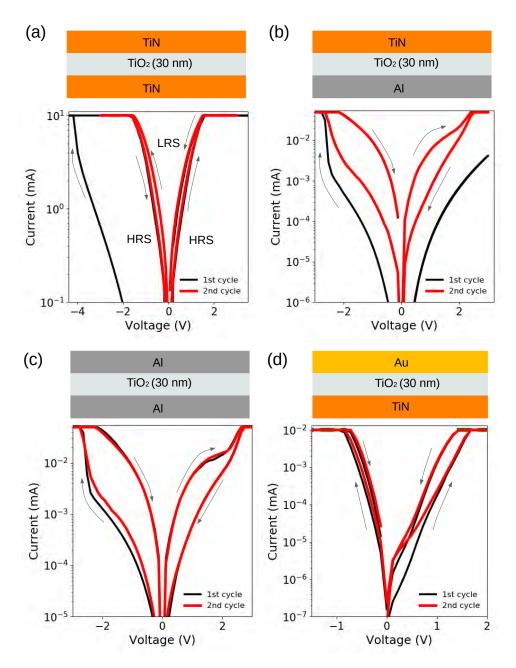


Figure 5.4: Schematics of structures of memristive devices and influence of the electrodes on the RS characteristics in (a) a TiN-TiN device, (b) an Al-TiN device, (c) an Al-Al device, and (d) a TiN-Au device.

5.2 Modulation of Oxide Properties in Bilayer Oxide System

In the previous sections (ch.5.1), TiO₂-based memristive devices showed stable filamentary-type RS operations (see VCM-type in ch.2.1), when Al was used as electrodes (see Figure 5.4(b) and (c)). We assume that an aluminum oxide (AlO_x) layer was formed at the Al/TiO₂ interface, resulting in a bilayer oxide system of AlO_x/TiO_x. In the AlO_x layer, oxygen anions could be stored. They could move back and forth between the two oxides driven by an applied electric field. In the TiO₂ layer, they form/dissolve a CF structure, resulting in RS operations. Similarly, many other researchers have reported successful RS operations by using bilayer oxide systems that consist of one oxide for the oxygen reservoir and one for the switching layer [NSS+17, PAA+16, YDZ+16]. In particular, this stack design has improved RS performance in many respects such as endurance, analog switching, retention, and so on [CMB⁺19, SKT⁺17, CHH⁺15, LCW⁺08]. However, filamentary-type devices suffer from a large variance of RS operation due to the randomness in the CF formation. This high variability challenges efficient programming and high performance in neuromorphic applications [CAA+20, KNK+20]. In terms of RS variability, interface-type devices (see VCM-type in ch.2.1) are superior due to the RS based on homogenous interfacial processes [BMBB17, GDPM+16]. To realize interface-type RS devices, a high Schottky barrier is required at the interface between the switching layer and the electrode [HZK+15]. In this regard, HfO₂ can be a better choice than TiO₂, as discussed in the previous chapter (see ch.5.1.2). For memristive devices with desired performance with low variability, a bilayer stack of TiO₂/HfO₂ can be considered. Here, the TiO₂ layer can serve as a reservoir layer due to its higher oxide formation energy than the HfO₂ layer [CYH⁺11]. The HfO₂ can serve as the main switching layer that allows for interface-type RS. As electrode materials to enable interface-type RS, three points should be considered: i) higher oxide formation energy than oxide layers, ii) high work function for a high Schottky barrier, and iii) asymmetry in Schottky barrier heights. For instance, Au and TiN have higher oxide formation energy than HfO₂ and TiO₂ layers, respectively. Therefore, the formation of oxygen vacancies can be suppressed at the interfaces, which suppresses a feasible creation of a CF. Au and TiN have high work functions, which can build high Schottky barriers at both TiN/TiO2 and HfO2/Au. Additionally, those two Schottky barrier heights are asymmetric, which could present a clear current rectification in I-V curves [JWW⁺22]. Furthermore, oxide properties such as stoichiometry, thickness, and composition are important factors to determine the RS characteristics in memristive devices [BCN+18]. Thus, investigating the impact of those factors on the RS operations can help find methods to adjust RS operations precisely.

In this section, memristive devices consisting of $TiN/TiO_x/HfO_x/Au$ are investigated. Two different types of devices are fabricated using different oxygen stoichiometry of the HfO_x layer. Here, the x in the HfO_x denotes the ratio of the O/Hf. The fabricated devices in this section have non-stoichiometric films x < 2, whereas an ideal stoichiometric oxide film has x = 2. The RS characteristics of the two different types of devices are presented, and the RS mechanisms are discussed concerning the influence of the oxygen stoichiometry in the HfO_x film. Furthermore, we systematically varied the physical parameters of the devices such as the thickness of HfO_x layers, and the device area size. The impact of those controlled physical parameters on the RS properties is analyzed using various statistical methods. The investigated RS characteristics include operating voltages, scaling of resistance with device area, and variability.

5.2.1 TiO_x-HfO_x Memristive device

Two different types of TiO_x -HfO_x bilayer memristive devices were fabricated. The relevant layer stacks are shown in Figure 5.5. Both types of devices had TiN as a bottom electrode and Au as a top electrode.

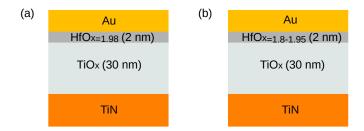


Figure 5.5: Schematics of relevant layer stacks of (a) an I-type device and (b) a F-type device

In between the electrodes, they had the same thickness of switching layers consisting of TiO_x (30 nm) and HfO_x (2 nm). However, the oxygen stoichiometry of the HfO_x was different in each type. In one type of device the stoichiometry of x=1.98 in the HfO_x was achieved by depositing the film using the rotation mode (see Influence of Substrate Rotation in ch.4.3). In the other type of devices, the HfO_x stoichiometry was x<1.95, for which the stationary mode (see ch.4.3) was used during sputtering. In the following, the former is referred to as I-type and the latter as F-type devices. The fabrication methods are detailed in ch.3.1. The detailed material properties of the TiO_x and the HfO_x are found in ch.4. In this subsection, the RS characteristics of the two different types of devices were investigated. Both types of devices had the same area sizes of the active parts of $100~\mu m^2$. The RS characteristics were examined using DC voltage sweep measurements, in which current compliance was used to prevent the devices from a hard electrical breakdown. The details of the electrical measurement methods are described in the ch.3.2.

Interface-type TiO_x-HfO_x Memristive Device

The RS characteristics of the I-type devices were investigated via DC voltage sweep measurements. Two consecutive sweep cycles were executed using the positive-first scheme (see Figure 5.2(a)). A representative I-V curve is shown in Figure 5.6(a). In the first cycle, a gradual increase in current was observed with increasing sweep voltage, which was limited by the current compliance (I_{cc}) . With decreasing sweep voltage, the resistance switched to an LRS. Notably, the current at a negative voltage was significantly smaller than at a positive voltage, indicating self-rectifying RS behavior. During the voltage sweep back to 0 V, the LRS was switched back to an HRS (RESET process). In the second consecutive sweep cycle, the resistance in the HRS was lower than the pristine resistance of the device. With increasing voltage sweep, an increase in the current was observed, but it was limited by the $I_{\rm cc}$. When the voltage was swept back to 0 V, a transition from the HRS to the LRS was observed (SET process). Afterward, a RESET process was shown at -1 V. Although a reduced resistance in the HRS was observed in the second sweep cycle compared to the pristine resistance in the first cycle, the general trend in the I-V curves was the same as in the first sweep cycle. The gradual SET and RESET processes, as well as self-rectifying behavior, resemble the RS characteristics of interface-type devices (see Figure 2.2(a) and (e)). The interface-type devices typically exhibit uniform resistivity over the entire device area [BMBB17]. Therefore, a constant R-A product, which is resistance (R) multiplied by device area (A), is obtained in the interface-type devices. In particular, a clear constant value in the R-A product is expected in the HRS, while in the LRS a linear increase in the R-A product with increasing A might be observed [PKI⁺21]. To investigate the R dependency on the A, resistance values were extracted at 1 V from the I-V curves of the I-type devices. From that, the R-A product was calculated. The median values of the R-A product are shown as a function of A in Figure 5.6(b). A constant R-A product was observed in the HRS, identifying the devices as an interface-type.

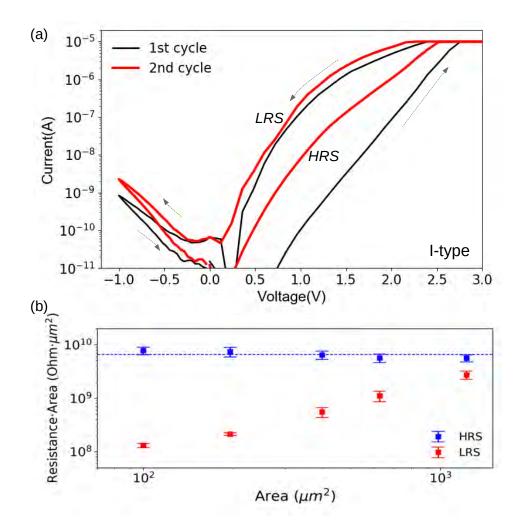


Figure 5.6: (a) I-V characteristics and (b) R-A product of the I-type devices

Filamentary type TiO_x-HfO_x Memristive Device

The RS characteristics of the F-type devices were investigated using DC voltage sweep measurements. The measurements were conducted in the positive-first scheme (see Figure 5.2(a)), in which two consecutive sweep cycles were performed with I_{cc} . A typical I-V curve is shown in Figure 5.7(a). In the first sweep cycle, high resistance of the pristine device was observed. At 2.5 V the resistance dropped abruptly, which was limited by the I_{cc} . While the voltage decreased to 0 V, a lowered resistance was observed, which is referred to as HRS in the following. At -0.7 V a change in the resistance was observed, which was limited by the I_{cc} . When the voltage was swept back to the 0 V, a more lowered resistance was shown, which implied a transition from the HRS to an LRS (*SET process*). In the consecutive sweep cycle, an increase in the resistance was observed at 1 V. With decreasing sweep voltage, the resistance switched to the HRS (*RESET process*), and at -0.7 V it switched back to the LRS.

The F-type devices showed bipolar RS behaviors (see basic terminologies in ch.2.1). The RS operations were initiated after a significant resistance drop in the first sweep cycle. Therefore, we assume that the sudden resistance drop was an EF process. An EF process and bipolar RS behaviors are often observed in a filamentary-type device (see Figure 2.2(b) and (f)). The RS behavior in the filamentary-type devices is caused by a CF that is a localized current path connecting two electrodes. Therefore, this type of device is characterized by a constant resistance irrespective of the device area. To check the relation of R and A in the F-type devices, the R at 0.1 V from the I-V curves was extracted. The R-A products as a function

of A are shown in Figure 5.7(b). A linear increase in the R-A product with increasing A was observed. The result implies the constant resistance regardless of the A in the F-type devices. Thus, we assume that the F-type devices are a filamentary-type.

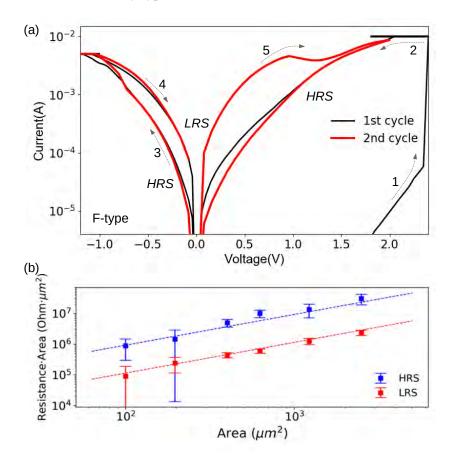


Figure 5.7: (a) I-V characteristics and (b) R-A product of the F-type devices

Comparison of the Two Types of Memristive Device

In the two types of memristive devices, the only difference was in the stoichiometry of the HfO_x layer. In the RS characteristics, two distinctions were exhibited: EF process and self-rectifying behavior. F-type devices showed a noticeable EF process as well as a constant resistance irrespective of device area. Therefore, the devices in the F-type are assumed to be filamentary-type devices. Filamentary-type devices require sufficient oxygen vacancies in the oxide layers. The number of oxygen vacancies can be deduced by the specific resistivity (ρ) of the HfO_x layer compared to the ideal HfO₂ layer. For instance, when HfO₂ contains more oxygen vacancies, a larger decrease in ρ is observed compared to the ρ of ideal HfO₂ layer of $10^{10} \,\Omega$ · m [HKM+11]. When we assume the extreme case that the only resistive part is the HfO_x layer in the F-type device, an upper limit for ρ can be deduced to $10^8 \,\Omega$ · m. The obtained ρ of the HfO_x in the F-type is still much smaller than the ideal HfO₂ layer. Thus, we assume a considerable amount of oxygen vacancies exhibited within the HfO_x layer. (Here, the resistance of the pristine F-type device was obtained at 0.2 V, at which oxygen ions can barely move due to a large activation energy for migration in the oxide layers [GSMS19, LLZ+12]. Additionally, the HfO_x thickness of 2 nm and the device area of $100 \mu m^2$ were used to obtain the ρ).

In the I-type devices, prominent self-rectifying behavior was observed as shown in Figure 5.6 (a). Additionally, a constant R-A product in the HRS supported the interface-type RS operation. In the devices,

an estimated Schottky barrier height and ideality factor of the Schottky contact was 708 meV and 3.9 for the HRS, and 615 meV and 4.45 for the LRS, respectively (see the details in [PKI+21]). During the SET process (which is the transition from the HRS to the LRS), existing oxygen ions in the HfO_x film drift toward the HfO_x/Au interface. Because of their negative charges the Schottky barrier height is reduced, which can lead to an image force adjustment [DHZ+16]. This phenomenon can be expressed as an increased ideality factor [BKK14]. By a decreased effective Schottky barrier height, a high current can flow through the device, resulting in an LRS [PKI+21]. Considering the apparent decrease in the Schottky barrier and a larger ideality factor in the LRS, a plausible scenario for the RS mechanism is the modulation of the Schottky barrier height caused by variation of oxygen ion concentration at the HfO_x/Au interface [PKI+21].

Another plausible scenario for the RS is the modulation of the Schottky barrier profile (width and height) by the charge trapping/release in the interfacial layer formed between the HfO_x and the Au [BKK14]. In this scenario, electrons in the interface trap states are injected into the electrode at positive voltages, which induces an increase in the electron affinity (χ) of the HfO_x to compensate for the loss of the electrons according to the charge neutrality. It results in the shrinking of the Schottky barrier profile, thus an LRS is established. In contrast, at negative voltages, electrons are injected into the interface states. It causes a decrease in the χ accompanied by increasing the Schottky barrier profile, resulting in an HRS. Further investigation is required using capacitance-voltage measurements, however, the modulation of the Schottky barrier height plays a major role in the RS operations.

5.2.2 Resistive Switching and Statistical Examinations

As shown above, two distinctive features were observed in the RS characteristics: EF process in the F-type devices and self-rectifying behavior in the I-type devices. We conducted statistical investigations on the two different types of devices for a more precise discussion of rectifying features and the EF process. In this subsection, the impact of physical device parameters such as the HfO_x thickness and the device area on these two features are investigated. Additionally, the variability of RS operations in each type of device is analyzed. In the analysis, several statistical measures are used such as mean, standard deviation, quantile, and cumulative distribution function. The relation between the physical device parameters and RS operation allows for precise adjustment of the RS operation. The fundamentals of used statistical measures can be found in ch.2.3.

Device Fabrication for Systematical Investigation

The two types of devices were fabricated on 4-inch wafers where around 40,000 devices with different area sizes exhibit, as shown in Figure 5.8. The I-type devices consist of a HfO_x film with x=1.98, and a thickness of 2 nm over the entire wafer. The F-type devices consist of a HfO_x film with x<1.95 and a thickness gradient of 2 nm to 8 nm. The stoichiometry and thickness of the HfO_x films and the device area size were systematically controlled, which allowed for methodical investigation of the impact of those physical parameters on the RS operation, excluding any influence that might occur during the fabrication process.

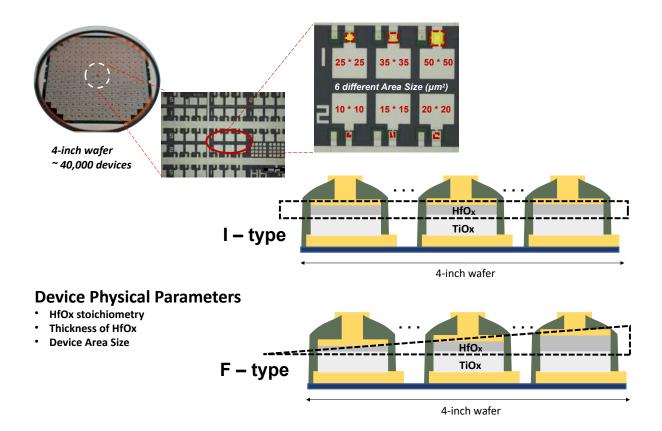


Figure 5.8: From upper left to lower right: a 4-inch wafer where around 40,000 memristive devices are situated. The devices have 6 different area sizes. Three device physical parameters including the stoichiometry and thickness of HfO_x layers and device area are varied to investigate their impacts on the RS operations. The I-type devices consist of a HfO_x film with x=1.98, and a thickness of 2 nm over the entire wafer. The F-type devices consist of a HfO_x film with x<1.95 and a thickness gradient of 2 nm to 8 nm.

Self-Rectification

State-of-the-art artificial neural networks require a large number of interconnected memristive devices [JKR⁺21, Kla18]. However, a common issue in such a massive network is the sneak-path problem [BK19, SZT⁺20]. The sneak-path is an unwanted current through the memristive network, which makes training the memristive network inefficient [FLL⁺19]. One promising solution to tackle the sneak-path problem is self-rectifying memristive devices as shown by devices in the I-type in Figure 5.6(a) [JKR⁺21, WLX⁺20, BK19].

We prepared I-type devices of five different active area sizes: $100~\mu m^2$, $196~\mu m^2$, $400~\mu m^2$, $625~\mu m^2$, and $1225~\mu m^2$. All the examined devices had a 2 nm HfO $_x$ layer. The I-V curves were obtained using DC voltage sweep measurements, in which the current values at 1 V and -1 V were extracted. Following, the rectification ratio was calculated using the equation: I_{1V}/I_{-1V} in which I_{1V} and I_{-1V} are currents at 1 V and -1 V, respectively. The results are plotted in terms of device area in Figure 5.9(a). The boxplots display the distribution of rectifying ratio including the median value marked by the red line and the average by the circle symbol (see boxplots in ch.2.3). The most pronounced rectification was observed in devices of the two smallest area sizes. The rectification ratio decreased with the increasing device area. It was because of the increased reverse current (I_{-1V}) with increasing area size, while the forward current I_{1V} is almost identical. The I_{-1V} proportional to the increasing device area or perimeter [RZD+00] can be related to defects induced during the fabrication process [KMM99]. In particular, a significant drop was observed for the area size larger than $400~\mu m^2$ (see Figure 5.9(a)). The result suggests that to employ a self-rectifying feature in the I-type devices, a device area smaller than $400~\mu m^2$ is ideal.

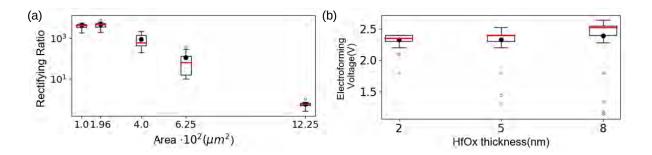


Figure 5.9: (a) Rectifying ratios in I-type devices for respective active area size. (b) EF voltages in F-type devices for respective HfO_x thickness.

Electroforming Voltage

Filamentary-type devices require an EF process to activate stable RS operations. As observed in our devices of the F-type (see Figure 5.7(a)) as well, the EF processes typically require a higher voltage than the RS operating voltages. However, demand for high voltage could limit the application of memristive devices for integrated circuits because it can damage peripheral elements on the chip [Che13]. Therefore, there have been many studies to decrease EF voltages [PSK+15, NLVE15, Che13] or completely eliminate EF cycles [YSY+14, SYM+13].

We prepared F-type devices consisting of different HfO_x thicknesses (d_{HfOx}): 2 nm, 5 nm, or 8 nm. Since the F-type devices showed a constant resistance irrespective of device areas (see in Figure 5.7(b)), the area sizes were not taken into account in the analysis. Using DC voltage sweep measurements, EF cycles were performed. Afterward, EF voltages (V_{EF}) were extracted. The distribution of V_{EF} for respective d_{HfOx} is presented in Figure 5.9(b). The V_{EF} increased proportionally with d_{HfOx} . All the devices showed

lower means than the medians, implying a skewed distribution. It is because of the outliers in the datasets. The thicker the d_{HfOx} was, the further the outliers were located from the bottom whisker. In particular, the lowest V_{EF} was observed in the d_{HfOx} of 8 nm. In AFM measurements, a rougher surface profile was found in a thicker d_{HfOx} (see ch.4.3). Increased roughness might cause an increased average electric field in the HfO_x layer, resulting in a decrease in the V_{EF} as well as the reliability of RS operations [BT15, NLVE15].

Variability in Resistive Switching Operation

Variability in memristive devices affects learning accuracy in memristive networks. High variability makes training the network challenging [CAA⁺20] and drops learning accuracy [XWY21]. Therefore, variability should be properly considered.

In the following, we show a qualitative investigation of the variability of the RS operations. First, to draw a reliable conclusion from statistical analysis, a normal distribution of the examined data is essential [KP19]. If the dataset does not show normality, the obtained statistical measures such as mean, median, and IQR (see ch.2.3) cannot represent how the system behaves. To check for normality, a distribution plot of the collected data is useful, e.g., cumulative distribution function. Afterward, variability of each device is examined. A detailed explanation regarding the distribution plot is found in ch.2.3.

Data Preparation for Statistical Analysis DC voltage sweep measurements were conducted on the I-type and F-type devices. In the measurements, ten consecutive sweep cycles were performed on each device. Afterward, resistance values were extracted at reading voltages of $V_r = 1V$, and $V_r = 0.1V$ for the I-type and F-type devices, respectively (see how to define V_r in ch.3.2). Among the resistance values extracted from ten sweep cycles in one device, the median value was chosen to represent the device resistance. It allowed taking the cycle-to-cycle variability into account in the analysis.

Cumulative Distribution Function The CDF of resistance values in HRS and LRS was plotted to assess the normality of the data. The details of CDF are explained in ch. 2.3. The CDF curves of I-type devices are shown for the respective device area in Figure 5.10(a). For all active areas, S-curves were visualized in a logarithm scale for both the HRS and the LRS, indicating a normal distribution of the examined resistance values.

The CDF curves of F-type devices are shown in Figure 5.10(b). In the plot, distributions of resistance for the three different thicknesses of HfO_x are shown. Here, the device area was not taken into account. For all thicknesses of HfO_x layers, the CDF curve followed an S-shape in a logarithm scale, implying a normal distribution in the examined resistance values.

Variability In the analysis, the logarithmic values of resistance (logR) were used as a feature to represent the RS operations since normality was found in resistance in the logarithm scale. In the CDF plots in Figure 5.10, the width of the CDF curves provided a rough hint of the variation of the examined resistance values. For a quantitative analysis of the variability of the devices, the CV was calculated using the following equation:

$$CV = \sigma/\mu \tag{5.2}$$

, in which the σ is the standard deviation and the μ is the median of the logR values. According to the equation, CV shows the spread of data relative to the μ . Therefore, comparing CV values allowed for comparing variations of the resistances that were different in several orders of magnitude. CV values of

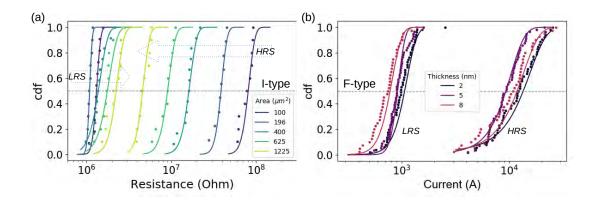


Figure 5.10: CDF curves of (a) I-type and (b) F-type devices

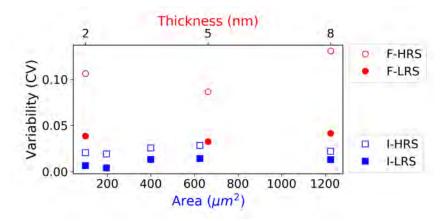


Figure 5.11: Coefficient of variation (CV) in the I-type devices for the HRS (I-HRS) and the LRS (I-LRS). CV in the F-type devices for the HRS (F-HRS) and the LRS (F-LRS).

I-type devices are shown for the respective device area in Figure 5.11. The smallest CV was found in the devices of 196 μm^2 . For the F-type devices, the CV was calculated for the respective thickness of the HfO_x layer as seen in Figure 5.11. The smallest CV was observed in HfO_x thickness of 5 nm. In general, low CV values were observed in the I-type devices compared to the CV values of F-type devices, implying low variability in the RS operations in the I-type devices.

Summary

Among I-type devices, high rectification ratios were obtained in devices that had an area size smaller than 400 μm^2 . Thus, devices of 196 μm^2 seem to be the most reasonable choice for the stack of I-type devices for efficient neuromorphic computing. However, a longer retention time is often obtained in filamentary-type devices than interface-type devices [FHD⁺16, SPWT16]. Thus, F-type devices could be more advantageous for neuromorphic applications in terms of long retention than I-type devices. Among F-type devices, devices consisting of a 5nm HfO_x layer showed the lowest variability and a moderate V_{EF} for EF processes. Therefore, devices consisting of a 5 nm thick HfO_x layer seem to be the most promising candidate for the stack of F-type devices.

5.3 Modulation of Oxygen Transport in Trilayer Oxide System

In the previous chapter, the bilayer devices consisting of TiO_x and HfO_x showed interface-type RS operations (see the VCM mechanisms in ch.2.1). The RS operation exhibited a self-rectifying feature, which allows for implementing efficient learning algorithms by suppressing sneak-path issues (see ch.2.2.2) [SZT+20, FLL+19]. Yet, the bilayer devices required external current compliance to be imposed for stable RS operations. The demand for current compliance leads to complicated circuit design for the application of memristive devices [LSS+09, MK18, TLT15]. Another challenge for the development of interface-type devices is the short retention time. This is because a concentration gradient of oxygen ions is created in the switching layers during the SET process, which makes ions diffuse back along the concentration gradient when the applied electric field is released [DHZ⁺16]. Among several methods to tackle the need for external current compliance and retention issue, inserting an AlO_x layer into the switching layers, or modifying oxygen vacancies in the oxide systems have achieved remarkable improvement [HCZ+16, JKR+21, LZC+20, CGC+13, HLL+20]. It implies that precise control of the ion motion at the nanoscale is necessary [HZK+15, WDSS09, WA10]. This includes adjustment of the respective ion types and their mobility and adjustment of local electric fields. To control the ion motion, the geometry of the switching layers, as well as the adjustment of ionic, electrical, and thermal conductivities of the material system, is critical [DHZ+16, HYY+17, HCL+16]. However, the properties of such multilayer systems differ significantly from the bulk material properties of the individual layers [HZK⁺15, ZZWA17, SKT⁺17]. This calls for a systematic approach to adjusting RS behaviors by relating the relevant technical parameters to physical processes such as ion motions and underlying interface effects.

In this section, we present the development process to tailor interface-type RS characteristics to have advantageous features for neuromorphic applications such as electroforming-free and compliance-free features, improved endurance, and long retention time (see the basic terminologies in ch.2.1). Motivated by the TiO_x/HfO_x stacks that showed interface-type effects (see ch.5.2.1), a trilayer design is designed in which an AlO_x was inserted in between the two oxides. To investigate the role of AlO_x layer as well as the TiO_x and HfO_x layers in the trilayer stack, three different multilayer stacks are designed by employing TiO_x , HfO_x , or Al_2O_3 layers. The I-V characteristics of the three different devices are investigated and the roles of each layer are deduced. In the following, we present trilayer oxide-based memristive devices consisting of a $TiO_x/AlO_x/HfO_x$ stack. The RS characteristics are investigated in terms of the requirement of current compliance and operating voltage range. The retention times are examined by controlling maximum applied voltages to the trilayer oxide-based memristive devices. Furthermore, the oxygen stoichiometry of the HfO_x layer in the trilayer oxide stack is controlled to analyze the impact of oxygen stoichiometry of the HfO_x on the RS characteristics. Lastly, to deepen the understanding of the underlying switching mechanisms, the experimental findings are described by a physics-based device model with which a numerical simulation is performed.

5.3.1 Tailoring of Resistive Switching Characteristics in Multilayer Systems

To study the impact of the material system on the RS operation, three different types of devices were fabricated: TiN/TiO_x/HfO_x/Au, TiN/TiO₂/Au, and TiN/Al/AlO_x/HfO_x/Au. All three types of devices had TiN as the bottom electrode and Au as the top electrode. However, the oxide stacks for the switching regions were differently designed, as depicted in Figure 5.12. The fabrication methods and the material properties of the used metal oxides are described in ch.3.1 and ch.4, respectively. DC voltage sweep measurements were conducted on the three types of devices. In the following, the representative I-V

characteristics of each type of device are shown. The measurement methods are detailed in ch.3.2. Based on understanding the role of each oxide layer, a trilayer oxide system is proposed as a memristive stack.

Self-rectifying Resistive Switching

In TiN/TiO_x(30 nm)/HfO_x(2 nm)/Au devices, which are referred to as TiO-HfO devices in the following, the x denotes a deviation from the ideal stoichiometry of TiO_2 or HfO_2 . For the HfO_x layer, x = 1.98 was observed (see ch.4.3). The layer stack is depicted in Figure 5.12(a). DC voltage sweep measurements were conducted on TiO-HfO devices. In the measurements, the positive-first scheme (see Figure 5.2(a)) was used and current compliance (I_{cc}) was imposed. Figure 5.12(a) shows a representative I-V curve of the TiO-HfO devices. In the I-V curve, a gradual SET process was observed at 2 V, which required I_{cc} to prevent an electrical breakdown of the device. The RESET was observed at -1 V. The TiO-HfO device showed RS operation with a pronounced self-rectifying feature. Based on the high asymmetry in the I-V curve, we assumed a high Schottky barrier formed at the HfO₂/Au interface. To validate our assumption, TiN/TiO₂(30 nm)/Au devices (so-called TiO-devices in the following) were fabricated. The TiO-devices consisted of a single TiO₂ layer as the switching layer, as shown in Figure 5.12(b). TiO₂ has a larger electron affinity than HfO₂ [LMR⁺15]. Thus, a lower Schottky barrier is formed at a TiO₂/Au interface than at a HfO₂/Au interface according to Equation 5.1. Therefore, we expected a weak asymmetry in the I-V curves of the TiO-devices. On the TiO-devices, DC voltage sweep measurements were carried out using the positive-first scheme, in which Icc was used. A representative I-V curve is shown in Figure 5.12 (b). The current increased with increasing voltage, which was limited by the I_{cc} . With decreasing voltage, a lowered resistance was shown. At -1 V, the current was limited by I_{cc}. When the voltage was swept back to 0 V, a much lower resistance was observed. In the TiO-device, current rectification was hardly observed. The result supported that the rectifying features in the TiO-HfO device were caused by a high Schottky barrier formed at the HfO_x/Au interface.

In the TiO-device, a pinched I-V loop was not observed, indicating the single TiO_2 layer fabricated here alone cannot be used for a switching layer combined with TiN and Au electrodes. Also, the results implied that the HfO_x layer plays a major role in the RS operation.

In the TiO-HfO devices, the Schottky barrier lowering and the increased ideality factors in the SET process were estimated (see the details in [PKI⁺21]). Thus, we assume that the RS mechanism is the modulation of the Schottky barrier height caused by variation of oxygen ion concentration at the interface of the HfO_x/Au (more detailed discussion for the RS mechanism is found in ch.5.2.1). The RS mechanism can be explained as the following: existing oxygen ions in the HfO_x film drift toward the HfO_x/Au interface at positive voltages, which reduces the Schottky barrier height due to their negative charges. Thus, a high current can flow through the device, resulting in an LRS [PKI⁺21]. At the negative voltages, oxygen ions move away from the interface, resulting in an HRS. Based on this scenario, numerical simulations were conducted, which showed good agreement with the experimental I-V curves, which is demonstrated in [PKI⁺21].

Compliance-free Resistive Switching

Although the TiO-HfO devices featured reproducible RS behavior and sufficient rectification to suppress the sneak path issue [LX19], they required I_{cc} during the RS operation. TiO₂ needs lower energy to generate oxygen vacancies than HfO₂ (see Table 5.1). Thus, in the TiO-HfO device, oxygen vacancies could be generated in the TiO_x layer when a sufficiently large voltage is applied. An increasing number of vacancies in the TiO_x layer reduces the formation energy for oxygen vacancies [GR14]. The decreased formation energy presumably leads to generating more oxygen vacancies in the TiO_x layer. To limit this

plausible positive feedback loop, we assume that the TiO-HfO devices needed external current compliance. To block such an accelerated generation of oxygen vacancies, the TiO2 layer can be replaced by an AlO_x layer that requires larger energy for forming oxygen vacancies than TiO₂ [JKR⁺21, GR14]. Devices consisting of TiN/Al(10 nm)/AlO_x(2nm)/HfO_x(3 nm)/ Au stack were fabricated, which are referred to as AlO-HfO devices in the following. In the AlO-HfO devices, AlO_x and HfO_x were used as the switching layers as shown in Figure 5.12(c). Here, the oxygen stoichiometry of the HfO_x layer was x = 1.98. DC voltage sweep measurements were conducted using the positive-first scheme, in which I_{cc} was turned off. Figure 5.12(c) shows a representative I-V curve of the AlO-HfO devices. A SET process was observed at 2 V, which was limited by itself without the need for I_{cc} . With decreasing sweep voltage, the resistance was in an LRS. A RESET process took place at -0.8 V, which did not need I_{cc} either. After that, the resistance of the device was in an HRS. The AlO-HfO device showed pronounced RS behavior with a self-rectifying feature. Moreover, the RS operation did not require Icc. Following, we continued the voltage sweep cycles on the AlO-HfO device. As shown in Figure 5.12(c), from the second to the fourth consecutive sweep cycle, the HRS in the device shifted toward the LRS with increasing cycle number. In the fifth sweep cycle, the device showed an electrical breakdown. Although the AlO-HfO device exhibited compliance-free behavior, it showed poor cycling endurance. With the increasing number of cycles, the resistance kept decreasing and the rectifying feature weakened. We assume oxygen vacancies were generated in the HfO_x layer by a strong voltage application. An increasing number of oxygen vacancies reduce the resistance of the HfO_x layer [HKM⁺11, KVZ⁺21]. Therefore, the electric field applied to the layer might not be sufficient to facilitate a complete RESET process [WVWH⁺21]. Also, an increased number of oxygen vacancies reduces the formation energy for oxygen vacancies in the HfO_x layer [GR14]. We assume that generated oxygen vacancies piled up within the HfO_x layer, which presumably caused the breakdown of the device. To combine the beneficial properties of stability in the TiO-HfO devices and compliance-free features in the AlO-TiO devices, a trilayer oxide stack of $TiO_x/AlO_x/HfO_x$ can be employed as switching layers.

Advantageous Electrical Features for Use in Neuromorphic Hardware

 $TiN/TiO_x(15 \text{ nm})/AlO_x(2 \text{ nm})/HfO_x(3 \text{ nm})/Au$ devices (trilayer devices) was fabricated using TiO_x , AlO_x , and HfO_x layers. The relevant layer stack is depicted in Figure 5.12(d). Here, the stack design of the AlO_x , and HfO_x were the same as the AlO-HfO devices. The thickness of TiO_x was 15 nm which was thinner than in the TiO-HfO devices. This is because the major contribution of the compliance-free feature was observed in the AlO_x/HfO_x stack design, and a thinner layer reduces the operating voltage of devices. DC voltage measurements were conducted on the trilayer devices, in which the positive-first scheme was used and I_{cc} was turned off. Figure 5.12(d) shows a representative I-V characteristic of the trilayer memristive devices for 100 consecutive sweep cycles. The RS behavior in the 100th sweep cycle was almost identical to the RS in the first sweep cycle. A SET process was observed at 2.5 V, which did not require external I_{cc} . The RESET process took place at -2 V. The trilayer device showed self-rectifying and compliance-free RS operations similar to the AlO-HfO devices. Furthermore, the cycling endurance was significantly improved compared to the AlO-HfO devices.

Based on the observation from the three different types of devices above, we conclude the role of each layer of the trilayer stack in the RS operation as the following: the HfO_x contributes to the major RS operation with a self-rectifying feature. The AlO_x serves as a diffusion barrier for oxygen ions, which allows for compliance-free behavior. By employing the TiO_x layer, the RS operation can be stabilized. In the following, the trilayer devices are further investigated.

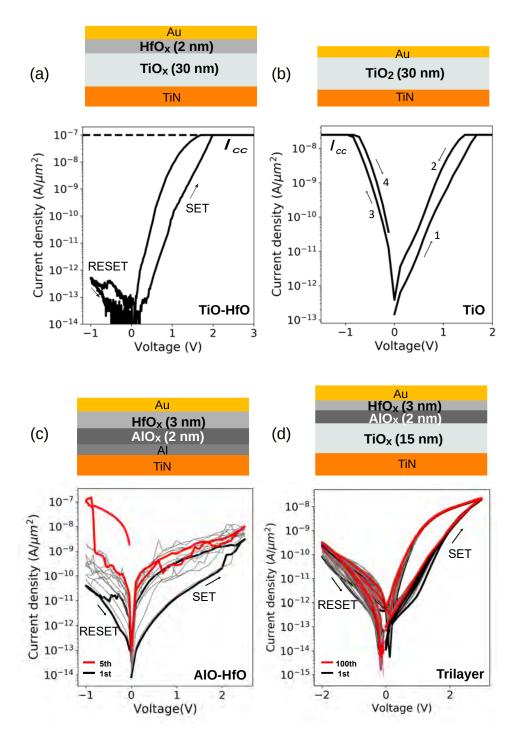


Figure 5.12: Schematics of relevant layer stacks and representative I-V characteristics of (a) TiO-devices, (b) TiO-HfO devices, (c) AlO-HfO devices, and (d) trilayer devices.

5.3.2 Incorporating AIO_x layer: TiO_x/AIO_x/HfO_x Memristive Device

Details in RS characteristics depend on the material system used in memristive devices [WWNX10, SAR+18, SJV+16, MSJ+11]. For example, the number of oxygen vacancies in HfO_x layers determines the resistivity and the chemical interaction with contacting layers. Therefore, for a precise adjustment of RS operation, the details of the material system need to be controlled. As demonstrated in the previous

section, the HfO_x layer played a major role in the RS operations. The HfO_x layer was further modified by varying the stoichiometry. Two different types of trilayer devices were fabricated, whose relevant layer stack is depicted in Figure 5.12(d). Both types of devices had TiN as the bottom electrode, Au as the top electrode, and a trilayer metal oxide of $TiO_x/AlO_x/HfO_x$ stack. However, they had two different oxygen stoichiometry in the HfO_x layers. In one type of device, the stoichiometry of x=1.98 in the HfO_x was achieved by depositing the film using the rotation mode (see ch.4.3). In the other type, the HfO_x stoichiometry was x<1.95, for which the stationary mode (see ch.4.3) was used during sputtering. In the following, the former is called H-type devices, and the latter is called L-type devices. The detailed fabrication methods are described in ch.3.1. DC voltage sweep measurements are conducted on the trilayer devices of $35\times35\mu m^2$ to investigate the RS characteristics. The investigated RS characteristics include symmetry in I-V curves, operating voltages, and resistance dependence on device areas. Furthermore, retention properties are examined using pulse measurements. Finally, the impact of the oxygen stoichiometry of the HfO_x layer on the RS characteristics is analyzed. Details of electrical measurements are described in ch.3.2.

Trilayer Device with High Oxygen Stoichiometry in HfO_x Layer

Voltage sweep measurements were conducted in two different voltage ranges. Those two ranges are referred to as "mode-low", or "mode-high", according to the relative magnitude of the maximum voltage used during electrical measurements.

DC voltage sweep measurements were conducted on an H-type device in the mode-low range. In the measurements, the positive-first scheme (see Figure 5.2(a)) was used. The resulting I-V curve is presented in Figure 5.13(a). The pristine resistance of the device was in an HRS. With increasing sweep voltage, the current increased gradually. At 2 V a slight change in the resistance was observed, which was limited by itself without using current compliance. When the voltage was swept back to 0 V, a lowered resistance was observed, which is referred to as an LRS (SET process). The LRS was retained up to -2 V. When the voltage was swept to 0 V, the resistance switched back to the HRS (RESET process). The switching voltages of the device are summarized in Table 5.5. The RS operation in the mode-low range showed gradual transition in both the SET and the RESET processes. At large voltages, rectification was observed. The rectifying ratio $(I_{@+2V}/I_{@-2V})$ at \pm 2V was 15. To investigate the RS mechanisms, the dependence of resistance on device areas was examined [BMBB17]. Resistance values were extracted at 1 V from the I-V curves. Figure 5.13(b) shows resistance as a function of device area. In the mode-low range, the resistance was scaled with the device area, implying an interface-type device.

Table 5.5: Switching voltages for the SET (V_{SET}) and the RESET (V_{SET}) processes in the H-type device. Rectifying ratio(@voltage) shows ratio of the $I_{@vol}/I_{@-vol}$ at the \pm respective voltage

The voltage sweep measurements were performed on the H-type device in the mode-high range. During the measurements, two consecutive sweep cycles were conducted. The resulting I-V curves are presented in Figure 5.13(c). In the first sweep cycle, the current increased with increasing sweep voltage. When the sweep voltage decreased, a lowered resistance was observed, which is referred to as an LRS-1 in the following. At -2 V a change in the resistance was observed. While the voltage was swept back to 0 V, an increase in the resistance was observed (*RESET process*). The resistance of the device was in an HRS, which is called HRS-1 in the following. In the consecutive sweep cycle, the resistance in the HRS-1

was lower than the resistance in the first sweep cycle. With increasing sweep voltage, a decrease of the resistance in the HRS-1 was observed at 3 V. Notably, a further decrease was limited by itself despite the absence of external current compliance. With decreasing sweep voltage, the LRS-1 was observed (*SET process*). In the following voltage sweep, the identical RESET process was observed, which implied stable RS operation. The switching voltages in the mode-high range are summarized in Table 5.5. In the mode-high range, the RS operation showed a rectifying feature at large voltages. At $\pm 4V$ the rectifying ratio was 8, which was smaller than rectification in the mode-low range. The RS behavior in the high-mode range was observed after an irreversible resistance change in the first sweep cycle. However, the resistance decreased gradually and the required voltage for the process was smaller than the RS operating voltages. It was distinctive from an EF process in filamentary-type devices (see the VCM mechanisms in ch.2.1), considering that EF processes in filamentary-type devices are abrupt and the EF voltages are typically larger than SET voltages [Was12]. To examine the RS working mechanism, resistance dependence on the active area size was investigated. Resistance values were extracted at 1 V from the I-V curves. Figure 5.2(d) shows the resistance of the devices as a function of device areas. In the mode-high range, the resistance decreased with increasing area size, implying an interface-type device.

Retention Property Retention tests were performed on the H-type devices via pulse measurements. Firstly, the resistance of devices is obtained at reading voltage pulses (V_r^p) . After that, SET voltage pulses (V_{set}^p) are applied to the devices to switch the resistance state to an LRS. In the following, the evolution of the resistance states was tracked using a series of V_r^p . The retention tests are conducted using two different V_{set}^p . Those two V_{set}^p are referred to as "mode-low" or "mode-high", according to the relative magnitude of V_{set}^p . The details of the used voltage amplitude and width of pulses are summarized in Table 5.6.

To investigate retention time, relative resistance ($R_{\rm on}/R_{\rm off}$) at $V_{\rm r}^{\rm p}$ were plotted as a function of time (t), since the resistance of devices was switched to the LRS. Here, the $R_{\rm off}$ was the firstly read resistance of the respective device. The relative resistance allowed for comparing the retention times using a common scale. The retention characteristics of the H-type devices for the respective $V_{\rm set}^{\rm p}$ and the TiO-HfO device are shown in Figure 5.13(e). The resistance of the TiO-HfO device gradually increased and reached the $R_{\rm off}$ after approximately 3 hours. However, the trilayer devices (H-type devices) showed a comparatively longer retention time. It implied the important role of the AlO_x layer in the retention time. In the retention plot in Figure 5.13(e), change in the R_{on} was slower in the mode-high $V_{\rm set}^{\rm p}$ than in the mode-low $V_{\rm set}^{\rm p}$. It indicates the device in the mode-high $V_{\rm set}^{\rm p}$ has a longer retention time than in the mode-low $V_{\rm set}^{\rm p}$. In the DC voltage sweep measurements above, the device in the mode-high range exhibited a lower resistance with weaker rectification than in the mode-low range, which implied an increased number of oxygen vacancies in the HfO_x layer. To investigate the impact of the oxygen vacancies on retention time, we fabricated trilayer devices using HfO_x layers with a modified oxygen stoichiometry.

Type	mode	$V_{\text{set}}\left(\mathbf{V}\right)$	$t_{\rm set}({ m ms})$	$V_{\rm r}({\sf V})$	$t_{\rm r}({\rm ms})$
Н	low	3.5	10	1.2	50
Н	high	5	50	1.2	50
L	low	3	10	1.2	50
L	high	-2	10	0.1	50

Table 5.6: Parameters used in pulse measurements for retention test

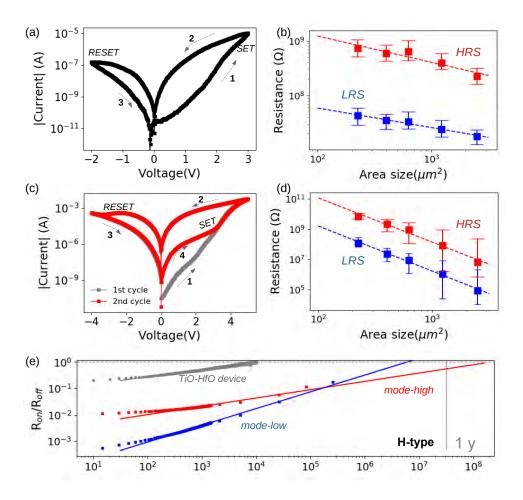


Figure 5.13: RS operations in the H-type devices in (a) the mode-low range and (c) the mode-high range. Resistance as a function of device area in the H-type devices in (b) the mode-low range and (d) the mode-high range. (e) Retention tests for the H-type devices in the mode-low $V_{\rm set}^{\rm p}$ and mode-high $V_{\rm set}^{\rm p}$, and for the TiO-HfO device. The solid lines are obtained by fitting the experimental results using the equation as follows: $R_{on}/R_{off} \propto t^{\alpha}$ (see retention property of the L-type device in the next section)

Trilayer Device with Low Oxygen Stoichiometry in HfO_x Layer

DC voltage sweep measurements were conducted on an L-type device. In the measurements, two different voltage ranges of the mode-low and the mode-high were used in the same manner as the experiments for the H-type devices.

DC voltage sweep measurements were conducted in the mode-low range using the positive-first scheme. The resulting I-V curve is presented in Figure 5.14(a). The pristine resistance of the L-type device was in an HRS. At 1.5 V a slight change in the resistance was observed. The current increased with increasing sweep voltage, which was limited by itself despite the absence of external I_{cc} . When the sweep voltage decreased, a lowered resistance was observed (*SET process*), which is referred to as an LRS. The LRS was retained until the sweep voltage reached the negative peak voltage. While the voltage was swept back to 0 V, the LRS switched to the HRS (*RESET process*). The switching voltages are summarized in Table 5.7. The L-type device exhibits RS behavior, in which both the SET and the RESET processes were gradual. At high voltages, self-rectifying behavior was observed. At $\pm 2V$ the rectifying ratio was 31. To

investigate the RS mechanisms, the resistance dependence on the device area was examined. Resistance values were extracted at 1 V from the I-V curves. Figure 5.14(b) shows the resistance decreased with increasing area size, implying an interface-type device.

Table 5.7: Switching voltages for the EF (V_{EF}) , the SET (V_{SET}) , and the RESET (V_{SET}) processes in the L-type device. Rectifying ratio (@voltage) shows ratio of the $I_{@voltage}/I_{@-voltage}$ at the \pm respective voltage.

Voltage sweep measurements were conducted in the mode-high range. During the measurements, two consecutive sweep cycles were performed. The resulting I-V curve is presented in Figure 5.14(c). In the first sweep cycle, a sudden resistance drop was observed at 3 V, which was limited by itself without using I_{cc}. A lowered resistance was observed when the voltage sweep decreased, which is called HRS-1 in the following. The HRS-1 was retained until the second resistance drop at -1.8 V. Further decrease of the resistance was not observed despite the absence of I_{cc}. While sweeping the voltage back to 0 V, the resistance was in a low resistance state (LRS-1), which indicated a SET process. In the consecutive sweep cycle, the LRS-1 was switched to the HRS-1 at 1.8 V (RESET process). The HRS-1 showed a gradual lowering of the resistance at a negative voltage. While the voltage was swept back to 0 V, the LRS-1 was observed, implying a SET process. The switching voltages are summarized in Table 5.7. In the mode-high range, sudden resistance drops were observed in the first sweep cycle, which is assumed to be an EF cycle. It was noticeable that the abrupt change was limited by itself without the need for external Icc. After the resistance drop, stable RS was activated which did not need Icc either. In particular, the RS operations in the mode-high range showed a significantly lower resistance with the absence of current rectification compared to the RS operation in the mode-low range. We assume that during the EF process, a considerable amount of oxygen vacancies were generated in the HfO_x film, and the Schottky barrier was locally disrupted. A sufficient amount of oxygen vacancies causes filamentary-type RS behavior [McK14]. One indication of the filamentary-type device is the dependence of the resistance on area size. Resistance values of the L-type device were extracted at 1 V from the I-V curves. Figure 5.14(d) presents the resistance values were fairly constant regardless of device areas, implying that the working mechanism of the L-device changed to the filamentary-type RS in the mode-high range.

Retention Property Retention tests were performed on the L-type via pulse measurements. In the measurements, two different V_{set}^p were used in the same manner as the experiments with the H-type devices. The details of the used voltage amplitude and width of pulses are summarized in Table 5.6. To investigate retention time, resistance values $(R_{\text{on}}/R_{\text{off}})$ at V_r^p were plotted as a function of time (t), since the resistance of the device was switched to the LRS. The retention characteristics of the L-type devices are shown for the respective V_{set}^p in Figure 5.14(e). In the plot, change in the R_{on} was negligible in the mode-high V_{set}^p compared to in the mode-low V_{set}^p . The result showed much improved retention in the mode-high V_{set}^p . For a quantitative evaluation of the retention characteristics the following equation was employed [MHSS14]:

$$R_{\rm on}/R_{\rm off} \propto t^{\alpha}$$
 (5.3)

, where α is a parameter characterizing the retention time. The retention times of the H-type and the L-type devices in Figure 5.13(e) and Figure 5.14(e) were fitted using this equation. Based on these fits, retention time (t_{ret}) was calculated for which the R_{on} returned to the R_{off}, i.e., R_{on}/R_{off} = 1. The values

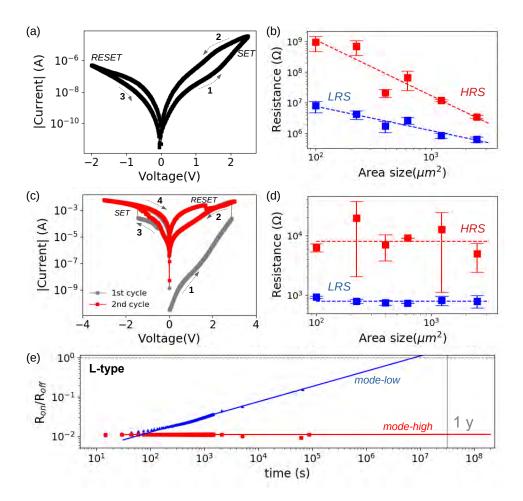


Figure 5.14: RS operations in the L-type devices in (a) the mode-low range and (c) the mode-high range. Resistance as a function of device area in the L-type devices in (b) the mode-low range and (d) the mode-high range. (e) Retention tests for the L-type devices in the mode-low $V_{\rm set}$ and mode-high $V_{\rm set}$. The solid lines are obtained by fitting the experimental results using the equation as follows: $R_{on}/R_{off} \propto t^{\alpha}$.

for the t_{ret} are summarized in Figure 5.15. The t_{ret} values of the L-type was slightly larger than the H-type devices when mode-low $V_{\rm set}^{\rm p}$ was used, showing several months of retention times. It indicates that a larger number of oxygen vacancies in the HfO_x layer could enhance the retention time. The t_{ret} value for the H-type device showed retention times in the range of about 6 years when the mode-high $V_{\rm set}^{\rm p}$ was used. These retention times are comparable to other reported interface-type devices with good retention properties [JKR+21, MFL+17, YYS+16]. In particular, a significantly long retention time was achieved in the L-type device using the mode-high $V_{\rm set}^{\rm p}$. The calculated t_{ret} was longer than 10 years, which satisfies the requirements for non-volatile memories [JT15]. The distinctively large t_{ret} compared to the other three values implies a different RS mechanism in this device. Filamentary-type devices typically show a longer retention than interface-type devices [FHD+16, SPWT16]. Filamentary-type RS operations at high voltages is further supported by the dependence of the resistance on the device area (see Figure 5.14(d)).

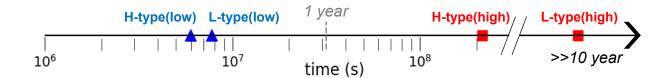


Figure 5.15: Retention time (t_{ret}) calculated by fitting for trilayer devices in the mode-low $V_{\text{set}}^{\text{p}}(\text{low})$ and mode-high $V_{\text{set}}^{\text{p}}(\text{high})$.

Switching Mechanisms in the Trilayer Memristive Device

To understand the RS mechanisms in detail, a numerical simulation was conducted. For the simulation, a physics-based device model is developed based on the experimental results.

Summary of Experimental Results A trilayer oxide stack of TiO_x/AlO_x/HfO_x was designed for memristive devices. In the trilayer stack, the HfO_x layer played a major role in the interface-type RS operation. The AlO_x layer served as an oxygen barrier to allow for compliance-free RS operation. The TiO_x layer was used as a stabilizing layer to enhance endurance. The trilayer devices (H-type) showed a tuned RS operation via the maximum applied voltage. In the mode-low range, electroforming-free and self-rectifying features, and compliance-free RS behaviors were observed. The retention time was significantly improved compared to the TiO-HfO devices. It implied that the AlO_x layer plays the important role in the improvement of the retention time. By applying a large voltage to the H-type devices, a longer retention time was observed than in the mode-low $V_{\rm set}^{\rm p}$. The obtained retention time was a comparable performance to already reported interface-type devices with good retention. We assumed that an increased number of oxygen vacancies in the HfO_x layer improved the retention time. Therefore, the Ltype devices were fabricated by modifying the oxygen stoichiometry of the HfO_x to have more oxygen vacancies than in the H-type devices. The L-type devices exhibited tuned RS operations by the maximum applied voltage as well. In the mode-low range, the RS operations featured electroforming-free and self-rectifying features, and compliance-free behavior. Moreover, enhanced retention time was observed compared to the H-type devices. It supported our assumption that a sufficient amount of oxygen vacancies in the HfO_x layer could improve the retention. In the mode-high V_{set}^p , significantly longer retention time was obtained in the L-type device. However, the device exhibited filamentary-type RS behaviors.

Physical Device Model for Trilayer Memristive Devices To study the RS mechanism in detail, a physics-based device model was developed for a numerical simulation. The main RS characteristics were associated with the HfO_x and the AlO_x layers (see ch. 5.3.1), therefore the two oxide layers were focused in the model, as shown in Figure 5.16(a). It emulates the two oxide layers by serial RC elements and a Schottky diode at the HfO_x/Au interface [PKI+21]. The overall idea of the simulation approach is as follows: mobile ions (positively charged oxygen vacancies (Vo) and negatively charged oxygen ions (O)) in the HfO_x drift driven by an applied electric field, which causes the ionic current. From this, the ohmic resistance of the HfO_x can be obtained, followed by the voltage drop across the HfO_x (V_{HfOx}). According to Kirchhoff's voltage and current laws for the circuit model, the individual voltage drop (V_S and V_{AlOx} . See Figure 5.16(a)) is calculated. In detail, the important features in the simulation are as follows: i) mobile ions of Vo and O can be described independent of each other [LTZB+19], ii) but they are connected in concentrations according to:

$$N_{Vo} \cdot N_O = N_i^2 \tag{5.4}$$

Here, the N_{Vo} , the N_O , and the N_i are concentration of Vo, concentration of O, and a layer-specific intrinsic ion concentration.

The concept of the simulation above is described with the mathematical formulas in the following. The spatial and temporal change (dx) of Vo and O in the HfO_x layer is caused by the ionic current which can be expressed as:

$$\frac{dx}{dt} = c_{drift-O} \cdot I_O + c_{drift-Vo} \cdot I_{Vo}$$
 (5.5)

Here, $c_{drift-Vo(O)}$ is drift constants of the respective ions (see equation 6 in [PKI⁺21]), which is related to the mean resistance of HfO_x layer (R_{HfO_x}). The R_{HfO_x} is expressed as:

$$R_{HfO_x} = \frac{R_{Vo}R_O}{R_{Vo} + R_O}$$
 (5.6)

The R_{HfO_x} depends on the particular channel resistances of O and Vo, which are calculated using the effective switching area and respective ion concentration (see equation 2 in [PKI⁺21]). Regarding the effective switching area, for example, for the RS caused dominantly by Vo, only the filament area is relevant. On the contrary, for the RS caused dominantly by O, the whole device area is involved in the RS operation.

The I_{Vo} and the I_O in Equation 5.5 are the ionic currents of the Vo and O, respectively, defined as the following equation [LTZB⁺19]:

$$I_{Vo(O)} = 4A_{Vo(O)}e \,\mathcal{N}_{Vo(O)}a \,\nu_0 \cdot e^{\left(-\frac{\Delta W_{Vo(O)}}{V_T}\right)} \cdot \sinh\left(\frac{a \cdot \mathcal{E}_{HfO_x}}{V_T}\right) \tag{5.7}$$

, where the $\Delta W_{Vo(O)}$ is the diffusion barrier for the respective ion species $(Vo\ o\ O)$, the a an ion hopping distance, the E_{HfOx} an electric field, the ν_0 an attempt frequency, and the V_T a thermal voltage. A_O and A_{Vo} are effective areas for interface-type and filamentary-type devices, respectively. The scenario for the ion currents is the following: for a set process with a positive bias, O is significantly involved in the RS process, while with a negative bias the Vo is attributed to the RS process.

The electronic contribution of the AlO_x is captured in the model. The electron current through metal oxide layers is modeled via [JWY⁺16]:

$$I_{el} = I_{elo} \cdot \sinh(V_{AlO_x}), \tag{5.8}$$

, where the I_{el_0} is a fit parameter and the V_{AlO_x} a voltage across the AlO_x layer.

The charge transport over the Schottky diode was modeled using the thermionic emission theory [SN06]:

$$I_S = I_R(e^{\frac{eV}{nV_T}} - 1),$$
 (5.9)

with n the ideality factor and I_R the reverse current, which is given by

$$I_R = A^* A_{Vo(O)} T^2 \cdot e^{\frac{-e\phi_B}{V_T}} \quad \text{for V} \ge 0$$
 (5.10)

$$\mathbf{I}_R = -A^* A_{Vo(O)} T^2 \cdot e^{\frac{-e\phi_B}{V_T}} e^{\frac{-e\alpha_T \sqrt{|\mathbf{V}|}}{V_T}} \quad \text{for } \mathbf{V} < 0. \tag{5.11}$$

Here, the ϕ_B is a Shottky barrier height, the A^* the effective Richardson constant, the T a local temperature, and the α_r a device-dependent parameter. The model further assumes that the RS effects influence the ϕ_B and the n:

$$\phi_B(x) = \phi_B^{LRS} \cdot \frac{x}{x_{max}} + \phi_B^{HRS} \cdot \left(1 - \frac{x}{x_{min}}\right)$$
 (5.12)

$$n(x) = n^{LRS} \cdot \frac{x}{x_{max}} + n^{HRS} \cdot \left(1 - \frac{x}{x_{min}}\right)$$
 (5.13)

the $n^{\rm HRS}$ and the $n^{\rm LRS}$ as well as the $\phi_B^{\rm HRS}$ and the $\phi_B^{\rm LRS}$ are the values for the n and ϕ_B in HRS and LRS. For normalization, the maximum x_{max} and minimum x_{min} values of the state variable (ion position) are employed. Finally, to also account for the influence of ion movement due to local temperature changes, Joule heating is incorporated (see Equation 15 in [PKI+21]). The results of the simulation model are compared with experimental I-V curves in Figure 5.16(b). The used simulation parameters are summarized in Table 5.8. The simulation results showed good agreement with experiments including all the important characteristics such as the I-V non-linearities, resistance values, and switching voltage polarities. As the result of the simulation are as follows: i) the stoichiometry of the HfO_x layer determines the N_i . A larger N_i was obtained in the L-type device than in the H-type devices. In Figure 5.16(e), the plot presents the N_{Vo} in HfO_x as a function of N_O in HfO_x for the respective device. A constant N_i is seen for both devices. According to Equation 5.4, when the N_O that involves the RS decreases, the N_{Vo} increases. However, it is noticeable that with a lower N_i , i.e. better HfO_x quality in the H-type devices, the N_{Vo} is significantly lower than in the L-type devices.; ii) interface-type RS dominates in the presence of O for the H-type device. The N_O was constant in the mode-low and mode-high ranges, which implies the same amount of O seems to contribute to the RS. However, in the experiments, a lower resistance in the HRS and ϕ_B were found in the mode-high than in the mode-low range. According to Hildebrandt et al.[HKM⁺11], the oxygen vacancies in HfO_x reduce the resistance and alter the energy band. However, those oxygen vacancies can have different charge states [CSB+14]. The charged states affect activation energy for the migration, which leads to the different mobility in the HfO_x [CBP07]. For example, neutral oxygen vacancies have significantly higher energy for the migration than positively charged Vo [CBP07]. Therefore, we assume that by a strong voltage application, oxygen vacancies with high activation energy were generated in the HfO_x in the H-type device. It resulted in a decrease not in the concentration of mobile ions but in resistance and ϕ_B .; For the L-type devices, the change from O dominant RS (interface-type) to Vo dominant (filamentary-type) was observed after the EF process. It agreed with the experimental results in resistance dependence on device area (see Figure 5.14(b, d)) and retention (see Figure 5.14(e)).

Insertion of the AlO_x layer in between HfO_x and TiO_x led to outstanding properties such as electroforming-free and self-compliance properties as well as long retention. In order to understand the influence of the AlO_x layer, we have examined the processes occurring at the HfO_x/AlO_x interface in more detail. We assume redox processes at the interface in which O is generated in AlO_x layer leaving an Vo in HfO_x behind, as sketched in Figure 5.16(c). The O flux at the interface is determined by $[HLTC^{+}18]$:

$$\frac{d\mathbf{N}_{O-AlOx}}{dt} = \frac{1}{2 \cdot e \cdot A \cdot d_{Alox}} \cdot \mathbf{I}_{ion}$$
 (5.14)

Using the Butler-Volmer equation, I_{ion} can be written as follows [BDA⁺14]:

$$I_{ion} = k_{red} \cdot e^{-\frac{2\alpha_{Alox}V_{Alox}}{V_T}} + k_{ox} \cdot e^{\frac{2(1-\alpha_{Alox})V_{Alox}}{V_T}}, \tag{5.15}$$

where k_{red} and k_{ox} are the reduction and oxidation rates given by

$$k_{red} = 2eAN_{O-AlOx}\kappa_{red} \cdot e^{\frac{-\Delta G_{red}}{V_T}}$$
(5.16)

$$k_{ox} = -2eAN_{O-HfOx}\kappa_{ox} \cdot e^{\frac{-\Delta G_{ox}}{V_T}}$$
(5.17)

Here, $G_{ox(red)}$ and $\kappa_{ox(red)}$ are the diffusion barriers and reaction rate coefficients for the respective redox process. The simulation is performed within the voltage range that corresponds to the partial voltage across the AlO_x layer during the EF process. The results obtained are summarized in Figure 5.16(d) and the parameters used are listed in Table 5.8. As shown in Figure 5.16(d), we found that for the L-type device a change in the concentrations of mobile ions is induced at around $V_{AlOx} = 0.65 \text{ V}$, whereas the H-type device did not show a change. Starting at $V_{AlOx} = 0.65 \text{ V}$, the N_{Vo} is increasing and, at the same

Table 5.8: Simulation parameters

	$\mathrm{HfO}_{1.8}$		HfO_2	
	high	low	high	low
ϕ_B^{LRS} (eV)	0.06	0.39	0.25	0.375
ϕ_B^{HRS} (eV)	0.225	0.46	0.35	0.55
n^{LRS}	8.8	8.6	16	7.0
n^{HRS}	7	7	6.4	6.4
$N_i~(\mathrm{m}^{-3})$	5.10^{23}		$5 \cdot 10^{21}$	
$N_O~(\mathrm{m}^{-3})$	$3 \cdot 10^{22}$	$1 \cdot 10^{19}$	$1.4 \cdot 10^{22}$	
$I_{el0}(\mathrm{A/m^2})$	$7.24 \cdot 10^7$	$2.8 \cdot 10^7$	1.10^{5}	
c_{back}/c_{drift}	4.10^{-12}	$1 \cdot 10^{-11}$	$0.96 \cdot 10^{-12}$	
ΔW_O (eV)	0.31		0.65	
ΔW_{Vo} (eV)	0.72		0.65	
$\mu_n (\text{m}^2/\text{Vs})$	10^{-5}	ϵ_r^{HfOx}	5.5	
ν_0 (Hz)	3.10^{11}	ϵ_r^{AlOx}	17	
R_{therm} (K/W)	$1.1 \cdot 10^4$	d_{HfOx} (nm)	3	
$T_o(\mathbf{K})$	273	d_{AlOx} (nm)	2	
a (nm)	0.4	$A_{Vo}(\mathrm{nm}^2)$	6.4	
κ_{ox} (C/s)	10^{4}	$\Delta G_{ox}\left(\mathbf{V}\right)$	1.05	
κ_{red} (C/s)	10^{4}	$\Delta G_{red}\left(\mathbf{V}\right)$	1.3	
$lpha_{AlOx}$	0.5			

time, the N_O is decreasing, satisfying the Equation 5.4 (see Figure 5.16(e)). For the L-type devices, the influence of the AlO_x on the Vo that is generated during the EF process is presented in Figure 5.16(f). In the plot, the N_{Vo} in HfO_x as a function of the inertial concentration of O in AlO_x are shown. N_{Vo} is dependent on the N_O in the AlO_x . It can be interpreted that the lower the N_O in the AlO_x is, the more likely it is to induce filamentary-type RS in the L-type device. The result shows that not only the stoichiometry of HfO_x but also the quality of the AlO_x layer plays a decisive role in the EF process.

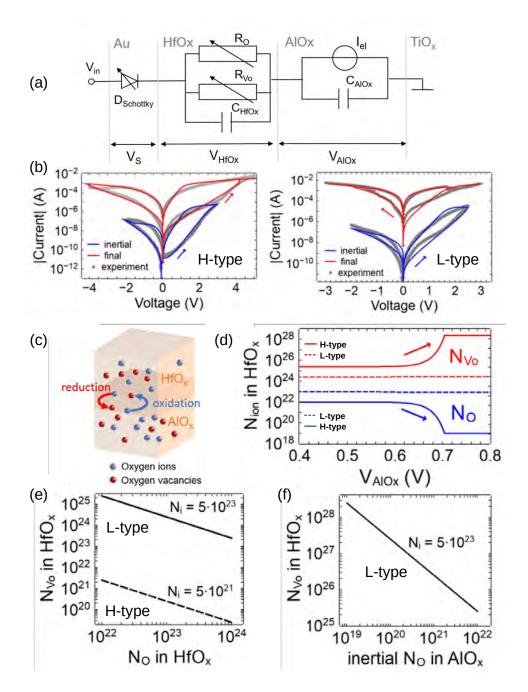


Figure 5.16: (a) Physics-based device model used in the simulation, (b) I-V curves of H-type (left) and L-type (right) from experimental and simulation results. They show good agreement. (c) Redox processes at the interface of the AlO_x and the HfO_x . (d) The concentration of mobile ions in the respective HfO_x layer as a function of the applied voltage across the AlO_x layer. L-type showed the change in the dominant ion species at around $V_{AlOx} = 0.65 \text{ V}$. (e) N_{Vo} in the HfO_x layer as a function of N_O in the HfO_x layer. The stoichiometry of HfO_x layer determines the N_i . According to $N_{Vo} \cdot N_O = N_i^2$, the concentration of one ion species determines the other. (f) N_{Vo} in HfO_x in terms of inertial N_O in AlO_x . To obtain a large enough N_{Vo} to induce an EF process, the concentration of inertial N_O in AlO_x is a decisive factor.

6 System Integration of Memristive Devices

Crossbar arrays (CRAs) consisting of memristive devices are the most promising approach for the application of neuromorphic computing in terms of density, speed, and energy efficiency [LA21, KJT⁺19, YWG⁺20]. Their advantages originate from the efficient calculation based on parallel vector-matrix multiplication which accelerates training and inference tasks [ILC⁺19]. In CRAs, the weights of the matrices used for the vector-matrix multiplication are represented by the conductance of individual memristive cells. Among CRA architectures, CRA consisting of self-rectifying memristive devices (passive CRA) [SZT⁺20, WLX⁺20] and One-transistor-one-memristor (1T1R) systems [PMBH⁺15, YWG⁺20] have drawn significant attention. Passive CRAs offer high scalability due to their simple structures, allowing for a large memory capacity [PMBH⁺15, JKR⁺21]. However, to achieve the desired performance using the passive CRAs, careful analysis and assessment of device variability are required at the system level [PAHR16]. On the other hand, the 1T1R CRAs benefit from mature fabrication technologies, programmability, and reliability [MMMCI20]. However, manufacturing 1T1R CRAs needs a sophisticated alignment between the transistors and memristive devices [MSW⁺21, JKR⁺21].

In this chapter, CRAs based on self-rectifying memristive devices are first presented. Their RS characteristics and variability are investigated with a focus on their impacts on the reliability of CRA performance. In the following, 1T1R cells are demonstrated. Important device parameters are discussed for designing 1T1R cells based on the examined RS characteristics.

6.1 Passive Crossbar Array

Memristive devices can emulate the synaptic function of human brains when they are arranged in CRAs. In the CRAs, memristive devices are massively interconnected to one another, which allows for parallel operation. However, one of the main obstacles to the development of CRAs is the sneak-path currents flowing through adjacent memory cells. A sneak path is formed by the reverse current through memristive devices, which results in an error in programming/reading. Many researchers have tackled the issue by adding a selector device to a memristive device [JCE+10, LWZ+21, CDL+19]. However, it limits the maximum scalability of the CRAs. An alternative to tackle the sneak-path issue is employing self-rectifying memristive devices in CRAs [JKR+21, LX19]. The self-rectifying features prevent the sneak-path current due to a sufficiently low reverse current. In previous ch.5.3, TiO_x/AlO_x/HfO_x-based-memristive devices presented self-rectifying RS behaviors. We fabricated CRAs using the TiO_x/AlO_x/HfO_x-based-memristive devices which are introduced in this section. Along with the self-rectifying RS behaviors, the production yield and the key device parameters for CRA reliability are investigated. Furthermore, we propose several methodologies to apply our CRAs for neuromorphic computing.

6.1.1 Resistive Switching Characteristics in TiO_x/AlO_x/HfO_x-based Crossbar Array

Based on $\text{TiO}_x/\text{AlO}_x/\text{HfO}_x$ -based-memristive devices (trilayer devices), CRAs were fabricated. As seen in Figure 6.1(a), the CRAs consist of TiN-bottom electrode lines (BL) and Au-top electrode lines (WL). The BL are placed parallel to each other in rows and the same numbers of WL are perpendicularly overlaid on top of the BL paralleling each other. At each cross point, $\text{TiO}_x/\text{AlO}_x/\text{HfO}_x$ switching layers are sandwiched in between the BL and the WL. The relevant device stacks are shown in Figure 6.1(b). Here, the oxygen stoichiometry of the HfO_x layer was x = 1.98 (see ch.4.3). The area size of the active part was $20 \times 20 \ \mu m^2$. Figure 6.1(c) shows four different sizes of crossbar arrays: 9×9 , 16×16 , 25×25 , and 32×32 . The size of the CRAs is determined by the number of electrode lines. Nearby the CRAs, test structures were placed which is visualized in Figure 6.1(c) as well. The test structures include single memristive devices with different device area sizes. In the test structures, the supply voltage was biased to only a single memristive device, while in the CRAs, the supply voltage was shared with other devices placed in the same BL or the WL. The details of the used fabrication methods are found in ch.3.2.

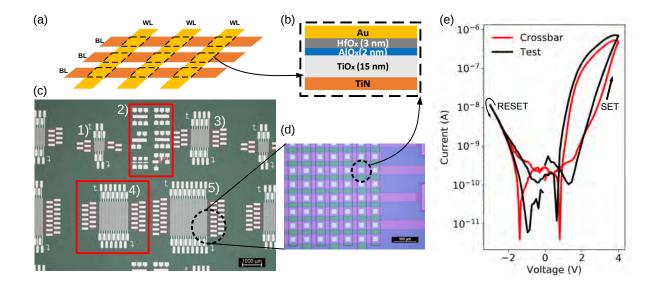


Figure 6.1: (a) A schematic of a crossbar array consisting of BLs and WLs. Memristive cells are sandwiched between the BLs and WLs at the cross points. Where memristive cells are positioned is marked with dashed lines. (b) Relevant layer stacks of $\text{TiO}_x/\text{AlO}_x/\text{HfO}_x$ based-memristive devices. (c) Optical microscope (OM) image displaying 2) test structures and CRAs with different sizes of 1) 9×9 , 3) 16×16 , 4) 25×25 , and 5) 32×32 . (d) Closed-up OM image of the CRA. A cross point where a memristive cell is placed is marked.

DC voltage sweep measurements were performed on a selected memristive cell within the CRAs. In the measurements, the positive-first scheme (see Figure 5.2(a)) was used and current compliance was turned off. During the measurements, unselected cells were left floating. A representative I-V curve of memristive cells is shown in Figure 6.1(e). At the beginning of the voltage sweep, the resistance of the memristive cell was in an HRS. The current increased with increasing sweep voltage, which was limited by itself without the need for current compliance. While the voltage decreased, a decreased resistance was observed, showing an LRS (SET process). The LRS was retained up to -2 V. In particular, the current at negative voltages was smaller than at positive voltages, indicating a pronounced self-rectifying feature.

When voltage was swept back to 0 V, the resistance was switched back to the HRS. An apparent hysteresis I-V loop points out RS operations of the memristive cells in the CRAs. The RS behaviors showed electroforming-free features, gradual switching operations, and self-rectifying features. In the memristive CRAs, a bias scheme can be used to suppress the sneak current [Che15, KZL14, KKC15]. For instance, Jeon et al. [JKR⁺21] demonstrated the so-called one-third biasing scheme in their passive CRAs. In this biasing scheme, the switching voltage is applied to a selected cell, while its negative one-third voltage to unselected cells. Their passive CRAs successfully suppressed the sneak-path current using this biasing scheme in 320 x 320 CRA. In their CRAs, a large selectivity of $\sim 10^4~(I_{@setV}/I_{@-1/3\cdot setV})$ was obtained, thanks to the rectifying features in the CRAs. When this biasing scheme is applied to our memristive CRAs, a selectivity of $\sim 10^3$ can be obtained. It is approximately one order magnitude lower than the passive CRAs reported by Jeon et al. [JKR⁺21]. The smaller selectivity might limit realizing passive CRAs as large as a 320 x 320 CRA since a higher selectivity can eliminate the sneakpath current better [SZT⁺20]. However, it is worth mentioning that our CRAs were fabricated using sputtering techniques, while the CRAs with the selectivity of $\sim 10^4$ were fabricated using atomic layer deposition (ALD) [JKR⁺21]. Sputtering technologies have advantages compared to ALD technologies in terms of cost-effectiveness, a high deposition rate, and a scalable process [GK20]. Moreover, simple metal oxide compounds in our trilayer devices (TiO_x, AlO_x, and HfO_x) offer replicability as well as flexibility in tailoring the oxygen stoichiometry of metal oxide layers. For example, in the previous ch.5.2.1, the concentration of oxygen vacancies (N_{Vo}) in the HfO_x layer affected the current rectification features in the RS operations by either reducing the Schottky barrier height [TLL+09] or the depletion layer width [EKGVJ09] at the HfO_x/Au interface. Also, the N_{Vo} in the HfO_x is influenced by the quality of the AlO_x (see Figure 5.16(f)). Thus, if the N_{Vo} in the HfO_x layer or AlO_x quality is further optimized in our trilayer devices, an improved selectivity can be achieved. Therefore, building passive CRAs using our trilayer devices is a promising approach for practical applications.

DC voltage sweep measurements were conducted on single memristive devices in the test structure. In the measurements, the positive-first scheme was used, and current compliance was turned off. A representative I-V curve is shown in Figure 6.1(e). A gradual SET was observed at 4 V, in which an increase in the current was limited by itself without using external current compliance. At negative voltages, current rectification was observed. A RESET process occurred at -2 V, which was also a gradual transition. The RS characteristics were almost identical to the memristive cells in the CRAs. It means that parasitic effects of interconnects in the CRAs such as parasitic capacitance, inductance, and resistance are negligible [CL11, TMC+21, FEK17]. Therefore, it allows for extrapolating electrical properties of the single devices for predicting the RA behaviors of memristive cells in the CRAs.

6.1.2 Key Reliability Concerns

Desired performance of memristive CRAs is ensured by the reliable operation of the memristive devices in CRAs. Important factors to assess reliability include endurance, retention, and variability of memristive devices [AR+16]. Endurance is the number of cycles that memristive devices can reversibly switch. Therefore, endurance determines the number of training iterations [ZGT+20, ZCIL17]. Retention is the time until a programmed conductance value (weight) is maintained in memristive devices. Devices with poor retention lead to weight drift on CRAs, which impacts computation results [Yu22]. Variability in CRAs introduces errors in implementing vector-matrix multiplication. High variability makes training the CRAs challenging [CAA+20, KNK+20] and drops learning accuracy [XWY21]. Therefore, those three factors should be properly analyzed and assessed when designing training procedures for neuromorphic computing applications [ZGT+20].

Endurance

Endurance of the trilayer devices was examined using single devices in the test structure. For endurance tests, DC voltage sweep measurements were conducted with 10³ consecutive sweep cycles, in which current compliance was not used. Resistance values for the LRS and the HRS were extracted at 1.5 V accordingly from the I-V curves and plotted as a function of cycle number. As shown in Figure 6.2(a), the switching window, which is the ratio between the resistances in the HRS and the LRS $(R_{\rm HRS}/R_{\rm LRS})$, was larger than 10^2 within the first 600 cycles, after which an endurance degradation was observed. However, a clear switching window was maintained for at least up to 10^3 sweep cycles. An endurance requirement for training tasks is $> 10^6$, however, it should be noted that this requirement is applied to typical binary memory devices [CY18]. For analog memory devices, the requirement for endurance is a bit relaxed, because the conductance only changes incrementally instead of the full dynamic range in each iteration $[ZYX^{+}19]$. For instance, Gao et al. $[GWC^{+}15]$ demonstrated successful programming cycles of 10^3 for training using their analog memristive devices. This implies that our CRAs can be applied to neuromorphic computing. Moreover, reliability issues in CRAs caused by limited endurance can be further overcome at a system level by using adaptive reconfiguration methodologies [AR+16]. It is a method to allocate redundant local CRAs inside a global CRA. In this configuration, when one memristive device in a local CRA fails, the system can replace the failed memristive device with a spare one in the global CRA. Our trilayer CRAs showed a high production yield (see Figure 6.3(a, b)). Therefore, this design methodology seems to be a feasible approach for our CRAs to implement neuromorphic computing.

Retention

Retention time of the trilayer devices was examined on single devices in the test structure via pulse measurements. In the retention tests, firstly the resistance of devices was obtained with reading pulses (V_r^p) . After that, SET pulses $(V_{\rm set}^p)$ were applied to switch the resistance state to an LRS. Following, the evolution of the resistance states was tracked using a series of V_r^p . The details of the used amplitudes and widths of pulses are summarized in Table 6.1. To investigate retention time, relative resistance values (R_{on}/R_{off}) at V_r^p were plotted as a function of time (t) since the resistance of devices was switched to the LRS. Here, the R_{off} was the initially read resistance of the respective device. Figure 6.2(b) shows two different retention times when using different switching pulse widths (t_w) . When t_w was 50 ms, the LRS switched back to the R_{off} within 10^4 s. However, increasing t_w to 1 s, the LRS was retained within 10% range up to 7×10^3 s. The result proposed that a longer t_w can enhance the retention time. The retention time of $\sim10^4$ at $t_w=1$ s is a comparable range to other reported rectifying memristive devices $[JKR^+21, MFL^+17, YYS^+16]$. It showed a possibility to apply our CRAs for neuromorphic computing. For example, Jeon et al. $[JKR^+21]$ demonstrated successful acceleration of vector-matrix multiplication (see the definition ch.2.2) using CRAs that showed retention of $\sim10^4$ s.

Table 6.1: Pulse parameters used for retention tests

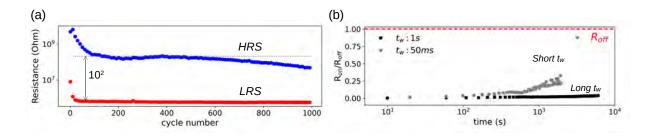


Figure 6.2: (a) Endurance tests with 10^3 consecutive sweep cycles. (b) Retention tests modulating switching pulse widths

Variability of Memristive Characteristics

We assess the variability of resistance states and the programming nonlinearity of conductance states in the trilayer device-based-CRAs. Furthermore, we provide compensation approaches that can be adopted to reduce the impact of variability for practical applications with the CRAs.

Vairability in Resistance States: Device-to-device variability in a 25×25 CRA was investigated which is marked in Figure 6.1(c) - 4). All memristive cells in the CRA were fully addressable. DC voltage sweep measurements were conducted on a single selected cell, while the other unchosen cells were left floating. From the measurements, resistance values at a reading voltage of 1.5 V were extracted for the HRS and the LRS, accordingly. Figure 6.3(a) and (b) shows the distribution of resistance values in heatmaps for the HRS and the LRS, respectively. Each small block in the heatmaps stands for a memristive cell in the CRA, and the color of the block represents the resistance values. Among 625 memristive cells, only one memristive cell was electrically-shorted, indicating a high production yield. The resistances in the HRS presented similar colors to each other (see Figure 6.3(a)), whereas the resistances in the LRS a broad range of colors. It means lower variability in the HRS than in the LRS. For a quantitative investigation, the distribution of the resistance values was visualized using a histogram, as shown in Figure 6.3(c). Here, the resistance of the electrically-shorted cell was excluded. Two distinguishable resistance states of the HRS and the LRS were observed without overlap. It is a desirable feature for applications of neuromorphic hardware since substantial overlaps between different resistance states challenge precise computing operation [PLJJD⁺20, PAI21]. In Figure 6.3(c), the resistance in the HRS showed high uniformity, featuring an average resistance of $1.8 \cdot 10^9 \Omega$. However, in the LRS two distinct states were observed at $10^7 \Omega$ and $5 \cdot 10^7 \Omega$. The resistance state close to the HRS appears to be caused by not-fully-switched resistances from the HRS to the LRS. The spread in the resistance values in the LRS can be adjusted by the programming (switching) pulses algorithm if memristive devices exhibit analog characteristics (validated below). For instance, after each programming pulse, the resistance is verified until it has reached the target value [PAI21].

Variability in Conductance Update: A linear trend in conductance linearity (CL) is an indication of analog switching. It allows for efficient programming of the memory cells because analog behaviors enable linear adjustment of conductance by modulating programming pulses proportionally [JC22]. However, variability of obtained conductance updates can impact the learning accuracy of the CRAs [LBL+18]. Thus, we investigated the probable deviation of obtained new conductance values. By being aware of device variations, an estimated penalty of variations can be introduced to training proce-

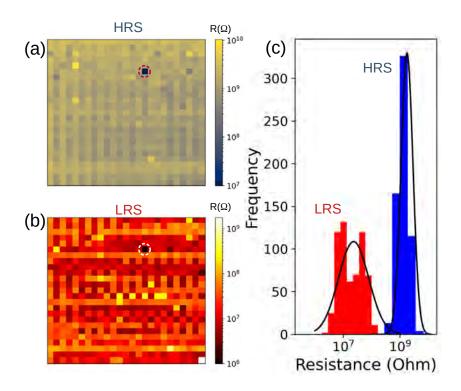


Figure 6.3: Distribution of resistance values in heatmaps for (a) the HRS and (b) the LRS. The electrically-shorted cell is marked with dashed line. (c) Distribution of resistance values in a histogram

dures [LLC+15].

CL was investigated via pulse measurements on the 25×25 CRA that was examined for device-to-device variability above. A series of 20 $V_{\text{set}}^{\text{p}}$ of 4 V and subsequent 20 RESET voltage pulses ($V_{\text{reset}}^{\text{p}}$) of -3 V were applied on 624 memristive cells in the CRA. Here, the electrically-shorted cell was excluded. Pulse widths were 5 ms for both the $V_{\rm set}^{\rm p}$ and the $V_{\rm reset}^{\rm p}$. The median values of the conductance values were calculated for the respective pulse number (pulse count). The median conductance values are presented as a function of pulse count in Figure 6.5(a). The dispersion of the conductance values is also marked using the IQR (see the definition in ch.2.3). During the SET, conductance increased non-linearly to the first four V_{set}^p . After that, a gradual increase in the conductance was observed with additional V_{set}^p . The dispersion of the conductance values increased with increasing number of V_{set}^p . When the number of V_{set}^p is increased, space charges are accumulated in the vicinity of electrodes, which can increase the electric field strength within the device [CJP95, LZMC16]. In memristive devices, RS behaviors are caused by the migration of oxygen ions driven by an applied electric field. Since the migration of oxygen ions depends exponentially on the electric field [Was12], an increased electric field within memristive devices might cause a larger variation in conductance. In pulse measurements, charge accumulation can be mitigated by tuning timing characteristics of programming pulse signals such as pulse width and pulse period [LZMC16].

The first $V_{\rm reset}^{\rm p}$ triggered an abrupt conductance drop as seen in Figure 6.5(a). In the RESET process, the conductance was significantly smaller than the conductance in the LRS. Therefore, we separated the SET and the RESET processes to investigate in more detail as shown in Figure 6.5(b) and (c), respectively. In Figure 6.5(c), the RESET showed a clear non-linear behavior to the fourth $V_{\rm reset}^{\rm p}$. After that, an improved linear trend was observed in the conductance change compared to the previous $V_{\rm reset}^{\rm p}$ signals. However, the spread of the conductance at each pulse count was significant, showing overlaps between all different conductance states. Therefore, it seems difficult to realize an analog switching without overlapped states

by using these pulse parameters ($V_{\rm reset}^{\rm p}$:-3 V, 50 ms). The problem of overlapping conductance states can be solved by reducing the highly nonlinear conductance drop at the first $V_{\rm reset}^{\rm p}$. As demonstrated in ch.7.2, a highly nonlinear conductance change can be tuned by incorporating the opposite polarity of pulse with a smaller voltage.

In Figure 6.5(b), the SET process presented a possibility for an analog switching with fairly separable states. Thus, we investigated in detail the CL in the SET process. The examined range was from the 4th V_{reset}^p to the 20th V_{reset}^p , in which a linear trend was observed as shown in Figure 6.5(a). We defined a nonlinearity factor (NLF) that is the ratio of the conductance increment at half the number of pulses (ΔG_1) to that at the total number of pulses (ΔG_2) as the following equation:

$$NLF = \frac{\left(\frac{\Delta G_1}{\Delta x_1}\right)}{\left(\frac{\Delta G_2}{\Delta x_2}\right)} \tag{6.1}$$

Here, the Δx_1 and the Δx_2 are the numbers of applied pulse signals which are 9 for both. Figure 6.4(a) shows the method to calculate NLF. According to Equation 6.1, a value close to 1 will indicate a linear conductance update. We calculated the NLFs of the 624 memristive cells in the CRA. The distribution of the NLFs is presented using a histogram in Figure 6.4(b). The median value was observed at the NLF of 1.02, implying a uniform and linear conductance update.

6.1.3 Summary

Based on $TiO_x/AlO_x/HfO_x$ -based-memristive devices (trilayer devices), CRAs were fabricated. They demonstrated advantageous electrical features for use in neuromorphic hardware, such as electroforming-free and compliance-free switching. Furthermore, the self-rectifying allows suppressing the sneak-path problems in crossbar structures. The device reliability (endurance, retention, and variability) was investigated to assess the possibility of applying the CRAs to neuromorphic applications. The endurance of $>10^3$ and the retention time of $\sim 10^4$ s provide sufficient performance to implement neuromorphic computing, compared to other CRAs that demonstrated successful results. Additionally, a high production yield, distinct two resistance states without overlap, and analog switching of the CRAs showed potential in neuromorphic computing applications.

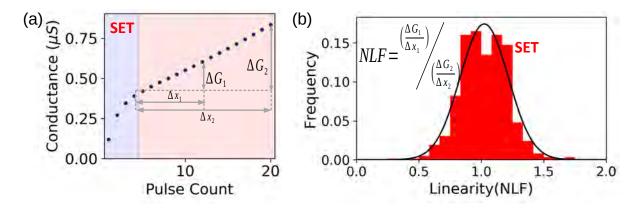


Figure 6.4: (a) Method to calculate NLF in the linear regime (see Figure 6.5(a)). (b) Distribution of NLF from 624 memristive cells in a CRA

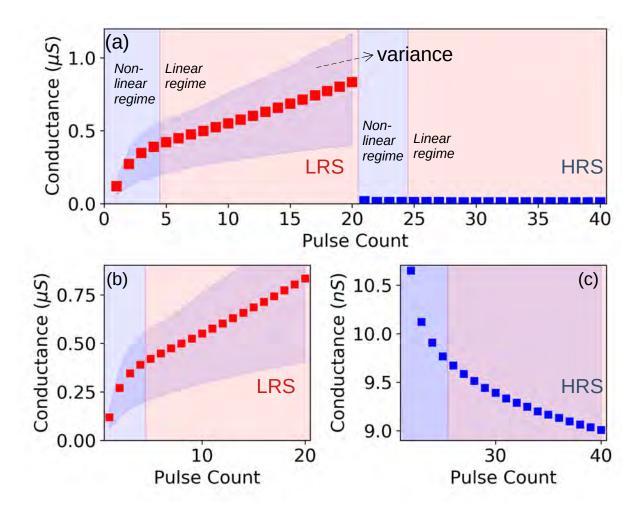


Figure 6.5: (a) Median conductance values from 624 memristive cells obtained in CL tests. Spread (variance) of conductance values at each pulse count is filled with gray color. Conductance increased non-linearly to the first four $V_{\rm set}^{\rm p}$ (Non-linear regime). After that, a gradual increase in the conductance was observed with additional $V_{\rm set}^{\rm p}$ (Linear regime). Closed-up median conductance values (b) in the LRS and (c) in the HRS. In the HRS, the spread of the conductance at each pulse count was significant, showing overlaps between all different conductance states.

6.2 Active Crossbar Array: TiO_x-HfO_x-based Memristive Device Connected to N-type Transistor

Most successful applications of memristive devices into crossbar arrays have been demonstrated in a one-transistor-one-memristor (1T1R) architecture [PMBH+15, HGL+18, LBL+18, LLW+20]. In a 1T1R crossbar array, a memristive device is connected to a transistor in series, which allows for addressing a single memristive cell. They have shown logic programming of memristive devices as well as improved reliability by minimizing the sneak path problems [XRC+09, ACL+16, MMMCI20]. However, several issues should be considered when designing 1T1R cells, i.e. selecting a type of transistors (n- or p-type), selecting a type of memristive devices (uni- or bipolar RS), and aligning the operating voltages/currents between transistors and memristive devices. [MSW+21].

In this section, 1T1R memory cells are presented, in which n-type transistors (IHP GmbH, Frankfurt Oder) and memristive devices consisting of $TiN/TiO_x/HfO_x/Au$ are connected. Here, the ratio of Hf/O in the HfO_x layer was x=1.98 (see ch.4.3). Fabrication methods for the memristive devices are described in ch.3. Firstly, the electrical properties of the transistors and the memristive devices are individually investigated via DC voltage sweep measurements. In the following, RS operations in the 1T1R cells are introduced. Based on the experimental observations, important device parameters for designing 1T1R cells are discussed.

6.2.1 Basic Electrical Properties of Components in Active Crossbar Array

Before investigating the 1T1R cells, the individual components of transistors (IHP GmbH, Frankfurt Oder) and memristive devices were examined. After the transistors were fabricated on a Si wafer (IHP GmbH, Frankfurt Oder), memristive devices were placed on top of the transistors as shown in Figure 6.6(a). Several single transistors were on the same substrate to check the electrical characteristics. Single memristive devices were fabricated on a different Si wafer using the same fabrication procedures as the memristive devices in the 1T1R cells. Details of fabrication methods for memristive devices are found in ch.3.

N-type Metal-Oxide-Semiconductor Field-Effect Transistor

Electrical properties of n-type metal-oxide-semiconductor field-effect transistors (MOSFET), which are called transistors in the following, were examined via DC voltage sweep measurements. To obtain the output characteristics, voltage ($V_{\rm DS}$) was applied between the drain and the source of the transistors, in which the $V_{\rm DS}$ was swept from 0 to 2 V. During a sweep cycle, the gate voltage ($V_{\rm GS}$) was fixed at a certain value (0 V to 2 V), while the source and the body were grounded. Figure 6.6(d) shows a representative output characteristics of a transistor, in which the output currents were plotted as a function of $V_{\rm DS}$ for the respective $V_{\rm GS}$. At $V_{\rm GS}$ =1 V, current did not flow even with an increase in $V_{\rm DS}(off\text{-state})$. In the off-state, the leakage current was approximately 1 μA . When $V_{\rm GS}$ exceeded 1 V, the output current initially increased with an increase of $V_{\rm DS}(on\text{-state})$. A complete saturation in current was not observed for all output curves, but a clear bias point was seen where the transistor entered a saturation region. The larger the $V_{\rm GS}$, the larger the saturation current (at $V_{\rm DS}$ =2 V) was observed. The pinch-off voltage, after which the transistor goes into the saturation region, was approximately 1 V at $V_{\rm GS}$ = 2V at which the current was 35 μA . The transistor went to an electrical breakdown at $V_{\rm GS}$ =4 V. On-resistance ($R_{\rm on}$) of

the transistor was estimated in the linear regime of the output curves, as marked in Figure 6.6(d). At $V_{\rm GS}$ = 2 V, an $R_{\rm on}$ of 14 $k\Omega$ was obtained.

Figure 6.6(e) shows the transfer characteristics of the transistor, in which saturation currents at $V_{\rm DS}$ = 2V were plotted as a function of $V_{\rm GS}$. At $V_{\rm GS}$ smaller than 1V, the transistor was in off-state. At the $V_{\rm GS}$ larger than 1 V, the transistor was turned on.

TiO₂-HfO_x-based-Memristive Devices

Electrical properties of TiO_x -HfO_x-based-memristive devices of $100~\mu m^2$ were investigated via DC voltage sweep measurements. In the measurements, the positive-first scheme (see Figure 5.2(a)) was used while imposing the current compliance of $10~\mu A$. From the measurements, the median current values at respective voltage were calculated from 10 different devices. It allowed for analyzing the RS operations taking the device variability into account. The median RS behavior of the memristive devices is presented in Figure 6.6(f). The resistance of the pristine device was in a HRS. Current increased with increasing sweep voltage, which was limited by the current compliance at 2 V. While the voltage decreased, the resistance was in a LRS (SET process). The LRS was retained up to -1 V. When the voltage was swept back to 0 V, the HRS was observed, implying a RESET process. Additionally, the current was significantly smaller at negative voltages than at positive voltages, indicating self-rectifying behavior. The resistance in the HRS was 1 MOhm, and in the LRS 0.1 GOhm at 1 V. Details of the RS mechanisms are described in ch.5.2.1.

6.2.2 One-Transistor-One-Memristor Cells

Schematics of a 1T1R cell are depicted in Figure 6.6(c). The 1T1R cell consists of a TiO_x -HfO_x-based-memristive device of 144 μm^2 and an n-type MOSFET (IHP GmbH, Frankfurt Oder). In the following, the former is referred to as M, and the latter as T. The TiN bottom electrode of the M was connected to the drain of the T. DC voltage sweep measurements were conducted on the 1T1R cell. In the 1T1R cells, RS operations of the M are supposed to take place, once the T is in the on-state. Thus, voltages were applied to the source of the T, while the top electrode of the M was grounded. The applied V_G of 2 V was chosen to turn on the T. During the measurements, the positive-first scheme (see Figure 5.2(a)) was used and current compliance was imposed to prevent an electrical breakdown of the 1T1R cell. Three different sweep measurements were performed, in which the sweep voltages and current compliance were varied. The used operating parameters for the measurements are summarized in Table 6.2.

Sequence	minimum sweep voltage (V)	maximum sweep voltage (v)	current compliance (A)
1	-2	4	5e-5
2	-2.5	7	5e-5
3	-2.5	10	1e-4

Table 6.2: Operating parameters in DC voltage sweep measurements on the 1T1R cell

Firstly, the current increased linearly when increasing the sweep voltage from 0 V to 1 V, as seen in Figure 6.7(a). At a voltage larger than 1 V, a saturation of the T was observed. With decreasing voltage, hysteresis in the Current-Voltage (I-V) curve was not observed. In other words, the RS operation was hardly recognizable. The pinch-off voltage was 1 V, which was almost identical to the single transistor (see Figure 6.6(d)). It implies that the majority of the voltage dropped over the T. Therefore, we assume

that the R_{on} of the T is larger than the resistance of the M.

In Figure 6.7(b) (see sweep sequence 2), a saturation region was shown, once the voltage exceeded 1V. The current rapidly increased at a voltage larger than 5 V, and it reached the current compliance (I_{cc}) at 7 V. When the voltage decreased, a lowered current was observed, showing a hysteresis loop in the I-V curve (see Figure 6.7(c)). It indicates that there was a RESET process at a voltage between 5 V and 7 V. The resistance of the M seemed to be already in a LRS before the voltage sweep was performed.

As seen in Figure 6.7(b) and (c), the pinch-off voltage of 1 V was observed, which was almost identical to the single transistor (see Figure 6.6(d)). We assume the majority of the voltage dropped over the T due to a larger $R_{\rm on}$ of the T than the resistance of the M. The RESET in the M required a voltage larger than 5 V. Considering that the RESET voltage of a single memristive device required 1 V as seen in Figure 6.6(f) (because of the reversed direction of the voltage application in the 1T1R cell), the resistance of the M ($R_{\rm M}$) was estimated. The T and the M were connected in series in the 1T1R cell. Thus, an applied voltage was distributed over two components according to the relative magnitude of the resistance. Given the $R_{\rm on}$ of the T was 14 $k\Omega$, the $R_{\rm M}$ is estimated to be 3.5 $k\Omega$, according to Ohm's law. The $R_{\rm M}$ was significantly smaller than the resistance of the single memristive device ($R_{\rm single}$). The $R_{\rm single}$ was 1 $M\Omega$ in the LRS (see Figure 6.6(f)) when the $I_{\rm cc}$ of 10 μA was used. However, the saturation current in the T was larger than 10 μA . It means larger $I_{\rm cc}$ was imposed on the M in the 1T1R cell. A level of current compliance determines the resistance of the memristive devices, as shown in Figure 6.6(g). Thus, we assume that a larger $I_{\rm cc}$ in the 1T1R cell led to a lower $R_{\rm M}$ than the $R_{\rm single}$.

In Figure 6.7(b), the current at negative voltages increased rapidly and reached the current compliance practically immediately. When negative voltages are applied to the source of the T, the depletion regions of the source-body and the drain-body junctions can form a single depletion region deeper in the body. It leads to a leakage current path (punch-through current) [BK⁺17, RT14]. We assume that this leakage current was much higher than the current flow through the M. Thus, it was difficult to trigger or observe a SET process.

The sweep voltage and current compliance were extended to trigger a SET process (see sequence 3 in table 6.2). In Figure 6.7(c), current increased linearly at low voltages. The pinch-off was observed at approximately 1.6 V. At 5 V a rapid increase in the current was observed. With decreasing sweep voltage, a lowered current was observed, which implied a RESET process in the M (see Figure 6.7(c)). At negative voltages, we could not observe any indication of RS behavior. When comparing the I-V curves of sweep sequence 2 and 3, i) a clear overlap in the current between the two sweep cycles was observed at positive voltages. It implies the resistance written in the M during the 2nd cycle (sweep sequence 2) was maintained until the 3rd cycle (sweep sequence 3).; ii) The pinch-off voltage in the 3rd cycle was larger than that in the 2nd sweep cycle (see Figure 6.7(c)). By applying a larger voltage in the 3rd cycle, the resistance was increased compared to that in the 2nd cycle. We assume the increased resistance in the 3rd cycle led to a larger voltage drop over the M.; iii) However, a SET process was not observed despite larger current compliance being imposed for negative voltages.

Challenges in the 1T1R cells and Methodologies to tackle

Issues that we faced in the 1T1R cell were 1) difficulty in checking the operating parameters and whether the individual components in the 1T1R cell operate correctly, 2) different operating voltage/current of the two electronic components, and 3) high leakage current in the T at negative voltages. In the following, we discuss the three issues in detail. Furthermore, decisive device parameters for designing 1T1R cells are introduced that can be useful when designing 1T1R cells.

1) In the electrical measurements, we only observed the conjugated electric properties of the 1T1R cells. Thus, it was difficult to understand the origin of the obtained electric characteristics of the 1T1R cells.

6.2 Active Crossbar Array: TiO_x-HfO_x-based Memristive Device Connected to N-type Transistor

Test devices for the transistors and the memristive devices should be included on the same substrate where the 1T1R cells are fabricated. Also, separate electrode lines can be added to the individual components in order to identify their operating parameters and whether the individual electronic components are operated as desired. It allows for investigating production yield and understanding the electrical characteristics of the 1T1R cells in detail.

2) **Voltage Application:** High leakage current was observed at negative voltages in the 1T1R cells. Therefore, a change in voltage polarity should be executed by changing the electrodes to which voltage is applied [CZL+20]. The single memristive devices are switched on (SET process) at a positive voltage, and off (RESET process) at a negative voltage. In the 1T1R cells, the SET process can be activated by applying positive voltages on the top electrode of the M. For the RESET process, positive voltages are applied to the source of the T, while the top electrode of the M is grounded. Therefore, using negative voltages on the T can be avoided.

Operating Voltage: When the applied voltage overcomes the pinch-off voltage of the T, the current in the T is saturated. Thus, this saturated current serves as current compliance for the M. Since the level of current compliance determines the RS operations (see Figure 6.6(g)), a precise alignment is required between the operating parameters of the two components. For instance, an optimal condition for the SET is that the pinch-off voltage is smaller than the SET voltage. Thus, current compliance can be imposed during the SET process. If the SET voltage is smaller than the pinch-off voltage, the subthreshold swing of the T should be low. If not, an effective hysteresis can be only partly visible in I-V curves. Additionally, the SET voltage should be smaller than the breakdown voltage of the T.

An optimal saturation current of the T should be pre-determined to ensure RS operation with large hysteresis, and at the same time to prevent an electric breakdown of the M. Here, the level of the saturation current can be modulated by varying V_G .

The optimal condition for the RESET voltage is similar to that for the SET voltage. However, in case the SET and the RESET process requires different current level, V_G needs to be differently set to provide optimal current compliance to the M. Additionally, the sweep voltage can be differently set for the SET and the RESET processes. As shown in Figure 6.6(g), a larger voltage induces a more-lowered resistance in the M.

 $\mathbf{R_{on}}$ of the T is also an important parameter since the supply voltage is divided into the two electronic components in the 1T1R cell. R_{on} should be smaller than the resistance of the M. If R_{on} is too large, the majority of the voltage drops over the T, failing the switching process (SET and RESET) in the M.

3) Current in the off-state in the T (off-current) was 1 μA , which was the same level as the current of a single memristive device at 1.5 V (see Figure 6.6(f)). It means that the RS operation is hardly recognizable in the 1T1R cell.

To be compatible with the T, memristive devices should have i) operating voltage smaller than 4 V, ii) operating current of between 1 μA and 35 μA , and iii) R_M of $\sim 10~k\Omega$. Considering the ii) and iii), the TiO_x-HfO_x-based-memristive devices used here (so-called M) are not an optimal device for the T. For instance, the M needs current compliance of at least 500 μA for an R_M of 36 $k\Omega$ in the LRS, as shown in Figure 6.6 (g). An alternative memristive device for 1T1R cells (when using the T) is the TiO₂-based-memristive devices presented in ch.5.1. For example, the Al/TiO₂/TiN devices, which are referred to as TiO-device in the following, can be fabricated on top of the source of the T. The resistance of the pristine TiO-device is three orders of magnitude larger than the R_{on} of the T, as shown in Figure 5.4(b). Additionally, the TiO-device is turned on and off in negative and positive voltages, respectively. When the T is in the on-state ($V_{GS} = 2V$) and V_{DS} is applied on the drain of the T, the majority of the voltage would drop over the TiO-device. It means that the T cannot serve as current compliance on the TiO-device, since the voltage drop over the T is not likely to overcome the pinch-off voltage. Therefore, external current compliance (let's assume 50 μA) is needed for an electroforming process in the TiO-device.

Here, the external current compliance prevents the TiO-device from an electrical breakdown. Once the LRS is written on the TiO-device, the R_M of $\sim 50~k\Omega$ is comparable to the R_{on} . Afterward, a stronger SET process might take place, if a $V_{\rm GS}>2$ V allows for saturation current larger than $50~\mu\rm A$, together with a different LRS in the TiO-devices. $V_{\rm DS}>3$ V is applied to the drain of the T. The resistance of the TiO-device decreases further, which leads to a larger voltage drop over the T. In this case, the T can serve as current compliance on the TiO-device. For a RESET process, it is recommended to apply $V_{\rm DS}<3$ V to the top electrode of the TiO-device, since the RESET voltage is smaller than the SET voltage.

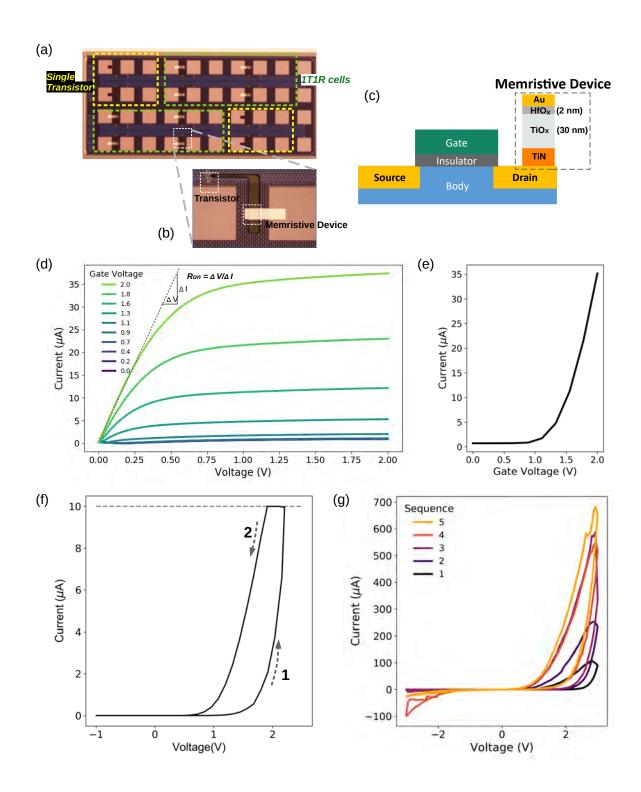


Figure 6.6: (a) Optical microscope (OM) image of 1T1R cells with single transistors. (b) Close-up OM image of a 1T1R cell. (c) Schematic of the structure of a 1T1R cell. (d) Output characteristics of a single transistor. (e) Transfer characteristics of a single transistor. (f) RS operation in a single memristive device. (g) RS operations without using current compliance.

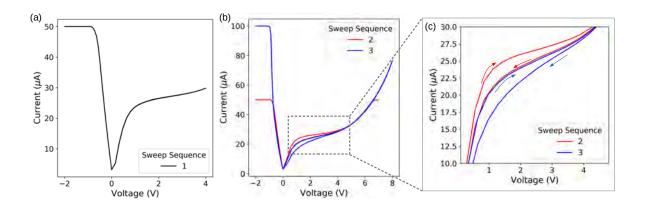


Figure 6.7: (a) I-V characteristics of a 1T1R cell in the first sweep condition(see table6.2). (b) I-V characteristics of a 1T1R cell in the second and the third sweep condition(see table6.2). (c) Close-up of the I-V characteristics in the second and the third sweep conditions.

7 Application of Memristive Devices in Neuromorphic Computing

For neuromorphic computing with high energy efficiency and high throughput, memristive devices should have i) low latency with low power consumption, ii) linearity for conductance update, and iii) reliability (retention, endurance, variability) [IA19a, CSS+19]. However, a priority in the device parameters depends on the assigned tasks in neuromorphic computing such as inference and training algorithms (see ch.2.2.2). In the inference algorithms, long retention is a critical parameter for memristive devices. In the training algorithms, high linearity of conductance update is more important for efficient programming with high accuracy than retention property [CSS+19]. In the previous ch.5.3 we studied the retention property. In this section, we focus on CL. Investigated devices are the TiO_x/HfO_x-based memristive devices (see ch.5.2) and TiO_x/AlO_x/HfO_x-based memristive devices (see ch.5.3) that showed possibilities to tailor the RS characteristics. The methods to optimize the linearity is introduced in two aspects: internal engineering and external engineering. In our study, internal engineering includes designing physical device structures with appropriate materials and the sequence of the oxide materials. On the other hand, external engineering includes applying designed pulse waveforms on memristive devices. Fabrication methods for the devices in the internal engineering are detailed in ch.3.1. The study of the external engineering was conducted by Nayoun Kim [Kim22].

7.1 Optimization of Conductance Linearity: Internal Engineering

RS mechanisms are strongly related to material properties of switching layers [WWNX10, SAR+18, SJV⁺16, MSJ⁺11] and interfacial interactions between different materials [Val17, CBM⁺21]. In the following, we present how CL can be tuned by the design of metal oxide stacks in metal-oxide-basedmemristive devices. Two different oxide stacks are presented: TiO_x/HfO_x and TiO_x/AlO_x/HfO_x. Their relevant layer stacks are depicted in Figure 7.1. All have TiN as the bottom electrodes, and Au as the top electrodes. The TiO_x/HfO_x-based-memristive devices (bilayer devices) have TiO_x (30 nm) and HfO_x (2 nm) as the switching layers. The TiO_x/AlO_x/HfO_x-based-memristive devices (trilayer devices) consist of TiO_x (15 nm) and HfO_x (3 nm) layers, and between the two oxide layers AlO_x layer (2 nm) is inserted. In these two different oxide stacks, the oxygen stoichiometry of the HfO_x layers was further modified. In one type of device, the stoichiometry of x = 1.98 in the HfO_x was achieved by depositing the film using the rotation mode (see ch.4.3). In the other type of devices, the HfO_x stoichiometry was x < 1.95, for which the stationary mode (see ch.4.3) was used during sputtering. Therefore, four different types of memristive devices were fabricated. The trilayer devices showed compliance-free RS operations in DC voltage measurements (see ch.5.3), while the bilayer devices required current compliance during the RS operations (see ch.5.2). Moreover, the trilayer devices showed an improved retention time compared to the bilayer devices. We assumed that the AlO_x layer served as an oxygen diffusion blocking layer [JKR⁺21, PPL⁺11], suppressing the diffusion of oxygen vacancies between the TiO_x layer and the HfO_x layer. The details of the RS characteristics for the bilayer devices and the trilayer devices were





Figure 7.1: Relevant layer stacks of (a) bilayer devices and (b) trilayer devices.

dealt with in the ch.5.2 and the ch.5.3, respectively. In this section, CL is investigated in terms of the impact of the AlO_x layer and the stoichiometry of the HfO_x layer.

7.1.1 Conductance Linearity

Pulse measurements were conducted on the four different types of memristive devices. The used waveforms of pulse signals are depicted in Figure 7.2. Firstly, the conductance of devices was read at reading voltage pulses (V_r^p) . Following, a train of switching pulse signals was applied which comprised of 20 consecutive SET voltage pulses (V_{SET}^p) and 20 subsequent RESET voltage pulses (V_{RESET}^p) . Here, a V_r^p followed every switching voltage pulse to track a change in conductance states caused by switching pulse signals. The pulse parameters for the respective devices are found in Table 7.1. The measured conductance values were normalized to have values between 0 to 1 based on the maximum conductance values of the respective devices, which allows for comparing the CL of different devices using a common scale.

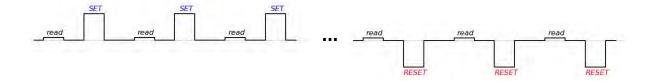


Figure 7.2: Waveforms of pulse signals for the investigation of CL.

Type	$V_{\text{SET}}\left(\mathbf{V}\right)$	$t_{\rm SET}({\rm ms})$	$V_{\text{RESET}}\left(\mathbf{V}\right)$	$t_{\rm RESET}({\rm ms})$	$V_{\rm r}({ m V})$	$t_{\rm r}({\rm ms})$
Bilayer-H	3	10	-2	10	1	100
Bilayer-L	-1.5	1	1.5	1	0.1	10
Trilayer-H	2.5	50	-1.5	50	1.2	50
Trilayer-L	2.5	50	-1.5	50	1.2	50

Table 7.1: Parameters used in pulse measurements for investigating CL. The type of device is denoted to device-H or device-L depending on the stoichiometry of HfO_x . The former represent x=1.98, while the latter x= 1.80 - 1.95.

Pulse measurements for CL tests were conducted on the bilayer devices (see Figure 7.1(a)). Two different types of bilayer devices were examined. One type of the bilayer device had the HfO_x layers with

the oxygen stoichiometry of x = 1.98, while the other type with x < 1.95 (see ch.4.3). The former is referred to as bilayer-H devices and the latter as bilayer-L devices in the following.

CL of a bilayer-H device is presented as a function of pulse count in Figure 7.3(a). At the first V_r^p , a noticeable increase in the conductance was observed. In the following V_r^p , however, the conductance increased gradually with increasing number of V_r^p . For the RESET process, the first V_{RESET}^p reduced the conductance immediately. However, the following conductance change by the additional V_{RESET}^p appeared fairly smooth.

CL of a bilayer-L device is present in Figure 7.3(b). By applying the very first $V_{\rm SET}^p$, an immediate increase in the conductance was triggered. In the subsequent $V_{\rm SET}^p$, the change in the conductance was barely recognizable. However, as soon as the first $V_{\rm RESET}^p$ was applied, an abrupt conductance drop was seen. In the additional $V_{\rm RESET}^p$, the conductance remained almost constant. The conductance change was highly nonlinear, presenting two distinguishable states.

The bilayer-H devices presented an improved CL (see Figure 7.3(a)) compared to the bilayer-L devices (see Figure 7.3(b)). The bilayer-H devices showed interface-type RS operations, whereas the bilayer-L devices filamentary-type RS operations (see the details in ch.5.2). CL is strongly related to the rate of the migration of oxygen-related ions [PLK+19]. In the interface-type devices, the migration of oxygen-related ions occurs over the entire device area, which attributes to the RS operations. On the contrary, in the filamentary-type devices, a localized CF connecting two electrodes causes RS behaviors. During the growth of the CF, high local temperatures along the CF can occur due to the localized currents and high voltages [Was12]. It promotes the migration of oxygen-related ions [ZGT+19]. Therefore, the RS of the filamentary-type devices is a highly non-linear process compared to the interface-type devices, as seen in our bilayer devices as well.

Pulse measurements for the CL were conducted on the trilayer devices. Two different types of trilayer devices were examined. Similar to the bilayer devices, one type of the trilayer device had the HfO_x layers with the oxygen stoichiometry of x=1.98, while the other type with x<1.95. The former is referred to as trilayer-H devices and the latter as trilayer-L devices in the following. Both devices showed interface-type RS operations (see ch.5.3).

CL of a trilayer-H device was examined as shown in Figure 7.3(c). The SET process showed a sufficiently gradual and linear conductance update by the application of 15 $V_{\rm SET}^p$. After that, the conductance seemed to be saturated. Following, the first $V_{\rm RESET}^p$ caused around 50% decrease in overall conductance change. While the additional $V_{\rm RESET}^p$ were applied, nonlinearity in the conductance was observed. At the 25th $V_{\rm r}^p$, saturation in the conductance was exhibited. In the trilayer-H device, the conductance change during the RESET process was nonlinear compared to the SET process. It is because for the RESET process the oxygen ions migrate driven by applied voltage as well as the gradient of ion concentration that is created during the SET process [DHZ⁺16].

CL of a trilayer-L device was investigated as shown in Figure 7.3(d). The conductance update followed a clear linear trend for the SET process. For the RESET process, the first $V_{\rm RESET}^{\rm p}$ decreased the resistance by 20 % of the overall change. Afterward, a fairly gradual decrease in conductance was observed. At the 30th $V_{\rm r}^{\rm p}$, saturation in the conductance was observed. The trilayer-L device presented an improved CL compared to the trilayer-H device (see Figure 7.3(c)). We assume that an increasing amount of oxygen vacancies in the HfO_x layer might adjust the upper limit for the conductance saturation point, allowing for continuous ion migration during the RS operation [PLK+19].

We found a fairly linear conductance update by repeated switching pulses in the three interface-type devices of the bilayer-H, trilayer-H, and trilayer-L devices. Among them, the best linearity was achieved in the trilayer-L device. Insertion of a thin AlO_x layer between the TiO_x and HfO_x improved the linearity in conductance update. We assume that the AlO_x layer suppresses the nonlinear behavior of the migration of oxygen-related ions between the TiO_x layer to the HfO_x layer due to its low diffusion coefficient compared to the two layers [JKR $^+$ 21, HPW85].

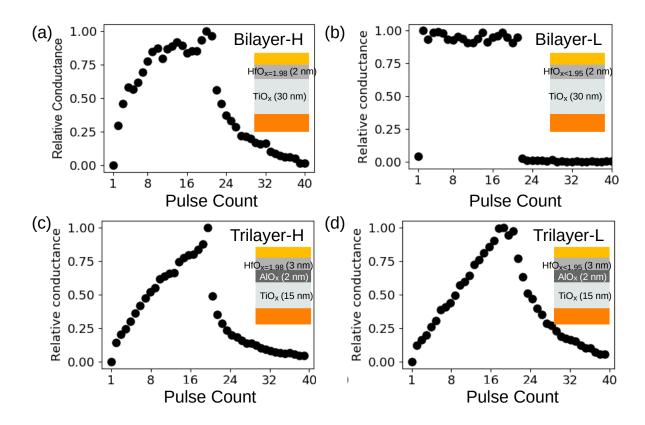


Figure 7.3: CL for (a) the bilayer-H device, (b) the bilayer-L device, (c) the trilayer-H device, and (d) the trilayer-L device. The relevant layer stacks of the examined devices are shown in the subset of the corresponding figures.

The bilayer-L devices showed a highly nonlinear conductance change when using identical switching pulses. They were further investigated to check the influence of the switching pulse amplitude on the CL. The designed waveform is depicted for the SET and the RESET process in Figure 7.4(a) and (b), respectively. Firstly, the conductance state (G_0) was read at V_r^p . Afterward, a V_{SET}^p or a V_{RESET}^p was applied. After that, 200 consecutive V_r^p were applied to check whether the conductance state was maintained over time. This measurement was repeated varying the switching voltage incrementally for the SET and the RESET, accordingly. The parameters used in the measurements are summarized in Table 7.2. The measured conductance (G) was subtracted by G_0 to calculate the conductance change (ΔG) as the following equation: $\Delta G = G - G_0$. Figure 7.5(a) shows the ΔG per pulse count for the respective switching voltage. The ΔG was affected by the applied switching voltage. The smaller the $V_{\rm SET}^{\rm p}$ was, the larger ΔG was observed. The greater the $V_{\rm RESET}^{\rm p}$ was, the smaller ΔG was observed. A conductance state stimulated by corresponding switching voltages was retained for 200 consecutive V_r^p , implying a good retention (supported further by retention tests of the bilayer devices in Figure 5.14(e)). The different conductance states were well separated both in the SET and the RESET. Furthermore, we calculated median values of the conductance (G_{median}) at each switching voltage and calculated the respective ΔG $(G_{median} - G_0)$. Afterward, the ΔG was normalized to have a value between 0 to 1. The resistance of the SET and the RESET were different in orders of magnitude. Thus, the ΔG values were compared using a common scale. The normalized conductance value (ΔG_{norm}) is presented in terms of applied switching voltages for the SET and the RESET processes in Figure 7.5(b) and (c), respectively. By modulating $V_{\rm SET}^{\rm p}$ or V_{RESET}^{p} , the linearity in the conductance change was successfully achieved in the bilayer-L devices.

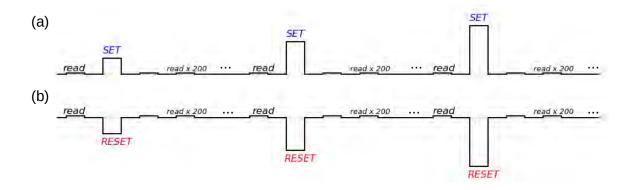


Figure 7.4: Waveform of designed pulse to investigate the impact of switching voltages on the CL of the bilayer-L devices. (a) Incrementally increasing $V_{\rm SET}^{\rm p}$. (b) Incrementally decreasing $V_{\rm RESET}^{\rm p}$

Type	HfO _x stoichiometry	V_{\min}, V_{\max} (V)	$t_{\text{set or reset}}(\text{ms})$	$V_{\rm r}({ m V})$	$t_{\rm r}({\rm ms})$
Bilayer-L device	SET	-1.2, -0.86	1	0.1	10
Bilayer-L device	RESET	0.67, 0.98	50	1.2	50

Table 7.2: Parameters used in pulse measurements for CL tests in the bilayer-L devices

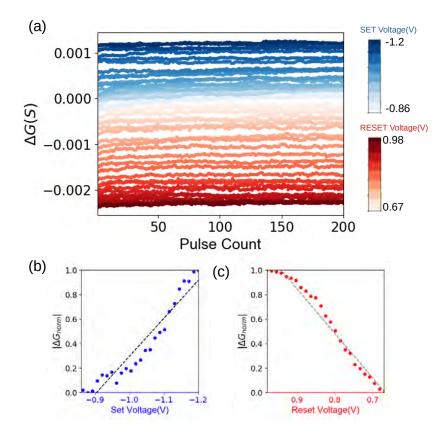


Figure 7.5: CL by adapting switching voltages in the bilayer-L devices

7.2 Optimization of Conductance Linearity: External Engineering

Pulse measurements need a wide range of parameters to be controlled such as pulse width, pulse amplitude, and pulse period, as shown in Figure 7.6. Therefore, a careful setting of the parameters is required to control the CL of memristive devices. In this section, CL of the TiN/TiO_x/HfO_x/Au memristive devices are examined via pulse measurements. A representative RS behavior of the TiN/TiO_x/HfO_x/Au devices are shown in Figure 7.7(a). In DC voltage sweep measurements, the SET process was observed at a voltage larger than 2 V, and the RESET process was observed at a voltage smaller than -0.1 V. The memristive devices showed scaled currents with the device area as shown in Figure 7.7(b), which indicates an interface-type RS behavior. Further details are described in [Kim22]. For the pulse measurements, pulse parameters are controlled to investigate their impacts on CL of the TiN/TiO_x/HfO_x/Au devices. The investigated pulse parameters are shown in Figure 7.6: pulse width for switching, pulse amplitude for switching, and pulse period. Only one of the pulse parameters is varied during pulse measurements, holding the others constant. Based on the examined conductance change, the impact of the pulse parameters on CL is evaluated. Furthermore, a concept of anti-pulse incorporation is introduced, which is an opposite polarity of voltage pulse (anti-pulse) combined with SET or RESET pulses as shown in Figure 7.11. The impact of anti-pulse signals on the conductance change in the TiN/TiO_x/HfO_x/Au devices is investigated. Finally, a method to analyze CL via machine learning is proposed using the collected data during the pulse measurements.

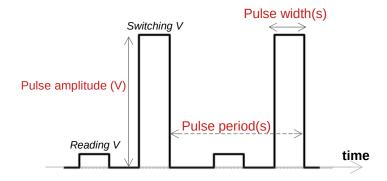


Figure 7.6: Investigated pulse parameters: switching pulse width (Pulse width), switching pulse amplitude (Pulse Amplitude), and pulse period.

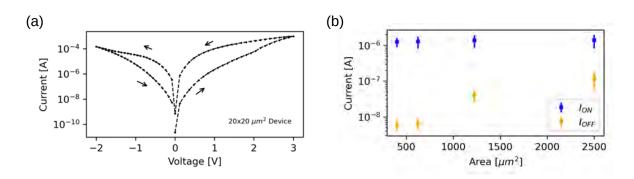


Figure 7.7: (a) an I-V relation of the TiN/TiO_x/HfO_x/Au memristive devices conducted in a DC voltage sweep measurements [Kim22]. (b) Scaled current I_{OFF} with device area of the TiN/TiO_x/HfO_x/Au memristive devices [Kim22]

7.2.1 Conductance Linearity

In the measurements, the initial device state (G_0) is firstly read at reading pulse (V_r^p) . After that, *test cycle* is started which refers to a set of 100 consecutive switching pulses (V_w^p) and V_r^p . In a test cycle, a V_r^p follows an individual V_w^p in order to read the conductance state of the devices. At the end of every test cycle, a DC voltage sweep measurement is executed to return the device to the G_0 . The used V_r^p is 0.5 V for 0.5 ms, and the base voltage (off-voltage) is 0 V.

Switching Pulse Width

 $V_{\rm w}^{\rm p}$ includes the SET pulses ($V_{\rm SET}^{\rm p}$) and the RESET pulses ($V_{\rm RESET}^{\rm p}$). Switching pulse width ($t_{\rm w}$) is defined as the elapsed time between the rising and falling edges of a single $V_{\rm w}^{\rm p}$. While a $V_{\rm w}^{\rm p}$ is applied to memristive devices over $t_{\rm w}$, surface charges can be accumulated in the vicinity of the electrodes, which can enhance electric field within the device [CJP95, LZMC16]. During RS operations in memristive devices, oxygen ions are transported within the switching layers. The migration of ions exponentially depends on the electric field [Was12]. Thus, enhanced electric field by accumulated charges can lead to nonlinear conductance update in memristive devices [LWC18]. Therefore, $t_{\rm w}$ is one of the most important parameters to determine CL [CCL+19, PSK+13, PMBH+15, XGT+20].

Pulse measurements on a TiN/TiO_x/HfO_x/Au device were conducted. In one test cycle, a series of 100 consecutive identical V_w^p was applied, during which the conductance change was traced at V_r^p . In the subsequent test cycle, only the $t_{\rm w}$ was varied. The $t_{\rm w}$ ranged from 0.1 s to 1.3 s with an increment of 0.1 s. The other parameters were held constant: the off-voltage width was 0.1 s. The V_w^p were 2 V and -1 V for the SET and the RESET processes, respectively. Measured conductance value at $V_{\rm r}^{\rm p}$ per pulse count is plotted for the respective t_w . In the Figure 7.8(a), for all widths of SET pulses (t_{SET}), the conductance increased rapidly by the first 20 $V_{\rm SET}^{\rm p}$ signals compared to the following $V_{\rm SET}^{\rm p}$ signals. We investigated in detail the magnitude of the conductance change. Firstly, the total conductance change (ΔG) was calculated, subtracting the conductance at the 100th V_r^p from the initial conductance (G_0) . In Figure 7.8(b), the ΔG increased proportionally to the $t_{\rm SET}$. The result shows a possibility to achieve multistate in the conductance by adjusting t_{SET} . Furthermore, the CL was evaluated, for which an increment of conductance values between the first V_r^p and the second V_r^p was calculated. Afterward, the calculated values were normalized to have between 0 to 1 by dividing by the ΔG for the respective $t_{\rm SET}$. It allowed for comparing the CL using a common scale. Figure 7.8(c) displays nonlinearity (NL) in the conductance. The NL was in the range between 0.15 to 0.28. It means that the first two $V_{\text{SET}}^{\text{p}}$ signals increased the conductance by the minimum 15 % to the maximum 28% of the ΔG . Considering total 100 $V_{\rm SET}^{\rm p}$ signals were applied, the CL appears to follow a nonlinear trend.

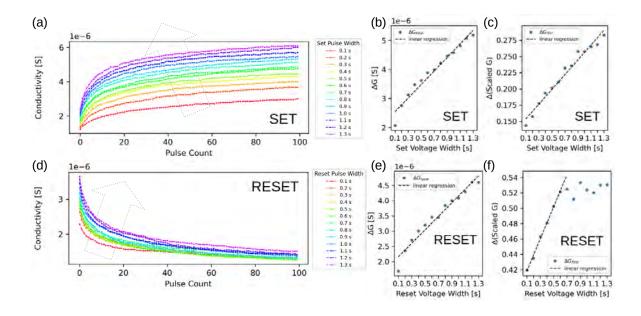


Figure 7.8: Impact of switching pulse width on conductance states [Kim22]. Measured conductance per pulse count in (a) the SET process and (d) the RESET process. Calculated total conductance change (ΔG) and linear fits for (b) the SET process and (e) the RESET process as a function of $t_{\rm SET}$ and $t_{\rm RESET}$, respectively. Normalized ΔG values (Δ (Scaled G) in the figures) which shows NL and linear fits for (c) the SET process and (f) the RESET process as a function of $t_{\rm SET}$ and $t_{\rm RESET}$, respectively.

The measurement results for the RESET process are shown in Figure 7.8(d). Most conductance changes occurred by the first 20 RESET pulses ($V_{\rm RESET}^{\rm p}$) similar to the SET process. Analysis for the RESET process was performed similarly to that for the SET process. The ΔG linearly increased with increasing the RESET voltage width ($t_{\rm RESET}$) in Figure 7.8(e), implying the multistate in the conductance. In Figure 7.8(f), the NL values are greater than those for the SET process. The values are close to 0.5, which means

that 50 % of ΔG was caused by the first two $V_{\rm RESET}^{\rm p}$. The NL increased with increasing the $t_{\rm RESET}$, but it was saturated to 0.53 at a $t_{\rm RESET}$ of 0.7.

For both the SET and the RESET process, the multistate in the conductance was observed. The ΔG was comparable for the SET and the RESET processes, which means symmetric ΔG is expected using the same $t_{\rm w}$ for the SET and the RESET processes. For the SET process, the $t_{\rm w}$ appears as an effective measure for tuning the CL. However, for the RESET, the NL was significantly greater than for the SET process. Furthermore, the NL increased faster for the RESET than for the SET process by modulating $t_{\rm w}$, when the two slopes of the linear fit-lines in Figure 7.8(c) and (f) are compared. Summarizing, a $t_{\rm w}$ of 0.1 s seems to be the best option to achieve symmetric ΔG and NL at the same time among the other $t_{\rm w}$, if the same pulse widths should be used for the $t_{\rm SET}$ and $t_{\rm RESET}$.

Pulse Period

We varied the pulse period by changing the off-voltage pulse width $(t_{\rm off})$. Over $t_{\rm off}$, voltages are turned off. Oxygen ions (or oxygen vacancies) within switching layers can diffuse back by the concentration gradient when an applied electric field is removed [DHZ⁺16]. Therefore, $t_{\rm off}$ can affect the RS behaviors. On a TiN/TiO_x/HfO_x/Au device, pulse measurements were conducted similarly to the experiments for the $t_{\rm w}$ tests above. In the measurements, the $t_{\rm off}$ was varied in every test cycle, while all other parameters were kept constant. Pulse parameters for $V_{\rm w}^{\rm p}$ were taken from the $t_{\rm w}$ tests above that showed the best symmetry in the ΔG and the NL. The switching pulse amplitude was 2.0 V for the SET and -1.0 V for the RESET. For both the SET and the RESET, $t_{\rm w}$ was 0.1 s.

For the SET process, the conductance change per pulse count is shown in Figure 7.9(a) for the respective $t_{\rm off}$. For all $t_{\rm off}$ the conductance increased rapidly by the first 20 $V_{\rm SET}^{\rm p}$ signals than in the following $V_{\rm SET}^{\rm p}$. A similar analysis was conducted with the $t_{\rm w}$ tests above. The ΔG linearly decreased with increasing $t_{\rm off}$, as seen Figure 7.9(b). However, ΔG is much smaller than the ΔG in the $t_{\rm w}$ tests (see Figure 7.8(b)). In Figure 7.9(c), the NL was less than 0.15, implying that less than 15% change of the ΔG occurred at the first two $V_{\rm r}^{\rm p}$. It appears an improved linearity could be obtained by modulating $t_{\rm w}$.

For the RESET process, pulse measurements were carried out similarly to that for the SET process. Figure 7.9(d) shows the conductance change for the respective $t_{\rm off}$ in the RESET process. Conductance decreased faster by the first 20 $V_{\rm RESET}^{\rm p}$ signals, which is a similar trend to the SET process. The ΔG seemed to decrease with increasing $t_{\rm off}$ as shown in Figure 7.9(e). In terms of the NL, in Figure 7.9(f), there was not a clear trend, although the NL values appeared to decrease with increasing $t_{\rm off}$.

The smaller ΔG was observed than that in the $t_{\rm w}$ tests, and a trend in the NL was barely recognizable by modulating $t_{\rm off}$ for both the SET and RESET processes. The $t_{\rm off}$ of 0.1 s seems to be the best choice to achieve an adequate ΔG with symmetry in the CL. Although the impact of the $t_{\rm off}$ is weaker than that of the writing pulse width, the results showed a possibility of a fine-tuning in conductance by adjusting the $t_{\rm off}$.

Pulse Amplitude

The amplitude of switching voltage determines the strength of the applied electric field in the device. To achieve RS and the adequate ΔG , a sufficient electric field is required in memristive devices [LWC18]. We investigated the effect of the amplitude of $V_{\rm w}^{\rm p}$ focusing on the RESET process, since the RESET process showed a high NL compared to that in the SET process (see the tests for $t_{\rm w}$, and $t_{\rm off}$).

A TiN/TiO_x/HfO_x/Au device was investigated using the pulse measurements in which only the amplitude $V_{\rm RESET}^{\rm p}$ was varied for every test cycle, while the other parameters were kept constant. The $t_{\rm off}$ and

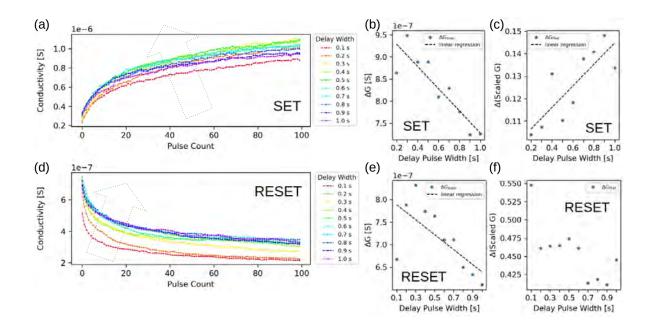


Figure 7.9: Impact of pulse period on conductance states [Kim22]. Measured conductance per pulse count in (a) the SET process and (d) the RESET process. Calculated total conductance change (ΔG) and linear fits in (b) the SET process and (e) the RESET process as a function of $t_{\rm SET}$ and $t_{\rm RESET}$, respectively. Normalized ΔG values (Δ (Scaled G) in the figures) as a function of $t_{\rm SET}$ and $t_{\rm RESET}$, respectively, and linear fits for (c) the SET process and (f) the RESET process.

the $t_{\rm RESET}$ was 0.1 s. ΔG and the NL are investigated in the similar manner with the previous two tests for $t_{\rm w}$ and $t_{\rm off}$. In Figure 7.10(a), the ΔG increased linearly as $V_{\rm RESET}^p$ increased. However, the ΔG was saturated at around -1.5 V. Figure 7.10(b) presents that the NL increased with increasing $V_{\rm RESET}^p$. The slope of the fit-line of the NL is higher than that in the other two tests (for $t_{\rm w}$ in Figure 7.8(f) and for $t_{\rm off}$ in Figure 7.9(f)). It indicates the strongest impact than the other two parameters for the RESET process. At a $V_{\rm RESET}^p$ smaller than -0.7 V, the NL values were comparable to the NL for the SET process (Figure 7.8(c)). Yet, the ΔG was also affected by $V_{\rm RESET}^p$ as well. It means the device will not be fully turned off at a small $V_{\rm RESET}^p$. Given that the range of the ΔG for the SET process was between 2 μS to 5 μS (see Figure 7.8(b)), a $V_{\rm RESET}^p$ larger than -0.5 V seems to be the bottom limit for the RESET voltage to achieve symmetric RS. When considering the ΔG and the NL altogether, a $V_{\rm RESET}^p$ of -0.6 V seems to be the best choice among the other tested voltages.

Anti-pulse Incorporation

Incorporation of the opposite polarity of voltage pulse (anti-pulse) with SET or RESET pulses has been introduced in several works of literature to control CL [LWC18, WCC+16, KCLL14]. The integration of the anti-pulse is expected to diminish the effect of $V_{\rm w}^{\rm p}$ resulting in a steadier change in conductance. In this section, the impact of anti-pulse incorporation on CL is investigated. The designed anti-pulse waveforms are shown in Figure 7.11. Pulse measurements are conducted on a TiN/TiO_x/HfO_x/Au device. In the experiments, the amplitude of the anti-pulse was varied for every test cycle, holding the other parameters constant. $V_{\rm SET}^{\rm p}$ and $V_{\rm RESET}^{\rm p}$ were 2 V, and - 1 V, respectively. $t_{\rm w}$ and $t_{\rm off}$ were 0.1 s. For the test cycles in the SET process, the anti-pulse voltage ($V_{\rm anti}^{\rm p}$) was varied from -0.1 V to -1.2 V. The

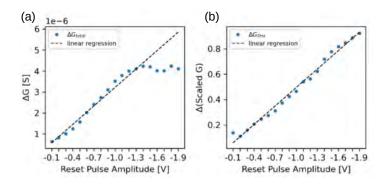


Figure 7.10: Impact of RESET pulse amplitude on conductance states [Kim22]. (a) Calculated total conductance change (ΔG) and the linear fit as a function of $V_{\text{RESET}}^{\text{p}}$. (b) Normalized ΔG (Δ (ScaledG) in figures) and the linear fit as a function of $V_{\text{RESET}}^{\text{p}}$.

measured conductance was normalized to have between 0 to 1, divided by the corresponding maximum conductance for the respective $V_{\rm anti}^{\rm p}$ test cycles. Figure 7.12(a) shows the normalized conductance change per pulse count. The larger the $V_{\rm anti}^{\rm p}$ was, the more improved CL was observed. However, a $V_{\rm anti}^{\rm p}$ greater than -1 V hardly showed conductance change or even decreased the conductance, as shown in Figure 7.12(b). Further investigation was carried out in a similar way to the $t_{\rm w}$ analysis. The ΔG decreased with increasing $V_{\rm anti}^{\rm p}$, as seen in Figure 7.12(c). At $V_{\rm anti}^{\rm p}$ smaller than -0.5 V, the ΔG dropped rapidly. Moreover, in Figure 7.12(d), the NL showed a slight decrease when using a $V_{\rm anti}^{\rm p}$ larger than -0.7 V. The NL values were overall small compared to the NL observed in the other parameters tests ($t_{\rm w}$, and $t_{\rm off}$).

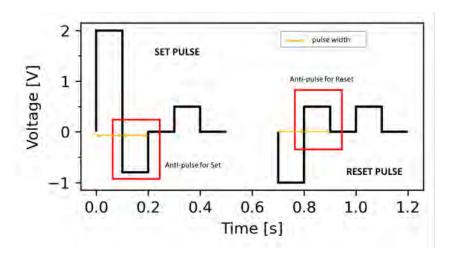


Figure 7.11: Waveforms of anti-pulse signals for the SET (left) and the RESET processes (right) [Kim22]

For the RESET process, the pulse waveform of incorporated anti-pulse is seen in Figure 7.11(right). $V_{\rm anti}^{\rm p}$ was varied from 0 V to 2 V. Figure 7.13(a) shows the normalized conductance for the respective $V_{\rm anti}^{\rm p}$. It is difficult to find a clear trend in the conductance by modulating $V_{\rm anti}^{\rm p}$. However, a $V_{\rm anti}^{\rm p}$ of 2 V showed an increasing conductance after the application of the 30th $V_{\rm RESET}^{\rm p}$, as seen in Figure 7.13(b). A $V_{\rm anti}^{\rm p}$ greater than 2 V will not reset the device anymore. We further investigated ΔG and NL similarly to the analysis for the SET process. The ΔG was hardly affected by $V_{\rm anti}^{\rm p}$ as seen in Figure 7.13(c). However, there was a drop in the ΔG at a $V_{\rm anti}^{\rm p}$ greater than 1.3 V. We assumed that the impact of the $V_{\rm anti}^{\rm p}$ became stronger than the $V_{\rm RESET}^{\rm p}$ on the RS operation, which was clearly observed at a $V_{\rm anti}^{\rm p}$ of 2 V (see in Figure 7.13(b)).

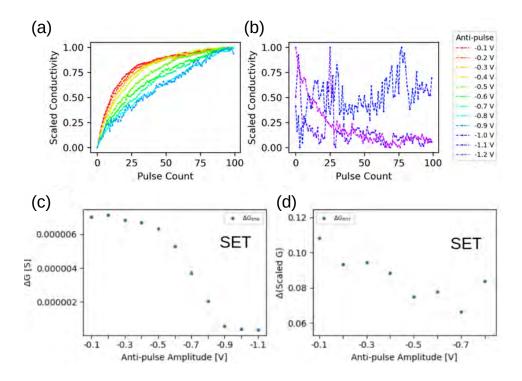


Figure 7.12: Impact of $V_{\rm anti}^{\rm p}$ for SET process on conductance states [Kim22]. Measured and normalized conductance values (Scaled Conductivity in the figures) per pulse count for the SET process (a) for the anti-pulse voltage from -0.9 V to -0.1 V, and (b) from -1.0 V to -1.2 V. (c) Calculated ΔG as a function of $V_{\rm anti}^{\rm p}$. (d) Normalized ΔG (Δ (Scaled G) in the figure) as a function of $V_{\rm anti}^{\rm p}$.

Furthermore, as shown in Figure 7.13(d), the NL decreases with increasing $V_{\rm anti}^{\rm p}$. The NL values were the smallest among other three tests ($t_{\rm w}$, $t_{\rm off}$, and $V_{\rm RESET}^{\rm p}$). It implied that incorporating $V_{\rm anti}^{\rm p}$ is the best method to improve the CL for the RESET process among the other test parameters.

The $V_{\rm anti}^{\rm p}$ incorporation method was the most effective method among other tested parameters for both the SET and the RESET processes. For the SET process, the best linearity was achieved using a $V_{\rm anti}^{\rm p}$ of -0.8 V. However, a $V_{\rm anti}^{\rm p}$ between -0.5 V and -0.8 V is recommended, considering the trend change in the ΔG and the NL. For the RESET process, the impact of the $V_{\rm anti}^{\rm p}$ was weaker than for the SET process. However, the result showed a possibility to tune the linearity gradually using $V_{\rm anti}^{\rm p}$. The best option seems to be a $V_{\rm anti}^{\rm p}$ of 1.3 V with the RESET voltage of -1 V, considering a sufficient ΔG with a small NL value.

7.2.2 Machine Learning in Analysis of Conductance Linearity

Machine learning is a field of study that trains computers to make a prediction on complicated problems without being explicitly programmed to do so [Bur26, McC26]. The accuracy of the prediction is tuned through training algorithms dealing with data with millions of dimensions. This section introduces a procedure to train an algorithm to estimate the impact of pulse parameters on the CL in the TiN/TiO_x/HfO_x/Au devices. Here, the SET process was focused on which showed a noticeable conductance modification compared to the RESET process. In the following, the architecture of the used

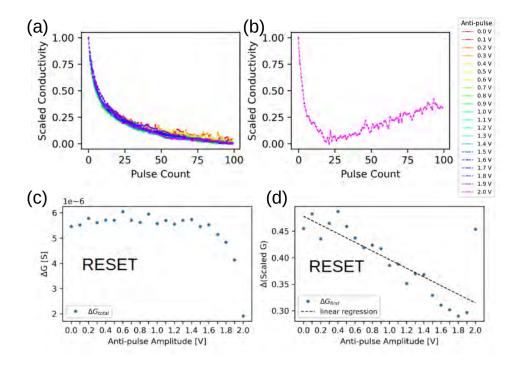


Figure 7.13: Impact of anti-pulse amplitude for RESET process on conductance states [Kim22]. Measured and normalized conductance values (Scaled Conductivity in the figures) per pulse count for the RESET process (a) for the anti-pulse voltage from 0 V to 1.3 V, and from (b) 1.3 V to 2.0 V. (c) Calculated ΔG as a function of $V_{\rm anti}^{\rm p}$. (d) Normalized ΔG (Δ (Scaled G) in the figure) as a function of $V_{\rm anti}^{\rm p}$.

training model, methods of the data preparation, parameters for training the model, and the evaluation of the trained model are presented. To be familiar with a few terminologies in the following section, it is recommended to check ch.2.2.1 and ch.2.3.

Architecture: The used algorithm was a multilayer perceptron neural network model (NN). The architecture of the NN consists of the input features (X) in one input layer, one hidden layer with 64 neurons, and one output layer with one neuron. The schematic of the NN is depicted in Figure 7.14. Six features of the X in the input layer are fed to the neurons in the hidden layer. Each neuron in the hidden layer computes the weighted average of the X. In the hidden layer, the weighted average is passed through an activation function for which the *Rectified Linear Unit* was used (see ch. 2.3.2). Additionally, the *Dropout* function was added which randomly drops out outputs of the neurons in the hidden layer with a dropout rate of 20 %, which prevents over-fitting [Bro03] (see ch.2.3.2). The outputs of the hidden layers are weighted and fed to the neuron in the output layer. The weighted average in the neuron is passed through the linear activation function (see ch.2.3.2), which results in the output feature (Y).

Data Preparation: X includes pulse number (pulse count), t_{SET} , $V_{\text{SET}}^{\text{p}}$, t_{off} , t_{r} , and $V_{\text{anti}}^{\text{p}}$. X values were normalized to have zero mean and a standard deviation of one for the respective features using the following equation:

$$X' = \frac{X - X_{mean}}{\sigma} \tag{7.1}$$

Here the X', the X_{mean} , and the σ are the normalized X, the mean value of X and the standard deviation of X. Y values were the measured conductance values that were scaled between 0 to 1 divided by the maximum conductance for the respective test cycles according to the following equation:

$$Y = \frac{G_{100} - G_0}{G_{max}} \tag{7.2}$$

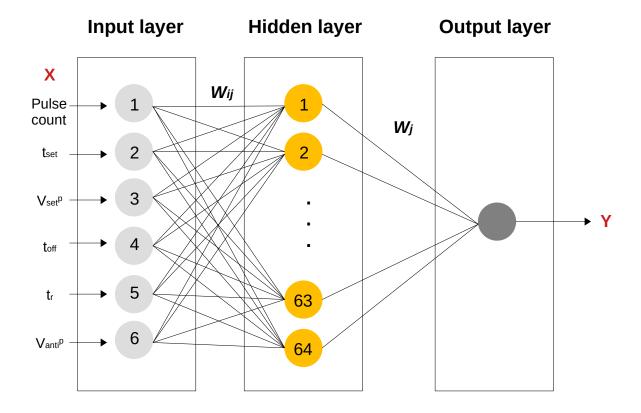


Figure 7.14: The architecture of the used NN. Six input features (X) are in the input layer, 64 neurons are in the hidden layer, and one neuron is in the output layer. W_{ij} and W_j represent the weights between neurons in the Input layer-Hidden layer and the Hidden layer-Output layer, respectively (i=1, 2, ..., 6 and i= 1, 2, ..., 64).

Here, the G_{100} , the G_0 , and the G_{max} are the conductance measured at the 100th pulse count, the initially measured conductance before applying switching voltage pulses, and the maximum conductance value, respectively. A total of 26,600 sets of data were split into a 3:1:1 ratio for the training, validation, and test [Bah17]. Those datasets are used for training, evaluation, and test, respectively.

Training: In the training, the *Adaptive Moment Estimation* optimization algorithm was used (see ch.2.3.2). To train the model, the epochs were 100, which means 100 times iterative training cycles. The trained model is simultaneously evaluated using the validation dataset after every epoch. The evaluation of the model (loss function) was conducted using the *mean squared error* algorithm (see ch.2.3.2). As shown in Figure 7.15(a), the training loss and the validation loss were decreasing with increasing training iteration (epoch) at the learning rate of 1e-4. At the same time, the two *loss* values fit each other closely, and they are stabilized at a certain low point (1.6%) and 1.3% for the training loss and the validation loss, respectively), which indicates a well-trained model [bae10].

Test: A set of X (SET voltage of 2.2 V, anti-pulse of -0.7 V, and all the pulse widths of 0.5 s) was randomly chosen among the test dataset, and the pulse parameters were fed to the trained model. Figure 7.15(b) shows the experimental result for the selected set of X and the predicted conductance values generated by the trained model. The prediction presented an almost identical trend in conductance update at the corresponding pulse number.

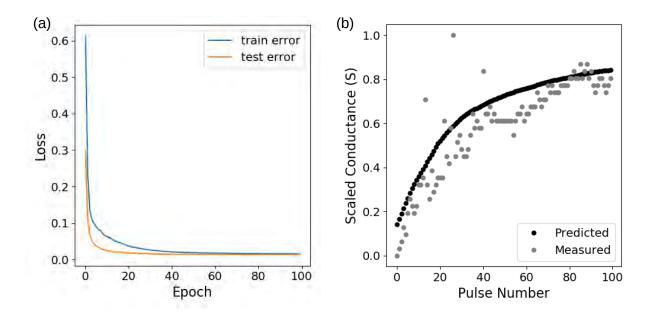


Figure 7.15: (a) Training loss (train error) and the validation loss (test error) as a function of epoch. (b) The predicted trend in the CL generated by the trained model and the Y values corresponding to the chosen X are compared. *Predicted* and *Measured* represent the predicted and the measured (and scaled using Equation 7.2) conductance values, respectively.

8 Conclusion and Outlook

The research aimed at finding methodologies to tailor resistive switching (RS) characteristics in metal-oxide-based-memristive devices toward specific applications for neuromorphic computing. Three metal oxide films (TiO_x , HfO_x , and AlO_x) were deposited via DC magnetron sputtering. By using the optimal flow of reactive gas, HfO_x and TiO_2 obtained desirable material properties for unipolar and bipolar RS operations, respectively. Using TiO_2 -based devices, the impacts of interface layers and metal electrodes on RS were investigated. When using Al as electrodes, an AlO_x layer was induced at the interface with TiO_2 , creating a bilayer oxide system. As a result, stable RS characteristics were obtained, compared to devices using TiN and Au as electrodes. Furthermore, the TiO_2/Au configuration featured currents scaling with device area, in contrast to the filamentary-type devices. This feature can minimize switching variability.

An interface-type device, which is characterized by a lower RS variance than the filamentary-type, was realized using a TiO_x/HfO_x bilayer oxide system. The interface effects were on account of a high Schottky barrier formed at the HfO_x/Au interface. By controlling plasma conditions via the rotation of the substrate holder, the HfO_x films in the bilayer oxide stack obtained desirable material properties for filamentary-type RS. Furthermore, via systematic experiment design and statistical analysis, it was found that:

- the thickness of the HfO_x is a critical factor to determine the electroforming voltage and variability in the filamentary-type devices
- device area is a critical factor to determine the rectifying ratio in the interface-type devices

Based on the bilayer devices¹, one-transistor-one-memristor cells were realized. However, further optimization is required to establish transistor-memristor compatibility.

By adding an AlO_x layer to the bilayer oxide system, the TiO_x/AlO_x/HfO_x-based memristive devices showed advantageous electrical features for use in neuromorphic hardware, such as electroforming-free and compliance-free switching as well as long retention. Moreover, the stoichiometry of the HfO_x layer was further modified in the trilayer oxide system, which improved retention time. Our conclusion from experiments and numerical simulation of these devices are:

- stoichiometry of the HfO_x determines the concentration of mobile oxygen ions in the HfO_x layer
- the redox process at the AlO_x/HfO_x plays an important role in the RS operations

Based on the trilayer devices¹, crossbar structures with high yield and low variability were realized. Sufficient endurance, retention, and selectability for neuromorphic applications were observed. Pathways to further optimization were shown and discussed.

Finally, two methods to tailor analog switching for efficient neuromorphic applications were demonstrated. The first method was based on the design of the oxide layer stacks. In the $TiO_x/AlO_x/HfO_x$ stack and TiO_x/HfO_x stack, successful analog switching was achieved by using repetitive identical pulse signals and increasing/decreasing voltage pulses, respectively. The second method was using designed pulse waveforms with the TiO_x/HfO_x devices. A successful analog switching was obtained when using anti-pulse designs. The data from experiments were further analyzed via a machine learning algorithm. The predictions by the well-trained model showed good agreement with experiment results.

¹The stoichiometry of HfO_x films was x = 1.98 which was sputtered using the rotation mode (see ch.4.3)

In conclusion, a comprehensive study of multilayer metal-oxide-based-memristive devices was conducted to bridge the gap between material designs and RS characteristics. The study allowed establishing methodologies for tailoring RS characteristics, which include designing oxide properties, designing multilayer stacks, and optimizing operating parameters. Furthermore, tailored devices were successfully integrated into systems with a high production yield. Yet, challenges remain in implementing efficient neural networks using the developed systems. The challenges should be tackled in two aspects simultaneously i) optimizing RS properties in single devices, employing the established tailoring methodologies in this thesis; and ii) designing training procedures to compensate for the crossbar non-idealities in terms of variability, retention, etc.

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List of Acronyms

RS resistive switching	4
I-V Current-Voltage	4
EF electroforming	4
HRS high resistance state	5
LRS low resistance state	4
VCM valence Change Memory	6
TMO Transition Metal Oxide	6
CF conductive filament	6
TCM Thermochemical Memory	7
ECM Electrochemical metallization memory	7
DNN Deep Neural Network	8
CMOS Complementary metal-oxide-semiconductor	10
IQR interquartile range	15
RSD relative standard deviation	15
CV coefficient of variation	15
QCD quartile coefficient of dispersion	15
PDF probability density function	15

Bibliography

CDF cumulative distribution function	16
SE spectroscopic ellipsometry	22
XPS X-ray photoelectron spectroscopy	23
XRD X-ray diffraction	23
AFM Atomic force microscopy	23
FWHM full width at half maximum	33
RMS root mean square roughness of surface	34
MO metal oxide	40
BE bottom electrode	41
TE top electrode	41
CRA crossbar array	72
ALD atomic layer deposition	74
NLF nonlinearity factor	78
CL conductance linearity	76
NL nonlinearity	94
NN multilayer percentron neural network model	99

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Declaration

I certify that I prepared the submitted thesis independently without undue assistance of a third party and without the use of others than the indicated aids. Data and concepts directly or indirectly taken over from other sources have been marked stating the sources. When selecting and evaluating the following materials, the persons listed below helped me in the way described respectively:

• Prof. Dr. rer. nat .habil. Martin Ziegler; Interpretation of the results of the entire work

Further persons were not involved in the content-material-related preparation of the thesis submitted. In particular, I have not used the assistance against payment offered by consultancies or placing services (doctoral consultants or other persons). I did not pay any money to persons directly or indirectly for work or services which are related to the content of the thesis submitted. So far the thesis have not been submitted identically or similarly to an examination office in Germany or abroad. I have been notified that any incorrectness in the submitted above mentioned declaration is assessed as attempt to deceive and, according to § 7 para. 10 of the PhD regulations, this leads to a discontinuation of the doctoral procedure.

Dresden, 16. June 2022, **Seongae Park**