High-Bandwidth Voltage-Controlled Oscillator based architectures for Analog-to-Digital Conversion

by

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List of publications

Journal papers

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- L. M. Alvero-Gonzalez, G. Gielen, and E. Gutierrez, "Linearized delay cell for Current-Controlled Oscillator-based Analog-to-Digital Conversion," submitted to *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2022.

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Conference papers

- L. M. Alvero-Gonzalez, E. Gutierrez and L. Hernandez, "A Highly Linear Ring Oscillator for VCO-based ADCs in 65-nm CMOS," *2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Bordeaux, France, 2018, pp. 465-468, doi: 10.1109/ICECS.2018.8617839.

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- L. M. Alvero-Gonzalez, L. Hernandez Corporales and E. Gutierrez, "High-Speed and Energy-Efficient Ring-Oscillator for Analog-to-Digital Conversion," *2020 XXXV Conference on Design of Circuits and Integrated Systems (DCIS)*, Segovia, Spain, 2020, pp. 1-5, doi: 10.1109/DCIS51330.2020.9268623.

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- E. Gutierrez, L. M. Alvero-Gonzalez, L. Hernandez and P. Rombouts, "VCO-ADCs with a Quadrature Band-Pass Noise-Transfer-Function," *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan, 2019, pp. 1-5, doi: 10.1109/ISCAS.2019.8702590.
- L. M. Alvero-Gonzalez and E. Gutierrez, "Nyquist VCO-based ADC with Programmable Pulse Shaping Filter for Mitigation of Blockers," *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, Texas, United States, 2022 (available online soon through IEEE Explore Website).

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Other research contributions

- V. Medina, L. M. Alvero-Gonzalez, E. Gutierrez, S. Paton and L. Hernandez, "Continuous Time Sigma-Delta Modulator with VCO-based integrators and optimized NTF zeros," *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Genoa, Italy, 2019, pp. 470-473, doi: 10.1109/ICECS46596.2019.8964936.
- R. Garvi, L. M. Alvero-Gonzalez, C. Perez, E. Gutierrez and L. Hernandez, "VCO-ADC Linearization by Switched Capacitor Frequency-to-Current Conversion," *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, Seville, Spain, 2020, pp. 1-5, doi: 10.1109/ISCAS45731.2020.9180397.
- E. Gutierrez, L. M. Alvero-Gonzalez and G. Gielen, "All-digital Pulse-shaping-based 11-dB Flicker Noise Reduction Technique in 65-nm VCO-based ADC with minimun-sized Ring OScillator," submitted for *2023 International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA. (pending approval)

Abstract

The purpose of this thesis is the proposal and implementation of data conversion open-loop architectures based on voltage-controlled oscillators (VCOs) built with ring oscillators (RO-based ADCs), suitable for highly digital designs, scalable to the newest complementary metal-oxide-semiconductor (CMOS) nodes.

The scaling of the design technologies into the nanometer range imposes the reduction of the supply voltage towards small and power-efficient architectures, leading to lower voltage overhead of the transistors. Additionally, phenomena like a lower intrinsic gain, inherent noise, and parasitic effects (mismatch between devices and PVT variations) make the design of classic structures for ADCs more challenging. In recent years, time-encoded A/D conversion has gained relevant popularity due to the possibility of being implemented with mostly digital structures. Within this trend, VCOs designed with ring oscillator based topologies have emerged as promising candidates for the conception of new digitization techniques.

RO-based data converters show excellent scalability and sensitivity, apart from some other desirable properties, such as inherent quantization noise shaping and implicit anti-aliasing filtering. However, their nonlinearity and the limited time delay achievable in a simple NOT gate drastically limits the resolution of the converter, especially if we focus on wide-band A/D conversion. This thesis proposes new ways to alleviate these issues.

Firstly, circuit-based techniques to compensate for the nonlinearity of the ring oscillator are proposed and compared to equivalent state-of-the-art solutions. The proposals are designed and simulated in a 65-nm CMOS node for open-loop RO-based ADC architectures. One of the techniques is also validated experimentally through a prototype. Secondly, new ways to artificially increase the effective oscillation frequency are introduced and validated by simulations. Finally, new approaches to shape the quantization noise and filter the output spectrum of a RO-based ADC are proposed theoretically. In particular, a quadrature RO-based band-pass ADC and a power-efficient Nyquist A/D converter are proposed and validated by simulations.

All the techniques proposed in this work are especially devoted for high-bandwidth applications, such as Internet-of-Things (IoT) nodes or maximally digital radio receivers. Nevertheless, their field of application is not restricted to them, and could be extended to others like biomedical instrumentation or sensing.

Resumen

El propósito de esta tesis doctoral es la propuesta y la implementación de arquitecturas de conversión de datos basadas en osciladores en anillos, compatibles con diseños mayoritariamente digitales, escalables en los procesos CMOS de fabricación más modernos donde las estructuras digitales se ven favorecidas.

La miniaturización de las tecnologías CMOS de diseño lleva consigo la reducción de la tensión de alimentación para el desarrollo de arquitecturas pequeñas y eficientes en potencia. Esto reduce significativamente la disponibilidad de tensión para saturar transistores, lo que añadido a una ganancia cada vez menor de los mismos, ruido y efectos parásitos como el "mismatch" y las variaciones de proceso, tensión y temperatura han llevado a que sea cada vez más complejo el diseño de estructuras analógicas eficientes. Durante los últimos años la conversión A/D basada en codificación temporal ha ganado gran popularidad dado que permite la implementación de estructuras mayoritariamente digitales. Como parte de esta evolución, los osciladores controlados por tensión diseñados con topologías de oscilador en anillo han surgido como un candidato prometedor para la concepción de nuevas técnicas de digitalización.

Los convertidores de datos basados en osciladores en anillo son extremadamente sensibles (variación de frecuencia con respecto a la señal de entrada) así como escalables, además de otras propiedades muy atractivas, como el conformado espectral de ruido de cuantificación y el filtrado "anti-aliasing". Sin embargo, su respuesta no lineal y el limitado tiempo de retraso alcanzable por una compuerta NOT restringen la resolución del conversor, especialmente para conversión A/D en aplicaciones de elevado ancho de banda. Esta tesis doctoral propone nuevas técnicas para aliviar este tipo de problemas.

En primer lugar, se proponen técnicas basadas en circuito para compensar el efecto de la no linealidad en los osciladores en anillo, y se comparan con soluciones equivalentes ya publicadas. Las propuestas se diseñan y simulan en tecnología CMOS de 65 nm para arquitecturas en lazo abierto. Una de estas técnicas presentadas es también validada experimentalmente a través de un prototipo. En segundo lugar, se introducen y validan por simulación varias formas de incrementar artificialmente la frecuencia de oscilación efectiva. Para finalizar, se proponen teóricamente dos enfoques para configurar nuevas formas de conformación del ruido de cuantificación y filtrado del espectro de salida de los datos digitales. En particular, son propuestos y validados por simulación un ADC pasobanda en cuadratura de fase y un ADC de Nyquist de gran eficiencia en potencia.

Todas las técnicas propuestas en este trabajo están destinadas especialmente para aplicaciones de alto ancho de banda, tales como módulos para el Internet de las cosas o receptores de radiofrecuencia mayoritariamente digitales. A pesar de ello, son extrapolables también a otros campos como el de la instrumentación biomédica o el de la medición de señales mediante sensores.

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List of Abbreviations

ADC	**A**nalog-to-**D**igital **C**onverter/**C**onversion
BW	**B**and**w**idth
CCO	**C**urrent-**C**ontrolled **O**scillator
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
CTDSM	**C**ontinuous-**T**ime **D**elta-**S**igma **M**odulator
DAC	**D**igital-to-**A**nalog **C**onverter/**C**onversion
DCO	**D**igitally-**C**ontrolled **O**scillator
ENOB	**E**ffective **N**umber **o**f **B**its
FIR	**F**inite **I**mpulse **R**esponse
FoM	**F**igure-**o**f-**M**erits
IC	**I**ntegrated **C**ircuit
IoT	**I**nternet-**o**f-**T**hing
LS	**L**evel-**S**hifter
MASH	**M**ulti-**S**tage Noise **SH**aping
MDAC	**M**ultiplying **D**igital-to-**A**nalog **C**onverter
NS	**N**oise-**S**haping
NTF	**N**oise-**T**ransfer-**Function**
opamp	**op**erational **amp**lifier
OSR	**O**versampling **R**atio
PCB	**P**rinted **C**ircuit **B**oard
PFM	**P**ulse **F**requency **M**odulation/**M**odulator
PSD	**P**ower **S**pectral **D**ensity
PVT	**P**rocess **V**oltage **T**emperature
RO	**R**ing **O**scillator
SAR	**S**uccessive **A**pproximation **R**egister
SINAD	**Si**gnal-to-**N**oise **a**nd **D**istortion Ratio
SNDR	**S**ignal-to-**N**oise and **D**istortion **R**atio
SNR	**S**ignal-to-**N**oise **R**atio
SQNR	**S**ignal-to-**Q**uantization **N**oise **R**atio
STF	**S**ignal-**T**ransfer-**F**unction
T2B	**T**ermometer-**to**-**B**inary
THD	**T**otal **H**armonic **D**istortion
TI	**T**ime-**I**nterleaved
VCO	**V**oltage-**C**ontrolled **O**scillator
VLSI	**V**ery **L**arge-**S**cale **I**ntegration

Chapter 1

Introduction

1.1 Context and motivation

Today, continuous interaction with the physical environment is becoming increasingly important to provide a better quality of life and demands optimal communications and sensor systems. Actions like checking with the mobile phone the number of steps per day or the activity during sleep, looking for a restaurant with our favorite food, receiving an alert message or calling from our watch while running are some of the more common activities of our daily routine. In such scenario, the network of smart electronics devices needs a highly energy-efficient interface between the analog physical world and the digital world with high energy efficiency, especially in portable battery-dependent devices. Additionally, these systems must be small and cheap while maintaining robustness and enough resolution.

All the physical magnitudes from the surrounding world like humidity, temperature, or pressure, to name a few, are represented by analog electrical signals. This analog data defined in an infinitive range of amplitudes in time needs to be transformed into digital data compatible with the evolving digital world. The bridge between analog and digital worlds is performed by data converters: analog-to-digital and digital-to-analog converters (ADCs and DACs).

The evolution of complementary metal-oxide-semiconductor (CMOS) technology into modern deep submicron nodes has led to a better performance of digital circuits. The scaling down of the CMOS processes supposes the reduction of the voltage supply and the size of the transistors, in order to decrease the power consumption and allow a higher number of devices on an integrated circuit (IC). Due to its scalability property digital circuits take advantage of this miniaturization process offering benefits such as higher operation speed, smaller silicon occupied area and power savings. However, the design of analog circuits has become complex. Devices in narrow processes with a low voltage headroom lack enough intrinsic gain, and their performance is strongly affected by mismatch, higher noise impact, and parasitic effects [1], [2].

In consequence, the current trend is towards mostly digital implementations, imposing a new paradigm in the field of data converters, typically implemented with mixed signal blocks, where opamps, comparators and DACs are still needed.

Voltage-controlled oscillator (VCO)-based ADCs implemented with ring oscillators (ROs) have emerged as a promising solution due to their highly digital nature adequate for very low voltage supplies, scalable designs and excellent sensitivity [3]–[5]. Diverse hybrid data converter structures with VCOs have been published: with VCOs as integrators/ quantizers in Continuous Time Delta Sigma Modulators (CTDSMs) [6]–[11], placing it into SAR-based structures for pipeline ADCs [12]–[15] or in multi-stage noise shaping (MASH) architectures [16]–[19]. If we look for simplicity, they are of special interest within an open-loop configuration [20]–[22], where the spectral properties of pulse frequency modulation enable first-order noise-shaped output data, with a performance similar to CTDSMs [23]. The main impairment is the nonlinear voltage-to-frequency response of the ring oscillator. This relation strongly limits the resolution we may get from the whole converter [24] restricting it to 7-8 Effective Number Of Bits (ENOBs) for 100 mV_{pp} input voltages. Several ways of correcting the RO nonlinearity have been proposed in the literature. Firstly, we may use digital calibration [20], [25], but higher power consumption and higher area are required for calibration circuits. Secondly, we may think of a VCO-based $\Delta\Sigma$ loop [26], where the nonlinearity is corrected by the gain of the loop. Here the limitation is the requirement of analog circuits and the partial loss of the digital nature of the VCO-based solution. Recently some of the proposals are headed towards limiting the amplitude of the VCO input signal [27], [28]. If the input signal is of low amplitude, the voltage-to-frequency relation approximates better to a linear function, resulting in less distortion. Nevertheless, if the input signal amplitude is limited the ring oscillator frequency sweep will be limited as well. Consequently, the final resolution of the converter will be constrained, restricting this solution to high and medium oversampling ratio (OSR) applications [23].

Some works have been focused on the use of open-loop VCO-based ADCs for wide-band data conversion with low OSR [29], [30]. The highest achievable resolution depends on the minimum delay time available to discriminate between two different events, which in the simplest structure is the propagation delay of a NOT gate. In literature some techniques to "artificially" increase the highest achievable resolution have been proposed. In [31], a modified differential delay cell is used to increase the oscillation frequency of the ring oscillator. The modified cell consists of changing the connection of the traditional cross-coupled NOT gates to performed feed-forwards that pre-charge the outputs of the next cell in the ring oscillator. The ratio of the main and auxiliary NOT gates must be correctly selected to maximize the oscillation frequency without incurring a power consumption penalty. [32] presents an oversampling stochastic VCO-based ADC wherein the final resolution is improved by leveraging inherently uncorrelated quantization errors of multiple VCO-based quantizers in parallel. The idea exploits the simplicity and high scalability of open-loop structures but does not

offer a power-efficient solution. Recently, the relationship between the pulse frequency modulation (PFM) and the VCO-based data conversion has been proposed and analyzed in detail [23], setting new fundamental Signal-to-Noise Ratio (SNR) limits and giving new opportunities to enhance the performance of open-loop VCO-based architectures in power, area and resolutions.

1.2 Scope of the dissertation

The aim of this dissertation is the design and implementation of data conversion architectures with open-loop configuration using ring oscillators. Firstly, some basic concepts of the data conversion are targeted for a general characterization. Secondly, the time encoding technique is described as the core of this work. Then, several ideas are proposed to tackle VCO-based ADCs issues like distortion and limited frequency from the oscillator, which restrict the achievable resolution of the converter. Starting from the foundations described in [23] novel data converter architectures are also proposed in this document for wide-band communication applications; resulting in a quadrature band-pass structure and a Nyquist-rate ADC robust against external interferences. The proposals are specially oriented to meet the requirements of new communication protocols for wide-band applications [33], although their field of apllication can be extended to others fields such as biomedical instrumentation of medium-bandwidth sensing.

The objectives of the research are the following:

- Studying the nonlinear behavior of a ring oscillator and its influence in the performance of open-loop VCO-based ADCs resolution, and proposing and validating with simulations new techniques to minimize the resulting distortion at the output data.
- Validating experimentally one of the techniques in the previous point with a prototype implemented in 65-nm CMOS process.
- Analyzing the effect of the technology speed on the minimum inversion cell delay and the VCO oscillation output, and proposing and validating with simulations techniques to deal with the limited achievable resolution of the converter.
- Proposing new architectures using the recent PFM-based interpretation of VCO-based ADCs for maximally digital radio-receivers.
- Comparing the results to the state-of-the-art in terms of area, power consumption, bandwidth and resolution, showing figure-of-merits (FoM) of the proposed architectures and techniques.

1.3 Organization of the document

This dissertation is divided into five chapters: Chapter 2 contains the basic theory under the operation of ADCs, the most conventional structures used for the implementation of ADCs, and a detailed description of the foundations of VCO-based ADCs; Chapter 3, 4, and 5 describe the proposals, designs and implementations of this research work; and Chapter 6 summarizes the results and possible future research lines.

Chapter 2: Background on Analog-to-Digital Conversion and RO-based ADCs.

This chapter provides an introduction to data conversion: basic concepts about the digitization process, types of ADCs, the differences between Nyquist-rate and oversampled ADC architectures, a general description of $\Delta\Sigma$ Modulation as a starting point to understand spectral performance of VCO-based ADC, and how to use RO-based VCO for data conversion systems.

Chapter 3: Circuit-based techniques for linearity correction of open-loop RO-based ADCs.

A new delay cell for linear RO-based current-controlled oscillators (CCO) is introduced in the first part of this chapter. The proposed circuit structure offer an approximate linear current-to-frequency response, ensuring that the modulated delay of the output phases is linearly proportional to the current that feeds the ring oscillator. The cell structure uses three inversion stages: the first one connected to a voltage-controlled current source and the two others connected to a fixed voltage. Thus, level-shifter circuits are not required to saturate the output phases to a voltage level compatible with the digital circuitry afterwards, saving power. A prototype with a 5-stage CCO with the proposed cell delay is implemented in a 65-nm CMOS technology. The measurement results shows an excellent performance in terms of power and a proper linearity behavior. **Validation with 65-nm prototype.**

In the second part, another circuit-based approach to reduce the distortion open-loop RO-based ADC is proposed. The idea consists of using a front-end circuit with multiple transconductors to drive the current into the RO implementing the inverse current-to-frequency curve of a CCO. The approach linearizes the RO transfer function and provides great attenuation of the harmonic terms while keeping similar parameters of area and power compared to the conventional architecture with a single transconductor. Validation with simulations.

Chapter 4: Resolution enhancement of RO-based ADCs for high-bandwidth applications.

Firstly, interpolation and injection techniques are combined in order to increase the number of effective bits of a RO-based ADC without modifying the oscillation frequency. The presented method employs a resistive network to passively obtain an interpolated phase between two consecutive phases of a ring oscillator and inject that new phase into another identical ring oscillator. This way, the propagation delay of the VCO stages is artificially halved, doubling the effective oscillation frequency of the system. Validation with simulations.

Secondly, a new ring oscillator circuit wherein the transconductance and the inversion stages are embedded into the same delay stage. Every cell comprises two devices: one transistor driven by the input modulating signal and another one connected to the previous output phase. The new topology shows a higher oscillation frequency than the conventional configuration and better power performance operating at the same conditions if a reduced number of taps is employed to build the ring oscillator. Validation with simulations.

Chapter 5: Programmable digital pulse shaping filters for RO-based ADCs.

The first part presents a quadrature band-pass RO-based ADC. The architecture uses the equivalence between a RO as a signal encoder and a PFM. By designing a customized pulse shaping filter to shift the band of interest to middle frequencies, a quadrature band-pass noise transfer function (NTF) is implemented. Validation with simulations.

In the second part, a power-efficient Nyquist RO-based ADC robust against blockers is proposed. In this case, the pulse shaping filter is customized to remove interferences by placing the nulls at certain frequencies. At the same time, a high attenuation of the modulation components is achieved, leading to the same performance of an oversampled ADC but avoiding the implementation of the decimation filter. Validation with simulations.

The solutions proposed in this chapter are completely digital because the pulse shaping filter is adjusted by software through pre-loaded values in LUTs located at the back-end, whose input index is also calculated by means of digital structures. Due to the back-end LUT for both solutions, a single front-end circuit can be shared by several digitization channels, making possible multichannel reception in all-digital radio-receivers.

Chapter 6: Conclusion and future work

This chapter draws the conclusions, summarizes the contributions of this dissertation, and discusses some activities to improve and extend the presented work in the future.

Finally, Appendixes A and B comprise some mathematical details of Chapter 3 and 5.

Chapter 2

Background on Analog-to-Digital Conversion and RO-based ADCs

2.1 Analog-to-digital conversion overview

Analog-to-digital converters (ADCs) serve as a bridge between the analog quantities from the physical world and the digital systems employed in information processing, storing and data transmission. The basic operation of an ADC can be split into four main functions, as illustrated in the diagram of Figure 2.1.

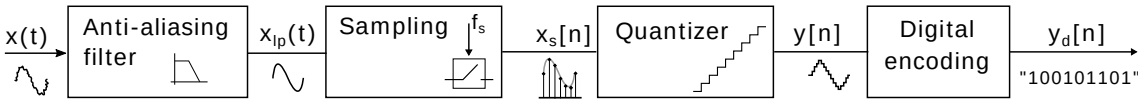


FIGURE 2.1: A generic A/D conversion block diagram.

The anti-aliasing filter, typically a low pass filter, removes all the frequency components out of the interest band of the input signal (bandwidth, BW) so that the replicas of the spectrum do not interfere with each other when sampling, phenomenon called aliasing. The purpose of a sampler is transforming a continuous-time signal into a discrete-time signal with the sampled data equivalent value. During this process the spectrum is replicated at sampling rate (f_s) and its multiples. The sampled analog level is assigned to a discrete amplitude by means of the quantizer block. After the quantization process the output data is digitally processed to be used. The diagram of Figure 2.1 essentially represents the basic ADC operation. Consequently some other additional blocks may be needed depending on the architecture. In some cases, the input signal of the quantizer is a discrete wave and the conversion is performed in the discrete-time domain. In Figure 2.1, a sample and hold (S&H) block before the quantizer holds the analog value throughout the sampling rate for the next quantization process. In other cases, the analog input of the quantizer is a continuous signal and the quantization is performed in the continuous-time domain. The sampler block in Figure 2.1 comes after the quantizer or is often involved in the quantization process itself.

2.1.1 A/D conversion techniques

To provide an overview and a better understanding of ADCs the most relevant techniques for data conversion will be next described, putting in context the best candidates in the emerging technologies. Flash ADCs are usually implemented for high-speed A/D conversion [34]. However, the power consumption increases exponentially with the number of bits, making them less power-efficient for more than 10 ENOBs [35]. Additionally, they are extremely sensitive to mismatch phenomena when implemented with minimum-size devices. Thus, they are not scalable. To minimize this impact, devices' dimensions are often increased at the cost of a larger occupied area and higher power consumption [36], [37].

Successive Approximation Register (SAR) ADCs are low-power, simple, and friendly digital architectures. They are more energy-efficient than Flash-based architectures due to their mostly-digital implementation [38], [39]. Nevertheless, their sampling rate is limited by the need for a high-speed clock for the control logic [34], limiting their use for medium bandwidth and leading to dramatically high-power solutions when used for MHz-bandwidths [40]–[43].

Pipeline ADCs divide the A/D high-resolution conversion operation into several low-resolution conversion stages operating sequentially, showing a proper balance between accuracy and operation speed. The drawback of this kind of ADCs is the high-performance operational amplifier (opamp) mandated by a multiplying digital-to-analog converter (MDAC) [34]. This block consumes a large amount of power, reducing the power efficiency, and entails challenging designs in deep submicron CMOS nodes [33], [44].

Time-interleaved (TI) architectures combine low-speed ADCs connected in parallel and sampled with uniformly distributed different phases from a single clock signal to achieve a high sampling rate and high energy efficiency [34]. SAR, Flash, and pipeline ADCs are commonly used in TI-based structures. However, mismatch phenomena among the channels significantly degrade the resolution. To alleviate this issue, calibration circuits are needed, which require extra power consumption and increase the system complexity [45], [46].

Continuous-Time Delta-Sigma Modulator (CT$\Delta\Sigma$M) ADCs have also been reported for wide-band A/D conversion [47], but some key points such as the analog nature of the filter loop, the excess loop delay, and the clock jitter increase the complexity design especially with narrow processes nodes. Noise-Shaping SAR (NS-SAR) structures combined with time-interleaving techniques remove the need for analog circuits, relaxing technology scaling requirements and enabling high-bandwidth conversion with lower power consumption [48], [49].

The state-of-the-art A/D conversion is currently dominated by these three techniques: Pipeline, SAR and $\Delta\Sigma$ Modulators. The latter cover the widest conversion region and may apply to many different applications, from low-power wearable biomedical devices to wide-band wireless communications. For the

new nanometer technologies, one approach that makes highly-digital implementations feasible, exploiting scalability and low operation voltages with a very limited power budget, is time-encoded conversion where the information is encoded in time events instead of amplitude. VCOs play a major role in this kind of architectures, particularly if they are implemented with ring oscillators [24], [25]. The output of these structures is a signal whose frequency varies according the amplitude changes in the input.

2.1.2 Nyquist-rate and overampled ADCs

ADCs are mainly classified into two categories according the relationship between BW and the sampling frequency f_s: Nyquist-rate and oversampled converters. In the first category, the input signal can be sampled as low as twice the highest frequency component, f_s >2BW. In practice, a sampling rate somewhat higher than 2BW (Nyquist rate) is usually necessary. That condition is established by Nyquist-Shannon sampling theorem to avoid aliasing within BW of the captured information with f_s. In Nyquist-rate converters there is an output sample for each input sample, and every those input samples are individually processed. The accuracy of conversion can be evaluated by comparing the discrete quantized output and the analog input.

The input amplitude range is divided into a number of quantization intervals or steps (M) which represents a given analog value. For an input range x_{FS}, the amplitude of each quantization step or least-significant bit (LSB) is given by

$$LSB = \frac{x_{\max} - x_{\min}}{M} = \frac{x_{FS}}{M} = \frac{x_{FS}}{2^N}, \tag{2.1}$$

where N is the number of bits of the quantizer required to the number of quantization intervals M being a power of 2 for a digital binary code.

Therefore, the quantized output does not correspond exactly to the analog input value, and this process leads to the quantization error, ϵ_q. Considering an ideal A/D conversion with infinitive quantization steps, which is unfeasible in practice, ϵ_q becomes zero. The effect of this noise is theoretically quantified by the signal-to-noise ratio (SNR or signal-to-quantization noise ratio-SQNR) defined as:

$$SNR(dB) = 10\log_{10}\frac{P_{sig}}{P_{noise}} = 20\log_{10}\frac{Vrms_{sig}}{Vrms_{noise}} \tag{2.2}$$

where V_{RMS} is the root mean square value or effective value.

A common measure of a converter's accuracy is the SNR assuming a single sine-wave input. By estimating the power of ϵ_q the SNR value can be calculated.

The time average power and V_{RMS} of ϵ_q over the Nyquist bandwidth ($f_s/2$) are given by:

$$\begin{aligned} P\epsilon_{\mathrm{q}} &= \frac{LSB^2}{12} \\ Vrms_{\mathrm{noise}} &= \frac{LSB}{\sqrt{12}}. \end{aligned} \tag{2.3}$$

The power and V_{RMS} of a full-scale input sine-wave with amplitude V_{peak} = $x_{FS}/2$ are expressed as follows:

$$\begin{aligned} P_{\mathrm{sine}} = \frac{V_{\mathrm{peak}}^2}{2} &= \frac{\left(LSB \cdot 2^N\right)^2}{8} \\ Vrms_{\mathrm{sine}} = \frac{V_{\mathrm{peak}}}{\sqrt{2}} &= \frac{LSB \cdot 2^N}{2 \cdot \sqrt{2}}. \end{aligned} \tag{2.4}$$

The SNR with a full-scale sine-wave over BW is therefore:

$$SNR(dB) = 6.02 \cdot N + 1.76. \tag{2.5}$$

This SNR calculation only accounts for the quantization noise as a fundamental limit of an ADC. The elements in real circuits bring additional noise components that deteriorate the performance of ADCs like thermal and flicker noise or distortion. The relationship that quantifies the effect of all noise and harmonic distortion over the input signal is now the signal-to-noise and distortion ratio (SNDR or SINAD). The inverse relationship defines the equivalent number of bits (ENOB) or the resolution of the converter, as follows:

$$ENOB = \frac{SNDR - 1.76}{6.02}. \tag{2.6}$$

The SNR term will be used through this first part of the chapter, only considering the effect of ϵ_{q}.

The simplified spectral analysis of the quantization noise leads to equation (2.3) which is accurate enough to approximate the effect of ϵ_{q} on the converter' accuracy [50]. The power spectral density (PSD) of the quantization noise ϵ_{q}, assuming a random signal and uncorrelated with the input signal, is white spread uniformly over the entire Nyquist bandwidth. Then, the quantization process can be described as the addition to the analog input of a noise with a white spectrum that generates the quantized output signal [51], as depicted in Figure 2.2.

Note that in Nyquist-rate converters, BW equals $f_s/2$, and all the integrated quantization noise is inside the band of interest of the converter. Consequently, the SNR for an ideal N-bit Nyquist-rate converter is defined by equation (2.5).

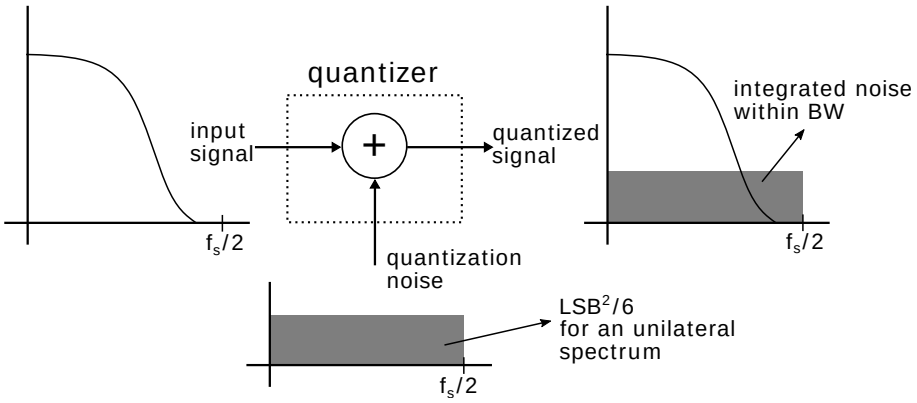


FIGURE 2.2: Linear model of the quantization process by an additive white noise.

In this category of data converters, the performance is often degraded by the matching accuracy of the analog components used in the implementation, which in many cases may restrict the resolution. Additionally, the design of the anti-aliasing filter is critical as it is the first block of the conversion chain and definitely a challenge for a transition band sharper. Increasing f_s the requirement on transition band sharpness is reduced, and hence, the filter complexity.

Oversampled converters use sampling rates much higher than the Nyquist rate, $f_s \gg 2 \cdot BW$, typically by a factor higher than 8. The oversampling rate (OSR) is defined as the ratio between f_s and BW, given by:

$$OSR = \frac{f_s}{2 \cdot BW}. \tag{2.7}$$

Since ϵ_q is measured over the entire Nyquist bandwidth, in oversampled converters the BW is much lower than $f_s/2$ and hence the effect of quantization noise is reduced by the increase of the sampling rate, resulting in a SNR improvement by including into equation (2.5) a factor which depends on OSR:

$$SNR(dB) = 6.02 \cdot N + 1.76 + 10 \log_{10} OSR. \tag{2.8}$$

The resolution limitation of Nyquist-rate converters can be traded off against a higher conversion speed. Differing from Nyquist rate converters, in the oversampled converters there is no one-to-one correspondence between the input and the output samples. Each output depends on the preceding input values, thus the converter's accuracy can be only evaluated by comparing the complete input to the output. Moreover, the implementation of oversampled converters relaxes the accuracy requirements of the analog components compared to Nyquist-rate converters.

The price paid for a high achievable SNR with oversampling includes faster operation and additional digital circuitry, both take advance from the technology downscaling. For instance, a decimation operation after the quantization is needed to decrease f_s to the Nyquist rate, then the data is suitable for storing or transmitting with a sampling rate compatible with the band signal. However, even though the in-band noise decrease with increasing the sample rate, the SNR improvement is relatively slow. The combination of oversampling and quantization noise shaping is the key concept of ΔΣ Modulators in an attempt to reduce further the noise power inside the band of interest [52], [53].

2.2 Basis of Delta-Sigma (ΔΣ) modulation

The ΔΣ ADCs provide a great versatility, cover the largest conversion region of the resolution versus bandwidth plane offering the most efficient solution for a wide variety of applications, including digital telephony, digital audio, wireless and wired communications, medical electronics, and industrial, and scientific instrumentation [54].

ΔΣ Modulation can be applied to either continuous or discrete architectures. The behavior of both approaches is quite similar, and the principles of this technique described in this document are valid for continuous and discrete conversion structures. The simplest diagram of a ΔΣM is depicted in Figure 2.3(a) and consists of a loop that involves an integrator (loop filter), an N-bit quantizer, and a negative feedback path from the output y[n] to the input signal x(t) through a DAC that transforms the digital output into a quantized analog signal. Figure 2.3(b) and Figure 2.3(c) shows the linear equivalent model of a first-order continuous-time (CT) and discrete-time (DT) ΔΣ converter respectively. The quantizer is replaced by an addition operation to incorporate ϵ_q term of the quantization process as previously explained (see Figure 2.2), and H(z) denotes the loop filter.

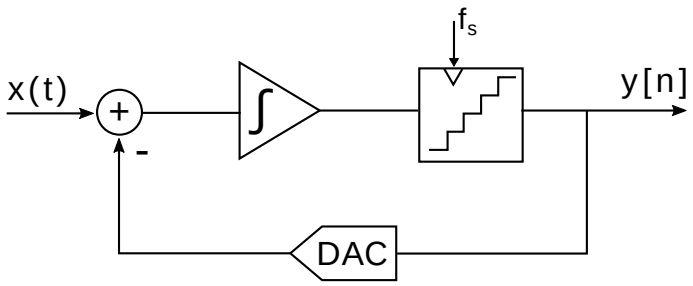
By analyzing the discrete-time model, to simplify the operations, the output of the ΔΣ modulator is developed in the z-domain as follows:

$$Y(z) = [X(z) - Y(z)] \cdot H(z) + \epsilon_q, \tag{2.9}$$

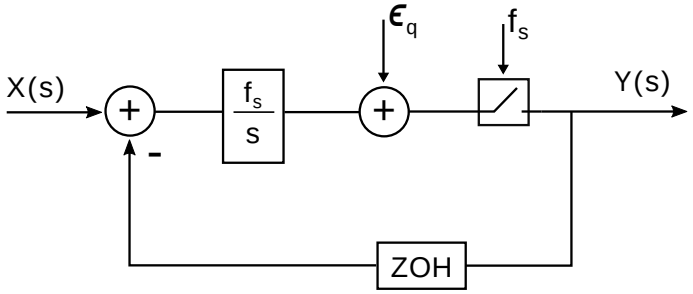
and thus obtain

$$Y(z) = X(z) \cdot \frac{H(z)}{1 + H(z)} + \epsilon_q \cdot \frac{1}{1 + H(z)}.$$

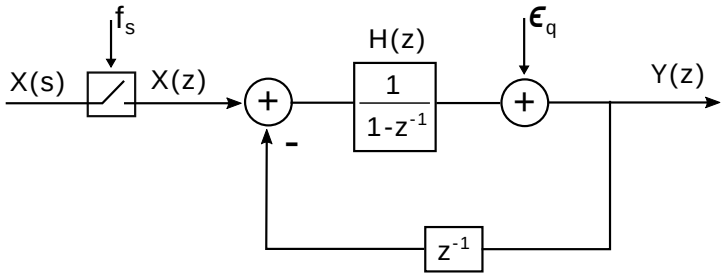
The above equation shows that the signal and the quantization error are differently processed by the modulator. To generalize, it is stated



(a) First-order ΔΣ Modulator structure.



(b) Linear equivalent model of a first-order continuous-time ΔΣ Modulator. ZOH is a zero-order hold.



(c) Linear equivalent model of a first-order discrete-time ΔΣ Modulator.

FIGURE 2.3: Basic diagram of a ΔΣ Modulator.

$$Y(z) = X(z) \cdot STF + \epsilon_q \cdot NTF, \tag{2.10}$$

where STF is the signal transfer function, and NTF is the noise transfer function. To ensure that X(z) passes through the system with no attenuation or changes, Y(z)≈X(z), the STF has to be a unitary gain. On the contrary, the NTF has to filter the quantization noise to reduce its effect on the output. Hence, the STF should be a low pass transfer function, and the NTF should be a high pass transfer function. To achieve those desired responses, the loop filter must be an integrator-type function, H(z)≫1. The delay element in the feedback path of the modulator associated with the DAC delay (see Figure 2.3(b)) is pushed into the forward path

(that only means the delay of the input by one sample), leading to

$$Y(z) = X(z) \cdot z^{-1} + \epsilon_q \cdot \left(1 - z^{-1}\right). \tag{2.11}$$

According to equation (2.11), to digitize the output ϵ_q pass through a function (1-z^{-1})that corresponds to a first-order high-pass filter, allowing noise suppression at low frequencies over a range $f_s/2$ (noise shaping). Then, the maximum SNR of the first-order ΔΣ Modulator is given by:

$$SNR(dB) = 6.02 \cdot N + 1.76 - 5.17 + 30 \log_{10} OSR. \tag{2.12}$$

A way to increase the resolution is using a high-order loop filter. Thus, the in-band noise contribution is reduced more than in the first-order architecture, and the SNR enhanced compared to equation (2.12). The order of the modulator stems from the number of integrators contained in the system. The structure in Figure 2.4 shows a second-order ΔΣ Modulator with an additional integrator and a feedback path. The NTF is now (1-z^{-1})^2, and the maximum SNR of this topology is

$$SNR(dB) = 6.02 \cdot N + 1.76 - 12.9 + 50 \log_{10} OSR. \tag{2.13}$$

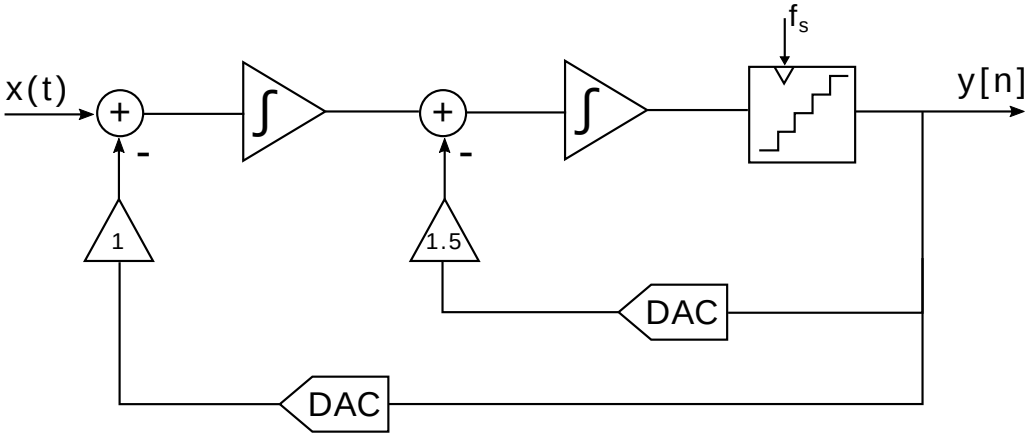


FIGURE 2.4: Second-order ΔΣ Modulator.

In principle, by adding more integrators and feedback branches to a ΔΣ loop resulting in a very high-order noise shaping (NTF = (1-z^{-1})^L), high SNRs can attain for relatively small OSR. However, stability issues are an important point to be considered in high-order architectures and substantially reduce the achievable resolution. MASH topologies are an alternative strategy to overcome the stability

problems [53], [55]. Figure 2.5 shows the magnitude of NTF for different orders ΔΣ modulators and a Nyquist-rate converter [56].

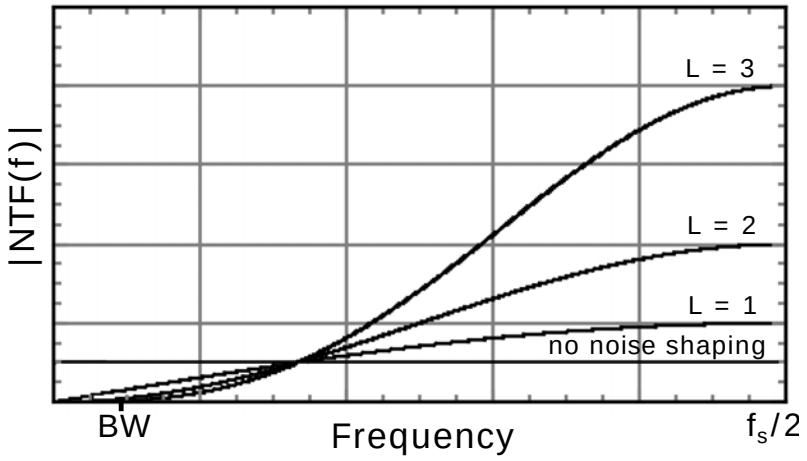


FIGURE 2.5: Magnitude of NTF for different orders ΔΣ Modulator.

Comparing CT and DT ΔΣ architectures, the former ones possess an inherent anti-aliasing filtering function. In Figure 2.3(b) the sampler comes after the quantizer block within the ΔΣ loop (the sampler is embedded into the quantizer in Figure 2.3(a)). Accordingly, the high frequency components of the input signal x(t) are filtered by the integrator (H(z), low-pass transfer function) before the sampling, so the loop filter itself works as anti-aliasing filter. Therefore, the first block of the conversion chain (see Figure 2.1) is unnecessary. Conversely, in the DT ΔΣ Modulator of Figure 2.3(c), the sampler is at the input outside of the loop, so the anti-aliasing filter is still needed. In addition, the implementation of DTΔΣ converters is typically realized with switched-capacitor circuits that requires high-speed DACs and opamps, elements which negatively impact the power dissipation of the architecture. However, DTΔΣM designs offers a lower sensitivity to clock jitter and improve the immunity to excess loop delay.

2.3 RO-based ADC

Nowadays, the progress of very large-scale integration (VLSI) has led to the development of deep-submicron technology. These new CMOS processes have supposed the reduction of the voltage supply and the length of the transistors [57], which entails new challenges for A/D conversion, especially from the analog design perspective. Analog circuits have become increasingly complex to design due to the reduction of the voltage headroom and limited devices' gain, higher noise impact, mismatch, and parasitic effects [1], [58]. On the contrary, digital logic consumes less power, occupies less area, works faster as design processes

get smaller, and is less sensitive to transistor non-desired effects [59]. Thus, the current trend is towards highly digital implementations.

Although the ΔΣ Modulation technique is an attractive solution to classic A/D conversion systems, they are still limited by the main integrator present in the loop, typically implemented with conventional analog blocks such as opamps or transconductors. Last years, time-encoding architectures have appeared as an alternative for the design of high-performance analog ICs [60], [61], by using the input information (voltage or current) to modulate a timing property such as frequency, duty cycle, period, etc [62], [63]. Time-encoding-based systems can be implemented with mostly digital circuitry that takes advantage of the scaling down of CMOS technology.

Within this evolution, ADCs with RO-based VCOs (RO-based ADCs) have emerged as a promising candidate. Under two approaches, this architectures can be analyzed and applied to different systems. On the one hand, RO-based ADCs whose digital output has an intrinsic first-order noise shaping spectral property, making their performance very similar to ΔΣ Modulators but with more digital implementations. In this approach, the RO-based VCO is modeled as a phase integrator which is addressed next. On the other hand, RO-based conversion architectures are derived from the PFM theory [21], [23].

2.3.1 VCO-based phase integrator

A VCO (similarly, CCO) produces a period waveform of duty cycle of 50%, with an instantaneous oscillation frequency which is a function of the input signal voltage (input current in the case of CCO) x(t), as follows:

$$f_{\text{osc}}(t) = f_{\text{o}} + K_{\text{VCO}} \cdot x(t), \tag{2.14}$$

where f_{o} is the rest oscillation frequency, K_{VCO} is the ring oscillator gain expressed in Hz/V, and x(t) is the input voltage centered at zero. Thus, a voltage value (or current) is translated to a frequency encoded information performing a voltage/current-to-frequency conversion. This corresponds to an ideal description of a RO response.

In an attempt to seek a different way to implement an integrator that is not potentially affected by the miniaturization of technology when designing ΔΣ modulators, and considering that the phase is the integral of its frequency, it is found from 2.14 that:

$$\theta(t) = 2\pi \int_0^t f_{\text{osc}}(\tau)\, d\tau = 2\pi f_{\text{o}} t + 2\pi K_{\text{VCO}} \int_0^t x(\tau)\, d\tau, \tag{2.15}$$

where θ(t) is the phase of the VCO output. Then, traditional analog integrators can be replaced by VCOs by reading the VCO output as the phase of the output signal. It is observed that $2\pi f_o$ is a constant term which represents the unmodulated oscillation frequency by the input x(t), therefore it can be considered an offset. According to equation (2.15), a VCO can be modeled as illustrated in Figure 2.6. These structures can be implemented with mostly digital circuits very suitable for new nanometer processes and are detailed below.

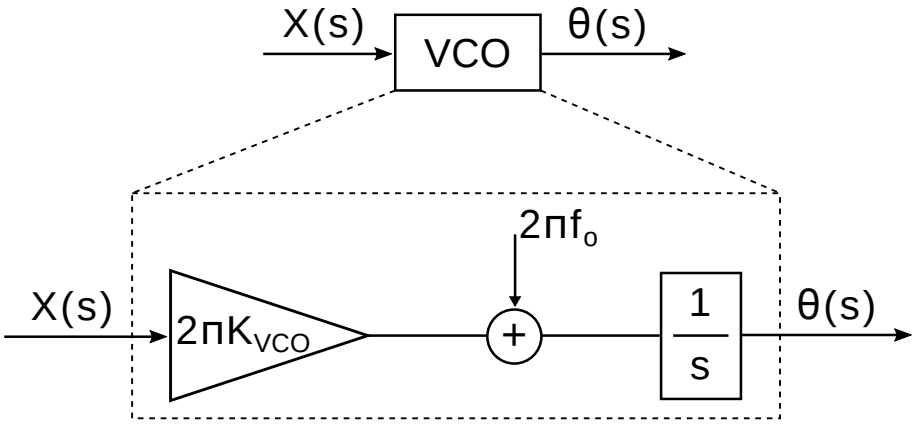


FIGURE 2.6: Linear model of a VCO as a phase integrator.

2.3.1.1 A digital VCO: The Ring Oscillator

Ring oscillators (ROs) have gained popularity inside the designer community as a potential solution to design VCOs due to its digital nature and hardware simplicity [64]. A ring oscillator is realized with a set of an odd number of CMOS inverters, NOT gates, in a closed loop with positive feedback, as depicted Figure 2.7. The output of each stage is connected to the input of the next stage thus inverting and propagating the signal along the ring. Since every stage has an output signal associated, the signal w(t) is a multi-phase output (N).

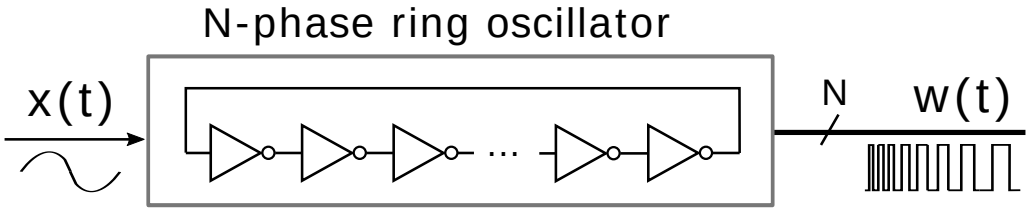


FIGURE 2.7: Ring oscillator-based VCO: a digital integrator implementation.

The oscillation frequency is expressed as:

$$f_{\text{osc}}(t) = \frac{1}{2 \cdot N \cdot \left(t_{\text{phl}} + t_{\text{plh}}\right)} = \frac{1}{2 \cdot N \cdot t_{\text{pd}}(t)}, \tag{2.16}$$

where N is the number of stages in the RO and t_{pd} is the propagation delay of each inverter cell, assuming that the inverters are identical, and the propagation delays corresponding to the high-to-low transition (t_{phl}) and the low-to-high transition (t_{plh}) are equal. During a single oscillation period the inverters switch twice which determines the period of the oscillation being $t_{phl}+t_{plh} = 2 \cdot t_{pd}$ [51]. The delay time $t_{pd}(t)$ depends on the input signal x(t), hence the $f_{osc}(t)$ varies as a function of x(t) as well.

Applying a square pulse with a frequency f_{osc} to the input of a NOT gate, it either feeds a load capacitance (C_L) from supply source (V_{RO}) or sinks the charge stored to ground for each state change. The current (I_{RO}) is defined by the average amount that the NOT gate pulls from V_{RO} when the PMOS device is on. Therefore, the power dissipated is given by:

$$P_{\text{average}} = V_{\text{RO}} \cdot I_{\text{RO}} = {V_{\text{RO}}}^2 \cdot C_{\text{L}} \cdot f_{\text{osc}}. \tag{2.17}$$

The average power dissipated by the NOT gate has a dynamic behavior as a function of f_{osc}. This is the major advantage of the dynamic logic in CMOS circuits that supposes a low power consumption.

That is how a VCO is typically implemented to seize the advantages of narrow design processes, based on a digital implementation using NOT gates as the simplest delay cell circuit [3]. The delay cell can be designed with a single-ended [65] or differential topologies [27], [66], [67]. Single-ended structures show better power dissipation while differential structures exhibit better performance in terms of the supply noise rejection. Different ways to drive the input signal and hence the delay time modulation of each stage can be also applied [68]–[70].

2.3.2 RO-based ADC configurations

In summary, VCOs can be implemented very efficiently using ROs in order to replace conventional analog integrators with simple digital circuits. Consequently, ROs can be incorporated into a $\Delta\Sigma$ modulator to design conversion architectures well-suited for current deep-submicron technologies. Considering the equivalence with the traditional $\Delta\Sigma$ modulator, there are two-kinds of RO-based configurations: open-loop and closed-loop structures.

2.3.2.1 Open-loop structure for RO-based ADCs

Several RO-based ADCs have been published using this kind of configuration such as [24], [66], [71], [72].

The basic open-loop architecture built with a RO-based VCO and its linear equivalent model in the time-domain is depicted in Figure 2.8. In this configuration, the loop filter (integrator block) in Figure 2.3 has been replaced by the VCO phase integrator model and the feedback path of the loop by the first-order difference (high pass filtering function, 1-z^{-1}). The input signal x(t) is directly connected to the VCO that generates a square signal w(t) given by equation (2.15). This signal is sampled and first-differentiated to obtain the output data y[n] with first-order noise shaped.

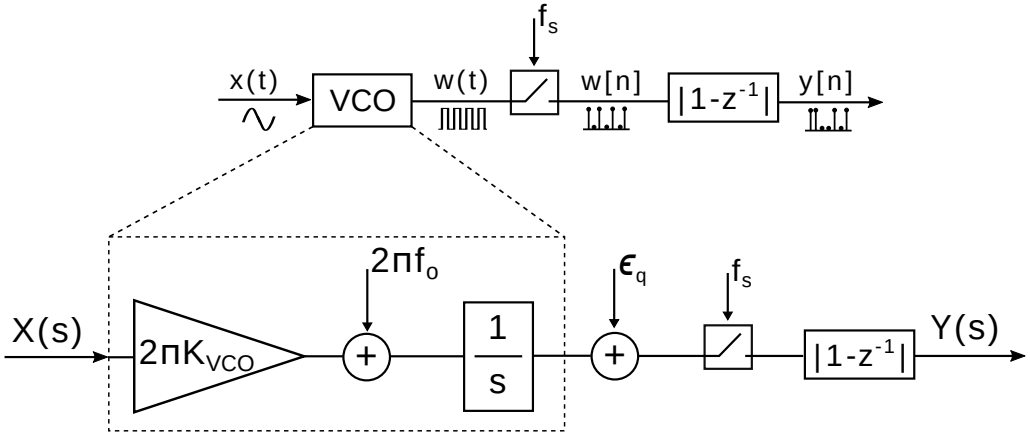


FIGURE 2.8: RO-based ADC open-loop architecture and its linear equivalent model.

Some equations are intuitively derived from the linear model above, and ignoring the constant term $2\pi f_o$ to ease the use of the model and simplify the calculations, the output of the system Y(s) can be approximated as follows:

$$Y(s) \approx 2\pi K_{VCO} \cdot X(s) + \left(1 - z^{-1}\right) \cdot \epsilon_q, \tag{2.18}$$

assuming that the input is a slowly varying signal relative to the sampling rate, $f_s \gg f_{in}$. Thus, the equivalence in terms of quantization noise of a RO-based ADC with a first-order $\Delta\Sigma$ Modulator is established, and the maximum SNR of a first-order RO-based ADC using a multiphase ring oscillator can be approximated to [29]:

$$SNR(dB) \approx 6.02 \cdot M_q + 1.76 - 5.17 + 30 \log_{10} OSR, \tag{2.19}$$

where M_q is the effective number of quantization bits which is determined by the phase resolution of the RO during the sampling period, T_s, following the next equation:

$$M_q = \log_2 \left(\frac{2V_{peak} \cdot K_{vco} \cdot N}{f_s} \right). \tag{2.20}$$

The term $2V_{peak} \cdot K_{VCO}$ corresponds to the full-scale oscillation frequency variation, $f_{osc\text{-}max}$-$f_{osc\text{-}min}$. Here, ϵ_q is considered a random signal and uncorrelated with the input signal with a white noise spectral distribution, similar to the approach employed for classical $\Delta\Sigma$ Modulator. The truth regarding ring oscillators states that the quantization noise depends on the input signal and, in some cases, the resolution can be significantly different from the expected value from equation (2.19). This issue will be addressed later.

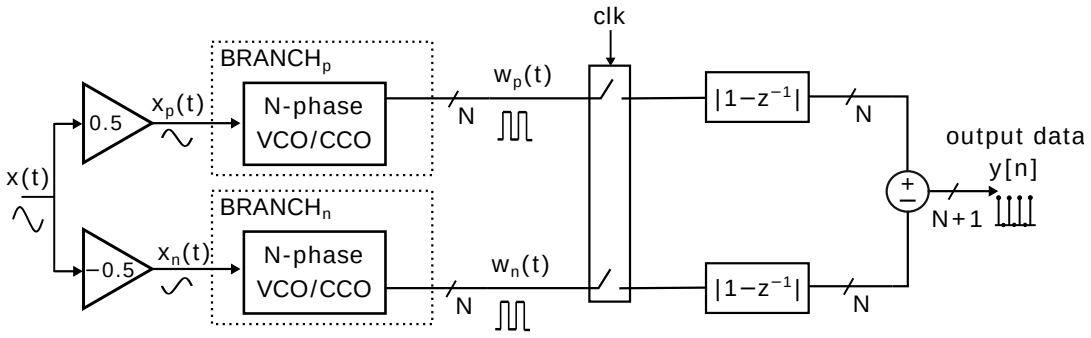
The oscillation period denotes the quantization step of the conversion, so the higher the oscillation frequency the higher the achievable resolution. In this structure, the RO works as a phase integrator and a quantizer simultaneously whose output is already a digital signal. The modulo arithmetic operation in Figure 2.8, $|1\text{-}z^{-1}|$, is needed to demodulate the signal from the ring oscillator.

The conceptual architecture that digitizes an analog signal with a RO-based ADC is realized with a digital counter which performs the integration operation by accumulating the number of pulses from the VCO during T_s. The amount of pulses can be counted with either a single-edge (rising or falling edge) or dual-edge polarity detection. Clearly, a better resolution is achieved for the latter case since a dual-edge responsive counter detects a smaller quantization step, so a higher number of quantization steps is counted with the same sampling frequency. Nevertheless, the implementation supposes larger area and power dissipation. The count, which represents the oscillation frequency quantization into an integer number, is registered with the clock signal, and then the counter is reset. The value in the register is a measure of the oscillation frequency and, therefore, a representation of the analog input level x(t). The higher the oscillation frequency, the higher the achievable resolution [62].

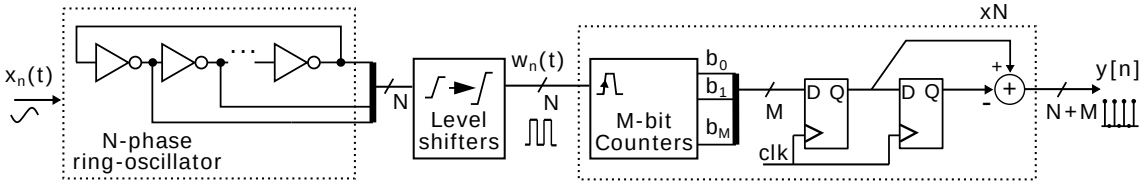
2.3.2.1.1 RO-based ADC implementation in open-loop configuration

The conventional structure for a pseudo-differential open-loop RO-based ADC is depicted in Figure 2.9(a), built with one VCO/CCO per branch followed by some digital logic that samples and computes the first difference of the output phases [28]. Finally, the outputs of the differentiators are combined into a multi-bit output digital signal y[n].

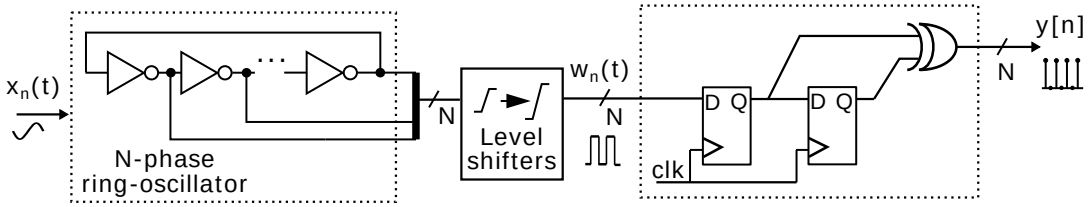
The practical implementation with counters is depicted in Figure 2.9(b). The value of the digital counter is increased with every rising edge that receives from the VCO output w(t). The number accumulated in the counter is sampled with a flip-flop every T_s. The relationship between the maximum value of oscillation



(a) Pseudo-differential configuration for an open-loop RO-based ADC.



(b) Circuit built with an N-phase RO, level-shifters, counters and flip-flops.



(c) Circuit built with an N-phase RO, level-shifters, flip-flops, and XOR gates.

FIGURE 2.9: Open-loop RO-based ADC and circuit.

frequency and the sampling rate determines the minimum number of bits of the digital counter (M). The first-difference operation after sampling is arithmetically computed by a subtractor block composed with digital adders. The input signal quantized is represented with a multi-bit digital sequence (M) obtained for each output phase of the ring oscillator (N). An optimization of this architecture is proposed in [70] which uses a novel coarse-fine counting circuitry in the quantization and shows a lower power consumption and occupied area.

A simpler alternative circuit for Fig. 2.9(a) is shown in Figure 2.9(c), where the count increment of the oscillation frequency measured at every sampling clock cycle does not need the use of counters. This circuit performs the modulo arithmetic operation in a very easy way with a few digital logic. The first-difference is computed by an XOR gate that compares the current sample at the output of the first flip-flop and the previous sample stored in the second flip-flop [23]. With

this architecture the digital output is a thermometric code and contains the information from both rising and falling edges. In contrast to the structure with counter of Figure 2.9(b), here the circuit encodes the number of the edges from the RO with a single-bit digital sequence for each RO output.

Both architectures require level-shifter circuits to saturate amplitude-modulated ring oscillator output signals before being sampled and operated in discrete time. This will be shown later.

The difference between the implementation of the digital logic lies in the relationship between the sampling frequency and the highest oscillation frequency in the RO. In the case of having f_{osc} restricted to lower than half of f_s, $f_s/2 > f_{osc\text{-}max}$, the implementation of Figure 2.9(c) is suitable. Otherwise, asynchronous M-bit digital counters connected to the ring oscillator output phases will be required, as shown in Figure 2.9(b).

According to [23], resolution in a RO-based ADC depends on the effective oscillation frequency, which is defined as follows:

$$f_{\text{osc,eff}}(t) = N \cdot f_{\text{osc}}(t), \tag{2.21}$$

where N is the number of delay cells in the RO. This means that similar resolution can be achieved with different number of delay cells while the effective oscillation frequency remains constant, either by reducing the stages in the RO and hence the delay of the cells to boost f_{osc}, or by using a higher number of stages resulting in a longer propagation delay time which produces a lower f_{osc}. In Chapter 4 two ways to increase the effective frequency are described in order to improve the resolution in RO-based ADCs.

In the system of Figure 2.9(b), the resolution can be improved by means of using a very high oscillation frequency. This would have a negative effect in terms of power consumption and could complicate the implementation of the counter that works at f_{osc}. Additionally, an increase of the bit width of the counters results in a larger digital circuitry afterwards, which also penalize the power. In the case of the structure in Figure 2.9(c), a very high sampling clock can be used to attain a better resolution. This requires a high-speed digital logic and increases the power consumption of the whole architecture. A proper selection of the structure is determined by the requirements of the converter application to find a better compromise between area, power and resolution to be achieved.

These RO-based ADC systems in open-loop configuration are implemented with highly technology-scalable architectures using only digital CMOS logic gates and without any conventional analog circuitry. Nevertheless, ROs based on ring oscillators offer an intrinsic nonlinear voltage-to-frequency response. Consequently, distortion components in-band will be observed at the output spectrum, and the final resolution will be restricted.

Up to now, we have assumed that the converter accuracy is only limited by the quantization noise. Considering the harmonic distortion terms (and other extra noises from circuits such as thermal and flicker noise), the relationship that

quantifies its effect and ϵ_q over the input signal is now the SNDR, as mentioned in Section 2.1. As a rule of thumb, we can state that getting an SNDR higher than 40 dB in open-loop configurations becomes quite challenging without any kind of RO linearity correction [71]. Even-order harmonic distortion is removed with a pseudo-differential architecture, but the remaining components can still severely degrade the performance for large input swings (>100 mV). Some alternatives to correct the nonlinear response of ROs are addressed in Chapter 3 of this document. The proposed ideas are introduced into open-loop RO-based conversion architectures without sacrificing simplicity of the implementation and scaling to future CMOS technologies.

2.3.2.2 Close-loop structure for RO-based ADCs

Conversion architectures with this configuration can be found in the literature, such as [4], [6],[7], [68], [73].

In the previous section a VCO-based ring oscillator that performs analog integrator functionality is used to implement an architecture whose output spectrum exhibits a first-order noise-shaped equivalent to the traditional first-order $\Delta\Sigma$ Modulator. Even though the performance of the presented open-loop RO-based ADC is similar and offers more scalable design solutions, the structure is different from the basic scheme of a $\Delta\Sigma$ Modulator and is limited to first-order filtering. To obtain a high-order noise-shaping, a RO can be used to replace the second integrator and the quantizer within the loop of second-order $\Delta\Sigma$ of Figure 2.4, as presented in [6].

It is usually placed a VCO inside a closed-loop to attenuate its input level, and thus the harmonic distortion seen at the converter output due to the ring oscillator nonlinearity is reduced. Nevertheless, opamp are employed as the first stage and DACs are required for the loop feedback. This architectures that include analog integrators as front-end circuit of the system, are very sensitive to a phenomenon called clock jitter. In practice, the clock signal is perturbed by electrical noise from the circuit generating the oscillation, which supposes randomly shifts of the time instants. The integration operation performed for a classic integrator with opamp, that directly depends on the duration of the sampling period, is significantly affected by the variations of the clock frequency. Also, closed-loop RO-based ADCs suffer from excess loop delay problem. This represents the time between the quantizer clock edge and DAC current pulse at the feedback point in the modulator. This issue deserves special attention because the system stability is compromised.

Structures have been published with a high-order noise-shaping using only RO-based integrators [74]. In [4] a third-order all-RO CT$\Delta\Sigma$ Modulator is presented, incorporating ring oscillators digitally driven (digitally-controlled oscillator, DCO) in the middle and at the end of the architecture. These types of structures are still quite complex and impose restrictions over certain parameters to offer adequate performance, for instance limiting the gain of the ring oscillator,

which reduces the RO sensitivity and hence the achievable resolution from the whole system.

2.3.3 Design considerations: RO nonidealities

When designing time-encoded conversion architectures using ring oscillators, there are some important considerations that severely degrades the performance of the converter. In a RO-based ADC, phase noise and distortion are the major concerns in the system implementations. Phase noise is a fundamental issue in low-bandwidth applications, like biomedical instrumentation devices, audio or sensing. The nonlinearity characteristic of the RO is the chief limitation of the accuracy from the converters in wide-band communications applications. Figure 2.10 illustrates the influence of the VCO nonidealities at the output spectrum of a first-order ring oscillator-based converter.

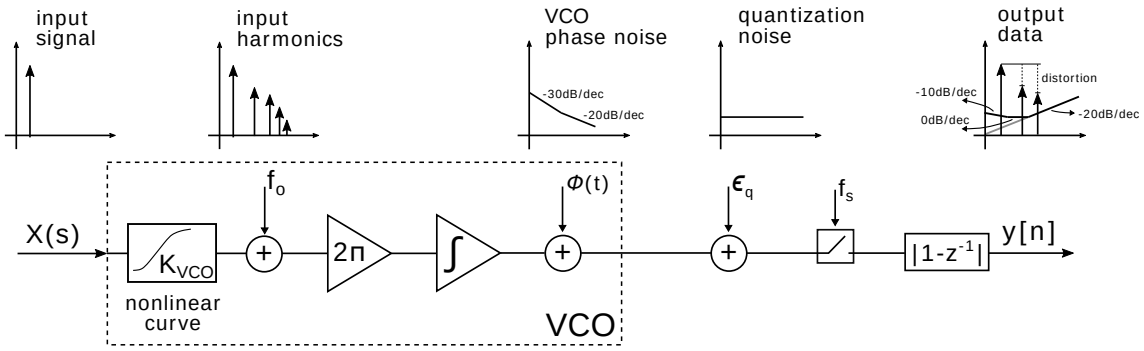


FIGURE 2.10: Influence of VCO nonidealities in a first-order ring oscillator-based ADC.

The distortion results from the nonlinear voltage-to-frequency curve of the ring oscillators and is seen as harmonic components of the input signal. Phase noise is represented by several noise components at low frequencies generated by phase fluctuations, ϕ(t), in the ring oscillators outputs.

2.3.3.1 Nonlinearity in ring oscillators

The most common circuit for a VCO with a ring oscillator is shown in Figure 2.11, composed of a transconductor-based front-end stage (g_m) and an N-phase CCO with conventional CMOS logic inverters. C_L represents the equivalent load of the digital logic connected to each phase and needed to generate the output data. The voltage-to-current conversion could be performed with a single CMOS device, either an NMOS or a PMOS transistor (see Figure 2.11a and Figure 2.11b). Ring oscillators can be also driven in voltage by a transistor as a common-drain amplifier or source follower. PMOS or NMOS device in this configuration acts as

a voltage buffer, whose the source gate follows the signal applied to the gate node with a unitary gain. In this document, ring oscillators are controlled in current mode using a transconductance-based stage, so the explanations are referred to this configuration.

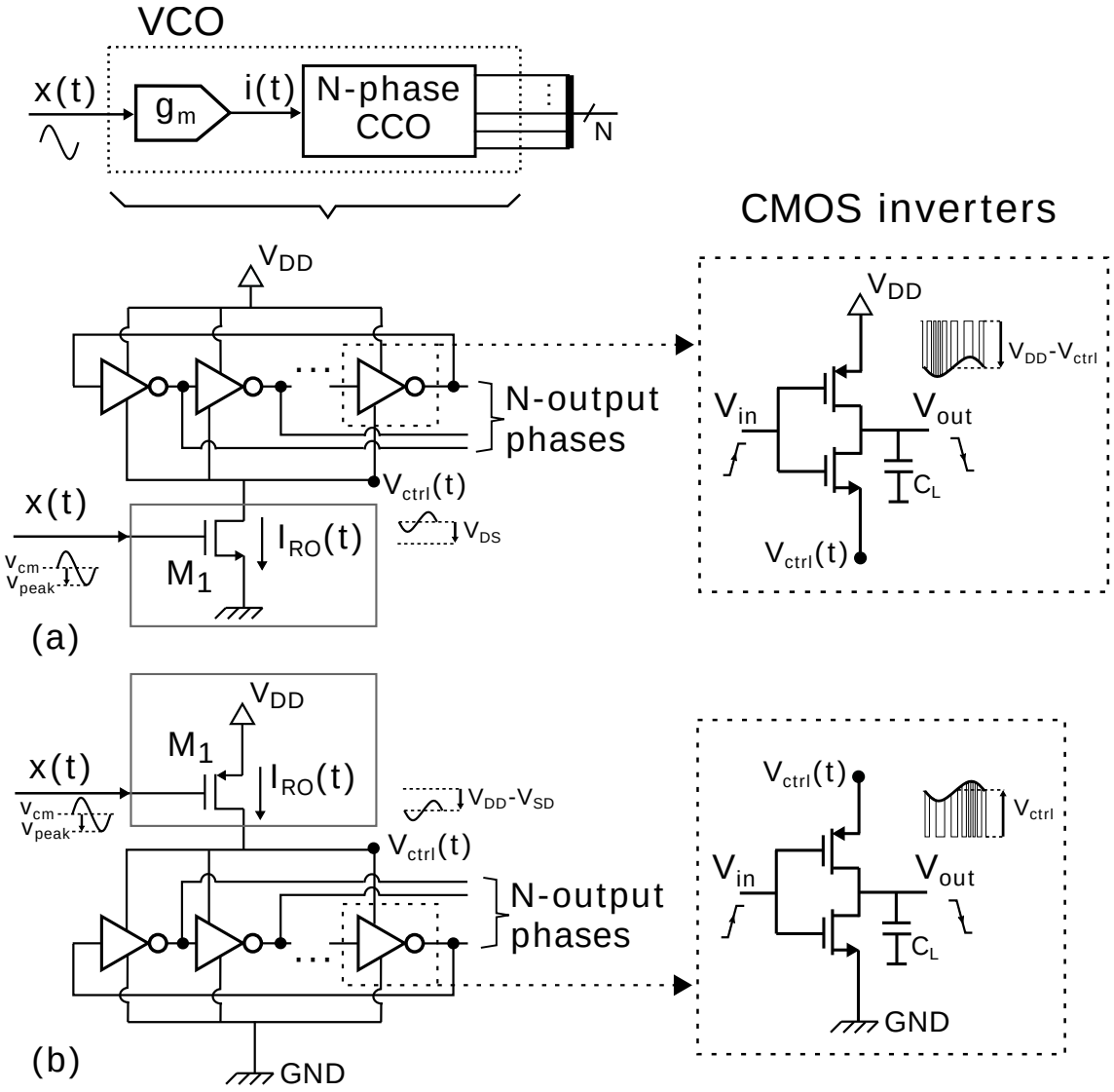


FIGURE 2.11: Conventional ring oscillator implementation for VCO-based ADCs: (a) NMOS-based transconductor and ring oscillator with CMOS NOT gates, and (b) PMOS-based transconductor and ring oscillator with CMOS NOT gates.

In any case, the output phases are both frequency- and amplitude- modulated by the input signal x(t), that is why level-shifter circuits are required to keep the level at the output compatible with the digital logic afterwards. The current I_{RO} flows through NOT gates connected in a ring configuration and modulating their

time delay, $t_{pd}(t)$. Here, the instantaneous oscillation frequency of the ring oscillator, $f_{osc}(t)$, ideally expressed as equation (2.14), incorporates a term associated with the front-end stage, and the new expression is as follows:

$$f_{\text{osc}}(t) = f_{\text{o}} + K_{\text{VCO}} \cdot g_{\text{m}} \cdot x(t), \tag{2.22}$$

where g_m is the transconductance of the front-end circuit: the single NMOS device in Figure 2.11a or PMOS device in Figure 2.11b.

However, as stated in [75], the voltage-to-frequency transfer function of this structure (Fig. 2.11) is not a linear relation due to two factors: the nonlinear delay dependence of the NOT gates of the ring oscillator with respect to the flowing current [51], and the nonlinear voltage-to-current relation in the transconductance g_m. The nonlinear response results in distortion and limits the dynamic range of the whole ADC. This corresponds to the most challenging ring oscillator characteristic for RO-based ADC design. The most realistic model to a ring oscillator response is translated into a high-order frequency components multiplies of the input signal tone, assuming the input of the converter as a sinusoidal signal. Thus, the ideal input x(t) in equation (2.22) can be expressed as a distribution of harmonic distortion terms as:

$$x'(t) = \sum_{k=0}^{n} p_{\text{k}} x(t)^k = p_0 + p_1 \cdot x(t) + p_2 \cdot x(t)^2 + p_3 \cdot x(t)^3 + ... + p_{\text{n}} \cdot x(t)^n, \tag{2.23}$$

where p_n corresponds to the coefficients of the polynomial approximation that describes the nonlinear behavior from the RO response. In equation (2.22), f_o and $K_{VCO} \cdot g_m$ corresponds to p_0 and p_1, respectively. Then, the oscillation frequency can be rewritten as follows:

$$f_{\text{osc}}(t) = f_{\text{o}} + K_{\text{VCO}} \cdot g_{\text{m}} \cdot x(t) + K_{\text{VCO-2}} \cdot g_{\text{m-2}} \cdot x(t)^2 + K_{\text{VCO-3}} \cdot g_{\text{m-3}} \cdot x(t)^3 + ... + K_{\text{VCO-n}} \cdot g_{\text{m-n}} \cdot x(t)^n. \tag{2.24}$$

The input signal passes through the ring oscillator, which produces a deviation in the conversion curve that corresponds to a nonlinear relationship between the input voltage/current and the frequency of the RO output phases.

The RO nonlinearity characteristic is a major concern for RO-based ADCs with large input signals for high-bandwidth applications. In Chapter 3 of this document two solutions to correct the nonlinear transfer function of ROs and mitigate for its effect over the converter are proposed, details about the implementation are presented, and the results are described and compared to other alternatives found in the literature. By extracting the oscillation frequency through a sweep of the input voltage/current, polynomial approximation of the RO transfer function

can be performed (written as equation 2.24). The resulting fitting curve allows us to statically model the harmonic distortion from the ring oscillator and, hence, estimate the final resolution of data converter. This static characterization seems to be enough accurate by comparing to the dynamic performance of RO-based ADCs when the input signal frequency, f_{in}, is sufficiently lower than the rest oscillation frequency, f_o. The equivalence between the static and dynamic performance of the data converter does not remain when the RO input frequency is close to f_o, with the distortion being increasingly higher from certain values of f_{in}. This behavior will be studied in the future to fully describe the RO nonlinearity property and how it impacts on the performance of RO-based ADCs.

2.3.3.2 Phase noise

The phase noise is manifest as random variations of the oscillation frequency at the output phase of an RO due to the electrical noise in the circuit [76], [77], and is typically the dominant noise in RO-based conversion architectures. The phase noise is described by the thermal and flicker noise components that come from circuits used in the RO as resistance and transistor, as in any conventional analog circuit. This noise is modulated by the oscillation and appears in the spectrum around f_{osc} and its multiples. In an RO-based ADC, phase noise is down-converted after sampling as a low-frequency noise component at the output that restricts the resolution, especially at low input levels for low-bandwidth applications.

Phase fluctuations, $\phi(t)$, are derived from the combination of several noise types. According to [78], the spectrum of the phase fluctuations is split up into different regions depending on the modulation source. The graph of Figure 2.12 depicts the simplified model of phase noise dominant in an RO-based ADC. The most significant two segments of the phase noise distribution are identified: $1/f^3$ describes the flicker noise contribution, and $1/f^2$ corresponds to white noise relative to thermal noise. This description is enough accurate in most applications.

The phase noise of a ring oscillator depends on many factors: the input amplitude, the number of stages, the size of the transistors, the current that feeds the delay cells, and the symmetry of the oscillation frequency edges [77], [79], [80]. By designing delay stages with equal rise and fall times, the flicker noise contribution is enhanced. Ring oscillators realized with transistors that occupy large area exhibits lower flicker noise component. Similarly, flicker noise is proportionally reduced with the increase in the number of taps. However, a high number of stages complicates the phase decoder design. Simultaneously, the thermal noise component is improved by burning more current consumption. Therefore, a suitable trade-off between the complexity of digital circuitry, area, power, and phase noise reduction must be carefully studied.

The chopping technique is a design option to minimize the impact of flicker noise in RO-based ADCs, which up-modulates the noise around a high frequency

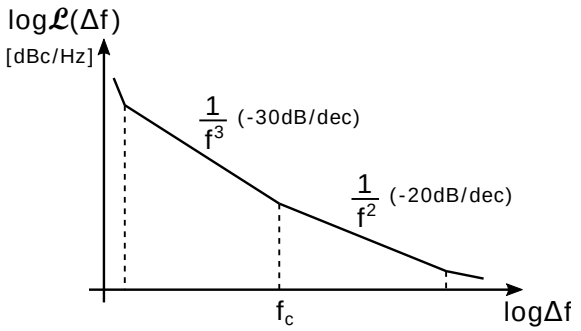


FIGURE 2.12: Simplified representation of phase noise, denoted by $\mathcal{L}$(f), in an RO-based ADC. The corner frequency, f_c, separates the regions corresponding to flicker noise and white noise, where both sources have the same noise contribution.

(chopping frequency) to avoid that falling inside the band of interest and degrading the performance of the converter at low frequencies. In [81]–[83] different ways to apply chopping to conversion architectures with VCOs in sensing applications are described.

2.3.4 RO-based ADC model with pulse frequency modulation theory

Up to this point, an RO has be seen as a digital version of an integrator to develop alternative implementations of ΔΣ Modulators. Now, the functionality of a ring oscillator will be analyzed by the relationship between the analog input and the output. We can be deduced from equation (2.14) that the input information x(t) is encoded in the frequency (f_{osc}) of the output, according to which an RO is therefore a signal encoder. PFM is a method to represent an analog input with a frequency-modulated signal of only two levels. Then, an equivalence between a first-order open-loop RO-based ADC and a pulse frequency modulator can be settled.

The PFM-based interpretation of open-loop RO-based ADCs is shown in Figure 2.13. The ring oscillator produces a square wave output w(t) with an oscillation frequency $f_{osc}(t)$ that varies with the instantaneous amplitude of the modulating input signal x(t).

In such RO, the information is encoded in the position of the edges of w(t). There is a direct mapping to PFM [23] if signal d(t) is generated as a Dirac delta pulse train coincident with the rising edges of w(t). In order to come to an RO-based ADC, d(t) is applied to a pulse shaping filter with impulse response h(t). The output of this filter y(t) is then sampled with a sampling frequency f_s to produce the output data y[n]. Note that in Figure 2.13, d(t) is a conceptual signal and what needs to be physically implemented is y(t). An important observation

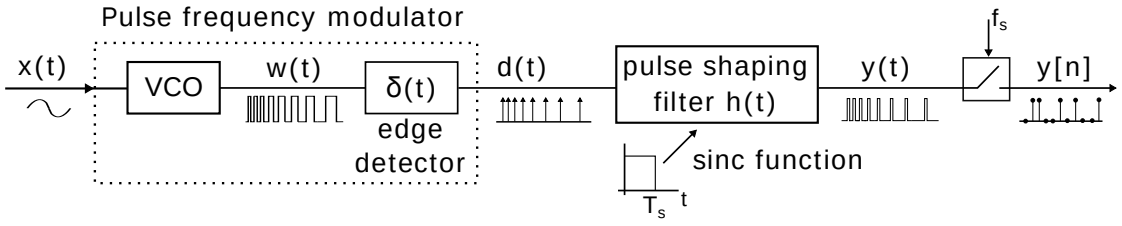


FIGURE 2.13: PFM-based interpretation of VCO-based ADCs.

is that the pulse frequency modulated signal d(t) contains the information of the baseband signal x(t). However, d(t) also contains a wide-band spectrum with many out-of-band tones [23]. A sketch of this spectrum is shown in Figure 2.14.

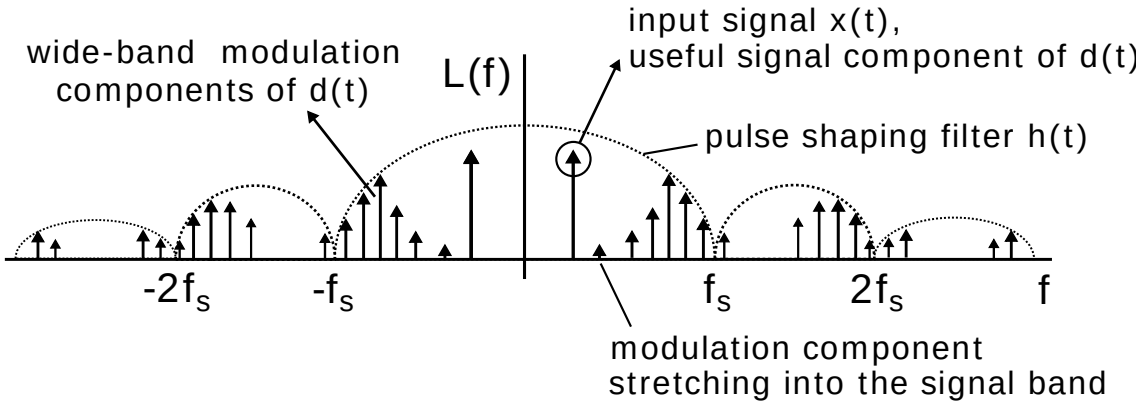


FIGURE 2.14: First-order *sinc* function as the pulse shaping filter.

There is a fundamental accuracy limit in the encoding of x(t) into the signal d(t): i.e. it might happen that modulation components of a sideband extend into the useful signal band (see Figure 2.14). If this happens, it causes a fundamental encoding error [23]. However, this fundamental encoding error is negligible if the VCO rest oscillation frequency f_o is sufficiently larger than the useful signal band. Apart from this fundamental encoding error, a second source of information loss happens in the sampling (due to the aliasing of the wide-band modulation components). Usually, this aliasing error is dominant, and it will be now addressed.

The spectral properties of the aliasing process can be shaped by the pulse shaping filter h(t). This means that, in theory, any type of spectral shaping can be achieved with a suitable choice of the pulse shaping filter. For the first-order low-pass case, a suitable pulse shaping filter is a *sinc*:

$$L(s) = \frac{1 - e^{-sT_s}}{sT_s}, \tag{2.25}$$

where T_s is the sampling period, $1/f_s$. For frequencies sufficiently below f_s, the gain of this filter is close to unity. This way, the baseband signal x(t) will pass unchanged. However, at multiples of f_s there are zeroes. This will provide first-order spectral shaping on the wide-band modulation components that will alias to DC in the sampling process. It is shown in [23] that the result is identical to the well-known basic RO-based ADC with first-order spectral shaping of the noise [24] (which in the PFM-based interpretation comes from wide-band aliasing).

Finally, note that the impulse response of the filter $L(s)$ is a square pulse of width T_s according to the following expression:

$$l(t) = \frac{1}{T_s} \left(u(t) - u(t - T_s) \right), \tag{2.26}$$

where $u(t)$ represents the Heaviside step function. According to (2.26), the output signal y[n] is digital, so we are able to directly build an ADC just by sampling y[n].

This theory is exploited in an attempt of designing more digital radio receivers structures using RO-based ADCs as detailed in Chapter 5 of this document.

2.4 Conclusion

In this chapter the theoretical basis of analog-to-digital conversion were provided, from the general fundamentals to the particular case being addressed in this document: RO-based ADCs. The principle of $\Delta\Sigma$ Modulation was described for a better understanding of the noise spectral shaping and how systems based on ring oscillators exhibit a similar performance, allowing the implementation of functional architectures. The advantages of using conversion structures with ring oscillators as replacement to classic $\Delta\Sigma$ Modulators was discussed, to develop solutions for all type of applications. The main reason that captures the attention of the international designer community is the possibility of implementing highly digital structures very suitable for the current nanometer process. Another approach of ADCs using ROs based on the PFM theory was provided wherein the ring oscillator was analyzed as signal encoder. This methodology make possible the noise shaping properties extension in order to design different filtering functions. Additionally, two major disadvantages of ring oscillator circuits were described, which restrict the accuracy of the converter. According to the application, the efforts to overcome these issues are focused on which supposes a higher limitation. Several ways to palliate the restricted resolution from RO-based ADCs were also mentioned. In summary, this chapter comprised the foundations and practical implementation of conversion architectures with ring oscillators. The comprehension of the content described is essential to understand the research work presented in this document.

Chapter 3

Circuit-based techniques for linearity correction in open-loop RO-based ADCs

3.1 Introduction

The main limitation of the ring oscillator is the nonlinear voltage/current-to-frequency response, which translates into distortion and limits the dynamic range of the whole ADC. Several ways of correcting the RO nonlinearity have been proposed in the literature. One of the most explored is digital calibration. This solution highly compensates for the nonlinearity of ring oscillators but the digital correction circuitry usually corresponds to complicate designs, and requires large occupied area and wastes a lot of power [20], [25]. Another alternative consists of placing the RO into a $\Sigma\Delta$ loop [7], [9], where the nonlinearity is corrected by the gain of the loop. In these cases, the architectures are complex and involve analog blocks, such as integrator-based opamps and DACs, limiting the scalability. Circuit-level solutions have also been introduced at the cost of a much lower RO gain [28] which directly entails a restricted final resolution, or more complex designs [84], being in many cases in applications for low-bandwidth ADCs. The performance of this type of solutions highly depends on the manufacturing process: mismatch and PVT variations. The contribution of the works introduced in this chapter are on this frontier, offering simplicity, high scalability, power efficiency and area savings.

In this chapter, two solutions to compensate for the nonlinear transfer function of ring oscillators are presented for open-loop RO-based ADC implementations:

- Section 3.2: Firstly, a new circuit to linearize the dependence between the propagation time of the delay cells and the current through the ring oscillator. The proposal is highly robust against PVT variations and does not involve a calibration procedure of any kind, occupies a small area and consumes low power consumption compared to the state-of-the-art. Validation by measurements in a 65-nm prototype.

- Section 3.3: Secondly, using a multiple trasconductor-based front-end circuit that implements the inverse curve of the RO current-to-frequency function. This solution requires of a calibration circuit to adjust the PVT operating point of the RO. The proposal exhibits better performance in terms of power and area compared to other techniques to correct the RO nonlinearity with similar resolution, specially digital calibration. Validation by simulations.

Both alternatives are summarized with the main improvements and compared to some other prior solutions.

3.2 Delay cell for linear ring oscillators

In the first part of this chapter, a new delay cell for current-controlled ring oscillators (RO-based CCO) is presented. This delay cell is built with a NOT gate connected to a modulated current source and two extra NOT gates connected to a fixed supply voltage. The output voltage level is compatible with digital circuitry afterwards, so level-shifter circuits are not required. A high-bandwidth design is validated by transient simulation with a TSMC 65-nm CMOS process, showing a competitive performance compared to a similar circuit-level solution reported in [27], significantly reducing the total harmonic distortion (THD) power for high-swing input signals. A prototype of the proposal for lower bandwidth is implemented and manufactured in a 65-nm technology, and experimentally validated. Several samples of the test chip are tested. The measurement results show that the solution is robust against different PVT conditions without calibration, achieving proper distortion mitigation. The new CCO structure exhibits appropriate dynamic range performance, and excellent area and power efficiency, especially compared to a similar solution in [85]. The proposal is easily implementable regardless the CMOS process employed, and is suitable for medium resolution and low-, medium- and high-bandwidth applications.

The content of this proposal is organized as follows. In Section 3.2.1, the equations of the oscillation frequency in ring oscillators implemented with modulated NOT gates are described, showing highly nonlinear behavior. Secondly, the novel circuit proposal which implements more linear ring oscillators is analytically detailed, and is also compared in terms of linearity to the conventional structure. To validate the approach, simulations are initially performed with both RO prototypes designed in a 65-nm CMOS process. Section 3.2.2 presents the practical validation results of the proposed CCO at transistor-level and the comparison with others alternative linearization solutions. As a proof of concept, a prototype of the new RO-based CCO is implemented and manufactured in a 65-nm CMOS technology. The layout implementation of the test circuit, the die photo and the measured linearity performance are shown in Section 3.2.3.

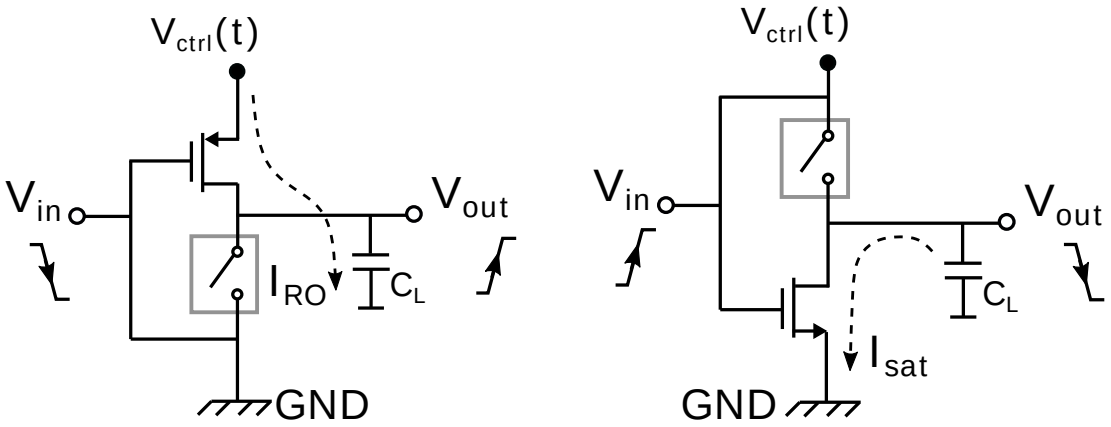
3.2.1 Foundations of the new delay cell circuit for ring oscillators

3.2.1.1 Propagation delay in a conventional NOT gate

Looking at one single phase of a ring oscillator with the structure in Figure 2.11(b), and considering the propagation delay of NOT gate [86], the period of the oscillating signal is expressed as:

$$T(t) \simeq N \cdot C_{\mathrm{L}} \cdot \frac{V_{\mathrm{ctrl}}(t)}{2} \left(\frac{1}{I_{\mathrm{sat}}} + \frac{1}{I_{\mathrm{RO}}(t)} \right), \tag{3.1}$$

where N is the number of phases, $\mathrm{I_{RO}(t)}$ is the RO current that flows through the PMOS transistor when the logic transition from '0' to '1' occurs, and $\mathrm{I_{sat}}$ is the saturation current flowing through the NMOS transistor when the logic transition from '1' to '0' occurs, as illustrated Figure 3.1(a) and 3.1(b), respectively.



(a) Transition from '0' to '1'. (b) Transition from '1' to '0'.

FIGURE 3.1: CMOS NOT gate operation in a ring oscillator

From equation (3.1), the resulting $\mathrm{f_{osc}(t)}$ as the inverse function of T(t) is calculated:

$$f_{\mathrm{osc}}(t) = \frac{2I_{\mathrm{sat}}}{NC_{\mathrm{L}}} \cdot \frac{1}{V_{\mathrm{ctrl}}(t)\left(1 + \frac{I_{\mathrm{sat}}}{I_{\mathrm{RO}}(t)}\right)}. \tag{3.2}$$

The expression for $\mathrm{f_{osc}(t)}$ is clearly a nonlinear function with respect to $\mathrm{I_{RO}(t)}$. This will result in distortion when using it for A/D conversion tasks. Note that distortion exists even when dealing with an ideal relation between $x(t)$ and $I_{\mathrm{RO}}(t)$ (Figure 2.11).

To have a look in more detail at the distortion due to the nonlinear function as stated equation (3.2), a 5-stage RO with the circuit of Figure 2.11(b) is designed in

a 65-nm CMOS process, but using an ideal voltage-controlled current source connected to V_{DD}. Transient simulations are performed with an equivalent behavioral model of Figure 2.9(b) in a pseudo-differential configuration. Apart from the ring oscillator, the circuit blocks for the simulation are ideally modeled with Verilog-A language. The result of the simulation is depicted in Figure 3.2. The oscillation parameters are f_o= 2.5 GHz and $K_{VCO} \cdot g_m$= 2.2 GHz/V, for a sinusoid input signal of 600 mV_{pp} single-ended amplitude using a single tone of 1 MHz. The sampling frequency f_s is equal to 3.5 GHz with an OSR equal to 175. The nominal supply voltage is 1.2 V. As observed in Figure 3.2, the resulting SNDR is 59 dB and the third harmonic distortion (HD3) term is -60 dBc. Considering that the SNR is equal to 72 dB, RO nonlinearity strongly limited the final performance of the converter.

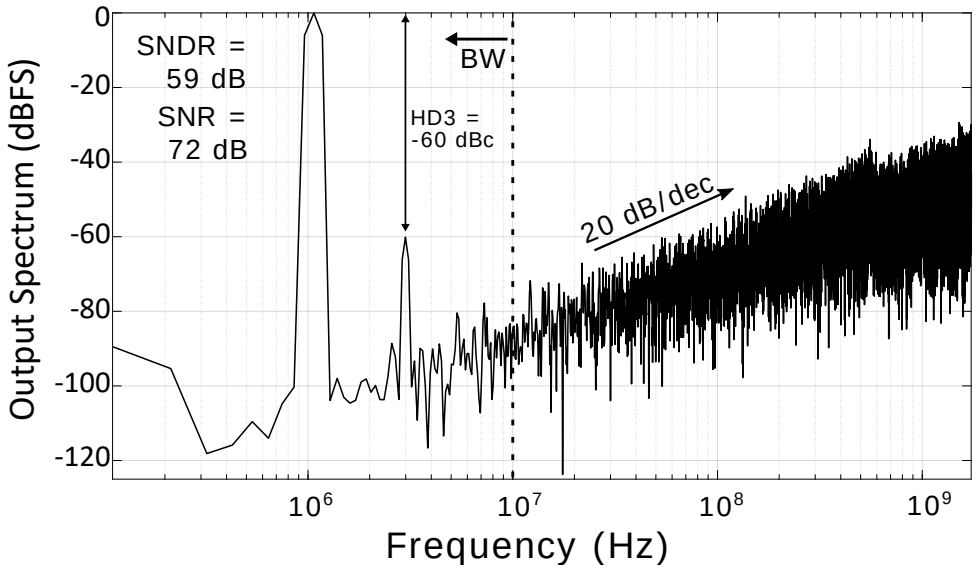


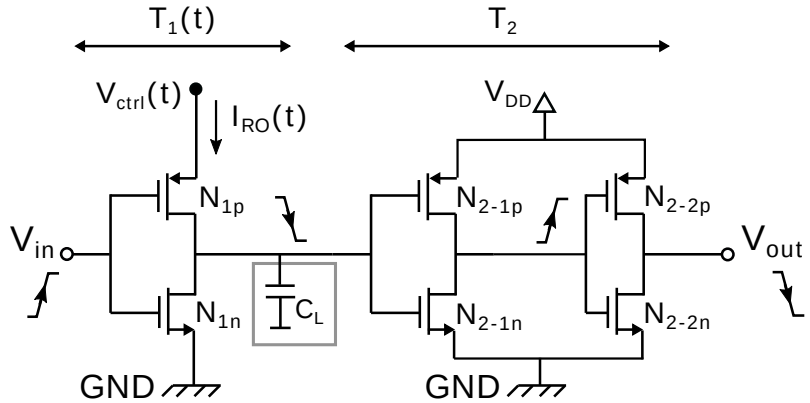
FIGURE 3.2: Output spectrum of the pseudo-differential VCO-based ADC with a conventional RO.

3.2.1.2 A linear delay cell

Alternatively to the conventional RO structure depicted in Figure 2.11, a new delay cell that achieves better linearity performance when included into a ring oscillator is proposed. The proposal consists of using the delay cell shown in Figure 3.3. The novel proposed delay cell is composed of three NOT gates connected in cascade, but with different voltage supply configurations. Whereas the first NOT is supplied by the voltage-controlled current source $I_{RO}(t)$ (similarly to the NOT gates of Figure 2.11), the following two NOT gates are connected to a constant supply voltage V_{DD}. Thus, the period of the oscillation frequency is as follows:

$$T(t) = N \cdot T_1(t) + N \cdot T_2 =$$
$$N \cdot \frac{C_L}{2} \cdot \frac{V_{DD}}{I_{RO}(t)} + N \cdot \frac{C_L}{2} \cdot \frac{V_{ctrl}(t) - \frac{V_{DD}}{2}}{I_{sat}} + 2N \cdot T_2, \tag{3.3}$$

where $T_1(t)$ represents the delay of the first NOT and T_2 the delay of the following two NOT gates. $T_1(t)$ is composed of the first two terms that correspond to the rising and the falling transitions of the first NOT gate. Note that T_2 is a fixed delay, not time dependent. The sizes of the transistors are properly selected to result in a symmetrical behavior at the transition states.



(a) schematic.

	W/L (µm/nm)
N_{1p}	20/65
N_{1n}	6/65
$N_{2\text{-}1p}$	10/65
$N_{2\text{-}1n}$	40/65
$N_{2\text{-}2p}$	30/65
$N_{2\text{-}2n}$	6.5/65

(b) device's sizes.

FIGURE 3.3: Proposed delay cell for a linear ring oscillator.

Equation (3.3) is comprised of three components. If we design the ring oscillator such that the following condition is accomplished:

$$N \cdot \frac{C_L}{2} \cdot \frac{V_{DD}}{I_{RO}(t)} \gg N \cdot \frac{C_L}{2} \cdot \frac{V_{DD}(t)}{I_{sat}} + 2N \cdot T_2, \tag{3.4}$$

the following approximation can be made:

$$T(t) \approx N \cdot \frac{C_L}{2} \cdot \frac{V_{DD}}{I_{RO}(t)}. \tag{3.5}$$

If the oscillation frequency is estimated from equation (3.5):

$$f_{osc}(t) = \frac{1}{T(t)} = \frac{2I_{RO}(t)}{N \cdot C_L \cdot V_{DD}}, \tag{3.6}$$

a linear function of f_{osc} with respect to $I_{RO}(t)$ is achieved.

The transistors in the new delay cell are sized to ensure that the condition imposed by equation (3.4) is met. Mainly by making large the second NOT gate in Figure 3.3(a) to have a huge load capacitance (C_L) seen by the first NOT gate changing the C_L node very slowly.

Additionally, as the last NOT gate in each cell is connected to the supply voltage V_{DD}, the output signal swing is always constant and there is no amplitude modulation. Consequently, level-shifter circuits connected to the RO phases are not required [4] in contrast to Figure 2.9(c).

3.2.2 Practical validation with simulations

To validate the proposed circuit, a transistor-based designed schematic in 65-nm with the same number of phases and oscillation parameters as the ring oscillator from Section 3.2.1 with a supply voltage of 1.2 V is designed, and transient simulations are performed. The transient simulation is computed with the same behavioral model and parameters used for Figure 3.2, but removing the level-shifter circuit blocks. Figure 3.3 contents the sizes of the transistors for the designed delay cell. $N_{2\text{-}1p}$ and $N_{2\text{-}1n}$ are big enough to accomplish with equation (3.4) and the rest of the devices are sized to ensure a proper flow of the digital oscillating signal. The output spectrum of the performed simulation is shown in Figure 3.4.

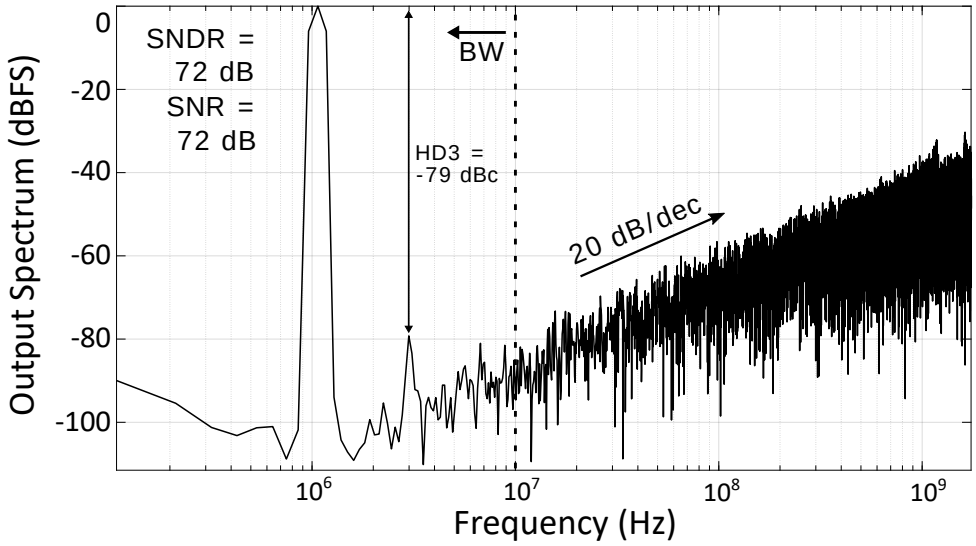


FIGURE 3.4: Output spectrum of the pseudo-differential RO-based ADC with the proposed delay cell.

The resulting HD3 term with the new RO structure is -79 dBc which is considerably smaller than the one obtained using the conventional RO circuit. In addition, the SNR and the achieved SNDR are both equal to 72 dB, so that the

converter performance is not now limited by distortion, but only by quantization noise.

Note that for the simulations an ideal voltage-controlled current source $I_{RO}(t)$ is used to drive both RO-based CCO architectures. In a practical implementation, this block will be replaced by a circuit whose linearity specifications must match with the desired resolution to be achieved. Consequently, a linear voltage-to-current conversion will be required. Several techniques to design linear transconductors have been proposed in the literature, such as [87], that are suitable for deep-submicron CMOS processes and for this proposal.

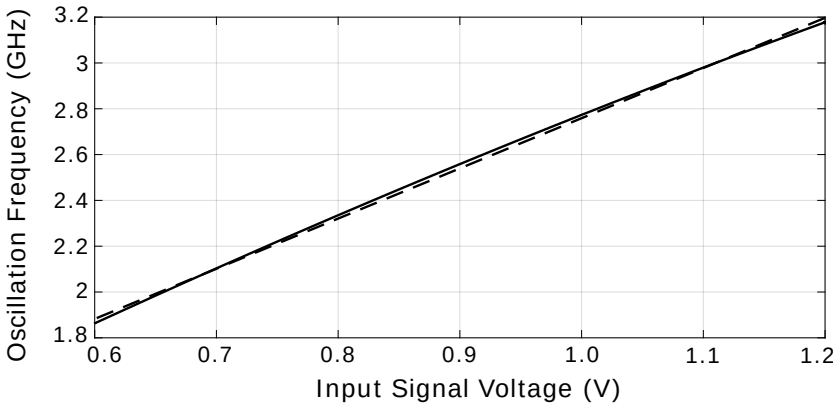
To provide additional data about the linearity of the new ring oscillator, Figure 3.5 shows relational measures between the real and linearized oscillation frequency curve and the input signal voltage. The voltage-to-frequency transfer function of the new oscillator is illustrated in Figure 3.5(a), where a slight difference between the ideal linear curve and the RO frequency is visible. A linear fitting is carried out to quantify the nonlinearity error of the new circuit. Figure 3.5(b) shows the difference between the real oscillation frequency and the ideal adjusted frequency. The largest deviation is $\pm$19 MHz for an input voltage of 600 mV_{pp}, which represents 1.4% of the RO frequency range from 1.86 GHz and 3.2 GHz.

3.2.3 Experimental validation

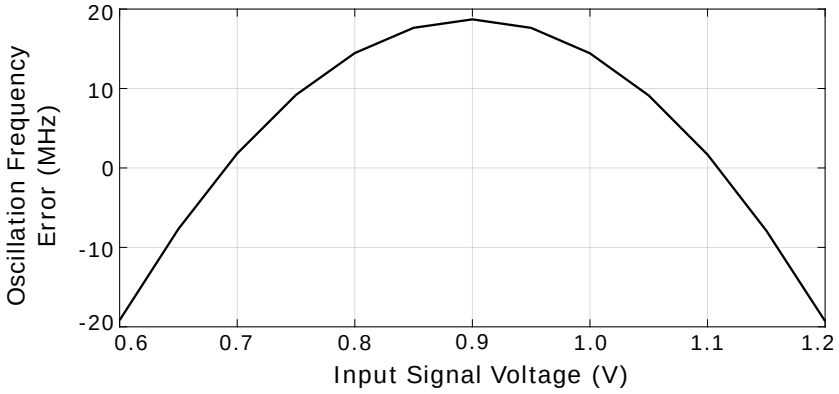
3.2.3.1 Layout implementation

We had the opportunity to include a 5-stage CCO with this new proposal on a die with other test circuitry for experimental measurements. The die photo of the test chip and the layout implementation of the ring oscillator prototype with the proposed delay cell circuit are shown in Figure 3.6. The design occupies 0.00094 mm^2. Due to speed requirements in the digital output data interface (max 50 MHz), a prototype for a lower bandwidth is proposed, but still suitable for experimentally testing the delay cell.

Therefore, the current injected into the ring oscillator is configured to achieve a lower oscillation frequency. Post-layout simulations are performed using an ideal current source with values between 6.75 μA and 14.25 μA achieving f_o= 26 MHz and K_{CCO}= 2.4 MHz/uA with a supply voltage of 1 V. The total CCO power consumption is 38 μW. By extracting one out of the 5 CCO phases from Cadence (noise enabled) at a sampling frequency of 4 GHz and post-processing in MATLAB, the output spectrum shows HD2 and HD3 terms of -44 dBc and -65dBc, respectively, by dealing with a single-ended configuration using a sinusoidal input signal at 7 kHz and 750 kHz. The HD2 term should be almost entirely removed in a pseudo-differential configuration, which does not affect the overall THD.



(a) Oscillation frequency: the solid line corresponds to the RO voltage-to-frequency transfer function and the dashed line illustrates the linear fitting.



(b) Ring oscillator frequency error.

FIGURE 3.5: Relational curves using the new ring oscillator circuit.

The design is highly robust to PVT variations. Transients simulations under different PVT conditions are performed: SS, FF, FS, and SF with a nominal temperature (27°C); critical operating points SS and FF with both -45°C and +120°C; and all of the conditions mentioned before including a variation of $\pm$50 mV in the supply voltage. The performance is not altered by that supply voltage variation. The worst case of HD3 term observed equals -63 dBc.

3.2.3.2 Measurement results

The test chip is manufactured in the low power (LP) TSMC 65-nm CMOS technology. In the test circuit, only one out of the 5 phases from the CCO is accessible. The phase is acquired by a 4 GS/s sampling logic analyzer to convert it into a bitstream. With a MATLAB script the digital data corresponding to the RO phase is processed (first-difference, FFT computation, SNDR, and SNR calculations) to obtain the resulting output spectrum. In another set of measurements, the ring

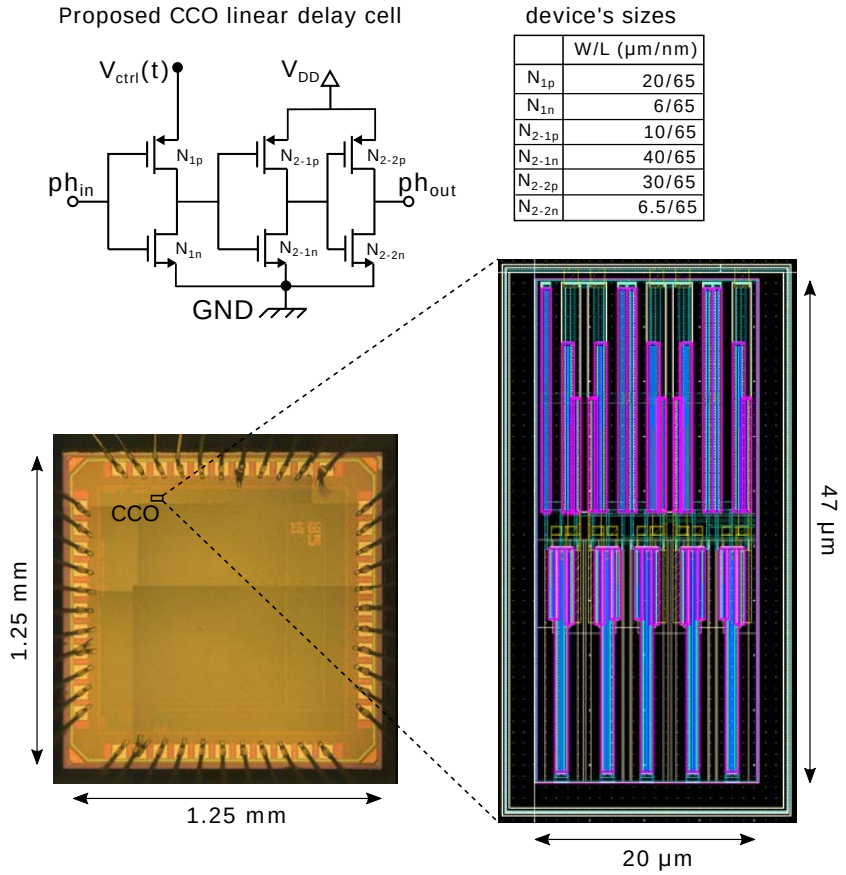


FIGURE 3.6: Die micrograph of the test chip in 65-nm technology, the layout implementation of the 5-stage RO-based CCO with the proposed linear delay cell.

oscillator is statically characterized by making a sweep of the input signal voltage to ensure a linear current through the RO-based CCO, extracting the oscillation frequency values at every point.

As a proof of concept, the transconductor providing the current that drives the ring oscillator, I_{RO}, is an off-chip resistor that performs the voltage-to-current conversion. The value of the resistor is larger than the equivalent resistance of the CCO ensuring that V_{ctrl} is approximately a constant voltage value and thus, providing a linear current flowing through the ring oscillator. The larger the value of the resistor, the more linear the voltage-to-current transfer characteristic. Therefore, the THD seen at the RO phase is fully determined by the nonlinearity response of the CCO. Figure 3.7 illustrated the circuit schematic which provides the current into de ring oscillator, and the printed circuit board (PCB) for measurements mode over the test chip. The CCO equivalent resistance estimated by post-layout simulations is approximately 55 kΩ, defined by the mean of $V_{ctrl}(t)$ and $I_{RO}(t)$, 550 mV and 10 μA respectively.

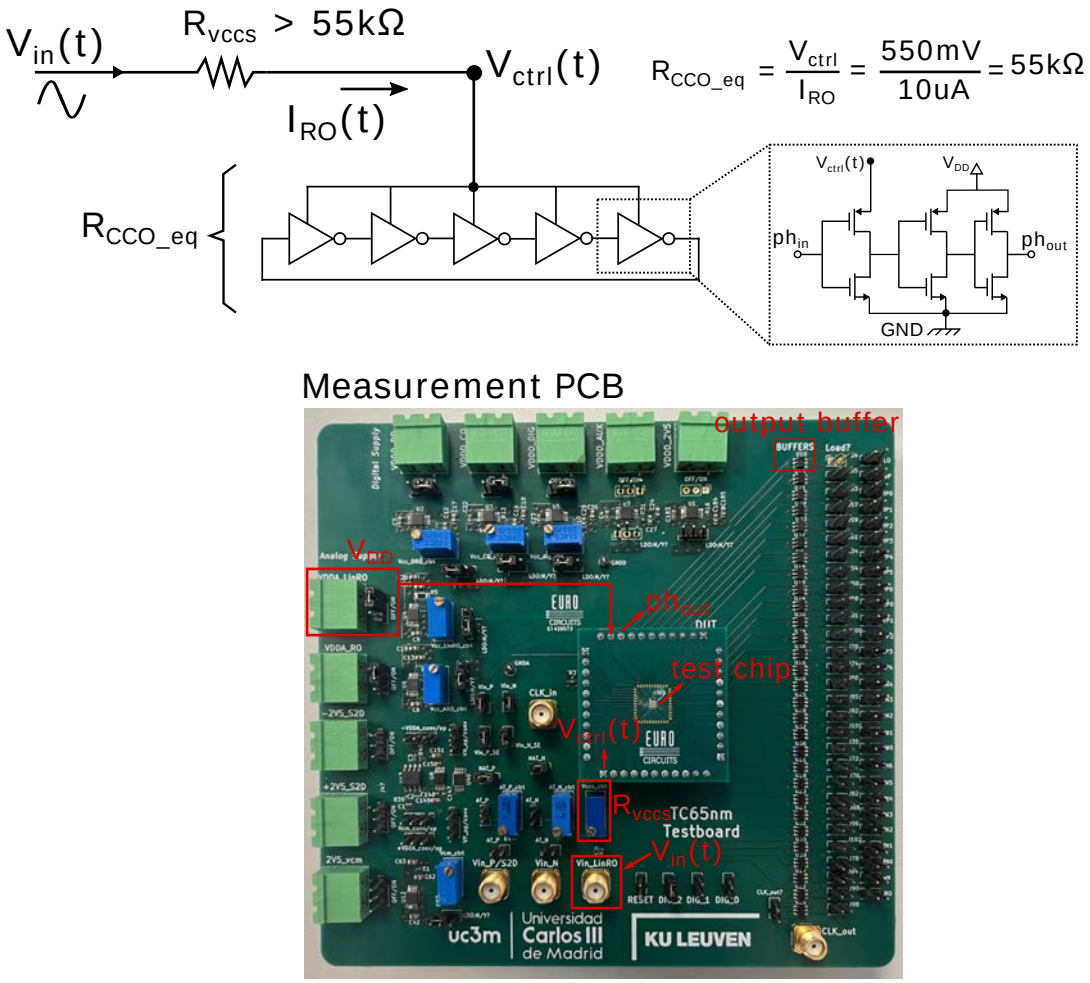
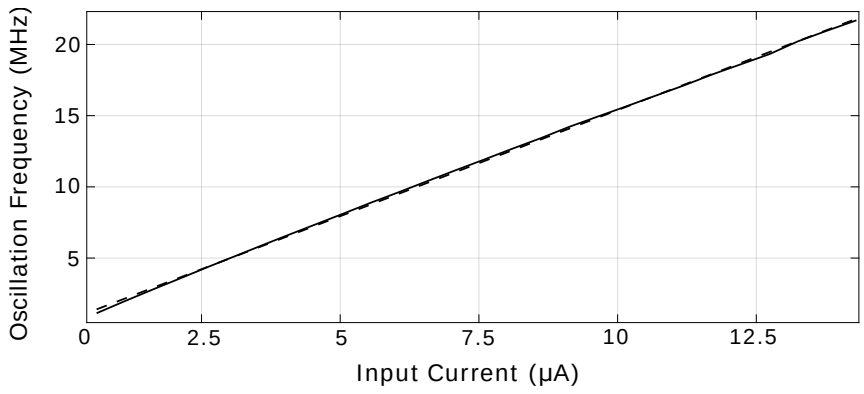
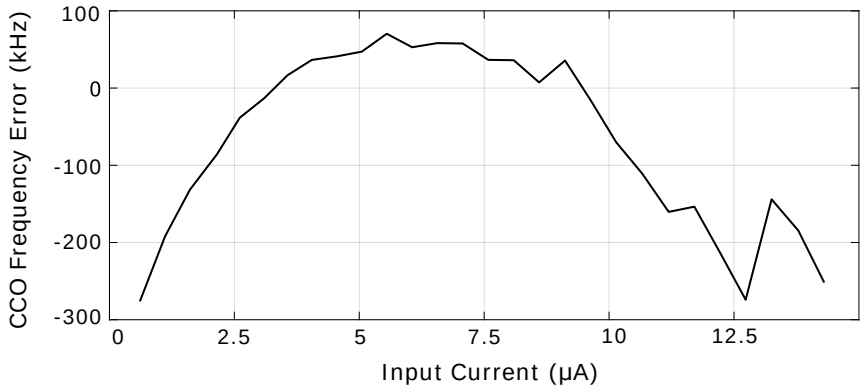


FIGURE 3.7: Off-chip resistor as the voltage-controlled current source and measurement PCB.

The plots in Figure 3.8 show the CCO static linearity measured making a sweep of I_{RO} with steps values of 500 nA. The current-to-frequency transfer curve and the ideal linear characteristic are illustrated in Figure 3.8(a). The performance of the proposed CCO closely approximates the linear curve adjusted. Figure 3.8(b) quantifies the nonlinearity through the error between the RO oscillation frequency (measured) and the ideal linear frequency. The CCO response exhibits a deviation of 270 kHz over the range from 1 MHz to 21 MHz for an input current of 13.5 μA_{pp}, which represents 1.3% of the entire oscillation frequency range (1.4% in the high-bandwidth design of Section 3.2.2). The lowest values of the error curve are found from 2.5 μA to 10 μA with a maximum variation of $\pm$70 kHz corresponding to 0.6% ([27] reports 0.6%). Within this range of current, the CCO provides the best linearity behavior.



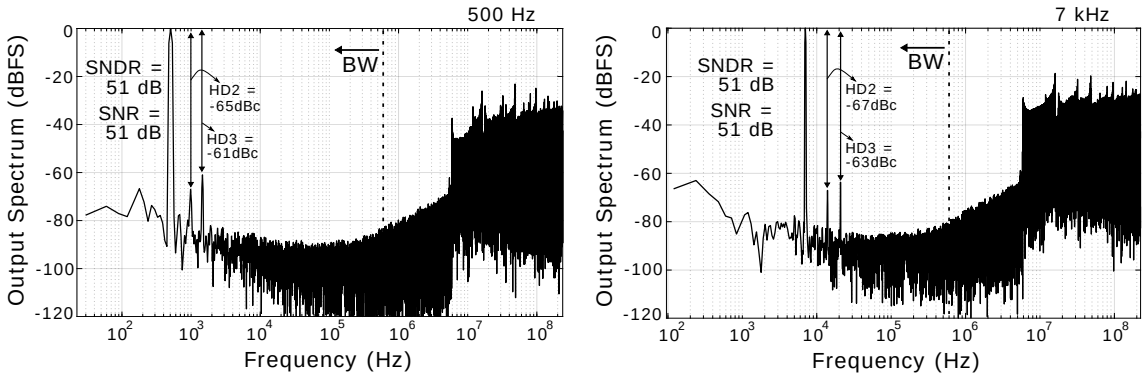
(a) Current-to-frequency transfer function.



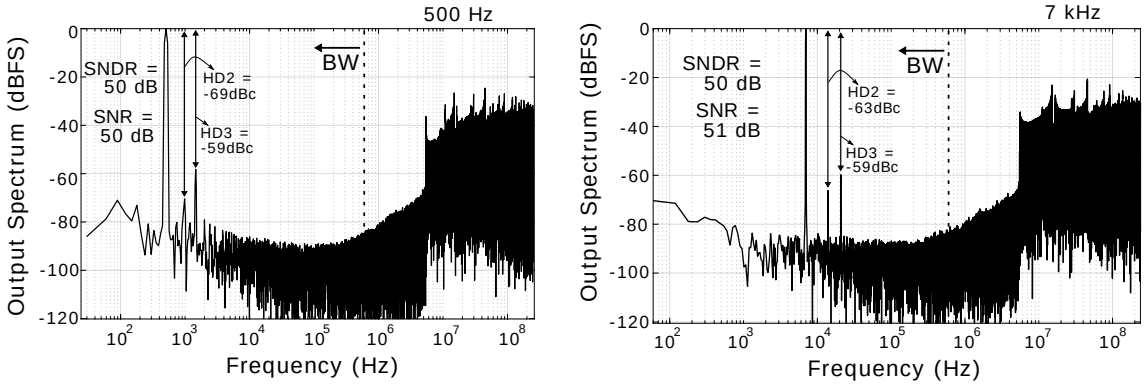
(b) Oscillation frequency error.

FIGURE 3.8: Measured static performance of the proposed CCO circuit.

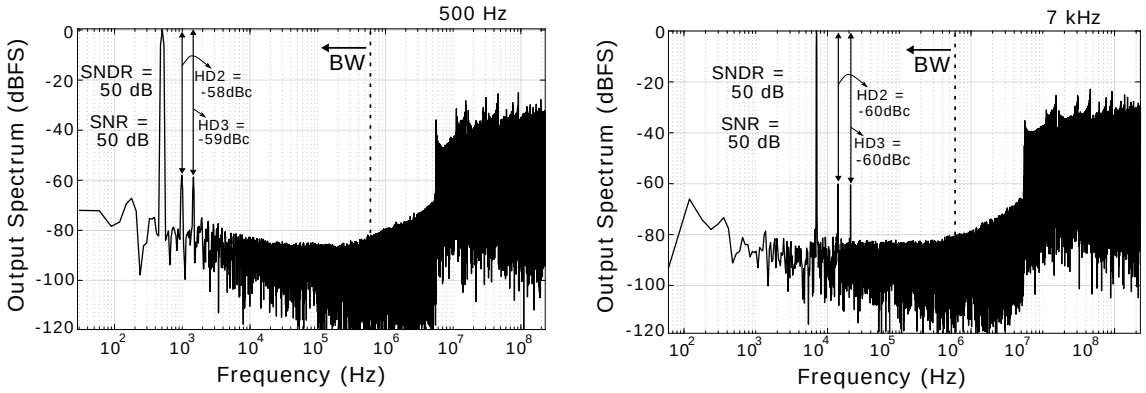
The dynamic performance is evaluated for a bias point of 7 μA, which corresponds to an input voltage of 1.2 V (V_{in} in Figure 3.7), with f_o = 11 MHz and K_{CCO} = 1.5 MHz/μA, and the measured value of V_{ctrl} = 530 mV. The best mitigation of the harmonic distortion is found for an input current of 7 μA_{pp}. The output spectra from the measured RO phase data from several samples in response to a single-tone sinusoidal input at 500 Hz and 7 kHz are depicted in Figure 3.9, obtained with R_{vccs} = 96 kΩ and f_s = 500 MHz. The plots show a noise floor consisting of the CCO flicker and the thermal noise. The flicker noise corner is seen at 30 kHz and the first-order noise shaping corner at 300 kHz. The harmonic distortion is defined by the HD2 and HD3 terms whose values are below -58 dBc for all the cases. The SNR and SNDR values are calculated for a bandwidth of 600 kHz. The dynamic range for the case of 7 kHz as the sinusoidal input frequency are shown in Figure 3.10. It is clear that, for input current amplitudes larger than 9.5 μApp, the CCO becomes increasingly nonlinear, where the dynamic range performance is limited by distortion leading to a peak SNDR of 51 dB.



(a) Sample 1.



(b) Sample 2.



(c) Sample 3.

FIGURE 3.9: Output spectra of single-ended configuration CCO-based ADC with the proposed RO cell circuit from prototypes on different dies for 500 Hz and 7 kHz, using 1 V as the supply voltage and input current amplitude of 7 μApp.

The CCO total power is defined by the power consumption of R_{vccs} and the two NOT gates supplied by V_{DD}: $(V_{in}\text{-}V_{ctrl})^2/R_{vccs} + 45\ \mu$W (with a supply voltage of 1 V) = 49.5 μW. In order to reduce the power consumption, the supply

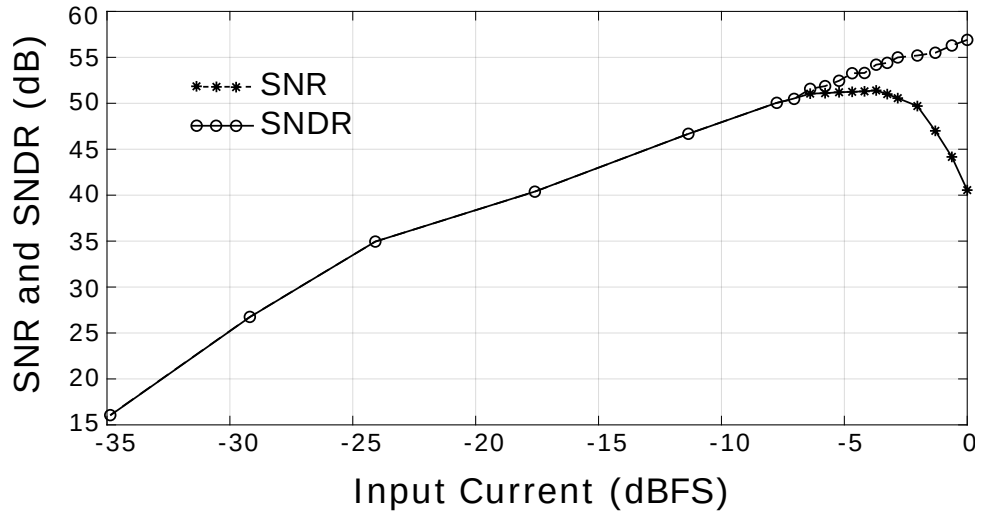


FIGURE 3.10: SNR and SNDR of single-ended CCO-based ADC with the proposed cell circuit from the prototype of sample 1 for different input current amplitudes.

voltage is decreased up to 0.7 V. The circuit remains operational, and the performance is not strongly degraded. The measured CCO gain is slightly higher, K_{CCO} = 1.66 MHz/μA, since the threshold voltage of the NOT gate composed by $N_{2\text{-}1p}$ and $N_{2\text{-}1n}$ is lower. Consequently, the time that takes I_{RO} charges C_L is reduced as stated in equation (3.5). This effect affects the CCO linearity characteristic but not significantly, resulting in higher harmonic distortion with HD3 being close to -60 dBc for an input frequency of 7 kHz from the prototype of sample 1 (compared to the resulting output spectrum of Figure 3.9(a) at the same input frequency), as illustrated in Figure 3.11. The CCO consumes a total power of 19.5 μW.

The plots in Figure 3.12 illustrate the static linearity performance of the CCO for a voltage supply of 0.7 V. The worst-case nonlinearity over the oscillation frequency range from 7 to 20 MHz is 130 KHz (input current between 4.2 and 12 μA), corresponding to 1%.

3.2.4 Discussion and conclusions

3.2.4.1 Discussion

The proposed idea offers an improved static linearity performance over a wide range of input signal compared to the conventional RO circuit. In the high-bandwidth design validated by simulations (Section 3.2.2), the proposed RO exhibits a proper dynamic performance where the achieved resolution of a pseudo-differential RO-based ADC is purely limited by quantization noise, with HD3

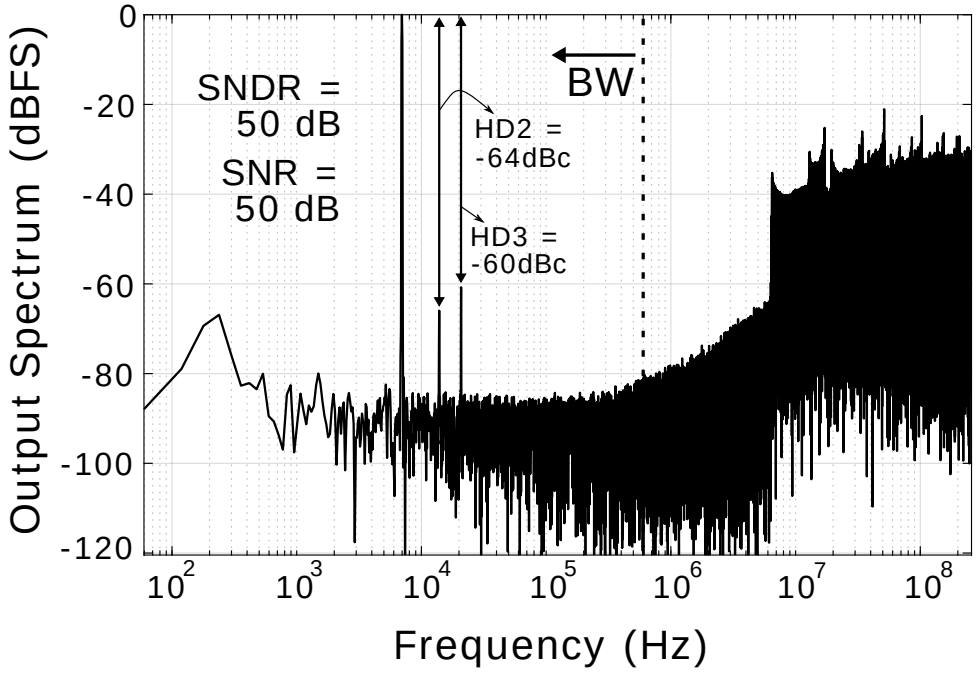
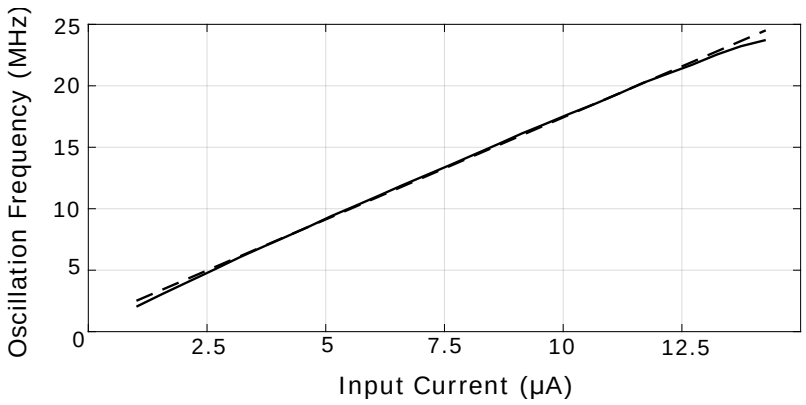


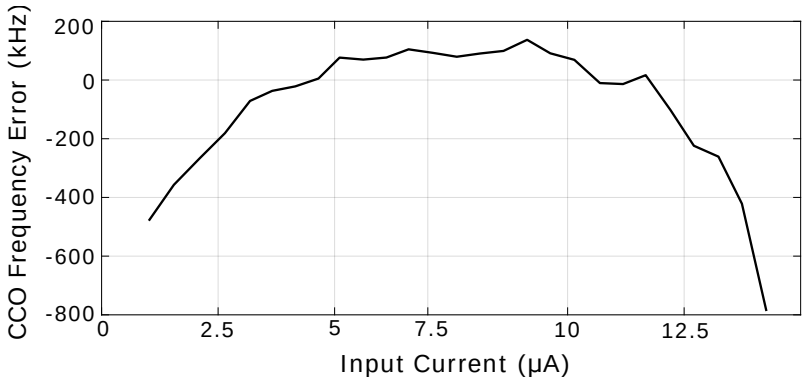
FIGURE 3.11: Output spectrum of single-ended configuration CCO-based ADC with proposed RO cell circuit from the prototype of sample 1, using 0.7 V as the voltage supply with a sinusoidal input at 7 kHz and 7 μApp of amplitude.

term being -79 dBc: SNDR = 72 dB over a bandwidth of 10 MHz for a single-ended input voltage of 600 mVpp. A similar circuit-based solution to correct RO nonlinear response is presented in [27]. A resistive network is used to attenuate the input amplitude which directly implies a reduction of the CCO gain. In a pseudo-differential architecture, the SNDR reported over a bandwidth of 2 MHz using one phase is 69 dB. The performance is reduced because only one out of the 18 VCO phases is used, however it is limited by distortion with HD3= -74 dBc for an input voltage signal of 400 mV_{pp}. The area for a single VCO is 0.0015 mm^2 and consumes 0.65 mW. Our proposal exhibits lower distortion for a RO input voltage higher.

The VCO-based ADC proposed in [10] corresponds to a complex architecture to mitigate the effect of the RO' nonlinearity at the digital output data. The scheme use two paths of VCO-based quantizers wherein the distortion of both ROs is canceled each other. The design is comprised of two DACs with passive substractors and four ROs with a conventional configuration (NOT gates cells and a transconductor) for pseudo-differential topology. The data converter delivers an SNDR of 59.5 dB over 40 MHz bandwidth. Our solution offers better area and power efficiency for simpler and highly-scalable data conversion architectures.



(a) Current-to-frequency transfer function.



(b) Oscillation frequency error.

FIGURE 3.12: Measured static performance of the proposed CCO circuit for a supply voltage of 0.7 V.

As a proof of concept, the RO test circuit is manufactured in 65-nm CMOS process: the design occupies 0.00094 mm^2 and consumes 45 μW. In [85] a similar solution is described and implemented in the same technology. The proposed CCO circuit corresponds to a design based on similar definitions to those described in Section 3.2.1. The peak SNDR of 50.1 dB over a bandwidth of 1 MHz and THD of -53.62 dBc are obtained for 1.5 μA_{pp} of current amplitude, corresponding to f_{osc} between 9 MHz and 22 MHz. The power consumption of the ring oscillator is 289 μA, six times higher than the CCO presented in this work with comparable oscillation parameters. The occupied area is similar with an approximate value of 0.00063 mm^2. For our solution, the peak SNDR of 51 dB over a bandwidth of 600 kHz and THD of -61.5 dBc is achieved for 9.5 μApp as the input current, with the oscillation frequency range from 4 MHz and 17 MHz. The proposed CCO design allows the supply voltage to be decreased, leading to a power consumption reduction of up to 33% and still getting a lower THD of -58 dBc. The presented CCO structure exhibits better performance with excellent power consumption and area.

The RO-based A/D conversion presented in [88] for neurochemical sensing applications also shows graphs for the static behavior of the proposal. The RO nonlinearity error corresponds to a 4% over an oscillation frequency range from 4 to 15 MHz (the same range as the proposed CCO) for an input current of 2.4 μA_{pp}, in comparison with 0.6% obtained with our ring oscillator for 7.5 μA_{pp}. A similar resolution is achieved for much lower input current amplitude, ± 600 nA_{pp}. The power consumption associated to the CCO is 31 μW, in line with our proposal, but the occupied area is 5 times larger.

The proposed CCO results in a very attractive solution with simpler and robust design offering competitive area and superior performance in terms of power consumption for similar data converter requirements. It must be noted that the solution involves a linear transconductor-based front-end design. The proposal is suitable for single-ended and pseudo-differential RO-based ADCs providing proper distortion mitigation with small area and excellent power efficiency.

Table 3.1 presents the summary of the measured performance of the proposed design and provides a comparison to prior works. Different CCO/VCO-based ADCs architectures are characterized as competitive alternatives. To achieve a fair comparison between the reference solutions and the proposed design, area, power, and Figure-of-Merit (FoM) values only include the ring oscillator and the associated linearization blocks for the cases where data are available (*).

3.2.4.2 Conclusion

In this section of the chapter, a new structure of linear ring oscillator for the implementation of oversampled ADCs was presented. This architecture is composed of a novel structure of delay cells, which consists of three CMOS NOT gates connected in cascade. Whereas the propagation delay of the first one is modulated by the input signal, the propagation delays of the others two are constant. This particular configuration allows us to implement ring oscillators with high linearity performance in comparison with the conventional structures of ring oscillators used for VCO-based ADCs. To validate the proposed approach, both circuits the conventional and the new ring oscillator were designed and simulated in a 65-nm CMOS process with a pseudo-differential architecture. The proposed design shows a superior performance compared to the typical RO circuit with NOT gates, resulting in a significant distortion reduction. A prototype of the new CCO design was manufactured in a test chip for measurement results. The occupied area is 0.00094 mm^2 and the power consumption is 45 μW with a supply voltage of 1 V. The nonlinearity error for a wide input current range as 7 μA_{pp} in a single-ended configuration produces a maximum deviation which corresponds to 0.6% of the oscillation frequency range. Additionally, the CCO circuit exhibits great robustness under PVT variations without calibration. The harmonic distortion is limited by HD3 term taking values below -58 dBc. The supply voltage can be reduce up to 0.7 V in order to minimize the total power consumption up to 33% without a significant degradation of the linearity property. Therefore, the

new delay cell offers a proper linearity response leading to a potential higher resolution performance in ADCs for large-swing inputs with competitive area and power efficiency, and with no need of calibration techniques. This solution can be applied to single-ended and pseudo-differential data converter architectures, specially appropriate for use with single-ended sensors such as biosensing applications.

TABLE 3.1: Comparison to state-of-the-art

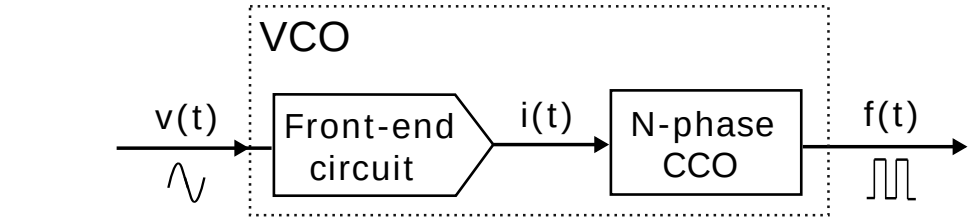
Parameter	[10]	[28] *	[84]	[85] *	[88] *	This work
Approach	VCO	VCO	ΔΣM	CCO	CCO	CCO
Meas./Sim. Results	MR	MR	SR	MR	MR	MR
Voltage Supply [V]	0.9	0.2	1	1.2	1	1/0.7
Process [nm]	40	28	28	65	65	65
BW [MHz]	40	0.061	10	1	0.0005	0.6
SNDR [dB]	59.5	68	62	50.1	53.19	51
THD [dBc]	-65.7	-72.5	–	-53.62	–	-61.5/**-58**
ENOB	9.59	11	10	8.03	8.54	8.18
Diff. Input Range	0.715V	0.355V	0.8V	1.52μA [a]	1.2μA [a]	9.5μA [a]
Power [mW]	2.57	0.0065	0.23	0.289	0.031[b]	0.05/**0.02**
Area [mm^2]	0.017	0.07	–	0.00063	0.005	**0.00094**
FoM [dB] [1]	160.9	167.7	166.4	145.5	125.4	151.8/155.9
FoM [fJ/s] [2]	42	26	14	552.8	83101	142.3/56
Linearization technique	Two-step VCO-ADC	Resistive network	Bulk driven	Linear cell	None –	Linear cell

FoM [dB] [1] = SNDR + $10log_{10}$(BW/Power).
FoM [fF/conv-step] [2] = Power/(2·BW·$2^{(SNDR-1.76)/6.02}$).
[a] This input current swing is for a single-ended CCO-ADC architecture.
[b] This power consumption is for the CCO-based ADC, the current acquisition stage from the neurochemical cell is not included.

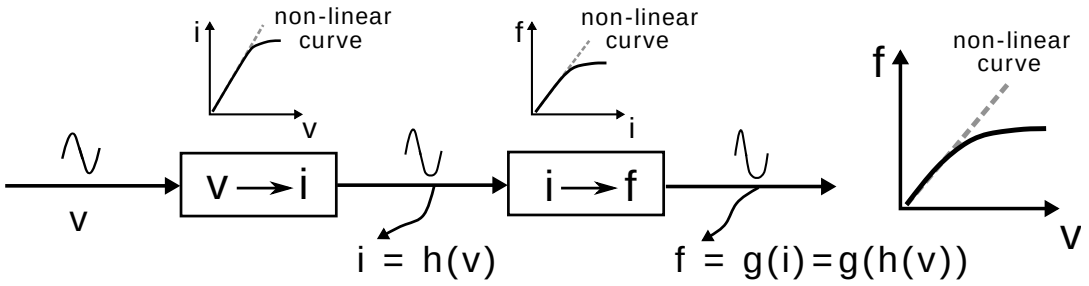
3.3 Multiple-Transconductor Ring Oscillator

In this part of the chapter, a new way to mitigate the distortion generated by the nonlinearity of ring oscillators is proposed, exploiting a circuit design with significantly lower power consumption and area comparing to prior art. The idea makes use of several transconductors with different bias conditions connected in parallel to inject the current into a CCO architecture. By means of selecting a

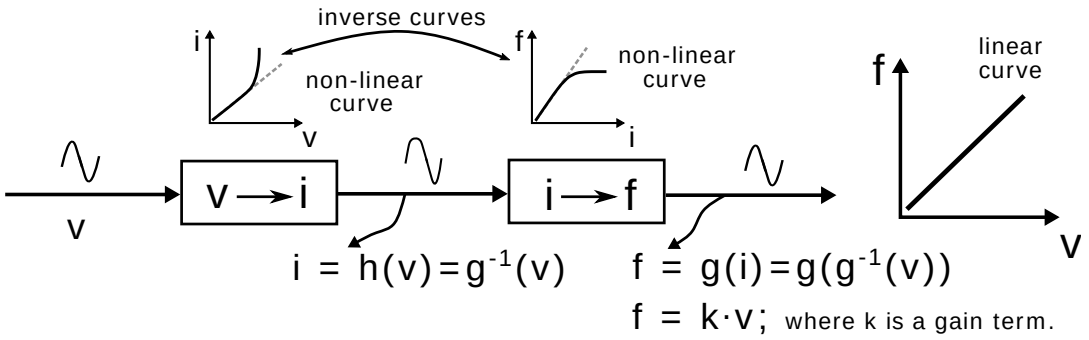
proper distribution of those bias conditions, a nonlinear voltage-to-current function that approximates the inverse nonlinear current-to-frequency CCO relation is implemented. Figure 3.13 depicts a scheme that summarizes the idea described above. The VCO is composed of an input stage that converts an input voltage into a current, and a CCO that makes a current-to-frequency translation as illustrated in Figure 3.13(a). The transfer functions of both the front-end circuit and the ring oscillator compose the whole response of the VCO as depicted in Figure 3.13(b). The current-to-frequency transfer function of the CCO is inherently nonlinear. This nonlinearity is compensated by artificially computing the inverse transfer function through the voltage-to-current relation in the front-end circuit as shown in Figure 3.13(c). Something similar is already proposed in [27] with a resistive divider as the RO front-end circuit. The main disadvantage is that the input signal attenuation directly entails a lower dynamic range.



(a) General scheme of a VCO.



(b) Nonlinear VCO operation.



(c) Proposed linearization technique.

FIGURE 3.13: General scheme of a VCO and response.

This proposal is evaluated by transient simulation with a low power (LP) TSMC 65-nm CMOS process, showing excellent performance in power and area, especially compared to digital calibration techniques [20], significantly reducing the THD power. In addition, PVT variation and Monte Carlo simulations prove that the solution is robust against those variations, but requiring calibration to achieve substantial distortion enhancement and proper resolution improvement for high-swing input signals. Finally, the proposed circuit is completely scalable as the calibration is also performed digitally, making it suitable for PVT/mismatch compensation in very deep submicron CMOS nodes such as 16-nm or 7-nm.

This part of the chapter is structured as follows. Section 3.3.1 illustrates the performance of a VCO-based ADC with a typical open-loop configuration (similarly to Section 3.2 but with others parameters) and describes the proposed idea to compensate for the VCO inherent nonlinearity response. Circuit implementation details and simulations results are provided in Section 3.3.2. Section 3.3.3 introduces a scheme for a foreground calibration and explains the basis of the proposed circuit.

3.3.1 Foundations of proposed multiple-transconductor RO

3.3.1.1 Nonlinearity in Ring Oscillators

A behavioral model of Figure 2.9(c) is designed in a 65-nm CMOS technology, using the most common structure for a VCO with a ring oscillator of Figure 2.11. The model in pseudo-differential configuration included a 45-phase ring oscillator per branch with the rest of the blocks modeled with Verilog-A. The sampling frequency (f_s) is 2 GHz with a bandwidth of 50 MHz. The oscillation parameters are $f_o = 450$ MHz and $K_{VCO} \cdot g_m = 1$ GHz/V, for a sinusoidal differential input signal of 800 mV_{pp}. The nominal voltage supply is 1.2 V.

Figure 3.14 depicts the spectra of the output data y[n] resulting from transient simulations for several input tones within the bandwidth: 3, 11 and 48 MHz. The harmonic distortion is clearly visible, with HD3 and HD5 terms equal to -44 dBc and -68 dBc, respectively (HD2 term is -39 dBc in a single-ended configuration). The average SNR is 64 dB and the SNDR is 44 dB for the cases whose harmonics fall inside BW (3 and 11 MHz input tones), which means a degradation of approximately 3 ENOBs due to distortion. In general, a peak SNDR higher than 50 dB becomes impossible for high input swings (hundreds of mVs), making this architecture unsuitable to achieve 10-12 ENOB of resolution within 5G-6G (WLAND) environments.

3.3.1.2 Foundations of the proposal

Figure 3.15 displays the voltage-to-frequency response and the linearity error of the oscillator simulated above. The ideal linear response has also been plotted.

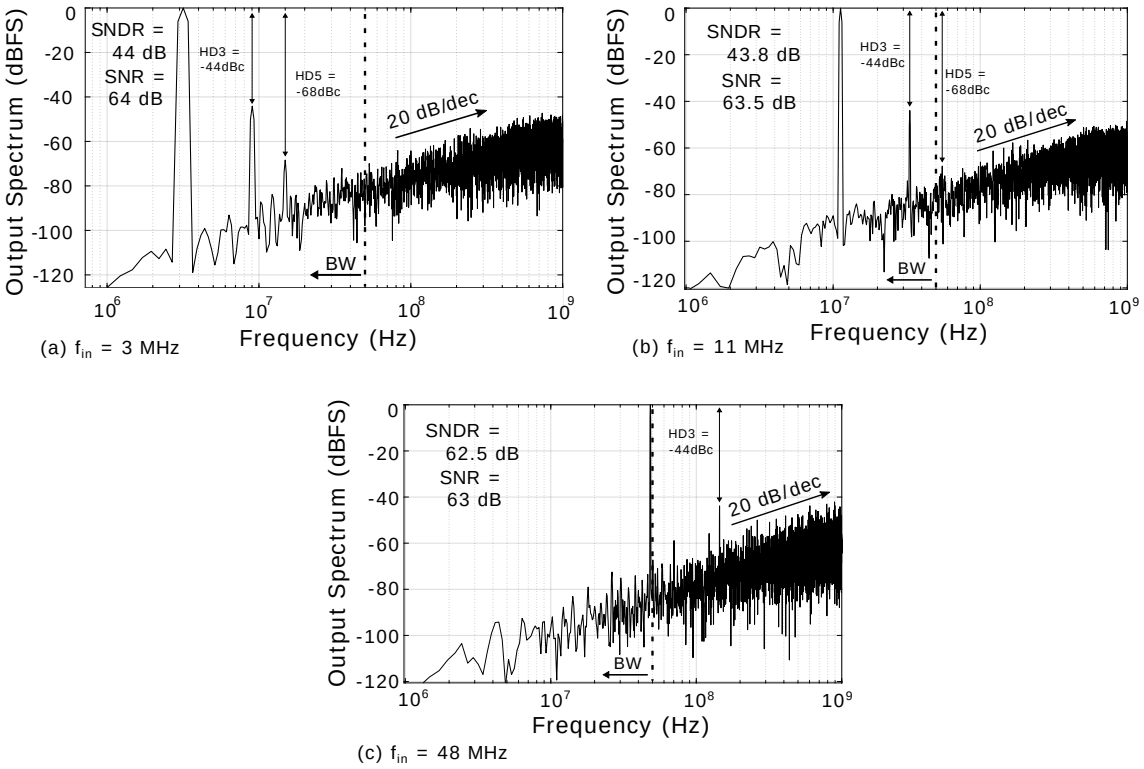
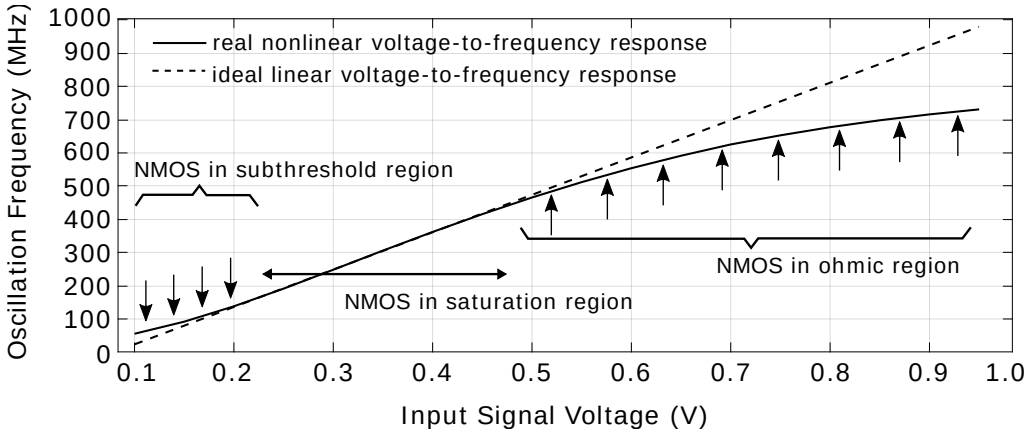


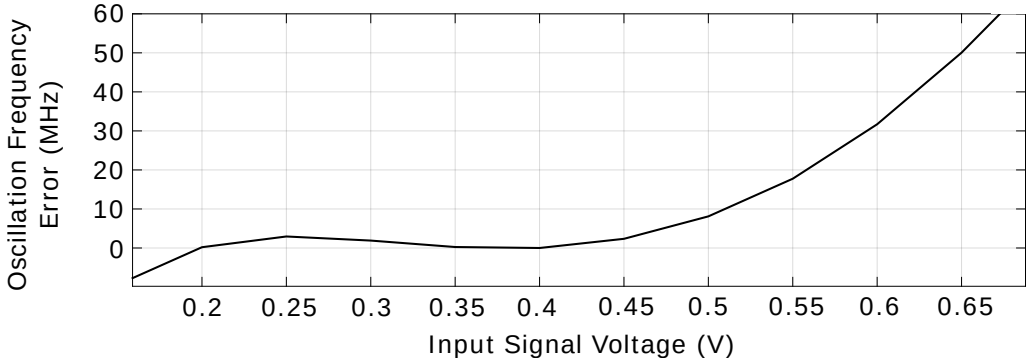
FIGURE 3.14: Distortion due to the RO nonlinearity in a pseudo-differential VCO-based ADC at several input tones, fin: 3, 11 and 48 MHz.

Assuming the ring oscillator configuration of Figure 2.11(a), three different regions for the NMOS transistor are distinguished: the saturated region, where the ring oscillator shows a behavior approximately linear; and the subthreshold and ohmic regions, where the nonlinearity is clearly visible. For the input signal voltage set as 0.25 V to 0.65 V, the useful range of the ring oscillator curve is from 200 MHz to 600 MHz, where the maximum deviation of the oscillation frequency from the linear approximation is 50 MHz which corresponds to a 12%, as can be observed in Figure 3.15(b).

When having the NMOS working at such regions, the harmonic distortion will increase due to the joint action of both the nonlinear voltage-to-current conversion and the nonlinear time delay dependence of the taps that compose the ring oscillator. This restricts the linear operating region to a small input voltage range, which might be suitable for low-swing input voltage applications [28], but not for high-swing ones. To increase the linear voltage range, more current may be injected into the oscillator in the ohmic region to move the curve up, and drained in the subthreshold region to move the curve down, as indicated by the arrows in Figure 3.15(a).



(a) Voltage-to-frequency conversion function of a conventional ring oscillator (solid line) and an ideal linear curve estimation (dashed line).



(b) Oscillation frequency error of a conventional ring oscillator.

FIGURE 3.15: Voltage-to-frequency response and linearity error of a conventional ring oscillator.

With that purpose in mind, a circuit-level solution to extend the linear response of the ring oscillator is proposed. The solution is based on handling the current injected into the ring oscillator with several transistors, instead of a single one, shifting the saturation regions of them throughout the whole desired input voltage range. This way, firstly, at least one device is working always in saturation at any point of the input voltage range, getting an approximately linear voltage-to-frequency response, and secondly, there is more flexibility to control the injected current into the ring oscillator and perform a voltage-to-current conversion that mitigates the distortion due to the nonlinear time dependence of the taps in the oscillator. Looking at Figure 3.15(a), two current-based operations are needed: injection and draining, requiring respectively both NMOS and PMOS-based devices in the front-end circuit (see Figure 3.16). Thus, the current flowing through the ring oscillator $I_{RO}(t)$ can be expressed as follows:

$$I_{\mathrm{RO}}(t) = \sum_{i=1}^{M} I_{\mathrm{N,i}}(t) - \sum_{j=1}^{N} I_{\mathrm{P,j}}(t), \tag{3.7}$$

where $I_{N,i}(t)$ is the current provided by the i-th NMOS device, and $I_{P,j}(t)$ is the current drained by the j-th PMOS device.

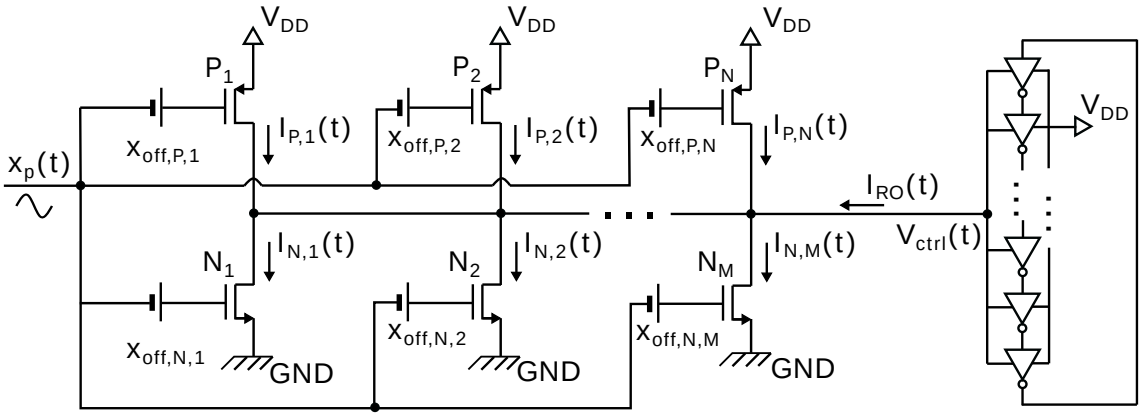


FIGURE 3.16: Circuit-based solution with several transistors to extend the linear response of conventional ring oscillators.

Using both PMOS and NMOS devices may suppose issues arising from matching and more complexity making the calibration of the circuit. That is the reason why, for a proof of concept, it is decided to correct and extend only the ohmic region by means of NMOS devices. Several NMOS devices are then connected in parallel. Each of these devices has its own offset component to control the point when they get into the saturation region. Figure 3.17 depicts a diagram of the proposed solution with a ring oscillator whose input current is provided by M NMOS devices, where $x_{off,i}$ represents the offset voltage for each of the transconductors. These offset values must be allocated throughout the desired input voltage range to feed the proper current that approximates the inverse current-to-frequency relation of the ring oscillator. Linearity is kept mainly because there is always at least one transconductor which is providing sufficient transconductance. For the case of Figure 3.17, the total transconductance, g_{mT}, is as follows:

$$g_{\mathrm{mT}} = g_{\mathrm{m,N1}} + g_{\mathrm{m,N2}} + ... + g_{\mathrm{m,Nm}}. \tag{3.8}$$

On this basis, although the rest of transconductors are still providing some current gain, as $g_{m,sat} \gg g_{m,ohmic}$ the transconductance contribution of the devices operating in the ohmic region are negligible compared to the one working in saturation, resulting in: $g_{mT} \simeq g_{m,Ni}$, where $g_{m,Ni}$ is the transconductance of the

transistor that is working in saturation. It is important to note that this method approximately computes the inverse current-to-frequency function of the ring oscillator making use of the voltage-to-current response of single transistors, so the removal of harmonic distortion is not complete, as will be shown later.

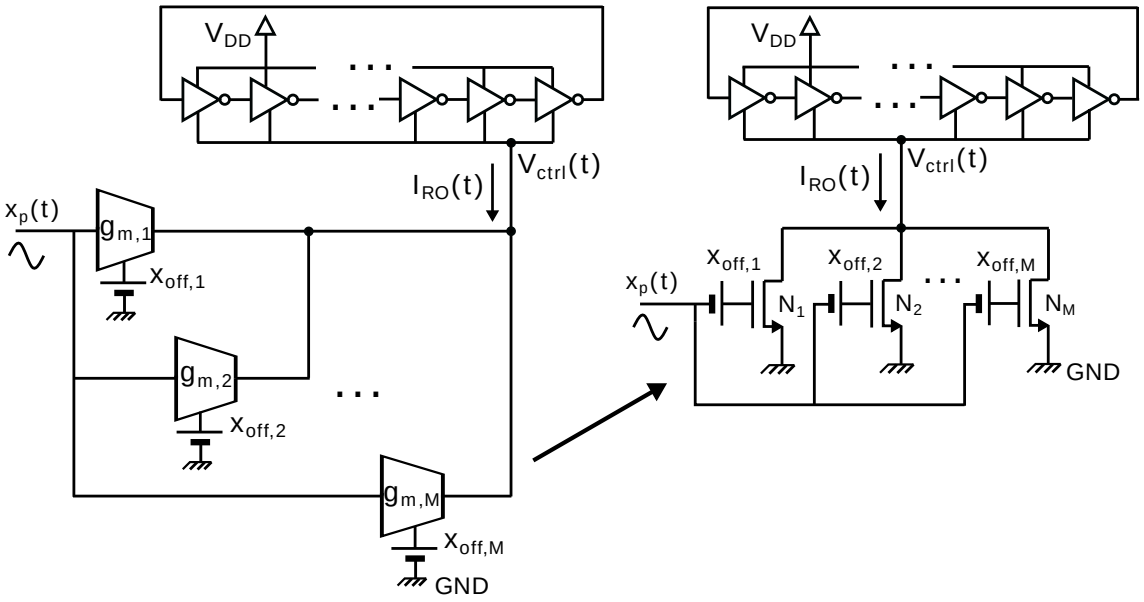
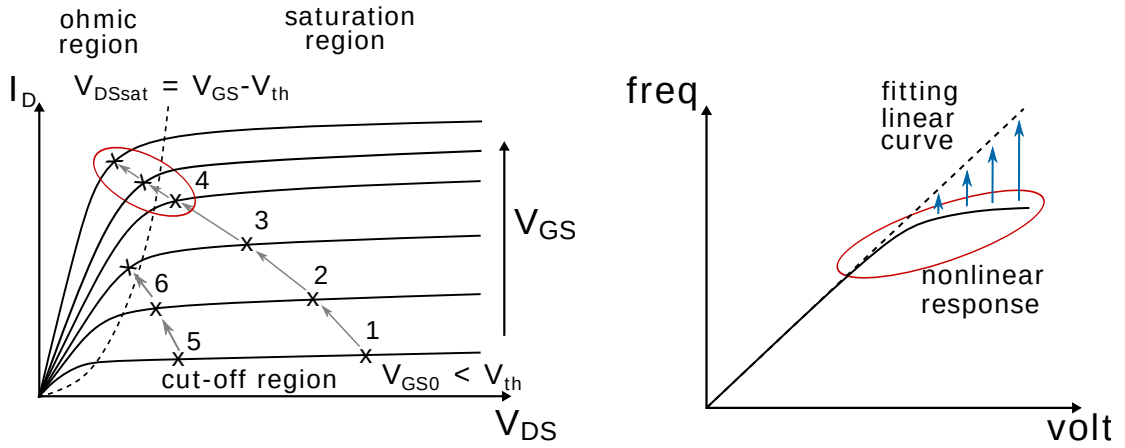


FIGURE 3.17: Proposed multiple-transconductor circuit for a linear RO-based A/D conversion.

Apart from the mitigation of the nonlinearity, the proposed structure could also be used to enhance the oscillator gain K_{VCO}. Note that, for the conventional approach (Figure 3.15), the oscillator gain is limited because the transconductor g_m drops into the ohmic region and is not able to provide sufficient current to keep increasing the oscillation frequency with the same slope as in the saturation region. With the proposed solution, at any point of the selected input range, there is at least one transconductor providing enough current to keep a linear relation, so that the highest achievable oscillation frequency increases.

Figure 3.18 summarizes the foundations of the proposed circuit: assuming a starting point with low V_{GS} (which is actually the input voltage, $x_p(t)$ in Figure 3.17) and increasing it. The operating point is shifted (grey arrow paths) throughout the I_{DS}-V_{DS} curves from numbers 1 to 4 (in our case, $V_{DS} = V_{ctrl}$). When the CMOS device gets into the ohmic region (number 4, red circled area for the black I_{DS}-V_{DS} curves) the ring oscillator transfer function starts to flatten out (red circled area in the frequency-to-voltage curve). At this point, another transconductor operating in the saturation region (number 5, blue I_{DS}-V_{DS} curves) provides the required current to maintain the linearity (blue arrows in

the freq-volt curve). The new transconductor is sized in such a way that the additional limited current provided by the former CMOS device (now in the ohmic region) is still keep in mind.



(a) Transconductors' operating points.

(b) Linearization of RO's volt-to-freq response.

FIGURE 3.18: Foundations of the proposed circuit operation.

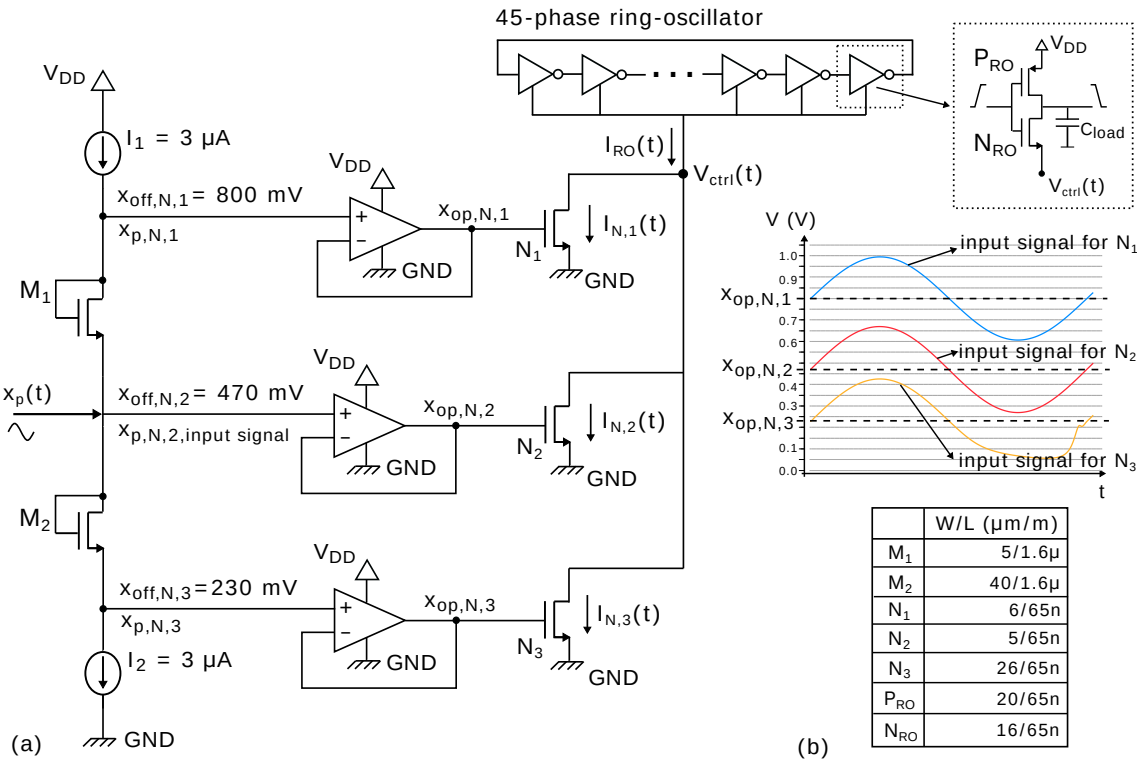
3.3.2 Results

3.3.2.1 Circuit Validation

To evaluate the proposed architecture, a version of the circuit of Figure 3.17 is designed in a 65-nm CMOS process with a pseudo-differential configuration, as illustrated in Figure 2.9(c), and 45 phases in the ring oscillators. Digital demodulation and sampling logic are modeled in VerilogA language. 10-fF capacitors are placed at the outputs of the ring oscillator to simulate the input capacitance of the digital logic. The front-end circuit of the ring oscillator, together with the circuit used to trim the offset component of each transconductor, is shown in Figure 3.19.

The front-end circuit and the current-controlled oscillator

The offset component of the input signal is one of the offset references needed, and the other voltage references are generated by means of fixed bias currents and diode-connected transistors M_1 and M_2 (as resistive dividers). In our case, three offset references are needed, with the values displayed in Figure 3.19. M_2 operates in subthreshold because of the limited available headroom. This does not suppose a significant difference as if this device would be working in saturation. Subthreshold current can be defined as $I_d = I_{d0} \cdot (W/L) \cdot e^{(V_{GS}/(nkT/q))}$, so while keeping constant I_d (3 μA), $V_{DS,M2}$ will remain.



	W/L (µm/m)
M_1	5/1.6µ
M_2	40/1.6µ
N_1	6/65n
N_2	5/65n
N_3	26/65n
P_{RO}	20/65n
N_{RO}	16/65n

FIGURE 3.19: Trimming circuit used to generate the offset references of the ring oscillator: (a) schematic; (b) device's sizes and chronograms.

The size distribution of the transconductors is chosen according to a static behavior, performing a sweep of several transient simulations with different DC input values to get the voltage-to-frequency relation and quantify the nonlinear coefficients. In Figure 3.20 the currents of the three transconductors are plotted against the input voltage ($x_p(t)$ in Figure 3.19). It can be seen that when N_1 gets into the ohmic region, N_2 is providing the main current, and when N_2 gets into the ohmic region N_3 provides the main current.

In general, the higher the number of transconductors the higher the accuracy to approximate the inverse oscillator's current-to-frequency, but the higher the complexity. This solution with three transconductors achieves a proper trade-off between linearity performance and complexity for a single-ended input signal voltage of 400 mV_{pp}. Figure 3.21(a) depicts the voltage-to-frequency conversion response of the circuit proposed in Figure 3.19. It can be observed the linear performance for voltages between 0.27 V and 0.67 V. Figure 3.21(b) illustrates the difference between the expected linear voltage-to-frequency response and the real one (in Figure 3.21(a) the dashed line and the solid line). The highest error between both transfer functions against the input voltage for TT with 27°C, corresponds to 0.06%, with a maximum deviation value of 300 kHz, of the full scale

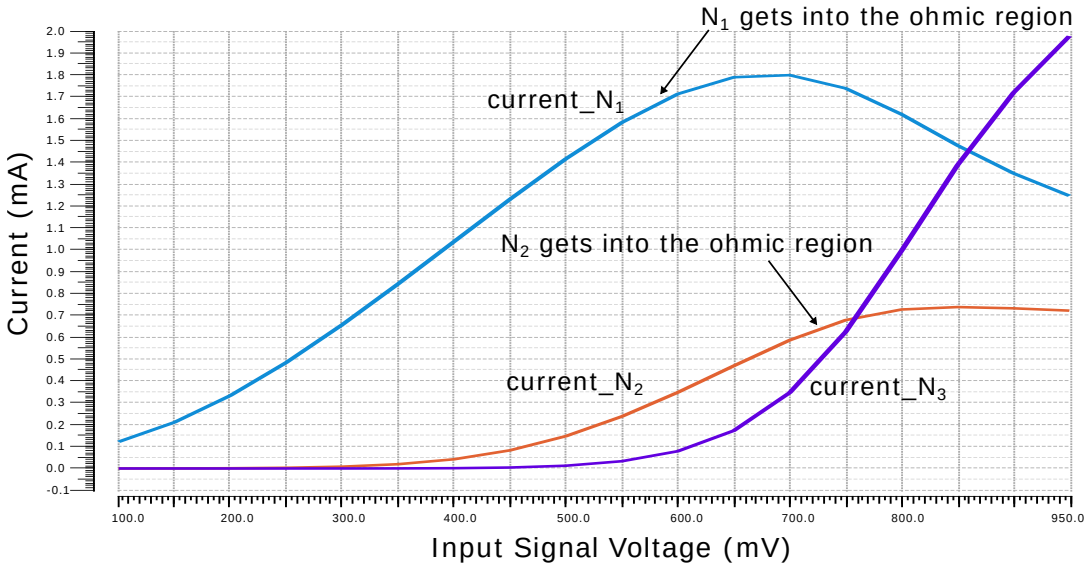


FIGURE 3.20: Currents of the three transconductors in Figure 3.19.

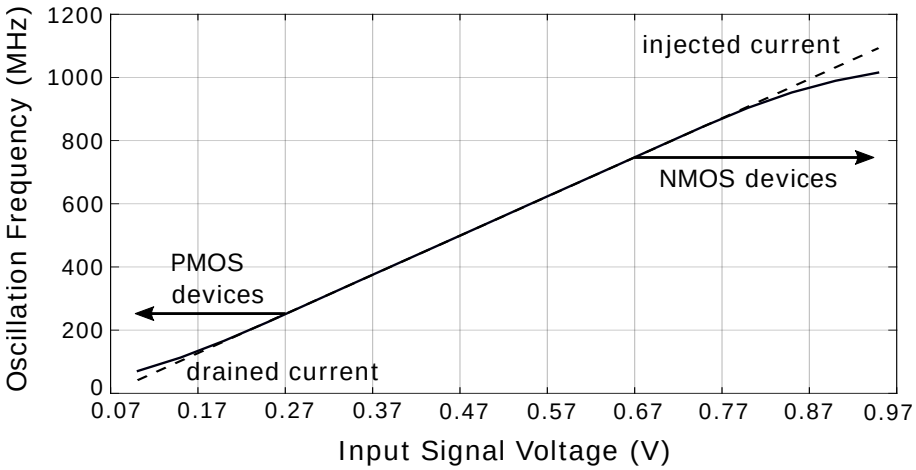
for a single-ended amplitude range of 470 mV $\pm$ 200 mV. A similar measurement can be found in [27], where an error equal to 0.6% for a single-ended input signal of 500 mV_{pp} in a 65-nm test chip is claimed.

In addition, the input swing can be expanded and the linearity can be effectively controlled by using more transconductors. Although for the proof of concept of this work only NMOS-based transconductors are used, with PMOS-based transconductors we can also extend the linear range by decreasing the lowest input voltage. The highest input voltage is defined by the supply voltage, but with enough voltage supply it could also be expanded.

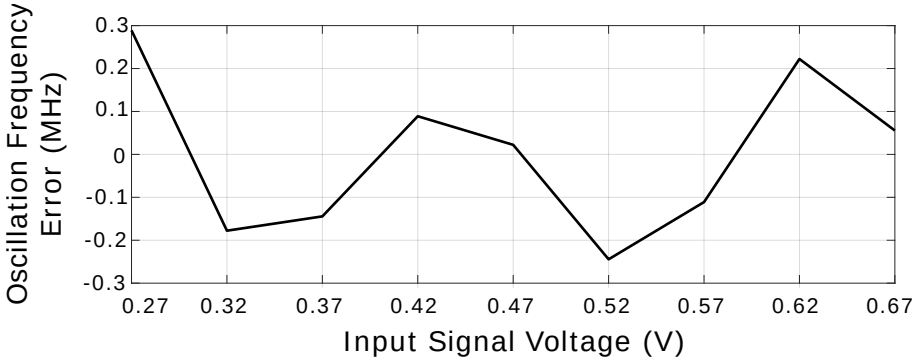
The real curves of the representation in Figure 3.13 can be observed in Figure 3.22. Both the voltage-to-current and the current-to-frequency curves are inverse. They are obtained by making an input voltage sweep with a step of 50 mV within the input amplitude range (470 mV $\pm$ 200 mV). Then the oscillation frequency is extracted from Cadence and a 9^{th} degree polynomial approximation is made in MATLAB, as depicted Figure 3.21(a).

Both the current sources in the top and in the bottom part of the branch are assumed to be ideal for simulations. To provide more reliability to the proposed idea, the ideal current sources are replaced with current mirrors, as shown in Figure 3.23. A transient simulation is performed to check their performance.

Figure 3.24 depicts different input signals $V_{p,N,i}$ which are the inputs of the opamps ($x_{p,N,i}$) for both the ideal current sources and current mirrors. It can be observed that they match correctly with slight differences that are negligible and do not affect the performance of the solution presented. The resulting output spectrum is unaltered by using the current mirrors.



(a) Voltage-to-frequency conversion function of the circuit in Figure 3.19: the solid line represents the transfer function of the proposal (f=k·v in Figure 3.13(c): the front-end circuit + the current-controlled oscillator), and the dashed line corresponds to the linear prediction.

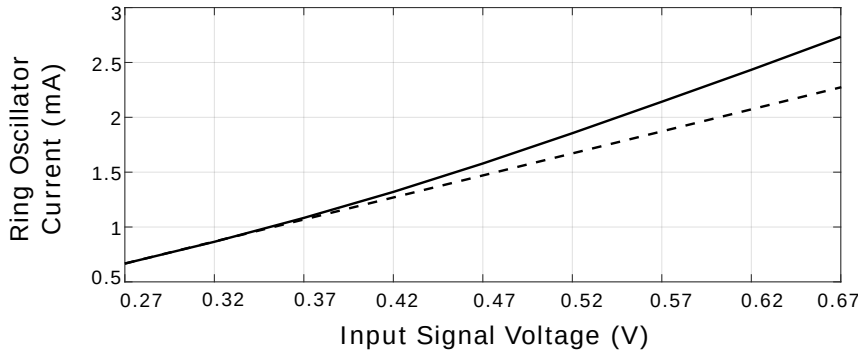


(b) Frequency error of the system with the circuit proposed in Figure 3.19.

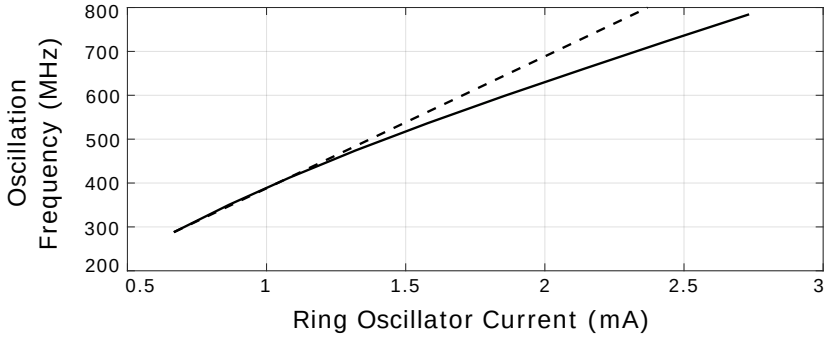
FIGURE 3.21: Voltage-to-frequency conversion function and linearity error of the circuit in Figure 3.19.

Operational amplifier

Low-power opamps connected in a buffer configuration are used to avoid kick-back noise. The opamp does not require high DC gain, hence its design does not lead to a technology scaling issue. The gain-bandwidth product value is 200 MHz and the margin phase is 55°, ensuring the proper operation of the system (see Figure 3.25). Figure 3.19(b) illustrates the time response of $x_{op,N,1}$, $x_{op,N,2}$, and $x_{op,N,3}$ from a transient simulation where $x_p(t)$ is a sinusoidal signal. The unitary gain configuration is accomplished totally for $x_{op,N,1}$, $x_{op,N,2}$, and partially for $x_{op,N,3}$, which gets distorted for voltage values lower than the threshold voltage (around 0.25 V). This is not relevant because, for gate voltage values lower than the threshold voltage, N_3 operates in the subthreshold region, and the current provided is negligible.

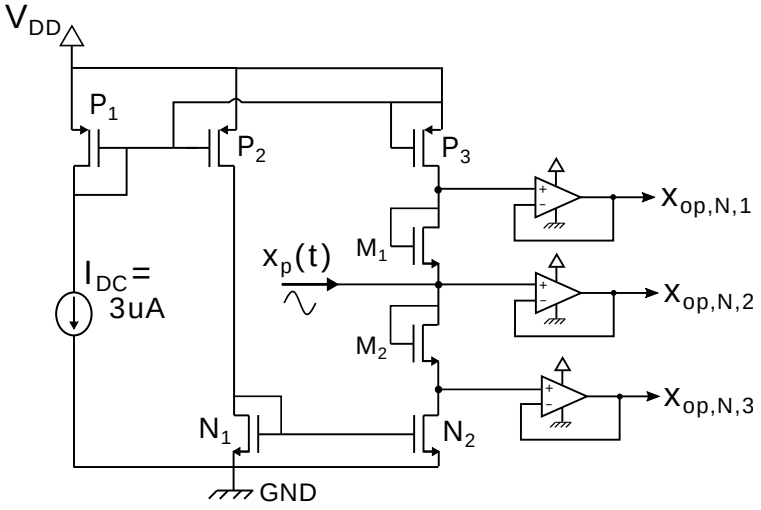


(a) Voltage-to-current function implemented in the front-end circuit, i=h(v) in Figure 3.13(c).



(b) Current-to-frequency function of the CCO, f=g(i) in Figure 3.13(c).

FIGURE 3.22: Real curves for the proposed idea of Figure 3.13(c): the dashed lines represent the ideal linear curves.



(a) schematic

	W/L (µm/m)
N_1	1/200n
N_2	1/200n
P_1	1/200n
P_2	1/200n
P_3	1/200n
M_1	5/4.6µ
M_2	40/1.6µ

(b) device's sizes

FIGURE 3.23: The front-end circuit with current mirrors.

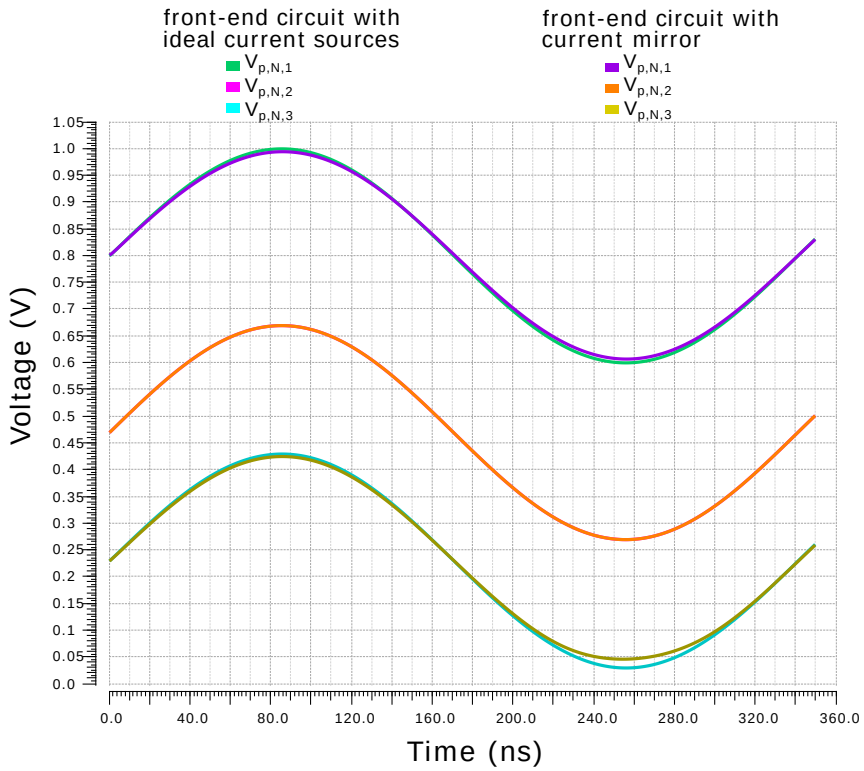


FIGURE 3.24: Input signals of the opamps for both the ideal current sources and current mirrors circuit.

In the proposed solution, N_3 is the transconductor enabled for the highest input voltage. It is required in saturation region when the input amplitude exceeds around 350 mV (see Figure 3.20), which is a sufficient voltage to make the buffer work properly. The frequency response of the unity-gain connection of the opamp for a DC voltage of 350 mV shows that the unitary gain remains constant within the whole band of interest (BW = 50 MHz).

The opamp shows small offset, around 3 mV, which is sufficiently low for proper performance. Opamp's circuit is depicted in Figure 3.26, which consists of a two-stage Miller-compensated opamp.

Nonlinearity mitigation

Transient simulations are used to check the nonlinearity mitigation. Oscillation parameters are kept similar to Figure 3.14, except $K_{VCO} \cdot g_m$, which is equal to 1.25 GHz/V, slightly higher than before due to linearity compensation. Figure 3.27 depicts the results of nominal transient simulations with the input signal frequency at 3, 11 and 48 MHz. The HD3 and HD5 are equal to -67 and -75 dBc,

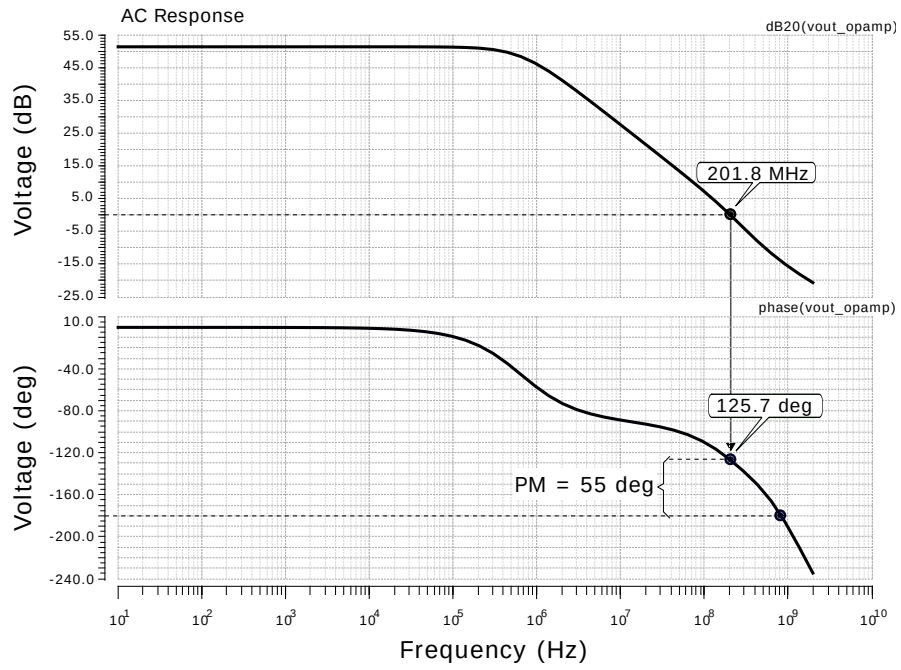
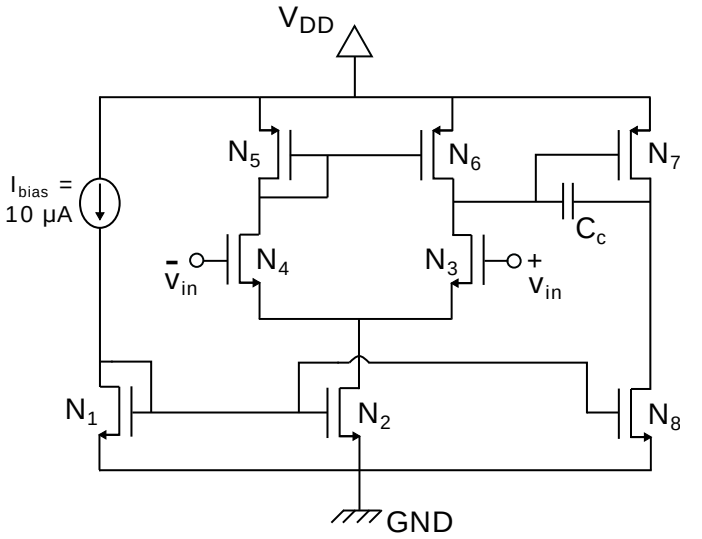


FIGURE 3.25: Open-loop frequency response of the opamp: AC magnitude and phase.



(a) schematic

	W/L (µm/nm)
N_1	1/200
N_2	1/200
N_3	60/200
N_4	60/200
N_5	2/200
N_6	2/200
N_7	60/200
N_8	10/200
C_c	50f F

(b) device's sizes

FIGURE 3.26: Two-stage Miller-compensated opamp.

respectively, leading to an SNDR of 63 dB (the HD2 value observed in a single-ended configuration is -63 dBc). The distortion is substantially mitigated in comparison to Figure 3.14. The proposed solution achieved a THD value of -66.4 dBc

for a differential input of 800 mV_{pp}, while [20] reported a THD chip measurement of -63.6 dBc for a differential input of 566 mV_{pp}, and [31] reported a THD of -65.3 dBc for a differential input of 400 mV_{pp} in simulation.

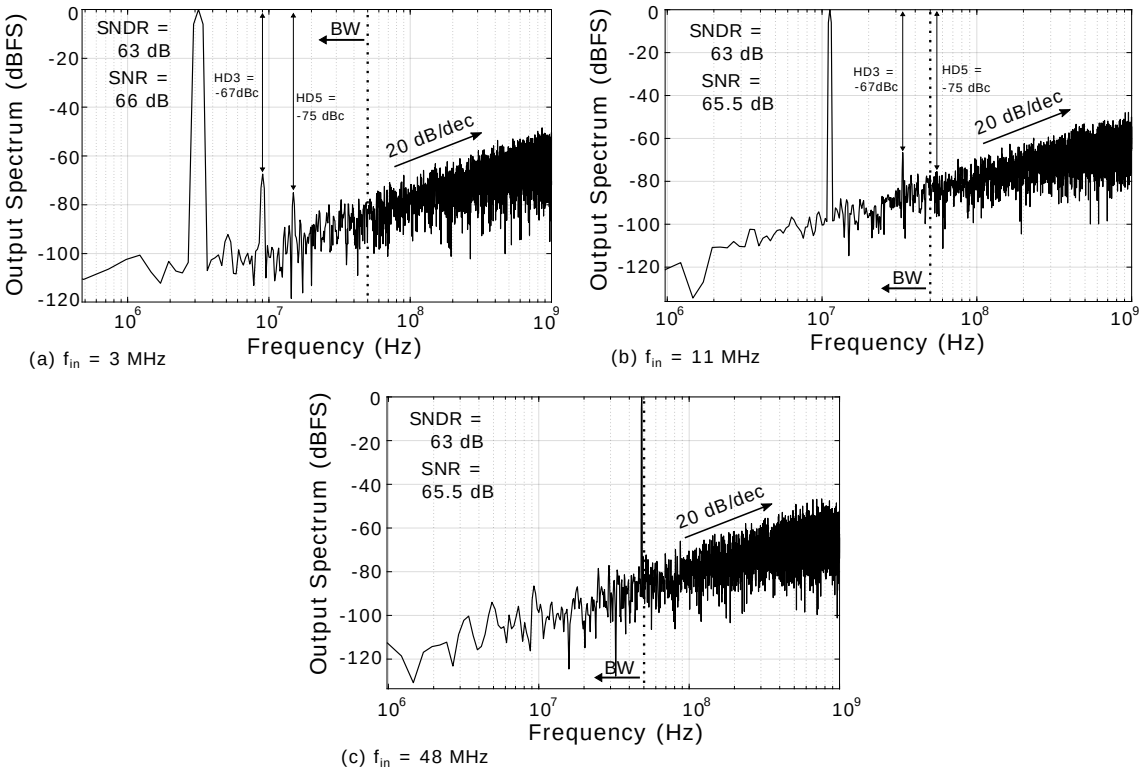
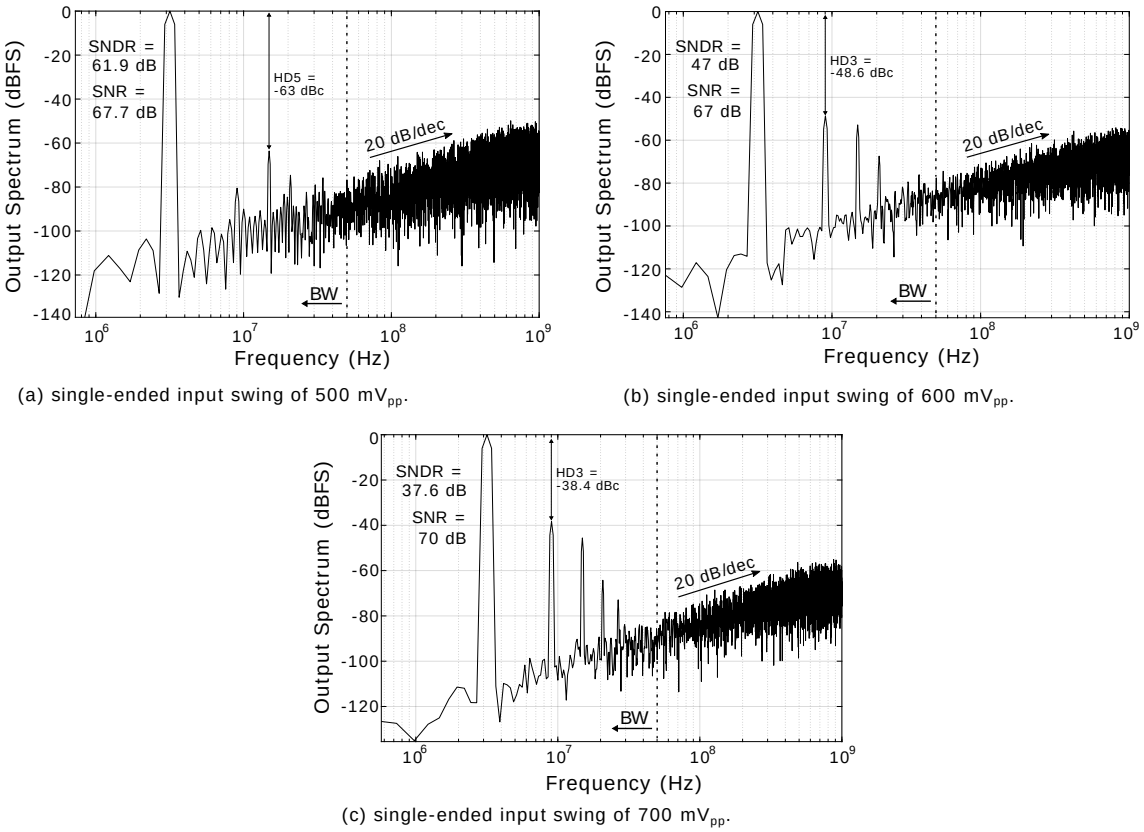


FIGURE 3.27: Output spectra of pseudo-differential VCO-based ADC with the circuit proposed in Figure 3.19 for several input signal frequencies, fin: 3, 11, and 48 MHz.

In order to illustrate the distortion for voltages below 0.27 V and above 0.67 V, the output spectra of the circuit are simulated for several input swings higher than 400 mV_{pp}: 500, 600 and 700 mV with a DC offset of 0.47 V. Figure 3.28 shows how the resolution is affected, evaluated in TT process, temperature of 27°C with a nominal voltage supply of 1.2 V. For an input amplitude of 500 mV_{pp} (single-ended), the resulting SNDR is not significantly reduced, but it is not the case for other corner process nodes where the performance is drastically reduced.

In addition, to fully characterize the input capacitance effect of the digital interface, several simulations is performed with different loads: 30, 50, 75, 100, 125 and 150 fF. Figure 3.29 depicts the voltage-to-frequency responses for several capacitance values. The analysis is performed up to 150 fF, considering that parasitic effects due to layout will not suppose such a large capacitance.



(a) single-ended input swing of 500 mV_{pp}.

(b) single-ended input swing of 600 mV_{pp}.

(c) single-ended input swing of 700 mV_{pp}.

FIGURE 3.28: Output spectra for VCO input voltage swings higher than 400 mV_{pp}: (a) 500 mVpp, (b) 600 mVpp, and (c) 700 mVpp.

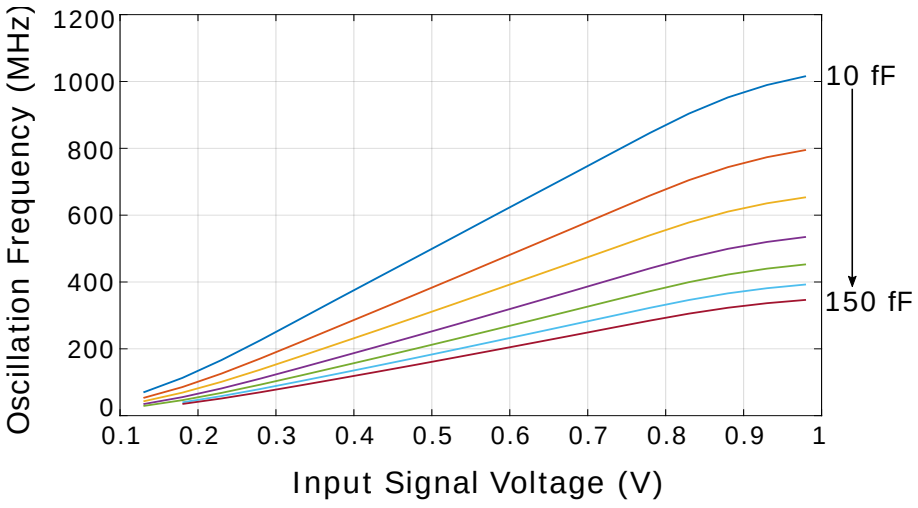


FIGURE 3.29: Voltage-to-frequency transfer functions for several loads at the RO output phases, from 10 to 150 fF.

The output spectra with different loads can be observed in Figure 3.30. The linearity properties are not affected and the decrease of the oscillator gain leads to a slight reduction in the SNR achieved.

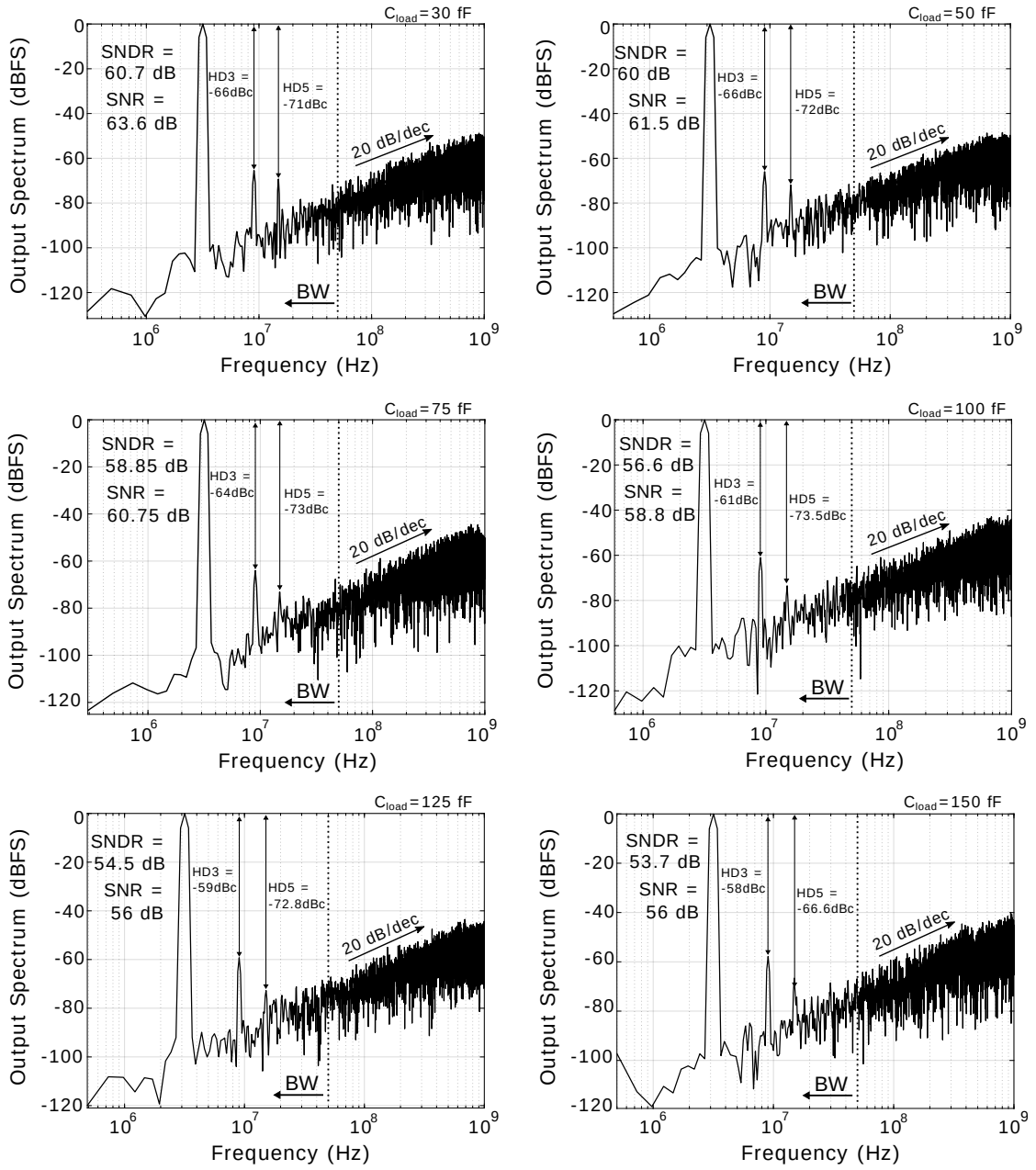
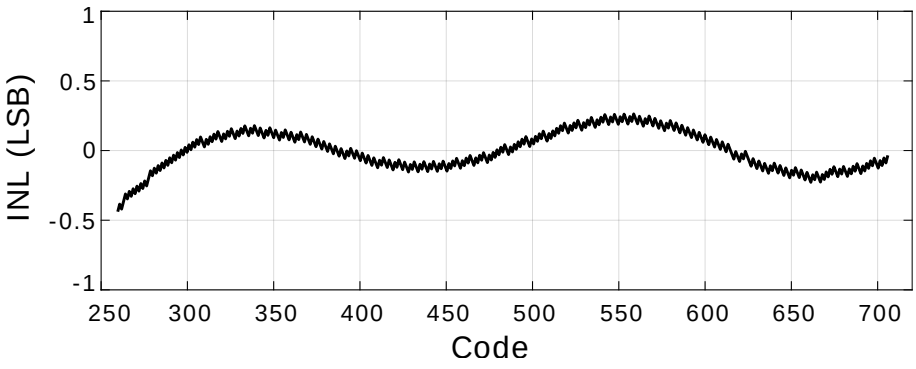


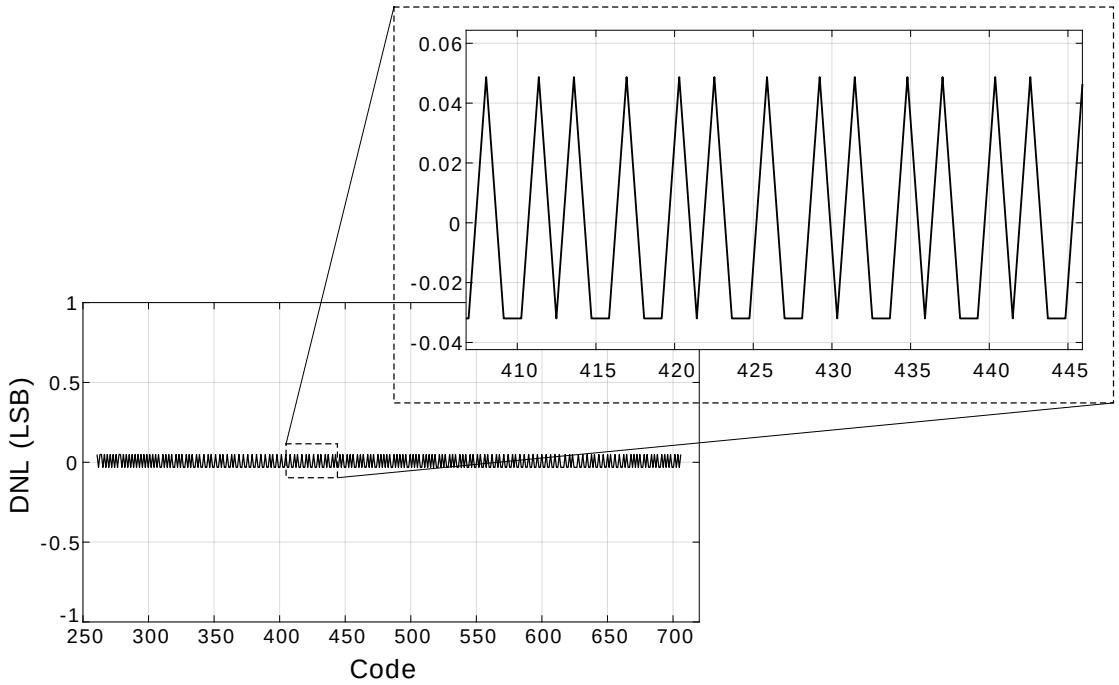
FIGURE 3.30: Output spectra for several loads at the RO phases, from 10 fF to 150 fF.

Integral nonlinearity (INL) performance, as a static characterization, is also analyzed. The results of a linear ramp test, using the best-fit straight-line approximation, are shown in Figure 3.31(a). The single-ended peak-to-peak INL error

is [0.44 0.26], within 1 LSB. In [89], a fully-synthesizable VCO-based ADC is presented, where the INL achieved after digital correction is in the range of [-1.40 1.49] LSBs and [1.90 1.60] LSBs for simulation and measurement results, respectively. Differential nonlinearity (DNL) for the proposal are in the range of [-0.032 0.049], as depicted in Figure 3.31(b). A detailed analysis about static parametrization with INL/DNL on VCO-based ADCs is presented in Appendix A.1.



(a) INL performance.



(b) DNL performance.

FIGURE 3.31: Static performance: INL and DNL of the VCO-based ADC with the circuit proposed in Figure 3.19.

3.3.2.2 Circuit-level Impairments

To achieve a correct performance from the proposed solution, proper offset references for each of the transconductors need to be selected. The ring oscillator will be affected by mismatch effects and PVT variations. This will result in variations in the oscillator current-to-frequency relation and in the required voltage-to-current function. The trimming circuit will be affected by these effects as well, modifying the transconductors' bias points. To reduce mismatch effects between devices, the diode-connected transistors (M_1 and M_2) are selected to be large.

Mismatching in the offset voltage for each of the transconductors

To analyze the variation of $x_{off,N,1}$, $x_{off,N,2}$, and $x_{off,N,3}$, and the oscillation frequency due to mismatch, a set of 300 runs (with mismatch and process variations) of Monte Carlo simulations is performed. These simulations is carried out making a voltage sweep in the VCO input signal, getting the oscillation frequency value in a range between 100 mV and 950 mV with a step value of 50 mV. The voltage variation is in the range between 4 and 9 mV with a maximum variation value observed for $x_{off,N,3}$. Data are exported and processed using MATLAB to calculate the RO voltage-to-frequency curve (like Figure 3.15 and Figure 3.21) with a polynomial approximation. The SNDR is estimated for 300 transfer functions with a Simulink behavioral model of the system in Figure 2.9(c). The SNDR is normally distributed with a mean value of 63 dB and a standard deviation of 1.8 dB, with a worst-case SNDR value, is equal to 59.5 dB. Figure 3.32 depicts the histogram plot for the probability distribution of the data and the probability density function (the orange line).

PVT variations

Apart from the mismatch verification, the impact of PVT variations in the VCO linearity is also checked. Figure 3.33 shows the voltage-to-frequency relation for different conditions considering variation process (SS, SF, FS, FF, TT) and temperature (-45°C, 27°C – environment temperature, +120°C): the curve for nominal condition (TT at +27°C, the blue one in the middle, curve number 5, and the solid blue line in Figure 3.21) is mainly shifted throughout the horizontal axis, but its shape did not vary significantly. Consequently, centering the input offset in the linear region is the easiest way to keep the oscillator working in a linear manner.

Figure 3.34 shows the SNDR values achieved for different PVT cases with the offset of the input signal ($x_{off,N,2}$) correctly tuned. SNDR degradation can be mainly observed for high temperatures. This degradation occurs when all the transconductors drop into the ohmic region (right side of Figure 3.15) due to the limited V_{ctrl}. Looking at Figure 3.17, the higher $I_{RO}(t)$, the lower V_{ctrl} and the lower the voltage available to make N_1, N_2, ... N_M work in saturation. When

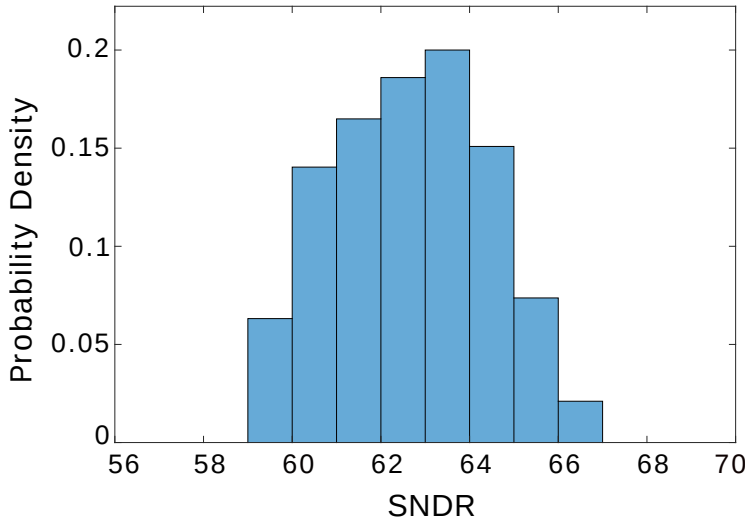


FIGURE 3.32: Histogram for SNDR data with Monte Carlo simulations and corresponding probability density function.

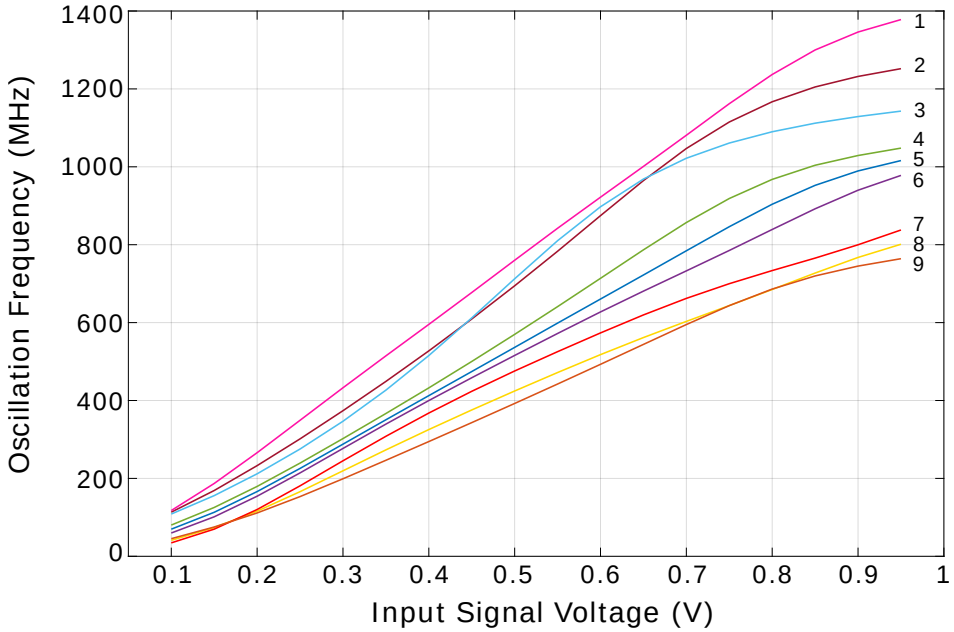


FIGURE 3.33: Voltage-to-frequency conversion functions for different PVT conditions: the extreme conditions (FF and SS processes at -45°C and +120°C, respectively - curves number 1, 3, 7, 9), and all processes (SS, SF, TT, FS, FF - curves 8, 6, 5, 4, 2) at environment temperature. The nominal voltage supply (1.2 V) is the same for all the cases.

dealing with +120°C the voltage drop in the ring oscillator (V_{DD}-V_{ctrl}) is higher, and V_{ctrl} is lower and the transistors get into the linear region for lower input voltages, limiting the linear operating region. In the FF case, the fast condition for the NMOS devices makes the transconductance values become higher, providing more current and reducing V_{ctrl} faster with the input voltage, resulting in the same phenomenon explained above. The linear operating region is reduced as well. In the particular case of FF +120°C (curve number 3 in Figure 3.33), this phenomenon is of special relevance because the working linear region is dramatically reduced. To improve the linearity of the proposed solution in these cases, the voltage supply could be increased at the expense of increasing the power consumption or resizing the ring oscillator at the expense of reducing the gain.

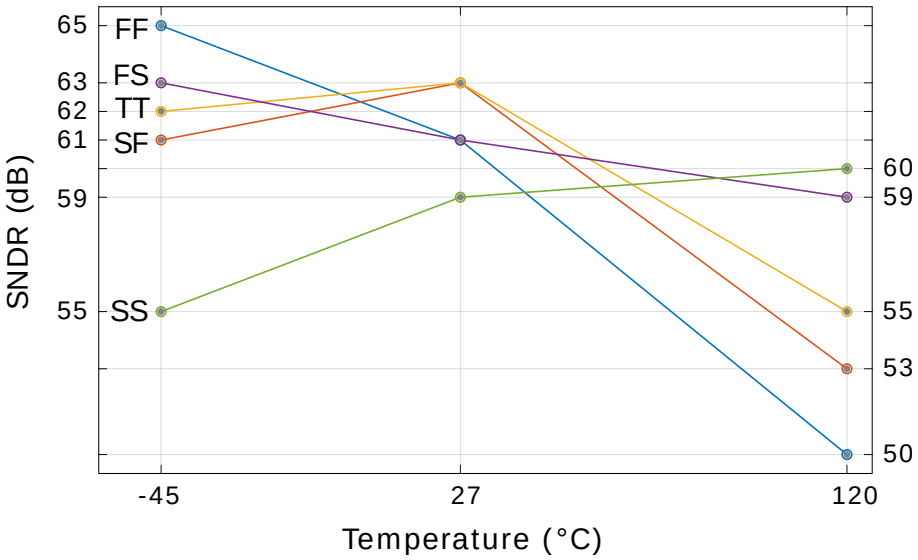


FIGURE 3.34: SNDR variation of Figure 3.27 due to different PVT conditions. Capital letters indicate devices' process: 'S' means "slow", 'F' means "fast", and 'T' means typical. The first letter refers to NMOS devices and the second one refers to PMOS devices. The nominal voltage supply (1.2 V) is the same for all the cases.

All of the simulation results depicted in Figure 3.34 is obtained with a nominal voltage supply of 1.2 V. The same simulations is repeated including a variation of $\pm$50 mV in the voltage supply. The resulting SNDR values did not differ from the ones shown in Figure 3.27, which means strong robustness against voltage supply variations.

Finally, periodic steady-state and phase-noise analyses are performed to evaluate the limitation that the oscillator imposes to the system in terms of phase noise [90]. The estimated value of SNDR regarding the oscillator phase noise is 71 dB, much lower than the quantization noise based SNDR limit observed in Figure 3.27.

3.3.3 Calibration circuit

A calibration circuit is required to correctly select the offset of the input signal $x_p(t)$, $x_{off,N,2}$, approximate the inverse current-to-frequency ring oscillator's function, and keep proper linearity. For that purpose, a digital foreground calibration circuit enabled periodically is proposed. The circuit is depicted in Figure 3.35. Its performance is based on measuring the rest oscillation frequency f_o, identifying the PVT operating point of the prototype and selecting the best input signal offset, similar to what is done in Figure 3.34. The rest oscillation frequency is measured by means of a digital delay chain (AND gates) that measures the semiperiod of the oscillating signal coming from one of the phases of the ring oscillator. The outputs of the AND gates are stored with flip-flops, whose outputs are thermometically-encoded and represent an estimate of the semiperiod of f_o. This digital word is connected to an array of XOR gates that selects the best offset of the input signal. This offset value is finally controlled by an opamp whose output offset component can be tuned. The presented idea is originally introduced in [91], here with some modifications.

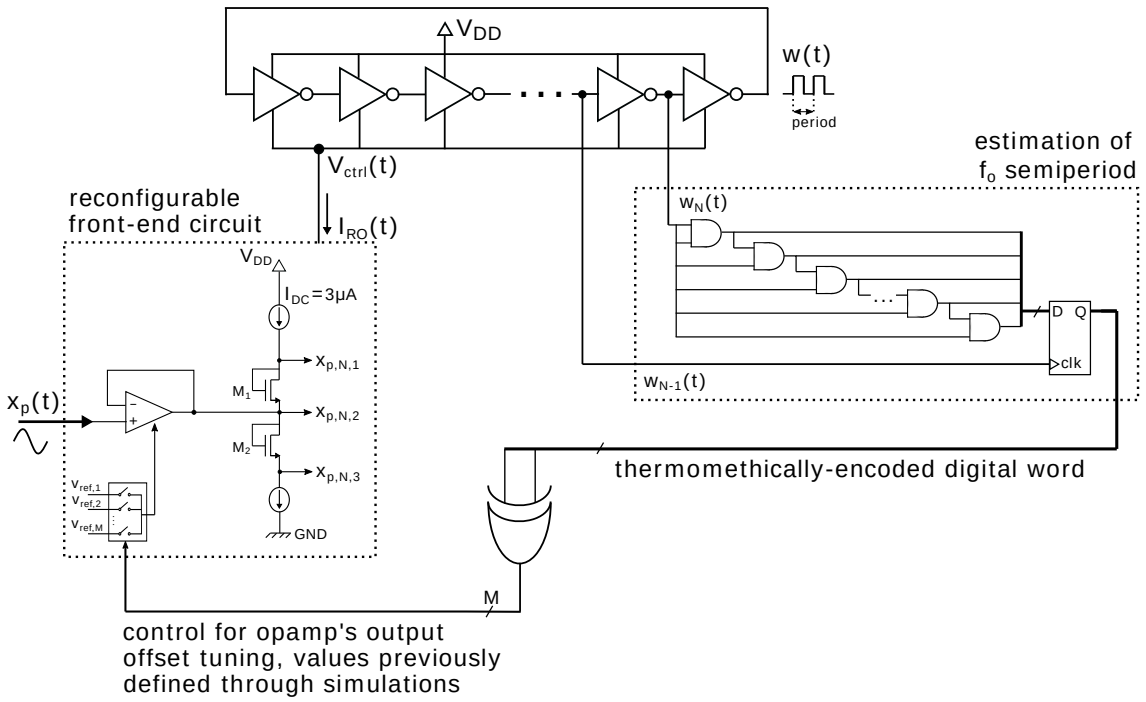


FIGURE 3.35: Scheme of the proposed calibration technique.

3.3.3.1 Circuit proposal

AND-based delay chain

The calibration consists of determining the PVT operating point of the RO. The RO oscillation frequency varies depending on the PVT condition, as observed in Figure 3.33. The proposed circuit will produce an estimation of the semiperiod of an RO output phase, w(t), using a fixed input voltage $x_p(t)$. This value is chosen in order to optimize area, because the proposed circuit suppose a foreground activity that does not increase significantly the power consumption.

The semiperiod of w(t) is computed by counting the time during which the VCO signal is high. For this, a delay chain is proposed, with an individual delay value in each cell defined by the smallest of two parameters (at most): the shortest time difference between two PVT conditions in order to distinguish two consecutive frequencies; and the shortest semiperiod that corresponds to the highest oscillation frequency. The number of chain elements is defined by the ratio between the cell delay and the longest semiperiod corresponding to the lowest oscillation frequency.

The elements of the delay chain are implemented with AND gates: the inputs are connected to the RO output phase and the output of the previous gate, except the first one whose both inputs are connected to the RO output phase (see Figure 3.35). When the RO output phase becomes '1', this logic value will be propagated through the AND gates until the phase turns into '0', cleaning all the cell outputs, as illustrated in the example of Figure 3.36. The circuit is based on considering the delay of a gate to measure the time during which w(t) is high.

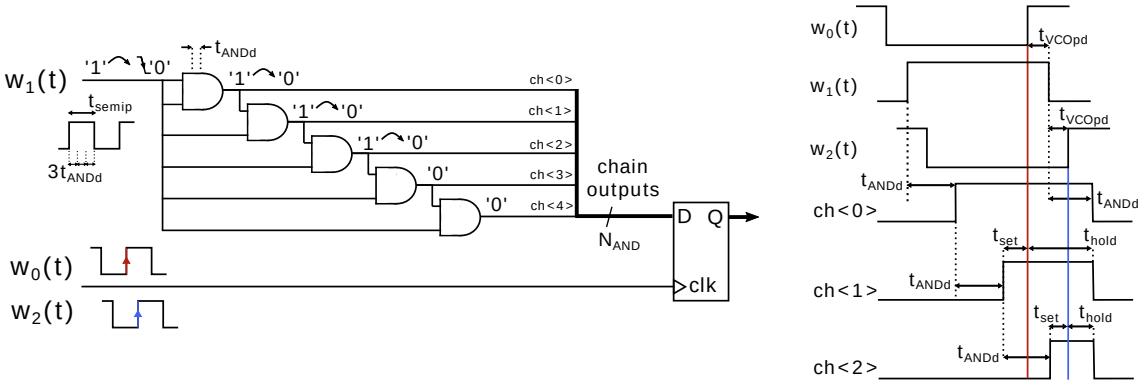


FIGURE 3.36: AND-based delay chain: schematic and chronogram.

To avoid losing data when a transition from '1' to '0' occurs, flip-flops register the chain outputs just before they reset. Using the preceding or the following output phase as the clock signal, the data are successfully sampled when the rising edge arrives, provided that the gate's delay time is greater than the propagation

delay of the RO's inverters. The flip-flop outputs are thermometer-coded and represents an estimate of the oscillation semiperiod. Thus, the semiperiod can be approximated, depending on which signal is used to sample, as follows: $t_{semip} = t_{ANDd} \cdot N_{high}$, or $t_{semip} = t_{ANDd} \cdot (N_{act}+1)$, the clock input of the flip-flops being the next phase and the previous phase respectively, where N_{high} is the number of delay units whose registered outputs are high, and t_{ANDd} is the AND delay time (see Figure 3.36). According to this proposal, a different thermometer code will be obtained for every oscillation frequency, thus allowing to establish the corresponding PVT condition.

To select the input voltage for the operating point identification, the period of signal w(t) is analyzed for every PVT condition making a voltage sweep in x_p. Figure 3.37 depicts the result. For the lowest voltage, 100 mV, the period values are much higher than the shortest time difference, leading to an excessive number of elements required in the delay chain. For the highest voltages, the period values are very close together, which entails an unfeasible minimum delay for the AND gates. A proper trade-off between the delay required in each AND gate and the amount of required AND gates is achieved at 250 mV.

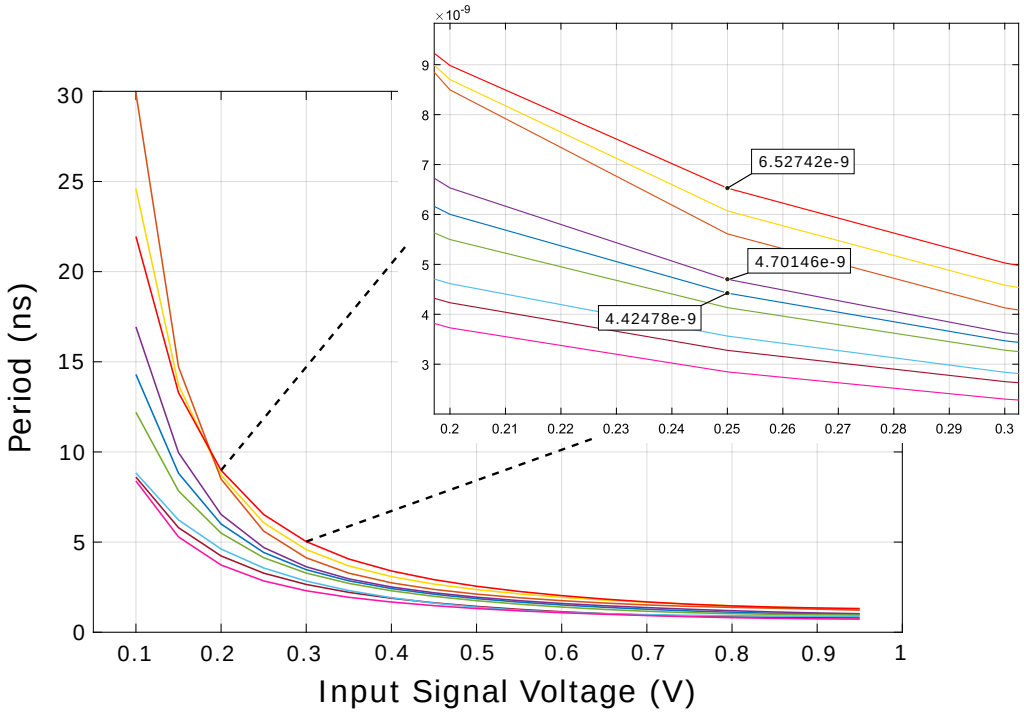
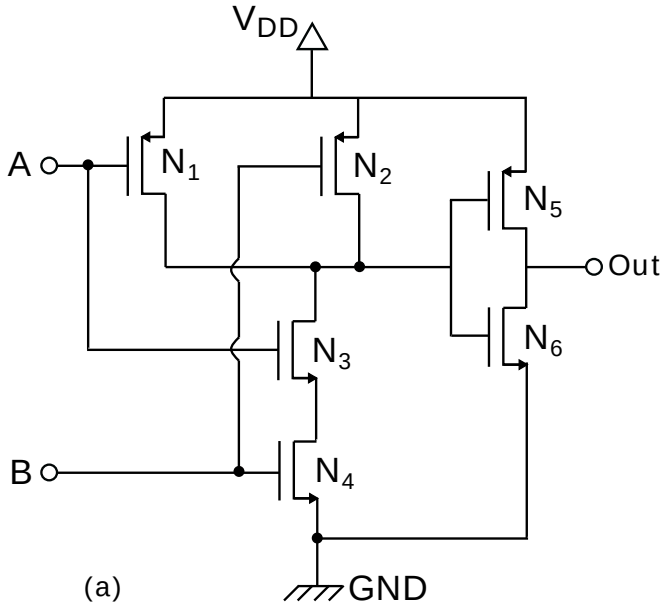


FIGURE 3.37: Period curves for every PVT condition.

Figure 3.37 shows the points with the shortest time difference that defines the delay required in a single AND gate (TT and FS processes with 27°C), and the longest period for this input voltage that corresponds to the total delayed by the chain (SS process with +120°C). The delay to be implemented for every unit is

138 ps, and the number of elements equals 24. The designed AND gate is built with a CMOS NAND structure followed by a NOT gate, as shown in Figure 3.38. A delay time of 133 ps with a voltage supply of 0.8 V is checked by simulation. The transistors used for the NAND gate circuit and the inverter circuits are high-voltage-threshold (hvt) type and low-voltage-threshold (lvt) type respectively.



	W/L (nm/nm)
N_1	120/65
N_2	120/65
N_3	120/65
N_4	120/65
N_5	240/65
N_6	120/65

(b)

FIGURE 3.38: AND gate circuit: (a) schematic, and (b) device's sizes.

The chronogram depicted in Figure 3.36 illustrates the hold and set-up times to be met for the register by using the preceding and the following signals of the RO's output phase $w_1(t)$ to sample the outputs of the delay chain: $w_0(t)$ and $w_2(t)$ respectively. The representation shows an ideal relation between the delay time to be implemented by the AND gates and the semiperiod of the oscillation frequency, for instance $t_{semip}=3t_{ANDd}$. The hold and set-up times are more relaxed when the clock input is driven by the previous output phase $w_0(t)$ instead the next one $w_2(t)$: equation (3.9) defines the times for w_0 by the rising edge marked in red, and equation (3.10) defines the times for w_2 by the rising edge marked in blue. The ideal expressions that determine the times are given bellow:

$$t_{\text{hold}} = t_{\text{ROpd}} + t_{\text{ANDd}} = 182 \text{ ps} \quad \text{and} \quad t_{\text{set}} = t_{\text{ANDd}} - t_{\text{ROpd}} = 83.8 \text{ ps}; \tag{3.9}$$

$$t_{\text{hold}} = t_{\text{ANDd}} - t_{\text{ROpd}} = 83.8 \text{ ps} \quad \text{and} \quad t_{\text{set}} = t_{\text{ROpd}} = 49 \text{ ps}; \tag{3.10}$$

where t_{ROpd} is the propagation delay of RO's inverters whose value is computed by equation 2.16. The flip-flop that samples the AND output does not demand tough performance requirements, more especially, if the previous output

phase is used as the clock input. However, whatever the signal is employed to register the chain word if any violation of those times is experienced, that causes metastability errors (it would result in the flip-flop switches late or does not switch at all), there is no time restriction to settle a stable output in this proposal. With sufficient time the output data will be established. Moreover, if the gate's delay time is shorter than the propagation delay of the RO's cells, $t_{ANDd} \leq t_{ROpd}$, with the preceding output phase as the clock signal of the registers the sampling of some data is ensured while using the following output phase all the chain outputs are cleaned before sampling. The D-type flip-flop design presented in [92], triggered by the preceding output phase, is implemented to evaluate the proposal.

For the resulting delay chain with 25 total elements and a delay time of 133 ps in each AND gate, the obtained thermometer words for every PVT operating points are reported in Table 3.2. The higher oscillation frequency the lower the amount of the chain outputs with '1'. A different thermometer code is obtained for every PVT condition, as expected.

TABLE 3.2: Chain output word for the resulting f_{osc} in every PVT condition with an input signal voltage of 250 mV and a fixed delay in each AND gate of 133 ps.

PVT	**f_{osc} [MHz]**	**estimated f_{osc} [MHz]**	**chain output word**
SS +120°C	153.2	156.6	"1111111111111111111111100"
SS 27°C	164.7	163.5	"1111111111111111111111000"
SS -45°C	178.2	179	"1111111111111111111100000"
SF 27°C	212.7	208.9	"1111111111111111100000000"
TT 27°C	226	221	"1111111111111111000000000"
FS 27°C	241.9	235	"1111111111111110000000000"
FF +120°C	280.6	268.5	"1111111111111000000000000"
FF 27°C	305.1	289.2	"1111111111100000000000000"
FF -45°C	351.3	341.8	"1111111111000000000000000"

It is important to note that the delay chain also suffers from PVT variations, and thus the delay time implemented is affected as well. Therefore, Table 3.2 does not characterize properly the performance of the circuit. The delay chain is assessed for every PVT condition in order to obtain the pertinent word. The chain outputs and the delay time are summarized in Table 3.3. The shortest delay times are achieved for FF process which corresponds to the fastest f_{osc}. Consequently, the amount of registered outputs with '1' is larger for these operating points, contrary to the performance observed in Table 3.2.

Notice that for the case of FF process with +120°C, the amount of cell delay required in the chain increases up to 27 to determine the corresponding oscillation

TABLE 3.3: Delay time of the designed AND gate in every PVT condition and the corresponding chain output word for the resulting f_{osc} with an input signal voltage of 250 mV.

PVT	f_{osc} [MHz]	estimated f_{osc} [MHz]	delay time [ps]	chain output word
SS +120°C	153.2	157.2	265	"11111111111000000000000000"
SS 27°C	164.7	165.8	335	"11111111000000000000000000"
SS -45°C	178.2	160.5	445	"11111000000000000000000000"
SF 27°C	212.7	213.4	213	"11111111111000000000000000"
TT 27°C	226	221	133	"11111111111111100000000000"
FS 27°C	241.9	241.4	109	"11111111111111111000000000"
FF +120°C	280.6	276.4	67	"11111111111111111111111110"
FF 27°C	305.1	303	66	"11111111111111111111111000"
FF -45°C	351.3	349.7	65	"11111111111111111111000000"

frequency, f_{osc}=280.6 MHz, with the obtained delay time in this particular operating point of 67 ps. By analyzing Table 3.3, the AND gate could be designed to implement a longer delay thus reducing the number of elements in the chain in order to optimize area. Using all devices hvt in Figure 3.38, the delay time values and the output word obtained are reported in Table 3.4.

TABLE 3.4: Delay time of a slower AND gate in every PVT condition and the corresponding chain output word for the resulting f_{osc} with an input signal voltage of 250 mV.

PVT	f_{osc} [MHz]	estimated f_{osc} [MHz]	delay time [ps]	chain output word
SS +120°C	153.2	150.6	415	"11111110000000000000000000"
SS 27°C	164.7	152.1	548	"11111000000000000000000000"
SS -45°C	178.2	158.2	790	"11100000000000000000000000"
SF 27°C	212.7	198.4	220	"11111111000000000000000000"
TT 27°C	226	227.3	200	"11111111110000000000000000"
FS 27°C	241.9	217.4	230	"11111111100000000000000000"
FF +120°C	280.6	280.1	86	"11111111111111111110000000"
FF 27°C	305.1	292.4	95	"11111111111111110000000000"
FF -45°C	351.3	357.1	100	"11111111111100000000000000"

Each delay unit has a load given by an AND gate and a flip-flop. To maintain the symmetry of the implemented time delay, a dummy NAND gate is connected to the last cell. The case of FF with +120°C is the condition that defines the total number of gates within the delay chain. The resulting chain is composed by 21 total identical delay units.

XOR gate decoding: control of the output offset tuning

For the described above, a different thermometer word is attained for the proposed circuit to estimate the semiperiod of f_{osc} corresponding to every PVT operation point. An XOR gate whose inputs are the last output of the chain with a logic value '1' and the next one will provide a signal in high when the circuit operates under certain PVT condition. For instance, the case of TT process with 27°C can be recognized by means of an XOR gate with the chain outputs ch<9> and <10> as inputs (see Table 3.4). The XOR gate output will be '0' either for higher or lower estimated f_{osc} and the inputs will be both '1' or '0' respectively. Applying this for all the cases of Table 3.4, every XOR output can be used to active a switch that controls the opamp's output offset (see Figure 3.35). The case of SS with -45°C, corresponding to the longest delay time, denotes the lower word to consider, so the outputs ch<0:1> can be ignored.

In the simulations shown in Figure 3.34, the input offset voltage must vary $\pm$125 mV for a proper calibration within all the possible states. For a real calibration circuit design intermediate values for $x_{off,N,2}$ must be ensured within that range. The higher the number of predefined offset values the higher the accuracy when linearizing the system, at the expense of higher complexity.

This way, the offset of the input signal $x_p(t)$ is adjusted according to the estimated operating point. Since the voltage drops on devices M_1 and M_2 remain constant, only by tuning $x_{off,N,2}$ the voltages $x_{p,N,1}$ and $x_{p,N,3}$ are shifted. For the sake of simplicity, the proposal has been limited only to the adjustment of $x_{off,N,2}$, but independently by modifying the current through the trimming circuit and hence the offset references $x_{off,N,1}$ and $x_{off,N,3}$, a more accurate approximation of the oscillator's voltage-to-frequency relation and better linearity performance might result. By means of programmable current sources in the front-end circuit different bias currents can be conveniently configured, as shown Figure 3.39.

3.3.4 Discussion and conclusions

3.3.4.1 Discussion

The proposal does not add extra relevant power consumption. The main contributor is the ring oscillator (1.5 mW per RO, in line with other previous publications). The power consumption of each opamp is 115 μW, and the branch needed to generate the offset references consumes 3.6 μW. As a consequence, the power consumption associated with the extra circuitry for linearization is less than 19% of the total required power, while, in [20], it is 60%. Although this power estimation will no doubt increase in an experimental prototype, it is expected that the power ratio between these elements remains. In relation to the area, it is not expected that our solution adds extra area growth in comparison to other digital calibration techniques. The disadvantage of the proposal remains on the

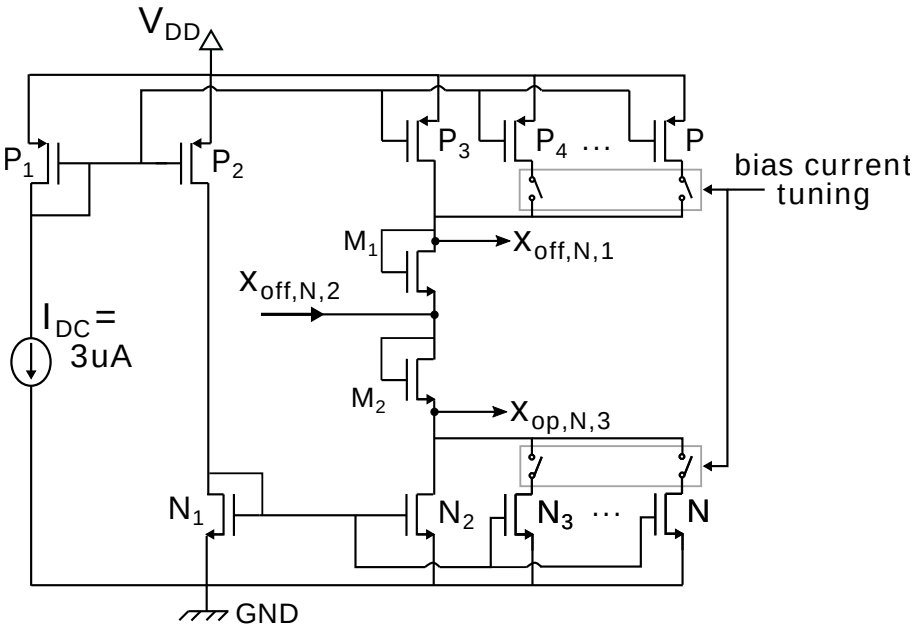


FIGURE 3.39: Front-end circuit with programmable current sources.

required calibration. The circuitry associated with this block has to be entirely implemented and evaluated to verify the proper function of the proposed scheme in Figure 3.35. Additionally, the time of periodic calibration, which depends on the variation of the RO's voltage-to-frequency response, needs to be defined for the operation of the whole system. Despite this, the calibration structure presents a simpler design and occupies less area than other reported calibration circuits.

The architecture in [20] introduces a VCO-based nonuniform sampling (NUS) ADC, which involves on-chip nonlinearity estimation and off-chip nonlinearity correction embedded within a nonuniform digital signal processing (DSP). The area of the set of structures dedicated to the calibration occupies almost the same of the ADC itself: 0.13 mm^2 and 0.14 mm^2, respectively. In [25], a reconfigurable CTSDM for analog-to-digital conversion is presented with an on-chip digital background calibration and self-canceling dither techniques. The calibration unit occupies 64% of the area of the whole chip and the voltage-to-current converter and the ring oscillator consume less than a fifth part of the total power dissipation [93]. Our solutions for nonlinearity mitigation does not involve background continuous intensive digital operations and are performed in the analog domain, reducing the required power consumption and also the occupied area.

The VCO-based open-loop configuration ADC in [28] presents a resistive network to tune the ring oscillator voltage-to-frequency function and reduce harmonic distortion. The principle of the resistive divider scheme is originally introduced in [27], and compromises ring oscillator's gain by attenuating the input amplitude. The second presented solution does not restrict the oscillator's

gain. In the case of the first proposed idea, the results in [27] show comparable performance for a lower input voltage swing with an area for an 18-tap RO of 0.0015 mm^2 and power consumption of 0.65 mW.

The structure explored in [6] contains a VCO as a quantizer within a $\Delta\Sigma$ loop. Nonlinearity is mitigated through a high-gain loop filter. The VCO-based quantizer only occupies 3.7% of the active area and consumes 13% of the total power, but it is hardly extended to low voltage supply environments. While enough voltage supply is granted to allow digital switching in the ring oscillator, the proposals can be implemented for lower voltage supply applications.

The possibility of going towards a fully-synthesizable architecture might be considered in the future, but it is currently out of the scope of this work, mainly due to the analog nature of the transconductors. All the digital parts can be implemented by using digital synthesis [35], [38], [39], [89], [94]–[97]. Tools for automated analog design are on-the-spot now and may become of application for the current architecture [98]–[101].

Table 3.5 summarizes the performance of the proposed designs and provides a comparison to prior works. Different VCO-based ADCs structures (a fully-synthesizable design [89] is also included), hybrid SAR-VCOs, and traditional Flash and SAR architectures are characterized as competitive alternatives. To achieve a fair comparison between the reference solutions and the proposed designs, area, power, and Figure-of-Merit (FoM) values only include the RO and the associated linearization blocks for the cases where data are available (*).

3.3.4.2 Conclusion

A circuit-level solution to linearize Ring Oscillators-based ADCs was proposed in this section of the chapter. The solution is based on making use of several transconductors connected in parallel with different bias conditions to implement a voltage-to-current function that approximates the inverse nonlinear current-to-frequency function of the ring oscillator. To evaluate the approach, a RO-based ADC with the proposed circuit was designed and simulated in 65-nm. Nonlinearity was strongly reduced resulting in an ENOB enhancement of more than three bits for a input swing of 800 mVpp in a pseudo-differential configuration. The proposed system delivers an SNDR of 63 dB over a signal bandwidth of 50 MHz, in line with other realizations. Additionally, mismatch effects, PVT variations, and noise impact was assessed. The proposal exhibited great robustness without resorting to a complex circuit design although a foreground calibration is required, with a simple and area-efficient structure in relation to the typical digital calibration procedures. The new RO-based ADC structure benefits from important power savings in comparison to state-of-the-art digital calibration circuits conventionally used to mitigate distortion. It is also expected to achieve area savings, but this needs to be confirmed through experimental prototypes.

TABLE 3.5: Comparison to state-of-the-art

Parameter	[6]	[10]	[13]	[20] *	[25]	[28] *	[35]	[41]	[84]	[89]	This work
Approach	VCO	VCO	SAR-VCO	VCO	ΔΣM	VCO	Flash	SAR	VCO	VCO	VCO
Meas./Sim. Results	MR	MR	SR	MR	MR	MR	MR	MR	SR	MR	SR
Voltage Supply [V]	1.2	0.9	1	1	1.2	0.2	1.2	1	1	0.6	1.2
Process [nm]	130	40	65	65	65	28	90	28	28	65	65
BW [MHz]	20	40	5	200	37.5	0.061	105	50	10	25.6	50
SNDR [dB]	67	59.5	75.7	57	70	68	35.89	67	62	50.3	63
THD [dBc]	-67.7	-65.7	-80.7	-63.6	-76	-72.5	–	-74.4	–	-53.9	-66.3
ENOB	10.84	9.59	12.3	9.18	11.34	11	5.67	10.85	10	8.06	10.17
Diff. Input Range [mV]	180	715	1800	566	800	355	280	2000	800	600 [a]	800
Power [mW]	40	2.57	0.51	35.4	39	0.0065	34.8	8	0.23	3.3 [b]	3.69
Area [mm^2]	0.42	0.017	–	0.156	0.11	0.07	0.18	0.1	–	0.026 [b]	–
FoM [dB] [1]	154	160.9	173.9	154.5	159.8	167.7	130.7	165	166.4	149.2	164.3
FoM [fJ/s] [2]	500	42	14.9	153	201.2	26	3256	43.2	14	235	32
Linearizat. technique	ΔΣ loop	2-step VCO-ADC	Dig. f-calib.	Dig. f-calib.	Dig. b-calib.	Resist. netw.	Inv.G. CDF	Dig. calib.	Bulk driv.	Dig. f-calib.	Multip. transc.

FoM [dB] [1] = SNDR + 10·log_{10}(BW/Power).
FoM [fF/conv-step] [2] = Power/(2·BW·$2^{(SNDR-1.76)/6.02}$).
[a] This input voltage swing is for a single-ended VCO-ADC architecture.
[b] These area and power consumption values are only for the ADC core, the digital correction block is not included.
Linearizat. = Linearization.
Inv.G. CDF = The inverse of Gaussian Cumulative Distribution Function (CDF).
2-step VCO = Two-step VCO-ADC.
Dig. f-calib./b-calib. = Digital foreground-calibration/background-calibration.
Resist. netw. = Resistive network.
Bulk-driv. = Bulk-driven.
Multip. transc. = Multiple transconductors.

Chapter 4

Resolution enhancement of RO-based ADCs for high-bandwidth applications

4.1 Introduction

In RO-based ADC architectures the effective oscillation frequency defines the quantization step of the conversion, as stated equation (2.21). Therefore, the minimum delay of the cells that compose the ring oscillator turns out to be a constraining factor, that limits the final resolution of the data converter. This is of special relevance if the voltage supply is decreased to reduce power consumption. Whereas oversampling allows us to get enough resolution for low-bandwidth architectures [23], this is not the case for high-bandwidth ones (dozens of MHz) in which the sampling frequency is restricted to some GHz in the fastest technology nodes. Looking at these applications, there are some alternatives to tackle this problem.

This chapter covers several solutions to deal with the restricted oscillation frequency in ROs, particularly suitable for high-bandwidth applications such as communication or IoT applications:

- Section 4.2: A way to artificially decrease the oscillation period in a RO-based ADC using phase interpolation. The interpolated phase between two consecutive output phases of a RO is computed with passive circuits. Then, that additional phase is injected into another RO. As a result, the total number of phases in a RO-based ADC is increased remaining the oscillation parameters of the ROs. Thus, the effective oscillation frequency is increased.

- Section 4.3: A new delay cell circuit for ROs that performs lower time delay than the conventional NOT gates. The design consists of using only two transistors between the supply nodes to merge the transconductance and the delay cell itself (see Figure 2.11). The approach allows the voltage supply to be reduced keeping the same oscillation frequency or increasing it by using the same supply voltage.

Section 4.4 draws the conclusion for the two proposals of the chapter which are both validated by simulations.

4.2 Passive Interpolation and Phase Injection

In this first part of the chapter, a simple way to improve the resolution of ADCs implemented with ring oscillators will be described. The proposal consist of inserting a passive resistive network into the differential delay cells of the ring oscillator to get additional interpolated phases. These interpolated phases are then injected to other similar ring oscillators. By increasing the number of phases coming from all the ring oscillators, the effective oscillation frequency of the system is higher and enhances the resolution of the converter. To validate the idea, a prototype of an open-loop RO-based ADC is built in VerilogA language with ROs designed with a 65-nm CMOS process. The results of transient simulations are compared to the results of a behavioral ideal model of the system built in MATLAB. As expected, the SNR is improved according to the increase in the number of phases. Finally, it is checked that the proposed circuit used to extract and inject the interpolated phases did not penalize the total power consumption.

This part is split up into two main sections. Section 4.2.1 describes how to undertake the problem mentioned above when the conventional open-loop configuration is used, and a new interpolated VCO-based architecture with no limitation in the number of phases is proposed. Section 4.2.2 validates the approach through behavioral simulations of the whole system and an implementation of the proposed technique in a 65-nm CMOS process.

4.2.1 Proposed circuit to increase the number of phases in a RO-based ADC with the same oscillation frequency

As mentioned in Chapter 3, one of the techniques employed to mitigate the nonlinearity effect of a RO-based ADC consists of introducing a low-amplitude input signal into the RO, making it works in a more linear range than when working in the whole range of oscillation [27]. Although this solution works nice for some applications, such as either audio or sensing [28], it strongly limits the RO's gain and restricts the resolution of the converter for high-bandwidth applications, where the front-end circuit must handle higher input amplitudes at the input signal. To overcome the lack of gain in these applications a novel, simple and passive way of increasing the number of phases of a ring oscillator but keeping the oscillation parameters is proposed. This solution does not depend on the time delayed by each tap in the ring oscillator, so it applies even when a ring oscillator with the fastest oscillation frequency possible is designed. Additionally, the resulting system keeps working in the same linear range of frequency, but with more phases.

A differential circuit for a multi-phase ring oscillator is shown in Figure 4.1. Each delay element consists of two main NOT gates and two cross-coupled auxiliary NOT gates. This differential configuration composed of four delay cells is widely used to design ROs with high common noise rejection ratio (CMRR) [27], [28]. This circuit structure will be taped to interpolate phases from a master RO and inject them into several slave ROs.

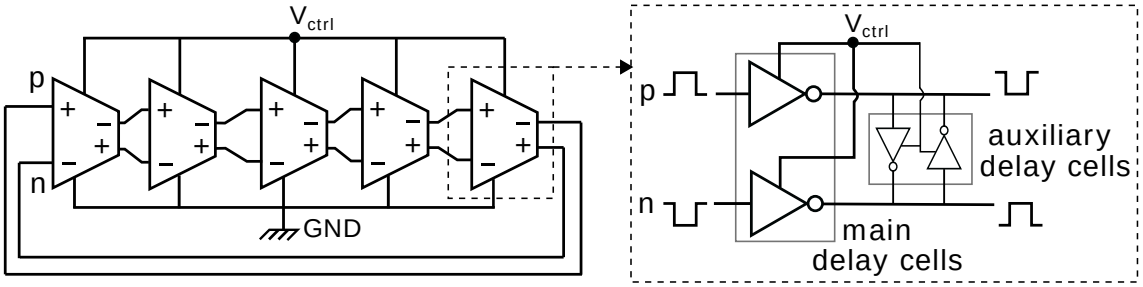


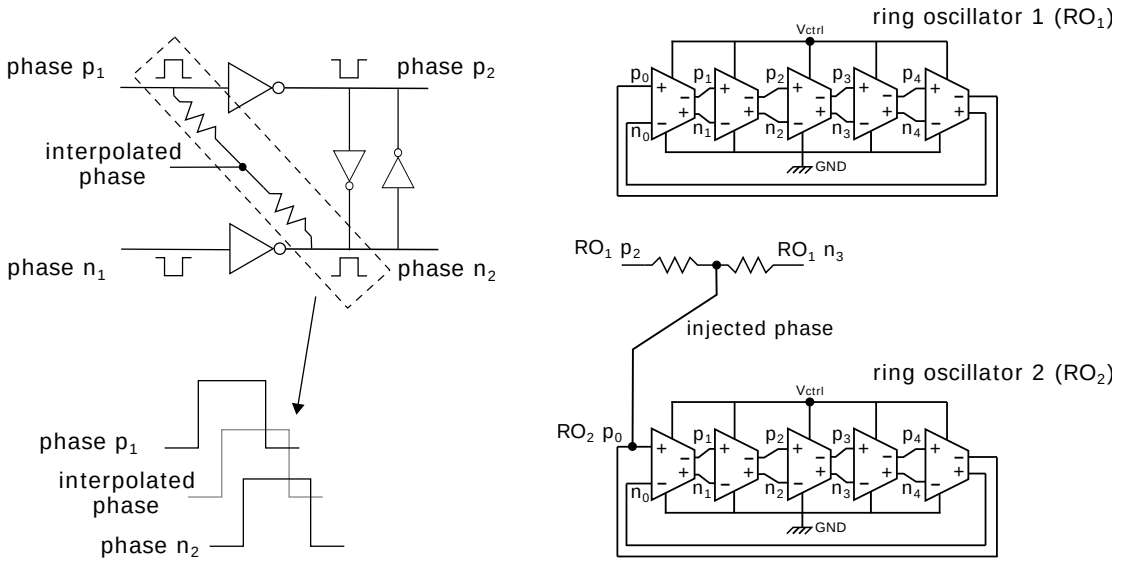
FIGURE 4.1: Differential delay cell for a ring oscillator.

To interpolate one phase a couple of resistors connected in series is placed between two consecutive opposite phases. Ideally, the higher the number of resistors connected in cascade, the higher the amount of interpolated phases. However, the number of interpolated phases is limited in practice. The proposed circuit for the case of two resistors is depicted in Figure 4.2(a). As can be observed, the new interpolated phase is in-between the two original phases. Then, this additional phase could be injected into another identical ring oscillator (with the same number of taps and the same delay cell circuit) to double the number of phases, as depicted in Figure 4.2(b), but guaranteeing the same oscillation parameters in both the master and the slave ROs. The slave ROs will take the interpolated phase as the phase reference and will generate additionally uniformly-distributed in-phase output phases. The unique condition here is to select a suitable value of the resistor network (low enough) for a proper injection of the phase.

This technique allows us to theoretically increase the number of phases and the amount of sampled edges in a certain period of time. According to [23], doubling the number of phases is equivalent to double the efficient oscillation frequency. In consequence, the SNR will be improved:

$$SNR_{\text{improvement}} = 6.02 \cdot \log_2\left(\frac{N'}{N}\right), \tag{4.1}$$

where N' is the new number of phases in the system, and N is the former number of phases.



(a) Resistive network for interpolation. (b) Phase injection connection.

FIGURE 4.2: Proposed interpolation and phase injection method.

Notice that this statement is only true if there is no overlapping between the phases. By selecting an adequate resistance value to obtain the edge of the interpolated phase exactly at the middle of the edges of the original phases and to inject it into other RO, a proper improvement at the final resolution will be ensured. The mismatch in the resistors of the passive network for interpolation might negatively impact on the uniform distribution of the edges of the output phases. The proper interpolation is defined by the resistors ratio, which is less prone to process variation. Once the resistance value is defined, no overlapped phases are produced by ensuring a resistor ratio equals 1, since the global variations is not critical. The mismatch between the ring oscillators should not be an issue because the injection forces the oscillators follows the frequency of the injected phase, nevertheless it is a factor to be evaluated in a final application. The differential configuration by means of using two resistive networks can be built as shown in Figure 4.3. This configuration also helps match the load in both branches of each tap and contribute to align the edges of both interpolated phases.

Keeping this configuration in mind, the proposal will be expanded to more than two resistors. In Figure 4.4 four resistors are placed in the resistive network to obtain three additional phases that can be used to inject three interpolated phases into three different slave ring-oscillators. In this case, as the number of phases is increased by four, so the expected improvement for the SNR equals 12 dB.

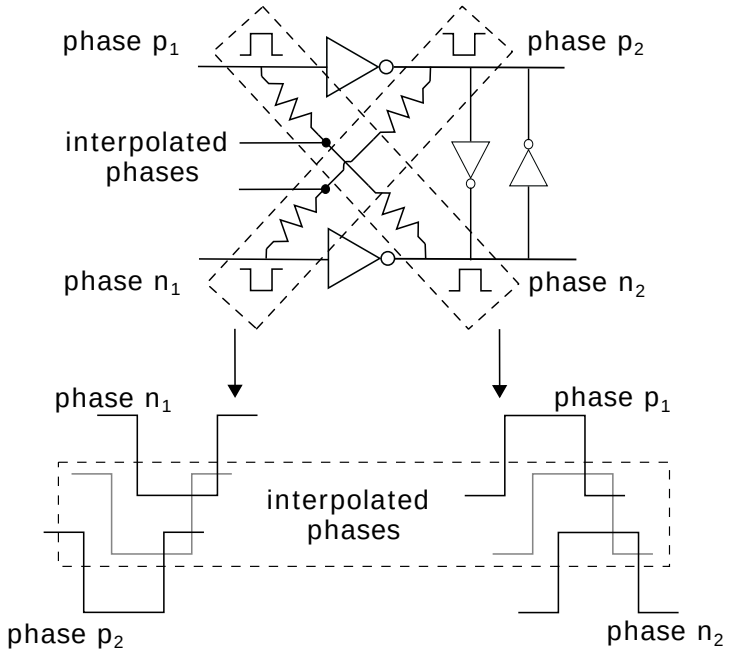
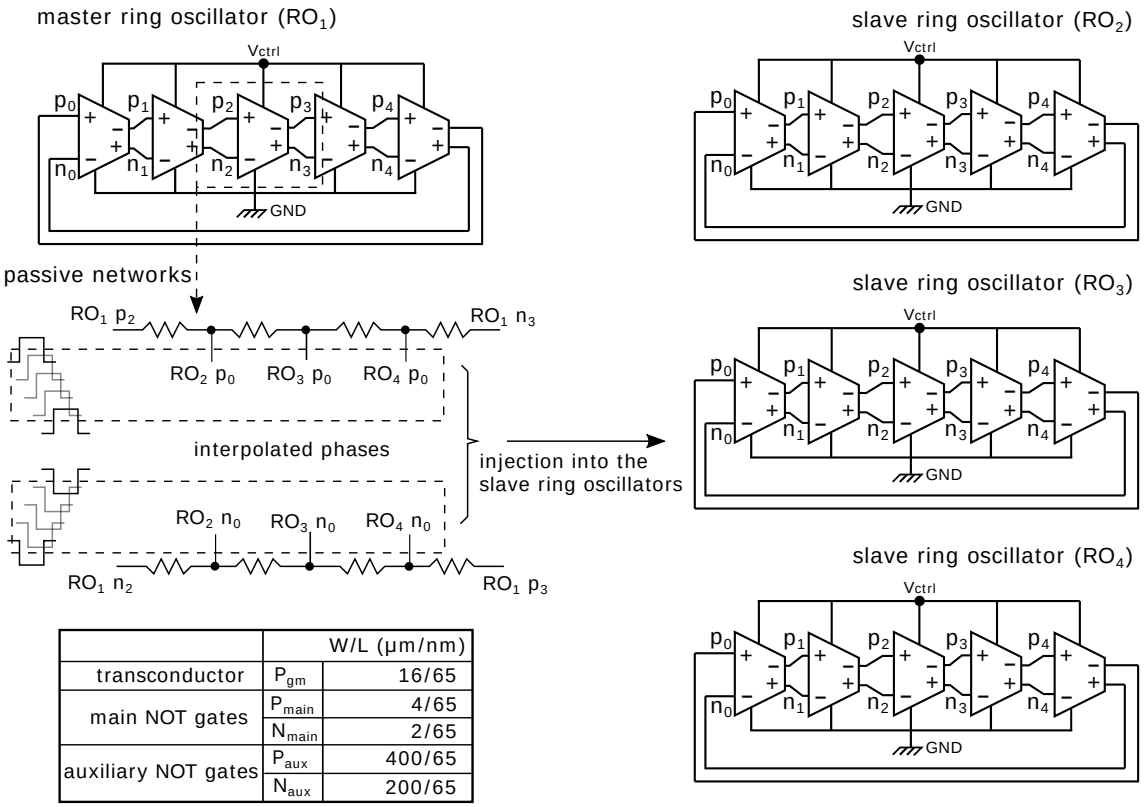


FIGURE 4.3: Dual resistive network connection in a differential cell for interpolation.

4.2.2 Practical implementation

To validate the correct performance of the proposed circuit, a pseudo-differential configuration with the architecture of Figure 2.9(c) is designed. A 9-stage differential RO is implemented in a 65-nm CMOS process, keeping the rest of the blocks modeled with VerilogA language including the resistances of the passive networks. Transient simulations are performed for three systems (see Figure 4.4): a system with a single 9-stage RO, a system with two 9-stage ROs (one master oscillator and one slave oscillator), and a third one with four 9-stage ROs (one master oscillator and three slave oscillators).

To observe the behavior of this technique, the simulation results from a behavioral ideal model in Simulink and processing of the outputs with a script in MATLAB, and the corresponding designs in 65-nm are compared. The interpolated phases of the systems with two and four ROs is shown in Figure 4.5. The resistance chosen for the resistive network equals 10 kΩ, which implies a very low current going through it. The even distribution of the output phases is clearly observable. Figure 4.6 depicts the output spectrum of the output digital signal for each of the simulated cases (2^{12} samples are used to calculate the spectra). The oscillation parameters are f_o = 540 MHz and K_{VCO} = 410 MHz, for a sinusoidal input signal of 200 mV_{pp} of amplitude (single-ended) at a frequency of 10 MHz. The nominal supply voltage is 1 V. The sampling frequency equals 2 GHz and the band of interest (BW) equals 50 MHz.



		W/L (µm/nm)
transconductor	P_{gm}	16/65
main NOT gates	P_{main}	4/65
	N_{main}	2/65
auxiliary NOT gates	P_{aux}	400/65
	N_{aux}	200/65

FIGURE 4.4: Proposed system with one master RO and three slave ROs, and the device's sizes.

The resulting SNR from an average of several input signal phases for the three systems are 57 dB, 62 dB and 68 dB respectively (HD3 term is -41 dBc). Regardless of RO nonlinearity effect that strongly degrades the resolution, the SNR is enhanced in steps of 5 dB and 6 dB (average values) when going from Figure 4.6(a) to Figure 4.6(b) and going from Figure 4.6(b) to Figure 4.6(c), as expected. The simulations computed with the ideal model in MATLAB provided values of SNR quite similar to obtained by transient simulations on the circuits: 56.3 dB, 61.8 dB, and 68 dB for cases (a), (b) and (c), respectively. With more data the average SNRs would be more accurate and better match with the theoretical SNR improvement of 6 dB. More simulations for a larger amount of input signal phases could not be carried out due to the long time required for transient simulations at 65-nm. Despite this, a proper resolution enhancement is obtained when making use of the proposed interpolation-injection technique. Considering the difference in the input capacitance of the NOT gates involved in the interpolation with respect to the others, any impairment is observed.

Additionally, looking at the spectra of Figure 4.6 it can be observed that the distortion power remains for the three cases as expected. This means that, for any application, the steps to apply this proposal are: firstly reducing the input signal

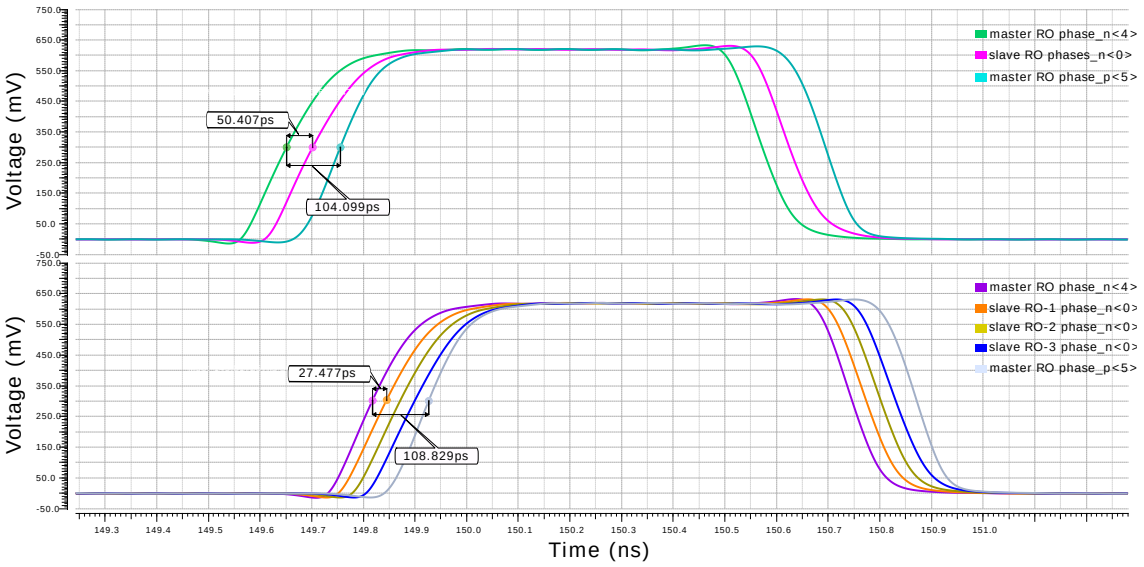
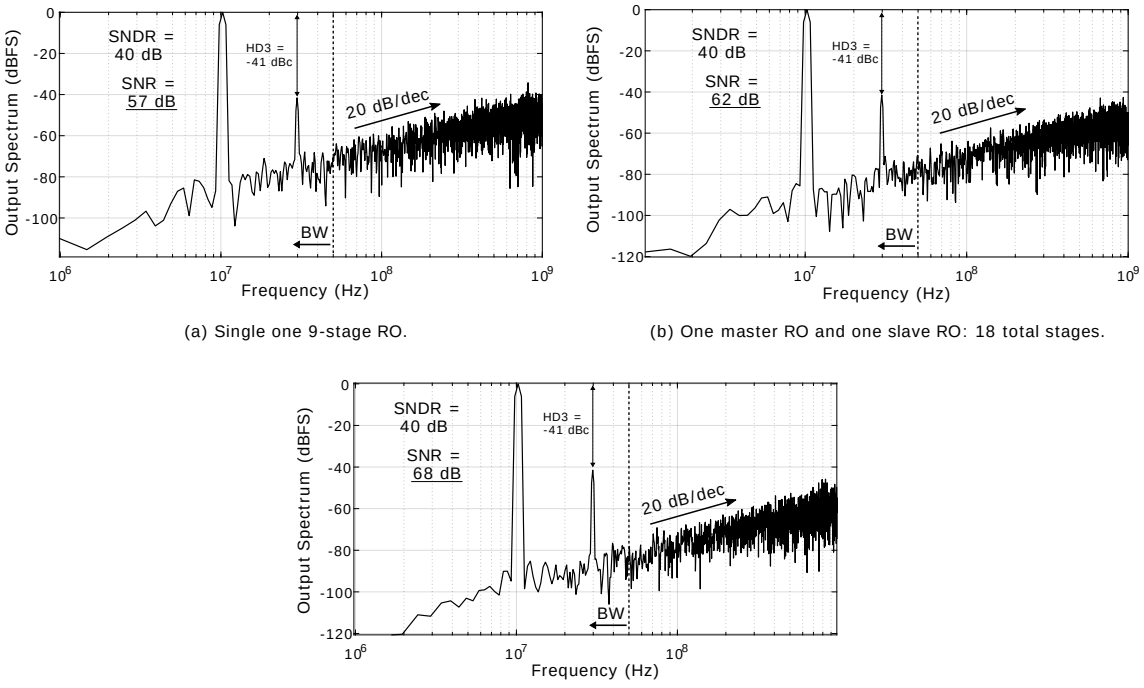


FIGURE 4.5: Output phases of the master RO and interpolated phases of the slave ROs in systems with two and four ROs.



(a) Single one 9-stage RO.

(b) One master RO and one slave RO: 18 total stages.

(c) One master RO and three slave ROs: 36 total stages.

FIGURE 4.6: Output spectra for the three systems.

amplitude until the distortion is not longer a restriction, and secondly increasing the number of phases to get a proper level of quantization noise. This feature

makes this solution especially suitable for high-bandwidth applications. In [31], a modified differential cell to boost the oscillation frequency of ring oscillators is proposed. The idea consists of using the auxiliary NOT gates to pre-charge the next cell outputs by changing the traditional cross-coupling into a feed-forward connection. This solution could be combined with the this work proposal to enhance further the final resolution of RO-based ADCs.

A case study of the power consumption is conducted for the ring oscillators designed in a 65-nm CMOS process. The power dissipation of the oscillators for the three systems shown in Figure 4.6 is calculated, the same value being obtained for all the oscillators, 133 μW. This means that the resistive passive networks used for the phase interpolation and injection does not suppose a power consumption penalty. Therefore, the total power will only depend on the number of ring oscillators added to the system.

Finally, with the goal of analyzing the impact of parasitic capacitances in the resistors, real devices are simulated in the passive interpolation network. Consequently, the oscillation parameters decreased a few MHz: f_o and K_{VCO} are 513 MHz and 405 MHz respectively. The previous values are 540 MHz and 410 MHz. The power consumption resulted unaffected and the decrease in the SNR is negligible.

The stochastic concept has been applied to RO-based ADCs, where multiple ADC channels in parallel are used to decrease the quantization noise of the system, similar to the proposal in this section. The idea consists of spatially averaging the noise contribution of each RO-based ADC. In this case, the quantization errors are uncorrelated sources and the resolution improvements is established by $10\log_{10}$channel, where channel corresponds to the number of RO-based ADCs used in the converter. In [32], the experimental results reveal 9 dB of improvement in SNR by employing eight conversion architectures based on oscillators. In our solution, the output phases in each RO are correlated in such a way the enhancement factor of the resolution is theoretically doubled comparing to stochastic RO-based ADCs. In a practical implementation, only by using four oscillators, the half of the channels used in [32], the SNR is increased 11 dB.

4.3 High-speed delay cell for RO-based ADCs

Highly dependence of the power consumption with respect to the voltage supply makes current finer CMOS technologies become supplied with voltages lower than 1 V. RO-based ADCs implemented scales properly with that requirement. However, conventional implementations of ROs limit the oscillation frequency due to the lack of available voltage to feed high currents. In this section, a novel circuit for a ring oscillator that overcomes this issue is proposed. A delay cell with only two devices between the supply nodes is built, in order to reduce the voltage supply for certain oscillation requirements. In addition, the lower number of devices connected to the output nodes supposes lower parasitic capacitance and

a reduction in the minimum achievable time delay, which increases the potential resolution. However, the power dissipation depends on the number of cells in the ring oscillator, unlike it occurs conventionally. Thus, the solution will be of interest when using a reduced number of cells in the RO in such a way that the computing load is moved from the RO to the digital logic afterwards, in theory highly scalable. The proposed circuit is theoretically described and validated by simulation in a 65-nm CMOS process. Comparisons to the conventional implementations are made, showing improvements in terms of resolution, power, and area.

The outline of this part of the chapter is as follows. Section 4.3.1 describes and compares the new delay cell to the conventional approach. The formulations that provide the operation conditions and an efficient way to compensate for the penalty in terms of power are defined for the new RO implementation in Section 4.3.2. Section 4.3.3 presents the practical validation of the approach in a 65-nm CMOS process with transient simulations.

4.3.1 Comparison to the classic CMOS-based NOT gate

In the most common circuit for a VCO (Figure 2.11), the higher I_{RO}, the lower the delay of the NOT gates and the higher the oscillation frequency. The lowest delay in the cells will define the highest time resolution of the converter. This becomes a limitation when oversampling ratio is low due to high bandwidths and restricted sampling frequency, such as in wireless or IoT applications. To overcome the resolution limitation, the delay cell of Figure 4.7 is proposed, with a minimum delay which is lower than the one achieved for the conventional delay cell.

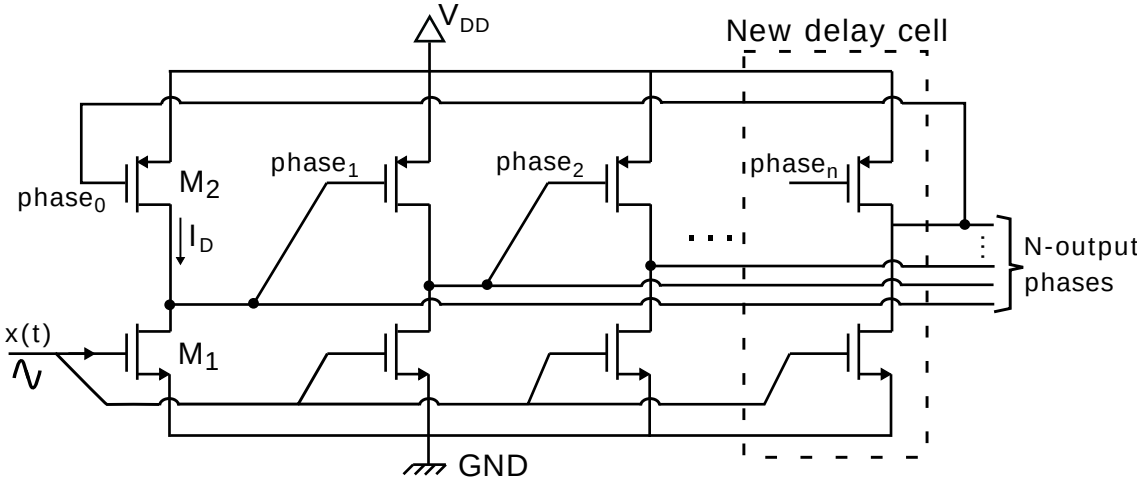


FIGURE 4.7: New high-speed delay cell for ring oscillators.

The new cell has the same structure of a common-source amplifier where the gate of the active load is connected to the output of the previous cell. M_1 makes

the voltage-to-current conversion and controls the oscillation frequency similarly to M_1 of Figure 2.11(a).

Whereas the conventional delay cell is composed of three devices as is shown in Figure 4.8(a), the NOT gate itself and the transconductor (M_1); in the new approach each cell is only composed of two devices depicted in Figure 4.8(b). Firstly, this alleviates the headroom voltage of M_1, allowing us to decrease the voltage supply V_{DD} for the same oscillation frequency. Secondly, the parasitic capacitance at the output nodes is reduced, which increases the highest possible oscillation frequency.

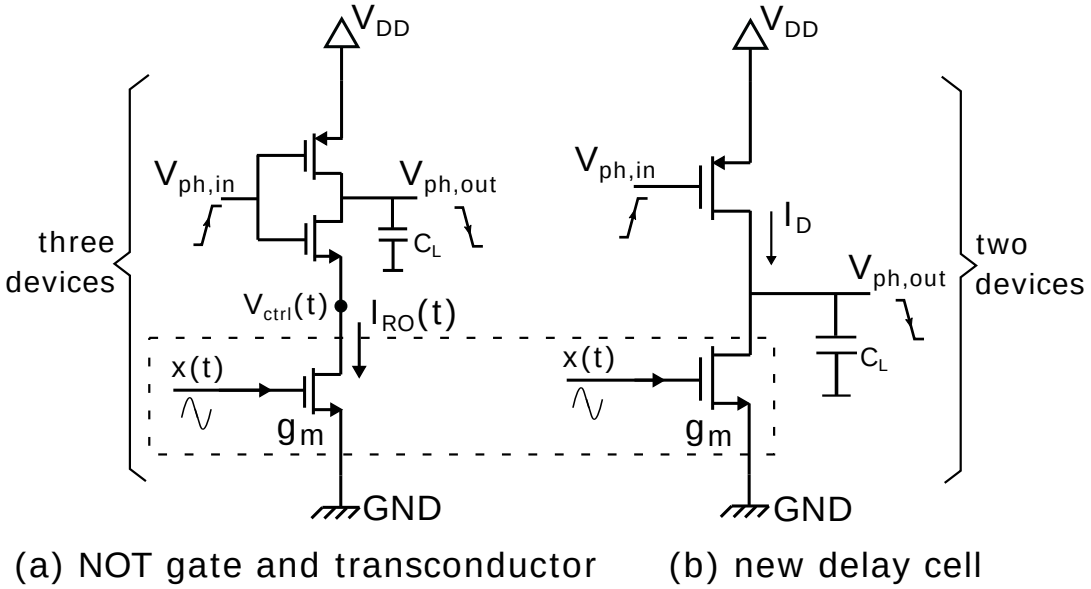


FIGURE 4.8: Conventional delay cell and the new one for a high-speed ring oscillators.

4.3.2 Delay cell's start-up conditions

If the sizes for both M_1 and M_2 devices are not correctly selected, there might be a solution for the operating region of both devices in which the input and the output of cell have the same voltage value, leading to a non-oscillating operating point. Looking at Figure 4.7 and considering three consecutive delay cells, a non-oscillating operating point will be achieved when the operating regions of M_1 and M_2 are reversed for each consecutive cell. The behavior of the cell proposed is depicted in Figure 4.9: according to the phase input voltage the operating region of each transistor is defined. The boundary between the non-oscillating operating point and the oscillating operating point occurs when M_1 and M_2 are in ohmic and saturation region, respectively, and interchanged for the next delay cell. This

condition will provide minimum sizes for M_1 and M_2. Going away from the calculated minimum sizes will make $phase_0$ become closer to V_{DD}, $phase_1$ become closer to GND, and $phase_2$ become closer to V_{DD}.

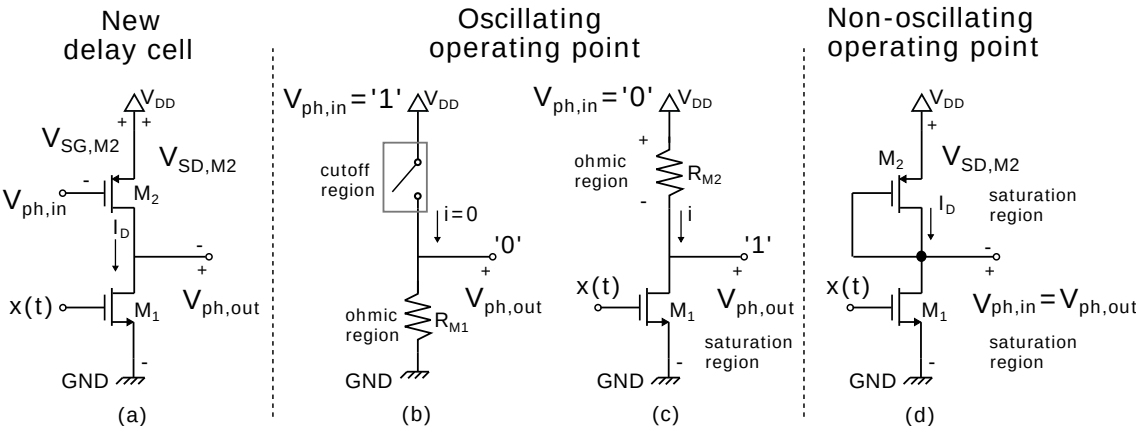


FIGURE 4.9: New delay cell circuit operation.

Below, the minimum size for both devices needed to make the structure oscillate will be calculated. Let's focus on the first cell of Figure 4.7 and suppose that M_1 is working in ohmic region and M_2 in saturation region (as illustrated in Figure 4.9(b) immediately before M_2 is off). With the assumption that capacitor C_L is charged, the currents that flow through M_1 and M_2 are equaled:

$$0.5K'_P\left(\frac{W}{L}\right)_{M2}\left(V_{DD}-V_{ph,0}-|V_{th,P}|\right)^2 = K'_N\left(\frac{W}{L}\right)_{M1}\left(x(t)-V_{th,N}-\frac{V_{ph,1}}{2}\right)V_{ph,1}, \tag{4.2}$$

where K'_P, K'_N is transconductance parameter, V_{th} is threshold voltage, and V_{ph} is the output phase voltage.

The same procedure for the next cell, but reversing the operating regions of M_1 and M_2, as depicted Figure 4.9(c):

$$K'_P\left(\frac{W}{L}\right)_{M2}\left(V_{DD}-V_{ph,1}-|V_{th,P}|-\frac{V_{DD}-V_{ph,2}}{2}\right)\cdot\left(V_{DD}-V_{ph,2}\right) = 0.5K'_N\left(\frac{W}{L}\right)_{M1}\left(x(t)-V_{th,N}\right)^2. \tag{4.3}$$

Taking both equations, 4.2 and 4.3, where $V_{ph,2}$ equals $V_{ph,0}$ and solving the resulting system of equations, an oscillating operation point will be achieved if both $V_{ph,0}$ and $V_{ph,1}$ are real and compatible with the initial operating points considered for M_1 and M_2 in two consecutive cells. The solution depends on the

value assigned to the input signal x(t), where the maximum value of x(t) defines the worst case possible to get oscillation. The minimum value determines the condition in which M_1 is not in cutoff operation region: x(t)$\geq V_{th,M1}$.

Considering the boundary between linear and saturation region for both M_1 and M_2 devices, the minimum size ratio required to make the structure oscillate is calculated as follows:

$$\frac{(W/L)_{M2}}{(W/L)_{M1}} \geq \frac{K'_N}{K'_P} \cdot \frac{(x(t) - V_{th,N})^2}{(V_{DD} - |V_{th,P}|)^2}. \tag{4.4}$$

For the sake of simplicity, the factor for the channel length modulation phenomenon is not considered in equations (4.2), (4.3) and (4.4). If assumed this, the minimum ratio defined in equation 4.4 would decrease, making it more suitable for newer processes. When the designed size ratio is lower than the value provided by equation (4.4) there will be no oscillation at the output phases.

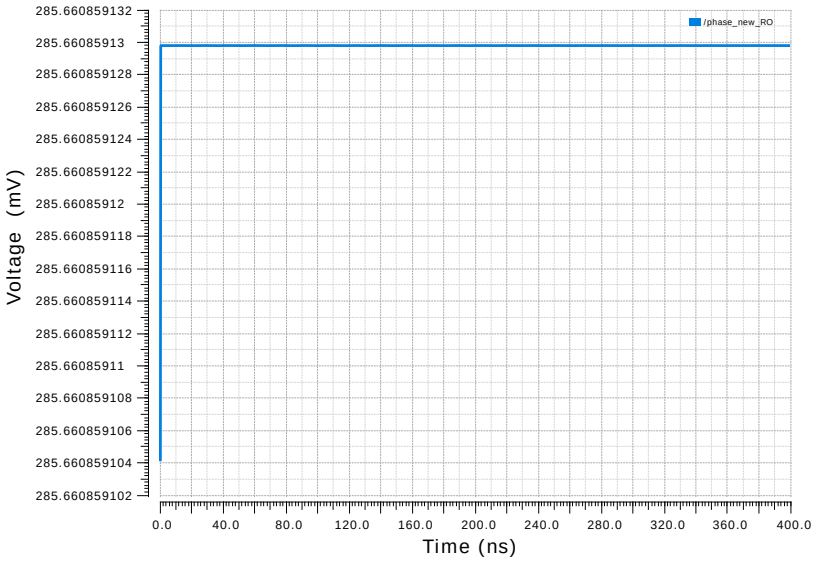


FIGURE 4.10: non-oscillating operating state in the proposed delay cell with inappropriate device' sizes.

To provide some intuition about the reference values for the minimum size ratio, the values for a 50-nm and a 1-μm CMOS technologies [51] have been taken. Whereas for the 50-nm process the minimum size equals approximately 1.5, for the 1-μm process equals approximately 3. This minimum size ratio value must be found out for each process, making use of it to reduce the occupied area and also speed up the oscillation frequency. Figure 4.10 shows the non-oscillating operating state of a new delay cell in 65-nm technology with devices equally sized, whereby the output phase takes an intermediate voltage level between GND and V_{DD}.

The minimum and maximum voltage for every output phase $V_{out,ph}$ are defined by the circuits in Figure 4.9(b) and (c), when the input phase voltage $V_{ph,in}$ is a high and a low state, respectively: the voltage across transistors in linear region limits the swing output, denoting a little amplitude modulation, as bellow:

$$V_{ph,out}(\max) = V_{DD} - V_{th,P}, \tag{4.5}$$

$$V_{ph,out}(\min) = V_{th,N}. \tag{4.6}$$

4.3.2.1 Energy-efficient delay cell configuration

It is important to note that the current I_{RO} in the conventional structure (Figure 2.11) flows only through those delay cells whose output signal is changing. This means that the power consumption of the structure does not depend on the number of delay cells but only on the oscillation frequency (equation 2.17). This is not the case of the new cell. The proposed design has the disadvantage of consuming static power when the input of the delay cell is at low state and M_2 is in the ohmic region. Including it into a ring oscillator configuration all the cells will spend half of the time at low state, and then an static current flows. Consequently, the higher the number of taps the higher the power consumption.

To reduce the power dissipation in the new proposal and get an energy-efficient architecture, the number of cells in the ring oscillator will be limited, keeping the same effective oscillation frequency according to equation (2.21), and moving the computing load from the analog side to the digital side, what requires a high-speed digital logic implementation. That is the reason why this proposal is specially suitable for newer narrow CMOS process, and portable between technology nodes.

4.3.2.2 Design extended to a differential configuration

The structure of the proposed cell can be applied to the design of a differential topology. Similar to the typical differential RO circuit with NOT gates wherein the output phases of two independent ROs are connected by means of auxiliary gates (as shown in Figure 4.1 in the first part of this chapter), in this proposal resistors can be used to plug the input of one cell into the output of another cell to obtain two complementary phases, as illustrated in Figure 4.11.

Matched resistors ensure the synchronism between phases signals of both interconnected ROs. The size value of the resistors must be carefully analyzed. Large resistors entail low cross currents, at the expense of higher white noise contribution related to the thermal noise of the resistors. Theres is a trade-off between good noise level and an acceptable power consumption. Therefore, the resistors value must be choose in order to offer a proper global performance.

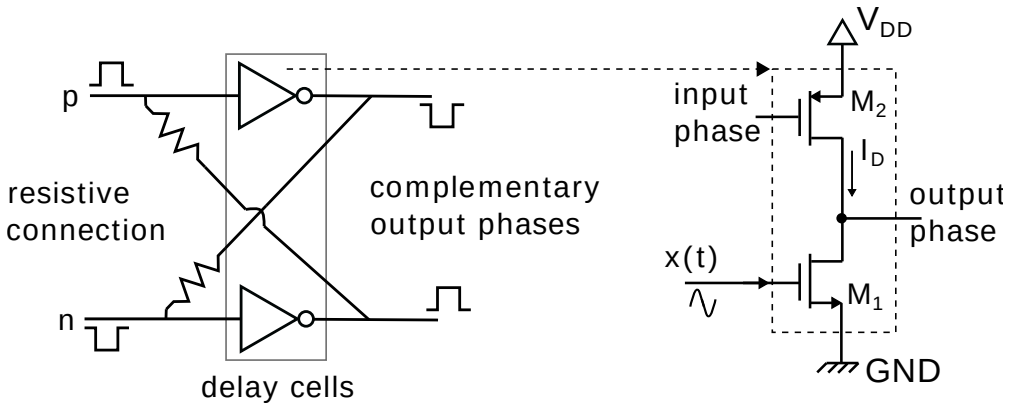


FIGURE 4.11: Proposed differential cell circuit.

4.3.3 Practical validation and simulations

As a first approximation, the single-ended topology of the proposed delay cell is evaluated in simulations and compared to the conventional one (Figure 4.8). Both RO structures are designed in a 65-nm CMOS process in order to validate the advantages of the new approach and verify its performance. Schematic level simulations are computed with nominal transistors to check the operating mode of the circuit. As a first set of simulations, the time delay for both cells are determined for certain supply voltage, to estimate how much faster the presented structure is. The propagation delays are 24 ps and 18 ps for the classic NOT gate driven by a CMOS-based transconductor and the new cell composed of two devices, respectively, with a supply voltage of 0.8 V. Thus, the new circuit allows the implementation of 25% faster ROs than those designed with the conventional circuit, using the same supply voltage.

The charts in Figure 4.12 exhibit the ROs performance and a comparison of the power consumption is carried out, for several voltage supply values, 0.8 V and 0.7 V, with input signal voltage of 200 mV_{pp}. Firstly, 3-, 5-, and 7-cell ROs are designed and simulated with the same voltage supply, which is 0.8 V. Here the delay for the conventional cell is minimized while not for the new one, what proves the possibility of reducing the minimum achievable time delay. The new ring oscillator (blue solid lines) consumes less than the conventional one (red solid lines) for the 3-cell implementation, as shows Figure 4.12(a), but not for the 5- and 7-cell ones plotted in Figure 4.12(b) and (c). In this particular case the new approach is more energy-efficient if less than 5 delay cells are used to built a ring oscillator. This limit could be enhanced if faster delay cells are used for the new RO and the voltage supply is reduced. It should be appreciated that, whereas the power consumption for the conventional RO (red solid lines) remains invariable, because only depends on the effective oscillation frequency regardless the number of cells, it is not the case for the new one. The power consumption in

the new RO depends on both terms, the effective oscillation frequency but also the number of cells that compose the ring oscillator. The most efficient solution is achieved when, for a given effective oscillation frequency, we design a ring oscillator with the lowest number of cells possible. Secondly, the voltage supply is set to 0.7 V for the new circuit, keeping the oscillation parameters of the previous analysis. In this case the new RO (blue dashed lines) consumes less than the conventional one for the 3- and 5-cell implementations, plots in Figure 4.12(a) and (b) respectively, but not 7-cell RO as shows Figure 4.12(c).

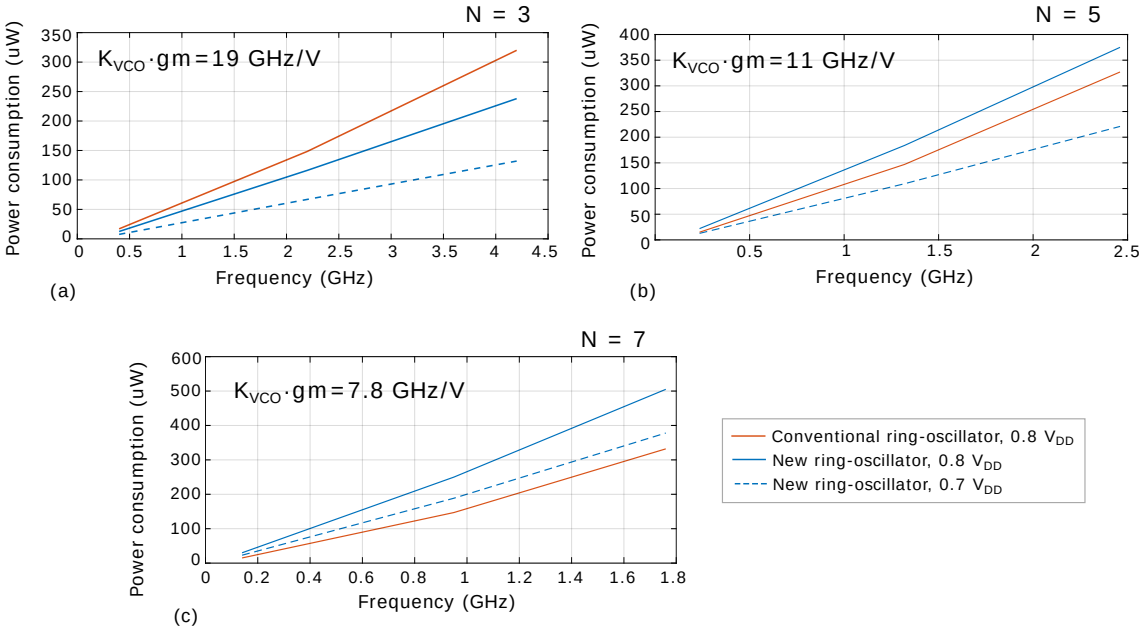


FIGURE 4.12: Power consumption comparison between conventional and high-speed cells: (a) 3-cell ROs, (b) 5-cell ROs, and (c) 7-cell ROs.

Finally, using a 3-cell implementation for both ring oscillators, the performance in terms of oscillation frequency is studied with a reduction of the voltage overhead. From earlier tests, it is concluded that the power consumption for the proposed RO with 3 stages is lower than the conventional one both for a voltage supply of 0.8 V and 0.7 V. This time, the voltage supply is decreased to 0.6 V and the oscillation frequency parameter. This reduction of the supply voltage supposed a RO gain degradation of 40% for the case of the typical structure whereas the performance of the proposed one is unaltered. The current are similar for both cases, 38 μA and 40 μA for the conventional and the proposed RO. By analyzing the oscillation frequency decrease for both configurations in these step-downs of the voltage overhead, the results conclude that the new delay cell circuit corresponds to an enhanced design regarding the oscillation frequency. This feature could be exploited for an application in which certain RO parameters, required

to achieve the final resolution of the data converter, are more relevant than the power consumption specification.

Regarding the linearity performance of the proposed RO circuit, the same nonlinear effects as the conventional RO structure discussed in Chapter 3 are exhibited: the nonlinear voltage-to-current conversion curve of a PMOS/NMOS-based transconductance, and the nonlinear dependence between the propagation delay of a transistor and the current flowing through it.

In [31] an alternative circuit to speed up the oscillation frequency of RO-based ADCs is published. The solution consists of modifying the connections of the cells that compose the ring oscillator. The circuit is based on the differential delay cell of Figure 4.1 to design a ring oscillator, using the auxiliary NOT gates to make feed-forward connections and couple the different phases in the same oscillator. Higher oscillation frequency is achieved because the output phase change of one single cell does not only depend on the immediate previous cells, but on several previous cells. Basically, that RO topology also suffers the same voltage overhead restriction as discussed before. The main advantage of the alternative presented in this section is the possibility of reducing the voltage supply resulting in a more scalable circuit in much finer processes, and additionally, with a more simple layout design compared to the intricate RO structure proposed in [31].

4.4 Conclusion

A simple passive circuit which allows us to increase the number of phases of a RO-based ADC without modifying the oscillation parameters was proposed in the first part of the chapter. The circuit is based on inserting a resistive passive network between two consecutive phases of a differential ring oscillator to get interpolated phases. These additional signals are injected into other similar ring oscillators to rise up the equivalent K_{VCO} and increase the final resolution of the converter. The proposed circuit was explained theoretically and validated through simulations of practical designs making use of a 65-nm CMOS process. The idea was tested with open-loop RO-based configurations, but it could be expanded to closed-loop configurations as well. The number of ring oscillators used in the architecture establishes a power consumption and occupied area increase, but the design optimizes the resolution enhancement compared to others solutions. Moreover, the input signal amplitude can be reduced in order to approximate the working region of the ring oscillators to a linear transfer curve, resulting in less harmonic components power, especially in open-loop RO-based ADCs. The resolution degradation due to the restricted RO gain will be compensated for by applying the proposed idea. The solution concept is very simple, power efficient, and digital friendly, only replicating the RO design as many times as required to achieve the desired accuracy.

In the second part, a novel delay cell for the implementation of RO-based ADCs was introduced. The proposed circuit is composed of one NMOS (as a

transconductance) and one PMOS, where the oscillation operating point depends on the size ratio between both devices. This particular configuration allows us to build ROs with a higher oscillation frequency, lower area, and, for an implementation with a few cells, lower power consumption in comparison to the conventional structure used for RO-based ADCs. The new circuit was theoretically characterized and validated by transient simulation in a 65-nm CMOS process, showing proper performance for very small voltage overhead. These features offer a very attractive solution for ADC architectures based on ROs in view of the development of deep-submicron CMOS processes. The new delay cell provides an alternative way to overcome the restricted resolution in A/D conversion architectures based on ring oscillators where the minimum delay defined the maximum achievable resolution.

Both proposals could be applied either open-loop or closed-loop RO-based ADC configurations. The results showed the correct performance of the presented ideas, being very suitable particularly for high-bandwidth applications, such as communication devices, implemented with new deep-submicron CMOS processes.

Chapter 5

Programmable digital pulse shaping filters for RO-based ADCs

5.1 Introduction

Going towards maximally digital radio receivers has become an imperative for highly integrated and limited power budget modern wireless communication systems [102]. Additionally as the amount of wireless communication standards increase, versatile and programmable multimode multiband receivers have received special attention. Analog receivers that include, low-noise amplifiers (LNA), variable-gain amplifiers (VGA) and low-pass filters (LPF) are hardly programmable and very sensitive to mismatch effects, and process, temperature and voltage variations (see Figure 5.1).

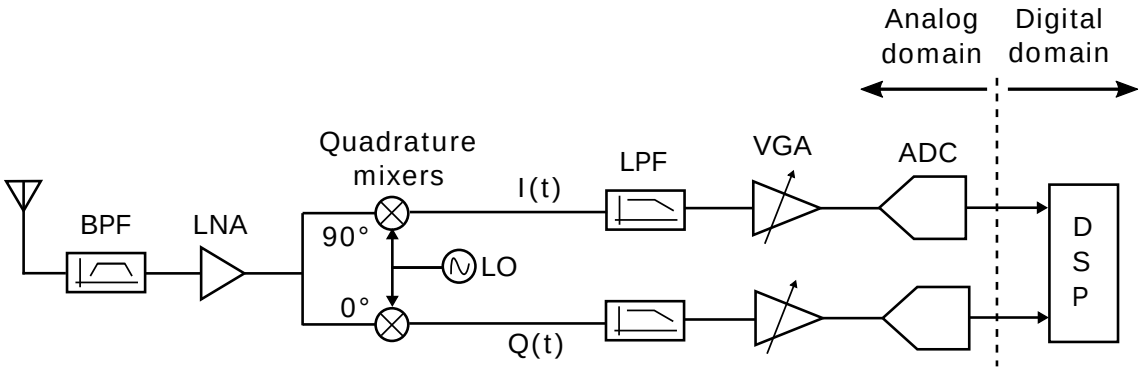


FIGURE 5.1: Generic receiver architecture.

Radio receivers with mostly digital circuits do not show these impairments, and enable the chance for cheaper structures because they can be designed with hardware modeling languages [30]. However, they require a high speed and high dynamic range ADC. As an intermediate solution, a time encoding-based receiver is proposed in [30]. Other similar approaches have been also published [33], [103], showing less power and especially much less occupied area due to the scalable nature of the solution.

In this chapter, two ways to introduce RO-based A/D conversion in radio receiver architectures are proposed. Both ideas consist of applying the PFM theory to customize the spectral properties of the A/D converter. The presented designs are oriented to highly digital implementation in radio receivers, exploiting the benefits of conversion architectures based on time encoding:

- Section 5.2: A new approach of RO-based ADCs performing a quadrature band-pass filtering. This solution allows expanding the range of applications of conversion structures with ring oscillators through digital logic.
- Section 5.3: A new low-pass RO-based ADC with the Nyquist Rate robust against interferences. The architecture shows a good performance in terms of power consumption compared to the conventional oversampled A/D conversion with oscillators and offers great solution for multi communication channels.

Although the architectures presented in the chapter are devoted for communication devices, the techniques proposed could be extended to other fields such as biomedical or audio applications. Both proposal are validated by simulations.

5.2 Quadrature band-pass VCO-based A/D conversion

Placing the ADC as close as possible to the antenna allows a much more efficient processing [29], [30] (see Figure 5.1), but needs a high-bandwidth ADC. The excellent input-referred noise and gain sensitivity of ring oscillators [3] greatly simplify the preceding preamplifier and signal conditioning stages. Until very recently, an important limitation of most practical designs is the restriction to first-order low-pass noise shaping. Today, some architectures implementing higher-order low-pass NTFs have been published [4], [74], [104], [105]. There also have been a few attempts toward band-pass architectures such as e.g. [29]. However, this structure is based on an N-path transformation which is well-known to lead to suboptimal performance. Another attempt is [106], but this work is based on an analogue feedback loop with multibit DACs, which partially hinders the advantages of the largely digital nature of RO-based ADCs.

In this first part of the chapter, a new approach that does not have these disadvantages and allows us a direct implementation of a RO-based ADC is presented, suitable for instance, for a radio receiver as shown in Figure 5.2, particularly devoted to intermediate frequencies (dozens or hundreds of MHz) [107]. The proposed approach is enabled by the new way to think about RO-based ADCs described in [23]. Here, the RO is not modelled as a phase integrator, but as a signal coder instead that represents the input signal with PFM, as addressed in Section 2.3.4. This alternative interpretation permits to devise new applications of RO-based ADCs. One of these new applications is the direct implementation of a

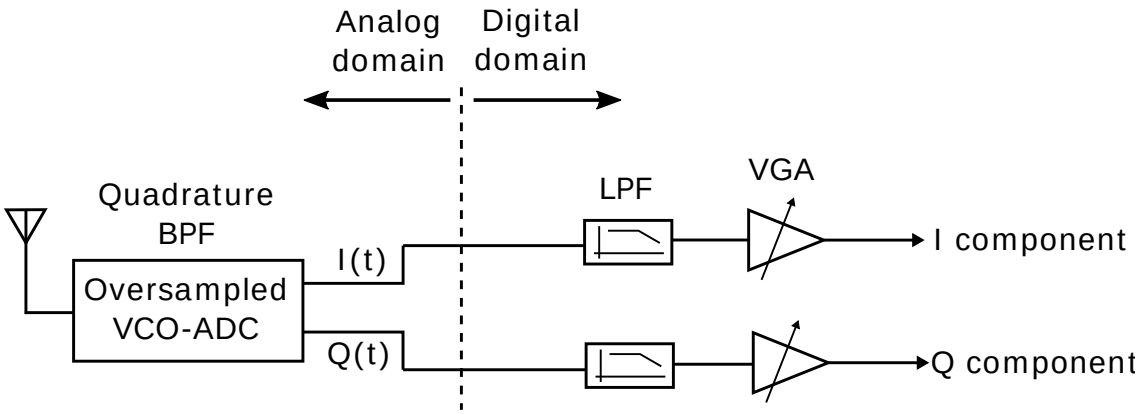


FIGURE 5.2: Diagram of the proposed radio receiver with RO-based ADCs.

quadrature band-pass NTF, which is the subject of this work. As will be clarified later, the NTF of the resulting modulator is not a regular band-pass, but instead a quadrature band-pass. Additionally, the structure is implemented with only one oscillator and the NTF is tuned digitally through lookup tables (LUTs). As a consequence of this, the same structure could be used for several applications just by changing the values stored in the LUTs.

This part of the chapter is structured as follows. Section 5.2.1 covers how to build the band-pass NTF with one single VCO in an open-loop structure. Section 5.2.2 shows a practical hardware implementation of the proposed architecture and the transient simulation results in Section 5.2.3. Additionally, power consumption estimations of the circuit proposal in 65-nm CMOS process is performed.

5.2.1 From the low-pass to the band-pass case

The presented band-pass ADC approach is derived from the formulations exhibited in the equivalence between PFM and RO in Section 2.3.4. The frequency response of $L(s)$ in equation (2.25) is shown in Figure 5.3 as L(f) in gray. This filter, L(f), has zeroes at multiples of the sampling frequency f_s, which leads to first-order low-pass spectral shaping of the aliased noise spectrum in the sampled output signal y[n]. To transform this structure toward band-pass spectral shaping, a frequency shift f_c is applied to the pulse shaping filter. Now, the zeroes of the pulse shaping filter will fall at the frequencies which would alias to f_c after sampling. Hence, the spectrum of the aliasing error will have a notch at f_c, which corresponds to quadrature band-pass spectral shaping. This idea is illustrated in Figure 5.3, which represents the shape of the frequency shifted filter B(f) (the dashed line).

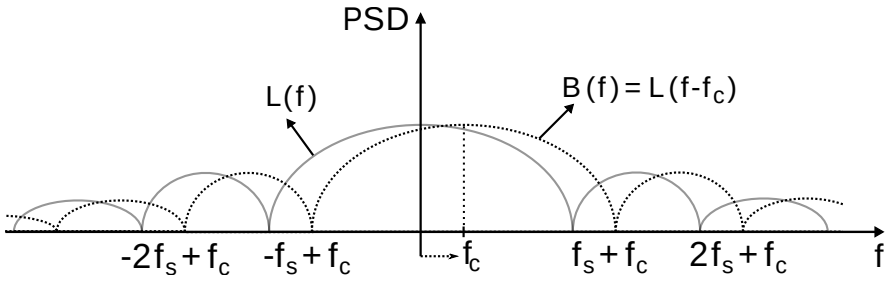


FIGURE 5.3: Using a *sinc* as the pulse shaping filter with a frequency shift f_c.

The time domain impulse response $b(t)$ of the new filter is written as:

$$b(t) = \mathfrak{F}^{-1}\left[L\left(f - f_c\right)\right] = e^{j\cdot 2\pi f_c t}\cdot l(t) = b_I(t) + j\cdot b_Q(t) = f_s\cdot\cos\left(2\pi f_c t\right)\left[u(t) - u(t-T_s)\right] + j\cdot f_s\cdot\sin\left(2\pi f_c t\right)\left[u(t) - u(t-T_s)\right]. \tag{5.1}$$

$\mathfrak{F}^{-1}$ represents the inverse Fourier transform, j the imaginary unit, and $u(t)$ the Heaviside step function, such that $l(t) = \frac{1}{T_s}\left[u(t) - u(t-T_s)\right]$ corresponds to the impulse response of the *sinc* filter of equation (2.25). As can be observed in equation (5.1), the new filter is a complex filter composed of a real (In phase) part $b_I(t)$ and an imaginary (Quadrature) part $b_Q(t)$. These filters must be applied to the pulse frequency modulated signal d(t) independently. Hence, the new RO-based ADC structure will look as in Figure 5.4. Here, there are two independent output data signals, $y_I[n]$ and $y_Q[n]$ from which the actual (complex) output signal y[n] follows:

$$y[n] = y_I[n] + j\cdot y_Q[n]. \tag{5.2}$$

The resulting structure implements a quadrature band-pass noise shaping architecture with a NTF having a notch at f_c and a unity gain STF at f_c.

Behavioural simulations is performed on the structure of Figure 5.4 to validate the correct operation of the proposed architecture. A typical simulated spectrum for the case of a center frequency f_c equal to $f_s/8$ is shown in Figure 5.5. Here, the RO model is an oscillator with 17 phases and $f_o = K_{VCO} \approx 0.4 f_s$. The pulse shaping filters of Figure 5.4 are applied to each of the phases. As explained in [23], a 17-phase RO is equivalent to a single-phase RO with a frequency that is 17 times higher. As a result, the fundamental encoding error due to unaliased modulation components that could stretch in the signal band (see Figure 2.14) is negligible and the performance is set by the spectrally shaped error. The OSR is set to 64 and the input signal is a -6 dBFS sine wave. The input frequency f_x is placed in the corresponding band-pass signal band at $f_x = f_c + BW/3$. As predicted by the theory, the plot exhibits a clear notch at f_c. The resulting SNDR equals 78 dB.

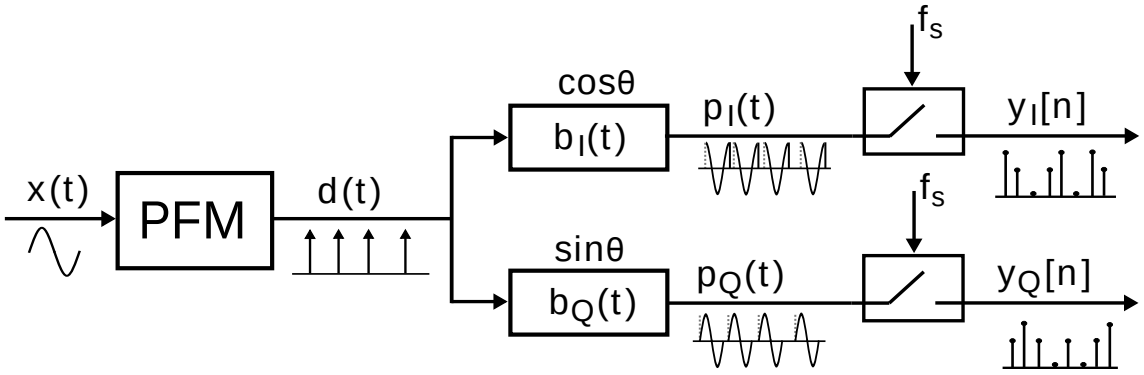


FIGURE 5.4: Band-pass PFM-based interpretation of RO-based ADCs.

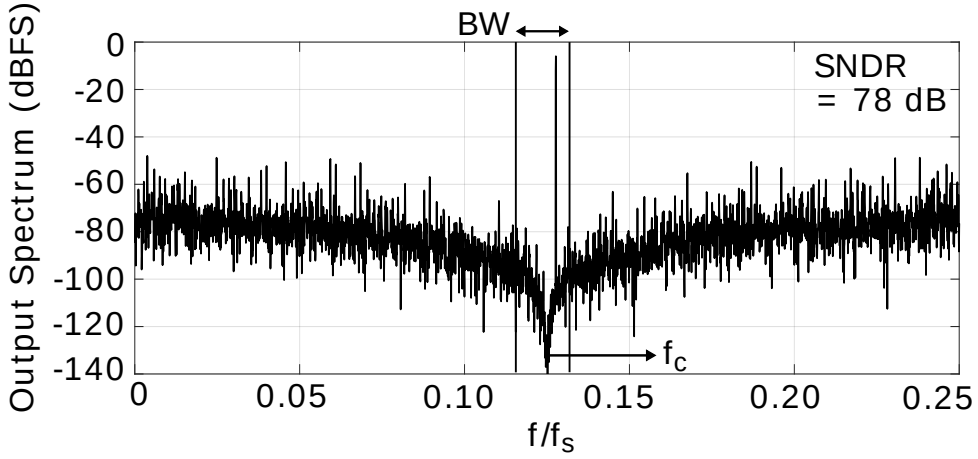
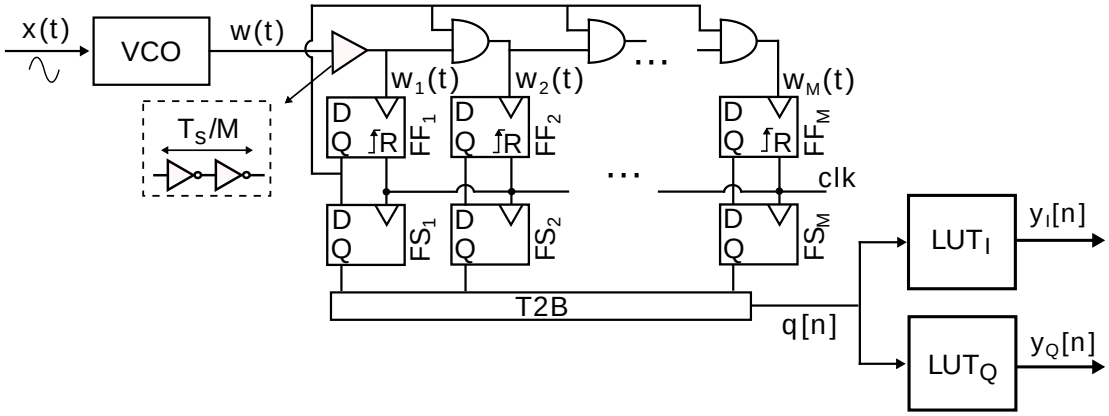


FIGURE 5.5: Behavioural simulation of the band-pass architecture of Figure 5.4. Sampling frequency normalized to 1 Hz, f_s=1.

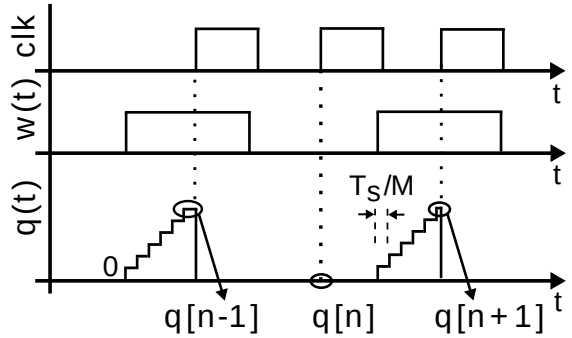
5.2.2 Practical implementation

Looking at Figure 5.4, it can be noticed that the output signals of the filters, $p_I(t)$ and $p_Q(t)$, take arbitrary real values at the sampling instants as stated equation (5.1), and hence do not immediately correspond to a digital representation. In contrast, p(t) in Figure 2.13 only has two possible levels in the conventional first-order low-pass case where a square pulse $l(t)$ is used as the pulse shaping filter, as stated equation (2.26). This ensures that y[n] is a binary sequence. If we now want Figure 5.4 to become an ADC, the output signal has to be quantized. In this architecture, the RO output phases will be quantized through digital delay lines working like a time-to-digital converter. Then, each digital value will be assigned to another digital value by lookup tables (LUTs) that contain an approximation of the time domain impulse response of equation (5.1).

The proposal consists of using the circuit depicted in Figure 5.6(a). Here, a digital delay line composed of M delay elements (AND gates and inverters) produces M delayed versions $w_i(t)$ of the oscillator signal w(t). The delay of each element is T_s/M. A rising edge in w(t) triggers consecutively flip-flops FF_1 to FF_M as the edge travels throughout the delay line. When a rising edge of the clock comes, the outputs of FF_1 to FF_M are sampled on flip-flops FS_1 to FS_M. The clock edge also resets flip-flops FF_1 to FF_M and clears the state of the delay line. After a thermometer-to-binary conversion, the outputs of FS_1 to FS_M represent a sample q[n] of a conceptual staircase signal q(t) synchronized with the oscillator. The values q[n] might be used as the index of a couple of lookup tables (LUTs) containing a discretized version of b(t), as illustrated Figure 5.6(b). Although Figure 5.6(a) describes a single-phase RO, extension to a multiphase case can be accomplished by replicating the circuit for all the RO phases and summing the intermediate digital output signals.



(a) Practical implementation.



(b) Chronogram.

FIGURE 5.6: Practical implementation of Figure 5.4.

The presented architecture is highly flexible and it is very easy to modify the modulator's center frequency in software. This can be understood from the observation that the center frequency depends only on the shape of the filter impulse response that is stored in the LUTs. Hence, several LUTs in parallel could be used

for different NTFs, or one single LUT could be tuned online to adapt the noise shaping performance. A final remark is that similar SNR performance can be obtained by using an equivalent low-pass RO-based ADC operated at a M times higher oversampling ratio. However, for the implementation of Figure 5.6(a), the complexity and speed requirements of the required decimation filtering is much lower.

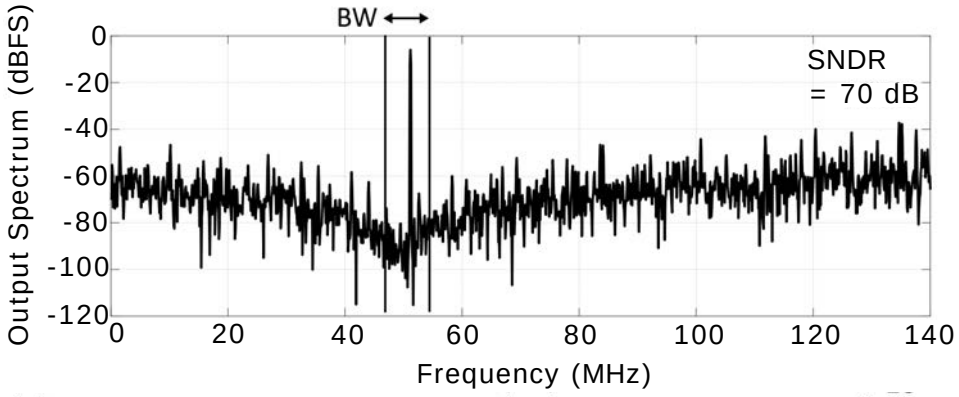
5.2.3 Simulations and circuit impairments

To validate the proper performance of the circuit of Figure 5.6, it is simulated using the same signal and oscillation parameters as for Figure 5.5 with f_s = 400 MHz. The result is depicted in Figure. 5.7. The delay line is composed of 70 delay elements for each of the RO phases. The quadrature band-pass NTF is still clearly visible in Figure 5.7(a) although the SNDR decreases somewhat due to the discretization of filter b(t). The higher the number of elements in the delay line, the better the approximation to b(t) and the higher the SNDR. In order to illustrate that the center frequency can easily be tuned by a software adaptation of the LUTs, the same simulation is performed, but now for the case where the LUTs are configured for a notch frequency f_c equal to $f_s/6$ = 67 MHz. The result is shown in Figure 5.7(b).

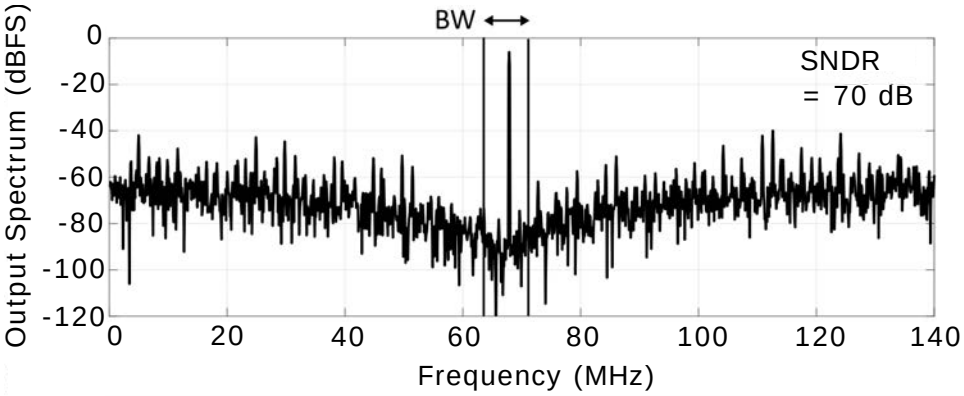
Again the notch is clearly visible. The SNDR equals 70 dB, the same value as in Figure 5.7(a). To get an estimation of the power consumption in a silicon implementation, a circuit design of the digital delay line and the sampling circuitry of Figure 5.6(a) is performed for a 65-nm CMOS process. These circuits are designed for a sampling frequency f_s of 400 MHz, corresponding to a total delay of 2.5 ns in the delay line. Making use of a supply voltage of 0.6 V to save power, the resulting power consumption per RO phase is of 37 μW in the delay line and 306 μW in the sampling circuitry. Hence, for our illustrative case of a 17-taps ring oscillator, the overall estimated power is equal to 5.8 mW. Due to the largely digital nature of the solution, the occupied area would be very low with a competitive power consumption. In addition, it can be observed that the delay line is the most power consuming element and it could be decreased if a more advanced CMOS process are used. The propagation delay of the digital delay line is highly sensitive to PVT variations. The total delay defines the notches of the pulse shaping filter. Thus, an error on the total delay will make the frequency notch position to be shifted. Figure 5.8(a) depicts the output spectrum when this total delay is increased by 10% uniformly for all the elements of the delay line. Note that the notch goes from f_c to f_c' according to the relation:

$$cos(2\pi f_c T_s) = cos(2\pi f_c' T_s'), \tag{5.3}$$

where T_s is the current total delay and f_c' the new position of the notch. For f_c = 50 MHz and an overall mismatch of 10%, f_c' equals 45.4 MHz, which is consistent with Figure 5.8(a). If we go one step further, the robustness of the circuit



(a) f_c = 50 MHz



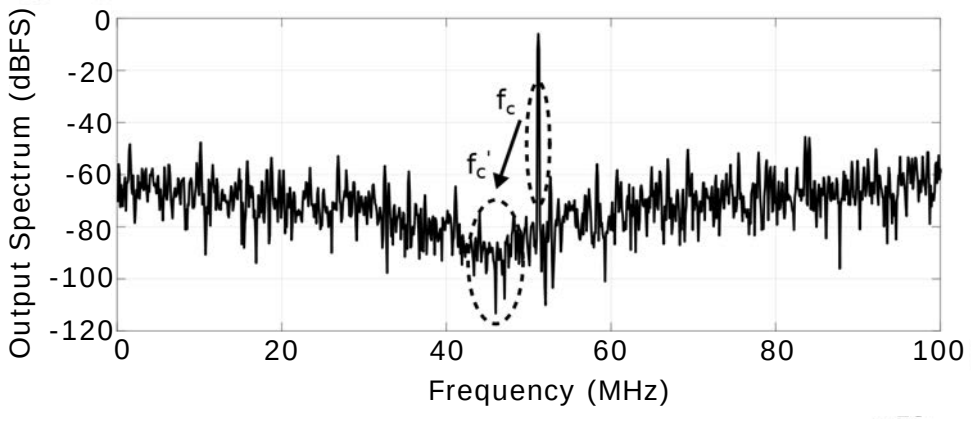
(b) f_c = 67 MHz.

FIGURE 5.7: Behavioral simulation of the proposed circuit of Figure 5.6(a) with: (a) f_c = 50 MHz, and (b) f_c = 67 MHz.

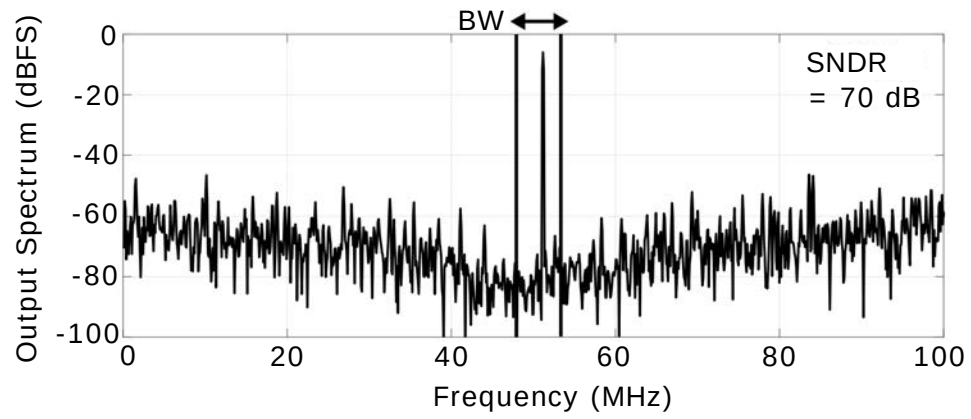
of Figure 5.6 can be tested against independent random variations of the digital delay line elements. With that purpose in mind, a simulation is performed randomizing the delay of the elements in the delay line following a gaussian distribution around the nominal value. The result is a SNDR degradation of only 3 dB for mismatches up to 30% of the nominal delay value, as depicted Figure 5.8(b). Therefore, the total delay is the meaningful parameter.

Finally, it is well-known that the performance of open-loop RO-based architectures is strongly degraded by oscillator nonlinearity. Nevertheless, several solutions have been already proposed in the literature to overcome this issue, such as digital calibration [20], [108] or circuit-level solutions [27], [69] like the structures described in Chapter 3 of this document.

In [29], a band-pass A/D converter using oscillators is proposed. The architecture consists of time-interleaving multiple first-order RO-based ADCs to perform a band-pass filtering. Each ADC channel operates at the same frequency (the sampling frequency divided by the number of channels) with different phases evenly



(a) Notch shifting due to slower delay line.



(b) 30% random mismatch.

FIGURE 5.8: Behavioral simulation of the proposed circuit of Figure 5.6(a) with slower delay line and variations of the digital delay line elements.

distributed and multiplexed back at f_s. The location of the nulls is f_s/channels, so the selection of the sampling frequency relies on the position of the interest band. In addition, the architecture uses S&H circuits at the input of the oscillators which require a highly linear function between the analog input signal and the sampled output to avoid degrading the ADC performance. A fourth-order ADC with the proposed architecture achieved an SNR of 68 dB over a bandwidth of 10 MHz, with a sampling frequency of 2 GHz (OSR = 100) and VCO tuning range from 100 MHz to 450 MHz. The final resolution of time-interleaved ADCs are very sensitive to mismatch. The system suffers an SNR degradation of 9 dB by introducing 1% mismatch between the tuning ranges of the VCOs. Moreover, the required sampling clock jitter is on the order of 0.1% for 62 dB of resolution. Another band-pass RO-based ADC is is introduced in [106]. The idea consists of a second-order CTΔΣM using RO-based integrators. The architecture involves

a feedback loop with two DACs as a generic second-order ΔΣM, and one more DAC in an additional branch. Although the implementation is free of transconductors or opamps, analog components are still present. The system achieved an SNR of 57 dB with $f_o = 2K_{VCO} = 15f_s$ and an OSR = 32. Table 5.1 compared and summarized the data reported above.

TABLE 5.1: Comparison to others band-pass architectures.

Parameter	[29]	[106]	This work
K_{VCO} [Hz/V] | f_o [Hz]	$0.09f_s$ | $0.138f_s$	$7.5f_s$ | $15f_s$	$0.4f_s$ | $0.4f_s$
f_s [GHz]	2	–	0.4
OSR	100	32	64
BW [MHz]	10	–	3.125
SNR	68	57	70

5.3 Nyquist VCO-based ADC with Programmable Pulse Shaping Filter for Mitigation of Blockers

RO-based ADCs are being progressively introduced in radio frequency applications. In [30] an architecture using ring oscillators is proposed where analog filtering is avoided and the ADC is performed after the down-conversion, as depicted in Figure 5.9.

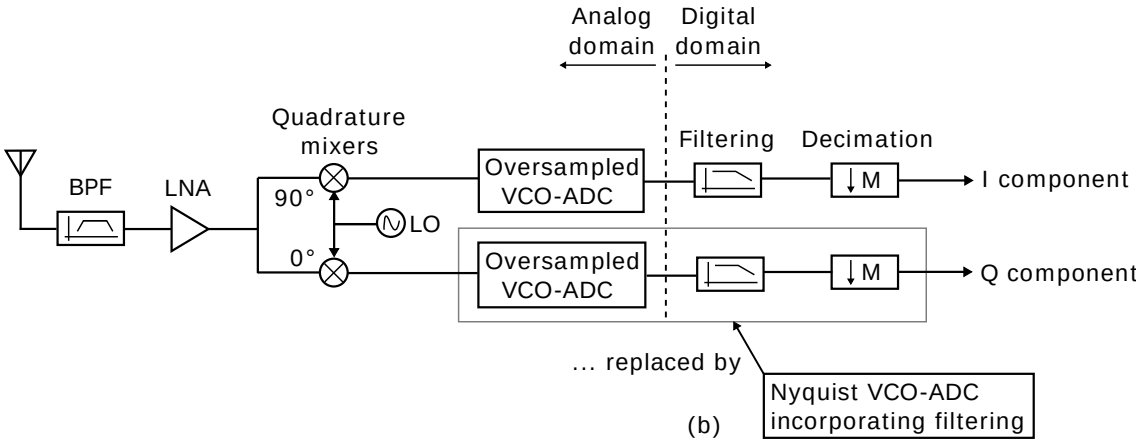


FIGURE 5.9: Radio receiver architecture with VCO-based ADC: (b) Proposal for robust-against-blockers VCO-based radio receiver structure

Another challenge for the design of such receivers is the continuously increasing number of adjacent communication channels in the radio spectrum. Therefore, the front-end ADC must deal with out-of-band power, which supposes, firstly, possible saturation of the ADC and, secondly, aliasing of the blockers within the band of interest. Continuous-time $\Sigma\Delta$ modulators are robust against this phenomenon due to their inherent anti-aliasing filtering and the possibility of designing appropriate signal-transfer-functions to remove blockers [109]. Nevertheless, analog integrators and quantizers are needed, so the digital nature we are seeking is partially hidden. In [103] a second-order *sinc* filter is placed in front of the ADC, zeroing the blockers at the multiples of the sampling frequency but allowing the pass of blockers at intermediate frequencies. These blockers could be removed afterward in the decimation stage at the expense of power-hungry and complex decimation filters.

In this part of the chapter, a Nyquist RO-based ADC for maximally digital radio receivers and blockers filtering is proposed, as illustrated Figure 5.9(b). The pulse shaping filter of the ADC is digitally programmable and can be tuned to null many different blockers at generic frequencies. The resolution and blocking capability performances will be similar to using an oversampled RO-based ADC with a digitally controlled decimation stage, but with much less power.

The outline is as follows. Section 5.3.1 describes the theory behind the proposed architecture. Section 5.3.2 shows a practical application in circuit. Power estimations and data-path analysis are made and compared to the conventional oversampled RO-based ADC.

5.3.1 Theoretical foundations

RO-based ADCs have been described in Section 2.3.4 as PFM with a pulse shaping filter (Figure 2.13) that defines the spectral properties and the nature of the output data y[n] [23]. The pulse shaping filter for the typical RO-based ADCs with an open-loop configuration (performed for the first-difference block) is a first-order *sinc* function, as depicted Figure 5.10(a), with nulls at the multiples of the sampling frequency f_s. Going towards more complex filters, as shown in Figure 5.10(b), supposes non-digital output data that requires digital approximation. Regardless of the complexity of such approximation, filters with customized spectral properties can be designed, for instance, to remove blockers.

Several *sinc* functions connected in cascade will generate a filter whose frequency response has nulls spread throughout the spectrum, not only at multiples of a frequency, but also at intermediate frequencies as depicted in Figure 5.10(c). This idea may be exploited for out-of-band blockers removal.

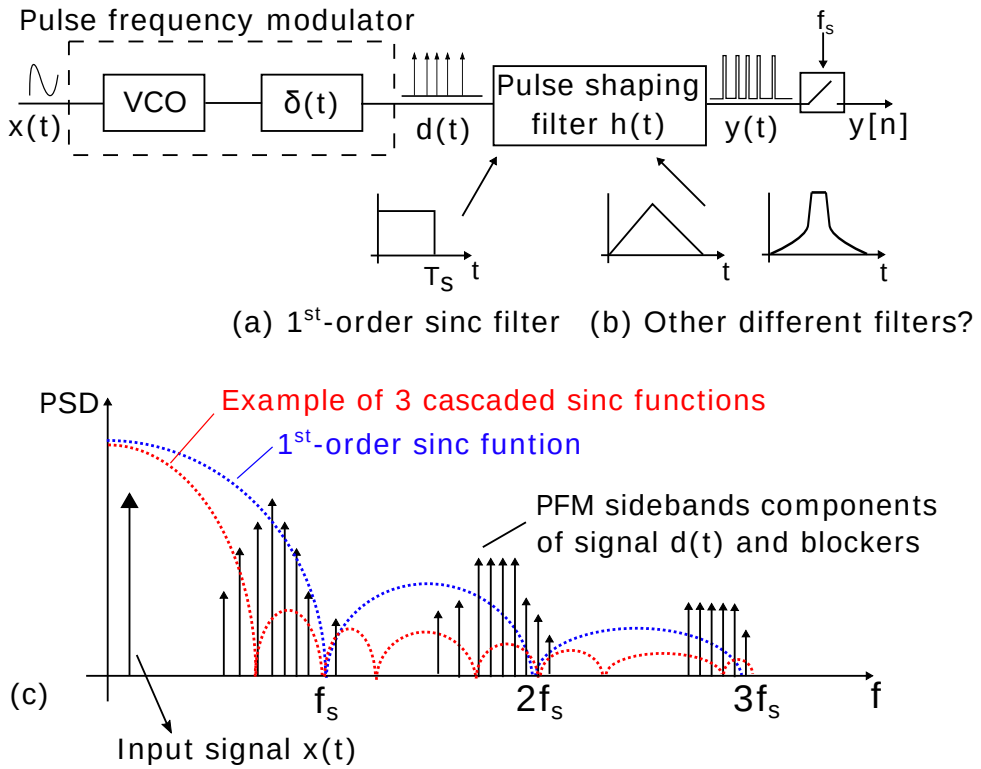


FIGURE 5.10: PFM representation of VCO-based ADC with different pulse shaping filters, (a) and (b); (c) spectral representation of d(t) and pulse shaping filters.

5.3.2 Practical application

5.3.2.1 Application example

As an application example, we are supposing that we have to deal with three out-of-band components at $f_1 = 60$ MHz, $f_2 = 70$ MHz and $f_3 = 90$ MHz (e.g. LTE-A standard [109]) for an application bandwidth of 60 MHz. The required pulse shaping filter h(t) to remove those blockers may result from the convolution of three square pulses (first-order *sinc* functions) of width $T_1 = 1/f_1$, $T_2 = 1/f_2$, and $T_3 = 1/f_3$, respectively. The equations that describe the proposed filter h(t) is a piecewise function defined in nine different intervals, according to equation (5.4). The detailed procedure of the convolution operation to obtain the behavior of the proposed filter is in Appendix B.1.

The time impulse response of the new pulse shaping filter is depicted in Figure 5.11. Note the analog nature of the pulse shaping filter, which means that a digital approximation is needed for full analog-to-digital conversion.

$$h(t) = \begin{cases} 0 & t \leq 0 \\ \frac{t^2}{2} & 0 < t \leq T_3 \\ T_3 \cdot t - \frac{T_3^2}{2} & T_3 < t \leq T_2 \\ -\frac{t^2}{2} + (T_2 + T_3) \cdot t - \left(\frac{T_2^2}{2} + \frac{T_3^2}{2}\right) & T_2 < t \leq T_1 \\ -t^2 + (T_1 + T_2 + T_3) \cdot t - \left(\frac{T_1^2}{2} + \frac{T_2^2}{2} + \frac{T_3^2}{2}\right) & T_1 < t \leq T_2 + T_3 \\ -\frac{t^2}{2} + T_1 \cdot t + \left(T_2 \cdot T_3 - \frac{T_1^2}{2}\right) & T_2 + T_3 < t \leq T_1 + T_3 \\ -T_3 \cdot t + T_3 \cdot \left(T_1 + T_2 + \frac{T_3}{2}\right) & T_1 + T_3 < t \leq T_1 + T_2 \\ \frac{t^2}{2} - (T_1 + T_2 + T_3) \cdot t + \left(\frac{T_1}{2} + \frac{T_2}{2} + \frac{T_3}{2}\right) + (T_1 \cdot T_3 + T_2 \cdot T_3) & T_1 + T_2 < t \leq T_1 + T_2 + T_3 \\ 0 & t > T_1 + T_2 + T_3 \end{cases} \tag{5.4}$$

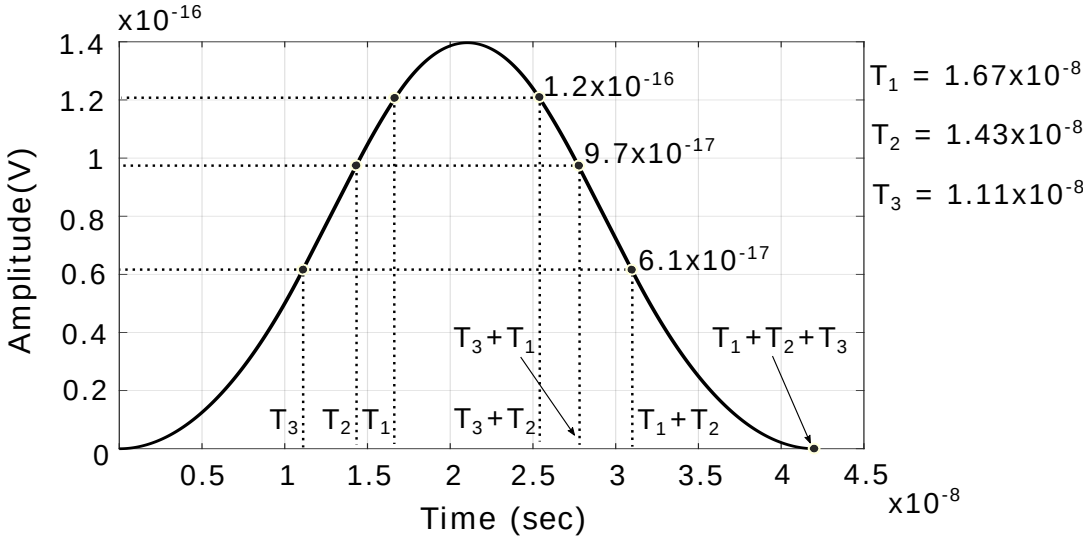


FIGURE 5.11: Time impulse response of the pulse shaping filter designed to remove blockers at 60, 70, and 90 MHz.

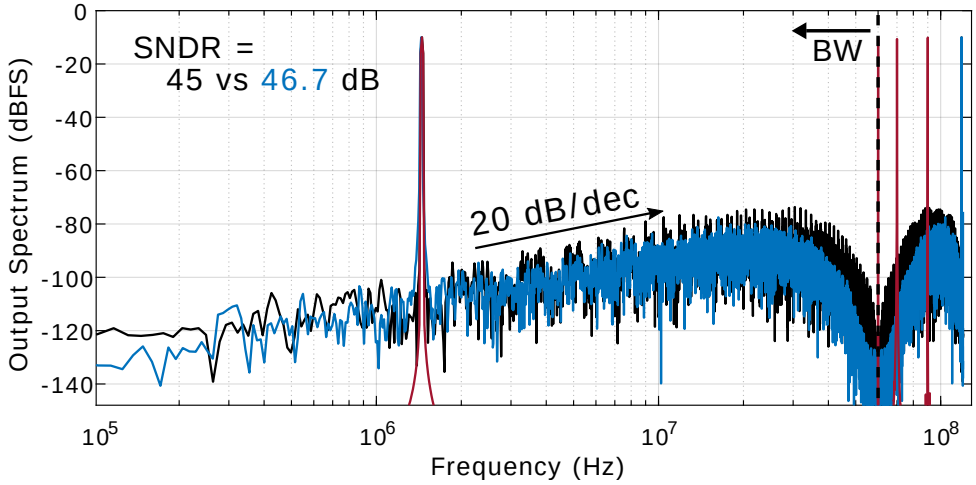
The spectral representation of this pulse shaping filter looks like the red example in Figure 5.10(c), as will be seen later on. Great attenuation of high-frequency modulation components is expected before sampling, enabling the chance to use a Nyquist RO-based structure in an attempt to save power, instead of an oversampled structure with subsequent decimation stage.

Behavioral simulations is performed to validate the correct operation of the proposed structure, and compare it with the equivalent oversampled RO-based ADC scheme of Figure 5.9. A 45-tap RO is used with a rest oscillation frequency of f_o = 18 MHz and a gain of K_{VCO}=15 MHz/V. The pulse shaping filter of Figure 5.11 is connected to all output phases of the oscillator. For the oversampled case, the first-order *sinc* function is used as a pulse shaping filter (as typically done). A decimation stage is connected after sampling. A low-pass direct-form Finite Impulse Response (FIR) filter is designed with a windowing method using a Blackman window with a sampling frequency f_s=6 GHz and a decimation factor of M=50. The digital filter had 602 coefficients allocating nulls at 60, 70 and 90 MHz. Figure 5.12(a) shows the result of simulating both systems (the output of the Nyquist-based one is still analog) for an in-band sinusoidal input signal and the three blockers. All these signals are of 300 mV_p of amplitude under a full-scale value of 1 V_p. For both cases, the blockers are completely filtered and the achieved SNDRs are approximately similar. The plots in Figure 5.12(b) correspond to the frequency response in magnitude of the new pulse shaping filter for the Nyquist structure and the FIR filter for the oversampled one.

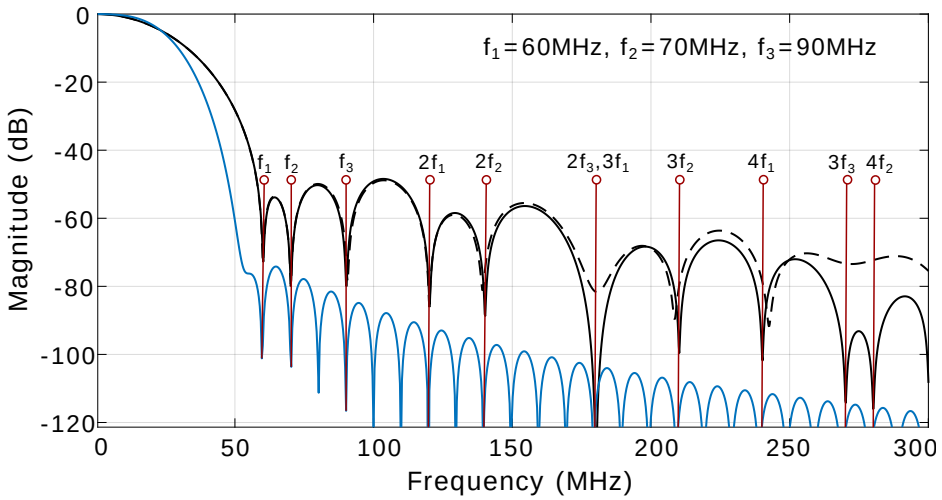
5.3.2.2 Circuit approach

For full analog-to-digital conversion, the output of the Nyquist system must be quantized, for instance, by approximating the function of the filter in Figure 5.11 to a staircase waveform. In Figure 5.10, the output of the VCO is a train of impulses d(t) that passes through a pulse shaping filter and generates the final output signal y(t). One impulse will generate one analog pulse with the shape shown in Figure 5.11 and will be sampled. By estimating the time between the impulses (that match with either the rising or the falling edges of the VCO phases) and the sampling instants, a digital value could be assigned to the output, corresponding to an approximation of the real analog output value.

With that purpose in mind, the circuit of Figure 5.13 is proposed. An external square waveform with a well-defined frequency is connected to a digital counter, which increases its count value when a rising edge occurs. The period of the external square waveform is used as the quantization step to discretize time. Sampling the output count value at both the VCO output phase and the rising edges of the clock signal, and making a subtraction will result in a quantized value of the time spent between both events. This digital value will be used as the index input value of a data pre-loaded lookup table (LUT) that assigns a final digital value to the output data according to the time-domain impulse response of Figure 5.11. This assignation operation applies to all the VCO phases. The higher



(a) Spectra of the in-band input signal and out-of-band blockers (red), Nyquist system output data (black), and oversampled system output data (blue)



(b) Frequency response in magnitude of the ideal proposed pulse shaping filter (black), the approximated one (dashed line), and the FIR filter (blue).

FIGURE 5.12: Output spectra of both data converters and frequency response in magnitude of the filters.

the frequency of the external square wave, the more accurate the approximation, plotted in Figure 5.12(b) with a dashed line, and the closer the final resolution to the theoretical one, the black spectrum depicted in Figure 5.12(a).

To illustrate the idea, the chronogram of Figure 5.14 describes the operation of the circuit in Figure 5.13. The count value c(t) is registered with the rising edges from the RO output phase w(t), and then resampled to be synchronized with the clock signal. Thus, the starting point for the pulse shaping filter h(t) is defined (the red lines). This value and every count value sampled after that (the gray lines) are subtracted to obtain a difference in quantization steps. The resulting

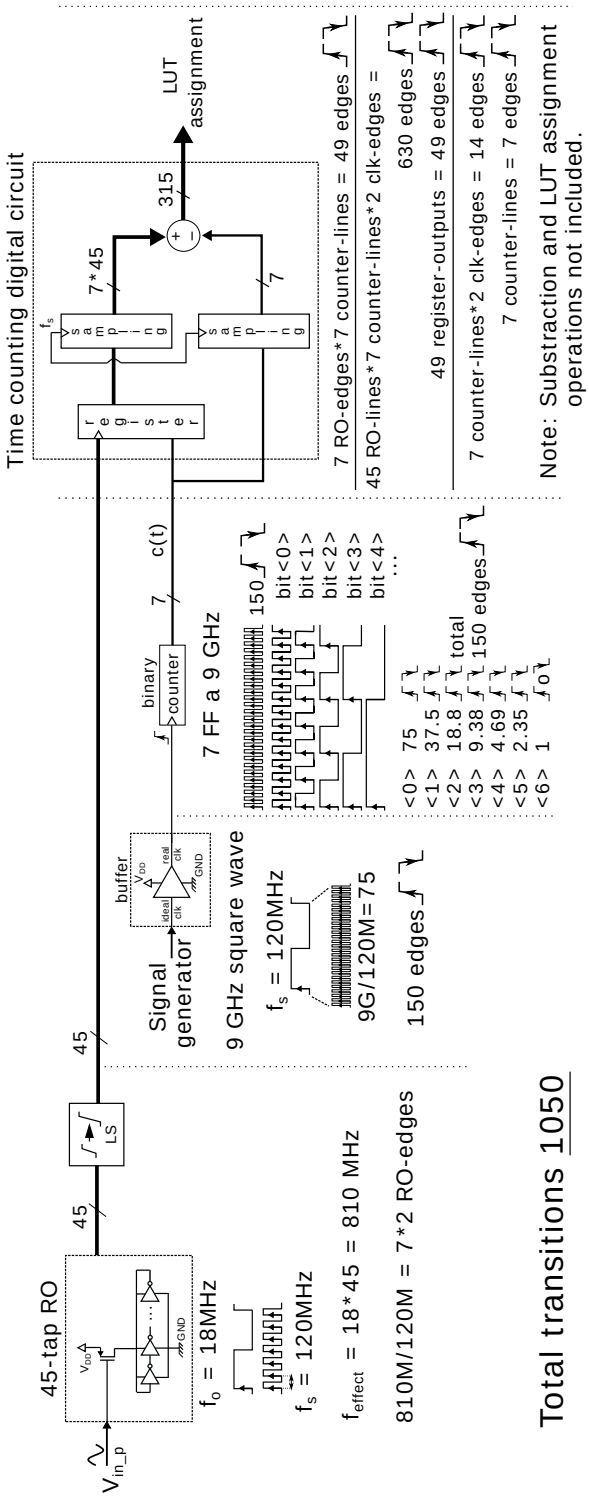


FIGURE 5.13: Circuit for the proposed Nyquist RO-based ADC converter.

output is a digital value that represents the discretized time q[n] determined by the external square signal. The output assigns the instantaneous amplitude corresponding to q(t) of the proposed pulse shaping filter as the final result (the black dots). This value is stored in a LUT whose index matches with q[n].

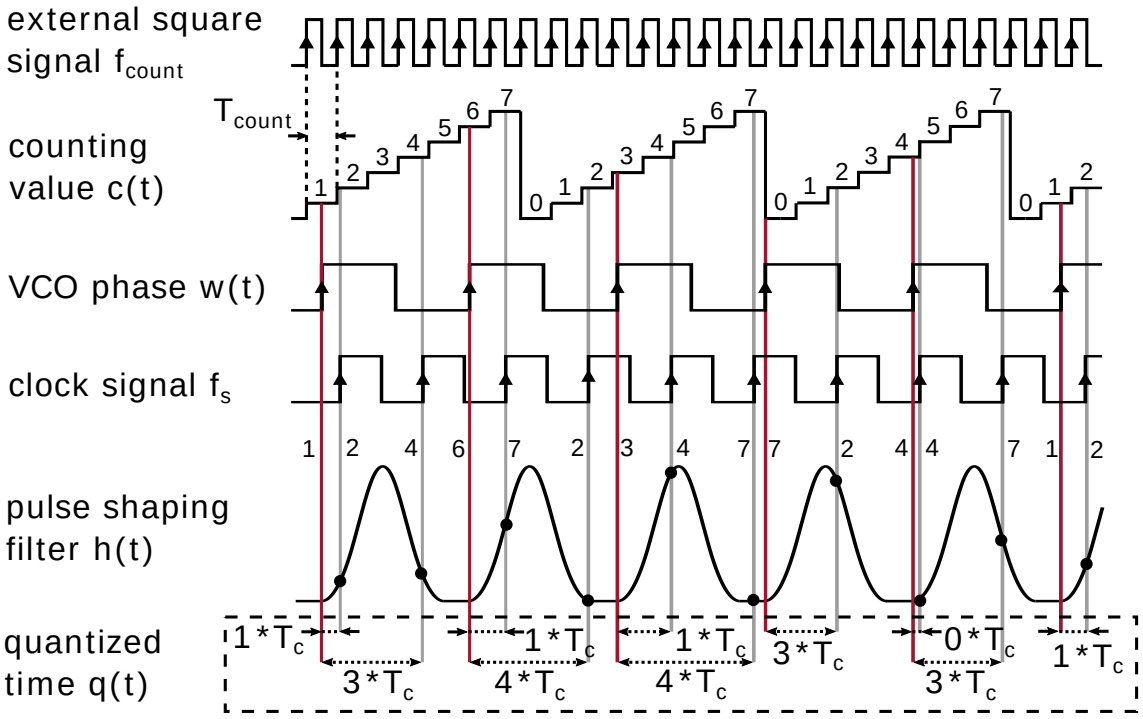


FIGURE 5.14: Chronogram from circuit of Figure 5.13.

5.3.2.3 Behavioral simulations

A behavioral model of the circuit shown in Figure 5.13 is built and simulated with the same parameters of Figure 5.12(a), using and ideal counter. The resulting output spectra for several oscillation frequencies of the external signal are depicted in Figure 5.15. 9 GHz of oscillation for the external square waveform is selected. Although the slope of the notch at 60 MHz is less noticeable and the spectrum is slightly flattened at low frequencies, the resolution is not significantly degraded, and the out-of-band blockers are completely removed.

To get a similar performance with the conventional oversampled approach, the required circuit will look as in Figure 5.16. The architecture corresponds to an open-loop configuration for VCO-based ADCs with a digital decimation filtering as the last stage.

In this conversion structure, the first-difference block, based on two flip-flops and an XOR gate, produces a pulse of width T_s for every rising and falling edge from the RO output phases. The proposed Nyquist RO-based ADC structure

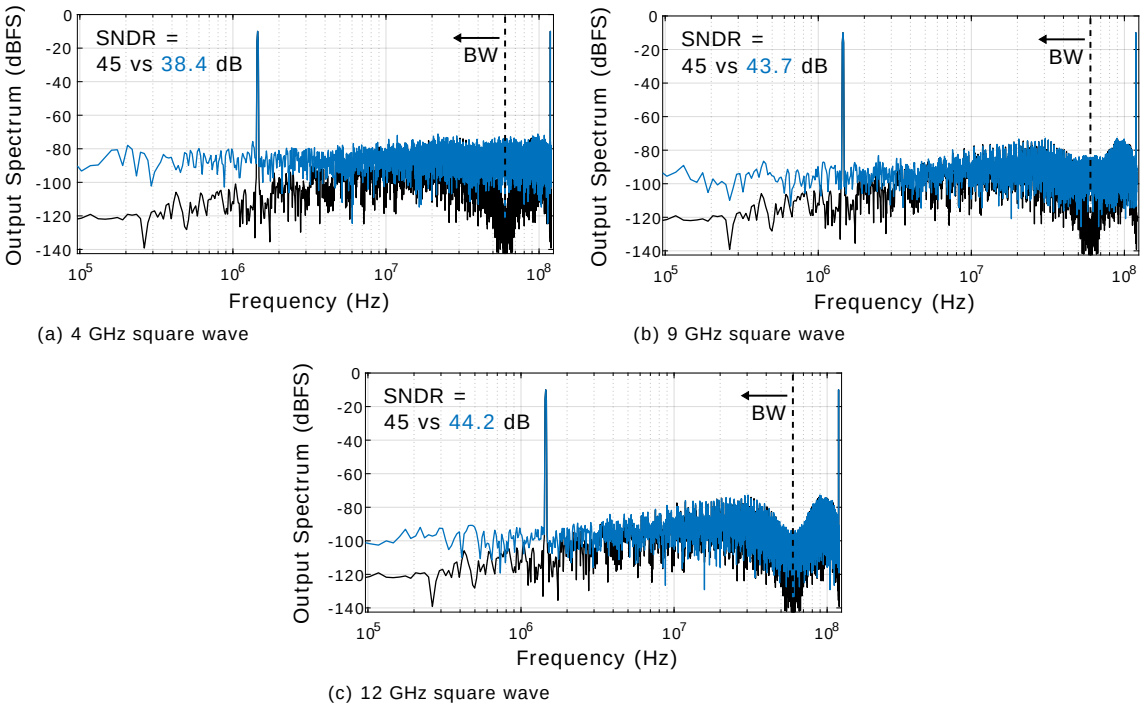


FIGURE 5.15: Output spectra of the proposed architecture digital output (blue) of Figure 5.13 using an external square signal of (a) 4 GHz, (b) 9 GHz and (c) 12 GHz, and the theoretical one (black) in Figure 5.12(a).

considers only the rising edges. Therefore, a resolution improvement might be achieved merely by using the inverted VCO signals and doubling the digital logic. Thus, the final resolution will theoretically enhance 6 dBs [23], being equivalent to double the number of RO output phases, with the same oscillation parameters. The spectrum depicted in Figure 5.17 shows the performance of this proposal taking into account both rising and falling edges from the oscillator signals. The resulting resolution improved as expected, at the cost of duplicating the digital sampling circuitry. This action supposes a power consumption increasing twice the value that corresponds to the digital logic, being still substantially less compared to the oversampled converter as discussed in Section 5.3.4, and with a higher resolution.

The proposed idea offers higher flexibility to modify the nulls location in software, only by changing the pre-loaded values of the LUT. Additionally, the presented structure allows us to connect different LUTs in parallel for programmable multimode multiband receivers using the same front-end circuit. The same operation in the oversampled case would require different digital filters, even going

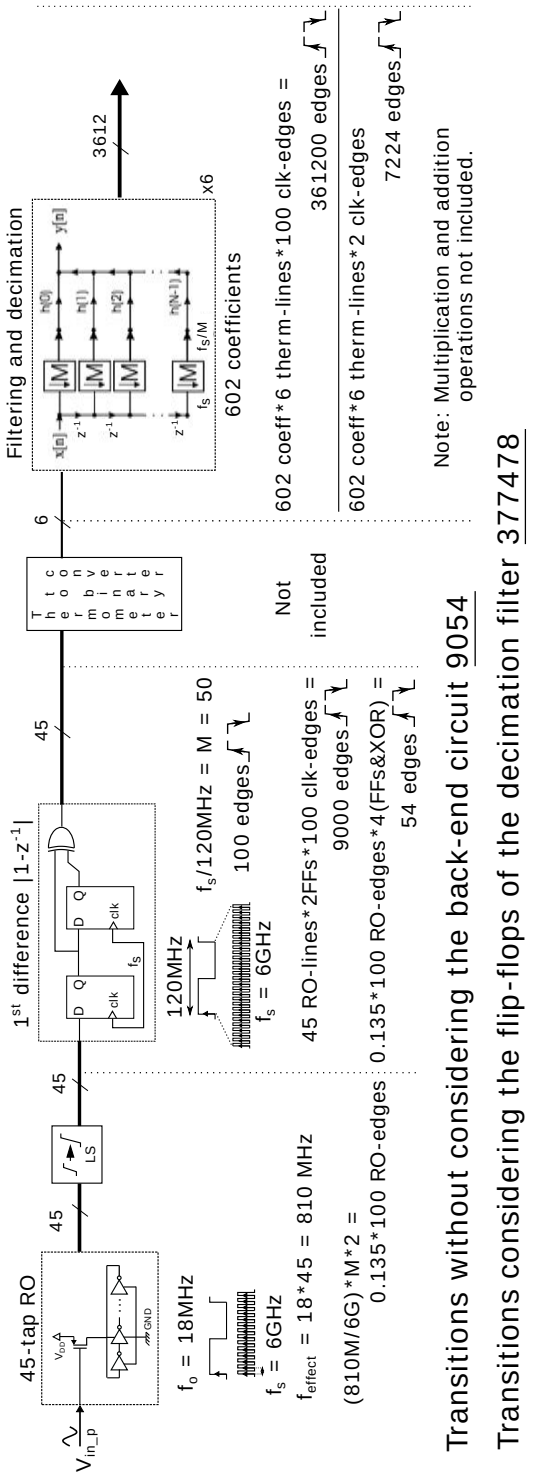


FIGURE 5.16: Circuit for conventional oversampled RO-based ADC converter.

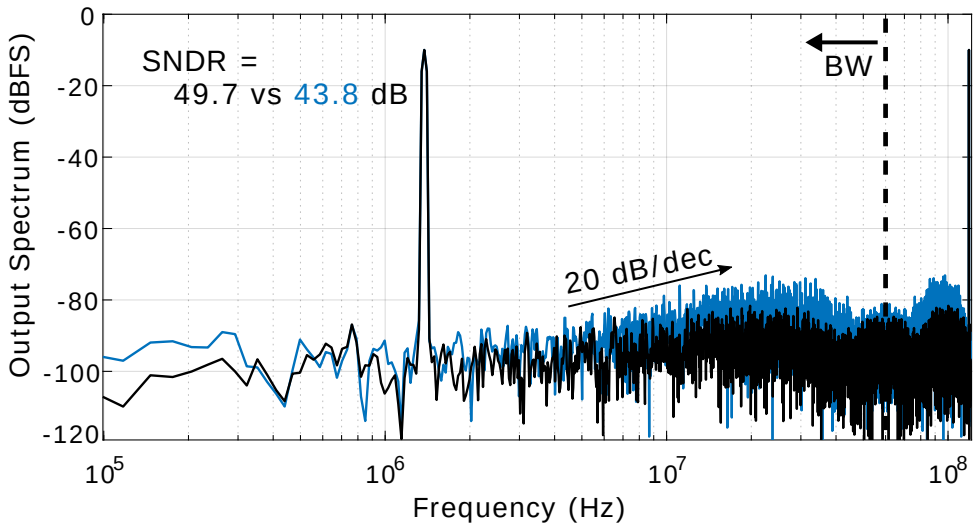


FIGURE 5.17: Output spectra of the proposed architecture digital output considering only the rising edges (blue) and both edges (black).

towards more complex filter proposals. Furthermore, the wide-band modulation components in our proposal are attenuated more than using a single first-order *sinc* function as in the case of the oversampled conventional architecture limiting the achievable resolution even before the decimation filtering stage (see Figure 5.18). Noise level can be reduced by increasing the sampling frequency, but the complexity and speed/memory requirements, mainly for the decimation filtering, are much higher.

The architecture in [29], discussed at the end of Section 5.2.2 about band-pass ADC implementations, also provides a solution for multistandard communication. The architecture is an oversampled ADC that still needs the decimation filter. Additionally, the number of the RO-based ADCs used in the system must be carefully analyzed because the converter performance could severely deteriorate due to the mismatch between the multiple channels, particularly the VCO and the S&H circuits. Furthermore, the higher the number of channels, the higher the power consumption, and the more complex becomes the layout implementation.

5.3.3 Data-path precision

As we are considering the full process of digitization for both cases, the data type and the word length used in the LUT (for the Nyquist case) and in the filtering and decimation digital operations (for the oversampled case) become relevant for a fair comparison. Fixed-point data type is used with two's-complement representation for both cases.

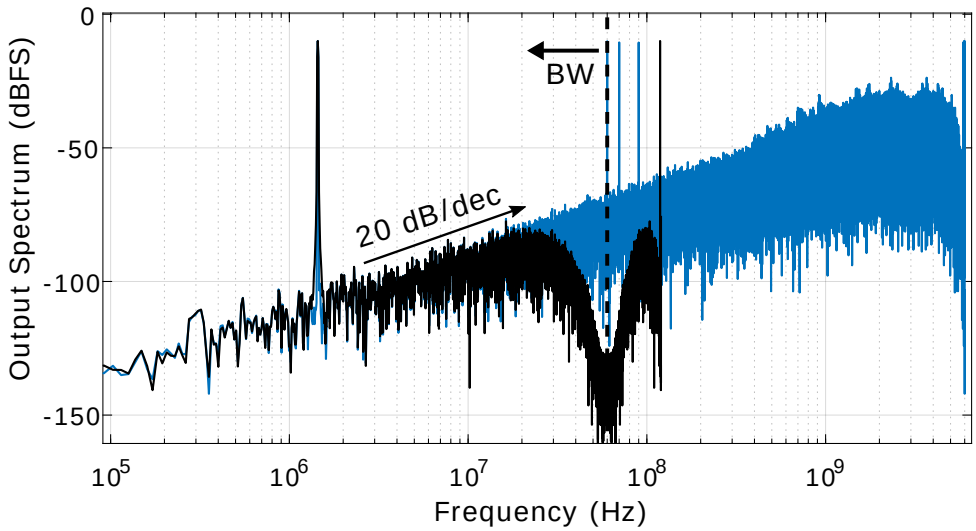


FIGURE 5.18: Output spectra of the digital output for the oversampled VCO-based ADC converter before (blue) and after (black) the decimation filtering stage.

For the Nyquist case, 20-bit binary word length is selected to get an SNDR of 40 dB, as is shown in Figure 5.19 (the black line). The blockers are still entirely removed. For the oversampled case, the word length used for the coefficients and the rest of the data-path of the decimation filter (the product output and the accumulator) are reduced to 14 bits, including the digital output. The output spectrum under this limitation is also plotted in Figure 5.19 (the blue line). The SNDR decreases by 5 dB compared to the theoretical spectrum, the blue one in Figure 5.12(a), while providing an out-of-band rejection ratio of 51 dB.

Higher sensitivity to the word length is observed for the Nyquist proposal, which entails dealing with more bits in the final application. However, the LUT addressing is still quite simple as neither additions nor multiplications are required. Greater attenuation of the blockers is also noticed in the Nyquist case.

5.3.4 Power consumption analysis

An estimation of the transitions per conversion step $T_s = 1/120$ MHz is performed to make a power comparison. Figure 5.13 and Figure 5.16 illustrate the number of transitions per block. The RO and the level-shifters (LS) are the same for both proposals, so these blocks are not considered. Also, all those operations that include a count of transitions highly dependent on the circuit implementation, such as additions/subtractions or multiplications, are skipped.

For the Nyquist case, the estimations are performed using a 7-bit binary counter considering that the external square signal frequency is selected of a value of 9 GHz. The number of transitions equals 1050 per conversion step, and for the

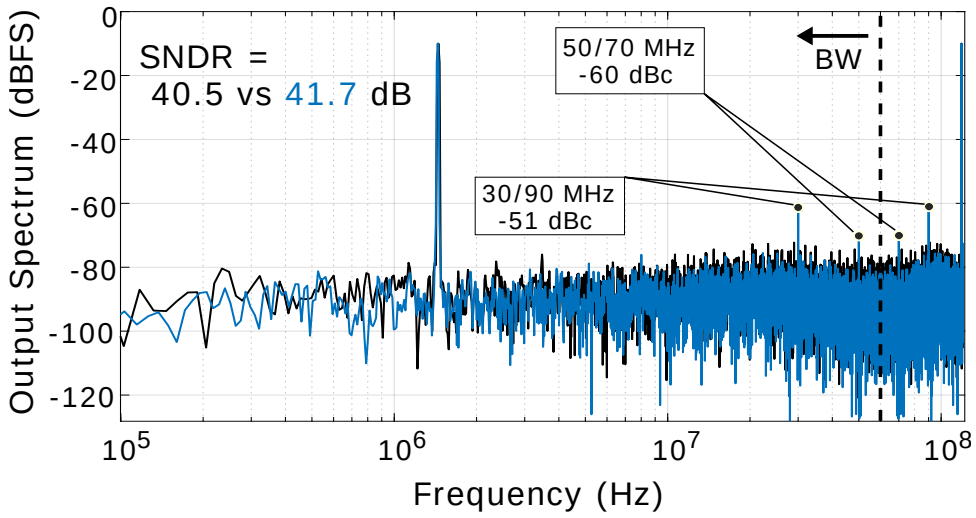


FIGURE 5.19: Output spectra of the digital output with a limited binary word for the oversampled VCO-based ADC converter (blue) and the proposed Nyquist converter (black).

oversampled case, the number of transitions equals 9054 (decimation and filtering operations not included). Even without taking into account the back-end circuitry of the oversampled case, the Nyquist structure shows more than 8 times less transitions. Considering the operation of the flip-flops needed in the delay line and the decimation stage, the number of transitions increases up to more than 350 times than in the Nyquist case. Table 5.2 below indicates the transitions in every block of both architectures. In the case of the circuit for the Nyquist converter considering both edges from the VCO signals, the number of transitions increases to 1800 (1050+750 transitions for the additional digital circuit), constituting an amount 5 times lower than for the oversampled case.

TABLE 5.2: Number of transitions per block of both architectures.

Nyquist-rate ADC	Buff. ext.s. 150	7-bit count. 150	Samp. TCDC 749	Adders TCDC Not included	Total **1049**
Oversampled ADC	1^{st}-differ. 9054	T2B Not included	Samp. Dec. 368424	Mult.&Acc.D. Not included	Total **377478**

Buff.ext.s = buffer for external square signal.
count. = binary counter.
Samp. = Sampling.
TCDC = Time Counting Digital Circuitry.
1^{st}-differ. = first-difference.
T2B = Thermometer-to-binary
Dec. = Decimation.
Mult.&Acc.D. = Multiplication and Accumulation for Decimation process.

5.4 Conclusion

In this chapter, two ways of applying PFM-interpretation of RO-based ADCs are introduced to implement maximally digital radio receivers architectures seizing the advantages of advanced ultra deep-submicron processes. In both proposals, programmable pulse shaping filters are designed to customize the spectral properties, which enables great flexibility in the implementation by using the same front-end circuit for several applications.

A new architecture to implement a VCO-based ADC with a quadrature bandpass NTF was proposed in Section 5.2 without the need of neither time-interleaved nor closed-loop structures. Additionally, the NTF can be tuned in software by adjusting the values stored in LUTs. This is of special interest for the implementation of flexible radio receivers. The architecture was explained theoretically, but a practical circuit was also proposed. Behavioral simulations were provided to validate the theory and the practical implementation, along with power estimations and circuit impairments.

In Section 5.3, a Nyquist RO-based ADC architecture incorporating a programmable pulse shaping filter was presented to remove blockers in wireless communication systems. The proposal was proven to be a more efficient solution in terms of power than the conventional oversampled RO-based ADC with a decimation filter stage. The pulse shaping filter is customized to place nulls at the frequencies where some blockers are expected. Due to the digital nature of this pulse shaping filter, the position of these nulls can be adjusted by software by means of pre-loaded values at LUTs, which makes the proposal suitable for multimode multiband radio receivers. A data-path analysis showed that the proposed system required a higher word length than the oversampled case for the same resolution, but the power consumption was substantially lower and the mitigation of the blockers is higher.

The proposed architectures were implemented with a simple and flexible digital design while offering a good performance suitable for modern communications systems.

Chapter 6

Conclusions and future work

6.1 Conclusion

In this thesis, several proposals have been described and discussed to be used in RO-based open-loop A/D conversion architectures. The proposed ideas are oriented to solve issues such as the RO nonlinearity and the restricted oscillation frequency. These issues severely restrict the achievable resolution of an ADC, especially for high-bandwidth applications. Recently, the equivalent between pulse frequency modulation and RO-based ADCs was established through a pulse shaping filter. Customized pulse shaping filters may suppose efficient spectral shaping properties to optimize parameters such as power and resolution. Finally, with this perspective in mind, two new RO-based architectures are proposed: a RO-based band-pass ADC and a Nyquist-rate RO-based ADC highly efficient in power. Both proposals are mostly digital, highly suitable for deep-submicron CMOS processes. Although the presented research is specially devoted for wide-band A/D conversion, the ideas proposed could be extended to other A/D conversion fields such as biomedical instrumentation or sensing. The document is split up into three blocks:

- Techniques for nonlinearity compensation.
- Techniques to increase the maximum oscillation frequency.
- Techniques to customize the pulse shaping filter.

Firstly, two solutions to compensate for the nonlinear transfer function of ring oscillators were presented in Chapter 3 for open-loop configurations. Firstly, a new delay cell is proposed to linearize the CCO transfer function. The circuit is composited by three NOT gates in parallel connected to different supply voltage levels. The proposal was experimentally validated with a prototype implemented in 65-nm technology. This solution suppose the design of a linear front-end stage that computes the voltage-to-current conversion. The second idea compensates for the RO nonlinearity by implementing the inverse of the CCO current-to-frequency response using several transconductors that provide the current into the RO. The proposed circuit was designed and validated by

transistor-level simulations in a 65-nm CMOS process. This alternative requires calibration technique to achieve a significant distortion reduction for any PVT variation. The solutions showed great mitigation of the distortion at the output data for large-swing differential input signals. Comparisons to the state-of-the-art were performed, which demonstrated that the proposed circuits are highly robust with considerable less complex design, and well-suited for all applications like biomedical instrumentation, sensing or Internet-of-Things (IoT) modules.

Secondly, some methods to boost the effective oscillation frequency of RO-based A/D conversion architectures were proposed and described. Chapter 4 covered several ways of overcoming the gain limitation of RO-based ADCs and improving the final resolution. Both ideas are based on minimizing the delay between the output phases. The first solution uses a passive network to get interpolated phases between two consecutive phases of a RO and inject it into identical ROs, increasing the number of taps without penalizing the effective oscillation frequency. The second alternative proposed a new delay cell circuit to reduce the propagation delay in RO. Both proposals were validated by transistor-level simulations in 65-nm CMOS process showing a proper power-efficiency. The solutions are highly portable between technology nodes and well-suited for high-bandwidth (dozens of MHz) and medium-resolution (10–12 ENOBs) applications, such as 5G or Internet-of-Things (IoT) devices.

Finally, two new conversion architectures for maximally digital radio receivers were described in Chapter 5. The approaches consist of customizing a pulse shaping filter using the PFM-interpretation of RO-based ADCs. The nulls are placed at interest frequencies, either removing blockers of the spectrum or implementing a quadrature band-pass NTF. The frequency response of the filter is approximated by digital quantization with LUTs, being tuned by software which enables high programmability and allows using the same front-end circuit for different approximations. Both architectures were implemented with a simple and flexible digital design of special interest for highly integrated modern communication systems.

6.2 Contributions

More specifically, the main contributions of this research work are summarized as follows:

Chapter 3

- A novel delay cell for ring oscillator circuit presented in Section 3.2, that improves the linearity of conventional CMOS-based NOT gate circuit by mixing two kinds of delay cells. A prototype of a CCO with the proposed structure is implemented and manufactured in 65-nm technology. The test circuit occupies 0.00094 mm^2 and consumes 45 μW. The measurements results show harmonics distortion terms below -58 dB for a 7 μA_{pp} input signal

amplitude. The power consumption can be minimized a 33% by decreasing the supply voltage with a low impact on the final resolution. Additionally, measurements to several dies revealed that the solution exhibits excellent performance to manufacturing process. The proposed structure offers a proper linearity performance and robustness with great area and power consumption efficiency. The design is also examined for high-bandwidth applications by transistor-level simulations using a pseudo-differential configuration. The HD3 term is attenuated -19 dB compared to the obtained value with the conventional RO structure, achieving an SNDR of 72 dB over a bandwidth of 10 MHz.

- A new circuit-based approach to mitigate nonlinearity in open-loop RO-based ADCs proposed in Section 3.3. The circuit designed in the 65-nm CMOS process and evaluated in an open-loop configuration led to a more than 3-ENOB enhancement in simulation for a high-swing differential input voltage signal of 800-mV_{pp}, with considerably less complex design and lower power and expected area in comparison to state-of-the-art circuit-based solutions. The power distribution of the proposed circuit per side of the pseudo-differential architecture is as follows: the VCO consumes 1.5 mW in line with similar previous works; the opamps for the three transconductors that drives the current into the RO consume a total power of 345 μW; and the branch that generates the required offset voltages consumes 3.6 μW. The architecture has also been checked against PVT and mismatch variations, proving to be highly robust, requiring calibration technique. Nevertheless, due to its highly digital nature, the calibration block occupies less area and presents a simpler design than other calibration circuits.

Chapter 4

- A simple and passive way of overcoming the gain limitation by increasing the number of phases in a ring oscillator described in Section 4.2. The proposed method combines a passive interpolation and phase injection to get extra phases from a ring oscillator and inject them into identical ring oscillators. This technique allow the delay cells in a RO-based ADC to be increased keeping the same effective oscillation frequency. The idea is validated by transient simulations with designs in a 65-nm CMOS process. The SNR is improved 5.5 dB by doubling the number of ring oscillators used in the data converter achieving a total enhancement of 11 dB from a data converter with four ROs. The power consumption associated to each ring oscillator is 133 μW. The solution enables the reduction of the input signal in order to minimize the total harmonic distortion and to get an adequate quantization noise level at the same time. The solution is very simple and exhibits proper resolution improvement with excellent power performance compared to other published works.

- A new delay cell for the implementation of high-speed low-power ring oscillators introduced in Section 4.3 with a minimum delay lower than the achieved one for the conventional delay cell used in ring oscillators. The presented delay cell is composed by two devices between the supply nodes, thus the voltage supply can be reduced for certain oscillation requirements. Unlike the typical RO structure, the power consumption of the proposal depends on the number of cells in the ring oscillator. Then, the solution is of interest by using a reduced number of cells in such a way that the computing load is transferred from the oscillator to the digital logic afterwards. In consequence, high-speed digital logic implemented with a narrow CMOS process is a must. Comparisons between a conventional oscillator and the proposed one showed improvements of the latter case in terms of resolution, power, and area. The circuits are designed in 65-nm technology and simulations are performed to validate the solution. The proposed delay cell circuit offers up to 25% faster RO designs for the same supply voltage. The RO circuit is more power-efficient than the conventional structure using less than 5 of the new cells. Furthermore, by reducing the supply voltage, the proposed RO exhibits a higher oscillation frequency consuming similar power.

Chapter 5

- A systematic way to implement a band-pass NTF in an ADC implemented with an RO proposed in Section 5.2. The approach is based on the PFM-interpretation of an RO-based ADC, where the NTF is defined by a suitable pulse shaping filter inserted after the oscillator. The pulse shaping filter is defined to implement a quadrature band-pass NTF. Hardware implementation is proposed using a digital delay line whose outputs are decoded with two LUTs. This enables tuning the NTF in software. Behavioral simulations are performed to validate the implementation and robustness of the approach. The band-pass ADC achieves an SNDR of 70 dB over a bandwidth of 3 MHz suffering a resolution degradation of only 3 dB with mismatch of 30% between the elements that compose the delay line. A case study of the power consumption is elaborated for the case of a 65-nm CMOS process. The overall estimated power is 5.8 mW, using 0.6 V as supply voltage. The solution consists of a fully digital and programmable design, enabling a very low area with competitive power consumption.

- A robust-against-blockers radio receiver structure using a Nyquist RO-based ADC presented in Section 5.3. The approach consists of customizing a pulse shaping filter, placing nulls at the frequencies where some blockers are expected. The frequency response of the filter is approximated by digital quantization with LUTs, which enables high programmability for multiband signal reception. The proposed structure is compared to the

conventional oversampled one, showing significant power reduction with similar resolution performance. An estimation of the transitions of both architectures reveals that the oversampled ADC supposes 8 times the required number of transitions per conversion step of the proposed Nyquist-rate structure without including the back-end stage for decimation process; considering this block the number of transitions is increased by 40, which is 350 times higher compared to the Nyquist case. The proposal is validated with behavior simulation.

6.3 Future work

This section will suggest improvements to the presented ideas and propose several guidelines of interest for future research:

Chapter 3

- Implementing a scaling-friendly and low-power linear transconductor for the proposal of Section 3.2.
- Designing the opamp's offset tuning circuit and implementing the proposed calibration circuit to evaluate the performance of the entire proposal in Section 3.3.
- Analyzing the RO linearity property according to the frequency of the input signal. Develop a method to characterize the dynamic behavior of nonlinear response and combine it with the static behavior employed in this chapter. This way, the RO nonlinear effect would be fully described and therefore the harmonic distortion of an RO-based ADCs could be precisely established.

Chapter 4

- Analyzing the effect of the mismatch between the oscillators employed in the idea proposed in Section 4.2. Verifying the phase noise behavior due to the thermal noise component relative to the resistive network and the component associated with the flicker noise of the oscillators.
- Evaluating the possibility of putting severals transconductors instead of using only one (approach introduced in Section 3.3 of Chapter 3) into the proposed delay cell in Section 4.3 to linearize the voltage-to-frequency transfer function.
- Implementation of test chips with the proposed circuits for experimental validation.

Chapter 5

- Implementing the oscillator and required level-shifters of the proposal in Section 5.2. Optimization of proposed digital circuitry in terms of power consumption.
- More accurate evaluation of power consumption and comparison between Nyquist-rate and oversampled solution.
- Circuit implementation and experimental chips for validation of the proposed ideas.

Appendix A

Appendix for Section 3.3

A.1 INL and DNL analysis

ADCs are fully characterized by both static and dynamic parameters. Testing methods commonly combine a histogram-based approach with a spectral analysis to obtain a total characterization. Depending on the application and the kind of ADC one or other parameters take more significance to describe the performance of the converter. However, studies about testing expose that the evaluation of dynamic parameters offers accurate information about variations in a system and describes well enough the global performance according to [110].

Nonlinearity in ring oscillators is due to the nonlinear voltage-to-frequency transfer function which leads to harmonic distortion at the output spectrum, as is discussed before. Usually, DNL parameter has a low value in VCO-based ADCs, but INL parameter shows a large peak error because of the difference between the ideal oscillation frequency and the achieved one.

INL value indicates the maximum deviation (positive and negative) from the ideal output. Nevertheless, the maximum value might not provide enough information, because it usually occurs when the input signal is sufficiently high only (see Fig.4). Thus INL might not be significant when dealing with low-voltage amplitude input signals because of its static nature. This is not the case as in Flash or SAR converters where the INL may affect even for low-voltage amplitude input signals. Additionally, static parameters such INL or DNL in VCO-based ADCs depend on the relative phase shift between the output phases and the sampling signal and on the selected sampling signal.

Therefore dynamic parameters like SNDR, SINAD, SFDR, or THD are preferable with VCO-based ADCs as a measurement of the system degradation as can be seen in the following references: [6], [10], [20], [25], [27], [28].

Static parametrization with INL/DNL values is difficult in VCO-based ADCs (time-encoded ADCs in general) because it depends on the sampling frequency and it is not clear when going from one code to the next one. For a DC input value, the digital code will toggle between two adjacent values. Assuming an OSR equal to 1 the INL is estimated as is done in [89] for VCO-based ADCs, estimating the code for each frequency value, calculating the difference between the ideal code and the real one, and finally extrapolating the results to LSBs. DNL

in VCO-based ADCs does not provide significant information as the digital word does not remain constant for a DC input value, and it is difficult to define which range of input values corresponds to 1 single LSB.

The static characterization is performed using a best-fit straight-line for a ramp test. Below the formulations for the procedure of INL and DNL calculations are provided along with a general representation (see Figure A.1) with the values achieved for the proposal.

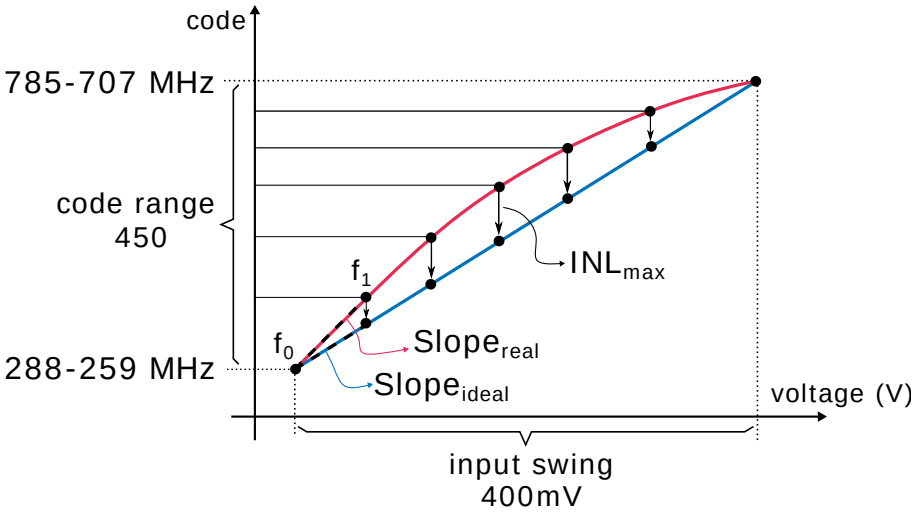


FIGURE A.1: DNL/INL representation for the presented VCO-based ADC.

For a ring oscillator, the frequency depends on the propagation delay of the NOT gates (t_{pd}) by equation (2.16), where the number of stages, in this case, is N = 45.

The digital code calculation for a VCO-based ADC is formulated as:

$$Dig.code = \frac{\frac{1}{t_{pd}}}{f_s}. \tag{A.1}$$

where f_s corresponds to Nyquist frequency (2·BW = 100 MHz, OSR = 1), and t_{pd} is modulated by the input signal. Finally, the digital code can be obtained by combining equation (2.16) and (A.1).

In the system, with $f_{osc\text{-}min}$ = 288 MHz (for $t_{pd\text{-}max}$) and $f_{osc\text{-}max}$=785 MHz (for $t_{pd\text{-}min}$), the digital code is in the range 259 and 707:

$$Dig.code_{low} = \frac{288e^6 \cdot 2 \cdot 45}{100e^6} = 259.2; \quad \text{and} \quad Dig.code_{high} = \frac{785e^6 \cdot 2 \cdot 45}{100e^6} = 706.5.$$

For a VCO-based ADC, since the conversion is based on time-encoding, LSB is represented by a frequency variation. The ideal relation obtained is:

$$R_{\text{LSB}} = \frac{\Delta freq}{\Delta code} = \frac{785\text{e}^6 - 288\text{e}^6}{706 - 259} = 1.11\ \frac{MHz}{LSB}.$$

The DNL error represents the difference between the conversion step for the ideal ADC transfer function and the achieved one. This value can be determined, for this case, by the relation between the slopes of the conversion curves. For the circuit proposed, with a single-ended input voltage swing equal to 400mV, the slope is:

$$Slope_{\text{idealADC}} = \frac{\Delta freq}{\Delta volt} = \frac{785\text{e}^6 - 288\text{e}^6}{0.4} = 1242.5\ \frac{MHz}{V},$$

and finally, the DNL is

$$DNL(LSB) = \frac{Slope_{\text{realADC}}}{Slope_{\text{idealADC}}} - 1.$$

The INL is described as the deviation of the values of the achieved ADC curve from the ideal one:

$$INL(LSB) = \frac{f_{\text{real}} - f_{\text{ideal}}}{R_{\text{LSB}}}.$$

Figure A.1 depicts how both deviations, INL and DNL, are graphically represented in a plot code versus input signal with the ideal response of the converter. Charts in Figure 3.31 and 3.31(b) show the resulting INL and DNL, respectively, of the system with the circuit proposed: INL and DNL errors are in the range of [-0.44 0.26] and of [-0.032 0.049], respectively.

Appendix B

Appendix for Section 5.3

B.1 Convolution operation

Figure B.1 illustrates the signals in time corresponding to the three out-of-band components to be removed. The convolution of those signals shows zeroes at the fundamental frequencies and theirs multiplies in frequency spectrum.

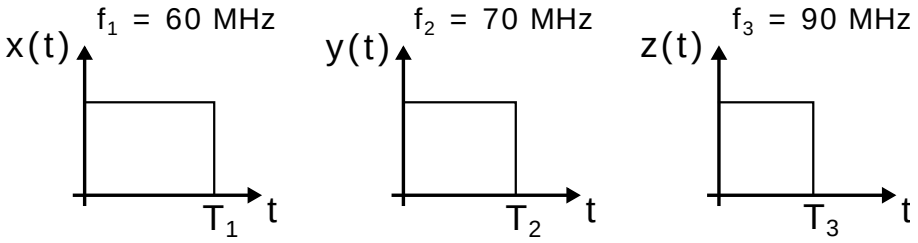


FIGURE B.1: Signals in time corresponding to blockers at 60, 70 and 90 MHz.

The mathematical analysis to develop the convolution of the two first signals and obtain the formulations that defines the variation on time of the resulting signal w(t) are below. The convolution of x(t) and y(t) is given by (see Figure B.2):

$$w(t) = x(t) * y(t) = \int_{-\infty}^{\infty} x(\tau) \cdot y(t-\tau)\, d\tau$$

The integral of the product of x(t) and y(t) on each overlapping interval between both signals are determined and depicted in Figure B.3, including the extremes of the right-side and the left-side of the resulting piecewise function w(t):

$$w(t) = \int_{0}^{t} x(\tau) \cdot y(t-\tau)\, d\tau = 1 \cdot \int_{0}^{t} d\tau = \tau|_{0}^{t} \quad 0 < t \leq T_2; \tag{B.1}$$

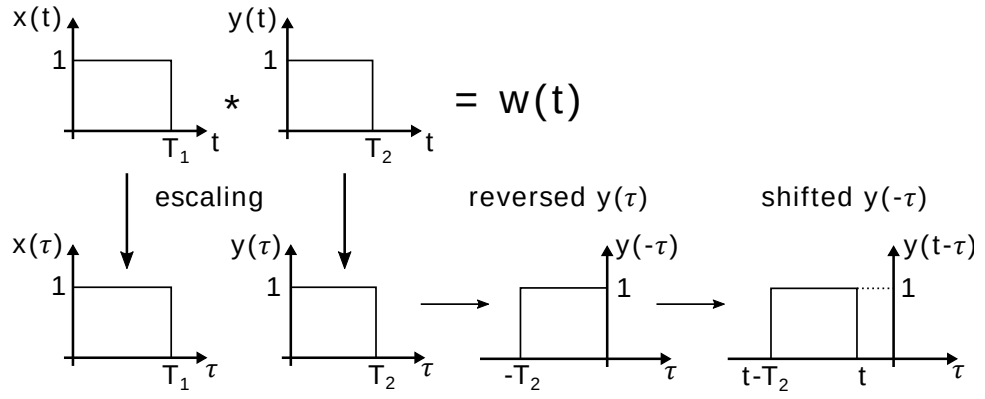


FIGURE B.2: Convolution operation on x(t) and y(t), where y(t) is reversed and shifted.

$$w(t) = \int_{t-T_2}^{t} x(\tau) \cdot y(t-\tau)\, d\tau = 1 \cdot \int_{t-T_2}^{t} d\tau = \tau|_{t-T_2}^{t} \quad T_2 < t \leq T_1; \tag{B.2}$$

$$w(t) = \int_{t-T_2}^{T_1} x(\tau) \cdot y(t-\tau)\, d\tau = 1 \cdot \int_{t-T_2}^{T_1} d\tau = \tau|_{t-T_2}^{T_1} \quad T_1 < t \leq T_1 + T_2. \tag{B.3}$$

Figure B.4 shows the resulting time responses of w(t) from the convolution of x(t) and y(t), pulses with width values of T_1 and T_2. The function w(t) is defined in five intervals given by:

$$w(t) = \begin{cases} 0 & t \leq 0 \\ t & 0 < t \leq T_2 \\ T_2 & T_2 < t \leq T_1 \\ -t + (T_1 + T_2) & T_1 < t \leq T_1 + T_2 \\ 0 & t > T_1 + T_2 \end{cases}$$

The convolution of the resulting w(t) and z(t) is expressed as follows (see Figure B.5):

$$w(t) = w(t) * z(t) = \int_{-\infty}^{\infty} w(\tau) \cdot z(t-\tau)\, d\tau$$

The integral of the product of w(t) and z(t) on each overlapping interval between both signals are determined and depicted in Figure B.6, including the extremes of the right-side and the left-side of the resulting piecewise function h(t):

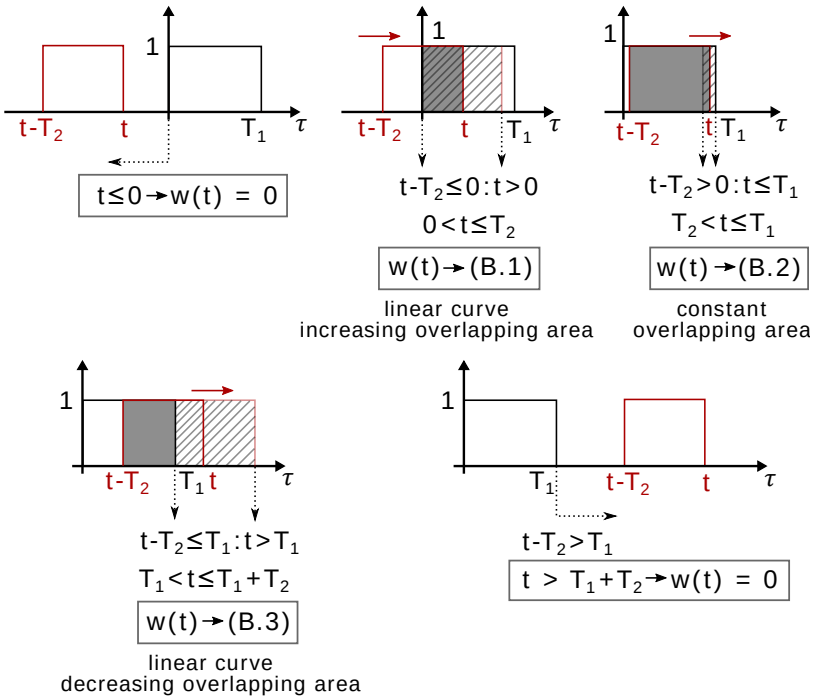


FIGURE B.3: Convolution operation on x(t) and y(t), intervals of the function w(t). The gray zones illustrate the moving overlapping areas between both x(τ) (the black one) and y(t-τ) (the red one) on each interval, defined by the integrals of the product of those two functions (equations B.1, B.2 and B.3). The zones with a strip pattern represent the intervals of the resulting function w(t) that delimits the shiftment of y(t-τ).

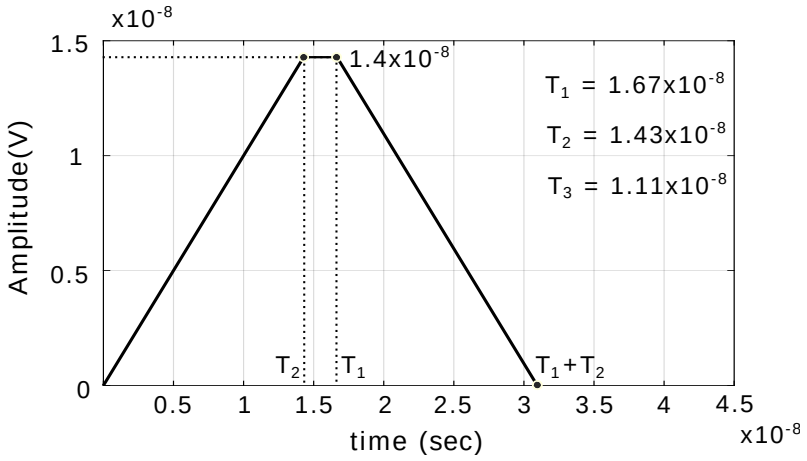


FIGURE B.4: Time impulse response of the pulse shaping filter w(t) designed to remove blockers at 60 and 70 MHz.

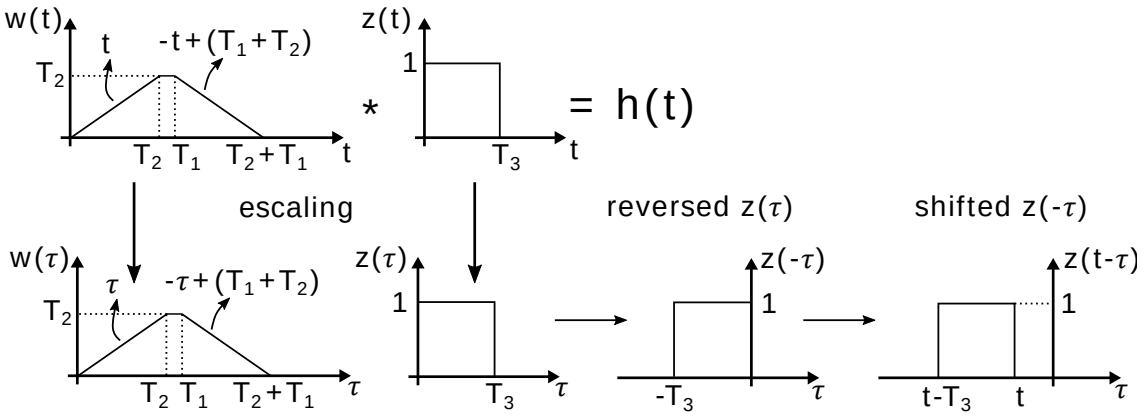


FIGURE B.5: Convolution operation on w(t) and z(t), where z(t) is reversed and shifted.

$$h(t) = \int_0^t w(\tau) \cdot z(t-\tau)\, d\tau = 1 \cdot \int_0^t \tau\, d\tau = \frac{\tau^2}{2}|_0^t \quad 0 < t \leq T_3; \tag{B.4}$$

$$h(t) = \int_{t-T_3}^t w(\tau) \cdot z(t-\tau)\, d\tau = 1 \cdot \int_{t-T_3}^t \tau\, d\tau = \frac{\tau^2}{2}|_{t-T_3}^t \quad T_3 < t \leq T_2; \tag{B.5}$$

$$h(t) = \int_{t-T_3}^{T_2} w(\tau) \cdot z(t-\tau)\, d\tau + \int_{T_2}^t w(\tau) \cdot z(t-\tau)\, d\tau =$$
$$1 \cdot \int_{t-T_3}^{T_2} \tau\, d\tau + T_2 \cdot \int_{T_2}^t d\tau =$$

$$\frac{\tau^2}{2}|_{t-T_3}^{T_2} + T_2 \cdot t|_{T_2}^t \quad T_2 < t \leq T_1; \tag{B.6}$$

$$h(t) = \int_{t-T_3}^{T_2} w(\tau) \cdot z(t-\tau)\, d\tau + \int_{T_2}^{T_1} w(\tau) \cdot z(t-\tau)\, d\tau + \int_{T_1}^t w(\tau) \cdot z(t-\tau)\, d\tau =$$
$$1 \cdot \int_{t-T_3}^{T_2} \tau\, d\tau + T_2 \cdot \int_{T_2}^{T_1} d\tau + 1 \cdot \int_{T_1}^t [-\tau + (T_1+T_2)]\, d\tau =$$

$$\frac{\tau^2}{2}|_{t-T_3}^{T_2} + T_2 \cdot t|_{T_2}^{T_1} - \frac{\tau^2}{2}|_{T_1}^t + (T_1+T_2) \cdot t|_{T_1}^t \quad T_1 < t \leq T_2 + T_3; \tag{B.7}$$

$$h(t) = \int_{t-T_3}^{T_1} w(\tau) \cdot z(t-\tau)\, d\tau + \int_{T_1}^{t} w(\tau) \cdot z(t-\tau)\, d\tau =$$
$$T_2 \cdot \int_{t-T_3}^{T_1} d\tau + 1 \cdot \int_{T_1}^{t} \left[-\tau + (T_1 + T_2)\right]\, d\tau =$$

$$T_2 \cdot t|_{T_3}^{T_1} - \frac{\tau^2}{2}|_{T_1}^{t} + (T_1 + T_2) \cdot t|_{T_1}^{t} \quad T_2 + T_3 < t \leq T_1 + T_3; \tag{B.8}$$

$$h(t) = \int_{t-T_3}^{t} w(\tau) \cdot z(t-\tau)\, d\tau = 1 \cdot \int_{t-T_3}^{t} \left[-\tau + (T_1 + T_2)\right]\, d\tau =$$

$$-\frac{\tau^2}{2}|_{t-T_3}^{t} + (T_1 + T_2) \cdot t|_{t-T_3}^{t} \quad T_1 + T_3 < t \leq T_1 + T_2; \tag{B.9}$$

$$h(t) = \int_{t-T_3}^{T_2+T_1} w(\tau) \cdot z(t-\tau)\, d\tau = 1 \cdot \int_{t-T_3}^{T_2+T_1} \left[-\tau + (T_1 + T_2)\right]\, d\tau =$$

$$-\frac{\tau^2}{2}|_{t-T_3}^{T_2+T_1} + (T_1 + T_2) \cdot t|_{t-T_3}^{T_2+T_1} \quad T_1 + T_2 < t \leq T_1 + T_2 + T_3; \tag{B.10}$$

Figure 5.11 in Section 5.3.2 shows the resulting time responses of h(t) from the convolution of x(t), y(t) and z(t) (the convolution between the intermediate piecewise w(t) and z(t)), pulses with width values of T_1, T_2 and T_3. The function h(t) is defined in nine intervals given by equation 5.4.

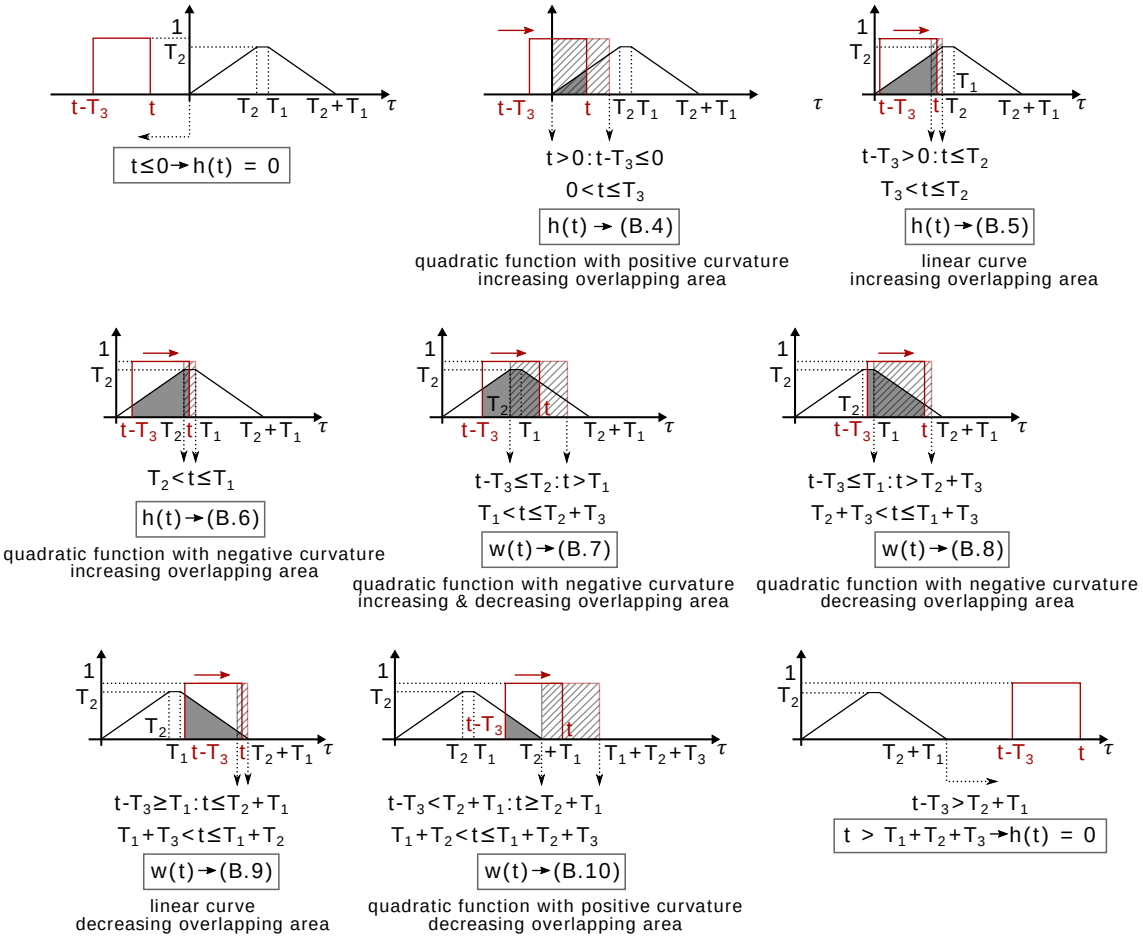


FIGURE B.6: Convolution operation on w(t) and z(t), intervals of the function h(t). The gray zones illustrate the moving overlapping areas between both w(τ) (the black one) and z(t-τ) (the red one) on each interval, defined by the integrals of the product of those two functions: equations from (B.4) to (B.10). The zones with a strip pattern represent the intervals of the resulting function h(t) that delimits the shiftment of z(t-τ).

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