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Characterization of turn off losses in Gallium Nitride switching devices-based power electronics converters

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Abstract

This thesis focuses on design and development of half bridge single phase inverter using Gallium Nitride switches. It includes step by step design of the hardware including PCB design, hardware test setup and its implementation. The thesis discusses double pulse test which is used to study the dynamic characteristics of the Gallium Nitride switches. Common mode noise is also measured at the same time. The effect of change in gate resistance on the switching losses and EMI is observed. Thus, the objective is to study the tradeoff between switching losses of the switches and electromagnetic interference in half bridge inverter.

After successful implementation of the setup, the results obtained from the double pulse test were analysed and findings were addressed. These findings can be used as a reference in order to select optimised values of gate driver components and parameters of the switches for a desired application. This approach will help in power electronic applications where priority is given to either minimising the switching losses or EMI.

Keywords Half bridge inverter, Gallium Nitride, Switching losses, EMI, Common mode noise, Hardware testing

Contents

Preface

I want to thank Professor Jorma Kyyrä and instructor D.Sc. Ahmad Bilal for their constant support and guidance throughout the thesis work. I would like to thank Yining Liu for helping me during the challenges I faced while testing.

I value the encouragement given by my friends who kept motivating me throughout the process. I am much obliged to Siddharth, Gandhali and Aniket who emboldened me.

I am eternally grateful for my family for their support and belief in me.

Shweta Kulkarni
Otaniemi, 4 November 2022

Symbols and abbreviations

Symbols

F	Switching frequency
I_D	Drain Current
P_{out}	Output power
Q_g	Gate charge
Q_{rr}	Reverse recovery charge
$R_{ds}(ON)$	On-state resistance
V_{DS}	Drain-to-source voltage
V_{GS}	Gate-to-source voltage
V_{in}	Input voltage
V_{out}	Output voltage
C_{GS}	Gate-to-source charge
C_{GD}	Gate-to-drain charge
P_{SW}	Switching power
I_L	Load inductor current
C_{oss}	Output capacitance C_{GS} + C_{GD}
R_s	Snubber resistance
C_s	Snubber capacitance
V_{DC}	DC voltage
E_{ON}	Turn on energy
E_{off}	Turn off energy
t_{rr}	Reverse recovery time
E_{oss}	Switching loss related to C_{oss}
t_{rise}	Rise time
t_{fall}	Fall time
C_{ISS}	Input capacitance
$V_{GS}(OFF)$	Gate-to-source turn off voltage
GND	Ground
V_{DD}	Positive voltage
V_{EE}	Negative voltage
C_{DC}	DC capacitor
I_{test}	Test current
L	Inductance
V_{sw}	Switching node voltage
Q_{GS}	Gate-to-source charge
Q_{GD}	Gate-to-drain charge
$R_{\theta JC}$	Thermal resistance junction to case
T_{on1}	On time
t_1	Pulse width of first pulse
t_2	Pulse break
t_3	Pulse width of second pulse
t_{don}	On time delay
t_r	Rise time
t_{doff}	Off time delay

t_f	Fall time
R_g	Gate resistance

Operators

$\frac{\mathrm{d}}{\mathrm{d}t}$	derivative with respect to variable t

Abbreviations

AC	Alternating Current
DC	Direct Current
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
GaN	Gallium Nitride
FET	Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
Si	Silicon
SiC	Silicon Carbide
WBG	Wide Band Gap
ZVS	Zero Voltage Switching
µC	Micro Controller
HEMT	High Electron Mobility Transistor
PWM	Pulse Width Modulation
EMC	Electromagnetic Compatibility
CM	Common mode
DM	Differential mode
DPT	Double pulse test
DSO	Digital Storage Oscilloscope
DUT	Device under test
LISN	Line impedance stabilization network
PC	Personal computer
UP-PWM	Unipolar PWM
IV	Current-Voltage
IC	Integrated circuit
ESL	Equivalent series inductance
SMD	Surface Mounted Device
CMRR	Common mode rejection ratio

1. Introduction

Power supplies are extensively used for various applications and have become a part of daily life. The electrification of these various applications has led it to become inevitable to use power supplies. Many power applications use inverters which require conversion of DC power into AC power; these applications include Switched Mode Power Supply (SMPS), Uninterruptible Power Supplies (UPS), solar power systems, and electric vehicles. Such inverters should ideally have less Total Harmonic Distortion (THD), Electromagnetic Interference (EMI), and high efficiency. The magnitude and the frequency of an inverter output can be controlled using different inverter topologies that include square wave inverter (VSI and CSI), and Pulse width modulated inverters. Thus, power converter topology plays an important role.

Apart from the topology, inverters can also be classified based on the type of electronic devices used for their switching. Wide band gap (WBG) devices, such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are new advancements in the field of semiconductor devices [1]. They are reliable to be the future scope in industries that manufacture power converters. Therefore, research regarding these new technology switches has been of great interest in the field of power electronics.

WBG devices have a higher band gap as compared to devices solely based on Si [2] enabling them to operate at a higher temperature, high frequencies, and voltage. Therefore, designing power converters based on these devices leads to higher efficiency performance. Thus, WBG devices have redefined the power conversion era. They have proven to be a major breakthrough in improving the performance of power converters with their availability. By replacing conventional Si devices with WBG devices, [3] shows that the hard switching losses can be reduced by 50-90%. Similar observations are found in various other studies, such as [4] [5] [6] [7] regarding the application of WBG devices in different power electronics applications. In addition to improving the efficiency by reducing the losses, these novel devices are able to operate at higher frequencies, thereby reducing the size of magnetic components required for the design. This helps to improve the power density of the system. [8] claims that there is 50% reduction in size of magnetic components by using GaN-based power converter with 1 MHz switching frequency.

However, with a higher switching frequency, the design becomes more prone to being affected by switching losses or ringing. The parasitic elements in the design that are responsible for the ringing become more sensitive with an increase in the frequency (dI/dt and dV/dt) [3] [9] [10]. Therefore, it is important to optimize the PCB layout design as well as the selection of corresponding electronic components along with the switches. Otherwise, the design may fail due to ringing leading to power loss and there will be a need for

using higher rated components, which will affect the cost of the design as well as the power density.

The fast switching of GaN High Electron Mobility Transistor (HEMT) results in a high slew rate in the voltage (*dV/dt*) and current (*dI/dt*). Moreover, these high *dV/dt* and *dI/dt* combined with parasitic inductive and capacitive elements in the power module will result in EMI noise in a wide frequency range, which will cause both conducted and radiated emission problems in differential mode (DM) and common mode (CM). Nevertheless, much research has begun towards developing multiple models and proposals that result in achieving higher efficiency high power applications [7] [8].

1.1 Objective and Scope

The aim of the thesis is to characterize the switching losses of GaN switches in an inverter by using an evaluation module which is a basic half bridge inverter based on GaN switches for the purpose of understanding the switching characteristics and EMI behavior of the device. Based on these, the gate driver, gate driver components, and inductor are selected. The rating of all the components is such that they are operated in their safe operating area. While designing any power converter, an overhead margin must be considered for the selection of electronic components. In order to validate the switching characteristics, a test setup is designed on which double pulse test method is performed to observe and measure dynamic characteristics or the switching losses. The dynamic characteristics of the switches are dependent on their dynamic gate resistance. The change in this specific parameter results into a change in the behavior of the switching characteristics. Thus, a comparison of change in the gate resistance versus the corresponding changes in the switching characteristics and EMI is measured from the hardware setup using the double pulse test. After satisfactory results are obtained, they are further analyzed and concluded.

The thesis represents a systematic approach towards the selection of switches and gate driver, gate driver components, circuit design and simulation, PCB layout design, PCB assembly, and testing of the hardware. The thesis is organized in such a way that, after Introduction chapter, the system overview is given in Chapter 2. It includes working of a half bridge inverter and its design considerations. There is an explanation of the design in detailed manner as per the design requirements and critical design parameters.

In Chapter 3, circuit design is discussed in detail where the chapter focuses more on the simulation, component sizing and selection, circuit schematic design, PCB layout and hardware assembly.

Furthermore, Chapter 4 consists of the test methods that are performed to measure the desired parameters. The hardware setup, equipment used and observations made are described in detail.

Chapter 5 is focused on discussion and analysis of the results obtained and deriving conclusions. Challenges and limitations faced during thesis are addressed here.

Following Chapter 5, Chapter 6 finally sums up the conclusion and the key learnings from the thesis. The future scope of the thesis work is also explored.

2. Technical Background

DC to AC conversion also called as inverter has many applications such as, uninterruptible power supplies, and speed control motor drives. Desired output with variable frequency and voltage is an advantage of using bridge inverters. A full bridge inverter consists of four switches whereas a half bridge inverter needs two switches as the name suggests. The switches in a half bridge inverter are connected in antiparallel along with two diodes and in a complementary manner. This indicates that when one switch is ON, the other is OFF and vice versa. Figure 2.1 shows the basic circuit diagram of a half bridge inverter.

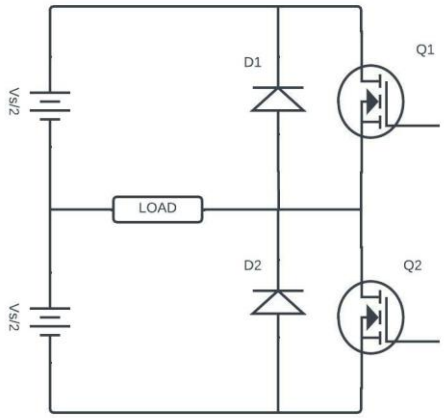

Figure 2.1: Half bridge inverter design

Operation of a half bridge inverter in detail:

Single phase half bridge inverter is a type of voltage source inverter (VSI: constant voltage source divided as VDC+ and VDC-). The input is a DC voltage source and output is single phase where single phase power means a two-wire alternating current power circuit. Hence the name, single phase inverter. The working principle of the half bridge inverter is such that, in the first half cycle, one switch conducts and for the other half cycle second switch conducts. Thus, the switches turn on and turn off in alternative half cycles. The frequency of the output is dependent on how duty cycle of the PWM signal applied to the switches for their switching is controlled. The operation of half bridge inverter with resistive load is discussed for understanding the operation. Input and output waveforms as shown in Figure 2.2 as per the switching pattern.

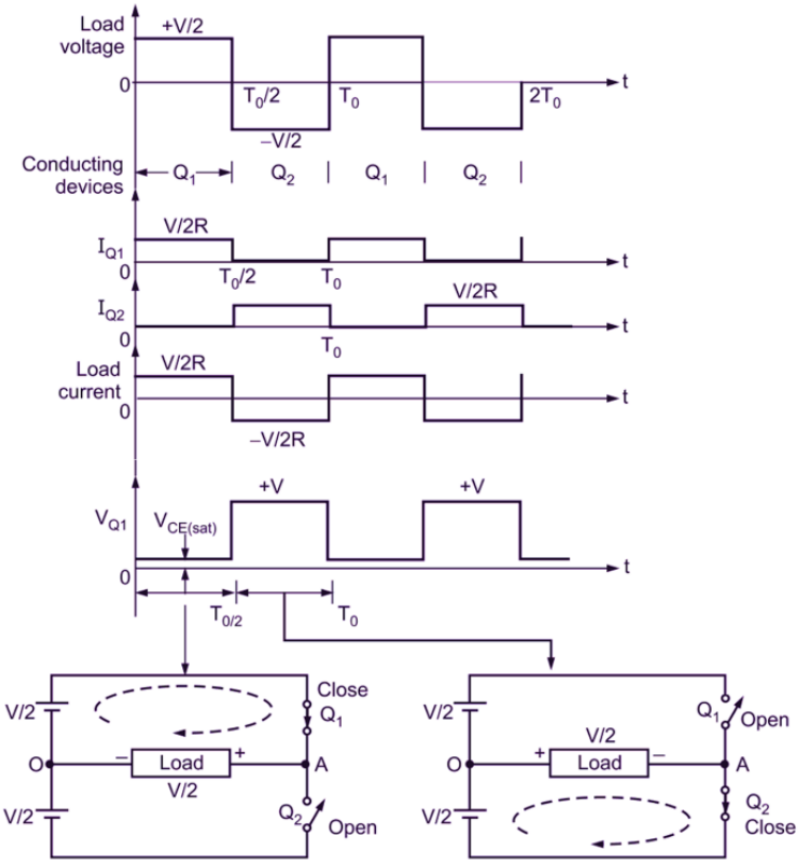

Figure 2.2: Operation of half bridge inverter with resistive load

Case 1. Top switch is ON and bottom switch is OFF

Q1 is turned on for time To/2. This makes voltage V/2 appear across the load, here resistance R. Thus, the value of output voltage is given as Vo=V/2. Q2 remains off during this time period.

Case 2. Top switch is OFF and bottom switch is ON

When bottom switch Q2 is turned on from To/2 to To and Q1 is off, voltage -V/2 appears across the load resistance R.

The amount of load current flowing can be determined by following:

Output current = V/2R [11]

2.1 Hardware requirements

Before proceeding to design of the half bridge inverter, it is important to define the design requirements. The requirements have limitations depending

on the operation and dimensions of the electronic components. Table 2.1 shows the requirements for design of the hardware.

Table 2.1: Design Requirements

Input voltage	0-60 Vdc
Frequency	100 kHz
Power delivered	12 W

The aim is such that the half bridge inverter should have low switching losses, high efficiency, high power density, thermal stability, and reliability. This can be quantified by measuring the switching transients of the switch during its operation and the amount of common mode noise is created by the switching transients. The control scheme for the inverter is mainly UP-PWM scheme. Advantages of using PWM scheme is that there is no need of external components. There are no low order harmonics and high order harmonics can be eliminated using a low pass filter.

2.2 Selection of Components

Selection of most of the components is primarily dependent on the switching frequency. Higher the switching frequency, lower the size of the components, such as, capacitors, and inductors. Thus, the size of peripheral components is reduced in such a way that the power density and efficiency become higher, significantly reducing the conduction losses. However, this comes with drawbacks such as, increase in the miller effect and EMI. Thus, these are the main problems faced by high frequency power converters.

2.2.1 Gallium Nitride HEMT power devices

Compared to Silicon (Si) based power switches, devices based on wide band gap material such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are able to provide a higher switching speed and lower power losses. GaN and SiC based switching devices are superior to the Si based devices based on their low loss and efficient performance at high temperature. Thus, the need for cooling is comparatively reduced whereas the power density is increased. Brief comparison of Si, SiC and GaN is given in Table 2.2 [12].

Table 2.2: Comparison of Si, SiC and GaN

Parameter	Impact	GaN	Si	SiC
Qg (nC)	Switching	5.8	64	30
Coss (pF)	speed and	64	48	60

Tdelay(on)/tdelay(off) (ns)	switching frequency	4.1/8.0	7/72	9/16
t_rise/t_fall (ns)		3.7/5.2	14/7	10/6
Eon/Eoff (μJ)	Efficiency	47.5/8		39/17
Eoss (μJ)		8	8	16
Qrr (μC)		0	10	131
trr (ns)		0	800	16

Selection of GaN over SiC and Si based components can be understood by observing Figure 2.3. It can be seen that the GaN based components have better performance over SiC and Si based components in applications where the compared parameters play an important role.

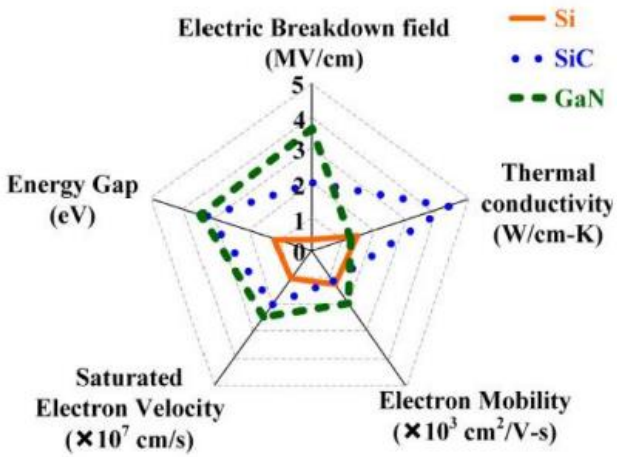

Figure 2.3: Properties of GaN compared to Si and SiC

GaN device package has significant improvement as compared to TO220 package since the latter can add parasitic inductance significantly. It is important to reduce parasitic inductance in gate loop and power loop as much as possible. This is possible with kelvin connection. The GaN switches have almost negligible reverse recovery losses. The reverse recovery current causes a high switching transient that can cause EMI issues. The part number of the device manufactured by GaN systems is GS66508T. It has zero reverse recovery charge, very small gate charge and has applications at very high frequencies around 10 MHz. GaN HEMT's with parameters are selected as per given in Table 2.3.

Table 2.3: Parameters of selected of GaN HEMT

Parameter	Value
V_{DS}, max	$650\ V$
I_D, max	$30\ A$

Characteristics of GaN

- Reverse conduction behaviour
  GaN HEMT does not have a build-in body diode due to the lateral structure. In addition to this, there is no reverse recovery charge. The device is capable of reverse conduction, even in the absence of a body diode. The reverse conduction characteristics is a function of gate to drain bias. The transistor starts to conduct in reverse direction when V_{GD} exceeds the gate threshold voltage. Plot of IV characteristics [13] of GaN HEMT is shown in Figure 2.4:

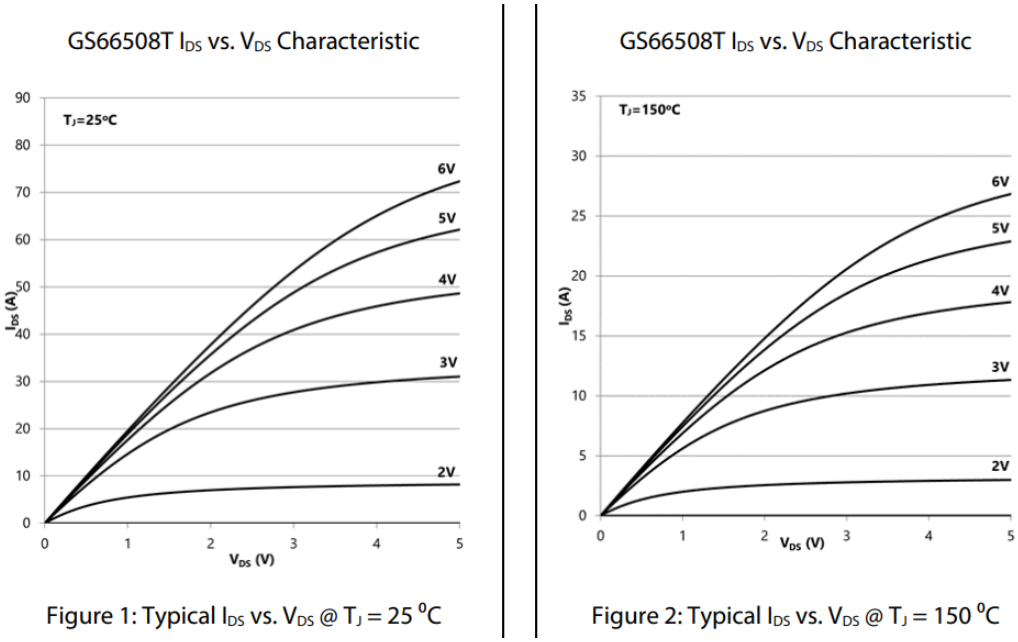

Figure 1: Typical I_{DS} vs. V_{DS} @ T_J = 25 °C

Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 °C

Figure 2.4: IV characteristics of GaN HEMT

- $R_{DS}(ON)$ (Dynamic on resistance)
  It is important to consider the dynamic characteristics of the on resistance of GaN HEMT in high power applications at high frequency. A double-pulse test which is used for characterization of semiconductor switching dynamics, can be used for hard-switching robustness and dynamic $R_{DS}(ON)$) degradation testing of GaN semiconductors. An increase in $R_{DS}(ON)$ can reduce efficiency causing thermal runaway. Thus, stable dynamic $R_{DS}(ON)$ and robustness of GaN devices can be tested under accelerated conditions using double-pulse test to detect poor performance [14]. Significant efforts are being taken to reduce the value of dynamic on resistance of GaN HEMT.

- Intrinsic capacitance

GaN transistors have an input capacitance (C_{ISS}) of about 30 times lower than Si MOSFETs. The small CISS of GaN HEMTs and small Qg lower the gate driver loss while reducing the delay time [14].

- Use of negative $V_{GS}(OFF)$
  Use of negative gate bias voltage increases the noise immunity and reduces the switch off losses under high current operating conditions.

2.2.2 Gate driver selection

Any standard gate driver can be used to operate GaN HEMT as long as it is capable to provide required gate drive voltage over its operating range. In order to have optimum performance, the gate driver should have following characteristics:

• Low inductance, small surface mount package

• Low output pulldown (sink) impedance, 2 Ω or less

• Peak output current of at least 4 A

While considering a high side gate driver, care should be taken for undervoltage lockout threshold and gate voltage regulation for GaN e-HEMT [15]. Features of existing driver is that the gate driver IC provides the required isolation between low power and high-power levels on the board. PCB layout also plays an important role where traces and ground planes under the isolator device can cause stray capacitance on the board. Gate drivers having low impedance and high peak current are preferable in case of high switching speed applications. Selection of the gate driver is such that it is used to ensure fast rise time of switches. If the gate driver is used for the control of slew rate, it is better to use separate turn on and turn off gate resistors. This will help in reducing the impedance at the gate. The turn on speed can be optimized to limit the voltage transients. The gate signals for the switches are referenced to a source. The gate driver being able to follow this source, provides isolation between the source, control signal i.e., control side and output side of the gate driver. Level shifter to operate high side MOSFET gate or bootstrap mode are used to provide voltage levels +6V and -4V for ON and OFF respectively. The latter value is selected to avoid the false turn-on of the transistor when the other transistor in the phase leg turns-on due to the miller effect [16] [17]. If there is excessive impedance in the gate loop, gate voltage can increase above its rated value which can cause excessive ringing at the gate. To reduce the gate loop inductance, the gate driver should be places as close as possible to the gate of the switch. The gate driver should have low gate voltage ratings so that is it compatible to use with any GaN HEMT device having lower gate voltage ratings. As the GaN HEMT have lower gate capacitance, the gate

driver can be used with a higher value of external gate resistance. This will significantly reduce the power loss the gate since the gate voltage is very small.

2.2.3 Capacitors

Different types of capacitors are available for their application in any power converter design. They are namely electrolytic, ceramic and film capacitors. The electrolytic capacitors have large capacitance to size ratio but they also have high ESR and ESL. Electrolytic capacitors are polar and cylindrical in shape. They can be used to reduce voltage ripple at low frequency. One of the disadvantages of these capacitors is that there are chances of leakage when they are under any overstress condition such as, high reverse voltage conditions. Ceramic capacitors have small capacitance values but they also have very small ESR and ESL. Thus, they have very high ripple current supply capacity. They are nonpolar and often available in SMD package. In overstress conditions, the SMD package body develops a crack. Film capacitors have a wide range of frequency for their application and have lower ESR and ESL. Thus, they are most commonly used in high frequency power applications. They are nonpolar and available in bulky sized cuboidal shape structure. Under overstress conditions, they are degraded and cause either open circuit or short circuit failure.

2.2.4 Inductor

An inductor can be directly used from available catalogues or it can be made by wire winding as per the requirements. The rated current should be such that it is able to sustain the load current with proper margin. An inductor with sufficiently high rated DC current rating is usually selected in order to avoid any losses from heating. Moreover, an inductor with a low DC resistance and self-resonating frequency much higher than the operating frequency is preferred.

2.2.5 Hard switching

The switching of the switching devices results into switching losses and electromagnetic interference EMI. If the switching frequency or switching speed is changed, either of the switching losses or EMI is changed in an acceptable behavior. Thus, it depends on the application whether to change the switching speed or switching frequency in order to reduce either switching losses or

EMI noise. Thus, there is a tradeoff between switching losses, thereby power losses and EMI. There is a need to quantify these two based on different parameters. Apart from the switch characteristics, there are other parameters which are responsible for switching losses and EMI such as, parasitic elements in the PCB layout or parasitic elements emerging from the DC link capacitors (Capacitors connected to GND path which give path for common mode noise or leakage current) and also capacitors in the devices. These parasitic elements are needed to be determined and addressed so that, the problems cause by EMI noise can be mitigated. Probable parasitic elements in the power module are DC link capacitors, poor PCB layout, thermal performance, PWM connections from external DSP module, and inductance of the power loop and gate loop of the switch. As the switching frequency increases, especially in case of WBG devices, the EMI noise occurred by these parasitic elements increases.

2.2.6 Driver power supply design

The gate drivers are provided power using an isolated power supply. It is a simple dc-dc converter which takes 9 V to 12 V input from a DC power supply. This 12 V is then converted into 5 V to provide supply to some of the devices in the circuit. Again, this 5 V is converted into isolated +10 V DC. A dual power supply circuit then divides this 10 V into positive bias +6 V and negative bias -4 V with the use of 6 V zener diode. This is then used for the gate bias voltage (VDD and VEE respectively) to turn on and turn off the switch respectively. Such bipolar gate power supply makes the gate driver design more robust and increases the noise immunity. The ability to remove the freewheeling diodes in converters is among the advantages of GaN in these components.

2.2.7 PWM dead time

The purpose of the dead time is to make sure that both the high side and low side switches are not ON simultaneously. Therefore, the deadtime should be set in such a way that it is sufficient for high side switch to turn off completely before the low side switch is turned on with some margin and vice versa. Deadtime of about 10 ns can be inserted which is by default in case of the evaluation board that will be used for testing.

2.2.8 Behaviour of on gate resistance

Turn on gate resistance is responsible for controlling the dv/dt slew rate of turn on instance. Higher the turn on gate resistance, higher the switching losses, since it slows down the switching. If the gate resistance is very small,

the device becomes prone under the influence of miller effect to severe gate oscillations resulting in EMI. Separate gate resistance for turn on and turn off in the gate loop is recommended. It is important to focus on *Rgon/Rgoff* ratio in order to achieve desired results of the gate driver performance and its stability. A separate turn off resistance provides a strong and fast pull down for robust gate drive. Lower turn off resistor ensures better immunity to cross conduction. Selection of right gate resistance is necessary to mitigate the gate ringing problems. Other ways to avoid gate ringing are use of ferrite bead and RC snubber.

2.3 Double pulse testing

Double pulse testing (DPT) is a test method used to investigate the performance of the gate driver and the switching performance of GaN HEMT. It is performed to measure the turn on and turn off parameters of a switch. The timing parameters of rising edge and falling edge are observed in this case. Based on these and with mathematical calculations, the energy losses can be calculated. Thus, double pulse test is carried out in order to ensure the proper switching behavior of the switch. GaN HEMTs have very low gate-source transient voltage tolerance. Therefore, a high gate drive loop inductance can generate high voltage spikes which could destroy the device severely. This can be avoided by increasing the gate drive resistance but that will ultimately reduce the turn-on speed of the switch and hence increase the switching losses. In a half bridge configuration, power loop parasitic inductance along with output capacitance of the switch can cause high voltage overshoots across the top switch during the time when bottom switch turns on. Switching losses can be reduced by faster turn on and turn off times but it increases the high frequency noise. As WBG devices are known for their ultra-high switching speeds, care should be taken when they are operated at their maximum switching speeds as it will create high frequency noise or ringing at the gate of the switch.

To determine the switching states, switching times and switching losses of a switch, configuration of the half bridge circuit is as Figure 2.5 [18].

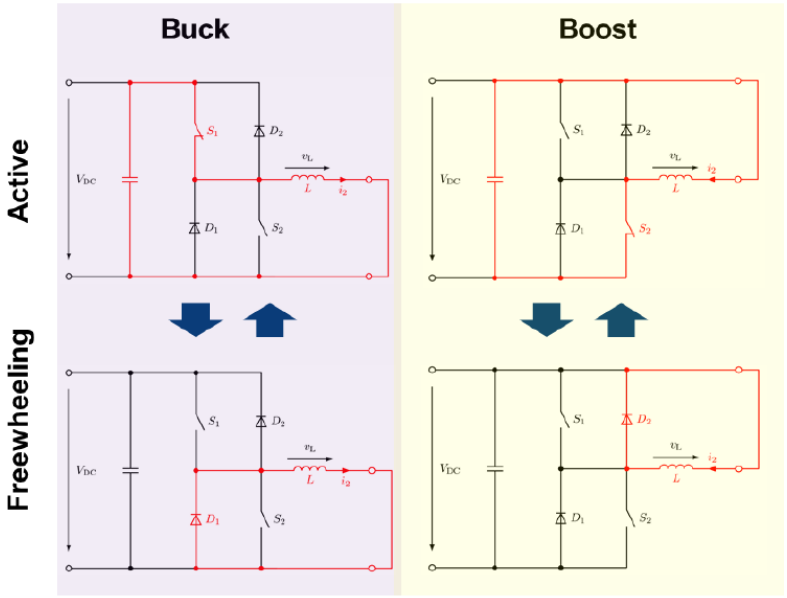

Figure 2.5: Overview of double pulse test circuit configuration of the half bridge circuit in buck and boost mode

Flowchart for double pulse test is shown in the Figure 2.6 [19].

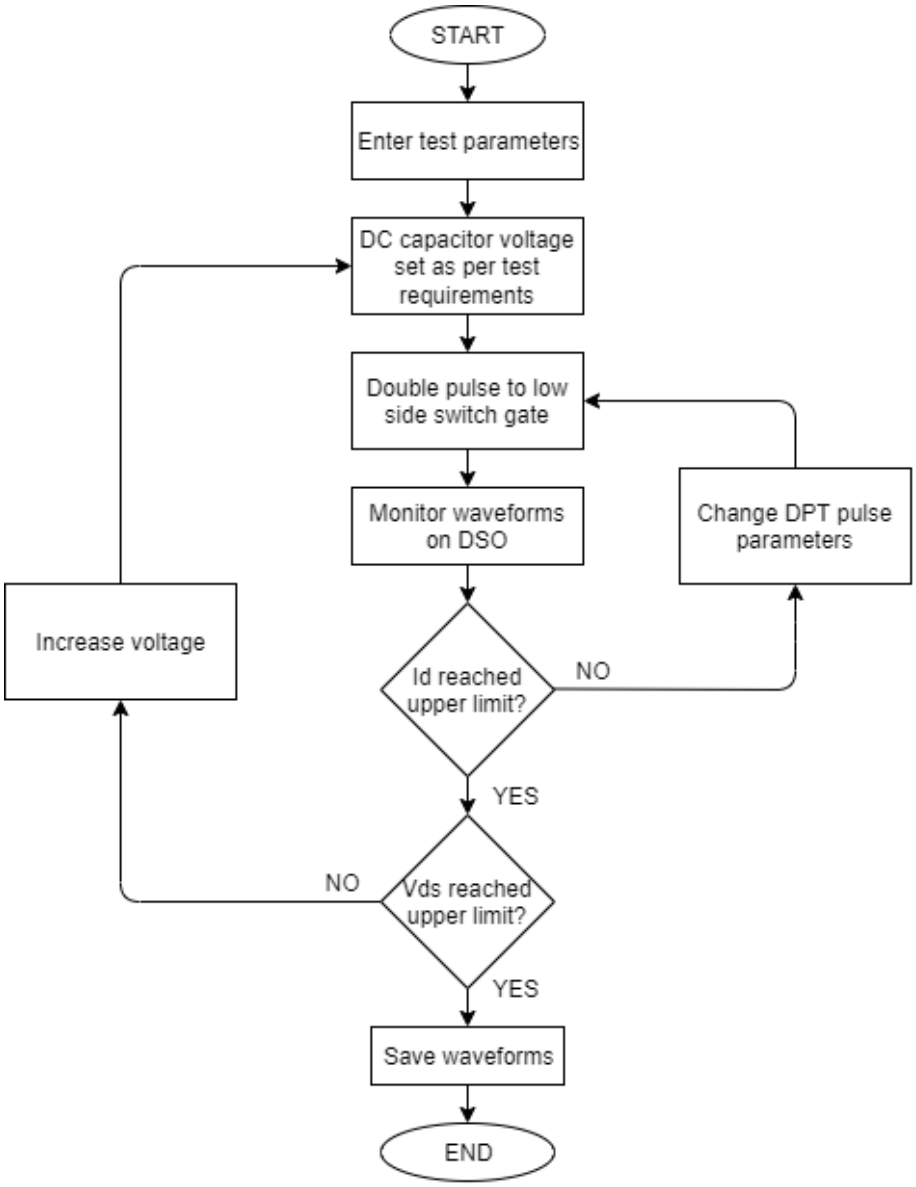

Figure 2.6: Flow diagram for double pulse test

Need for a capacitor bank?

As the test current increases, the need for a capacitor bank increases even up to μF or mF. The capacitor bank should be such that it has very low parasitic inductance. For capacitors selection refer previous chapter 2.2.3. In order to reduce parasitic inductance, it is beneficial to use many capacitors in parallel connection configuration as shown in Figure 2.7 instead of using a single high value bulky capacitor.

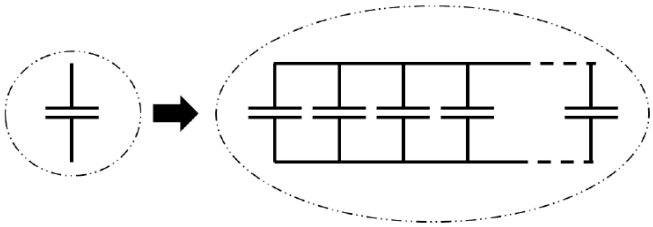

Figure 2.7: Representation of using parallel capacitors bank

Capacitor bank design criteria is given in the equation (2.1):

$$C_{DC} = \frac{L \cdot I_{test}^2}{\Delta V^2} \tag{2.1}$$

Voltage and current measurement

The aim is to measure both voltage and current in order to measure the switching characteristics. It is challenging to measure the comparatively larger values of switching transients dV/dt and dI/dt. Therefore, it is important to select the measuring probes such that they have higher bandwidth and wide range for the measurement of rising and falling edge of the switching waveforms. Similarly, measuring common mode voltages of small value is also very critical. For measurement of common mode voltage and current, a measurement probe with common mode rejection ratio (CMRR) is required. Passive probes can also be used to measure the less sensitive voltages and currents on the high side. Active probes need the calibration in order to measure the small parasitic sensitive currents and voltages. Measurement loops for such measurement probes should be as small as possible. Twisted leads of the differential measuring probes can minimize the unintended noise coupling.

2.4 EMI and Common mode noise

Fast switching of the switch creates issue of potential high frequency noise or electromagnetic interference. Parasitic elements in the switch gate loop and power loop are responsible for the cause of EMI. GaN devices have very low total gate charge Q_g therefore they have higher turn on and turn off transition speed [10]. Even though they can create higher EMI as compared to Si based devices, there is still reduction in the switching losses. Literature related to the research based on the EMI characteristics of GaN devices is comparatively less, therefore, it is required to investigate the EMI characteristics more [20]. A line impedance stabilization network (LISN) [21] is used to measure the common mode noise. It is connected in between the DC power source and the device under test (DUT). The switching devices are considered to be connected to heat sink. As the LISN is grounded, a parasitic capacitance is formed between the ground and the switch node that provides the main path

for common mode current to flow. Common mode noise propagation path is as shown in Figure 2.8 [22].

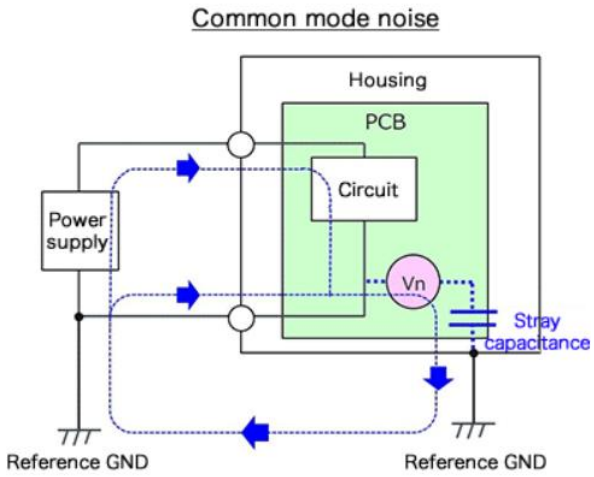

Figure 2.8: Common mode noise propagation path

Common mode noise caused due to *dV/dt* can cause malfunctioning of the control circuits. EMI should be mitigated in such a way that the power density and efficiency of the design are not compromised.

3. Hardware Design

Considering the design requirements discussed in previous chapter, hardware design is followed. The steps included are circuit design, circuit simulation, PCB layout design considering all the necessary standard design guidelines. The simulations give an idea of how the hardware prototype will behave with the similar components.

3.1 Circuit Design

The components required are selected based on the design requirements as discussed. The datasheet of each component, especially the switches and the gate driver provide an idea of how to select the peripheral components. The design also includes connectors for power supply and control PWM signals of appropriate rating so as to provide the required current and voltage without any drop. Gate driver for each high side switch and low side switch is considered in this case since this is a synchronous converter. The gate driver circuit includes driver IC along with its peripherals such as external gate resistance for both turn on and turn off and turn on diode. Protection devices such as, ferrite bead and RC snubber are also considered in design for further mitigations of the problems if any. There are DC link capacitors across the VDC and GND that help to eliminate the low frequency ripple and high frequency noise. The circuit schematic for design of a half bridge inverter is shown in Figure 3.1.

Circuit Schematic

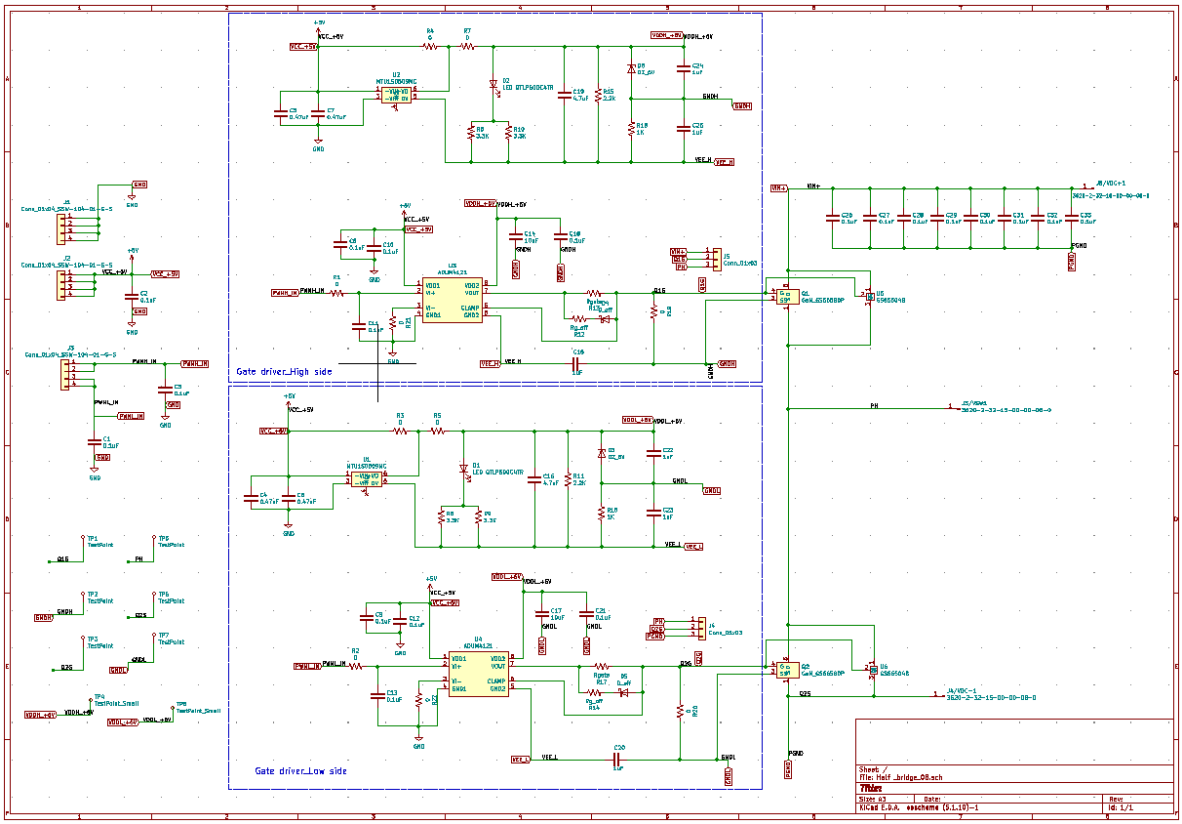

Figure 3.1: Circuit Schematic for half bridge inverter

Schematic components mainly used for the design are as per Table

Table 3.1: Main components used for circuit design

Sr No	Component part number	Description of the part
1	Gate driver IC ADUM4121	Single switch, isolated with internal miller clamp
2	GS-065-030-2-L	GaN MOSFETs Bottom cooled, V_{DS}=650 V, I_D =30 A
3	GS66504B	GaN MOSFETs Bottom cooled, V_{DS}=650 V, I_D =15 A
4	Dual output DC-DC converter MTU1S0509MC	+6 V, -4 V dual output at 100 kHz

Initial idea was to incorporate two GaN HEMTs having different current ratings in order to study their respective switching loss behaviour and response to change in various parameters, such as external gate resistance, and effect of addition of RC snubber.

A 12 V power supply is used to provide power to the circuit. A simple dc-dc converter is used to convert 12 V DC to 5 V which is used for other logic circuits in the circuit. This 5 V is then converted into +10 V which then is divided into bipolar power supply of +6 V and – 4 V using 6 V Zener diode. A 0 V to 400 V DC power supply is needed to supply the required DC bus voltage. The input PWM signal is provided by a microcontroller which generated the PWM signal using MATLAB Simulink. The PWM signal can also be directly given to the circuit by using a programmable signal generator. The inductor can be connected to either positive DC bus or the negative DC bus for inverter double pulse where the high side switch is active and low side is freewheeling synchronous rectifier [23]. A general example of double pulse test on half bridge inverter is shown in Figure 3.2.

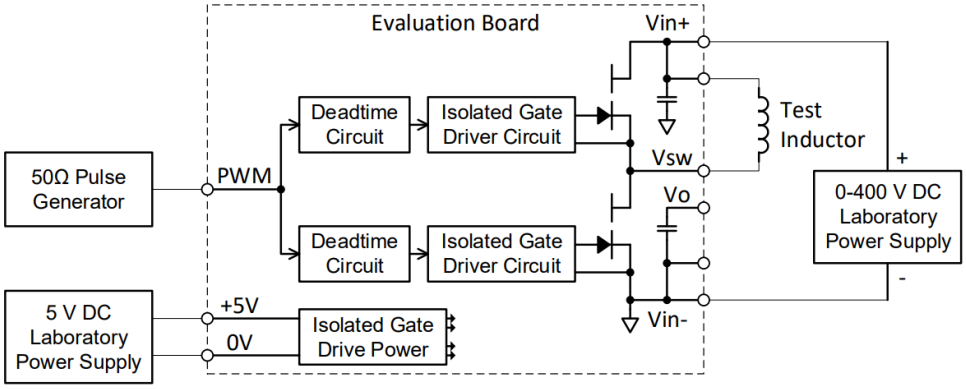

Figure 3.2: Typical example of double pulse test on half bridge inverter

3.2 PCB design

PCB design is an inclusive part of any power electronic system design. The main objective to design a PCB is to reduce the required number of connections/wirings, use of optimum space and size, to decrease the stray inductances and EMI caused due to the former. Thus, PCB design represents more of a practical design regarding any power electronics circuit. The PCB design can be done in various software such as Altium, KiCad, Eagle etc. While designing a PCB, there are many layout considerations that are needed to be taken care of. There are certain IPC standards according to which the PCB layout is done.

The PCB layout for the prototype is built in software called KiCad. The basis of the initial PCB assembly is that it is divided into two parts: Primary side voltage with the driver circuitry, and the control circuit and other part with the switches, capacitors and high side voltage. This acts as a universal half bridge-based topology board. The Figure 3.3 shows the PCB layout of the half bridge inverter circuit. The arrangement is such that the inductor to be

connected externally for double pulse test will be connected between VDC+ and VSW. The provision for this is given on the board. This is a four-layer board where majority of the components are on the top side of the board. The second layer is for GND, third layer is for POWER and then the fourth layer is again bottom copper layer. Thus, GND and POWER layers provide all the copper completely dedicated to different ground and power respectively needed for the high voltage side, low voltage side and for control circuits. There are provisions of test points for various measurements to be taken. Additional components such as required for RC snubber and ferrite beads are also provided with additional footprints.

The low side power signals including 5 V, PWM signals are given from one side of the PCB and high side DC voltage is given from the other side. All these signals are on the top side of the PCB. Therefore, ground and power signal are given separate copper layer so that parasitic inductance is reduced. Also, it reduces the need of additional routing and jumpers in the design. It can be seen that the bottom side of the PCB does not have any components placing. Instead, there is exposed copper alongside the MOSFET bottom side so that in case of overheating, a heatsink can be attached to avoid the damage to the components. This in turn has caused the PCB size to increase more than its optimum size.

It can be seen that there is provision to place two different footprints of the MOSFET which are namely GS66580P and GS66504B both having bottom side cooling. The footprint for GS66580P has 4 pads including one extra pad for source sense SS pin whereas GS66504B has 3 pads. Therefore, these two footprints are incorporated in such a way that the common pads coincide with each other without having to compromise with the layout considerations of the MOSFETs. This enables user to have the flexibility to use the same board for MOSFETs with two different ratings for various purposes. All the layout considerations such as critical loop paths like power loop and gate driver loop are kept as short as possible. The parasitic inductance is taken care of by keeping proper clearance between the copper areas dedicated for various signals and the width of the copper traces is kept sufficient enough for the amount of rated current flowing. All these clearances [24] are compliant to the standard IPC2221 [25] with the intention to reduce the possibility of electrical breakdown, reduce the parasitic inductances and capacitance and simplify the PCB assembly by giving fundamental thumb rules.

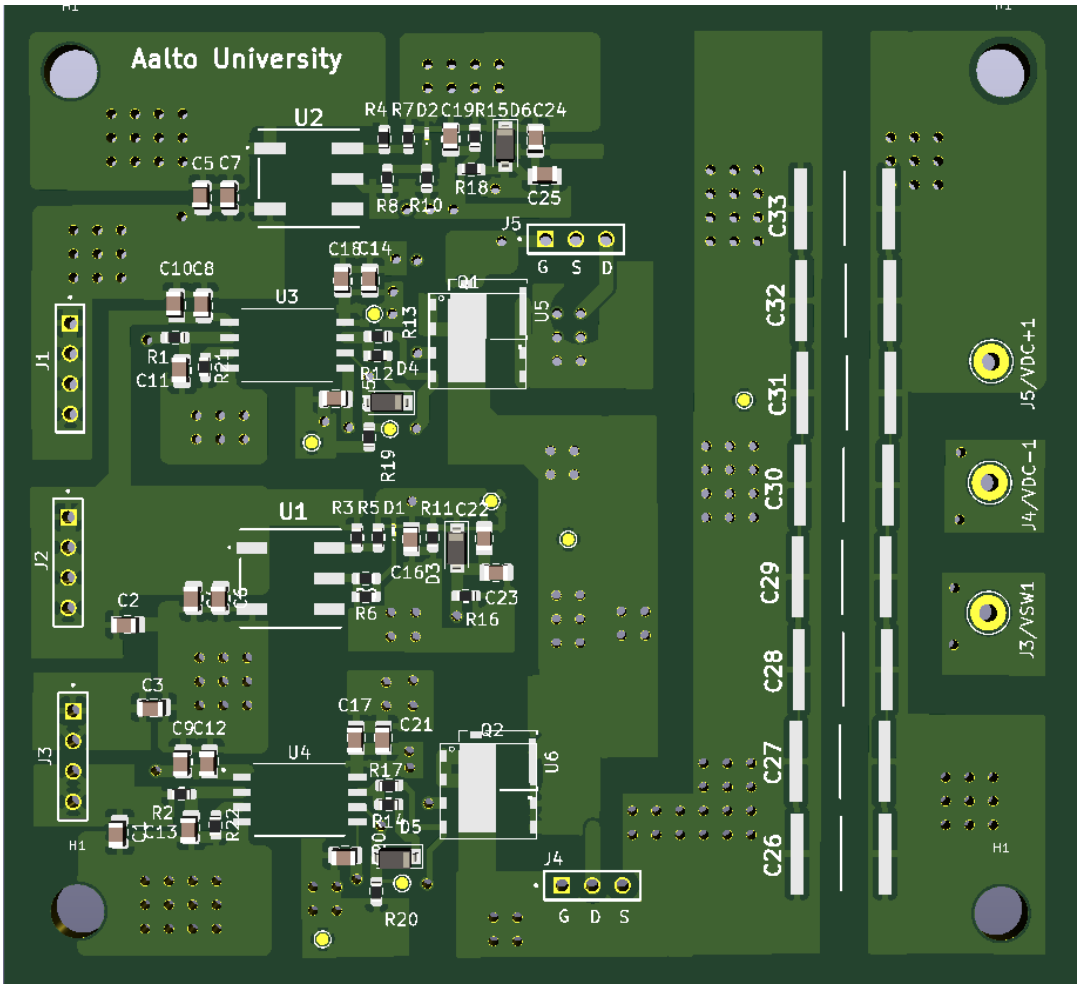

Figure 3.3: PCB design for half bridge inverter

The PCB designed as shown in Figure 3.3 was based on the GaN systems half bridge inverter evaluation board with same switches to replicate the resemblance of any probable avoidance of the switching losses and EMI. Recommendations from the manufacturer while designing the gate driver were also considered. Since the enhancement mode GaN HEMT are known for their ultra-fast switching capabilities, the gate driver design needs to be critical. The voltage rating of the gate terminal also needs to be taken care of by the gate driver where the gate turn-on voltage = +6V and turn-off voltage= -4V.

3.3 Use of evaluation board

The design considerations while designing the PCB for half bridge have some limitations. For example, even if all the design parameters in a PCB are as per the requirements, there is a possibility that the design may fail due to EMI. It might take a few iterations of the PCB layout design to reduce the EMI caused due to parasitic in the PCB created by poor design. In order to have

the best possible results for the switching losses and the noise measurements, an evaluation board of similar design has been used to avoid any undesirable delay in obtaining the results. The results obtained from the original PCB designed and the evaluation board can further be compared in future to study the impact of how change in layout design and few PCB design parameters can affect the performance of the design. Also, the evaluation board can also be used as an ideal design for PCB layout as well as the component selection. Based on the results obtained from evaluation board, further improvements can also be done in the previous PCB designed.

GS66508T-EVBDB2 GaN E-HEMT Daughter Board and GS665MB-EVB Evaluation Platform

GS66508T-EVBDB2 GaN E-HEMT Daughter Board consists of all necessary circuits including half bridge gate drivers, isolated power supplies, heat sink to form a functional half bridge driver stage. In this way, the performance of GaN E-HEMT can be easily evaluated. This board can be used as a reference design for any half bridge-based topology. The features of the board for its use as an evaluation tool are shows as per Table .

Table 3.2: Electrical characteristics of GaN HEMT GS66508T

Voltage rating	650 V
Current rating I_D (continuous)	30 A
On state resistance $R_{DS}(ON)$	50 mohm Tj=25˚C
Total gate charge $Q_g(total)$	5.8 nC
Gate to source charge Q_{GS}	2.2 nC
Gate to drain charge Q_{GD}	1.8 nC
Thermal resistance junction to case $R_{\theta jc}$	0.5 C/W

Features of the board

It has a 12 V input for power and an onboard voltage regulator that generates 5 V for the control logic circuits. There is also a provision for external DC fan connection. The PWM inputs for top and bottom switch can be controlled separately. The board has its own dead time generation circuit which can be used when the top and bottom switches are operated as complementary pair. Power connections are mostly screw mounted in this case for high volt DC power supply connections and external inductor [13]. External inductor is a power inductor chosen in such a way that it has low interwinding capacitance to achieve the optimum switching performance.

4. Hardware testing

This chapter discusses the hardware testing on the evaluation board. Results obtained from these tests are discussed in detail. Initially, while testing on the evaluation board, few failures related to the GaN HEMTs occurred as the input DC voltage was increased. This was mitigated by conducting the tests at lower voltages without any compromise with the results.

4.1 Double pulse test setup

Block diagram for a standard double pulse test is depicted in Figure 4.1. It is followed by the picture of the actual hardware setup used for testing.

Equipment required for double pulse testing are given as below and also listed in Table B.1

1. Device Under Test DUT
2. DC Power supply: High voltage power supply and power supply for gate driver circuit
3. Load inductor
4. Digital Storage Oscilloscope (DSO)
5. Measuring sensors for current
6. Measurement probes for voltage
7. Microcontroller and PC to generate PWM
8. Spectrum analyser
9. LISN

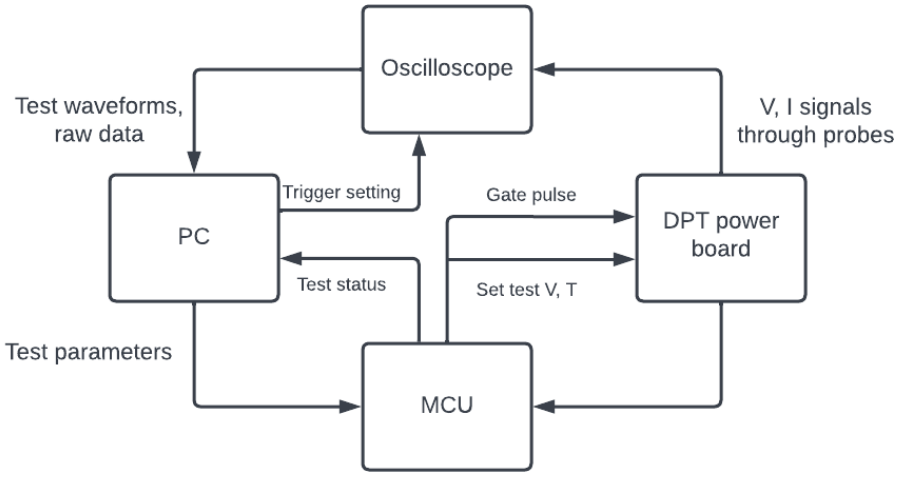

Figure 4.1: Block diagram for double pulse test

Basic setup is done as shown in Figure 4.2:

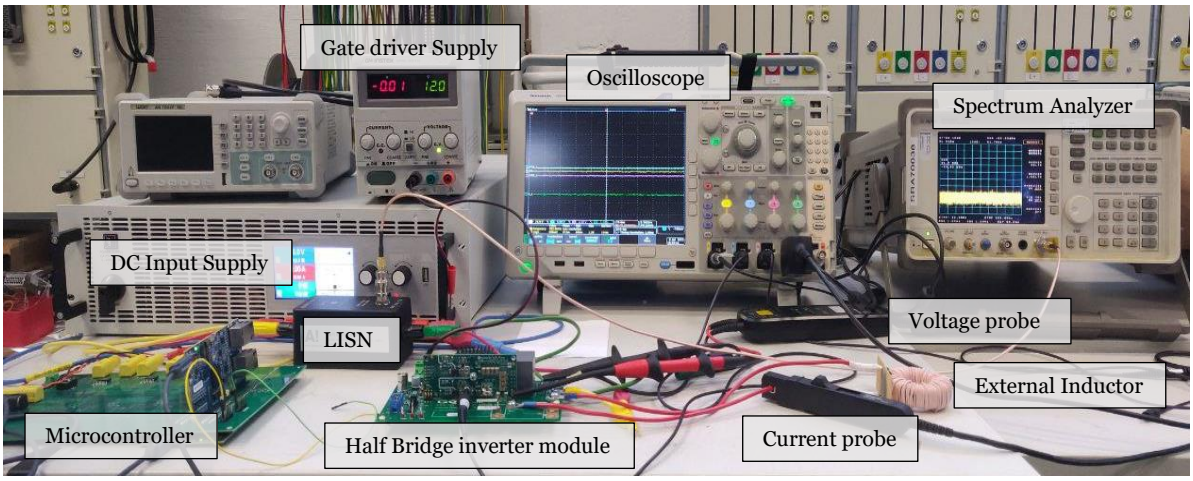

Figure 4.2: Hardware setup for double pulse test in laboratory

The required equipment along with the evaluation board and microcontroller module [26] for generation of PWM pulses is shown in Figure 4.2.

4.2 Test procedure

Creation of double pulse waveform

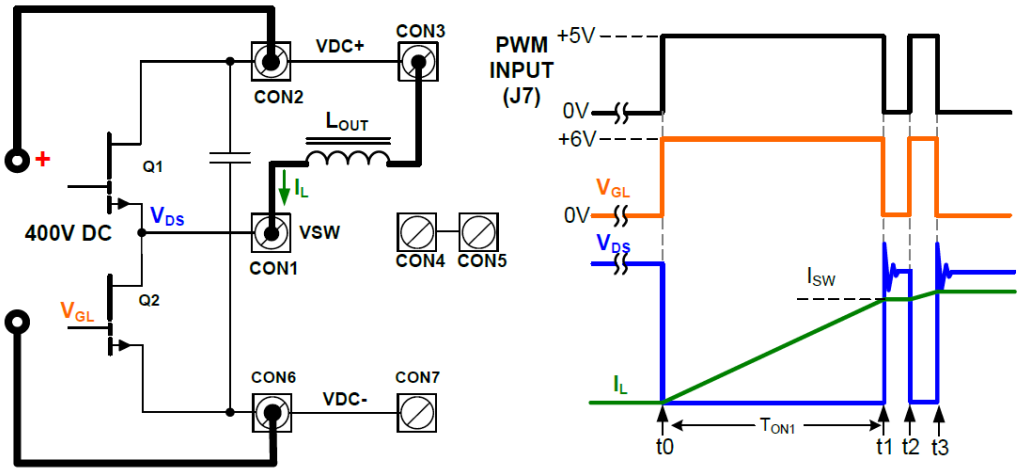

Figure 4.3: Creation of double pulse test waveform

There are three phases of the double pulse waveform depicted in Figure 4.3 [13]. The pulse sequence is such that the first pulse is of duration Ton1, then there is pulse break from t1 to t2 and second pulse with duration t2 to t3. The

durations are calculated and fed to the signal generator for the creation of the desired pulse sequence. The pulses can also be created by using a microcontroller and the step-by-step implementation of creating the pulses using Simulink is given in Appendix A.

The first pulse duration is calculated such that the DUT reaches the desired test current. During the pulse break, the DUT is turned off so that the current starts flowing through the freewheeling diode. Due to the parasitic series resistor, the inductor current drops slightly. The duration of the first pulse is significantly longer than the pulse break. Once the second pulse starts, the inductor current starts to rise again. The duration of second pulse is such that the current does not suddenly reach very high value beyond the limits. Still, the peak overshoot observed is due to the reverse recovery of the freewheeling diode. Hence, the turn on and turn off events of the DUT are observed over the entire duration of the double pulse waveform.

4.3 LT spice simulation for double pulse test

LTspice simulation for double pulse test on standard half bridge inverter setup acts as a means to confirm the desired behaviour of the design and identify any possible failures in the design. Simulation is beneficial because it helps to understand the working of the design and it can predict any failure that may occur in the actual hardware. The modelling of the parasitic elements in the design can be simplified in the simulation and their response at different operating conditions can be observed. Thus, the circuit is simulated in LTspice software. The spice models of all the components are either available in the LTspice libraries or from the component manufacture website.

Switching times:

td(on): turn on delay, tr: rise time, td(off): turn off delay time, tf: fall time can be understood as depicted in Figure 4.4 [27].

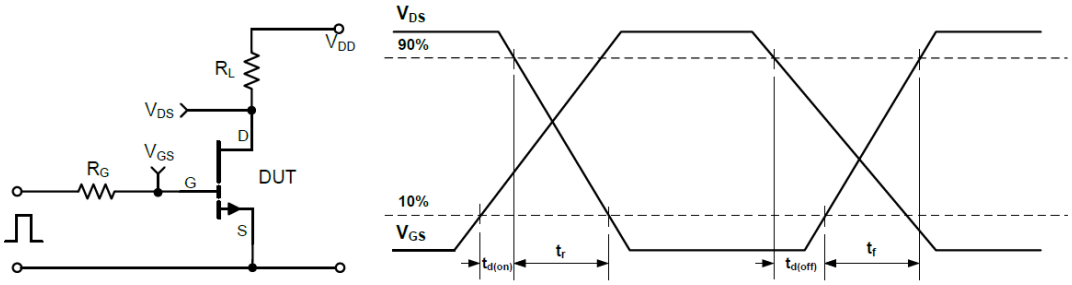

Figure 4.4: GS66508T switching time test circuit and waveforms

Switching energy

The switching energy can be calculated from the measured switching waveform with following equation (4.1)

$$P_{sw} = V_{ds} \cdot I_d \tag{4.1}$$

Thus, the integral of P_{sw} during switching period is the measured switching loss.

Figure 4.5 shows the LTspice circuit for double pulse test in a half bridge inverter.

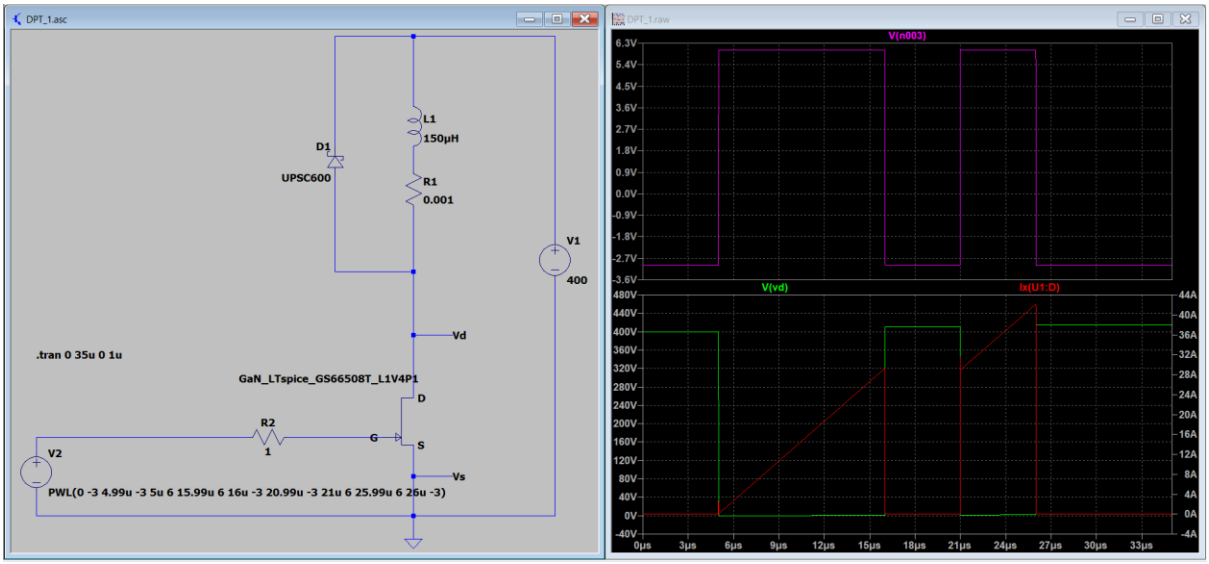

Figure 4.5: LTspice circuit of DPT on a half bridge inverter without gate driver

Turn off measurement instance captured in Figure 4.6 and turn off energy measurement in Figure 4.7.

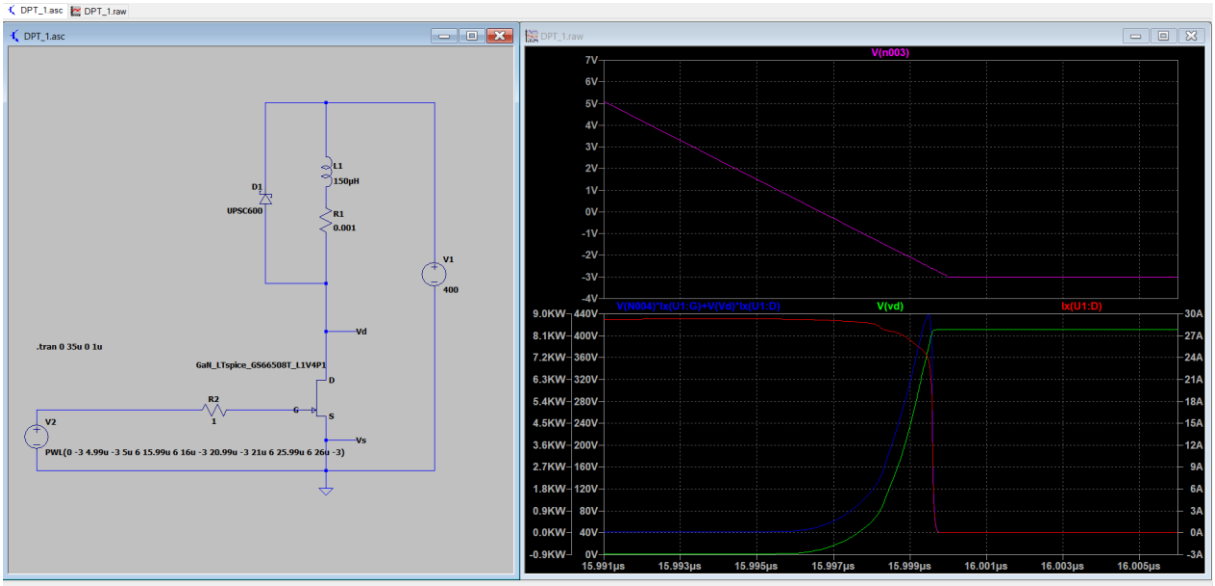

Figure 4.6: Turn off instance of the switch

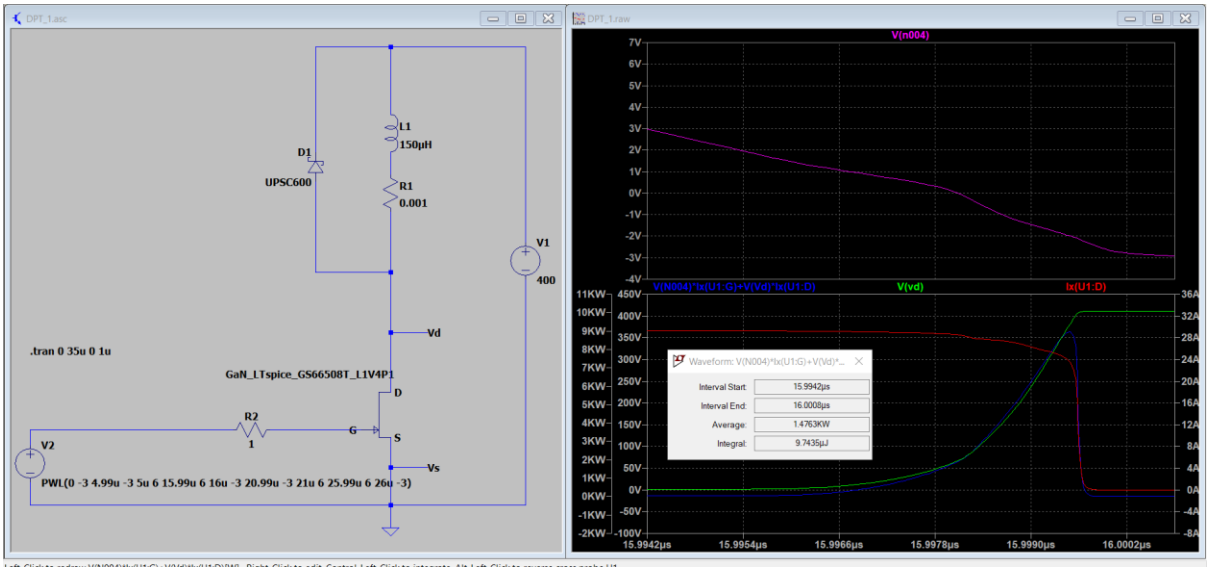

Figure 4.7: Turn off energy of the switch

During turn off event, initially, the input capacitance starts discharging. This input capacitance is in parallel connection with the gate to source capacitance C_{GS} and gate to drain capacitance C_{GD}. As a result, the gate to source voltage V_{GS} starts decreasing and the drain to source voltage V_{DS} starts increasing. Drain current I_D remains constant throughout the miller plateau. As the drain to source voltage V_{DS} reaches the DC voltage value, the drain current I_D starts decreasing. Then, as the gate to source voltage V_{GS} is further decreasing and reaches the off state, the drain current I_D and drain to source voltage V_{DS}

reach the off state. Further, the measurement parameters for turn off event in simulation and in the datasheet is compared in Table 4.1.

Table 4.1: Measurement parameters for turn off event

Turn off time in simulation	4.1 ns
Turn off time as per datasheet	5.2 ns

Turn on measurement instance is shown in Figure 4.8 and turn on energy measurement is given in Figure 4.9.

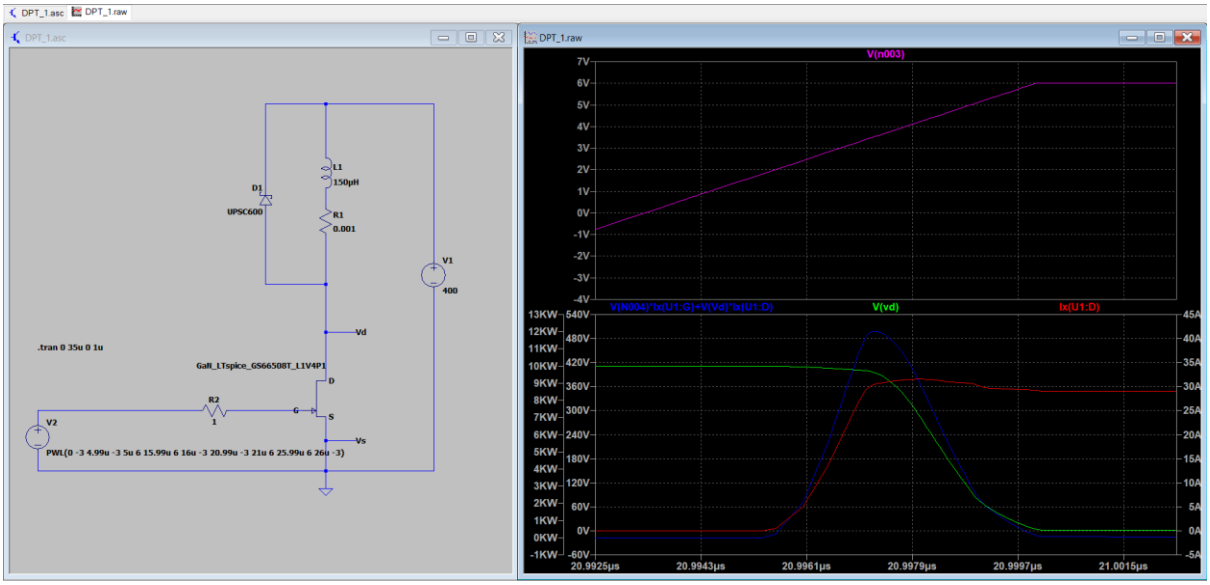

Figure 4.8: Turn on instance of the switch

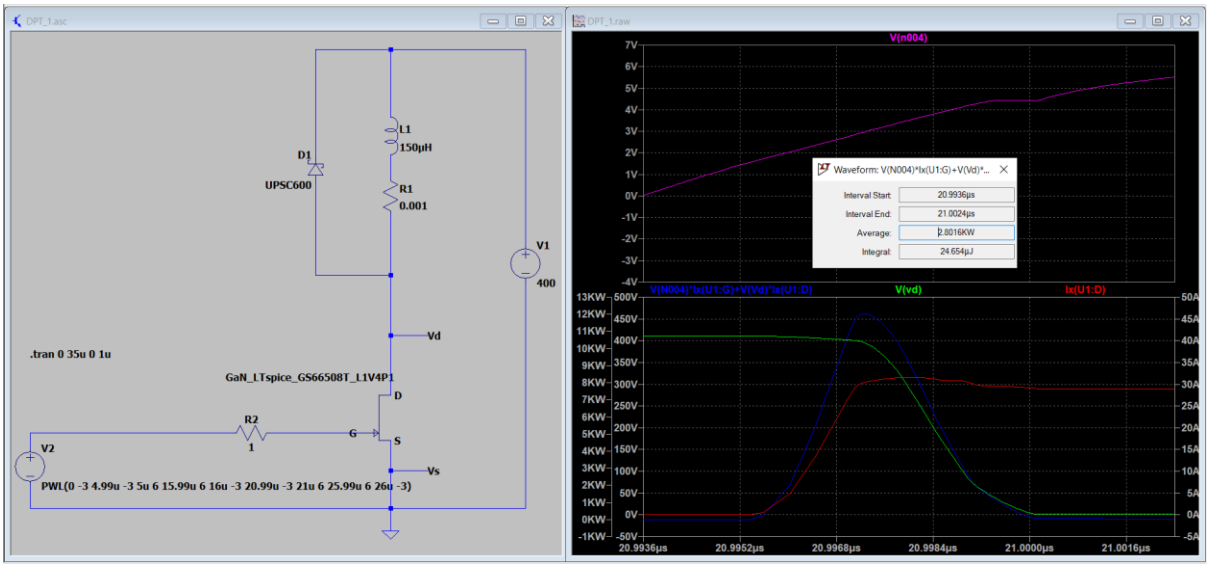

Figure 4.9: Turn on energy of the switch

Gate source capacitance is charged through the gate resistance. The gate to source voltage increases. When the gate to source voltage reaches a threshold voltage value of the switch, it starts conducting. The drain current and gate to source voltage further starts increasing. There can be a voltage drop in drain to source voltage due to parasitic inductances since the current is increasing in the power loop. Incidentally, the drain current reaches the load current value. Therefore, the load current is now completely passing through the switch. At this point, reverse recovery charge comes into picture. Miller effect is not considered in this case for ease of understanding. Then, the gate to source voltage reaches its on value and the drain to source voltage is in on state. Further, the measurement parameters for turn off event in simulation and in the datasheet is compared in Table 4.2.

Table 4.2: Measurement parameters for turn on event

Turn off time in simulation	4.9 ns
Turn off time as per datasheet	3.7 ns

4.4 Double pulse test on hardware

During the design phase of double pulse test equivalent circuit, external load inductor and capacitor bank were given highest priority. Apart from this, the surrounding components of the measuring circuit also have an impact on the

switching performance. Thus, following limitations or boundary conditions were considered while designing the circuit [18].

- Maximum turn off voltage
- Maximum test current
- Maximum rate of change of voltage and current
- Permissible self-heating of the semiconductor device
- Test temperature
- Possibility to perform short circuit test

Dimensioning of external inductor

The load inductor is required to ensure a constant current between the two switching states of the double pulse test. Measurement of the turn on and turn off switching events is done at the desired switching current. To achieve the desired current (30A in this case), the duration of the first pulse must be long enough for the inductor to get charged till the desired current. The external load inductor is usually larger in size (Selected inductor value=150 μH). Duration of the first pulse and the value of test current depends on value of the inductor.

$$I_{SW} = (V_{DS} * T_{ON1}) / L \tag{4.2}$$

While determining the turn on time of the switch, it is also important to consider the temperature rise of the switch. The operation of the switch might be affected if the temperature goes too high or above the operating conditions as per mentioned in datasheet [27]. Thus, there should be a limit to the duration of the first pulse to avoid the temperature rise of the switch as well as inductor. Therefore, the higher limit to determine the inductor value is given in equation (4.2).

Double pulse test waveform generation procedure is explained in detail in Appendix A

Double pulse test generated as Figure 4.10.

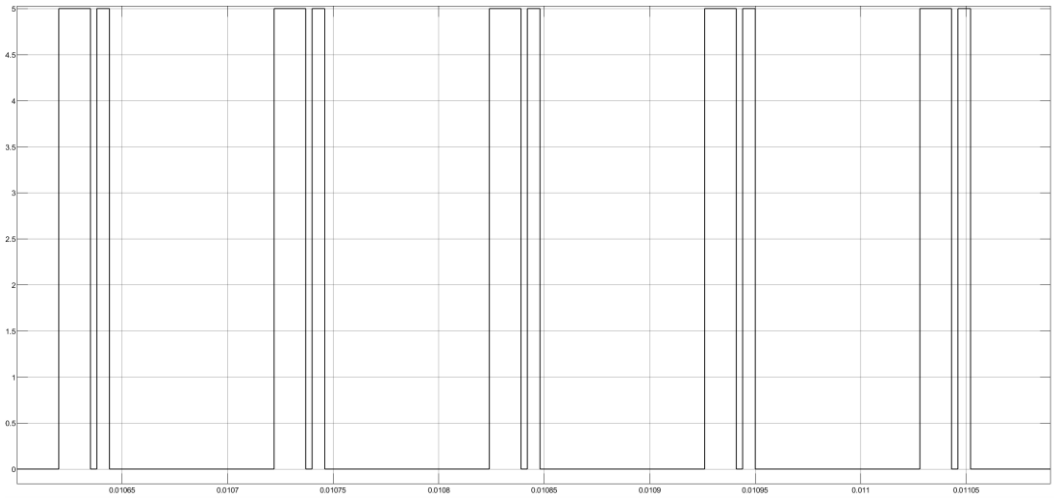

Figure 4.10: Double pulse test waveform of period 100 µs generated in Simulink

After this pulse is provided as input to the gate driver circuit, along with the DC power supply to the gate driver circuit and well as V_{DS}, the inductor current I_D is observed. It can be observed that the inductor current I_D not settling to zero further because the pulse period is not sufficient for it to discharge as shown in Figure 4.11. This can create stress on the switch resulting into temperature rise and may damage the device.

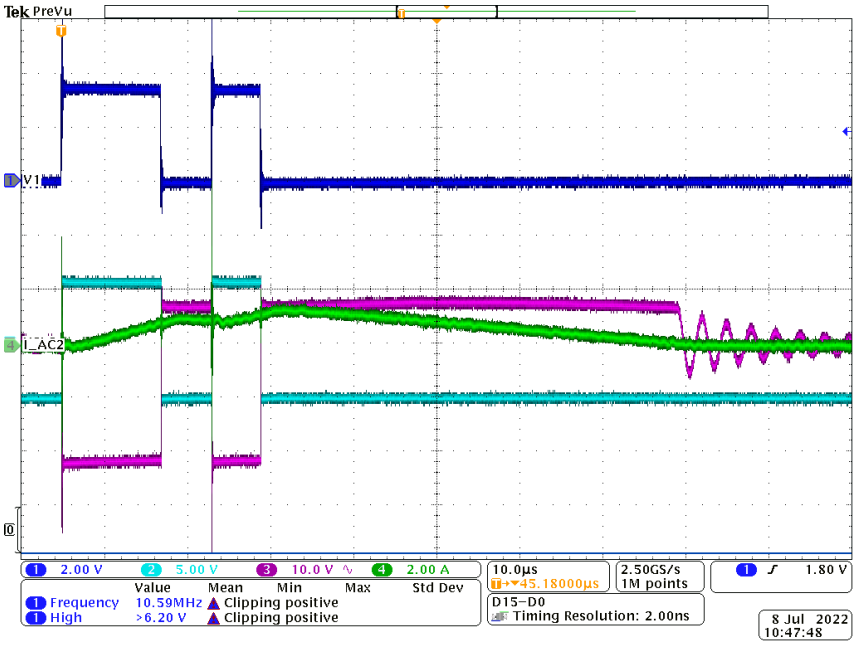

Figure 4.11: Inductor current I_D (CH4 2 A/Div) not reaching zero between two DPT pulses (CH2 5 V/Div)

Common mode noise

Common mode noise is measured using LISN and spectrum analyser. Various test cases were performed in order to check for the presence of common mode noise due to addition of different equipment in the test bench. When power supply is plugged in but not ON, the spectrum analyser shows results as per Figure 4.12

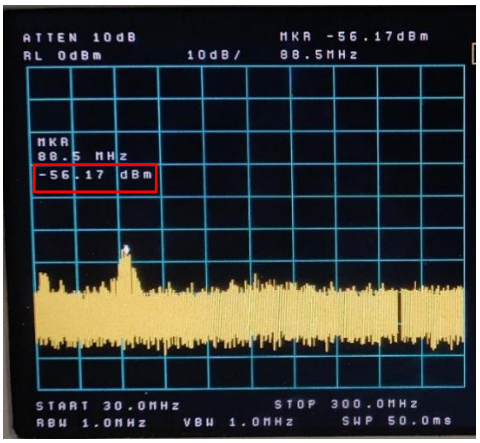

Figure 4.12: CM noise (-56.17 dBm) when the power supply is connected to DUT but not ON

Increase in common mode noise after the DC power supply is ON as shown in Figure 4.13. It can be seen that there is addition of common mode noise in the circuit due whose source is the power supply unit.

V_{in}=10 V (Start value of the power supply gradually increased in later test cases)

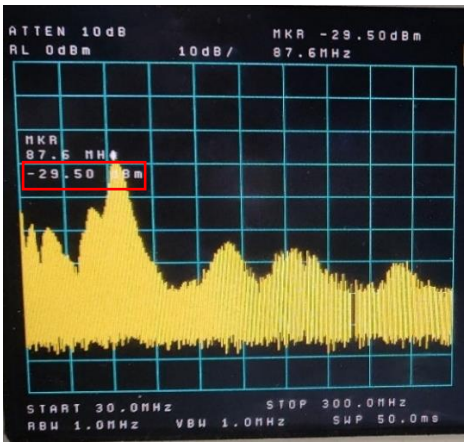

Figure 4.13: CM noise (-29.5 dBm) when the power supply is ON

The amplitude is set to 5 V. The width of the first pulse should be such that the inductor current does not exceed 30 A at 400 VDC. Thus, the on time for first pulse can be calculated as per stated earlier in equation (4.2). As a toroidal inductor of rating 150 μH 15 A is being used here, T_{ON1} is calculated to be 11.25 μs. The gap between the two pulses is set to be around 6 μs and the second pulse width is set to 6 μs. The period of one double pulse is set to be 100 μs and the burst of pulses is continued to be given for 100 ms. It is done to reduce the excess stress on the switches due high switching and current. Once the pulses are given to the gate of the bottom switch, V_{DS}, V_{GS} and I_L were measured. DC voltage is gradually increased to 60 V. During the time when DC voltage is being slowly ramped up, the given measurement parameters were observed on the DSO. It is observed that the inductor current is not settling to zero which is causing excess stress on the switch leading to its damage. Later, the double pulse test period is increased to **200 μs** which can be seen in Figure 4.14 in order to provide sufficient time for inductor to discharge completely (Refer Appendix A.2)

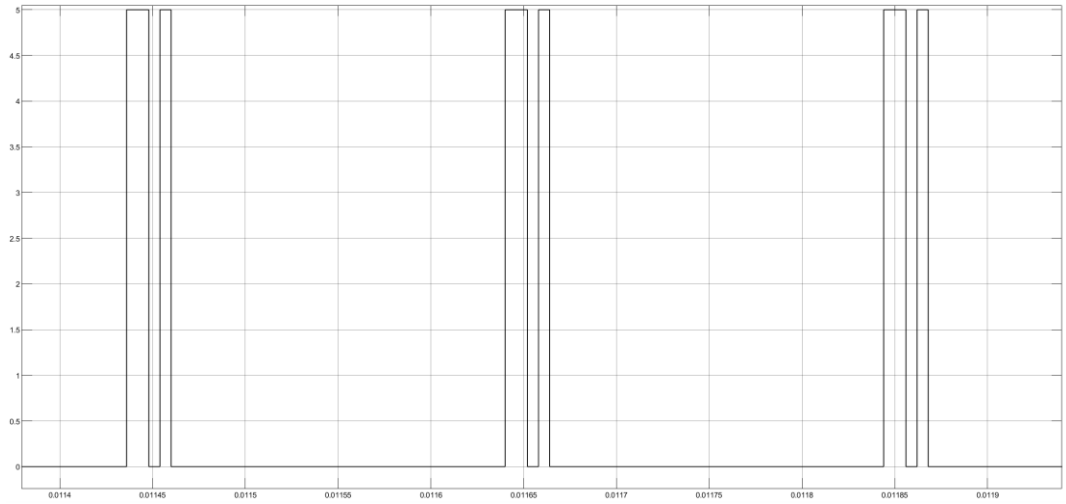

Figure 4.14: Double pulse test waveform of period 200 µs generated in Simulink

It can be observed that, as the top switch is always OFF whenever the bottom switch is turned ON, the current starts flowing through the inductor and then through the switch to the power ground. When the bottom switch is OFF, the inductor starts discharging through C_{oss} in a freewheeling state. Before the inductor is discharged full, again the bottom switch is turned ON. The first pulse width of the double pulse is such that the inductor current does not increase too much and go into saturation. The transition where the bottom switch is turning off at the falling edge of first pulse and then again turning on at the rising edge of the second pulse is measured for the turn off and turn on instances respectively. The measuring probes are connected in such a way that they make the shortest loop possible. A short ground clip is used to minimize the ground loop otherwise it might create undesirable inductances in

the path which will result into overshoot or ringing during the rising and falling edges. Thus, the ground loop of the measuring probe plays an important role in GaN HEMTs having very fast switching times. It is observed that at lower voltages, the drain to source current has a lot of ripple content after the inductor current reaches zero in Figure 4.15.

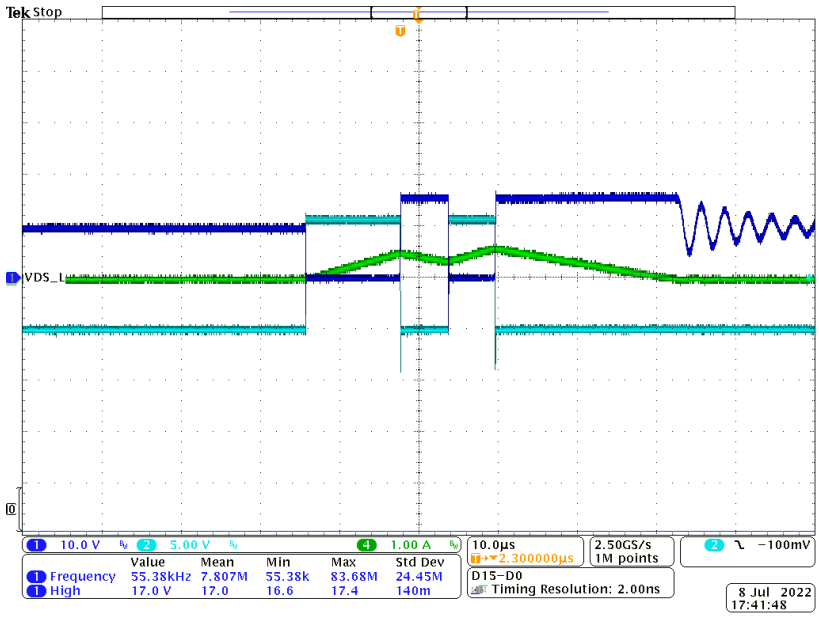

Figure 4.15: Inductor current I_D(CH4 2 A/Div) reaching zero between two DPT pulses (CH2 5 V/Div)

Turn on event captured as shown in Figure 4.16.

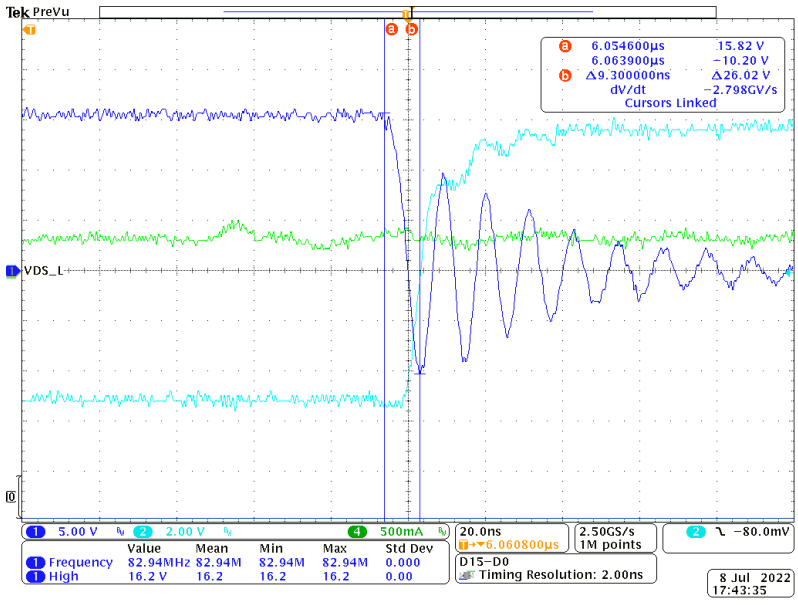

Figure 4.16: Double pulse test switching transient waveform turn on event V_{DS} $(CH1\colon 5\ V/Div), V_{GS}$ $(CH2\colon 2\ V/Div), I_D(CH4\colon 500mA/Div\ )$

Turn off event captured as shown in Figure 4.17:

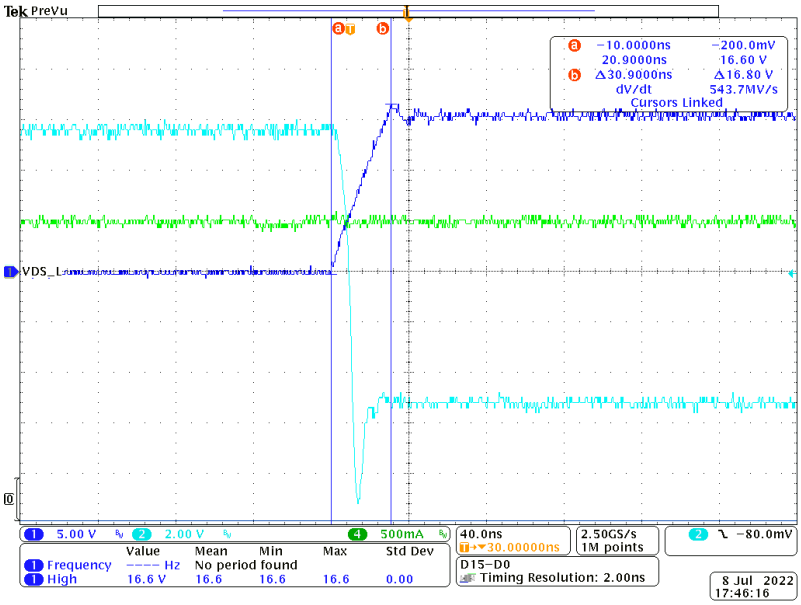

Figure 4.17: Double pulse test switching transient waveform turn off event V_{DS} $(CH1: 5\,V/Div), V_{GS}$ $(CH2: 2V/Div), I_D(CH4: 500mA/Div)$

EMI/ EMC

Fast switching of the switch creates high frequency noise or electromagnetic interference [28]. Parasitic elements in the design for example in the switch gate loop and power loop are responsible for the cause of EMI. GaN devices have very low total gate charge Q_g therefore they have higher turn on and turn off transition speed [29].

Experimental setup for conducted emission measurement

Required instruments as per the block diagram described in Figure

- Spectrum analyser
- Probe (common mode rejection probe) to measure V_{GS}
- DC power supply
- Oscilloscope
- LISN

It is ensured that the voltage probe is such that the measurement loop inductance is less.

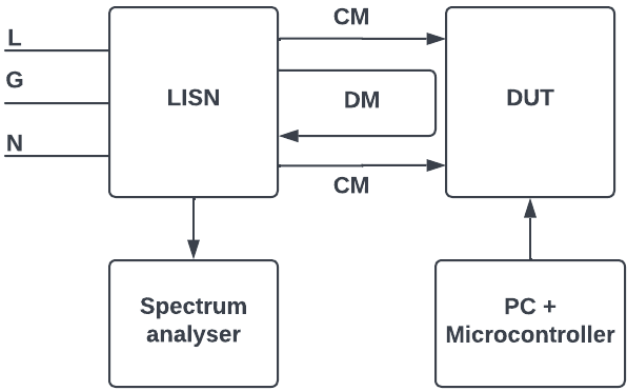

Figure 4.18: Common mode noise measurement

Common mode noise

Increase in common mode noise after the DC power supply is ON is shown in Figure 4.19

Vin=10V, frequency band 30 MHz to 300 MHz i.e., high frequency

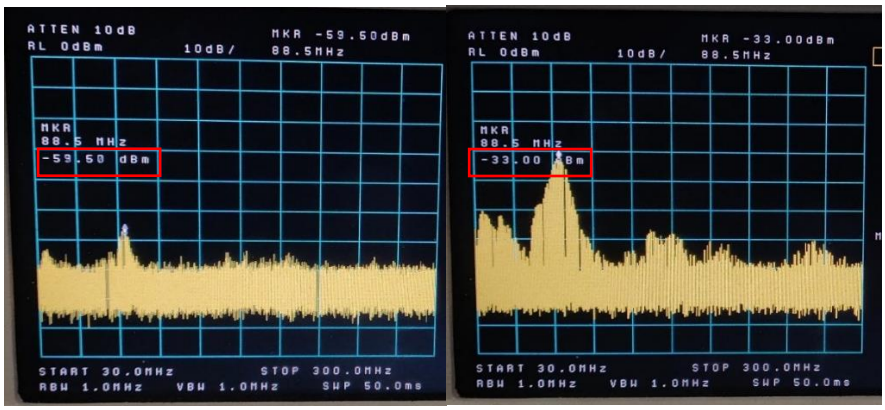

Figure 4.19: Increase in common mode noise after the DC power supply is ON can be observed as the noise peak is increased

Increase in external gate resistance:

Change is gate resistance changes the slew rate of GaN HEMT. The value of gate resistance is determined based on the type of application. The applications include optimization of gate resistance in order to achieve minimum switching losses, EMI or overshoot. Change is gate resistance brings modification in switching transitions which changes the slew rate dynamics i.e., dV/dt and dI/dt. This can be a solution to mitigate the problems related to EMI by changing the gate driver parameters i.e., gate resistance. When the gate resistance is increased, the slope of the switching transitions is decreased. This will reduce the generated EMI by creating a change in the slope

of voltage and current. However, this will increase the switching losses and decrease the efficiency. Thus, there is a trade-off between the switching losses and EMI. Research for new methods of driving techniques of the power converters has been one of the prime goals these days.

Table 4.3: Effect of change in external gate resistance on CM noise

R_{gate} in Ω	dV/dt in V/ns at $V_{dc} = 60\ V$		CM noise	
	Turn on	Turn off	dBm	dBµV
10	8.62	3.34	-12.7	94.29
15.5	8.48	3.6	-14.1	92.89
23.5	6.16	3.4	-16.2	90.79

Plot for change in gate resistance vs slew rate is shown in Figure 4.20 as per the results obtained from the measurements as per the Table 4.3.

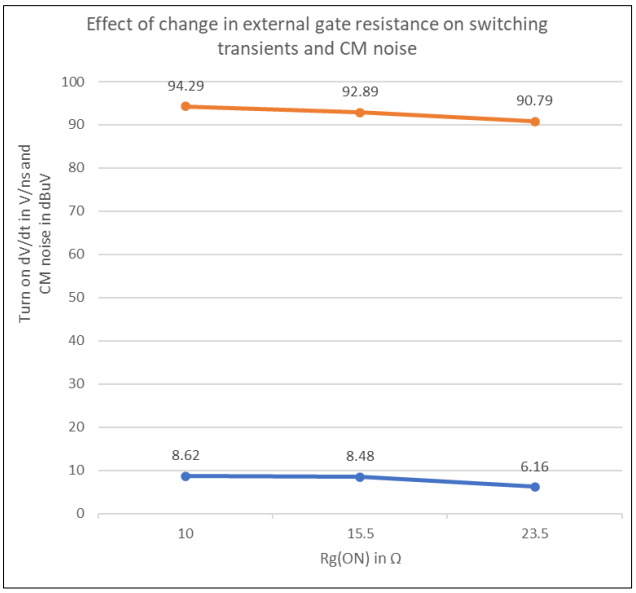

Figure 4.20: Plot for change in gate resistance vs slew rate and CM noise

These results are obtained from the following measurements of transient slope at turn on and turn off event on the DSO and measurement of the common mode noise on the spectrum analyser.

R_g =10 ohm

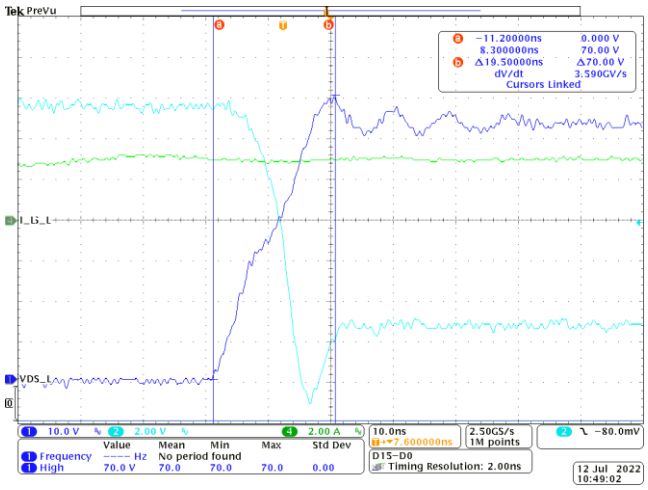

Figure 4.21: Turn off transient waveform of GS66508T for R_g= 10 Ω
V_{DS} $(CH1: 10V/Div), V_{GS}$ $(CH2: 2V/Div), I_D(CH4: 2A/Div)$

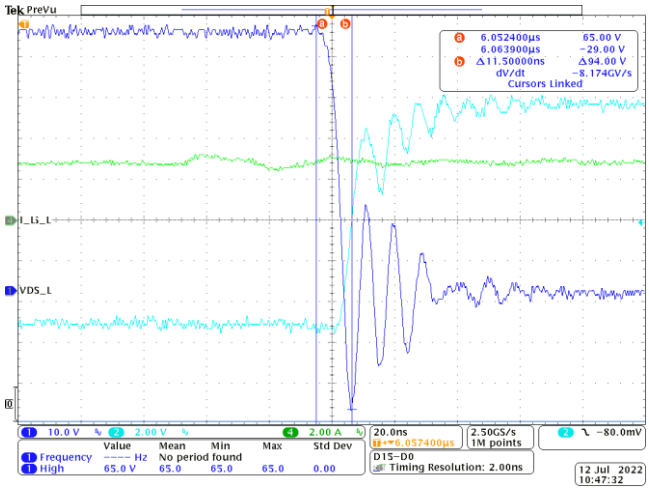

Figure 4.22: Turn on transient waveform of GS66508T for R_g= 10 Ω
V_{DS} $(CH1: 10\ V/Div), V_{GS}$ $(CH2: 2V/Div), I_D(CH4: 2\ A/Div)$

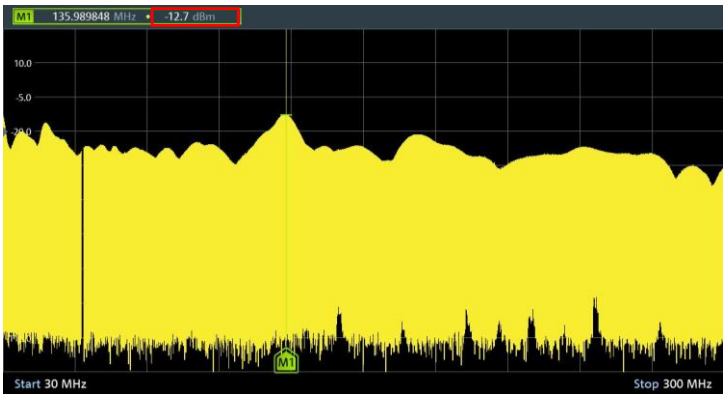

Figure 4.23: CM noise generated by GS66508T using 10 Ω gate resistance

R_g = 15.5 ohm

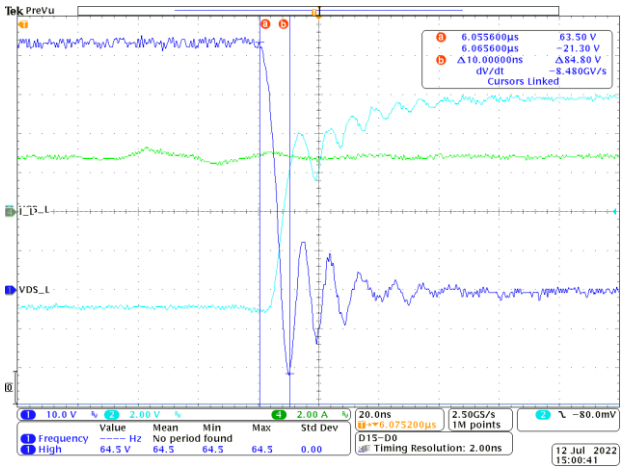

Figure 4.24: Turn off transient waveform of GS66508T for R_g= 15.5 Ω
V_{DS} $(CH1: 10\ V/Div), V_{GS}$ $(CH2: 2V/Div), I_D(CH4: 2A/Div)$

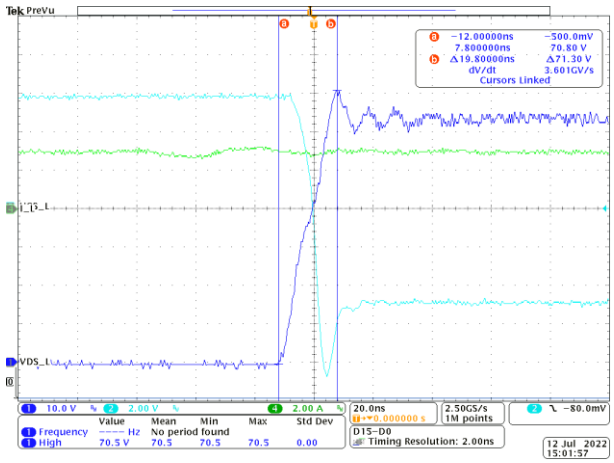

Figure 4.25: Turn on transient waveform of GS66508T for R_g= 15.5 Ω

V_{DS} $(CH1: 10V/Div), V_{GS}$ $(CH2: 2V/Div), I_D(CH4: 2\ A/Div)$

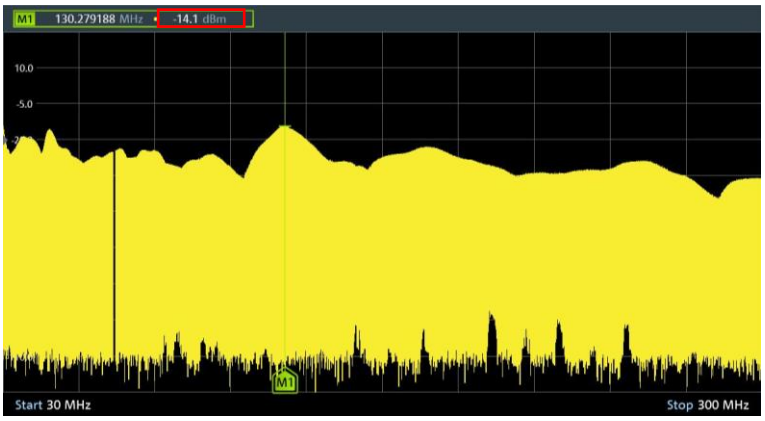

Figure 4.26: CM noise generated by GS66508T using 15.5 Ω gate resistance

R_g = 23 ohm

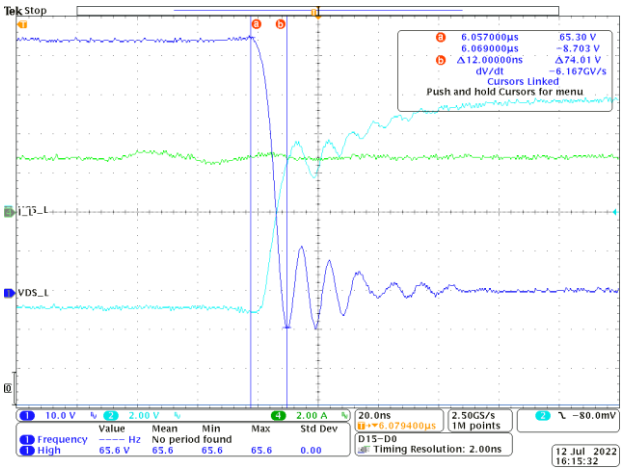

Figure 4.27: Turn off transient waveform of GS66508T for R_g= 23 Ω
V_{DS} $(CH1\colon 10\ V/Div)$, V_{GS} $(CH2\colon 2\ V/Div)$, $I_D(CH4\colon 2\ A/Div)$

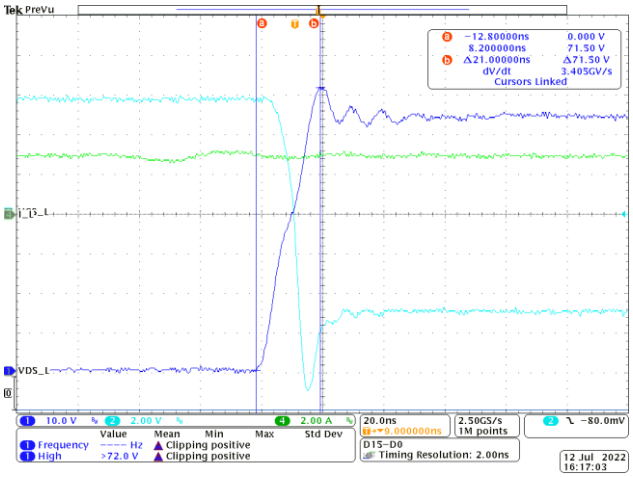

Figure 4.28: Turn on transient waveform of GS66508T for R_g= 23 Ω
V_{DS} $(CH1\colon 10\ V/Div)$, V_{GS} $(CH2\colon 2\ V/Div)$, $I_D(CH4\colon 2\ A/Div)$

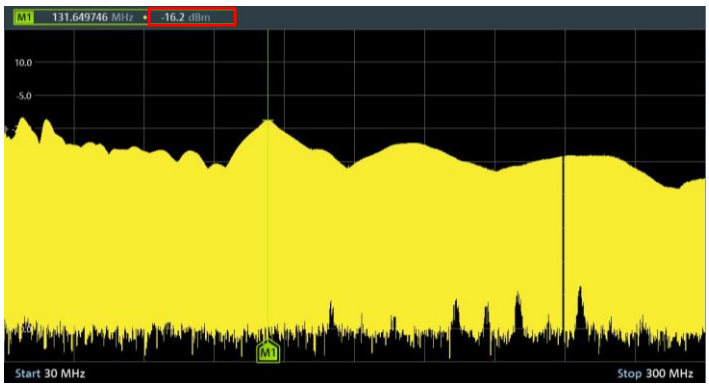

Figure 4.29: CM noise generated by GS66508T using 23 Ω gate resistance

It can be seen that as the external gate resistance is increased, the slew rate decreases. This means that it takes more time for the gate to turn on decreasing the transients. As the transition becomes slow, the noise is seen to be decreased shown in $dB\mu V$. The measured noise is at the highest peak which is within range of 130 MHz to 135 MHz of the spectrum under observation. There is a change of approximately 2 dB with each change in gate resistance value. As a result, the EMI performance can be significantly improved by reducing the switching speeds but at the cost of increase in switching loss. Thus, tradeoff between the switching loss and common mode noise has been quantified by parametrically changing the value of gate resistance.

5. Discussion

In order to check whether the external load inductor is responsible for any ringing in V_{DS} , the resonant frequency of the inductor is measured as 2 MHz which is far more than the switching frequency of the half bridge inverter module. Thus, the inductor itself is not adding in EMI in the V_{DS} of the switch. Furthermore, the interwinding capacitance of the inductor can be calculated in order to check if it has any effects on the parasitic elements. Figure 5.1 shows the resonant frequency measurement of the inductor in vector network analyzer which is around 2 MHz

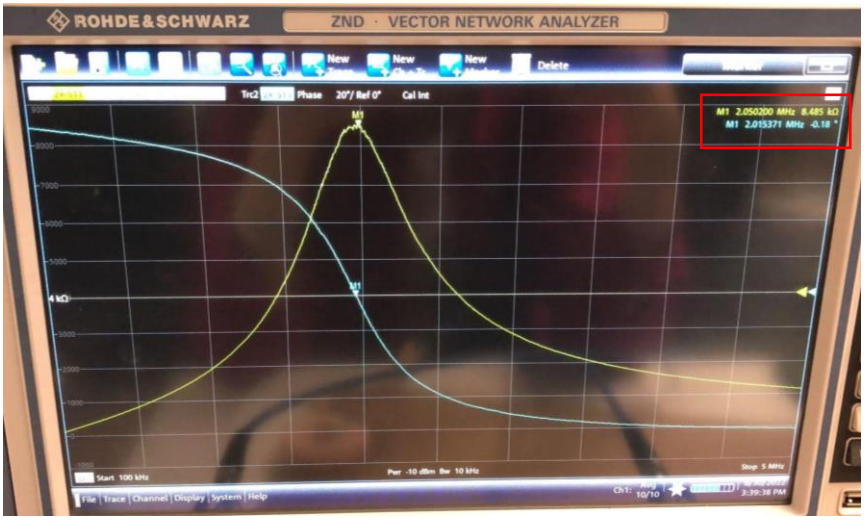

Figure 5.1: Measurement of resonant frequency of external inductor

Voltage overshoots and dips due to parasitic elements can be observed at the drain to source voltage V_{DS} and the drain current I_D [30]. It can also be seen that the ringing during turn off transient is more than that of the turn on transient. Such kind of ringing can be a result of improper placement of the current and voltage probes in the circuit. It is important to place short loops of probes inside the circuit to avoid unwanted coupling which may lead to ringing. Long leaded pins add to the parasitic elements in the circuit that result into ringing and overshoots in the waveforms to be measured. The device capacitance and stray inductance form a resonance circuit which can cause even higher unintended ringing.

Effect of gate resistance on EMI

External gate resistance is used to change the slew rate and switching speed to a desired value. Change in gate resistance changes the turning on and turning off dynamics of the switch. Increased R_g has comparatively apparent effect on dI/dt and dV/dt, it prolongs the time of switching on and off as well. That is because as R_g increases, the slew rate of V_{GS} will consequently decrease, which will not only slow down the turn-on delay of MOSFET, but also

reduces dI/dt during current commutation stage. When V_{GS} reaches the Miller platform, the varying of V_{DS} will largely depend on R_g during this stage. Besides, since the damping coefficient will increase with the rise of R_g, the switching ringing of V_{DS}, I_D, as well as V_{GS} can be quickly damped. This will increase the switching losses but the EMI will be reduced. Varying gate resistance will affect dV/dt and amplitude of V_{DS} ringing. It proves that the increasing R_g does have a suppressing effect on the level of the conducted EMI, whereas it multiplies the switching loss at the same time. In the interest of trading off the switching loss and the conducted EMI, the snubber resistance (R_S) and the snubber capacitor (C_S) could be used [31].

5.1 Challenges and limitations

- **Defining the final scope and objective of the thesis**

  Finalizing on aim of the thesis and defining its scope was the most important part of the thesis. It gives clarity and right direction in which one can start working on the goals. At first, the aim of the thesis was to design and develop HERIC inverter. Considering the scope would be vast as compared to a limited time period of Master's thesis, it was changed to design of a half bridge inverter. The aim of the thesis was then changed to characterize the turn off losses of GaN HEMT of different current and voltage rating by comparing two GaN switches on the same board using same gate driver. After the LTspice simulations of GaN models, it was observed that the turn off losses of GaN switches (Manufacturer: GaN systems) were so negligible that it was critical to measure those on hardware. Therefore, the final aim was set to characterize the switching losses in terms of common mode noise by parametrically varying the values of external gate resistor. Therefore, it was a prolonged process. Thus, it can be seen that, setting the proper deliverable and objective of the thesis is very important. It is beneficial to determine the scope of the thesis at the very start for the ease of understanding and work towards achieving the desired results.

- **Component availability and laboratory testing**

  After the aim of the thesis was finalized, the components were selected to work on the hardware testing. The availability of the components during that period was a critical factor because it would have added more delay in the thesis. Thus, the available components were studied and the best suitable components were selected and ordered. This decision making helped to start the hardware testing as early as possible. After the components arrived, then the laboratory setup was done along with managing all the required measuring instruments. The

current and voltage probes used for the measurements were compliant to the design test parameters and the measurement probes were selected as per the rating of the device voltage and current ratings. The ground cable loops of the probes were kept as small as possible to avoid creating unnecessary inductive loops that might hamper the result waveforms. However, the ringing observed in the voltage waveforms can be considered due to the presence of stray inductance in the circuit. Thus, it is important to have a proper probes placement inside the circuit.

- **Limitation with the testing**

  The LISN (Part number TBOH01 5 µH [21]) used for measuring common mode noise had input voltage limit of up to 60 V. Therefore, the supply voltage range to the evaluation board is from 0 V to 60 V. During the testing, it was found that the GaN HEMT were getting short after input voltage range 100 V onwards. After several iterations with the optimum timings of the pulses on double pulse test, the undesired stress on the switches was reduced along with the lower input voltage limit. Thus, measurements were made with the input range from 0 V to 60 V. The same hardware setup was tested with same input parameters and double pulse test specifications with Transphorm TPH3212PS GaN FET with some modifications considering its TO-220 package [32]. This was done in order to identify the cause of stress on GaN systems switches.

6. Conclusion

The aim of the thesis was to analyse the switching losses of GaN HEMT in a half bridge inverter with respect to common mode noise. Results and observations obtained from the double pulse test performed on the hardware setup confirms the aim has been achieved in form of a trade-off between the switching losses and common mode noise. The voltage waveforms indicate the switching transients such as dV/dt along with the rise time and fall time. They also indicate the losses are within limits with respect to the switching frequency. After testing the hardware with GaN HEMT with several iterations, optimum timings of the double pulse test were determined and the final results were obtained. The steps during the hardware setup and testing are supported by simulation. Thus, double pulse test performed on the hardware for characterization of the GaN switches helped in understanding of the proper way of designing the user cases, correct probing methods, accurate measurements of the critical parameters to derive the right conclusions.

The key learnings are stated below:

- Selection of electronic components as per the design criteria and market availability is necessary to avoid any unforeseen errors and delay in the design. While doing the PCB design, the gate loop and the power loop of the MOSFET gate driver should be as small as possible. A good PCB layout design can help in mitigating most of the problems related to EMI. The track lengths of the gate driver loop should be such that it does not create any parasitic inductance in the circuit. Provision of ferrite bead and RC snubber is kept in the design so that any unintended resonance occurring in the design due to parasitic elements can be reduced. In a power loop, the DC capacitors should be in form of a capacitor bank. At high voltage, if the parasitic inductance is too large, it might shoot up the voltage transients even more. Thus, the parasitic inductance in the power loop should be as small as possible.
- The selection of inductor is a critical criterion for the design while performing a double pulse test. The external inductor used in the double pulse test should have very low interwinding capacitance and very high resonant frequency. The inductor interwinding capacitance along with the circuit capacitance will result into ringing.
- The testing input voltage had some limitations and testing at a higher input DC voltage was causing damage to the switching components. Thus, the double pulse test was performed with a lower input DC voltage in order to get the desired results. The results pattern showed the exact behavior as it would have done at the higher DC voltage levels as per the results showed in some of the references.

6.1 Future Scope

Even though GaN switching devices have their respective challenges while implementing at high frequency and high voltage power electronic converters, this research work has successfully showed a way of optimizing the needs for suppressing the EMI. Another way can be addition of snubber circuit to depress the ringing and eliminate the number of oscillations without any effects on dv/dt and di/dt [31]. Thus, adding snubber does not affect switching losses which is an advantage over only changing the gate resistance to mitigate the EMI. Damping ratio is amplified due to addition of RC snubber thus, damping/ suppressing the peak overshoot noise at V_{DS}. This would help in improving the efficiency and power density of the system.

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Appendix A: Creation of double pulse test waveform

A.1 Creation of double pulse in MATLAB Simulink

A Simulink model is designed such that the double pulse generated is given to GPIO08 corresponding to PWM1A pin number 49 of the docking station through the microcontroller. Use of microcontroller gives flexibility and ability to control the pulse widths because the pulse width is a critical factor for double pulse test. If the operating current is undeterminable, then the number of pulses can also be conveniently limited using the Simulink.

TI C2000 series microcontroller TMDSCNCD2838x [26] is used to generate the PWM signal and is then given to the motherboard as PWML input for the bottom side switch. The configuration parameters for the elected microcontroller as they appear in Simulink are shown in Figure A.1

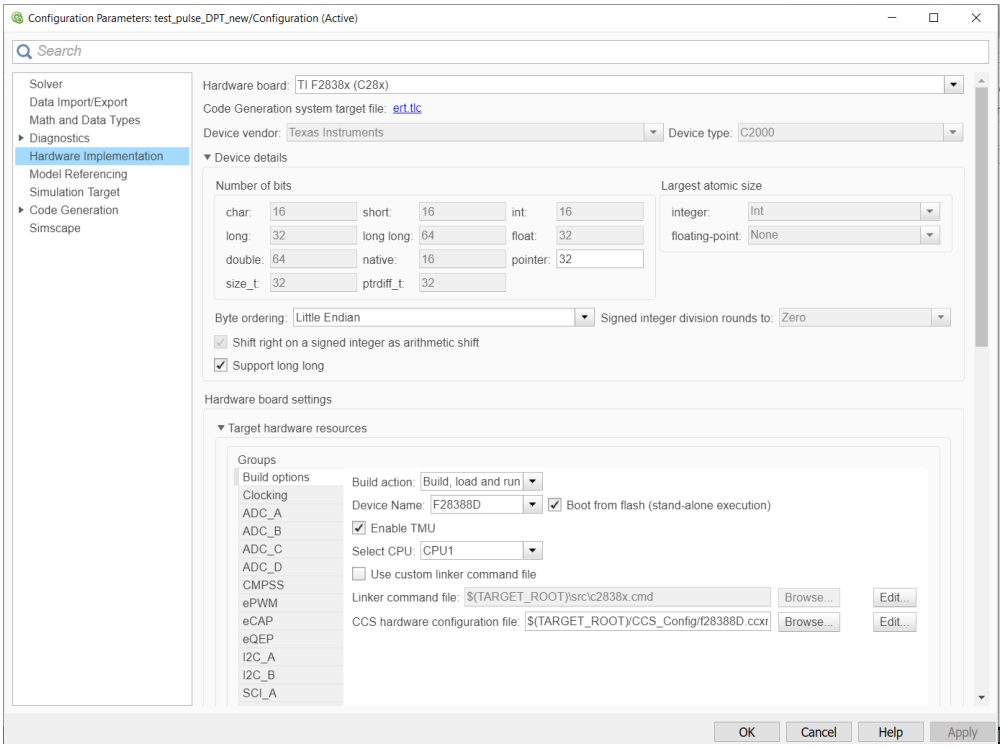

Figure A.1: Configuration parameters of TMDSCNCD2838x in Simulink

A Simulink model is designed as shown in Figure A.2 to create the double pulse test waveform. Two pulse generator blocks are used to create two different pulses for first pulse and second pulse respectively in the double pulse having different pulse widths. The generated pulses are then added to create one double pulse. The advantages of using Simulink model is that there is flexibility because the double pulse test is intended to be performed

in iterations. Therefore use of software tools where the pulse parameters can be easily changed is a preferable choice.

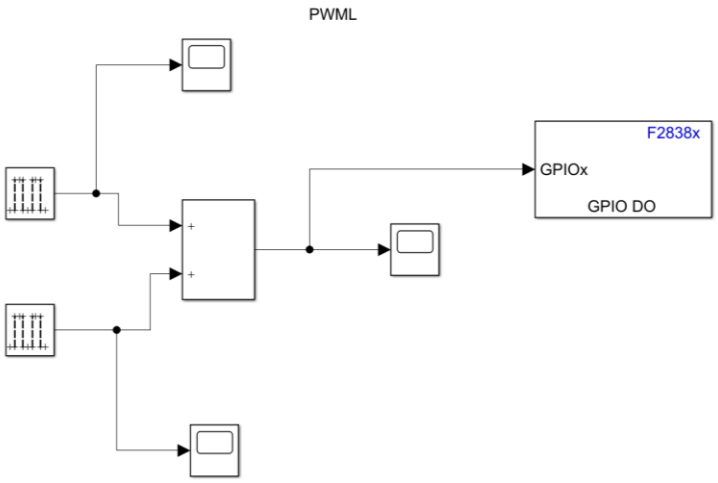

Figure A.2: Simulink model for creation of double pulse waveform

The parameters of each pulse generator block are given as Figure A.3 and Figure A.4. The amplitude of each pulse is set to be 5 V. The period, pulse width, delay and sample time are set so as to get the desired value of time duration of the pulses in a double pulse waveform.

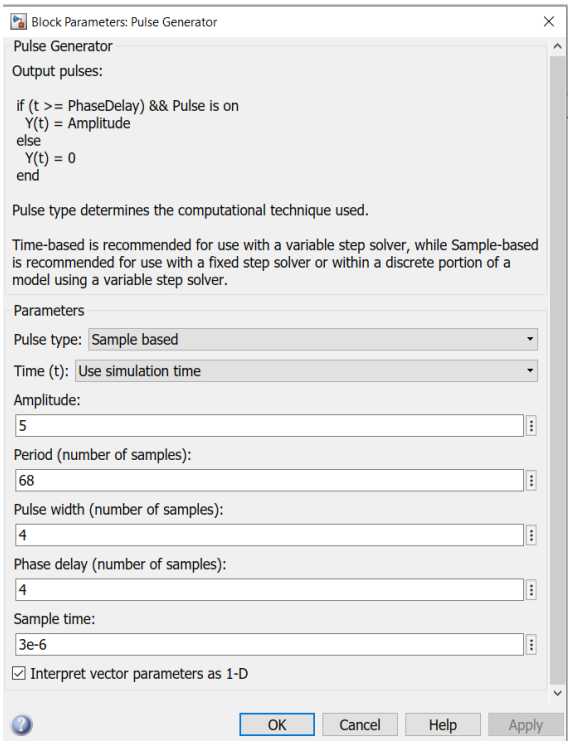

Figure A.3: First pulse generation block parameters

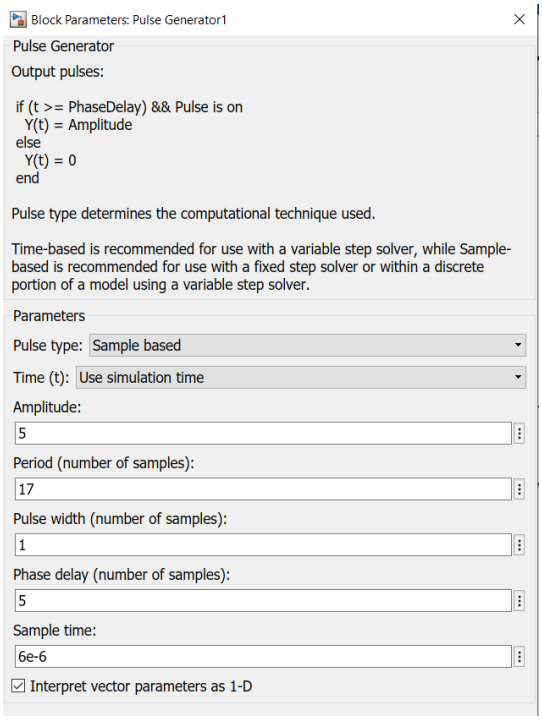

Figure A.4: Second pulse generation block parameters

After the addition of both the pulses, the result obtained which can be seen in scope block in Simulink is in Figure A.5

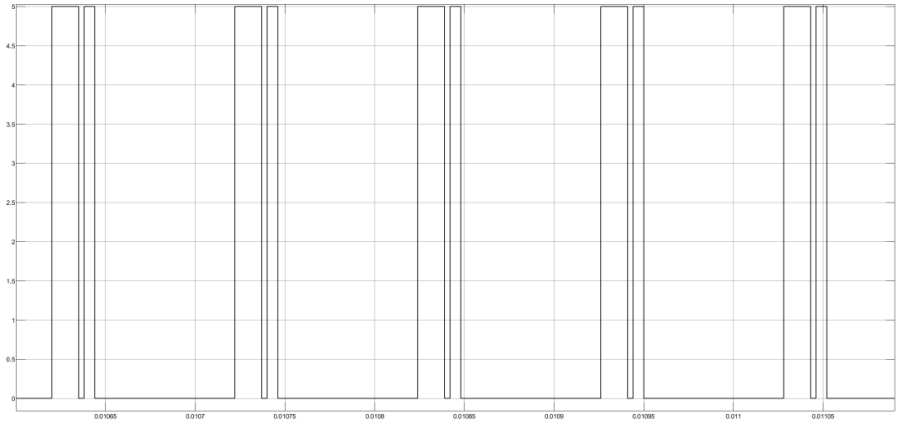

Figure A.5: Double pulse test waveform created in Simulink

A.2 Pulse generator block parameters for modified DPT waveform

For block 1, modified parameters are as shown in Figure A.6.

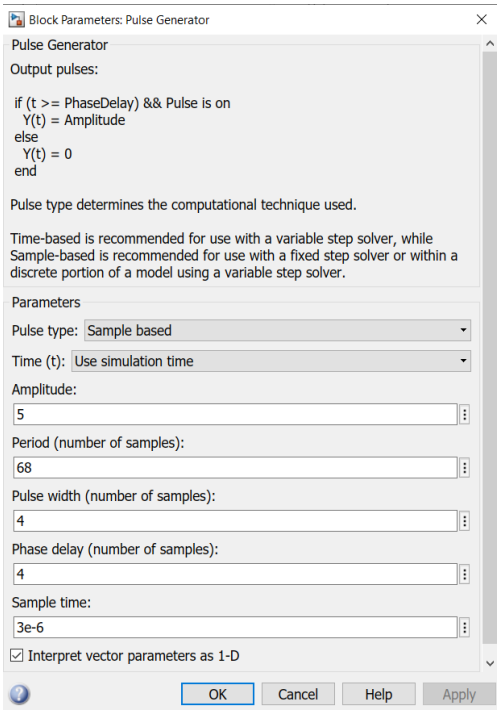

Figure A.6: First pulse generation block parameters

For block 2, modified parameters are as shown in Figure A.7.

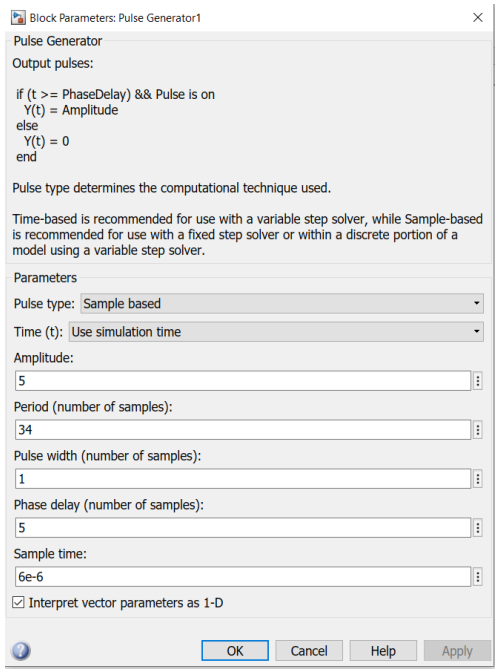

Figure A.7: Second pulse generation block parameters

After the addition of both the pulses, the result obtained which can be seen in scope block in Simulink is as shown in Figure A.8.

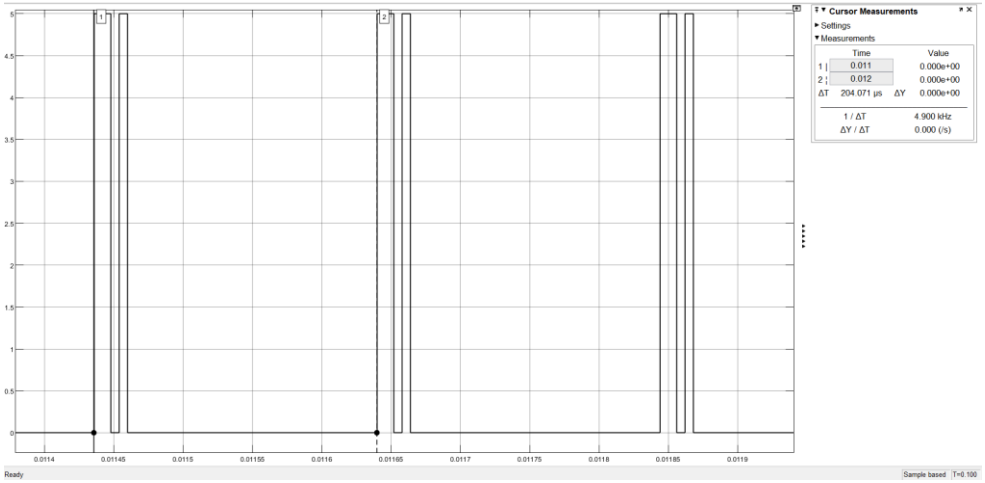

Figure A.8: Modified Double pulse test waveform created in Simulink

Appendix B: List of measuring instruments used for hardware testing

Equipment used for testing is chosen based on the parameters of the measurement values such as, voltage, current, frequency etc. Many equipment used during the thesis work for hardware as well as testing are listed in Table B.1.

Table B.1: List of equipment used during testing

Equipment	**Manufacturer**	**Part Number**	**Ratings**
Current Probe	Fluke	80i-110s	1kHz 100A
Curren Probe	Tektronix	TCP2020	$20A_{RMS}$
Voltage Probe	Tektronix	P5200A	50MHz 1300V
Voltage Probe	Tektronix	TPP0201	200MHz 300V
Power Supply	Gw Instek	SPS-3610	36V 10A
Power Supply	EA-PSI	9500-30	500V 30A 5kW
Oscilloscope	Tektronix	3 series MDO	1GHz 5GS/s
Microcontroller	Texas Instruments	TMS320C2000	16bit
Spectrum analyzer	Agilent	8564EC	30Hz - 40GHz
Spectrum analyzer	Rohde and Schwarz	FPC1000	5kHz – 1GHz
LISN	Tekbox	TBOH01	5uH
Vector Network Analyzer	Rohde and Schwarz	ZNB8 2 ports	9kHz – 8.5GHz
External Inductor	TrafΩx	45t 3x 250x0.071Cu	150µ 15A 400Hz
Multi meter	Fluke	28 II	1000V 10A
Solder Station	JBC	DDE-2C	450°C
Hot Air Rework Station	Duratool	D01841	480°C