Test results of ATLASPIX3 — A reticle size HVCMOS pixel sensor designed for construction of multi chip modules

R. Schimassek [a,*], A. Andreazza [b], H. Augustin [c], M. Barbero [d], M. Benoit [e], F. Ehrler [a], G. Iacobucci [e], A. Meneses [c], P. Pangaud [d], M. Prathapan [a], A. Schöning [c], E. Vilella [f], A. Weber [a,c], M. Weber [g], W. Wong [h], H. Zhang [a], I. Perić [a]

[a] *Karlsruhe Institute of Technology (DE), Germany*
[b] *Università degli Studi e INFN Milano (IT), Italy*
[c] *University Heidelberg (DE), Germany*
[d] *Aix Marseille Université, CNRS/IN2P3, CPPM, Marseille (FR), France*
[e] *Université de Genève (CH), Switzerland*
[f] *University of Liverpool (GB), United Kingdom*
[g] *University of Bern (CH), Switzerland*
[h] *formerly of University of Geneva (CH), Switzerland*

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ABSTRACT

High voltage CMOS pixel sensors will be or are proposed to be used in several particle physics experiments for particle tracking like Mu3e experiment. ATLASPIX3 is the first full reticle size monolithic HVCMOS sensor for construction of multi-chip modules. The specifications for the use case have been taken from ATLAS pixel upgrade in fifth layer where it was a candidate for. The size of the chip is 2.0×2.1 cm^2 with periphery at one side which makes the chip 3-side buttable. ATLASPIX3 has been implemented in a standard 180 nm HVCMOS process. Each pixel has an area of 150×50 μm^2 and contains a large charge collecting electrode implemented as deep n-well. The depleted volume around the n-well is enlarged by a high voltage bias and the usage of higher resistivity substrate. The readout electronics supports both triggered and triggerless readout with zero-suppression. ATLASPIX3 could be used for the construction of CMOS modules for particle tracking in experiments where high time resolution, high radiation tolerance, low power and low material budget are required. In the design phase, special attention has been paid to decreasing timing differences between pixels and the rate capability of the readout.

1. Introduction

High voltage CMOS (HVCMOS) sensors are depleted active pixel sensors implemented in a commercial standard CMOS process. Radiation hardness and fast charge collection, along with a simpler production process compared to hybrid silicon detectors, make them an option for experiments in high energy physics [1 3] and they were considered a candidate technology for the ATLAS experiment. As monolithic detector, they also allow for the reduction of the material budget by thinning down the sensor and saves costs removing the need for dedicated readout chips [4,5].

ATLASPIX3 is the first full reticle size monolithic HVCMOS sensor for construction of multi chip modules. It has been designed in a standard 180 nm HVCMOS process and submitted for production in April 2019. The size of the sensor is 2.0 × 2.1 cm^2 with 150 × 50 μm^2 pixel size. With the periphery including the readout on the bottom side only, the chip is three side buttable. The pixel consists of a large collection electrode with integrated amplifier and comparator. The readout is zero suppressed and has been optimised to cope with hit and trigger rates as expected for example in the outermost layer of ATLAS inner tracker after high luminosity upgrade [6,7].

With respect to its predecessors ATLASPIX1 and ATLASPIX2, pixel to pixel timing across the matrix has been optimised to stay within 25 ns with all pixels. This is necessary to be able to use triggered readout without losses or readout overhead from wider trigger windows. As a common feature with its predecessors, ATLASPIX3 implements in pixel tuning structures consisting of a three bit threshold tuning DAC (TDAC) for altering the global threshold and a disable bit for the comparator. The TDAC step size is adjusted with a global DAC. However, the structure of the TDAC is changed compared to the previous detector versions.

* Corresponding author.
E-mail address: rudolf.schimassek@kit.edu (R. Schimassek).

2. Readout system

For the ATLASPIX3 detector, the GECCO[1] ecosystem is used. It consists of an adapter board (the GECCO board) from a low pin count FMC connector to a card slot connector for the device under test driven by dedicated firm and software from FPGA and PC. It enables fast and easy reconfiguration of the measurement system. This feature has been used to derive a four layer beam telescope from the single detector set up with minimum effort.

Both telescope and single detector setup are read out by a single FPGA and the detectors in the telescope share all power lines. ATLASPIX3 is configured using a shift register scheme, an SPI bus or a single line command input. Addressing is done via veto gates in the load lines for the shift register scheme, with the chip select lines for the SPI bus and with addresses for the single line command input. Reference clocks as well as the single line command input are distributed between the detectors via LVDS fanout buffers.

For each layer, the configuration is kept individually in software. The four data outputs from the layers are received on the FPGA and merged into one data stream, where the data is also decorated with additional information as time stamp extensions and layer information. This data is then transmitted to the PC for storage and analysis. At 40 MHz time stamp speed, the 10 bit time stamp from the detector covers about 25 µs what is typically not sufficient for beam test measurements with bunch lengths in the order of milliseconds. Therefore, the time stamp from the chip is extended to cover at least several seconds.

3. Laboratory tests

Tests in the laboratory at KIT have shown a high yield with five of six tested samples to be fully functional. This statement includes that no dead or noisy pixels were found on them.

The detector has been measured to require 160 mW/cm^2 which may be decreased at the expense of time resolution. This comprises power for the pixel amplifiers and comparators as well as for the buffers for the readout. The major share of about 120 mW/cm^2 is consumed by the amplifiers and comparators. Compared to the 500 mW/cm^2 power consumption limit for ATLAS ITk, ATLASPIX3 has a large margin for settings with improved time resolution or power increases due to irradiation.

The achievable thresholds on single pixel level is 400 e^- which corresponds to a quarter of a signal from an ^{55}Fe decay. For this measurement, a noise signal rate $\ll 0.1$ Hz per pixel is chosen as limit. An example is shown in Fig. 1: Using test signal injections of increasing size, the detection threshold is measured by counting of the detected signals per signal set and fitting the transition with a Gaussian error function. From the fit, the threshold and noise parameters are extracted.

The test signal injections have been calibrated against ^{55}Fe decay signals via the amplifier output of the detector by recording both the ^{55}Fe decay, and injection signals of different charge with an oscilloscope. Afterwards, the signals are compared to find the charge injection that yields in the same signal amplitude as the ^{55}Fe decay signal.

Tuning of the whole matrix is performed using the same threshold and noise measurement procedure as above, with the goal of maximum width reduction of the threshold distribution. Performing the scan for each pixel, threshold and noise values are obtained. The found threshold values are compared to a target value and the TDAC settings are changed to reduce the distance of the individual pixel thresholds to the target threshold. With the new TDAC settings, the threshold measurement is repeated. Eventually, the TDAC values with the least difference to the target threshold are picked from all measurements to obtain the smallest possible threshold distribution for the given target value. Fig. 2 shows the untrimmed thresholds of a representative fraction of the matrix used to find a viable target threshold value at the low end of the untrimmed distribution and the threshold distribution after trimming. The vertical line marks the chosen target value. The distribution width decreased by a factor of four to $\sigma = 9.6$ mV which translates to 52 e^- for a threshold of 1200 e^- equalling an injection size of 220 mV.

An indicator for the quality of the trimming result is also the distribution of the used TDAC values: It should show a Gaussian shape centred around the middle value of 3.5 in case of ATLASPIX3 and have a width of $\sigma \approx 1.3$ to cover the full available range. The TDAC distribution for the trimming in Fig. 2 is shown in Fig. 3: From the distribution can be seen that the global threshold was slightly too high and the global TDAC scale almost right: The mean of the Gaussian distribution is below 3.5 but the width is close to the optimum value.

From the detection efficiency curves (as shown in Fig. 1), the noise of the system can be extracted from the fit with the Gaussian error function. These values are histogrammed and shown in Fig. 4: The average noise equals an injection voltage of (16.7 ± 2.4) mV or a charge of (86.7 ± 13.0) e^-.

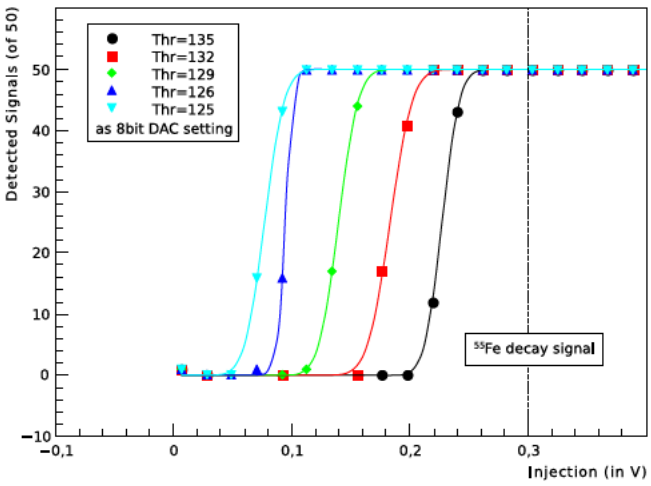

Fig. 1. To measure the detection threshold, signals of increasing size are generated in the pixel and the number of detected signals is recorded. For a noise signal rate $\ll 0.1$ Hz per pixel, a threshold of approximately 400 e^- has been achieved on one pixel at a time. The equivalent of an ^{55}Fe decay of 1639 e^- is indicated as vertical dashed line.

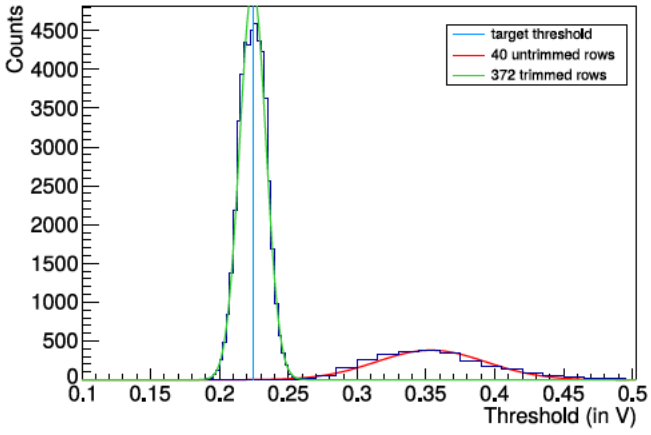

Fig. 2. The thresholds from a fraction of the matrix (40 rows) is used to find a viable target threshold for tuning indicated by the vertical line. This value is then used for setting the thresholds of all pixels resulting in the trimmed distribution of the whole matrix. The distribution width is reduced by more than a factor of four compared to the untrimmed distribution.

[1] GEneric Configuration and COntrol system. A generic readout system developed at KIT-ADL.

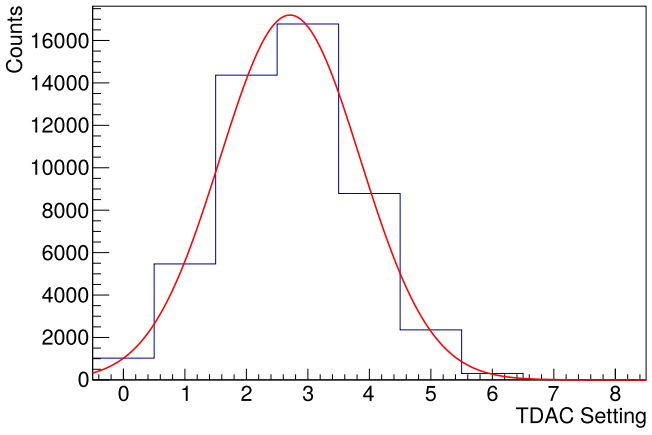

Fig. 3. The TDAC value distribution for the trimmed matrix indicates a slightly high global threshold for the trimming target materialising in a mean value below the optimum at 3.5. The width of $\sigma = 1.14$ is close to the optimum which means that the global scaling of the TDACs is chosen right.

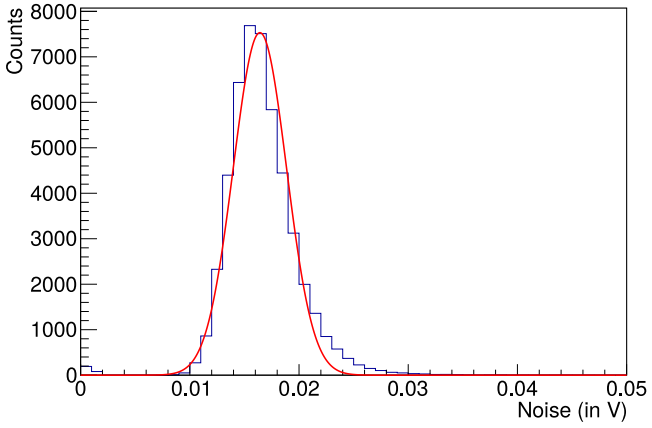

Fig. 4. The transition width in the detection efficiency measurement gives an indication for the noise in the system: This noise value is plotted for all pixels after trimming. The mean is (16.4 ± 2.4) mV which translates to $(86.7 \pm 13.0)\,e^-$.

4. System testing with an electron beam

Sensor modules typically share power supply and configuration lines between the chips, either via fanout chips or addressing. Hence, the beam telescope described in Section 2 differs from a sensor module only in the arrangement of the single sensors. As a consequence, a working beam telescope is a proof for fitness of ATLASPIX3 for module building. A beam test is one option for making sure that the single detector layers work as a system.

As first step, the time over threshold (ToT) measurement is used to verify that the single chips are detecting particles. Afterwards, the system functionality is probed using the layer to layer correlation.

ATLASPIX3 implements ToT to improve tracking performance. The measurement has a resolution of 7 bits. The improvement comes from off line time walk correction. The measurement granularity can be adjusted to match the expected signal length. It has been tested with the 3 GeV electron beam at DESY [8]. The measurement has been done with the beam telescope on all four layers simultaneously. Without tuning of the pixels, the overlay of all pixels in each layer forms a Landau Gaussian distribution each (see Fig. 5). The distributions have a similar shape and a large Gaussian contribution to the distributions. This Gaussian contribution consists of two parts: Firstly, the noise from the pixel electronics, and secondly, from the pixel to pixel differences. The latter contribution can be reduced by trimming the thresholds and calibrating the ToT measurement for the pixels.

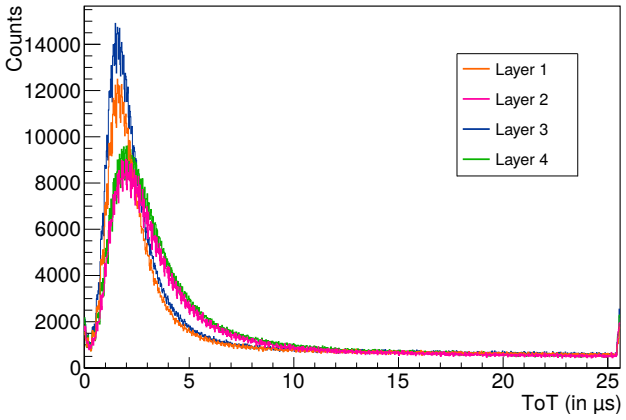

Fig. 5. In the 3 GeV electron beam at DESY, the Time-over-Threshold (ToT) distributions – overlaid for all pixels of each layer – have been measured with the layers of the ATLASPIX3 beam telescope. The distributions have been measured simultaneously showing the operability of the ATLASPIX3 detector in modules. Since the amplifier feedback settings have not been tuned, the Landau shape differs between the layers.

If the signals in Fig. 5 originate from particles passing the telescope, correlation between the signals in the different layers is expected. For the first two layers in the telescope, this is shown in Fig. 6: The sharp correlation lines indicate for particle dominated data content of the readout. The width of the correlation lines show a width of $\sigma \approx 50$ µm. This is the pixel size on the short edge and expectable due to charge sharing between the pixels.

5. Matrix timing

To achieve uniform timing across the whole matrix, the on chip transmission line capacitances have been adjusted to compensate for different lengths. In addition, pixel to pixel delay differences are min imised by applying concepts as avoiding different transmission line lengths. In the following, the measurement of the delay in one column is presented, before the result of a timing optimisation for the whole matrix is described.

Timing measurement

The signal delay can be probed with charge injections in the pixels and a time reference. The signal size is chosen to be 3000 e^- to exclude time walk. This is necessary, as the delay difference to be measured has been simulated to be 6 ns in total. The time stamp of the detector is set to 40 MHz for this measurement. With an external 400 MHz time reference, the signal delay differences can be measured precisely: The signals are generated synchronously to the time stamp epoch of the detector and the time stamps read out are stored. With the external time reference, the test signal is then shifted by 2.5 ns per step and the time stamp measurement is repeated.

The number of signals with a certain time stamp is recorded for all values of the external delay. Signals with this time stamp will be referred to as in time. This way, the transition between time stamps is used to measure the delay with the precision of the external time reference. The result is an in time efficiency window function that can be fitted with a multiplication of two Gaussian error functions (such a function is shown in Fig. 8). As the external delay is scanned, a shorter delay of a pixel results in a longer delay of the external reference to obtain the expected time stamp. The external delay for the middle of the rising edge of the pulse will be referred to as (signal) delay.

Performing the measurement for all rows, the delay change between first and last row can be probed. The statistics can be improved by

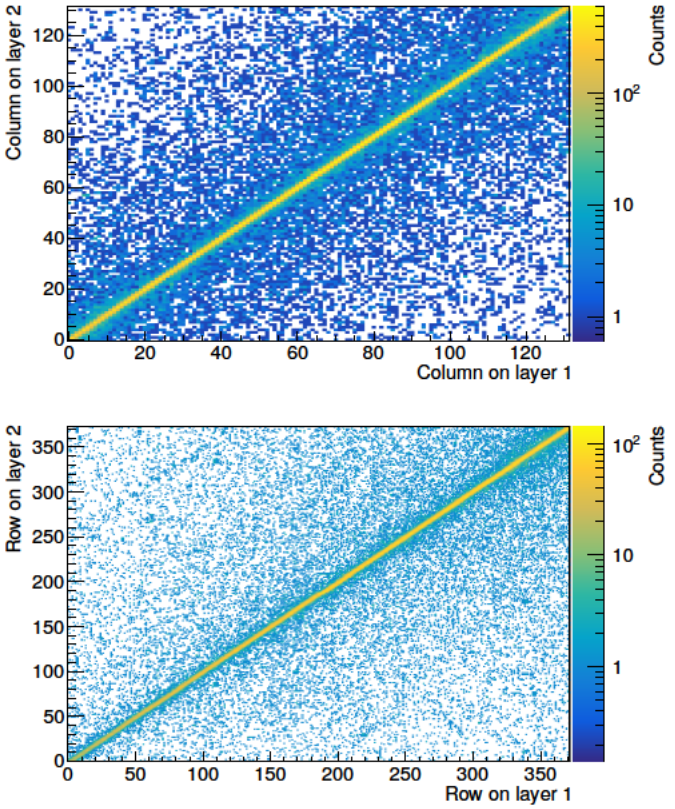

Fig. 6. The correlation of the data from the first two layers shows sharp correlation lines. The upper plot shows the horizontal correlation along the matrix columns, the lower plot shows the vertical correlation along the matrix rows.

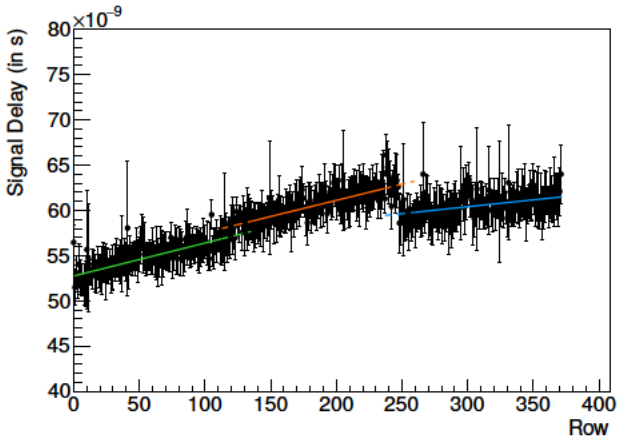

Fig. 7. The average of the delay from ten columns is plotted over the row index. The signal delay increases with the row between the routing changes visible around row 124 and 248 where the delay jumps by 1.1 ns or 3.2 ns, respectively. The total spread of the delay due to row dependency is (10.1 ± 0.7) ns.

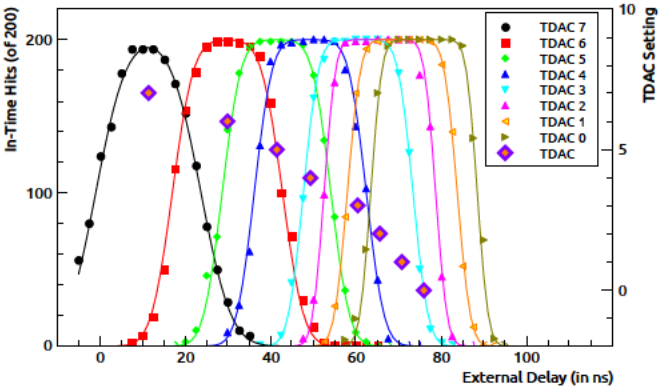

Fig. 8. Timing measurement for pixel (0|0) with a 400 MHz time reference. For different signal delays after the time stamp epoch, the number of signals with time stamp value 507 is plotted resulting in the pulse shape: Too short delays result in smaller and too long delays result in larger time stamps and are not counted. As the external signal delay is used as abscissa and the accepted time stamp value is fixed, a later detection has to be compensated by an earlier generation shifting the pulse to the left. The data series labelled *TDAC* is the TDAC value over the middle of the in-time window.

measuring several neighbouring columns, because the columns in the design are copies of each other. The mean from ten columns is calcu lated in Fig. 7: The delay increases with the row as expectable because of increasing signal path length. Around rows 124 and 248, changes in the routing are visible as steps in the delay and changes of the slope. The longest delay is found for the row just before the change in row 248 and the delay spread from the row dependency is (10.1 ± 0.7) ns.

Timing improvement

The limited power consumption imposed on the detector by the ATLAS ITk specification puts a lower limit on the rise time of the amplifier. The finite rise time leads to altered timing with a change of the threshold voltage. This can be exploited if the exact value of the threshold is not important.

This is the case for detecting large signals i.e. time walk can be neglected. This enables the usage of the threshold tuning DAC (TDAC) for timing adjustments. The threshold has to be higher compared to the threshold tuning in Section 3 to be able to change the threshold for all pixels without going to levels at which noise becomes a problem. However, this is excluded by the use case.

With the delay measurement as described in the previous section, the delay is measured for different TDAC settings: The lower the thresh old is, the earlier the signal is detected and the longer the external delay has to be to compensate for this in order to read out the same time stamp. For one pixel, the in time hits are plotted for all TDAC settings in Fig. 8. The lowest threshold at TDAC setting 0 shows the longest reference signal delay of all TDAC settings. The change is monotonous as indicated by the additional data series labelled *TDAC*: For it, the average of starting and falling edge delay of the in time efficiency pulse is used as abscissa and the TDAC value as ordinate giving an impression of the delay range available for timing tuning.

From the monotonous behaviour of the TDAC dependency of the pixel delay, a tuning procedure is derived measuring the timing for all pixels and setting the appropriate value to achieve equal timing. The target value for the delay is extracted from the distributions at highest and lowest threshold setting as average of the mean of Gaussian fits to both distributions.

The selection procedure results in a delay distribution which is narrower than the distributions for the single TDAC value distributions and is shown in Fig. 9 in solid green. The width of the delay distribution decreased to $\sigma = 2.34$ ns, which is almost a factor 4 smaller with respect to the untuned distributions as visible from the example of the highest threshold setting distribution at TDAC value 7 in dashed blue.

The resulting delay map for the full matrix does not show a gradient, but a uniform behaviour as shown in Fig. 10. Especially, the delay step at row 248 from Fig. 7 is not visible any more.

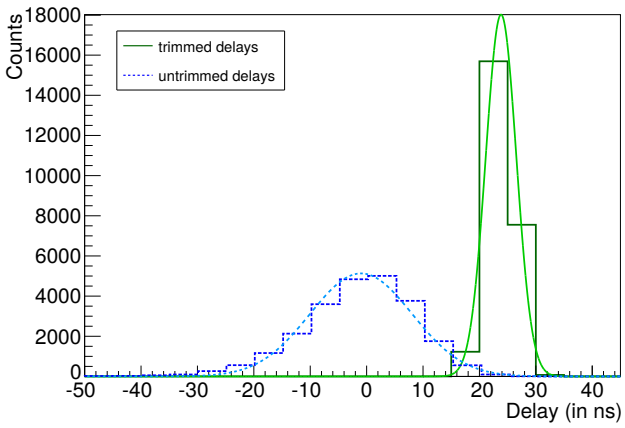

Fig. 9. The pixel delay distribution for the timing trimming result forms an almost four times narrower delay distribution than the distribution for all TDACs with the same value as indicated for TDAC value 7. The width is $\sigma_{\text{trimmed}} = 2.34$ ns compared to $\sigma_{\text{TDAC 7}} = 9.06$ ns.

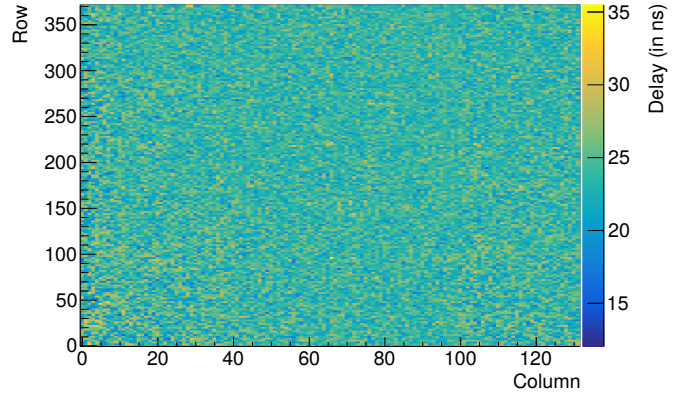

Fig. 10. The delay map of the tuning result does not show a gradient over the matrix being measured with the same signal source as the data used for the tuning. Also the step at row 248 from Fig. 7 is not visible.

6. Conclusions

The ATLASPIX3 detector has been fabricated, is working and the tested samples show a high yield. A power consumption of less than 160 mW/cm^2 has been measured and suitability for module building has been proven with a four layer beam telescope. Amplitude measurement via time over threshold method has been proven to work with an electron beam at DESY with a cross check of the data not being noise dominated by correlating the data between the telescope layers. The most probably value (MPV) of the ToT distributions from the beam test of 2 µs leads to the conclusion that the set thresholds are significantly smaller than the MPV signals. Threshold tuning to 1200 e$^-$ at a noise of $\sigma = 52$ e$^-$ has been performed. The row dependency of the signal delay has been measured to be (10.1±0.7) ns. And excluding time walk the matrix can be tuned to a pixel to pixel delay difference of $\sigma = 2.34$ ns.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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