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DESIGN OF TWO STAGE BULK-DRIVEN OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA) WITH A HIGH GAIN FOR LOW VOLTAGE APPLICATION

Pushkar N. Mishra
Syracuse University

Abstract

An Operational Transconductance Amplifier (further abbreviated as OTA) is a voltage controlled current source used to produce an output current proportional to the input voltage. A schematic architecture for a 180nm OTA is presented in this thesis with the goal of improving the open-loop gain for a 0.9V supply voltage with a rail-to-rail bulk-driven input stage. Results show an open loop gain 97.14 dB with a power consumption of 3.33uW. An OTA with over 90 dB open loop gain and lower power consumption is highly suitable for low-voltage applications. The slew rate of the OTA is 0.05V/uS with a unity-gain bandwidth of 8.4MHz. A 10uA ideal bias current reference is utilized for the design. The phase margin is around 49.2 degrees.

The threshold voltage for a 180nm N-channel Metal Oxide Semiconductor (also known as NMOS) device is around 400mV which restricts the low voltage applications in most amplifier circuits. The fourth terminal (bulk) of the MOS device is utilized to optimize the voltage headroom (V_{ds}). The bulk terminal uses a much lesser source to drain voltage than the gate-driven transistors, and the transistors remain ON with an input voltage as low as 0.1V. A bulk-driven input stage ensures the amplification in the subthreshold region (input signal less than the threshold voltage of the MOS device). However, even with the bulk input MOS device, a rail-to-rail input stage is employed to improve the dynamic range for the input signal from 0V to 0.9V with a supply voltage of 0.9V. The fluctuation in open loop gain concerning the change in input signal in the published research is because of the constant instability in the intrinsic transconductance of the input devices. A possible solution is presented in this thesis by adding a second dominant pole to the circuit (i.e., second stage for the OTA), which reduces the dependency of intrinsic transconductance (bulk-

driven device) on the total open loop gain of the amplifier. Thus, a significant gain of 97.14 dB with minimal fluctuations is achieved. Furthermore, adding a second stage improves the gain by distributing the dependency of the gain due to the first stage to both poles in the circuit. Hence, the problem of fluctuating transconductance of the input stage is resolved by the constant intrinsic transconductance of the MOS near the second pole (M19).

To improve the gain, a folded cascoded amplifier connected with the input stage results in a better impedance (in the first stage) known as the gain stage. In the second stage, a large PMOS common source amplifier gives a good output current compared to the input stage to enhance the output swing and drive a purely capacitive load of 0.5pF. Furthermore, a miller capacitance is used to compensate for the frequency between the first and the second stage and improving the unity-gain bandwidth. An additional biasing circuit in the second stage amplifies the current output of the first stage and thus improving the slew rate of the entire device. In addition, the biasing circuit resolves the biasing issues for the second-stage common-source amplifier. It improves the output swing of the device to obtain a clean/undistorted output waveform.

All the simulations are carried out in the LTSpice simulation tool to test the waveforms and bode plot for open loop gain and phase margin (49.2 degrees) at different processes (slow, typical, and fast), input voltages (0-0.9V), supply voltage (0.8V, 0.9V, 1.0V) and temperatures (-10 to 100 degree C).

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by

Pushkar Nath Mishra

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Chapter 1: Introduction

Portable electronics are becoming increasingly popular amongst many users in different application areas. Wearable intelligent devices make life hassle-free in terms of domestic applications (such as smart-ring, smart glasses, and smart earplugs) as well as biomedical applications like pacemakers, hearing aid for hearing-impaired individuals, blood pressure monitoring systems and other biosensors (Electrocardiography or ECG monitoring systems). In wireless body sensors, ECG amplifiers occupy a large proportion of chips in ECG monitoring systems [1]. For example, every small rhythm in your heart has hidden information regarding the health of a person. Sometimes these electrical activities can be significantly smaller, beyond imagination (as low as 0.001V), this calls for employing an addition amplifier circuit for observing every minute details of those electrical activities for understanding the depth of a person's health. An Operational Transconductance Amplifier (OTA) plays a significant role in amplifying the signals from the sensors (body sensors and intelligent sensors for low voltage applications) and further processing [2] the amplified signal to transmit the desired result through the communication channel.

The constant need for advancement in solid-state electronics forces researchers to optimize the device performance, reduce the cost, boost device speed, reduce area, lower power consumption and, most importantly, increase the battery life. The device's size is a significant factor when designing any analog circuitry. In such applications, reducing the device size optimizes most aspects, such as speed of operation, portability, economic feasibility, and user accessibility. Reducing the size of the battery (supply voltage) is the most common way to reduce the overall

footprint and weight of the device. Reduction in supply voltage reduces the power consumed by the amplifier and improves the device's battery life. However, with a reduction in supply voltage, comes the biasing issue because the threshold voltage of a 180nm MOS device used in this design is around 400 mV. This is where we utilize the bulk-driven functionality of our MOS device, hence bypassing the threshold voltage requirement of a transistor to turn ON. Several designing techniques [3], around low voltage analog design can be found in the literature, such as using the MOS in the sub-threshold region (poor gain-bandwidth product), floating gate MOS (increased cost and lower gain), and self-cascaded MOS devices (does not provide many advantages for low voltages). Hence, bulk-driven MOS device is beneficial for low-voltage applications. The main disadvantage of a bulk-driven device is that the intrinsic transconductance of the bulk-driven device is much lower than the gate-driven device, which lowers the total DC gain of the amplifier. To improve the overall gain of the OTA, a gain stage is added to the input stage bulk-driven transistor. This two-stage process improves the gain at the lower voltages.

In addition to reduced size, there is a need to maintain a balance between the stability and the dynamic range of the device to obtain uniformity in the device's operation. Improved dynamic range allows the use of maximum voltage headroom available in the supply using a rail-to-rail input stage described in detail, in Section 1.1 and Section 3.2. Moreover, adding a second stage to the device can improvise the frequency response, bandwidth, and common-mode gain. Higher gain reduces the dependency of the total open loop gain on the bulk-driven input. However, with an improved gain, the power consumption should also be balanced for the device allowing it to work in low power consumption levels. The uniformity in the device operation makes the device more reliable for adverse conditions such as under different Process, Voltages and Temperatures (also

known as PVT corners). To ensure the conformity with the expected results, the schematic design of the circuit is simulated in LTSpice tool using 180nm product design kit [4] (abbreviated as PDK), to avoid the leakage current as we reduce the chip size further. This improves the device performance by reducing the power consumption, leakage current, and hence improving the device speed.

1.1 Literature survey

The ever-rising popularity of OTA, in the field of low voltage application ushers the way for more research and development in the basic structure of amplifiers which desires an improved optimization in gain. A TSMC 0.35 μm MOS technology [5] was designed with a dual bulk-driven input at 0.9V supply voltage and reduced power consumption. The amplifier's open loop gain is 62 dB, where the input stage is rail-to-rail. The paper also includes a shut-down circuit which avoids the leakage current, and the risk of latch-up, making it highly suitable for the portable biomedical monitoring system and battery power devices. The input common mode range is not rail to rail, restricting the usage of the amplifier from many applications such as a rail to rail I/O swing described in [6]. A topology that combines the bulk-driven differential pair with dc level shifters with the transistors working in the weak inversion region. The circuit works on a 600-mV supply voltage which is even below the threshold voltage and provides a rail-to-rail input voltage swing, opening a completely new horizon in the field of Medical Electronics. Furthermore, it uses a set of passive elements designed to work in low-power, low-voltage applications with a gain of 69 dB [6].

To understand the application of an Operational Transconductance Amplifier (further abbreviated as OTA) in biomedical application [7] [8] [9], a PMOS input stage transistor operating in the subthreshold region [7] has proven to be more suitable than gate-driven or bulk-driven input stages. Nevertheless, biasing the input transistor in the subthreshold region can be problematic when implementing the circuit for adverse conditions where the supply voltage varies frequently. It can move the input MOS in the saturation/strong inversion region, which defeats the purpose of obtaining high transconductance necessary to obtain the required gain. The proposed circuit in [7], contains a pre-amplifier and low pass filter for attenuating higher frequency components which helps flatten the gain in the passband and attenuate the high-frequency signal with a cut-off of 100 Hz suitable for the ECG signals [7]. However, the unity gain bandwidth [7][8] is low for such a high gain application and makes the gain unstable at different process and temperatures. With an improved unity-gain bandwidth [9], the gain can be stabilized at higher temperatures. In addition, the frequency response is unsuitable for high-frequency operations such as the constant transconductance input stage [10] which affects the irregularity in total open loop gain of the amplifier. The transconductance depends upon the effective V_{gs} of the device as described in the equation below:

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{gs-effective}$$

Hence $V_{gs-effective}$ is kept constant for the NMOS and the PMOS input stage to achieve a balanced rail to rail input stage. To satisfy this criterion, [10] compares different type of devices that can keep the effective gate-source voltage constant using an ideal diode pair, and an Electronic Zener. An ideal diode conducts only in forward biased condition while an electronic Zener conducts in both forward and reverse biased conditions. An ideal Zener diode has a constant voltage V_c and it is placed between the NMOS input pair and the PMOS input pair because it satisfies the given

criterion [10] to keep the $V_{gs-effective}$ constant and hence a constant g_m. Instead of an ideal Zener diode (not used in practical applications), a diode pair can also be used to control the g_m using two diodes connected between the input pair. The aspect ratios are maintained significantly large (around 6 times the input stage transistors for the device) [10] to give voltage equal to that of the Zener voltage. The current in the diode reaches an estimated value of three-times the reference current while the input devices have a current of I_{ref}. This ensures the constant overall transconductance with approximate 23% variations [10] with the variation of the common mode input voltage. It is observed that the variation in transconductance of the input stages in the two-diode architecture is because of the transconductance (g_m) dependence on the current (I_{ref}) between them. This issue is resolved by increasing the gain of the input Zener using MOSFETs, mitigating the dependance of current variation on the g_m. This yields a better result and a more stable transconductance with a lesser deviation of 8% [10].

A similar architecture using a cost-effective 0.6um CMOS process with a gain of around 65.8 dB [11] and a rail-to-rail gate-driven input stage with lower power consumption can also be used for higher input common mode range. The proposed architecture provides constant transconductance over the common-mode range with a 6.5% variation like reference [10]. Two MOS devices connected in series in which one acts as a current source and another as a current sink [11]. The device that carries a higher current enters the triode region, and the lower current device remains in saturation. The device with lower current conducts, and the other one remains off or has the nominal value. The constant fluctuation in the total transconductance of the MOSFET is often observed because of the dependence of g_m on the difference in mobility of electrons (μ_n) and mobility of the holes (μ_p), which can be further improved by selecting W/L ratios of the n-channel

and p-channel MOS such that the beta values become equal ($\beta_n = \beta_p = \beta$) [11]. Width of the MOS devices can be modified in such a way that the ratios of W_n to W_p should be equal to $\frac{\mu_n}{\mu_p}$, if the lengths are matched. The circuit works with the least variation in the total transconductance. As depicted in [11], when current entering through any device goes to its nominal value, the transconductance shoots above the average value affecting the overall gain to a negligible value. This mostly happens due to the low input impedance (increased demand for bias current at the input) and one of the devices entering the triode region. The amplifier's input impedance is low, which limits the gain-bandwidth product and the overall gain. Therefore, an additional gain stage can further bolster the gain and the output voltage swing.

According to the rail-to-rail OTA described in [12], there can be three possible rail-to-rail OTA designs. We can either process the input stage close to the ground or positive supply voltage or both. To implement an input stage to reach the positive rail or the supply voltage, an N-channel MOSFET must be used, followed by fixing the drain voltage close to the given supply voltage. The input common mode voltage ranges from the VBS and VDSAT above the ground to the supply voltage V_{DD}. A negative/ground rail input stage for an OTA using a P-channel MOSFET should be implemented while fixing the device drain close to the ground or VSS. The input common-mode voltage ranges from ground to a voltage level which is VBS and VDSAT below the positive supply voltage V_{DD}. The above two topologies of input stages can be combined to form a complete rail-to-rail input stage which will work simultaneously even if one of the stages do not get enough input common-mode range. The only drawback in implementing a proper rail-to-rail input stage over the entire range of operation from ground/VSS to supply voltage/V_{DD} is the fluctuating

intrinsic transconductance of the transistors. The input transistors' transconductance varies in most cases, giving different gains at different input voltages which can be fixed by the topologies described [10][11]. Also, the gain of the amplifier can be divided into two stages to split the dependance of gain on the intrinsic transconductance of the input pair.

A 3-stage OTA operating on a supply voltage lower than the threshold voltage (around 0.25V rail-to-rail) [13] is designed for smartphones and wearable electronics with improved gain and the least power consumption using asymmetric self cascoded transistors which increases the output impedance with the help of source degeneration using the lower MOS device in each pair. The improved gain on a subthreshold supply voltage is a proficient way to design the circuit for low voltage applications but the number of transistors and their sizes shown in the paper [13] ($W/L_{M13} = \frac{320}{0.12} = 2{,}666$) are massively larger than usual transistors, which consequently makes the chip area larger and not suitable for applications where size is the main factor. gain can also be increased with a technique called gain-boosting [14][15], which is responsible for increasing the output impedance by adding a feedback loop, followed by the gain. The feedback amplifier is used to increase the gain by 1 and the drain-source voltage is kept as stable as possible. The amplifier increases the output impedance to a significant value using a feeder of one plus the loop gain as shown in fig. 1.1.

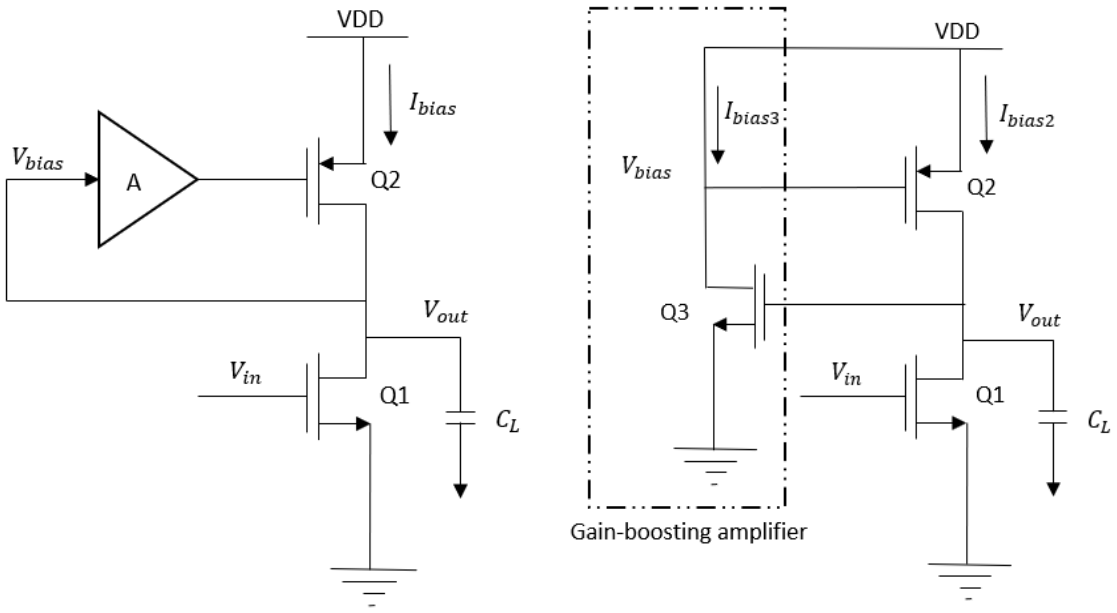


Figure 1.1: Gain boosting amplifier [14]

$R_{out}(s) = g_{m1}.r_{ds1}.r_{ds2}\ (1 + A(s))$

Gain of this stage is given by $A_v(s) = \frac{V_o(s)}{V_{in}(s)} = -g_{m1}.(R_o(s)||\frac{1}{sC_L})$. Since the output impedance is increased by a factor of (1+A(s)), therefore the gain of conventional cascoded amplifier will also increase significantly. To further enhance the gain, a parallel combination of several gain-boosting amplifiers can be cascaded, called Repetitive gain-boosting amplifiers [16]. Nevertheless, while designing an amplifier for low voltage applications one needs to consider reduction of the number of transistors between the two rails. To design a buffer amplifier for the NMOS and PMOS the number of transistors increase almost to the double of a conventional cascoded amplifier which gives rise to the depletion of voltage headroom required for biasing of each transistor at a low supply voltage thus causing the transistors to go in triode region. Hence, this type of design is good for 3V [15] and 5V applications [16] but not suitable for, which is the aim of this work, V_{DD} = 0.9 V.

A Gm-C filter is designed using 180 nm CMOS bulk-driven OTA with a THD (total harmonic distortion) of 0.057% [17]. The input common mode range is better than conventional amplifiers because of the bulk-driven input stage but the g_m variation with varied peak to peak input voltages and frequency variation is more than desired. The output frequency can still be improved by using a folded cascoded structure or a gain boosting technique [14]. A 14 dB OTA described in [18] is designed for medical applications on a 1V rail to rail supply. All the transistors used are bulk-driven and bulk to channel junctions are reverse biased so that the voltage between them control the current flow from source to drain hence it works on a very low voltage and low power consumption. The input common mode range achieved is the maximum but the effective intrinsic gain (g_{mb}) of a MOSFET is much lower than the intrinsic gain (g_m) of the gate driven MOS giving a lesser gain compared to the conventional amplifier. The paper [18] was reviewed to understand the working of a bulk driven MOSFET in an amplifier. Bulk-driven input stage is also used in Analog-to-Digital converters [19] where power consumption and low supply voltage is the main requirement. The input stage also provides a wide range of common mode input voltage using a supply voltage of around 0.8 V peak-to-peak. The gain stage uses a coupled differential pair to improve the gain 26.53 dB and reduce the power consumption to 0.44 mW [19].

Since the papers discussed earlier show that a bulk driven MOSFET provides a better common mode input range but has a lower intrinsic transconductance, therefore it is important to implement an additional gain stage differential pair for getting a better gain and output impedance. This stage can be included using a folded cascoded OTA with an additional gain of 42.78 dB [20] and a power consumption of around 13.64 uW. The amplifier can be designed based on any technology with

supply voltage of 1.8V or lower. It is observed that the folded cascoded amplifier can further give a higher gain by increasing the channel length and width proportionately taking into consideration the Channel Length Modulation effect. The increase in length of the channel will decrease the drain current and further increase the output resistance of the MOS to improve the overall gain of the circuit. This brings to the fact that one can does not achieve all the parameters simultaneously, there will always be a trade-off between gain, bandwidth, and supply voltage of the circuit. If we increase the gain, bandwidth will deteriorate. On the other hand, if we reduce the supply voltage for low voltage applications, it will be hard to achieve higher transconductance values from smaller transistors with a perfect biasing.

In contrast to the work [10][11], in this research, an attempt has been made to achieve a rail-to-rail OTA with the supply voltage as low as 0.9V and a gain as high as 97dB while maintaining an output gain which varies only 4.1% as a function of input voltage. This stable operation is achieved without the need of stabilizing the bulk transconductance of the input MOS pair. Moreover, a moderately good gain-bandwidth product of 8Mhz is achieved. With low voltage, the power consumption is also optimized for the OTA to work on lower power consumption levels. However, when scaling down the technology, the subthreshold leakage, and the gate leakage current increases [26] which further increases the power consumed by the device. To elaborate, static and dynamic are the two types of power consumptions in a MOS circuit. Static power consumption is the power consumed by the subthreshold leakage current which should be minimal. Dynamic power consumption keeps changing with the device parameters and this is the power consumption which should be more than the static power consumption [27] to minimalize the leakage current

and redundant power consumed by the circuit due to leakage. Therefore, 180nm technology is used rather than other available technologies (45nm, 65nm).

1.2 Thesis outline

A brief explanation of the principle of operation of MOS transistors is described in Chapter 2, which includes a variety of configuration techniques for single-stage amplifiers using NMOS and PMOS transistors. Chapter 3 states the method and approach of this thesis to overcome the issues of gain in bulk-driven OTA for low-voltage applications. Moreover, an explanation to understand the basics of generic OTA is provided with an approach to produce high open loop gain with the lower supply voltage and a better dynamic range. Finally, an additional circuit architecture is proposed for biasing of the second-stage OTA to improve the output swing.

The calculations for designing a 2-stage OTA to produce a gain-bandwidth product of 8 MHz and a slew rate of 0.05 V/uS are shown in Chapter 4. In addition, the calculation includes the derivation of the formulae for the transfer function, open-loop gain, phase margin, slew rate and aspect ratios of each MOS transistor. The dynamic range is further calculated using the results from calculations and LTSpice simulation. Chapter 5 shows all the simulations and compares the results from the calculations (in Chapter 4). Moreover, operating points are presented to confirm the expected results with the obtained simulations. Finally, Chapter 6 summarizes work done and its potential contribution towards the practical applications of OTA with low voltage low power applications compared to the earlier research in similar designs, including the future scope and advancements of this research.

Chapter 2 Background knowledge

2.1 IV characteristics of the NMOS

We start with a brief description of the DC characteristics of the NMOS to elaborate the impact of the change in drain to source voltage V_{DS} on drain current I_D with different values of V_{GS}.

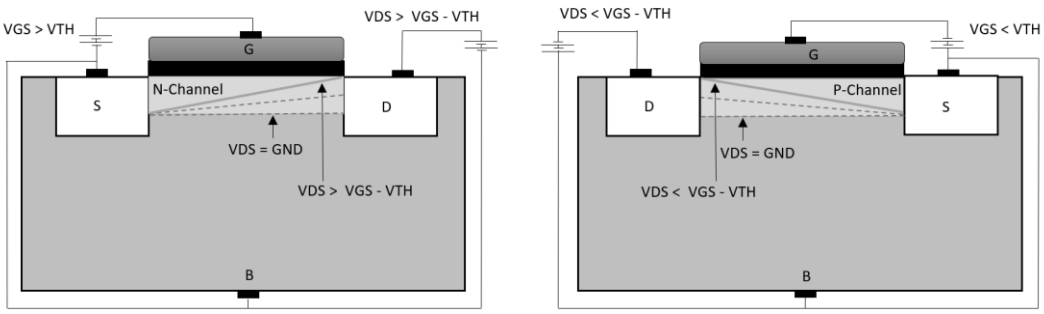


Figure 2.1: Cross-section of a) NMOS b) PMOS [36]

Figure 2.1 shows the cross-sectional view of (a) NMOS structure with the inverted layer (n-channel) and (b) PMOS structure with the inverted layer (p-channel).

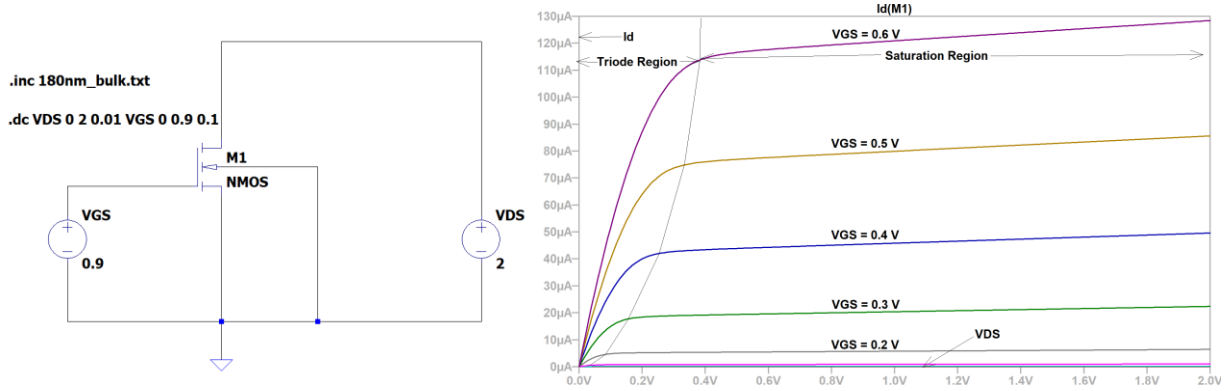


Figure 2.2: a) Biasing of 180nm NMOS b) Simulation for DC characteristics in LTSpice

The NMOS is operating in the saturation region when the drain current becomes almost independent of the drain-to-source voltage and starts acting like a constant current source, whereas

in PMOS, the voltage relation $V_{DS} \leq V_{gs} - V_{th}$ needs to be satisfied for it to operate in saturation region. In the proposed circuit, all the MOS devices are operating in the saturation region for amplifier application with a certain intrinsic gain and output resistance. The triode and saturation regions are shown in Figure 2.2, for the 180nm technology used in this work. We have analyzed the output current magnitude with different input voltages (V_{gs} = 0.2-0.6 V) and a fixed drain to source voltage (V_{ds}). In the next section, different existing configurations are shown for a MOS to work as a single stage amplifier.

2.2 Single stage amplifier

A single MOS transistor can be used either as a voltage controlled current amplifier (in Saturation region) or a resistor (in triode region). There are three basic types of configurations for a MOS device to amplify an input voltage signal: Common-source (CS) amplifiers, Common-drain amplifier, and a Common-gate amplifier. A CS amplifier can be designed with a resistive load, or a diode-connected load, or a current-source load, or an active load, or a triode load or a source-degeneration resistor.

2.2.1 CS stage with resistive load

As illustrated in Figure 2.3a, M1 is Off initially. As V_{in} increases from 0 ($V_{out} = V_{DD}$) till the input voltage reaches a threshold at this point V_{out} is maximum. When V_{in} approaches V_{th}, V_{out} starts drawing the current from the resistor (R_D), and the transistor is said to reach the saturation region

where drain current becomes independent of the input voltage V_{in} ($= V_{gs}$). The output voltage is formulated by applying KVL to the circuit shown in equation 2.1.

$$V_{out} = V_{DD} - I_D R_D = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{in} - V_{th})^2 \quad (2.1)$$

If we keep increasing V_{in} further, the V_{out} draws more current from R_D, and the V_{out} keeps lowering (i.e., $V_{in1} = V_{out} + V_{th}$).

$$V_{in1} - V_{th} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{in1} - V_{th})^2$$

Further increasing $V_{in} > V_{in1}$, M1 goes to the triode region where V_{out} is represented by:

$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox} \frac{W}{L}[2(V_{in} - V_{th})^2 . V_{out} - V_{out}^2] \quad (2.2)$$

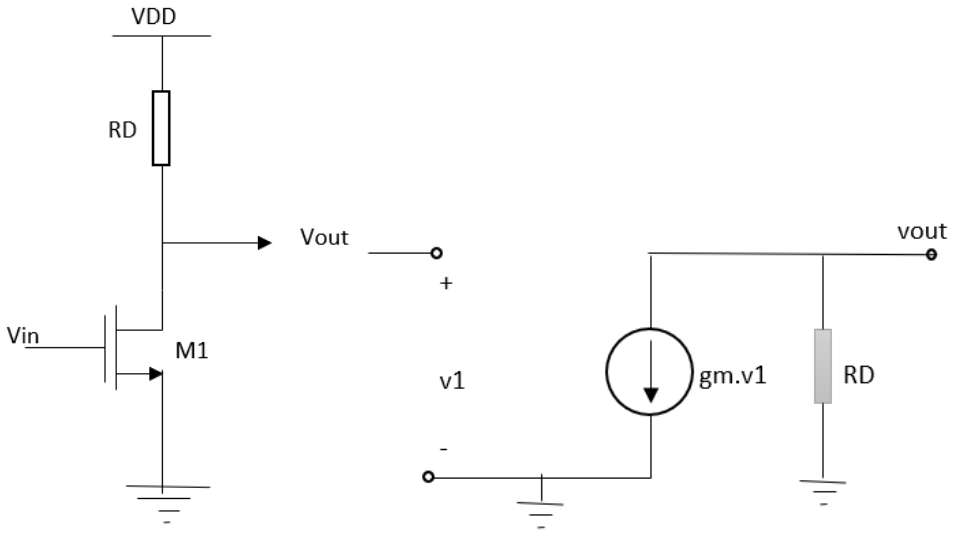


Figure 2.3: a) Common-source (CS) amplifier with resistive load b) AC analysis [36]

Small signal gain of the CS amplifier (fig.2.3b) with a resistive load amplifier is shown below:

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = -R_D \mu_n C_{ox} \frac{W}{L}(V_{in} - V_{th}) = -g_m R_D \quad (2.3)$$

Therefore, $V_{out} = -g_m V_1 R_D$ (2.4)

The transistor has an intrinsic output impedance (r_o) that impacts the intrinsic gain of the device,

$A_v = -g_m(R_d||r_o)$ (2.5)

Instead of gate terminal, if the bulk is controlling the channel, i.e., if the input is applied on the bulk rather than the gate, then gain of the device, $A_v = -g_{mb} R_D$ (2.6)

$I_d = g_{mb}.V_{in}$ (2.7)

It can be observed that as input voltage increases, drain current also increases and the output voltage V_{out} keeps decreasing. Hence, for the MOSFET to operate in saturation region for amplification, the input voltage should be in the range of V_{th} to $V_{out} + V_{th}$.

2.2.2 CS stage with diode connected load

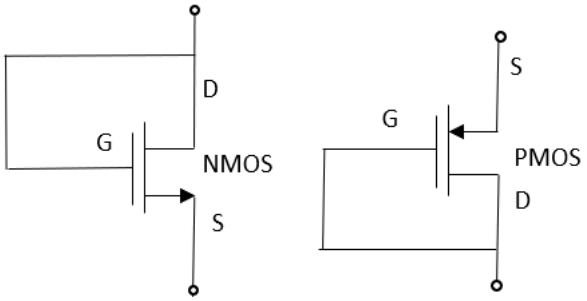


Figure 2.4: Diode connected a) NMOS b) PMOS

In a diode-connected stage, the gate and drain of the transistors are shorted together to operate as a small signal resistor. This forces the transistors to be in the saturation region as the gate and drain terminals are at the same potential. We already know that V_{ds} should be greater than or equal to

$V_{gs} - V_{th}$ for the device to be in saturation region. If $V_{ds} = V_{gs}$, V_{ds} will always be greater than $V_{gs} - V_{th}$. According to the AC circuit of diode-connected load in fig. 2.5,

$$V_1 = V_x$$

$$I_x = \frac{V_x}{r_o} + g_m V_x$$

Impedance = $\frac{V_x}{I_x} = {}^1/_{g_m} \,||\, r_o \approx {}^1/_{g_m}$

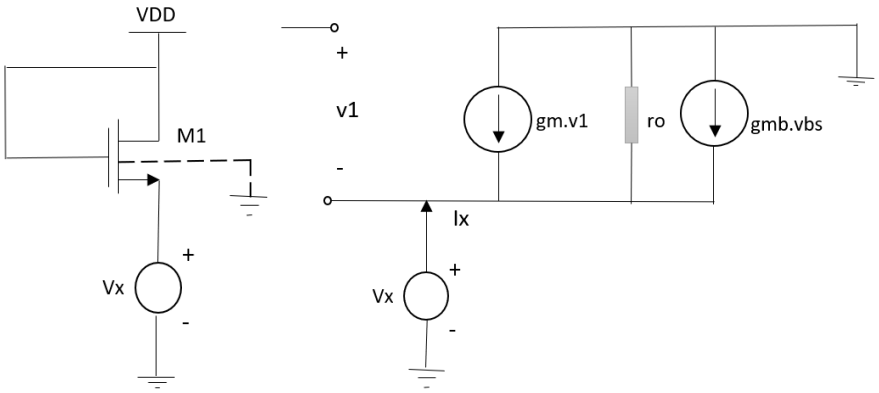


Figure 2.5: a) CS stage with diode connected load circuit b) AC circuit [36]

With the body effect:

$$V_1 = -V_x = V_{bs}$$

Impedance = $\frac{V_x}{I_x} = {}^1/_{g_m + g_{mb}} \,||\, r_o \approx {}^1/_{g_m + g_{mb}}$ (2.8)

2.2.3 CS stage with current source load

To obtain a large voltage in a single step, we need to increase the load impedance of the common source stage. In the previous two configurations, increasing the load resistor translates to a drop of

dc voltage across the load, which limits the output voltage swing. This phenomenon occurs due to ohms law. Hence, a CS stage with the current source load is suggested because both devices do not follow ohms law. According to Figure 2.6,

Total impedance = $r_{o1}||r_{o2}$

Gain, $A_v = -g_{m1}(r_{o1}||r_{o2})$ (2.9)

$|V_{DSmin}| = |V_{ds2} - V_{th2}|$ (2.10)

Lambda, $\lambda \propto {}^{1}/_{L}$ (2.11)

$r_o \propto {}^{L}/_{I_d}$ (2.12)

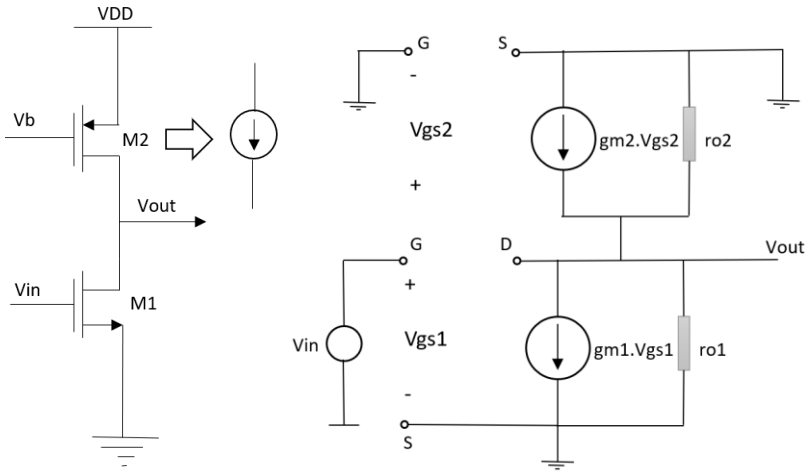


Figure 2.6: a) Circuit for CS stage with current source load b) AC analysis [36]

For low voltage applications, V_{DSmin} can further be minimized by simply increasing the width of M2. If r_{o2} is not high enough, then the length and width of the transistor M2 should be increased to achieve smaller lambda (maintaining the same overdrive voltage). If L1 is scaled up, the W1 should be scaled up proportionately because $V_{gs1} - V_{th1} \propto \frac{1}{\sqrt{W1/L1}}$. Hence, if the L and W are

not scaled up together, the overdrive voltage can increase, limiting the output voltage swing. Compared to a resistive load, a current source load provides a minor voltage swing, but one can achieve a higher gain by increasing the L1 and L2. This configuration is suitable for designing the second stage of an OTA which is discussed in section 3.4.

2.2.4 CS stage with active load (complementary CS)

Instead of using PMOS as the current source load in the previous configuration, we can apply the input voltage to the PMOS and convert it to an Active load (shown in Figure 2.7). Suppose both transistors are in saturation, V_{in} increases by a change in the output voltage. As I_{d1} increases, V_{out} drops because M2 injects lesser current in the output.

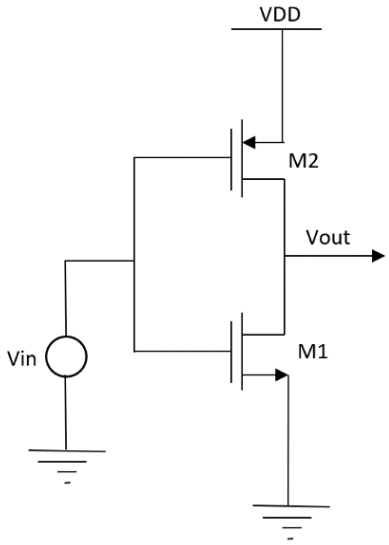
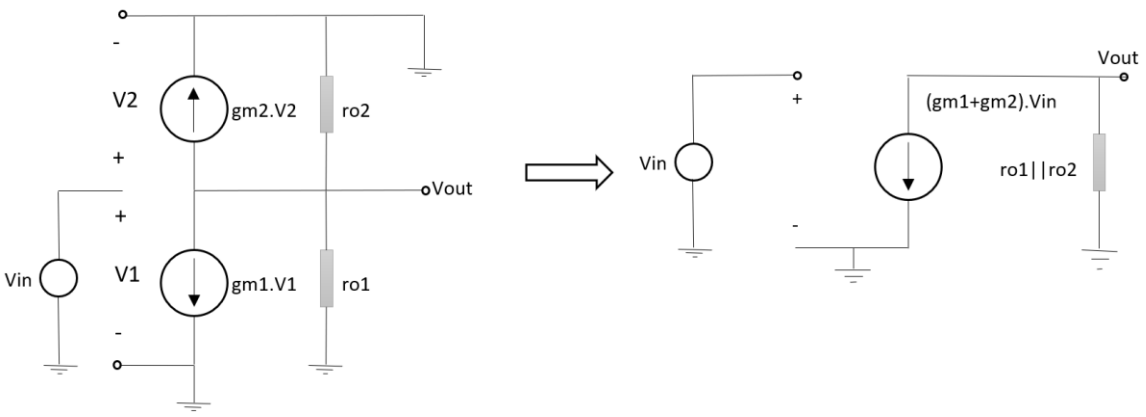


Figure 2.7: Complementary CS stage [36]



(a) *(b)*

Figure 2.8: a) Small-signal analysis for complementary CS stage b) Equivalent circuit [36]

Applying KVL to fig. 2.8:

$$V_{out} = -(g_{m1} + g_{m2}).V_{in}.(r_{o1}||r_{o2}) \tag{2.13}$$

Therefore,

$$\text{Gain, } A_v = \frac{V_{out}}{V_{in}} = -(g_{m1} + g_{m2}).(r_{o1}||r_{o2}) \tag{2.14}$$

Compared to the previous configuration, this has the same output impedance but a higher transconductance. This is a good configuration when size of the chip can be large because the number of transistors can be sufficiently large in design of a second stage OTA. Moreover, bias current is a vital function of the PVT variations. According to the figure 2.7, $V_{gs1} + |V_{gs2}| = V_{DD}$. Therefore, V_{gs} will vary if the V_{DD} fluctuates which leads to a change in the drain current. This makes the circuit unstable for any change in the supply voltage due to any fluctuation in process or voltage.

2.2.5 CS stage with triode load

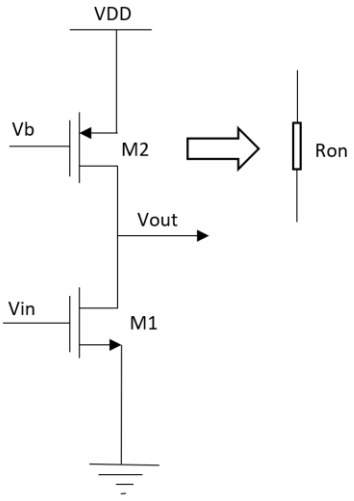


Figure 2.9: CS stage with triode load

In this configuration, the PMOS is kept in the triode region to act as a resistive load. The gate of M2 is biased to a sufficiently lower level to ensure that the load is in the triode region for the entire output voltage swing. The channel resistance of a MOS in triode region is represented as:

$$R_{on} = \frac{1}{\mu_p C_{ox} \cdot \frac{W_2}{L_2}(V_{DD} - V_b - |V_{THP}|)} \tag{2.15}$$

Ron depends on the $\mu_p C_{ox},\ V_b,\ and\ V_{thp}$ that varies with the process and temperature. Moreover, for keeping M2 in triode region one needs to generate precise value for V_b, which needs an additional complexity in the circuit. This is challenging to design in the practical application for smaller number of transistors, making the circuit less popular in the field of OTA design.

2.2.6 CS stage with source degeneration

The non-linear dependence of drain current (I_D) on the overdrive voltage ($V_{gs} - V_{th}$) introduces a nonlinearity, making it desirable to soften the device characteristics. CS stage with diode connected load allows post-correction of this nonlinearity. A "degeneration" resistor in series with the source terminal of the MOS is another way to make the input device more linear.

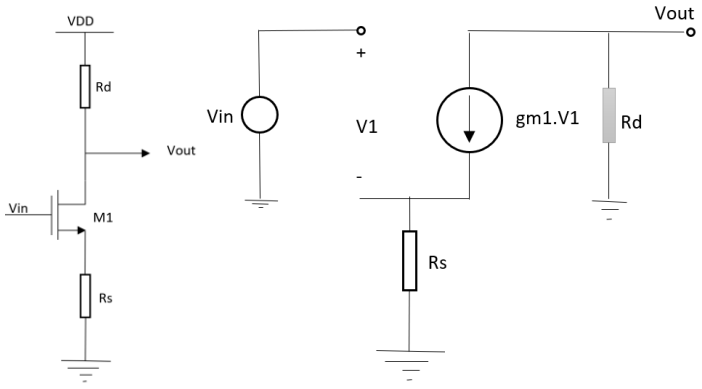


Figure 2.10: a) CS stage with source degeneration b) AC analysis [36]

As V_{in} increases, the drain current I_d and voltage across R_s increases simultaneously. Therefore, a fraction of change in the input voltage appears across the resistor rather than the gate-source overdrive. This softens the device characteristics by adding negative feedback to the circuit making a smoother variation of I_d.

According to KVL in Figure 2.10a,

Output voltage, $V_{out} = V_{DD} - I_D.R_D$ (2.16)

Non-linearity dependence of I_d on V_{in}: $\frac{dV_{out}}{dV_{in}} = -\frac{dI_d}{dV_{in}}.R_D$ (2.17)

Equivalent Transconductance, $G_m = \frac{dI_d}{dV_{in}} = \frac{g_m}{1+g_m.R_s}$ (2.18)

If R_s increase, G_m becomes a weaker function of g_m and I_D.

Gain, $A_v = \frac{-g_m R_D}{1 + g_m R_s}$ (2.19)

Applying KVL to the small signal circuit in fig. 2.10b, $V_{in} = V_1 + I_d R_s$ $(where, I_d = g_m V_1)$

Hence, most of the change in V_{in} appears across the R_s, and the drain current is linearized at the cost of lower gain and higher noise.

2.2.7 Source follower (Common-drain stage)

The common-source stage is suitable for achieving a high voltage gain with a limited supply voltage and an enormous output impedance. But a common-drain stage is used to drive a low impedance load with negligible reduction in gain. It is often used as a buffer placed after the amplifier to drive a low impedance.

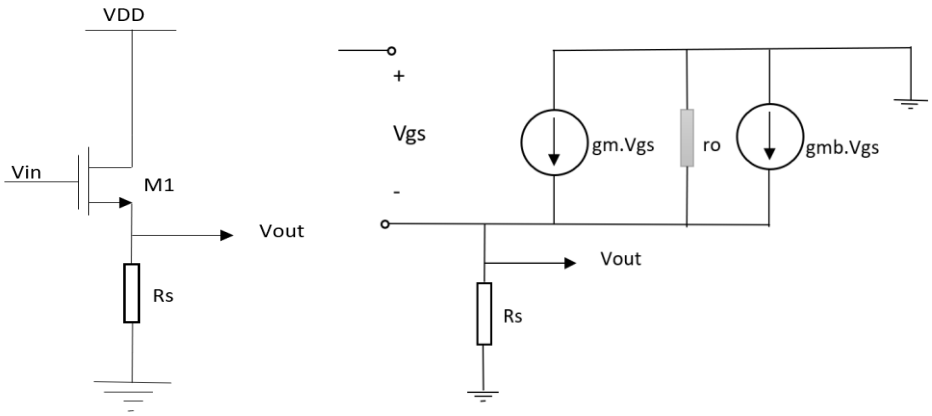
Applying KVL to fig. 2.11:

$V_{in} - V_1 = V_{out}$

$V_{bs} = -V_{out}$

$g_m V_1 - g_{mb} V_{out} = \frac{V_{out}}{R_s}$

Gain, $A_v = \frac{Vout}{Vin} = \frac{gm.Rs}{1+(gm+gmb)Rs}$ (2.20)



(a) *(b)*

Figure 2.11: a) Source follower configuration b) AC analysis [36]

According to the gain equation, even if Rs = infinity, the voltage gain of the source amplifier is not equal to 1. The resistor is replaced with a constant current source shown below to overcome this problem.

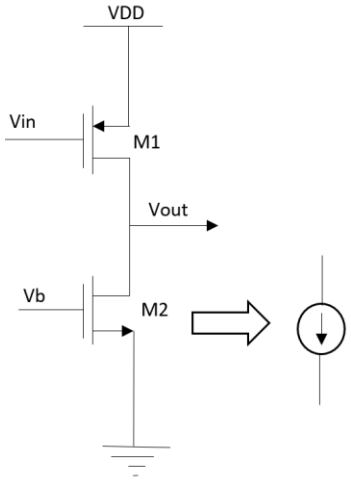
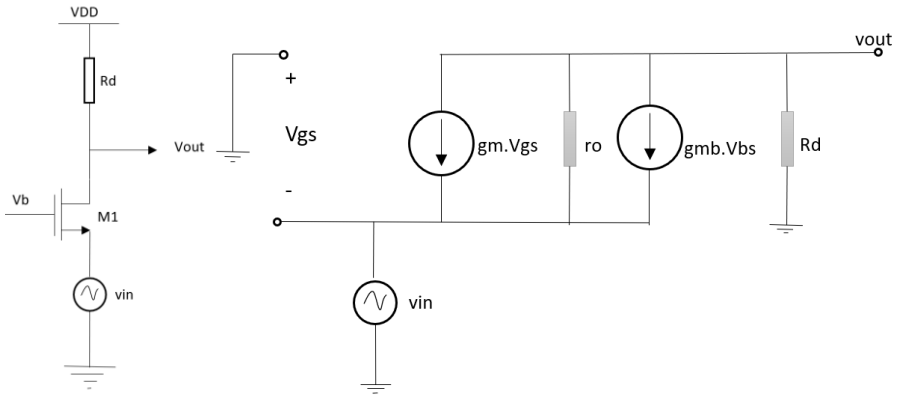


Figure 2.12: Source follower with constant current source

Hence, a source follower exhibits a high input impedance and a moderate output impedance at the cost of nonlinearity and voltage headroom limitation.

2.2.8 Common gate stage



(a) *(b)*

Figure 2.13: a) Common-gate circuit b) AC analysis [36]

A common-gate stage senses the input at the source and produces the output at the drain. Gate is connected to a DC voltage to ensure proper biasing such as a current mirror, voltage level shifter or any external DC biasing circuit. Gain of the device is positive, and the input impedance is comparatively lower than the CS stage and source follower stage. Although the input impedance of the CG stage can be increased by applying a bigger load resistor.

Chapter 3: Method and approach

3.1 Understanding the working of a generic OTA

An Operational Transconductance Amplifier (OTA) is the building block for many Analog and mixed-signal systems. The main feature of a transconductance amplifier is to convert the input voltage into a current output. The different levels of complexity in the design of an OTA are used to realize functions ranging from high amplification to a significant slew rate and smaller chip area [22]. The juxtaposition of different features of an OTA (like high gain, high slew rate, lesser chip area, higher input common-mode range) leads to a constant room for research and development in this specific area of Analog circuit design.

A traditional OTA design comprises two input voltages, an amplifier responsible for the transconductance (Gm) and an amplified output current. Output current is directly proportional to the difference in the two input voltages.

$$I_{OUT} = G_m.(V_{in}^{+} - V_{in}^{-}) \tag{3.1}$$

General input-output characteristics of an OTA are shown below. In a generic OTA, the width of the linear region is inversely proportional to the amplifier's transconductance. Thus, higher the transconductance, the lower the width of the Linear/Ohmic Region (Fig. 3.1). Ideally, an OTA should have infinite input impedance for maximum utilization of input voltage by the OTA, and infinite output impedance allows an efficient transfer of output current to the load.

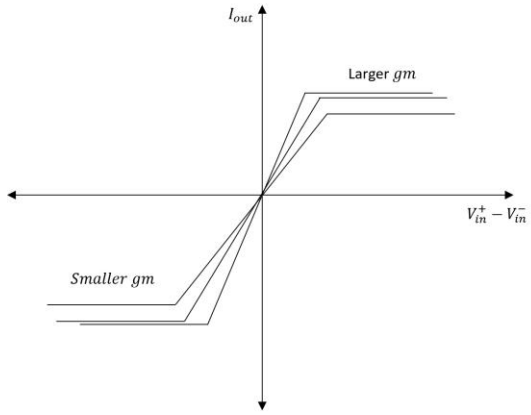
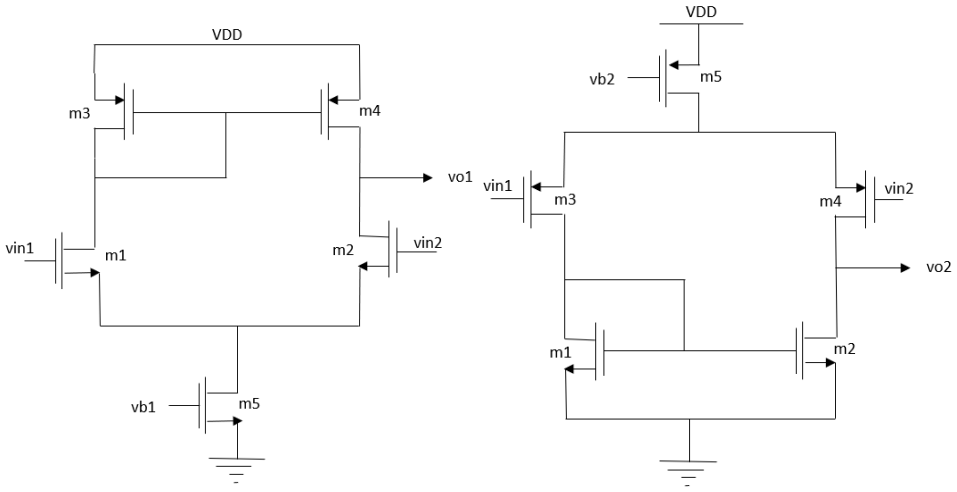


Figure 3.1 I/O characteristics of generic OTA [22]



(a) *(b)*

Figure 3.2 a) NMOS input OTA b) PMOS input OTA

Figure 3.2 illustrates the two standard topologies of OTA. First one is the NMOS input and the second one is the PMOS input. The common mode range in an NMOS input can go as high as V_{DD} but it has problem in going low towards V_{SS}. While in an PMOS input OTA the input common mode range can go even below low as V_{SS} but have problem to go higher voltage level towards

V_{DD}. At the same circuit configurations, the first one has the advantage over the PMOS input OTA in terms of high gain.

$$A_{vn} = g_{mn}(r_{o2}||r_{o4}) \quad (3.2a)$$

$$A_{vp} = g_{mp}(r_{o2}||r_{o4}) \quad (3.2b)$$

As we know that intrinsic gain (g_m) of NMOS is larger than the PMOS because of higher electron mobility, thus $A_{vn} > A_{vp}$. Hence, we choose the NMOS input transistor for better gain with a lower input common mode range while we use PMOS input pair for the device to operate on a low input voltage and a much better input common mode range. To run the device on low supply voltages we often use bulk-driven MOS transistors [1] which gives a comparatively lower gain but can operate on the input voltage as low as 0V. A bulk-driven transistor operation is discussed next in the section 3.2.

3.2 Bulk-driven input stage

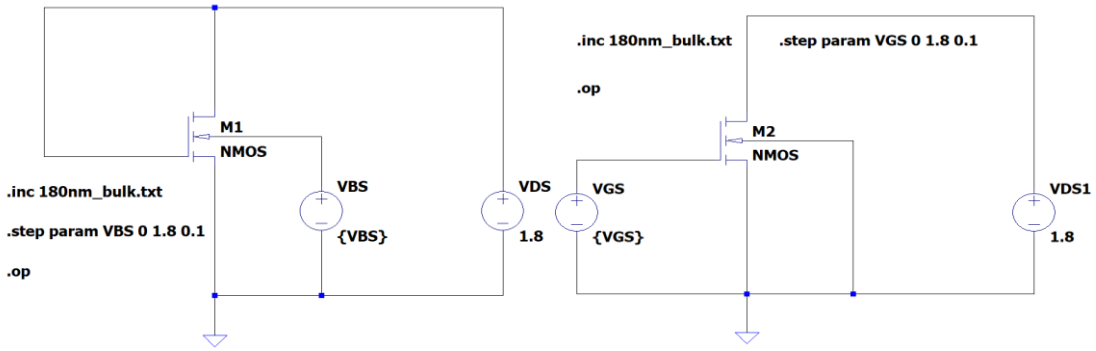
In a conventional OTA, we mainly use a gate-driven input stage to achieve better performance with the least complexity in the circuit. In medical applications, OTA is designed to operate under low bias and with lower supply voltage. The bulk terminal is often ignored in circuit design because it is tied to the source terminal to avoid the Body Effect; it is because of the change in threshold voltage when there is a potential difference between the source and body terminal. This phenomenon has been exploited in many gives' applications utilizing the bulk terminal as another

gate terminal with the intention of changing effective device threshold voltage (V_T). The equation [18] represents this effect:

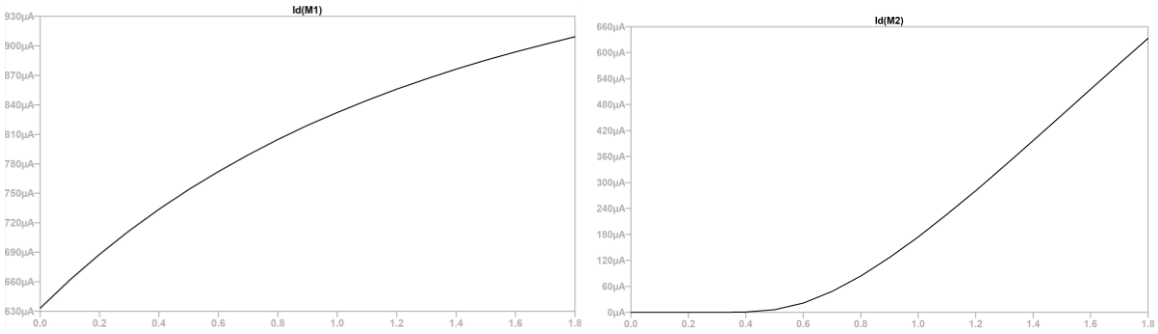
$$V_T = V_{T0} + \gamma[\sqrt{2.\emptyset_F + V_{BS}} - \sqrt{2.\emptyset_F}] \quad (3.3)$$

Where γ is the body bias factor, V_{BS} is bulk to source voltage and $\emptyset_F$ is the surface potential of the device. According to the above equation, one can easily control the device using the change of body to source voltage. V_{BS} is directly proportional to the device's V_T, i.e., the MOSFET's threshold voltage will change according to the applied input voltage at the bulk of the device. This topology allows the input voltage to be as minimal as possible to work in the strong-inversion region (saturation). In bulk driven MOSFET, the gate of PMOS is connected to the ground, and the gate of NMOS is connected to the positive supply voltage.

The simulation in figure 3.3 shows the DC characteristics of both the gate-driven and the bulk-driven input stages. According to the observation, the gate-driven NMOS enters the saturation region after a threshold of around 0.5V on a given power supply of 1.8V, which causes a limitation in the application of a low input voltage circuit application. For this purpose, we use a bulk-driven input stage which enters the strong inversion region on input as low as 0V producing a massive output drain current (around 9.09e-04 A) as compared to the former (around 6.33e-04 A). Bulk-driven MOS (g_{mb} = 7.15e-05) is much less than the gate-driven MOS's transconductance (g_m = 5.80e-04) shown in Figure 3.3e. The difference in the g_m of M2 and g_{mb} of M1 proves that bulk-driven devices are not the best suited [25] for acquiring a high gain with a least leakage current [27]. Hence, for obtaining higher gain a gate driven gain stage [25] is designed to further optimize the gain [28][29][30][31].



(a) *(b)*



(c) *(d)*

Semiconductor Device Operating Points:

	--- BSIM3 MOSFETS ---	
Name:	m2	m1
Model:	nmos	nmos
Id:	6.33e-04	9.09e-04
Vgs:	1.80e+00	1.80e+00
Vds:	1.80e+00	1.80e+00
Vbs:	0.00e+00	1.80e+00
Vth:	4.46e-01	1.62e-01
Vdsat:	9.90e-01	1.01e+00
Gm:	5.80e-04	6.35e-04
Gds:	1.84e-05	2.42e-05
Gmb	3.00e-04	7.15e-05
Cbd:	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00
Cgsov:	2.73e-15	2.73e-15
Cgdov:	2.70e-15	2.70e-15
Cgbov:	0.00e+00	0.00e+00
dQgdVgb:	3.66e-14	3.77e-14
dQgdVdb:	-2.71e-15	-2.72e-15
dQgdVsb:	-3.27e-14	-3.58e-14
dQddVgb:	-2.74e-15	-2.74e-15
dQddVdb:	2.74e-15	2.75e-15
dQddVsb:	7.85e-18	-9.14e-18
dQbdVgb:	-5.11e-15	-6.20e-15
dQbdVdb:	-1.00e-17	-1.65e-17
dQbdVsb:	-4.18e-15	4.80e-15

(e)

Figure 3.3 a) Bulk-driven NMOS b) Gate-driven NMOS c) I/V characteristics of bulk-driven NMOS d) I/V characteristics of gate-driven NMOS e) Operating point of m1 and m2 in LTSpice

A bulk-driven input stage can have either PMOS as the input or NMOS. Both has their advantage when one wants to increase the input voltage range as shown in the Fig. 3.4. A PMOS input stage gives a voltage headroom from ground to $V_{DSAT} + V_{BS}$ below the supply voltage while the NMOS input stage acts in a reverse manner and only allows $V_{DSAT} + V_{BS}$ above the ground to the supply voltage. To design a rail-to-rail circuit, both the above-mentioned input stages are clustered together to achieve the best possible input range and voltage headroom from ground to V_{DD}. The combination of NMOS and PMOS input stage improves the input dynamic range [25] and the intrinsic bulk-transconductance of the devices. In the mid-input range (between $V_{DSAT} + V_{BS}$ above the ground and $V_{DSAT} + V_{BS}$ below the supply voltage) both the devices are in active which ensures a better g_{mb} for the input transistor and further increases the gain of the first stage.

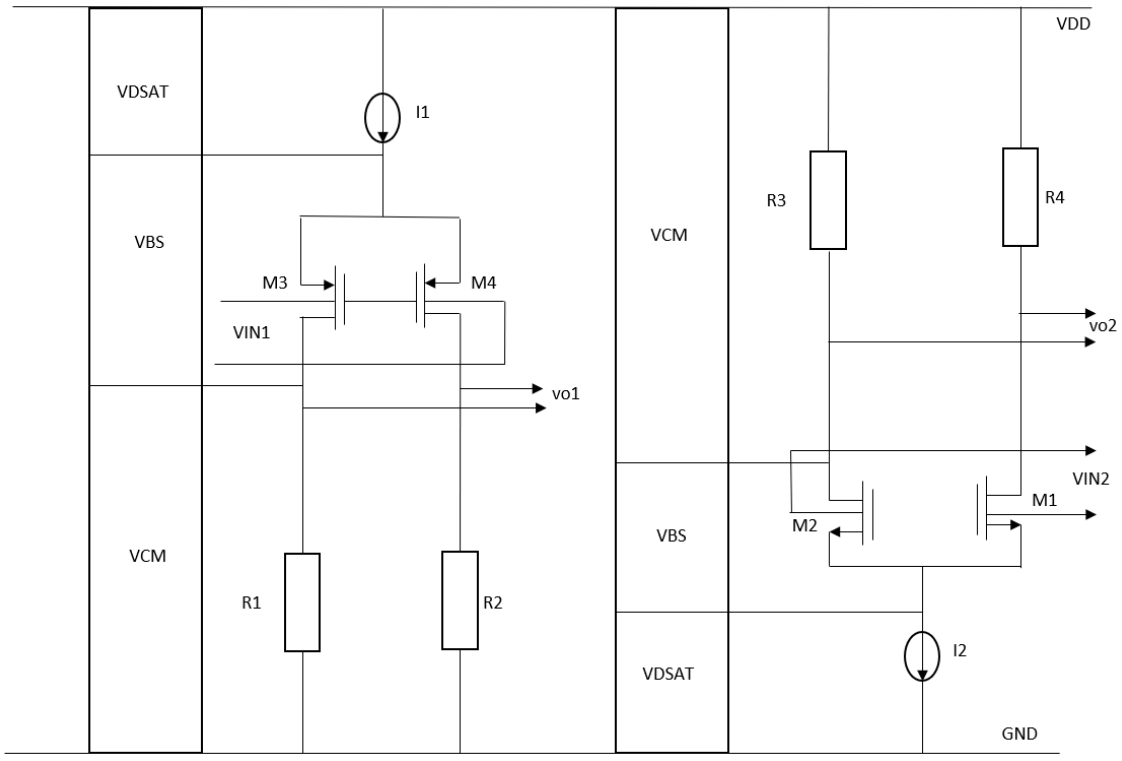


Figure 3.4 Input common mode range for PMOS and NMOS bulk-driven input stage

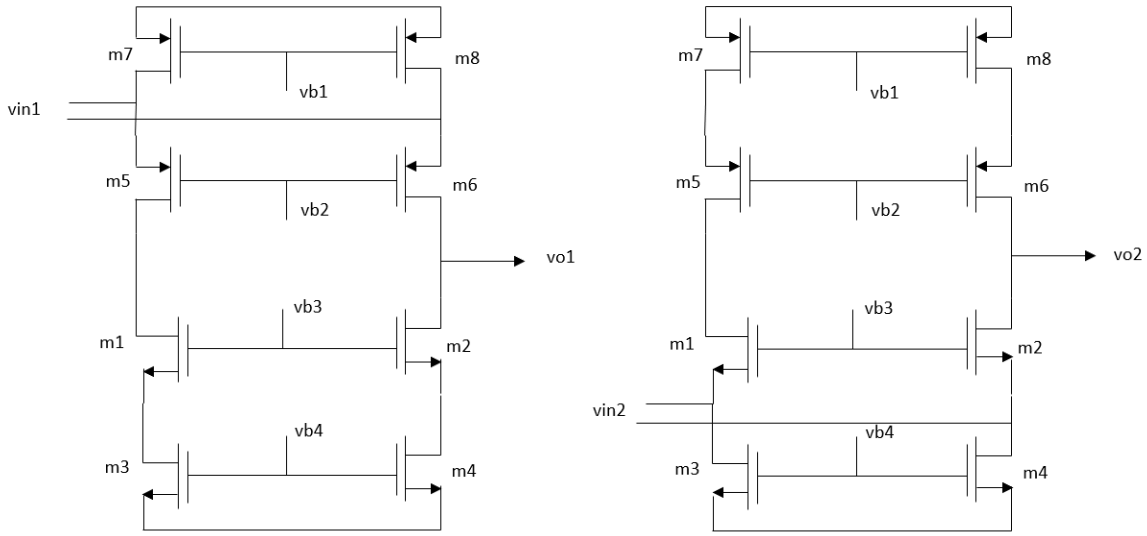
Hence, in this thesis bulk-driven device is used only as an input stage [32][33], making the circuit work on a very low input voltage, ideal for low voltage applications. In addition, there can be several types of gate-driven differential pair amplifiers which can be connected to the bulk-driven input pair to get a folded cascoded amplifier with a minimal input voltage to gain a much higher output impedance and in turn increase the total gain of the first stage.

3.3 Folded cascoded gain stage

The generic OTA discussed in section 3.1 is good for gate driven input stage but gives a poor gain when the device is bulk driven because of the low output impedance. Folded cascoded amplifier [8] is a very good approach in designing an amplifier to achieve a massive gain even if the input stage is not efficient to give a high intrinsic transconductance. In a folded cascoded amplifier, the gain depends on the intrinsic gain of the input stage and the output impedance of the gate-driven transistors of the OTA. Output impedance of an NMOS is calculated by the following equation:

$$r_o = \frac{I_D}{V_{DS}} = \; I_D = \frac{\frac{\mu_n . C_{ox}}{2} . \frac{W}{L} . (V_{GS} - V_{TH})^2}{V_{DS}} \tag{3.4}$$

Since the g_{mb} for input stage is comparatively lower than the g_m, we increase the output impedance of the transistors by increasing the W/L ratio of the transistors. Using the equation of ro, we can easily tweak (increase) the width of the transistor to increase the ro and hence the gain of the first stage. Figure 3.5 shows the cascoded differential pair with a NMOS input and a PMOS input for application in different input common mode range. Improved gain also improves the operating frequency and unity gain bandwidth of the amplifier. A proper calculation of gain and output impedance is shown in section 4.1.



(a) *(b)*

Figure 3.5 Folded cascoded OTA with a) NMOS input b) PMOS input

Fig 3.6 shows the bulk-driven rail-to-rail input stage with a folded cascoded gain stage amplifier which ensures low voltage operation of the OTA with a larger gain as desired. R1, R2, R3, R4 can further be replaced by MOS devices acting in saturation region and the current sources can be replaced by constructing current mirror using NMOS and PMOS. M1, M2 are responsible for the upper half of the input range amplification while M3, M4 are used for amplification in the lower half of the input voltage. Since M1, M2, M3, M4 play a crucial role in gain, the W/L ratio of the MOS is kept massively large to get an intrinsic transconductance like that of a gate-driven MOS. As a result, the input devices conduct from ground to V_{DD} achieving a high gain with the least variation in the transconductance.

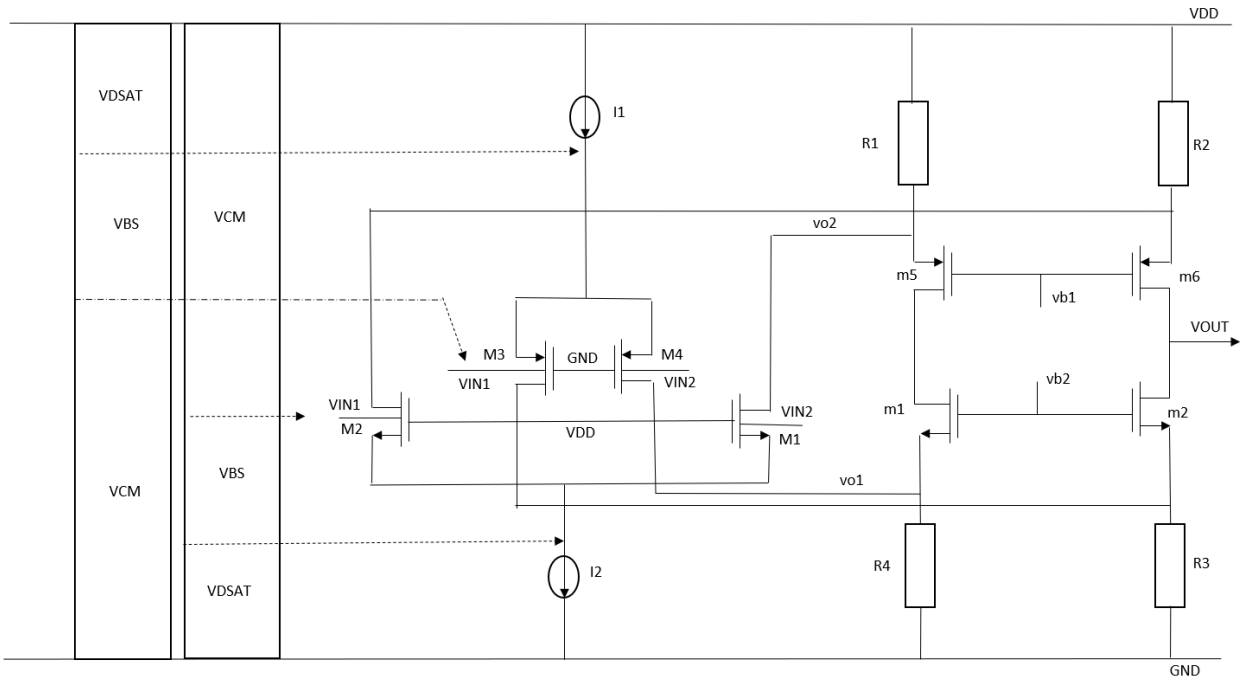
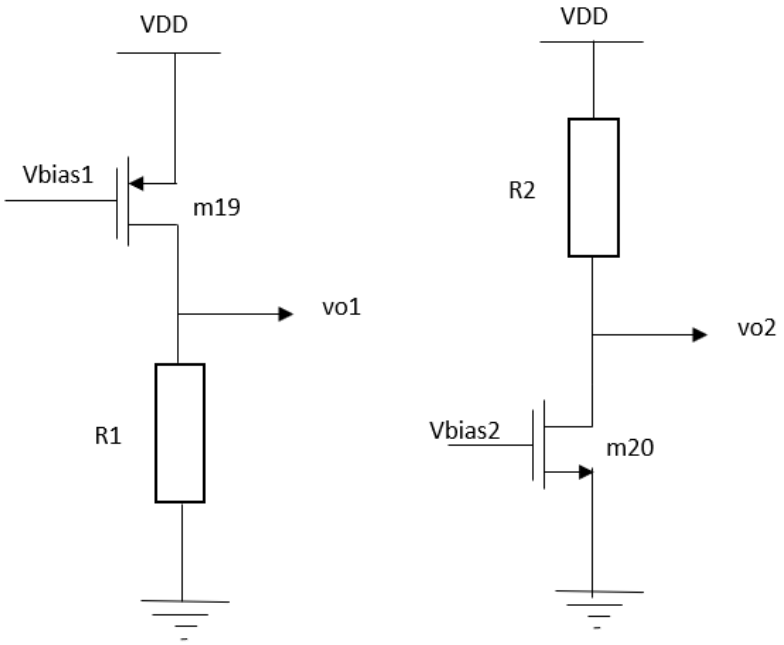


Figure 3.6 Folded cascoded OTA with bulk-driven rail-to-rail input

3.4 Second stage for OTA

As discussed earlier, gain of the single stage op-amp is solely dependent on the intrinsic transconductance of the input pair and the output impedance of the folded-cascoded amplifier limiting the gain and the output swing which is not adequate for high gain applications of the op-amp. The second stage of the amplifier is implemented to further increase the gain and give a better output voltage headroom. As discussed earlier in chapter 2, common source amplifier is more suitable for designing the second stage of the OTA to improve the output voltage swing. Fig 3.7 shows a generic common source amplifier using a PMOS and an NMOS.



(a) *(b)*

Figure 3.7 Common-source amplifier using a) PMOS b) NMOS

The output swing of the second stage is totally dependent on the overdrive voltages of the transistors in the cascoded differential pair from the first stage.

V_{DD} – Overdrive voltage of the transistor

To elaborate, let's compare the overdrive voltages of CS amplifier using NMOS vs PMOS,

$$I_D = \frac{1}{2}\mu_{n,p}C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \tag{3.5}$$

$$V_{OD} = V_{GS} - V_{th} = \sqrt{\frac{2I_D}{\mu_{n,p}C_{ox}\frac{W}{L}}} \tag{3.6}$$

According to the equation above, overdrive voltage is dependent on the W/L ratio of the device which is more in case of PMOS device. Hence, PMOS common source amplifier gives the least overdrive voltage giving a higher voltage swing. Therefore, using an NMOS CS amplifier is not

suitable for this type of cascoded circuit as it gives lower output swing as compared to PMOS CS amplifier. As illustrated in Fig. 3.8, the PMOS M19 can be used with an NMOS as a current source load M20. If the output resistance (r_{020}) is not high enough, then the length and width of the transistor M20 should be increased to achieve smaller lambda, maintaining a good overdrive voltage. L20 and W20 be scaled up proportionately as $V_{gs} - V_{th}$ h $\propto \frac{1}{\sqrt{W/L}}$. Hence, if the L and W are not scaled up together, the overdrive voltage can increase, limiting the output voltage swing. Hence the W/L ratio of M20 is designed to scale up the current in the branch and produce a good overdrive voltage for an optimum voltage swing. Gain of the second stage is dependent on transconductance of M19 in figure 3.8 which requires the transistor to be larger than the transistor used as a current source load.

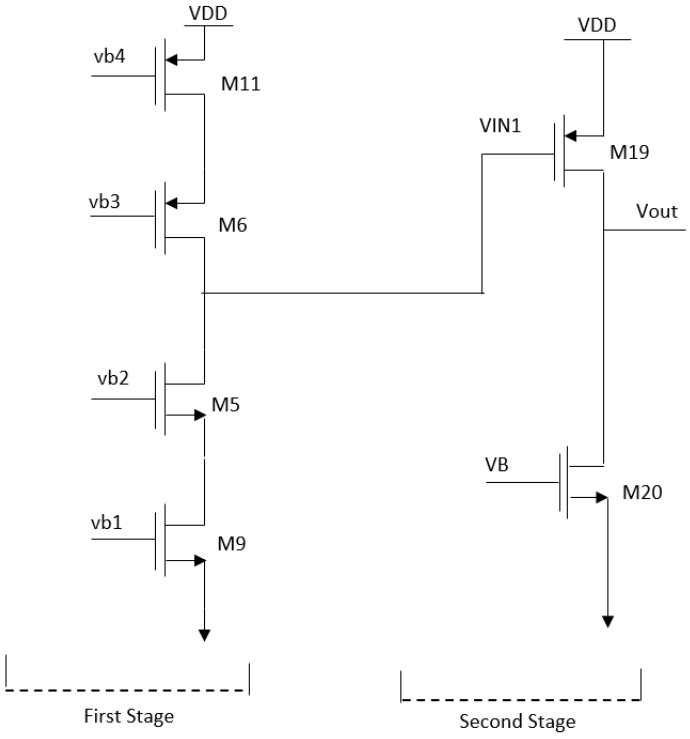


Figure 3.8 Second stage for the OTA using a PMOS common source configuration with current source load

It can be seen in the equation below that high current ($I_{D20} = I_{D19}$) in the branch and larger size of the transistor (M19) will increase the intrinsic transconductance g_{m19} to a sufficiently larger value which will further increase the gain and output swing of the 2-stage OTA.

$$I_D = \frac{\mu_n . C_{ox}}{2} . \frac{W}{L} . (V_{gs} - V_{th})^2 \tag{3.7}$$

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = \mu_n . C_{ox} . \frac{W}{L} . (V_{GS} - V_{TH}) \tag{3.8}$$

$$g_m = \sqrt{2 I_D . \mu_n C_{ox} . \frac{W}{L}} \tag{3.9}$$

Since M20 is used for current scaling to maintain high current in the branch, therefore it is very important to find the suitable node from which M20 can get the required biasing gate voltage (VB). There are several ways of biasing a transistor [29][32][33] but in case of low voltage application, it is important to consider the fact that gate voltage should not be greater than V_{DS20} which will force the transistor to operate in triode region. This can be done by adding a biasing circuit in the second stage that includes a series connected NMOS and a PMOS as shown in the figure 3.9. Biasing circuit consists of a PMOS M21 which is biased according to M11 and an NMOS provides a good biasing condition for M20 to be in saturation region using a current mirror. Current scaling is a very common technique to regulate the current flow in the branch using the concept of current mirrors. Hence, current I_{D21} can be scaled using the formula below and the same current can be mirrored into the CS amplifier circuit to increase the flow of charge in the output branch. As illustrated in Fig. 3.9, the current in the output branch can be scaled “m” times the current in the current in the first stage.

$$\frac{I_{D21}}{I_{D11}} = \frac{W/L_{21}}{W/L_{11}} = m{:}1 \tag{3.10}$$

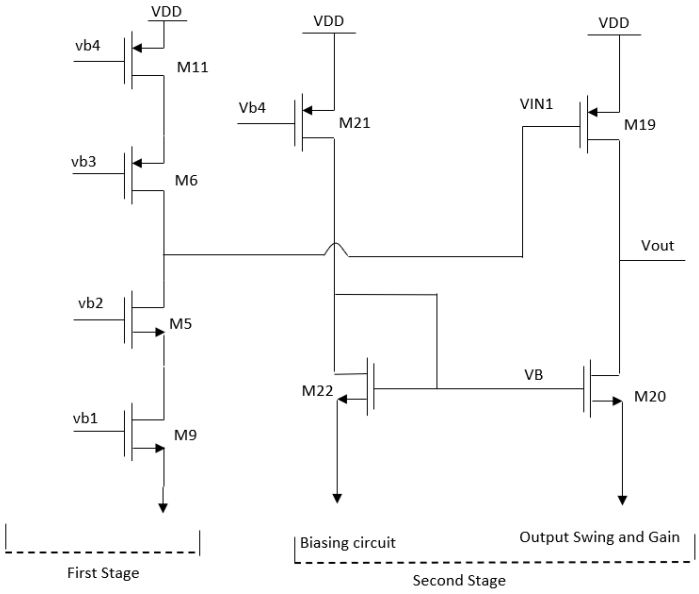


Figure 3.9 Biasing circuit for the second stage OTA

Equivalent circuit of proposed 2-stage OTA can be designed by combining the topologies described in sections 2-4, shown in fig.3.10.

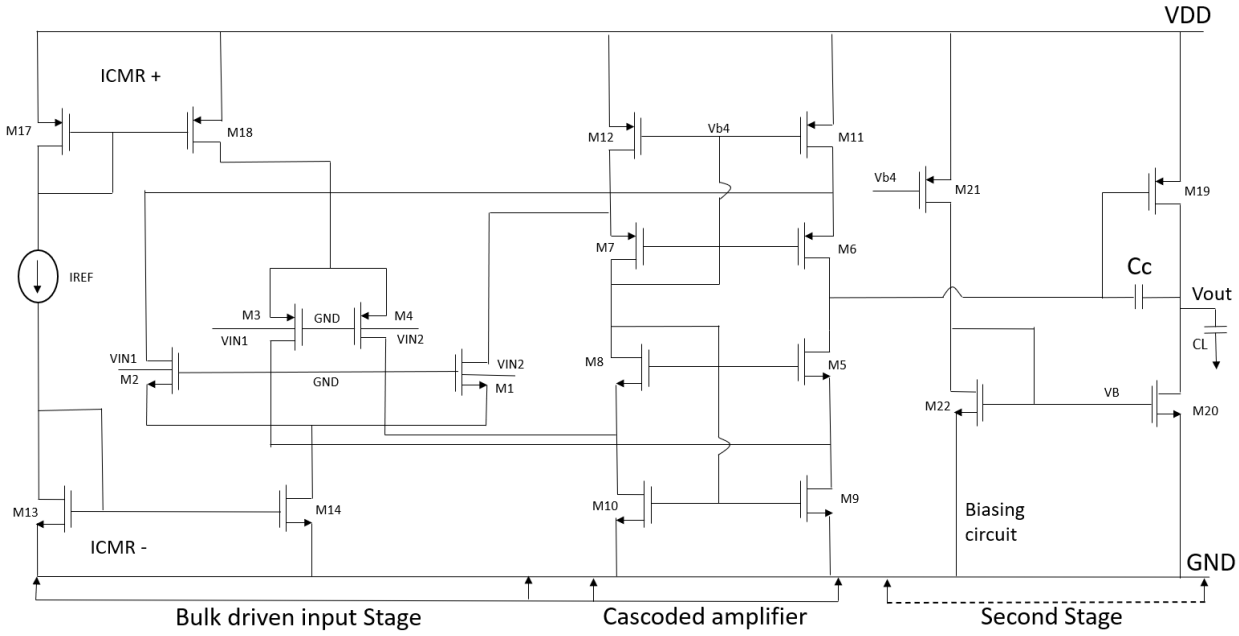


Figure 3.10 2-stage bulk driven OTA

Chapter 4: Analysis

4.1 Introduction

We started with the design of the first stage. We have used a differential amplifier to improve the gain. Next, is the design of the second stage which is a common-source amplifier for the maximum output voltage swing. The block diagram of the two stage OTA is shown in Figure 4.1 where a compensating capacitor (explained in section 4.2) is placed between the dominant pole of the first and second stage for frequency response.

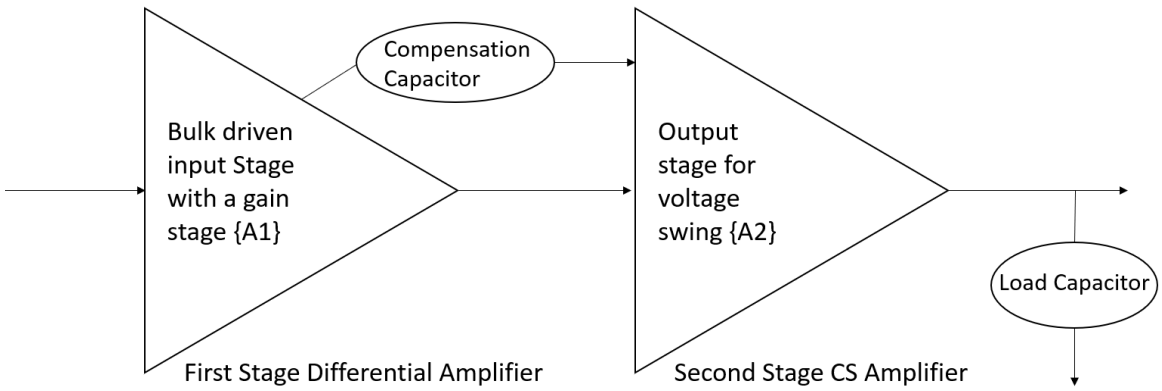


Figure 4.1: Block diagram of the 2-stage OTA

Figure 4.2 shows the circuit diagram of the first stage which has been used for the calculation of aspect ratios of different NMOS and PMOS transistors using respective functionalities. For instance, the bulk driven input MOS transistors (M1, M2, M3, M4) are used to define the gain-bandwidth product of the first stage. Similarly, M14 and M18 are a part of the input current mirror and work alternatively in triode and saturation region to give a rail-to-rail input voltage headroom for the input MOS transistors (as explained earlier in Section 3.2). Hence, M18 and M14 is

responsible for the input common mode range ($ICMR^+, ICMR^-$ respectively). To explain the working of circuit, we derive the transfer function of the first stage as shown in the next section.

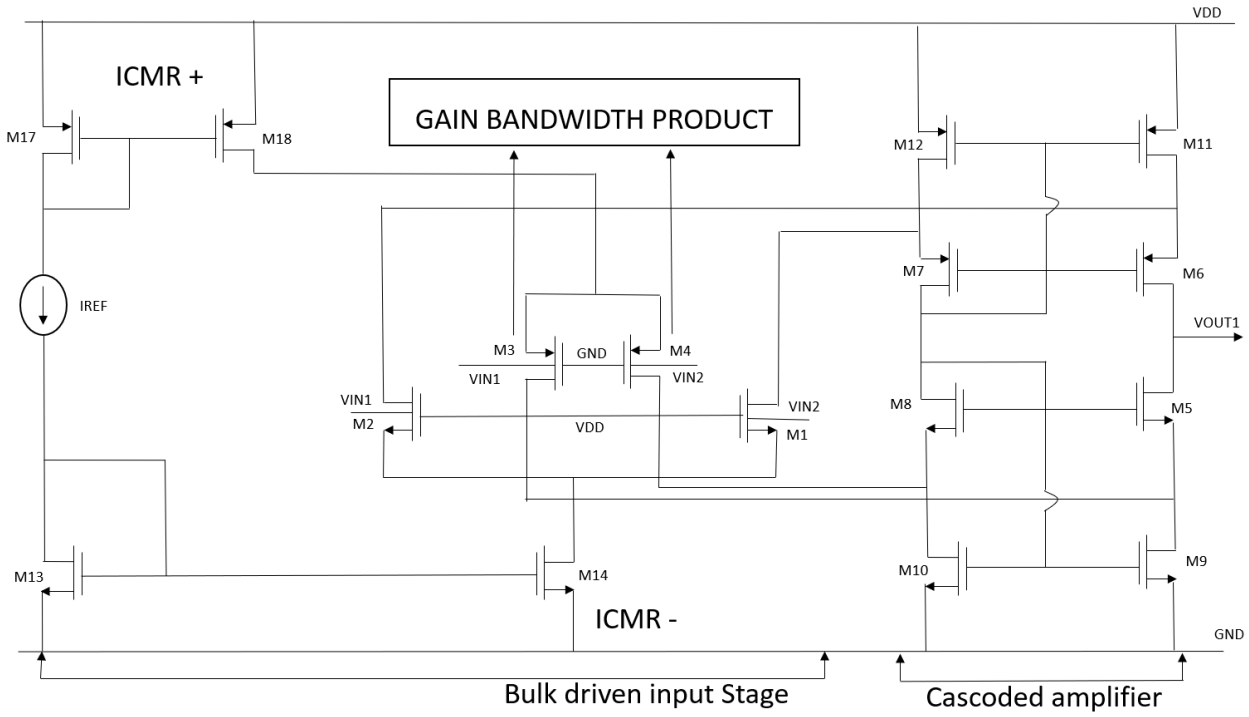


Figure 4.2: Circuit diagram of the first stage of OTA

4.2 Small-signal analysis and transfer function

To derive the transfer function for the first stage, AC analysis is done for the proposed circuit architecture to understand the dominant poles (responsible for transconductance, g_{mb}) in the circuit. Here, all other insignificant poles are ignored because their absence do not affect the transfer function. Fig. 4.3 shows the small signal equivalent circuit of the first stage.

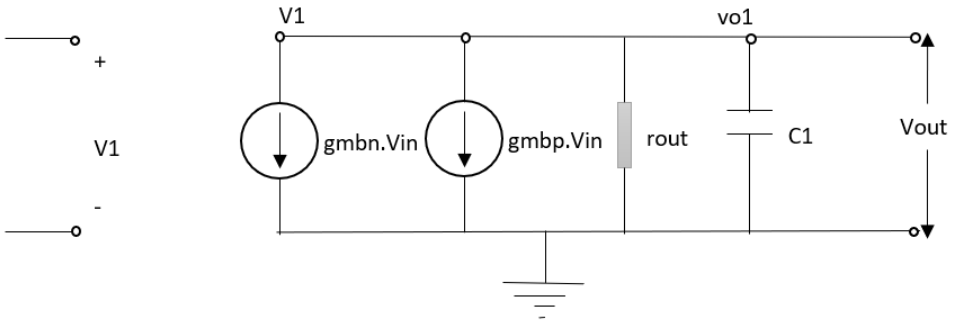


Figure 4.3: Small-signal analysis of the first stage

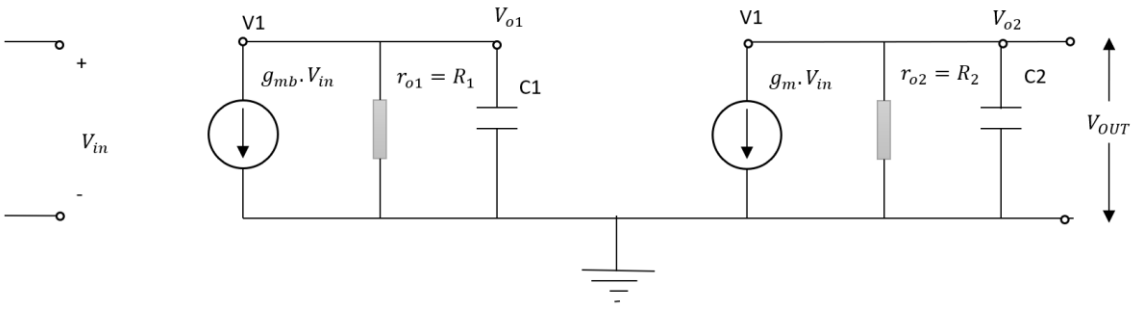


Figure 4.4: Small-signal analysis of the 2-stage OTA without the miller capacitance

Fig. 4 shows the small signal equivalent circuit of the second stage. The circuit in Figure 4.4 has two dominant poles:

$$P_1 = \frac{1}{R_1.C_1} \tag{4.1a}$$

$$P_2 = \frac{1}{R_2.C_2} \tag{4.1b}$$

P_1 is the dominant pole of the first stage whereas P_2 is the pole in the second stage. R_1 is the equivalent output resistance of the gain stage (first stage). Similarly, R_2 is the equivalent resistance of the second stage CS amplifier. Value of these equivalent resistances will be derived later in Section 4.3. C_1 is the parasitic capacitance of the NMOS and PMOS devices near the first dominant pole in the cascoded differential amplifier. C_2 is the gate capacitance of the PMOS (M19) in the

second stage. Before deriving the transfer function, we should also observe that in practical applications, the circuit is designed for a purely capacitive load. Hence, C_2 is parallel to the load capacitance (C_L) which is significantly larger than the gate capacitance of M19.

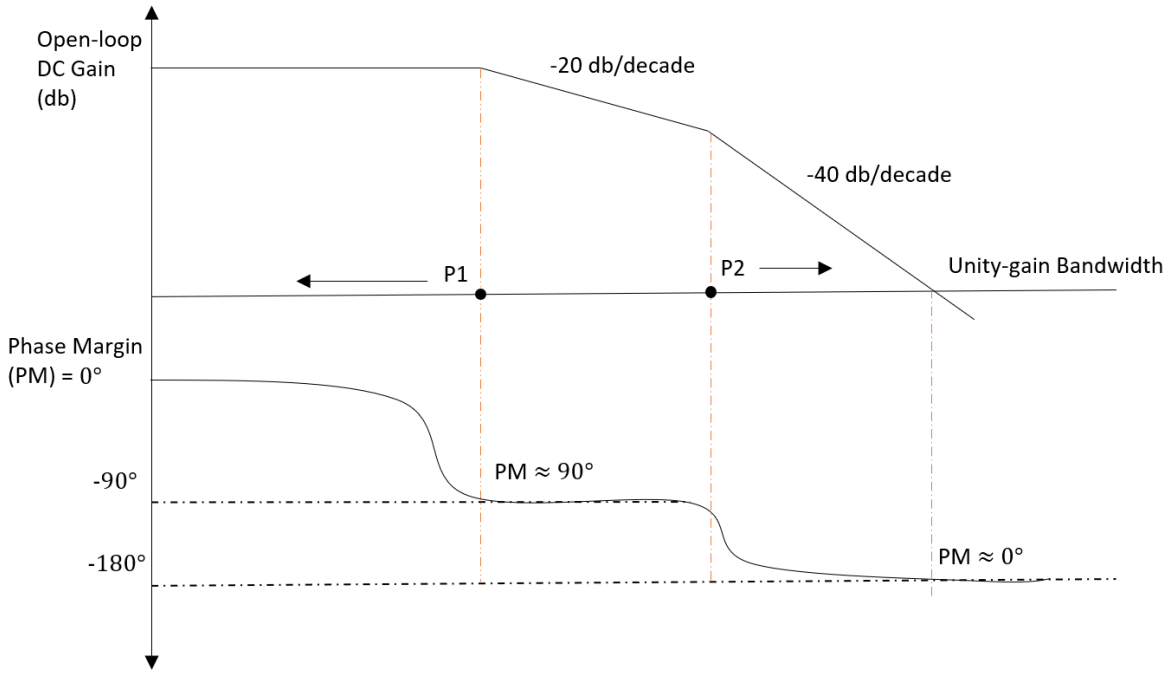


Figure 4.5: Problems for gain and phase without compensation capacitor

As illustrated in Figure 4.5, the bode plot for open loop gain with respect to phase shows a poor phase margin in the absence of compensation capacitor (C_C). The first pole can give a phase margin of around 90° but as the slope of open-loop gain after the second pole falls to -40dB/decade, the phase margin at the unity-gain bandwidth can be as low as 0°. This poor phase margin can be improved by adding a large capacitance in parallel to the parasitic capacitances of the first stage (C1) to push the first pole towards the left of the bode plot. According to equation 4.1, increasing C1 will decrease the pole frequency (P1) and move the pole towards the left in the graph. Similarly, the pole P2 can be moved towards the right of the bode plot to achieve the desired phase margin. Either a compensation capacitor [34] or a or Feed-forward compensation technique [35] can be

used in this type of topology. Adding a large capacitance to C1 increases the chip area and the power consumption, hence the concept of Miller effect [34] compensation method can be used to increase the capacitance.

Figure 4.6 shows how the miller effect increases the capacitance without using a big capacitor. If we add a small capacitor (C_C) as a feedback loop of the second stage OTA (Fig. 4.6a), the equivalent circuit looks like Fig 4.6b, where the effect of the capacitor C_C is multiplied by one plus the gain of the second stage. This makes capacitor C1 big compared to before.

$$P_1 = \frac{1}{R_1.C_1} = \frac{1}{R_1[C_1+C_c(1+A2)]} \approx \frac{1}{R_1 C_C} \tag{4.2}$$

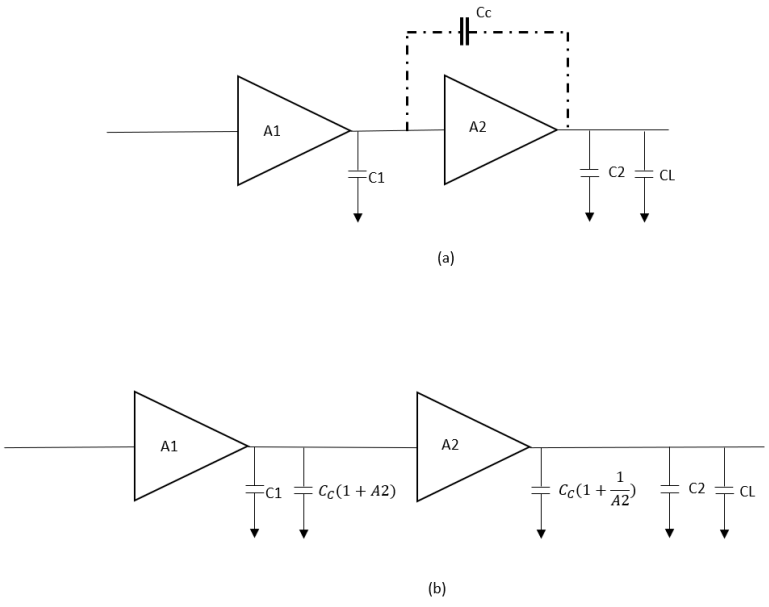


Figure 4.6: Miller-effect in the two stage OTA

According to Fig. 4.7, transfer function is calculated by the ratio of output voltage to the input voltage:

$$\frac{V_o}{V_{in}} = \frac{V_{out}}{V_1}.\frac{V_1}{V_{in}}$$

Next, adding the miller capacitance as shown in Figure 4.7 and applying Kirchhoff's Current Law (KCL) to the first and the second stage in the small signal model, we find:

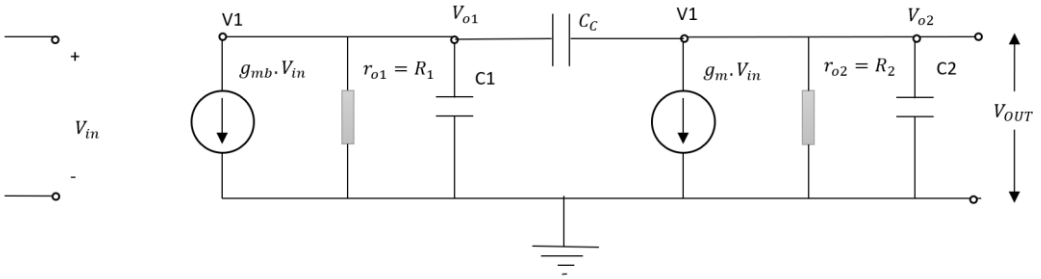


Figure 4.7: Small-signal analysis of the 2-stage OTA with the miller capacitance

Loop 1: First stage

$$\frac{V_1}{1/sC_1} + \frac{V_1}{R_1} + g_{mb1}.V_{in} + \frac{V_1 - V_o}{1/sC_c} = 0$$

$$\frac{V_1}{1/sC_1} + \frac{V_1}{R_1} + \frac{V_1}{1/sC_c} - \frac{V_o}{1/sC_c} = -g_{mb1}.V_{in}$$

$$sC_1R_1V_1 + V_1 + sC_CR_1V_1 - sC_cR_1V_o = -g_{mb1}.R_1.V_{in}$$

$$V_1 = \frac{V_o.sC_c.R_1 - g_{mb1}.R_1.V_{in}}{1 + sR_1(C_1 + C_c)} \quad (4.3a)$$

Loop 2: Second stage

$$\frac{V_o}{1/sC_2} + \frac{V_o}{R_2} + g_{m19}.V_1 + \frac{V_o - V_1}{1/sC_c} = 0$$

$$V_o\,[\,\frac{1}{R_2}\,+\,s(C_2+C_c)\,]\,=\,V_1\,(\,s.C_c\,-\,g_{m19}\,)$$

Substituting the value of V_1 from Loop1:

$$V_o\,[\,1\,+\,s.R_2(C_2+C_c)\,]\,=\,\frac{V_o.sC_c.R_1-g_{mb1}.R_1.V_{in}}{1+sR_1(C_1+C_c)}.R_2\,(\,s.C_c\,-\,g_{m19}\,)$$

$$V_o[1\,+\,sR_2(C_2+C_c)\,-\,sC_cR_1R_2(sC_c+g_{m19})]\,=\,\frac{-\,g_{mb1}R_1R_2V_{in}(sC_c-g_{m19})}{1+sR_1(C_1+C_c)} \qquad (4.3b)$$

Substituting the value of V_1 from equation 4.3a in equation 4.3b, we get the transfer function:

$$\frac{V_o}{V_{in}}=\frac{g_{mb1}.g_{m19}.R_1.R_2.(1-{}^{sC_c}\!/_{g_{m19}})}{s^2[\,R_1.R_2(\,C_1.C_2+C_1.C_c+C_2.C_c)\,]+s[\,R_2(C_2+C_c)+R_1(C_1+C_c)+C_c.g_{m19}.R_1.R_2]+1} \qquad (4.3c)$$

4.2.1 Simplification of the transfer function:

Equation 4.3d shown below is the standard transfer function for 2-stage system where A_{DC} is the open loop DC gain of the OTA, "s" is the frequency dependent parameter at which the gain is calculated (for DC calculations s = jω = 0), "z" is the zero for the amplifier (explained later in section 4.4), P_1 and P_2 are pole frequencies of the first and second stage respectively.

$$\frac{V_o}{V_{in}}\,=\,\frac{A_{DC}(1-{}^{S}\!/_{Z})}{(1+{}^{S}\!/_{P_1})(1+{}^{S}\!/_{P_2})} \qquad (4.3d)$$

$$\frac{V_o}{V_{in}}\,=\,\frac{A_{DC}(1-{}^{S}\!/_{Z})}{s^2(\frac{1}{P_1P_2})+s(\frac{1}{P_1}+\frac{1}{P_2})+1} \qquad (4.3e)$$

Since P_2 (C_L is larger compared to the gate capacitance of M19) is very large, therefore, $\frac{1}{P_2}\approx 0$ in equation 4.3e and neglected for further calculations.

$$\frac{V_o}{V_{in}} = \frac{A_{DC}(1 - {}^{s}/_{z})}{s^2(\frac{1}{P_1P_2}) + s(\frac{1}{P_1}) + 1} \quad (4.3f)$$

Comparing the general equation for a two-stage system (equation 4.3f) with the calculated transfer function in the equation 4.3c. We achieve the following values for zeros and value for the pole frequency at the dominant poles of both the stages:

$$z = \frac{g_{m19}}{C_c} \quad (4.4)$$

Next comparing the coefficients of "s" and "s^2" from the transfer function we get the value of both the poles in this system:

$$P_1 = \frac{1}{R_1R_2g_{m19}C_2} \quad (4.5a)$$

$$P_2 = \frac{R_1R_2g_{m19}C_c}{R_1R_2(C_1C_2+C_1C_c+C_2C_c)} \quad (4.5b)$$

C1 is the parasitic capacitance of the first stage so it is smaller than C2. Hence,

$$P_2 = \frac{g_{m19}}{C_2} \quad (4.5c)$$

$$A_{DC} = g_{mb1}.g_{m19}.R_1.R_2 \quad (4.6)$$

Equation 4.6 shows the open loop DC gain of the OTA, where g_{mb} and g_m are the transconductance of the respective transistors, R1 and R2 are the equivalent resistances of the first and second stages respectively.

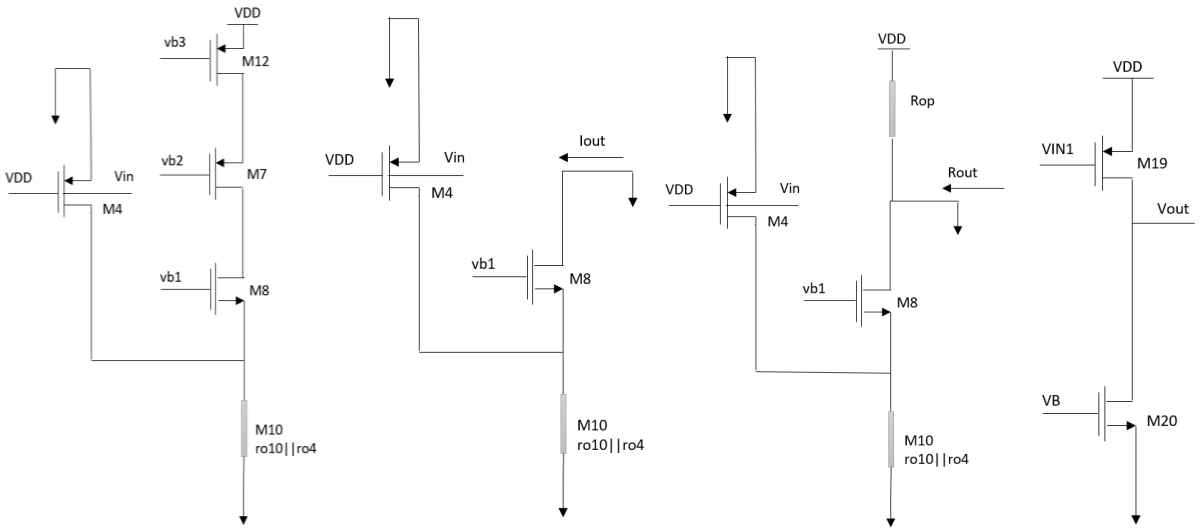
4.3 Gain of the OTA

The open loop gain of an ideal operational amplifier is infinite which is practically not possible, hence, the gain of a practical amplifier is kept sufficiently large (around 80-100 dB) to ensure a stable operation. For achieving such high gain, in this work a 2-stage OTA is used instead of a single stage. This is because single stage amplifier is not sufficient for achieving such high gain around 80-100 dB. Introducing a second stage adds a better intrinsic transconductance and output impedance to the proposed OTA. Gain of a single stage is calculated by the product of intrinsic transconductance of the input MOS and the total output impedance ($g_m . R_{out}$) as formulated in equation 4.6.

The total gain of the two-stage amplifier:

$$A_v = Gain\ of\ the\ First\ Stage * Gain\ of\ the\ Second\ Stage = A_{v1} * A_{v2} \quad (4.7)$$

By inspection, it can be observed that the folded-cascoded stage is responsible for the R_{out} of the first stage as shown in the half-equivalent circuit (Figure 4.8). Since the M4 and M10 are parallel to each other, therefore the equivalent resistance on the source of M8 will be $r_{010} \,||\, r_{04}$. In Figure 4.8b, the current coming from the output short circuit is equal to the drain current of M8 and impedance looking into the source of M8 is $(g_{m8} + g_{mb8})^{-1} \,||\, r_{08}$ which is much lower compared to $r_{010} \,||\, r_{04}$. Hence, $G_m \approx g_{mb4}$.



(a) *(b)* *(c)* *(d)*

Figure 4.8 a) Half equivalent circuit for gain stage b) G_m calculation c) R_{out} calculation d) Equivalent circuit for calculation for gain in second stage

According to Fig. 4.8c.:

$$R_{op} = (g_{m7} + g_{mb7}).r_{07}.r_{012}$$

$$R_{out} = R_{op} \,||\, [(g_{m8} + g_{mb8}).r_{08}.(r_{010} \,||\, r_{04})]$$

$$R_{out} = [(g_{m7} + g_{mb7}).r_{07}.r_{012}] \;||\; [(g_{m8} + g_{mb8}).r_{08}.(r_{010} \,||\, r_{04})] \tag{4.8a}$$

Substitute the values of the G_m and R_{out} to obtain the open loop gain of the first stage,

$$A_{v1} = g_{mb4}.R_{out} = g_{mb4}.\{[(g_{m7} + g_{mb7}).r_{07}.r_{012}] \;||\; [(g_{m8} + g_{mb8}).r_{08}.(r_{010} \,||\, r_{04})]\}$$

(4.8b)

Similarly, one can calculate the gain of the second stage using the same procedure. The input transistor for the second stage is M19 and the total impedance seen from the output node in Figure 4.8d is the parallel combination of output impedances of M19 and M20.

$$G_m \approx g_{m19} \qquad R_{out} = (r_{019} \,||\, r_{020}) \tag{4.8c}$$

$$\text{Gain} = A_{v2} = g_{m19}.R_{out} = g_{m19}.(r_{019} \,||\, r_{020}) \tag{4.8d}$$

Hence, the total gain can simply be calculated by multiplying the independent gain of the two stages.

$$A_v = A_{v1} * A_{v2}$$

$$= g_{mb4}.\{[(g_{m7} + g_{mb7}).r_{07}.r_{012}] \,||\, [(g_{m8} + g_{mb8}).r_{08}.(r_{010} \,||\, r_{04})]\} * g_{m19}.(r_{019} \,||\, r_{020}) \tag{4.8e}$$

4.4 Gain-bandwidth product and phase margin

Gain and bandwidth of an amplifier are inversely proportional to each other i.e., if the gain is increased, the bandwidth decreases. Low gain with a large bandwidth ensures the stability of an amplifier. Gain-bandwidth product (GBW) is the product of DC gain and bandwidth at which the gain of the OTA is calculated. Unity-gain bandwidth (UGB) is the bandwidth of the amplifier when the gain approaches unity. GBW is equal to the UGB if there is a single dominant pole in the circuit as there is only one constant slope of -20dB/decade which makes both the factors equal. In a 2-stage amplifier, there are two dominant poles which gives two different slopes of the bode plot for gain, here the slope fall -20dB/decade every time a new dominant pole is added. Hence, the unity gain bandwidth shifts more towards the right in the bode plot and the gain bandwidth towards the left. It is also observed that some amplifiers are observed to be unstable with higher gains at the unit-gain bandwidth [21]. In this work, the gain-bandwidth product is calculated from

the total DC gain of the OTA and the pole(P1) at the first stage achieved from the transfer function calculated in Section 4.2:

$$\text{GBW} = A_{DC} * P_1 = \frac{g_{mb4}.g_{m19}.R_1.R_2}{R_1.R_2.g_{m19}.C_c} = \frac{g_{mb4}}{C_c} \quad (4.9)$$

For ideal cases, the slope of the gain in Bode plot drops -20dB/decade for every stage. In case of second stage the slope will fall -40dB/decade after the second pole and goes back to 0dB/decade. This point is known as zero for the OTA (denoted by Z). We assume Z to be significantly larger than GBW (or UGB). Here, for simplification, zero (Z) is assumed to be greater than or equal to 10 times the GBW.

$$Z \geq 10.\text{GBW} \quad (4.10)$$

$$\frac{V_o}{V_{in}} = \frac{A_{DC}(1 - \frac{s}{z})}{(1 + {}^{s}/_{P_1})(1 + {}^{s}/_{P_2})} \quad (4.11)$$

$$Phase\ Margin\ (PM) = \angle\frac{V_o}{V_{in}} = -tan^{-1}\frac{w}{z} - tan^{-1}\frac{w}{P1} - tan^{-1}\frac{w}{P2} \quad (4.12a)$$

When the frequency is equal to the unity-gain, it is considered as GBW. Hence, Replace the frequency (w) by GBW and Z by 10.GBW.

$$PM = -tan^{-1}\frac{GBW}{10.GBW} - tan^{-1}\frac{GBW}{P1} - tan^{-1}\frac{GBW}{P2} \quad (4.12b)$$

Substitute the value of P1 from the equation 4.5a in the equation above:

$$PM = -tan^{-1}\frac{1}{10} - tan^{-1}\frac{g_{mb4}g_{m19}R_1R_2C_c}{C_c} - tan^{-1}\frac{GBW}{P2} \quad (4.12c)$$

$$PM = -tan^{-1}\frac{1}{10} - tan^{-1}A_{DC} - tan^{-1}\frac{GBW}{P2} \quad (4.12d)$$

For a maximum gain, replace $tan^{-1}(A_{DC})$ by 90^o

$$-180 + PM = -5.71 - 90 - tan^{-1}\frac{GBW}{P2}$$

$$PM = 84.29 - tan^{-1}\frac{GBW}{P2} \quad (4.12e)$$

Now let's calculate P2 for a good phase margin of 60^o :

$$60 = 84.29 - tan^{-1}\frac{GBW}{P2} \quad (4.13)$$

$$P_2 \geq 2.2\, GBW \quad (4.14)$$

$$\frac{g_{m19}}{C_2} \geq 2.2\, \frac{g_{mb4}}{C_c} \quad (4.15)$$

Since z = 10.GBW

$$\frac{g_{m19}}{C_c} = 10.\frac{g_{mb4}}{C_c} \Rightarrow g_{m19} = 10.\, g_{mb4} \quad (4.16)$$

Substituting the value of g_{m19} from equation 4.16 in equation 4.15, we find the value of the compensation capacitor (C_C) with respect to the load capacitor (C_L):

$$C_c \geq 0.22\, C_L \quad (4.17)$$

Let's take $C_L = 0.5\, pF$

$$C_c \geq 0.22\, C_L = 0.22 * 0.5pF = 0.11\, pF = 110\, fF \quad (4.18)$$

This is an important relation for tweaking the unity-gain bandwidth regardless of the transistor sizes. Increasing C_C, will move UGB to the left of the bode plot (according to equation 4.9) and vice versa.

4.5 Slew rate

To estimate the slew rate of the proposed circuit we have used the simplified circuit shown below in Figure 4.9.

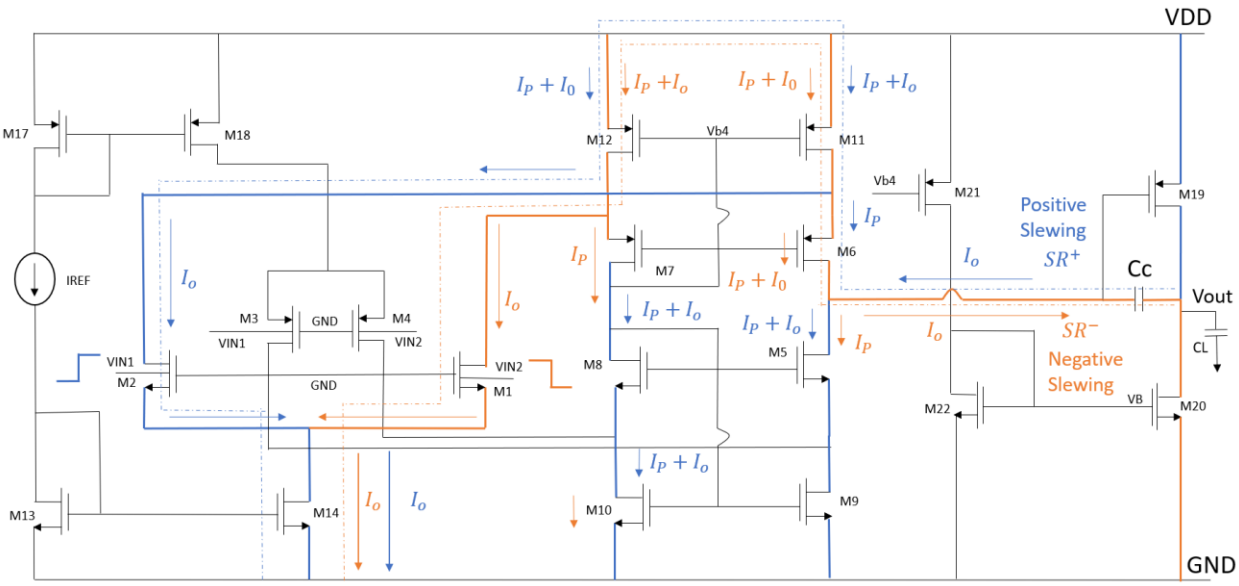


Figure 4.9: Simplified circuit during the positive and negative slewing

Slew rate is the rate of change of an amplifier's output voltage with a change in input signal. Figure 4.6 explains the slewing operation in the proposed OTA as the rate of change of output voltage signal varies from 10% to 90% of the magnitude.

At t = 0, if V_{in} experiences a large positive signal M1 and M4 turns off. Here the slope of the waveform is towards the positive edge of the signal. This is known as positive slewing, where the compensation capacitor C_c is charged by a constant current, I_o (neglecting the parasitic capacitances at C_c due to M19 and M20). The node at the gate of M19 becomes a virtual ground due to the gain of the second stage (i.e., $SR^+ = {I_o}/{C_c} = {I_{D14}}/{C_c}$). In addition, the PMOS M19

should be wide enough (large W/L ratio to amplify the current in the branch) to withstand both the currents ($I_o + I_{D20}$) simultaneously. Similarly, for the negative slewing, I_{D20} must accommodate I_o and I_{D19}. If $I_{D20} = I_o$, then the potential of node at the gate of M19 will increase, turning off M19. Moreover, if I_{D20} is less than I_o, M18 enters the triode region.

$$SR = \frac{I_o}{C_c} = \frac{I_{D14}}{C_c} \tag{4.19}$$

4.6 Aspect ratios(W/L) of the transistors

For calculation of the MOS sizes, we assume the GBW to be large to achieve maximum gain which cannot be achieved because of limitations in intrinsic transconductance of the bulk driven input MOS at a fixed V_{DS}. Therefore, we assume GBW ≈ 30 MHz

4.6.1 Calculation for M1, M2, M3, M4

$$g_{m4} = GBW * C_c * 2\pi = \frac{g_{mb4}}{C_c} * C_c * 2\pi = 30\,MHz * 800\,fF * 2\pi = 160\mu \tag{4.20a}$$

From simulation, $\mu_p C_{ox} = 26\mu \quad and \quad \mu_n C_{ox} = 67\mu$

$$\frac{W}{L}_4 = \frac{g_{m4}^2}{\mu_p.C_{ox}.2.I_{D4}} = \frac{g_{m4}^2}{\mu_p.C_{ox}.I_{REF}} = \frac{(160\,\mu)^2}{26\mu.10\mu A} = 98 = \frac{98u}{1u} = \frac{W}{L}_3 \tag{4.20b}$$

Similarly,

$$\frac{W}{L}_2 = \frac{g_{m4}^2}{\mu_n.C_{ox}.2.I_{D2}} = \frac{g_{m4}^2}{\mu_n.C_{ox}.I_{REF}} = \frac{(160\,\mu)^2}{67\mu.10\mu A} = 38 = \frac{38u}{1u} = \frac{W}{L}_1 \tag{4.20c}$$

Drain current to a bulk driven MOSFET is formulated by [17]:

$$I_D = \frac{\mu_n.C_{ox}}{2}.\frac{W}{L}.(V_{GS} - V_{T0} - \gamma\sqrt{2|\phi_f| - V_{BS}} + \sqrt{2|\phi_f|})^2 \quad (4.21)$$

When VBS is forward biased, the transconductance of the bulk driven MOS can be more than transconductance of gate driven MOS [19]. Transconductance in the strong inversion [20] is given by:

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\mu_n.C_{ox}}{2}.\frac{W}{L}.(V_{GS} - V_{TH})^2\left(-\frac{\partial V_{th}}{\partial V_{BS}}\right) = g_{mb}.\left(-\frac{\partial V_{th}}{\partial V_{BS}}\right) \quad (4.22a)$$

As we know that,

$$V_{TH} = V_{T0} + \gamma[\sqrt{2.\emptyset_F + V_{BS}} - \sqrt{2.\emptyset_F}] \quad (4.22b)$$

$$\frac{\partial V_{th}}{\partial V_{BS}} = \frac{-\gamma}{2\sqrt{2\phi_f - V_{SB}}}. \quad (4.22c)$$

$$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_f - V_{SB}}}.g_m \text{ [14]} \quad (4.22d)$$

According to [19]:

$$g_{mb4} = (0.2\ to\ 0.4).g_{m4} \quad (4.22e)$$

In this design,

$g_{mb4} \approx (0.3).g_{m4}$

4.6.2 Calculation for M17 and M18 using $ICMR^+$

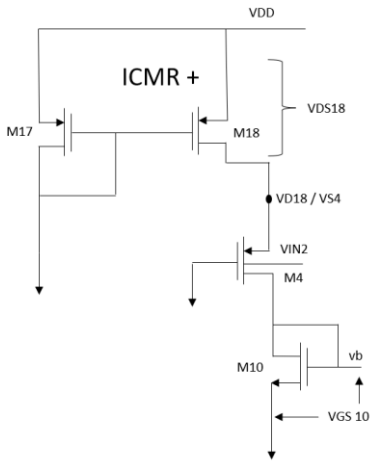


Figure 4.10: Equivalent circuit for $ICMR^+$ calculation

To calculate the W/L ratios of all the transistors, it is crucial to understand each transistor's contribution to the amplifier's operation. M18 is connected to the positive power supply, and the other terminal is connected to the input bulk-driven stage; therefore, it defines the positive half of the input common-mode range ($ICMR^+$). Hence, by the following formulae, one can calculate the W/L ratio of M18. M17 and M18 are designed to be equal to obtain current mirroring without any mismatch. For M18 to be in saturation, $V_{D18} \geq V_{GS18} - V_{TH18}$

When we increase $V_B(V_{IN})$ then the V_{S4}/V_{D18} will decrease because V_{GS18} is kept fixed by M17. Therefore, M18 can enter triode region. Let us calculate V_{DSAT} for M18 to stay in saturation region.

$V_{IN\_max} \geq V_{BS4} + V_{DSAT18}$

$$ICMR(+) \geq V_{BS4\_MAX} + V_{DSAT18}\,(fixed) \tag{4.23a}$$

$$ICMR(+) \geq \left[\sqrt{\frac{2I_{D4}}{\beta_4}} + |V_{t4}|\right]_{max} + V_{DSAT18} = \sqrt{\frac{2I_{D4}}{\beta_4}} + |V_{t4\_max}| + V_{DSAT18} \tag{4.23b}$$

$$V_{DSAT18} \geq ICMR(+) - \sqrt{\frac{2I_{D4}}{\beta_4}} - |V_{t4\_max}| \quad (4.23c)$$

From simulation, $\mu_p C_{ox} * \frac{W}{L}_4 = \beta = 26\mu * \frac{98u}{1u}$ and $V_{t4\_max} = -0.219\,V$

$$V_{DSAT18} \geq 0.8 - \sqrt{\frac{2*5\mu A}{26\mu * \frac{98um}{1um}}} - |-0.518V| = 0.219V = 219\,mV$$

For transistor 18, $\mu_p C_{ox} = 95u$

$$(\frac{W}{L})_{18} = \frac{2.I_{D18}}{\mu_p C_{ox} V_{DSAT18}^2} = 2.194 \approx 3$$

$$(\frac{W}{L})_{17} = (\frac{W}{L})_{18} = \frac{3u}{1u}$$

4.6.3 Calculation for M13 and M14 using $ICMR^-$

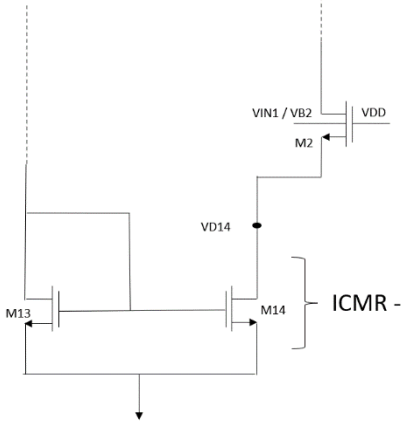


Figure 4.11: Equivalent circuit for $ICMR^-$ calculation

The NMOS M14 works as a current source between the ground and bulk-driven input stage; therefore, the V_{DSAT} of M14 will define the input common-mode range on the amplifier's negative half ($ICMR^-$). The aspect ratios(W/L) of M13 and M14 should be equal for copying the current from the reference current source.

When we decrease V_{B2} (V_{IN}) then V_{D14} also decreases as V_{GS14} is fixed by current mirroring with M13. Hence, M14 can go in the triode region. To prevent this issue and maintain the transistor in the saturation region, we need to fix V_{DSAT14}.

$$V_{IN\_min} \geq V_{BS2} + V_{DSAT14}$$

$$ICMR(-) \geq V_{BS2\_max} + V_{DSAT14}\ (fixed) \quad (4.24a)$$

$$ICMR(-) \geq \left[\sqrt{\frac{2I_{D2}}{\beta_2}} + |V_{t2}|\right]_{max} + V_{DSAT14} = \sqrt{\frac{2I_{D2}}{\beta_2}} + |V_{t2\_max}| + V_{DSAT14} \quad (4.24b)$$

$$V_{DSAT14} \geq ICMR(-) - \sqrt{\frac{2I_{D2}}{\beta_2}} - |V_{t2\_max}| \quad (4.24c)$$

From simulation, for Vin = 0.8V; $\mu_n C_{ox} * \frac{W}{L}_2 = \beta = 67\mu * \frac{98u}{1u}$ and $V_{t2\_max} = 0.321\ V$

$$V_{DSAT14} \geq 0 - \sqrt{\frac{2*5\mu A}{67\mu*\frac{38um}{1um}}} - |0.321| = -0.383V = -383\ mV$$

For transistor 14, $\mu_n C_{ox} = 307u$

$$\left(\frac{W}{L}\right)_{14} = \frac{2.I_{D14}}{\mu_n C_{ox} V_{DSAT14}^2} = 0.444 \approx 1$$

$$\left(\frac{W}{L}\right)_{13} = \left(\frac{W}{L}\right)_{14} = \frac{1u}{1u}$$

4.6.4 Calculation for M19

For phase margin of 60°, z = 10.GBW

$$=> \frac{g_{m19}}{C_c} = 10.\frac{g_{mb4}}{C_c} => g_{m19} = 10.g_{mb4} \quad (4.25)$$

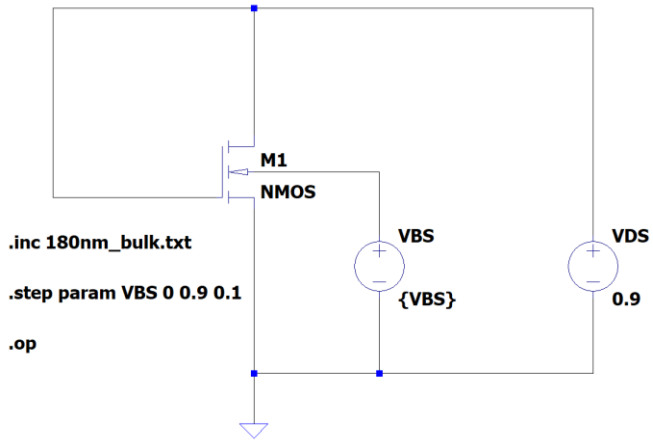
As calculated before $g_{mb4} = 160\mu \Rightarrow g_{m19} = 1600\mu$. However, from the simulation of the first stage, g_{mb4} = 27.5μ. Hence, the transconductance of M19 of the second stage using equation 4.24 will be g_{m19} = 275μ. Using the formula use in Equation 4.20b and 4.20c, the aspect ratio of M19 is 64u/1u. As we can observe in the table below, the transistor sizes obtained for a few MOS devices are big. Hence, W and L can be reduced to half of the original sizes calculated simultaneously maintaining the same W/L ratios. This can be done without affecting other significant parameters as the required length (L) for 180nm devices should be greater than two times L_{min}. $\{L \geq 2.L_{min} = 2 * 180nm = 360nm = 0.36u$ (Hence, L = 0.5u)}

Functions	MOS	W/L ratio
Bulk-driven input NMOS	M1, M2	38u/1u = 19u/0.5u
Bulk-driven input PMOS	M3, M4	50u/1u x 2 = 50u/0.5u
Cascoded NMOS	M5, M8, M9, M10	20u/1u | 40u/2u
Cascoded PMOS	M6, M7, M11, M12	10u/1u | 30u/2u
Current mirror for $ICMR^-$	M13, M14	1u/1u
Current mirror for $ICMR^+$	M17, M18	3u/1u
Second stage input PMOS	M19	64u/1u
Second stage current bias	M20	25u/1u
Biasing circuit	M21 M22	60u/1u x2 25u/1u x2

Table 4.1: Aspect ratios of MOS devices for the proposed OTA

Chapter 5: LTSpice simulations

5.1 DC characteristics of the 180nm technology



Name:	m1
Model:	nmos
Id:	1.20e-04
Vgs:	9.00e-01
Vds:	9.00e-01
Vbs:	0.00e+00
Vth:	4.46e-01
Vdsat:	3.71e-01
Gm:	4.37e-04
Gds:	7.72e-06
Gmb	1.51e-04
Cbd:	0.00e+00
Cbs:	0.00e+00
Cgsov:	2.73e-15
Cgdov:	2.70e-15
Cgbov:	0.00e+00

(a) *(b)*

Figure 5.1: a) Circuit for DC analysis of a single NMOS b) Operating points

The 180nm technology used in the design of the operational transconductance amplifiers and the PDK (product design kit) is imported from online sources [24]. LTSpice tool is used for schematic design and simulation for the circuit analysis. The supply voltage for 180 nm technology is kept low (around 0.9V) for low analysis of the amplifier in low voltage application. To understand the working of a PMOS and NMOS device in low voltage, we need to analyze the DC characteristics of the device.

After simulation in LTSpice, in Fig. 5.1 it is observed that an NMOS gives a maximum transconductance (g_m) of 437 $\mu A/V$ and g_{mb} of 151 $\mu A/V$. The bulk transconductance (g_{mb}) is an important factor for obtaining a high gain from the amplifier as the gain of first stage depends on it (section 4.3).

To find out the threshold voltage of a gate driven single NMOS for 180nm technology, DC sweep is shown in fig. 5.2. Input voltage (V_{gs}) is varied from 0 to 800 mV, to give a drain current ranging from 0 to 120 μA.

Threshold voltage, $V_{th} = 446\ mV$.

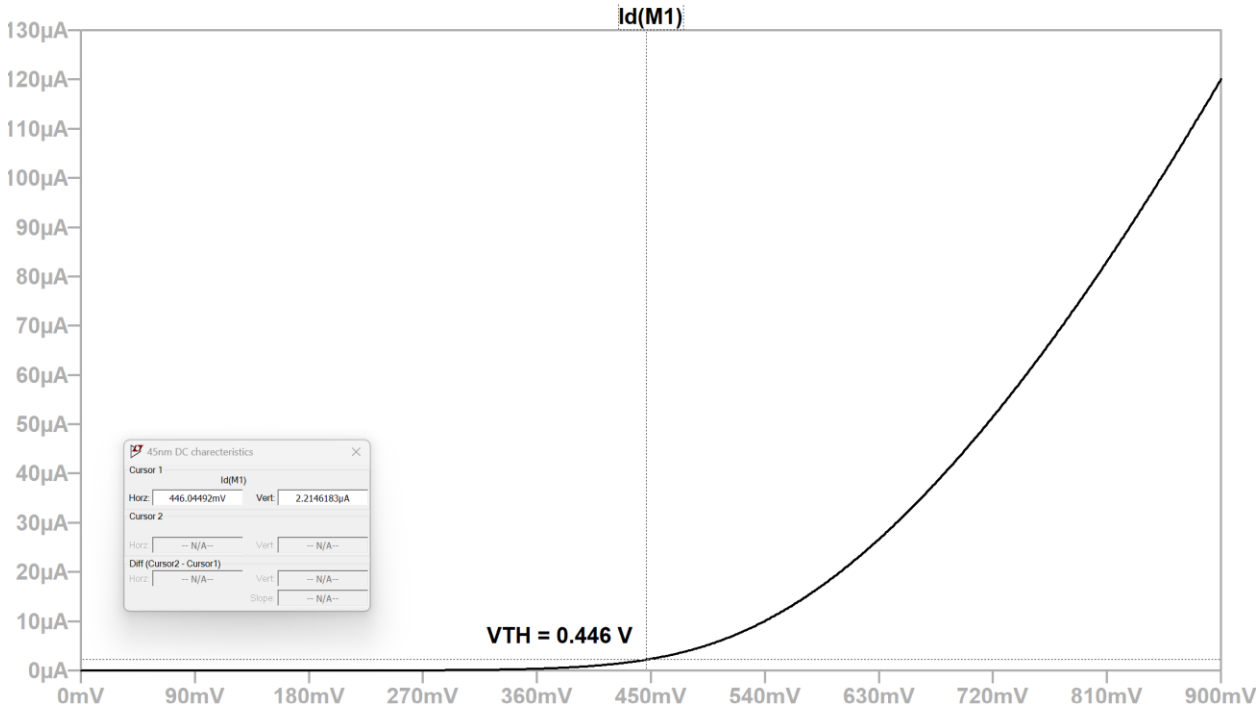


Figure 5.2: DC sweep for threshold voltage in gate driven NMOS

Figure 5.3 shows the output characteristics of the gate driven NMOS, output voltage (V_{DS}) vs the drain current (I_D). This shows the different regions of operation of the device on different drain to source voltages. There are three regions of operation of a MOS device:

- Triode or subthreshold region - (NMOS: $0 < V_{GS} < V_{th}$) and (PMOS: $0 > V_{GS} > V_{th}$)
- Linear Region – NMOS ($V_{GS} > V_{th}$ but $V_{DS} < V_{GS} - V_{th}$)
- Saturation Region – NMOS ($V_{GS} > V_{th}$ but $V_{DS} \geq V_{GS} - V_{th}$)

It can be observed from the simulated graph (Fig. 5.3), the device starts giving a constant current above the threshold when drain to source voltage is larger than the effective voltage ($V_{GS} - V_{th}$) and it has no effect on the current (I_D) i.e., the device saturates. In this thesis we use all the NMOS and PMOS devices (other than bulk driven input stage) in the saturation region to obtain a constant current from each MOS.

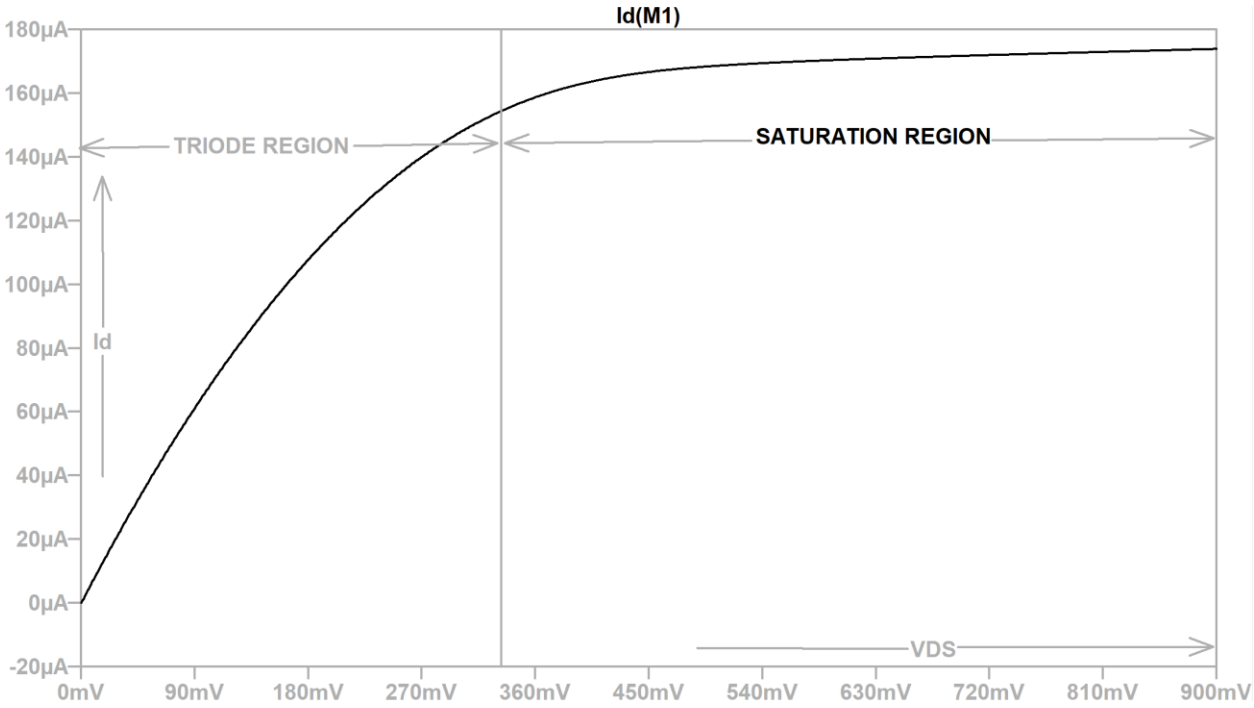


Figure 5.3: IV characteristics of the NMOS (variation of VDS from 0 to 0.9V at VBS = 0.4V)

For low voltage operation, the gate driven MOS described previously is not suitable as the input voltage (V_{GS}) for the device should be much larger than the threshold voltage (i.e., 446 mV). Low input voltage that is less than the threshold voltage will not turn on the device. Hence, the fourth terminal is used for the input stage of the OTA to obtain a good output with optimum variation in the input transconductance (g_{mb}). While in the output characteristics for a bulk driven NMOS, the input voltage is applied to V_{BS} and the output voltage is varied from 0 to 900 mV. It is observed that the device gives an output drain current of 120μA from an input voltage as low as 0V to a

drain current of 220μA on the maximum input voltage as shown in figure 5.4. This solves the problem for the need of lower threshold voltage for the device to operate as a constant current source.

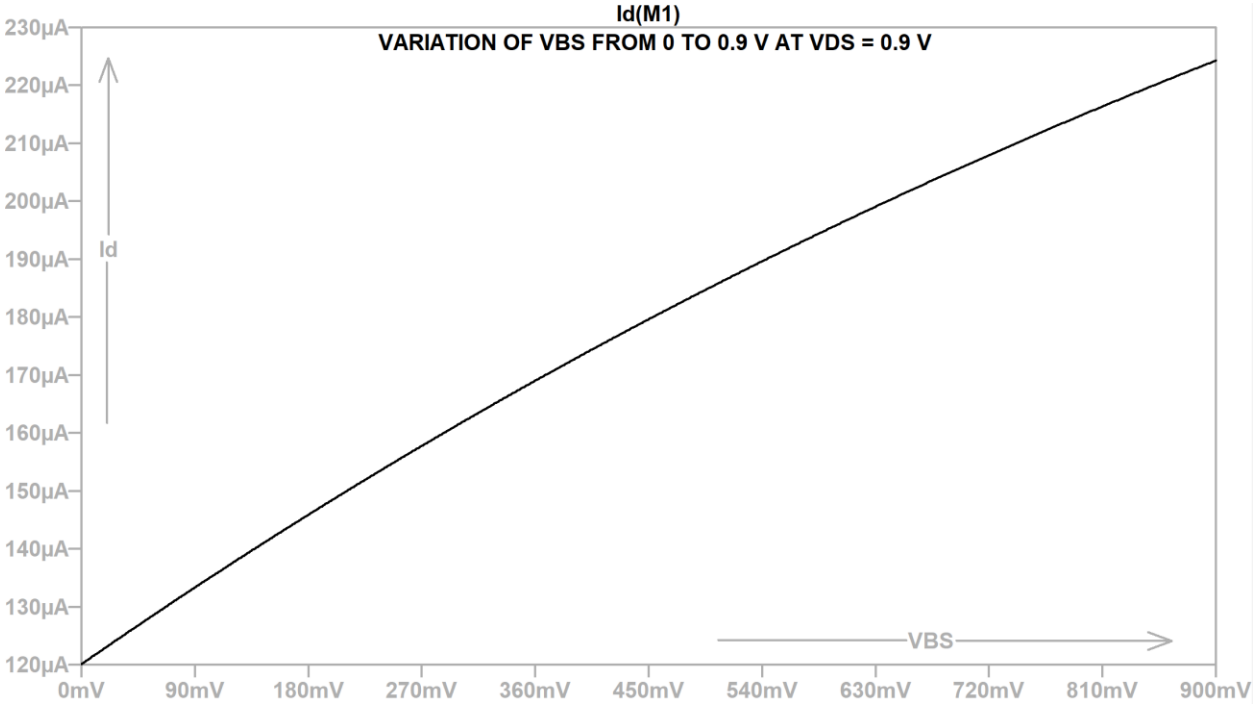


Figure 5.4: DC sweep for bulk driven NMOS (variation of VBS from 0 to 0.9V at VDS = 0.9V)

5.2 Variation of transconductance with input voltage

As shown in figure 5.5, the transconductance (g_{mb}) of the bulk driven input stage NMOS varies from approx. 130μS to 250μS by varying the input voltage (V_{BS}) from 0 to V_{DD}. The operating points are also collected from simulation in figure 5.6 at different input voltages (V_{BS} = 0, 0.2, 0.4 V) to obtain different transconductance values (g_m = 164, 201, 245 $\mu\Omega^{-1}$) respectively. It can be observed from the operating points that g_{mb} shows an increasing trend with an increasing input

voltage. This fluctuation in g_{mb} will not reflect significantly on the total gain at the output stage because of the addition of an extra pole in the circuit.

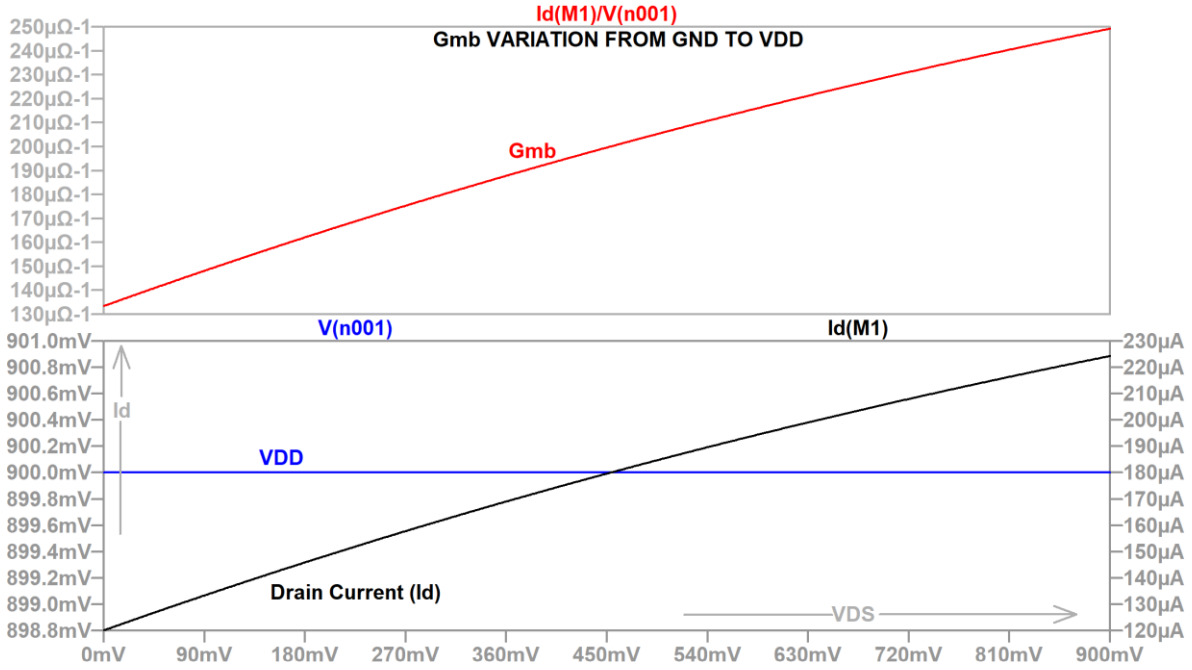


Figure 5.5: Variation of bulk driven NMOS intrinsic transconductance over the input common mode range

Name:	m1
Model:	nmos
Id:	1.45e-04
Vgs:	8.00e-01
Vds:	8.00e-01
Vbs:	0.00e+00
Vth:	3.61e-01
Vdsat:	3.43e-01
Gm:	3.89e-04
Gds:	2.96e-05
Gmb	1.64e-04
Cbd:	4.12e-16
Cbs:	8.00e-16

(a)

Name:	m1
Model:	nmos
Id:	1.82e-04
Vgs:	8.00e-01
Vds:	8.00e-01
Vbs:	2.00e-01
Vth:	3.15e-01
Vdsat:	3.63e-01
Gm:	4.10e-04
Gds:	3.60e-05
Gmb	2.01e-04
Cbd:	4.28e-16
Cbs:	8.53e-16

(b)

Name:	m1
Model:	nmos
Id:	2.26e-04
Vgs:	8.00e-01
Vds:	8.00e-01
Vbs:	4.00e-01
Vth:	2.63e-01
Vdsat:	3.80e-01
Gm:	4.23e-04
Gds:	4.37e-05
Gmb	2.45e-04
Cbd:	4.47e-16
Cbs:	9.06e-16

(c)

Figure 5.6: Operating points for variation in the values of g_m and g_{mb} over different input voltages a) at 0V b) at 0.2V c) at 0.4V

5.3 Operating points from LTSpice

All the operating points are collected and shown in the following tables (5.1a, 5.1b, 5.2a, 5.2b) from the LTSpice simulation of the proposed two-stage OTA. The current distribution (I_d) in the circuit, intrinsic transconductances (g_m and g_{mb}) and their respective operating regions (Saturation) are observed carefully. These values are further used to check whether the device is operating as per the expectations during the analysis of the amplifier (Chapter 4). The recorded parameters are further compared with the expected values to confirm the authenticity of the design.

Semiconductor Device Operating Points:					
--- BSIM3 MOSFETS ---					
Name:	M22	M20	M13	M14	M2
Model:	NMOS	NMOS	NMOS	NMOS	NMOS
Id:	7.07E-06	3.64E-06	1.00E-05	9.50E-06	1.35E-12
Vgs:	3.94E-01	3.94E-01	7.17E-01	7.17E-01	-2.83E-01
Vds:	3.94E-01	6.05E-01	7.17E-01	2.83E-01	5.82E-01
Vbs:	0.00E+00	0.00E+00	0.00E+00	0.00E+00	5.17E-01
Vth:	4.46E-01	4.46E-01	4.46E-01	4.46E-01	3.22E-01
Vdsat:	5.21E-02	5.21E-02	2.40E-01	2.40E-01	3.81E-02
Gm:	1.54E-04	7.95E-05	6.21E-05	5.78E-05	3.74E-11
Gds:	1.05E-06	5.11E-07	8.38E-07	3.44E-06	1.95E-13
Gmb	4.81E-05	2.48E-05	2.01E-05	1.88E-05	8.86E-12
Cbd:	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Cbs:	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

Region of Operation	Saturation	Saturation	Saturation	Saturation	Saturation

Table 5.1a: DC Operating points for the NMOS devices in the OTA

Name:	M9	M10	M8	M5	M1
Model:	NMOS	NMOS	NMOS	NMOS	NMOS
Id:	5.11E-06	5.11E-06	3.98E-07	3.98E-07	1.35E-12
Vgs:	4.25E-01	4.25E-01	3.22E-01	3.22E-01	-2.83E-01
Vds:	1.03E-01	1.03E-01	3.22E-01	3.22E-01	5.82E-01
Vbs:	0.00E+00	0.00E+00	-1.03E-01	-1.03E-01	5.17E-01
Vth:	4.46E-01	4.46E-01	4.53E-01	4.53E-01	3.22E-01
Vdsat:	6.04E-02	6.04E-02	4.21E-02	4.21E-02	3.81E-02
Gm:	1.03E-04	1.03E-04	1.01E-05	1.01E-05	3.74E-11
Gds:	4.42E-06	4.42E-06	3.39E-08	3.39E-08	1.95E-13
Gmb	3.22E-05	3.22E-05	3.02E-06	3.02E-06	8.86E-12
Cbd:	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Cbs:	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Region of Operation	Saturation	Saturation	Saturation	Saturation	Saturation

Table 5.1b: DC Operating points for the NMOS devices in the OTA

Semiconductor Device Operating Points:					
--- BSIM3 MOSFETS ---					
Name:	M21	M19	M3	M4	M6

Model:	PMOS	PMOS	PMOS	PMOS	PMOS
Id:	7.07E-06	3.64E-06	4.71E-06	4.71E-06	3.98E-07
Vgs:	3.12E-02	-1.80E-01	-1.03E-01	-1.03E-01	1.19E-13
Vds:	5.06E-01	2.95E-01	4.32E-01	4.32E-01	4.41E-01
Vbs:	5.06E-01	2.95E-01	6.97E-01	6.97E-01	4.75E-01
Vth:	-4.46E-01	-4.46E-01	-5.18E-01	-5.18E-01	-4.43E-01
Vdsat:	-5.25E-02	-5.25E-02	-5.14E-02	-5.14E-02	-4.39E-02
Gm:	1.58E-04	8.15E-05	1.10E-04	1.10E-04	9.40E-06
Gds:	1.11E-06	6.25E-07	7.42E-07	7.42E-07	3.08E-08
Gmb	4.41E-05	2.27E-05	2.75E-05	2.75E-05	2.61E-06
Cbd:	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Cbs:	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Region of Operation	Saturation	Saturation	Saturation	Saturation	Saturation

Table 5.2a: DC Operating points for the PMOS devices in the OTA

Name:	M7	M12	M11	M17	M18
Model:	PMOS	PMOS	PMOS	PMOS	PMOS
Id:	3.98E-07	3.98E-07	3.98E-07	1.00E-05	9.43E-06
Vgs:	0.00E+00	-4.41E-01	-4.41E-01	0.00E+00	-4.50E-01
Vds:	4.41E-01	3.43E-02	3.43E-02	8.14E-01	3.64E-01
Vbs:	4.75E-01	3.43E-02	3.43E-02	8.14E-01	3.64E-01
Vth:	-4.43E-01	-4.46E-01	-4.46E-01	-4.46E-01	-4.46E-01

Vdsat:	-4.39E-02	-5.25E-02	-5.25E-02	-2.57E-01	-2.57E-01
Gm:	9.40E-06	7.96E-06	7.96E-06	5.04E-05	4.74E-05
Gds:	3.08E-08	6.43E-06	6.43E-06	1.14E-06	1.89E-06
Gmb	2.61E-06	2.24E-06	2.24E-06	1.36E-05	1.28E-05
Cbd:	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Cbs:	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Region of Operation	Saturation	Saturation	Saturation	Saturation	Saturation

Table 5.2b: DC Operating points for the PMOS devices in the OTA

5.4 Bode plot (first stage)

Fig. 5.7 below shows the simulated bode plot for the first stage of the proposed circuit with 12.5% variation with respect to input voltage.

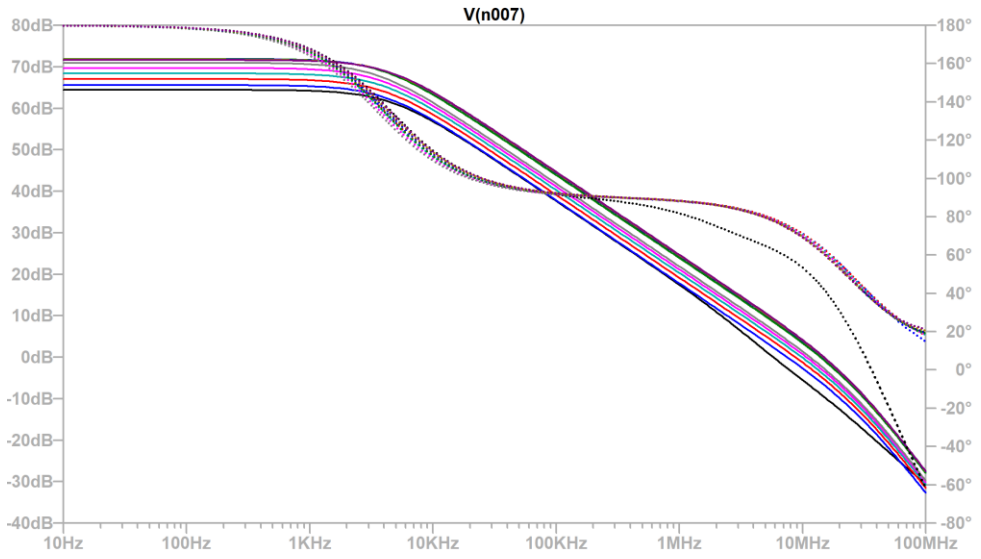


Figure 5.7: Bode plot for gain and phase of first stage

According to section 4.3:

$$A_{v1} = g_{mb4} . \{ [(g_{m7} + g_{mb7}) . r_{07} . r_{012}] \,||[(g_{m8} + g_{mb8}) . r_{08} . (r_{010} \,||r_{04})] \}$$

Or,

$$A_{v1} = g_{mb4} \left\{ \frac{g_{m7}+g_{mb7}}{G_{ds7} . G_{ds12}} \middle|\middle| \frac{g_{m8}+g_{mb8}}{G_{ds8}(G_{ds10}+G_{ds4})} \right\} \tag{5.1}$$

Substituting the values from the operating points (Section 5.3):

$$A_{v1} = 27.5\mu . \left\{ \frac{9.4\mu+2.6\mu}{(3.08*10^{-8})^2} \middle|\middle| \frac{10\mu+3\mu}{3.39*10^{-8}*(4.42\mu+0.742\mu)} \right\} = 2030.9$$

Gain of the first stage in dB = $A_{v1} = 20 * \log(2030.9) = 66.15\ db$

5.5 Phase margin:

Phase margin is calculated by equating the magnitude of the phase at unity gain in the bode plot and adding 180.

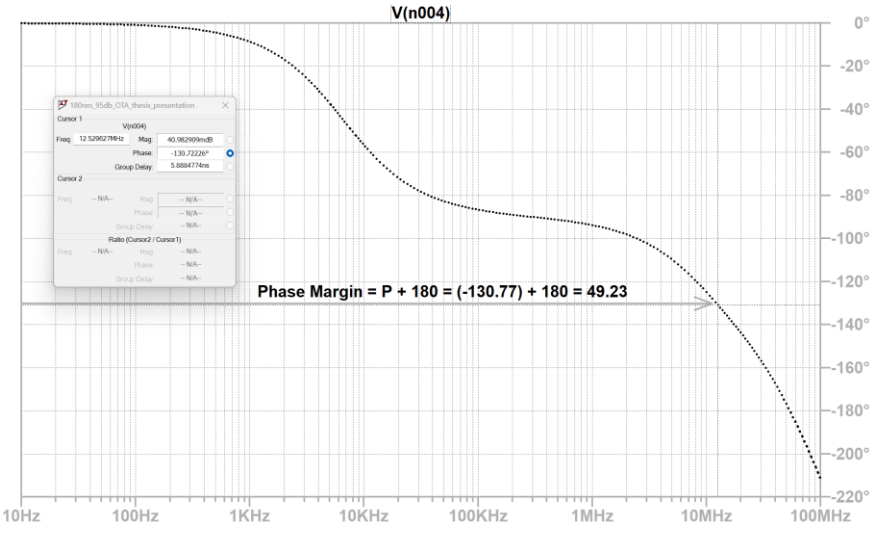


Figure 5.8: Phase margin for the proposed OTA

$$PM = P(at\ unity\ gain) + 180^o = -130.77 + 180 = 49.23^o \approx 50^o \quad (5.2)$$

The estimated and the simulated phase margin is compared as shown in Table 5.3. We observe some difference. This difference, we think, is stemmed from the limitations of the saturated intrinsic transconductance of the bulk driven MOS in the input stage with limited supply voltage.

	Expected	Simulation
Phase margin	60°	49.23° ≈ 50°

Table 5.3: Expected and simulated phase margin for the OTA

5.6 Bode plot (2nd stage)

Bode plot for the second stage is shown in fig. 5.9 below.

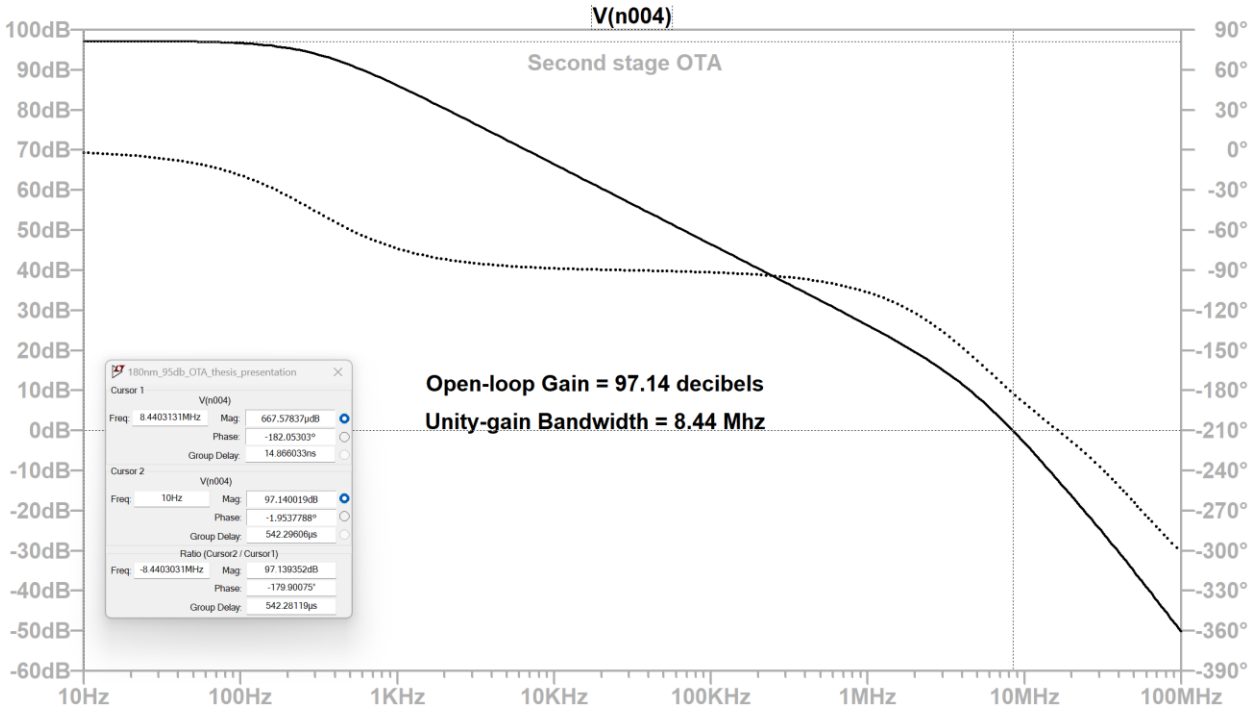


Figure 5.9: Bode plot for gain and phase of second stage

Gain of the second stage can be calculated using the formulae derived in section 4.3 and substituting the values from the operating point collected from the LTSpice simulations.

$$A_{v1} = g_{m19}(r_{019}||r_{020}) = \frac{g_{m19}}{G_{ds19}+G_{ds20}} = \frac{81.5\mu}{0.625\mu+0.511\mu} = 71.74 = 20*\log(71.74) = 37.11\text{dB}$$

Total calculated gain = 66.15 + 37.11 = 103.26 dB

5.7 Slew rate

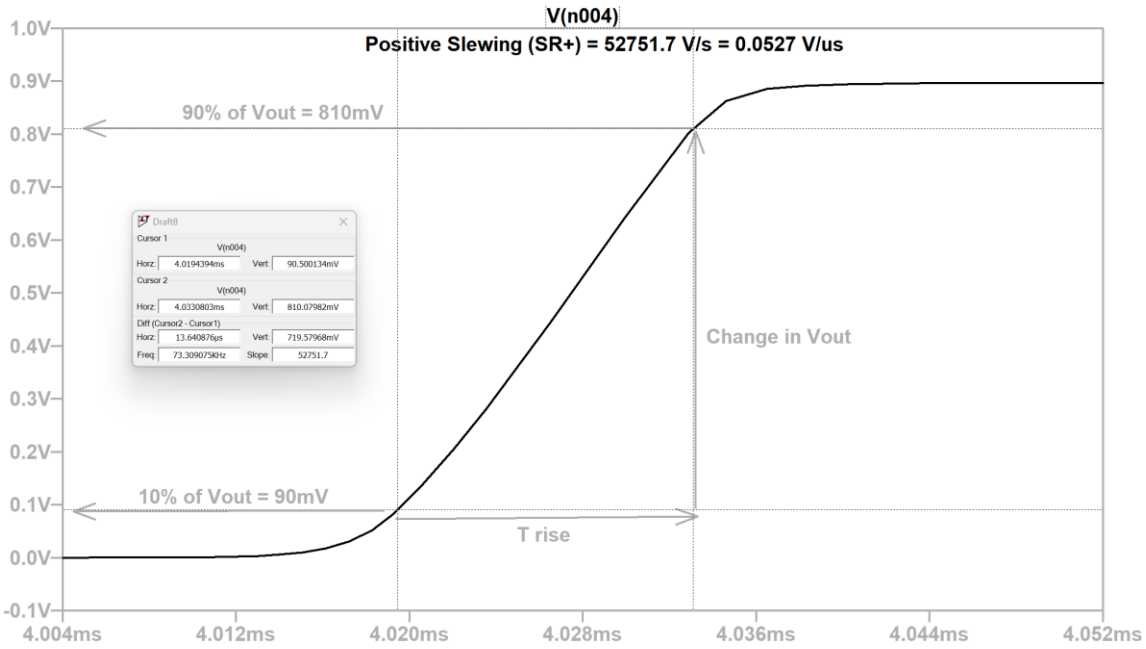


Figure 5.10: Positive slewing

Slew rate shown in the Figure 5.10 (positive slewing) and Figure 5.11 (negative slewing) is obtained by calculating the slope of the output swing. Formulated as:

$$SR = \frac{\Delta V_{out}}{\Delta T_s} \tag{5.3}$$

where ΔV_{out} and ΔT_s have different values for positive and negative slewing:

- ΔV_{out} is the change in the output voltage from 10% of the maximum swing to 90% of the swing and vice versa for the negative slewing
- ΔT_s can be either ΔT_{rise} in terms of positive slewing or ΔT_{fall} in terms of negative slewing

According to the simulation, SR^+ is calculated as 0.0527 V/μS and SR^- is equal to -0.043 V/μS.

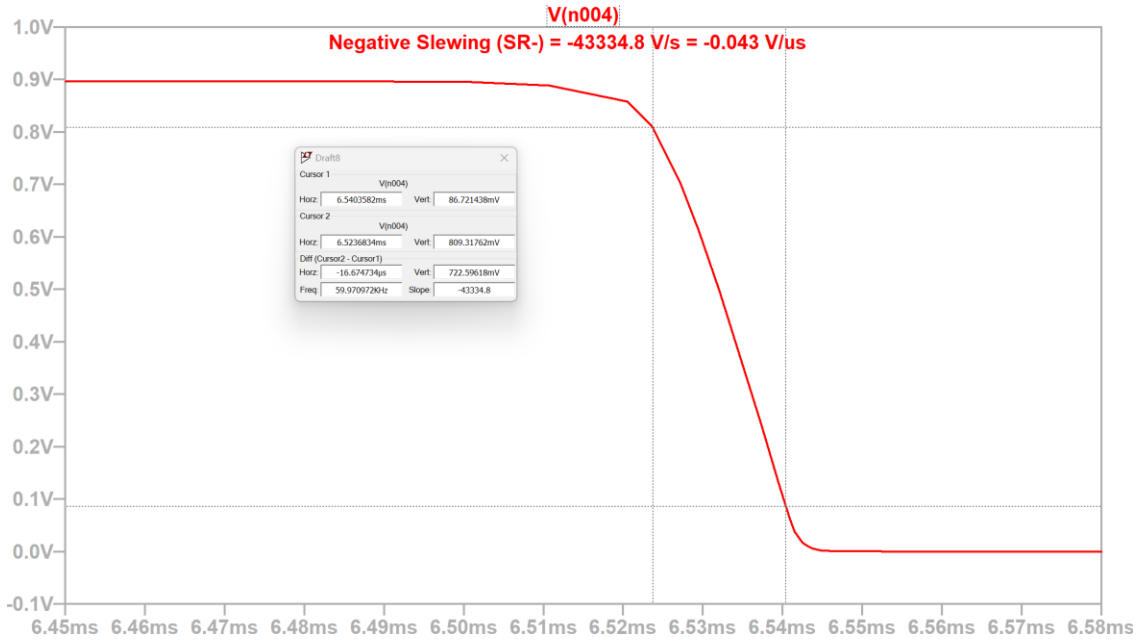


Figure 5.11: Negative slewing

5.7 Variation in supply voltage

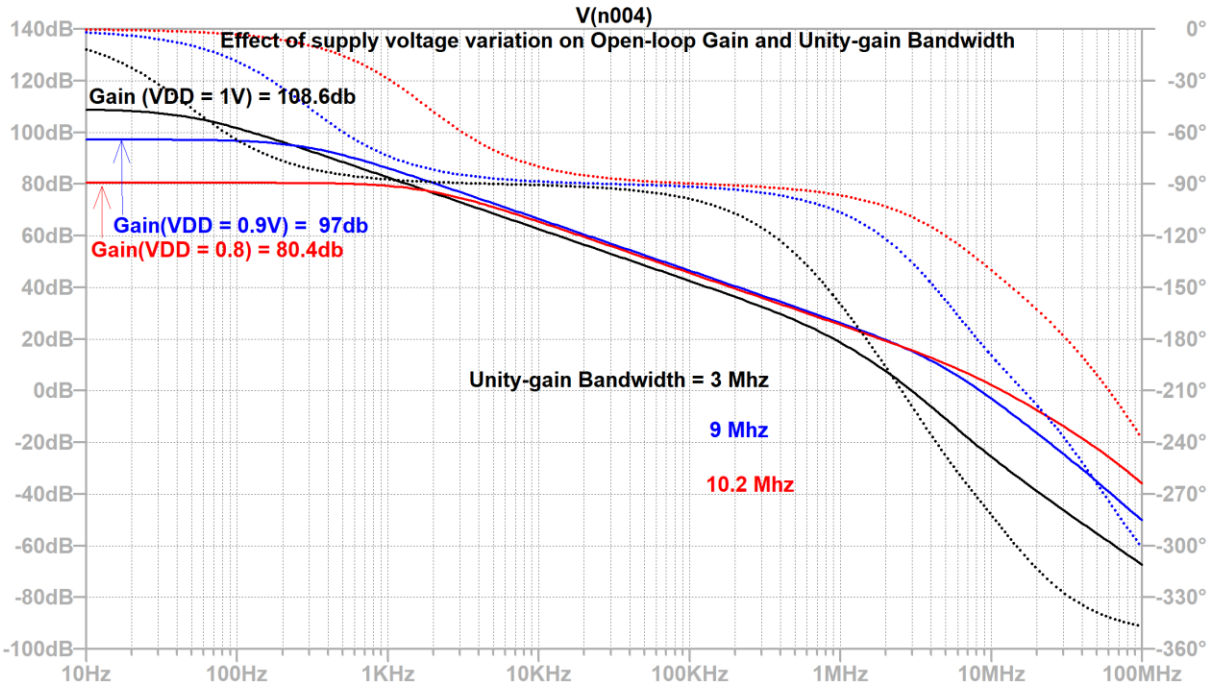


Figure 5.12: Effect of variation in supply voltage on gain and phase

Next, we studied the effect of the supply voltage on the circuit operation. Figure 5.11 shows the effect of variation in the supply voltage from 0.8 to 1V at a fixed input voltage, V_{in} = 0.5V. The major drop in gain from 97dB (at V_{DD} = 0.9V) to 80.4dB (at V_{DD} = 0.8V) is mainly because of the limited availability of voltage headroom (V_{DS}) for the NMOS and PMOS devices in the cascoded gain-stage at such a low potential. However, the significant rise in the gain (at V_{DD} = 1V) is mainly because of the abrupt rise in the $V_{effective}(V_{gs} - V_{th})$ of the device, increases the effective transconductances in both the stages. Similarly, unity-gain bandwidth is dependent on the ratio of transconductance and the capacitance C_c. With even a slight change in g_{mb4}, the unity-gain bandwidth will change from 3Mhz to 10.2Mhz as shown in the figure.

5.8 Variation in input voltage

The effects of input voltage on the device performance while keeping the supply voltage is studied next.

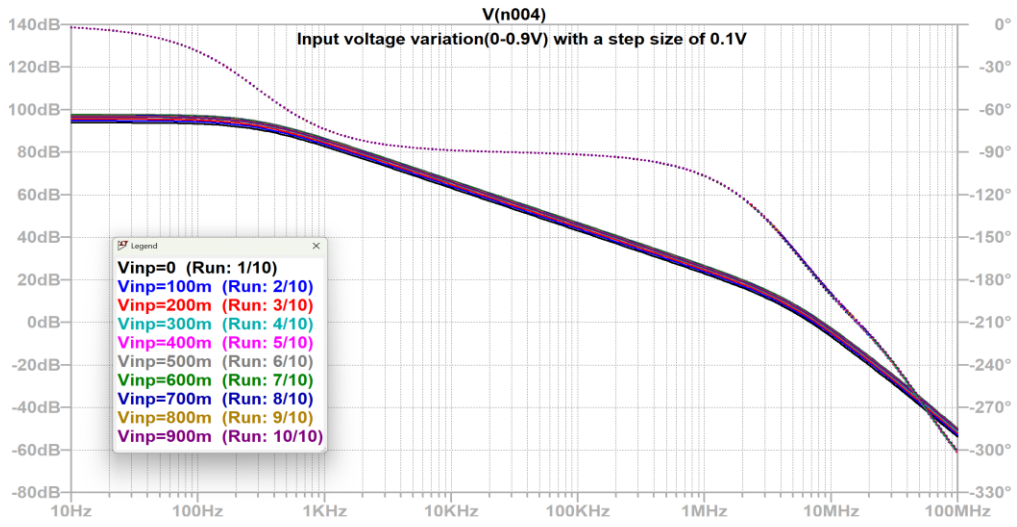


Figure 5.13a: Effect of variation in input voltage on gain and phase

To observe the variation in the gain and phase with respect to the change in input voltage signal, the input voltage is varied from 0 to 0.9V with a step size of 0.1 keeping the supply voltage fixed at 0.9V. The AC sweep is done from 10hz to 100Mhz at 100 data points per decade. As shown in Figure 5.13a, the phase remains stable on different input voltages. However, the open-loop gain has a negligible variation of 4.1% with a change in input voltage from 0V to 0.9V. This is a very reasonable fluctuation in the gain as compared to the significantly larger variations in the bulk transconductance of the input NMOS and PMOS transistors with respect to the change in input voltage (section 5.2). This happens mainly because of the improved gain-bandwidth product which makes the gain stable with any fluctuation in the input signal. Fig. 13b shows the magnified version of the important part of the Fig. 13b.

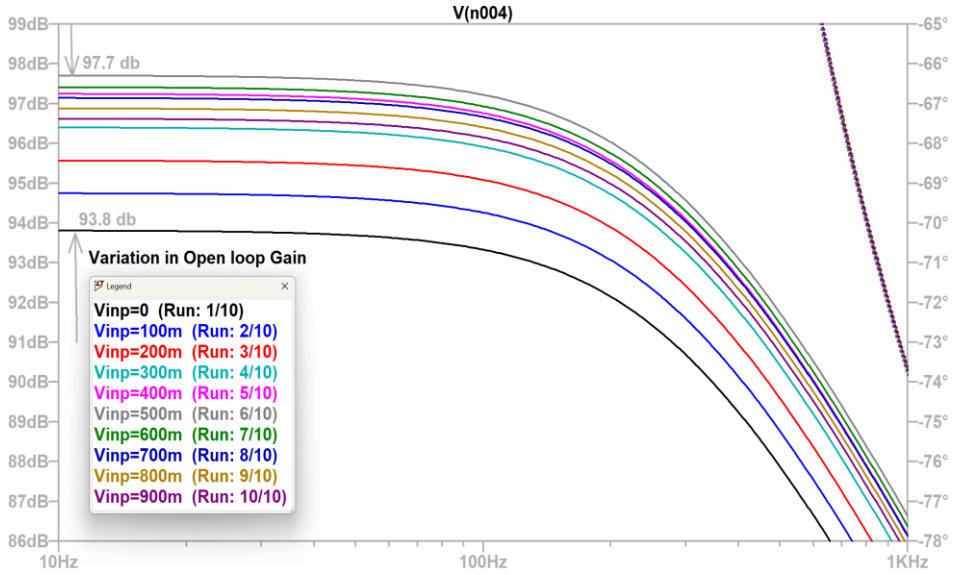


Figure 5.13b: Magnified version for 5.13a

5.9 Effect of different temperatures on the OTA

Work is continued to study the temperature effects on the operation of the designed OTA.

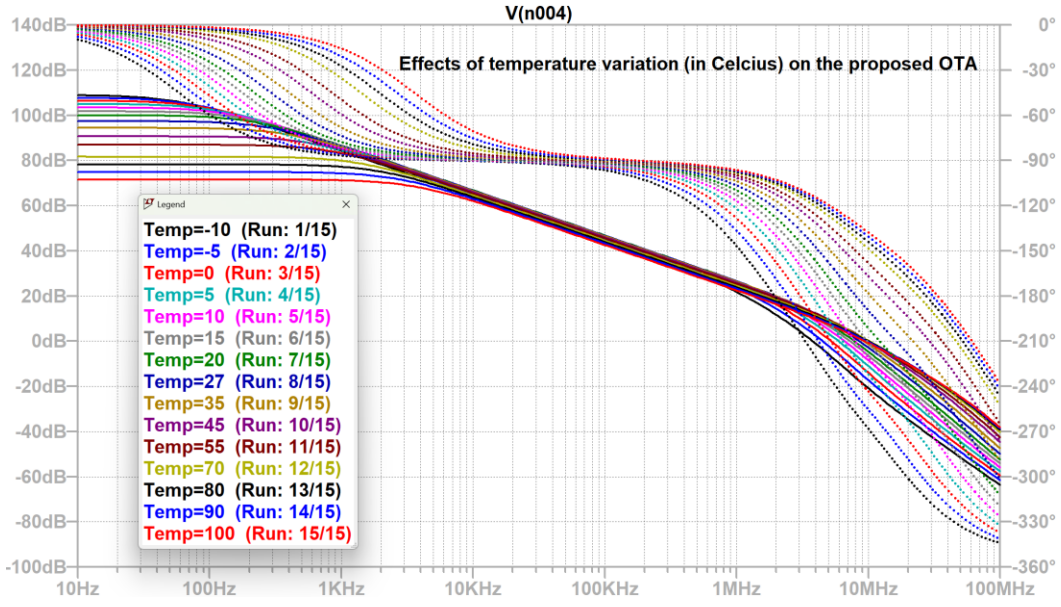


Figure 5.14: Effect of variation in temperature on gain and phase

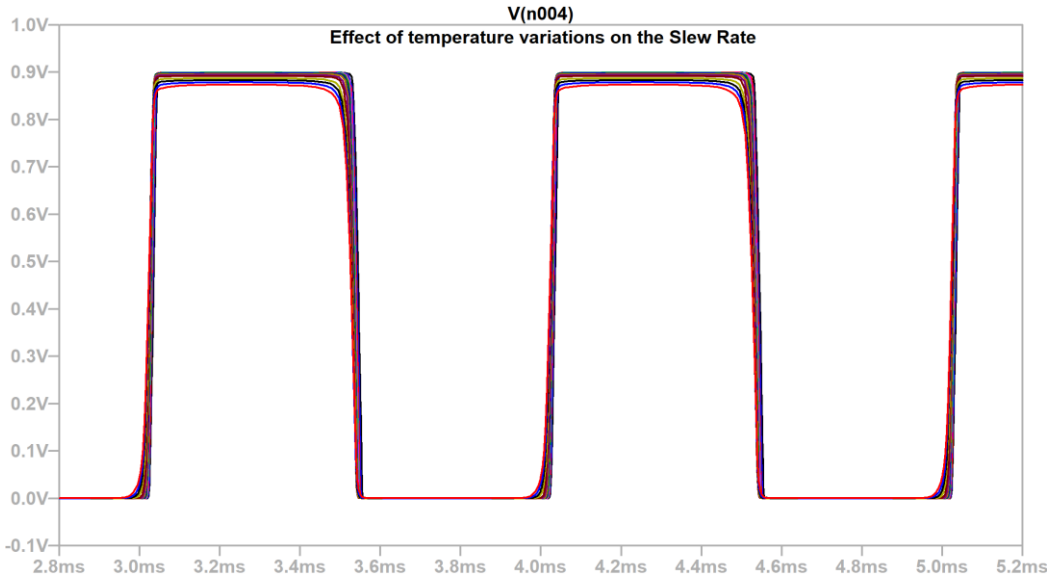


Figure 5.15: Effect of variation in temperature on slew rate

Figure 5.14 and figure 5.15 shows the simulation for the effect of temperature variation on the open loop gain and slew rate of the OTA proposed in this thesis respectively. It is observed that the amplifier works very well from -10℃ to 55℃. The OTA works very well on the typical room temperature ranging from 20-27℃. However, the OTA is not designed for 100℃ because in low voltage applications, portable electronics or any other device used in biomedical applications work on the room temperature or below.

5.10 Power consumption

The power consumption of the circuit is important for any applications. We estimated the power consumption using the simulated results as shown below, Fig. 5.16. The power consumption of the proposed OTA is calculated by the product of output voltage and the current flowing in the output branch (i.e., drain current of CS amplifier in the second stage).

Power consumed = $V_{out} * I_{out}$ = 3.33 μW (5.4)

Improvement of leakage current reduces the static power (power consumed due to leakage current) and allows further optimization of the dynamic power (effective power consumed).

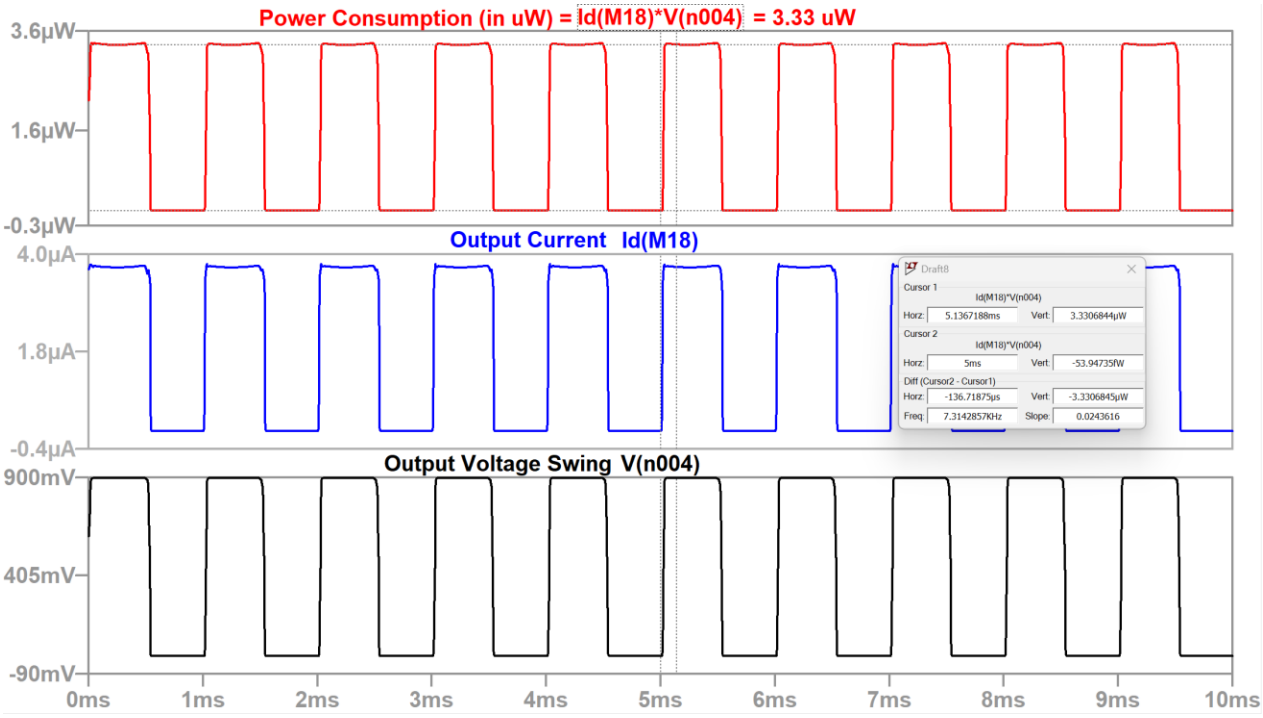


Figure 5.16: Power consumption

Chapter 6: Conclusion and future work

6.1 Conclusion

The proposed OTA architecture works efficiently on both rails of the supply voltages with a very good dynamic range suitable for low voltage applications. All the simulation results are presented and compared with the previously expected/calculated values in table 6.1. In the proposed rail-to-rail OTA design, the simulated values are significantly better than the expectations of this thesis. However, the gain and phase margin achieved in the simulations are slightly lower than the expectations. Achieving a gain of 97.14 dB with a moderately good phase margin of $50°$ is feasible in low voltage applications. In addition, the unity-gain bandwidth of 8.44 MHz helps to stabilize the gain achieved throughout the input common mode range of the OTA.

The proposed architecture for the amplifier is rail-to-rail i.e., it should work throughout the dynamic range of the common mode input on both the rails (V_{DD} and ground). It is observed from the simulation that the amplifier is stable even beyond the positive rail (V_{DD}) of the supply voltage to about 1.2V. As shown in section 2.2.1 earlier, a CS configured MOS input stage can only work in the range of V_{th} to $V_{in} + V_{th}$, for the MOSFET operation in the saturation region necessary for amplification. Beyond 1.2V, the input pair enters into the triode region. Hence, the dynamic range obtained is 0-1.2V compared to the expected range (0-0.9V).

	Expected	Simulation
Supply voltage (V)	0.9	0.9
Open-loop gain (dB)	103.26	97.14

Gain-bandwidth product (MHz)	5	8.44
Variation in gain with input voltage	< 6.5% [10]	4.1%
Power consumption (μW)	-	3.33
Slew rate (V/μS)	-	0.0527
Phase margin	60°	49.23° ≈ 50°
$ICMR^{+}$	0.9	1.2
$ICMR^{-}$	0	0
Common-mode input range	0-0.9	0-1.2

Table 6.1: Expected and simulated results for the OTA

6.2 Contribution

The thesis presents a unique architecture for a bulk driven second stage OTA with a reasonably high gain at a low voltage supply. The designed circuit accommodates rail-to-rail bulk input stage with a gate-driven cascoded gain stage to enhance the load impedance in the first stage. Addition of the second stage improves the gain and phase margin to an optimum value without compromising the stability. The simulated output for all the parameters matches the expected calculations to confirm the reliability of the design. The number of transistors and their sizes are designed to accommodate the circuit in smaller chip sizes. A 97.14 dB open-loop gain and 49.23° phase margin is achieved, which is a good improvement in the bulk-driven devices for 0.9V supply compared to the existing research [5] [25]. A brief comparison of the results obtained are shown in the Table 6.2.

The gain-bandwidth product for this design is optimized to the best possible value to ensure the least deviation of 4.1% in the output gain. The issues regarding fluctuating gain due to unbalanced rail-to-rail input stage [10][11], due to the changing transconductance of the input MOS device, is optimized by adding a significantly higher input impedance and a second stage using a compensation capacitor of 110fF.

After comparison of the results with other gate-driven applications (low voltage OTA) [1] [6] [9], it is concluded that the gain of this design is better in terms of stability and power efficiency. An additional, biasing circuit is proposed in this thesis to ensure a better current and optimum biasing voltage for the output branch, perfectly suitable for low voltage application.

Addition of an extra stage not only improves the gain, but also improves the dependence of open-loop gain on the input bulk-transconductances [10][11] without the need of any addition current injection in the input (to increase the input impedance) and further optimizes the number of transistors used. Furthermore, with large input transistor sizes and open-loop gain, the circuit is still able to achieve a good power consumption of 3.3 uW. The OTA is a second stage amplifier with a very high impedance at the first stage. The device is still suitable for low power consumption level on a sufficiently small supply voltage. The proposed OTA architecture is designed for a purely capacitive load of around 0.5pF with a compensation capacitance of 110fF. The slew rate of the output swing is 0.0527V/μS like the gate-driven OTA suggested in [6] with a much lower gain. However, with a large gain in the amplifier designed, comes a trade-off of a lower gain-bandwidth product because of the fixed load capacitance (at 0.5pF) and the saturated bulk

transconductance of the input MOS. The compensation capacitance is formulated as 0.22 times the C_L (section 4.4) making the gain-bandwidth product much smaller compared to the gate-driven OTA. It is observed in section 5.2, that the g_{mb} is much lower than g_m for the input stage MOS device at a fixed V_{DS}. Therefore, even if one increases the aspect ratio to a significantly higher value to achieve a higher transconductance, g_{mb} will saturate after point, limiting the gain-bandwidth product. However, a UGB of 8.44MHz is a much better value compared to the existing research [1][5][6][9][25].

	This design	[1]	[5]	[6]	[9]	[25]
Technology used	180nm	350nm	350nm	-	45nm	350nm
Supply voltage (V)	0.9	2.4	0.9	1	1.5	0.8
Open-loop gain (dB)	97.14	66	62	67.81	80	66
Gain-bandwidth product (MHz)	8.44	2	0.54	0.964	2	3.4
Power consumption (uW)	3.3	2.14	9.9	7.243	26	-

Slew rate ($V/\mu S$)	0.0527	-	-	0.052	-	4.7
Phase margin	49.23° ≈ 50°	-	52	45.9	50	>80
Input	Bulk	Gate	Bulk	Gate	Gate	Twin-well bulk
Common-mode input range	0-1.2	-	0-0.9	0-0.854	-	0-0.8
Bias current	10uA	12.5uA	10uA	-	-	-

Table 6.2: Comparison for results in similar research

6.3 Future work

The proposed OTA is highly suitable for low voltage, low power consumption and it can be used in many Biomedical, Portable electronics applications with a small chip area and low supply voltage. There are multiple ongoing research on low voltage application with a reduced chip size due to the rising demands of portable and compact semiconductor technology. Several manufacturers are moving towards 5nm, 14nm and 45nm technology. As we shrink the technology, the threshold voltage, and voltage headroom due to higher V_{DS} also decreases. This gives more transconductance and a higher intrinsic gain in the MOS device at a sufficiently lower voltage (around 0.8V) [4]. With a reduced chip area, the total power consumption also decreases.

Therefore, expected gain due to such small technology will be much more stable with a faster slew rate, better phase margin, and lower bias current.

Also, the proposed circuit is designed for purely capacitive loading. For a resistive load, the gain may be compromised with a poor power consumption level. This condition can be improved by adding a buffer to the output stage or giving a feedback loop, thereby, maintaining the gain and phase margin. The circuit can also be optimized for variable supply voltages by adding DC level shifters, for a hassle-free operation with the fluctuating supply voltages shown in the section 5.7. The slew-rate is lower than expected, to enhance the device speed and slew rate the output current must be increased further enhanced which is possible in lower technology levels (like 45nm tech.) with a trade-off for subthreshold leakage and power consumption.

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Vita (biographical data)

Name of Author: Pushkar Nath Mishra

Major: MS in Electrical Engineering, Syracuse University

Work Experience

Intern, EDA Team, NXP Semiconductor Pvt. Ltd., Bangalore, India

Analog Design Engineer, NXP Semiconductor Pvt. Ltd., Bangalore, India

Teaching Assistance, Professor Jean-Daniel Mejdo, Syracuse, United States

Education

M.S. Electrical Engineering, December 2022, Syracuse University, United States

B.E. in Electronics and Communication, July 2019, BMS College Of Engineering, India