Generating Bipolar Nanosecond Pulsed Electric Field using Open Circuit Transmission Line Technique and Avalanche Transistors

Davies, Ilan; Hancock, Chris

DOI:
10.23919/EuMC48046.2021.9338198

Published: 02/02/2021

Publisher's PDF, also known as Version of record

Generating Bipolar Nanosecond Pulsed Electric Field using Open Circuit Transmission Line Technique and Avalanche Transistors

I. W. Davies[#*1] and C. P. Hancock[#*2]

[#] School of Electronic Engineering & Computer Science, Bangor University, Bangor, United Kingdom.

[*] Creo Medical Group PLC, Creo House, United Kingdom.

{[1]eeu25b, [2] c.hancock}@bangor.ac.uk

***Abstract* — A nanosecond pulse electric field generator based on relatively slow charging and rapid discharging of an open circuit co-axial transmission line through a stack of avalanche transistors operating as a fast switching element, is demonstrated. This lowcost circuit design produces well defined symmetrical bipolar nanosecond pulsed electric fields with rise and fall times less than a nanosecond. The pulse polarity (monopolar negative, monopolar positive or bipolar), duration, repetition rate and amplitude are user controllable. The new pulse generator opens the opportunity for use in a range of medical applications, including tissue sparing tumour ablation, where only the cancerous cells are destroyed.**

***Keywords* — avalanche breakdown transistors, transmission lines, nanosecond pulse electric field, biomedical engineering.**

I. Introduction

Development of nanosecond pulse electric fields (nsPEFs) generators and their applications has been a growing field in the past decade. nsPEF generators have many applications, including use in laser technologies, high speed photography, ultra-wideband radar detection and wireless communication systems to name but a few [1]-[7]. One growing application of nsPEFs is nanoelectroporation of biological cells to cause cell apoptosis for focus tumor ablation without causing damage to the extracellular matrix [3]-[7].

Nanosecond electroporation a microbiology technique where pulsed electric fields, of high amplitude, in the nanosecond (ns) time regime is applied to cells and/or tissue. Literature suggests that nsPEF or nanosecond electroporation has potential for cell manipulation and control of cell physiology. Effects include increased plasma permeability of the cell membrane, allowing chemicals, drugs, or DNA to be introduced into the cell, calcium (Ca++) release, ion channel activation and apoptosis induction [3]-[7].

There are numerous methods of generating high amplitude, nsPEFs with a rise and fall time of 2 ns. Traditionally, coaxial transmission line-based implementations, such as Blumlein, in correlation with spark gap, Marx bank, or diode and laser opening switch techniques have been used to generate high-voltage nsPEFs [1]-[2],[5]-[7]. Traditional methods have been known to be costly and have their flaws.

This paper focuses on the development of a unique low-cost design of a monopolar to a bipolar high voltage (500 V+) nsPEF generator, which is achieved through an open circuit transmission line technique in conjunction with the stacking of low-cost avalanche transistors as a fast switching element, for medical applications such as nanosecond electroporation of biological cells.

II. Theory of Operation

A. Open Circuit Co-Axial Transmission Line Technique

A transmission line can be used as a technique of generating rectangular symmetrical pulses, Fig. 1. By charging an open circuit co-axial transmission line to a voltage level V_{CC}, through a high impedance resistor, R_C, and then discharging the line into a resistive load, R_L, through a fast switching element, provides a means of producing a rectangular pulse equal in length to twice the associated delay time, 2T, of the transmission line, Fig. 1b [1],[8].

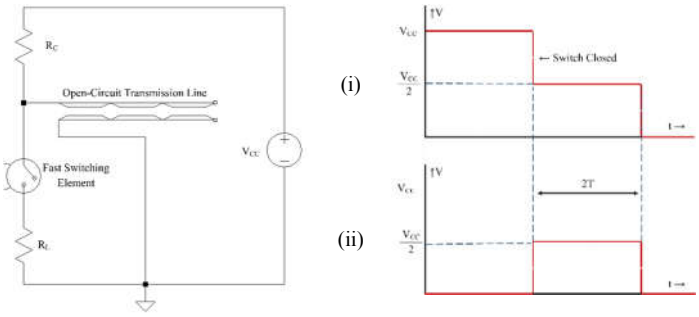

Fig. 1. Principle of a discharge line generator. (a) Basic circuit design (b) voltage waveforms at (i) the transmission line and (ii) the load [1].

The delay time, T, of the line and therefore the rectangular pulse width is determined by the open circuit coaxial transmission line parameters (1). Where l is the length of the transmission line, ε_r is the relative permittivity the co-axial transmission line and c is the speed of light (2.99×10^8 m/s).

$$T = \frac{l\sqrt{\varepsilon_r}}{2} \qquad (1)$$

The open circuit co-axial transmission line also has a characteristic impedance, Z_0. The amplitude and shape/ reflection of the incident pulse on R_L is determined by the relationship between the characteristic impedance of the transmission line, Z_0, and the incident load, R_L.

The pulse amplitude at the load, V_L, depends on the input voltage divider relationship of Z_0 and R_L in respects to the transmission lines voltage level, V_{CC} (2). Additionally, the relationship between Z_0 and R_L determines the reflection coefficient, Γ (3), and therefore the pulse shape across R_L (3).

The transmission line length determines the pulse width, the Z_0 and R_L relation determined the pulse shape/reflection and amplitude, whilst the switching element determines the pulse rise time. A single symmetrical pulse with zero reflection, is obtained when $R_L = Z_0$ (3) and the pulse associated amplitude would be $V_L = V_{CC}/2$ (2), Fig. 1.bii [1].

$$V_L = \left(\frac{R_L}{R_L + Z_0}\right) V_{CC} \quad (2)$$

$$\Gamma = \frac{R_L - Z_0}{R_L + Z_0} \quad (3)$$

B. Avalanche Transistors Technique

Avalanche transistors have been proven to be used as a fast switching element that provides reliable repeatable high-speed switching of high voltages signals with rise times as low as 300 ps [8]-[10].

Avalanche transistors are characterized by a negative resistance region in their $V_{CE} - I_C$ breakdown curve (Fig. 2). Where V_{CE} is the voltage across the collector and emitter and I_C is the current flowing into the collector. The transistors avalanche region lies between collector-emitter voltage, V_{CES} (when the base and emitter terminals are shorted together) and collector-emitter voltage, V_{CEO} (with base left open-circuit) with $I_B = 0$ and $I_E = 0$ [8]-[10].

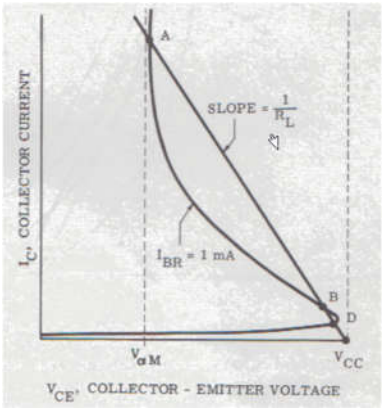

Fig. 2. Avalanche transistor VCE – IC breakdown curve; Load line for the basic bi-stable circuit for avalanche operation [8].

The rise time of the generated ns pulse is independent of the open circuit co-axial transmission line technique because of the peculiar interrelationship of the functional behaviour of the incremental avalanche capacitance and the $V_{CE} - I_C$ breakdown characteristic of an avalanche transistor curve (Fig. 2). The rise time is due to the current build-up, moving the operation point of the transistor from Point D to Point A in Fig. 2. Therefore, the avalanche transistor or the switching element determines the pulse rise-time, whilst the transmission line length determines the pulse width, and R_L and Z_0 relation determines the pulse shape/reflection and amplitude [2], [8]-[10].

In the designs presented, special function bipolar transistor, FMMT417 avalanche transistors, with avalanche breakdown voltages V_{CES} of 320 V and V_{CEO} of 100 V are used. The value for R_C is 1 MΩ, the transmission lines are RG214's co-axial lines of various length of 1 m, 5 m and 17 m, with associated delay times, T, of 5 ns, 25 ns and 85 ns, and characteristic impedance, Z_0, of 50 Ω, ε_r of 2.3. The load, R_L, of 50 Ω, unless stated otherwise. The trigger signal was a 5 V, 600 ns signal with a repletion rate of 50 Hz, unless stated otherwise.

In practice, a 50 Ω microstrip circuit was designed and etched on a double-sided copper FR4 board, and components where arranged using microwave component layout techniques to minimize reflection [11].

III. Monopolar nsPEF Circuit

A. Instrumentation

Utilizing a single avalanche transistor as a fast switching element, in conjunction with slow charging and fast discharging of an open circuit transmission line technique the maximum pulse amplitude of the nsPEF at the load R_L is limited to half the value of the transistor's collector-emitter breakdown voltage, V_{CES}, if $Z_0 = R_L$. A supply voltage, V_{CC}, above a transistors V_{CES} would permanently breakdown and damage the avalanche transistors as a switching element.

Increasing the nsPEF amplitude at R_L above V_{CES} /2 (~ 160 V) can be achieved by stacking multiple avalanche transistor in series.

The stack of multiple avalanche transistor, Fig. 3, operates like a single avalanche transistor circuit, as the open-circuit transmission line is discharge across the stacked transistors to the load. The supply voltage V_{CC}/n is dropped across each of the avalanche transistors in the series chain, where n is the number of avalanche transistor stacked. This results in a proportionally higher pulse amplitude at the load as the number of avalanche transistor stacked, n, dictates the maximum amplitude of the nsPEF at the load (4).

$$V_L = \left(\frac{R_L}{R_L + Z_0}\right) n V_{CES} \quad (4)$$

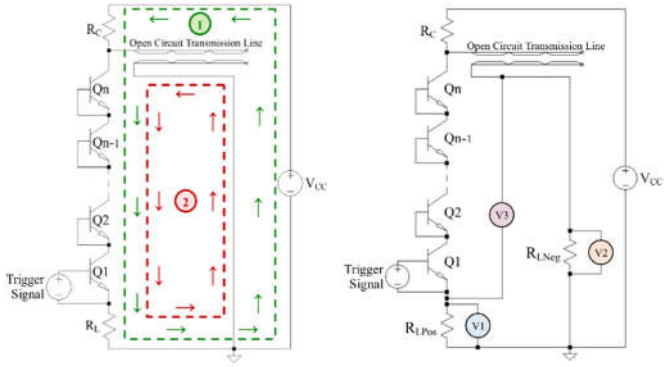

Fig. 3. Arrangement of an open circuit transmission line technique with a low-cost avalanche transistor stack to generate a (a) monopolar and (b) a bipolar nsPEF.

Initially, all the stacked avalanche transistors are in their off state, thus allowing a small current flow (loop 1 in Fig. 3(a)) to charge an open circuit transmission line via a high impedance resistor, R_C. When a positive trigger signal is applied to the base of the lowest transistor in the stack, Q1, the transistor is turned 'on' and places its collector voltage near ground potential. This results in the second transistor (Q2) having twice the collector-emitter voltage, creating the desired condition in terms of overvolting and therefore causes a non-destructive avalanching of Q2. This creates a sequential 'knock-on' effect of non-destructive avalanching of the transistors within the stack beyond Q1's threshold, to the final avalanche transistor in the stack, Qn, which is placed near the charged open circuit transmission line. When Qn is turned 'on', the charged open circuit transmission line to discharge through the stacked transistors, as a high current along loop 2 in Fig. 3(a) and producing a nsPEF pulse at R_L. The monopolar pulse produced at R_L in Fig. 3(a) has a positive polarity with a fast rise time, a width of 2T(1) and a relative pulse amplitude of V_L(4) with

repetition rate exact to the repletion rate of the trigger signal to the base of Q1.

(a)

(b)

(c)

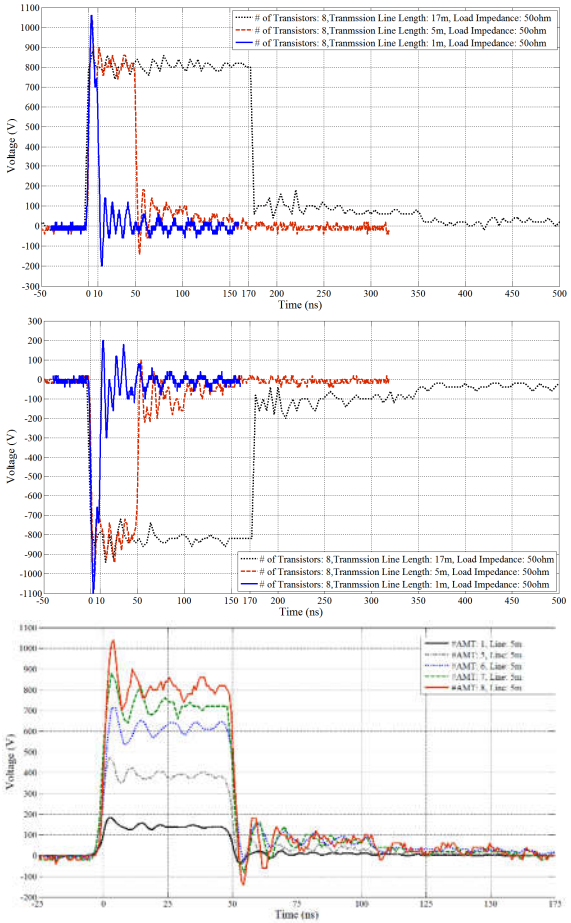

Fig. 4 Measured nsPEF result with 8 avalanche transistors stacked with a 17 m (black, dotted line), 5m (red, dashed line) and 1m (blue line) transmission line across a 50 Ω load located at (a) R_{LPos} only (Fig. 3(a)) and (b) R_{LNeg} only in Fig. 3(b). (c) comparing pulse amplitude of stacking of a single (black line), 5 (gray, dot-dashed line), 6 (blue, dotted line), 7 (green, dashed line) and 8 (red line) avalanche transistors with a 5m transmission line (Fig. 3(a)).

Manipulating the load position along high current loop 2 in Fig. 3(a) determines the incident pulse polarity on R_L. Placing R_L in series with the emitter of Q1 to ground (R_{LPos} in Fig. 3(b))a positive nsPEF should be observed whilst a negative nsPEF would be present across R_L when the load is placed in series with the outer conductor of the open-circuit transmission line to ground (R_{LNeg} in Fig. 3(b)).

B. Result and Analysis

Fig. 4(a) and (b) shows the measured nsPEF width is determined by the transmission line length (1), as a pulse width 10 ns, 50 ns, 170 ns is produced by 2T of a line length of 1 m line (T = 5 ns), 5 m line (T = 25 ns) and 17 m line (T= 85 ns) respectively. Fig. 4(c) demonstrates that stacking multiple avalanche transistors in series produces a higher pulse amplitude on R_L. With every avalanche transistor added to the stack the pulse amplitude increases by an estimated $V_{CES}/2$, confirming (4). All the nsPEF in Fig. 4 have identical sub-nanosecond rise times which emphasizes that the avalanche transistors determine this parameter of the nsPEF. Comparing Fig. 4(a) and (b) illustrates that the placement of the load within the circuit and the high current along loop 2 in Fig. 3(a) determines the pulse polarity of the nsPEF only as the attributes of the counterpart pulses in Fig. 4(b) are identical to Fig. 4(a).

IV. Bipolar nsPEF Circuit

A. Instrumentation

The bipolar nsPEf circuit operation, highlighted in Fig. 3(b) is identical to the monopolar designs, where the charged transmission line is discharged through the stacked avalanche transistors across a load. The difference is that multiple loads, R_{LPos} and R_{LNeg} is present in the circuit producing a total load, $R_{L\Sigma}$ ($R_{L\Sigma} = R_{LPos} + R_{LNeg}$), between the transmission line outer conductor and the emitter of Q1.

Depending on the voltage difference reference points within the high current flow loop (2), of the circuit in Fig. 3(b), three nsPEF can be observed. The voltage differences are V1, V2 and V3 in Fig 3(b). A positive nsPEF is observed across R_{LPos} (V1) whilst a negative nsPEF of identical attributes is observed across R_{LNeg} (V2). The nsPEF observed across V3 is a positive nsPEF of amplitude $V_{L\Sigma}$ across a total load, $R_{L\Sigma} = R_{LPos} + R_{LNeg}$. The nsPEF observes at V3 has an amplitude comprising of the peak-to-peak voltage of both V_{LPos} and V_{LNeg} ($V_{L\Sigma} = V_{LPos} + V_{LNeg}$). Therefore, (2) can be rewritten as (5) to determine the amplitude of the three nsPEF observed at point V1, V2 and V3 in Fig. 3(b).

$$V_{L\Sigma} = \left(\frac{R_{L\Sigma}}{R_{L\Sigma} + Z_0}\right) nV_{CES} = V_{LPos} + V_{LNeg}$$
$$V_{LPos} = \left(\frac{R_{LPos}}{R_{LPos} + R_{LNeg}}\right) V_{L\Sigma}, \quad V_{LNeg} = \left(\frac{R_{LNeg}}{R_{LPos} + R_{LNeg}}\right) V_{L\Sigma} \tag{5}$$

As the total load of the circuit differs in a bipolar design, the reflection coefficient (3) can be re-written as (6). (6) implies that for a single symmetrical nsPEF with zero reflection the total impedance, $R_{L\Sigma}$, of the load must amount to Z_0 and the pulse associated at V3 would be $V_{L\Sigma} = V_{CC}/2$ (5).

$$\Gamma = \frac{R_{L\Sigma} - Z_0}{R_{L\Sigma} + Z_0} = \frac{(R_{LPos} + R_{LNeg}) - Z_0}{(R_{LPos} + R_{LNeg}) + Z_0} \tag{6}$$

Considering equations (5) and (6), a single symmetrical bipolar nsPEF pulse of positive and negative pulses of identical attributes and amplitudes can be achieved if $R_{LPos} = R_{LNeg} = R_{L\Sigma}/2 = Z_0/2$. Alternatively, the amplitude of the positive (V_{LPos}) and negative (V_{LNeg}) nsPEF can differ. The difference between the V_{LPos} and V_{LNeg} is dependent on the impedance ratio between R_{LPos} and R_{LNeg}. i.e. if $R_{LPos} = R_{LNeg}$ then $V_{LPos} = V_{LNeg}$. If $R_{LPos} > R_{LNeg}$ then $V_{LPos} > V_{LNeg}$. If If $R_{LPos} < R_{LNeg}$ then $V_{LPos} < V_{LNeg}$. In all the cases mention $V_{L\Sigma}$ will always be $V_{LPos} = V_{LNeg}$ and all the nsPEF will have zero reflection if $R_{LPos} + R_{LNeg} = R_{L\Sigma} = Z_0$. All three nsPEF at V1, V2 and V3 are produce simultaneously.

B. Result and Analysis

All the nsPEFs in Fig. 5 have identical sub-nanosecond rise times which emphasizes that the avalanche transistors determine this parameter of the nsPEF. nsPEFs in Fig. 5 demonstrates that the transmission line length determines the pulse width, 2T (1). Transmission line length of 1 m, 5 m and 17 m produced a nsPEF widths of 10 ns, 50 ns and 170 ns respectively.

Fig. 5 (a) and (b) emphasizes (5) and (6) as the relationship between Z_0 and $R_{L\Sigma}$ determines the nsPEFs pulse shape/reflection and amplitude in this bipolar nsPEF generator

design. Fig. 5(a) illustrates the measured nsPEFs when $R_{L\Sigma}$ = 50 Ω and whilst $R_{L\Sigma}$ = 100 Ω in Fig. 5(b), with R_{LPos} = R_{LNeg} in both cases. This is highlighted (6) largely, via a square box in Fig. 5(b), as a reflection of the incident pulses is clearly shown with $R_{L\Sigma}$ = 100 Ω, while no reflection is seen in Fig. 5(a).

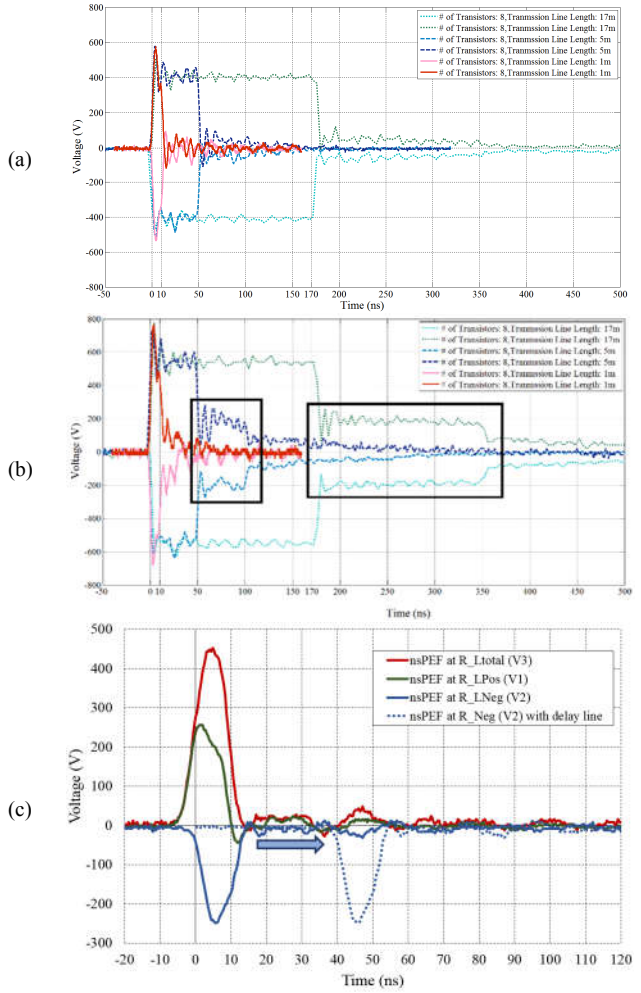

Fig. 5 nsPEF measured across R_{LPos} (dark colour) and R_{LNeg} (lighter colour) with a 1 m, 5 m and 17 m transmission line in circuit Fig. 3(b) with a total load, $R_{L\Sigma}$, of (a) 100 Ω (R_{LPos}= R_{LNeg} = 50 Ω) and (b) 50 Ω (R_{LPos}= R_{LNeg} = 25 Ω). (c) PEF measured across voltage difference V1 (V_{LPos}), V2 (V_{LNeg}) and V3 ($V_{L\Sigma}$) with a 1m T = 5 ns) transmission line.

Fig. 5(c) shows the measured nsPEF at the three-voltage difference point (V1, V2 and V3) in Fig. 3(b), with five avalanche transistors stacked, 1 m transmission line and R_{LPos} = R_{LNeg} = 25 Ω. All three nsPEF have identical pulse attributes except for there amplitude. The amplitude of V1 (V_{LPos}) and V2 (V_{LNeg}) are identical, and V3 ($V_{L\Sigma}$) amplitude identifies with the peak to peak voltage of V2 and V1, thus emphasising (5).

The bipolar nsPEF observed in Fig. 5 have little practical utility in nanosecond electroporation and other medical applications, whereas the ability to space up the two phases is hugely interesting for electroporation applications [3]-[5]. Placing a delay line prior to a or both loads it possible to manipulate the delay between the two pulses. The delay between the pulse will be the delay time - pulse width. A possible example of this, if employed, is dementated in Fig. 5 (c) as V_{LNeg} would delay the incident pulses of $V_{L\Sigma}$ and V_{LPos} by 40 ns if an 8 m delay line was implemented. To minimise reflection the delay line impedance must match its load. This have been proven in simulation.

V. Conclusion

Utilizing microwave design techniques to relatively slowly charge and rapidly discharge of a co-axial transmission line, in conjunction with a stack of low-cost avalanche transistors operating as a fast switching element can produce monopolar and bipolar nsPEF with the following attributes:

- Variable pulse width control, determined by the transmission line length (1) (Fig. 4(a) and (b));
- Variable pulse repetition rate at the load, determined by the controller trigger signal repetition rate;
- Variable pulse amplitude by switching in or changing the number of avalanche transistors stacked. Provides the ability to increase the amplitude of the pulse at the load (Fig. 4(c));
- Variable pulse polarity by changing the location of the load in relation to the transmission line (Fig. 4(a) and (b));
- The relation between the loads (R_{LPos}, R_{LNeg}, R_{LTotal}) to the Z_0 manipulates the monopolar and bipolar nsPEF shape (Γ) and amplitude (2), (3), (5), (6), (Fig. 6(a) and (b));
- The ability to space up the two phases of the bipolar pulses through the introductions of delay lines (Fig. 6(c));

This combination of transmission line theory and stacking of avalanche transistors has shown to produce well-defined symmetrical monopolar or bipolar nsPEF with rise and fall times less than a nanosecond, and adjustable amplitude and repetition rate to support nanosecond electroporation and other biomedical applications of nsPEF in a cost-effective manner.

Acknowledgment

This project has received funding from the European Union's Horizon 2020 research and innovation program under grant agreement No 737164.The authors would like to thank Creo Medical for their continued support in this project and for providing access to their equipment and expertise. Any IP that comes from this work is owned by Creo Medical Group PLC.

References

[1] W. Meiling and F. Stary, Nanosecond pulse techniques. New York: Gordon and Breach, 1970, p. 304.
[2] L. Jinyuan, S. Bing and C. Zenghu, "High voltage fast ramp pulse generation using avalanche transistor", Review of Scientific Instruments, vol. 69, no. 8, pp. 3066-3067, 1998.
[3] R. Sundararajan, Electroporation-based therapies for cancer from basics to clinical applications. Waltham, MA: Woodhead Pub, 2014.
[4] A. Pakhomov, Advanced electroporation techniques in biology and medicine, CRC Press, 2017.
[5] J. Weaver, "Electroporation of cells and tissues", IEEE Transactions on Plasma Science, vol. 28, no. 1, pp. 24-33, 2000.
[6] P. Wijetunga, X. Gu, T. Vernier, A. Kuthi, M. Behrend and M. A. Gundersen, "Electrical modeling of pulsed power systems for biomedical applications," Digest of Technical Papers. PPC-2003. 14th IEEE International Pulsed Power Conference (IEEE Cat. No.03CH37472), Dallas, TX, USA, 2003, pp. 423-428 Vol.1.
[7] M. Reberšek and D. Miklavčič, "Advantages and Disadvantages of Different Concepts of Electroporation Pulse Generation", Automatika, vol. 52, no. 1, pp. 12-19, 2011.
[8] W. Roehr, Switching transistor handbook. Motorola Inc., 1975
[9] N. Chadderton, The ZTX415 Avalanche Mode Transistor: An Introduction to Characteristics, Performance and Applications., Zetex, Application note 8, Issue 2, 1996
[10] Zetex, The ZTX413 Avalanche Mode Transistor: Low Voltage Operation up to 50A., Zetex, Design note 24, 1995
[11] B. Wadell, Transmission line design handbook. Boston, Mass.: Artech House, 1991.