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All-Standard-Cell-Based Analog-to-Digital Architectures Well-Suited for Internet of Things Applications

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Abstract: In this paper, the most suited analog-to-digital (A/D) converters (ADCs) for Internet of Things (IoT) applications are compared in terms of complexity, dynamic performance, and energy efficiency. Among them, an innovative hybrid topology, a digital–delta (Δ) modulator (ΔM) ADC employing noise shaping (NS), is proposed. To implement the active building blocks, several standard-cell-based synthesizable comparators and amplifiers are examined and compared in terms of their key performance parameters. The simulation results of a fully synthesizable Digital-ΔM with NS using passive and standard-cell-based circuitry show a peak of 72.5 dB in the signal-to-noise and distortion ratio (SNDR) for a 113 kHz input signal and 1 MHz bandwidth (BW). The estimated FoM_{Walden} is close to 16.2 fJ/conv.-step.

Keywords: analog-to-digital converters; high resolution; digital–delta modulator ADC; noise shaping; all-standard-cell-based; Internet of Things

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1. Introduction

The Internet of things (IoT) is heavily driven by significant semiconductor and nanotechnology breakthroughs. Low-cost, reliable, and highly integrated circuits and systems have been designed, allowing for the introduction of important features such as remote access control and the operation of large amounts of data [1].

High-resolution analog-to-digital (A/D) converters (ADCs) are relevant building blocks in different IoT systems. Applications such as high-precision sensor networks, communications, imaging, and signal processing require outstanding ADC performance, including high-accuracy, low-power consumption, and, in some cases, wide-bandwidth (BW) specifications [2].

To accomplish a high resolution, delta-sigma (ΔΣ) modulators (ΔΣM) and successive approximation register (SAR) ADCs (SAR-ADCs) are frequently utilized. While in ΔΣM, larger sampling frequencies (F_S) are used to achieve higher resolutions, in conventional SAR-ADCs, energy efficiency is often sacrificed to reach the target resolution. Furthermore, old-fashioned architectures and techniques were revisited, and hybrid structures are currently a reality, mixing these schemes with popular structures. Employing noise shaping (NS) in an SAR-ADC and using a delta modulation in a ΔΣM, resulting in a delta-delta-sigma (ΔΔΣ) modulator (ΔΔΣM), are examples of this new era of hybrid ADC architectures pursuing the most outstanding and efficient ADC [3–5].

Taking into consideration that the ADC design is a complex and time-consuming task, it is desirable to reduce this effort, especially when porting between different nodes or technologies is required. Moreover, the lower nodes' technology constraints (low intrinsic

gain, reduced supply voltage, leakage current, etc.) bring other challenges in porting tasks, sometimes requiring a complete redesign or the implementation of different circuit schemes.

Circuits based on digital logic can be quickly realized and modified to accomplish specifications and technological changes. Therefore, the use of digital circuits is becoming popular in analog or mixed-signal circuit design, such as in the case of ADCs. Consequently, synthesizable solutions using standard cells are used to further reduce redesign time and effort [6–8].

In this work, the most-suited ADC architectures for IoT applications are described. A hybrid ADC solution, a digital–delta (Δ) modulator (ΔM) with NS, is proposed that can be implemented using only passive and digital circuitry based on standard cells. Circuit details and some simulation results are also provided.

This paper is organized as follows. Section 2 presents the most popular ADC architectures for IoT applications, where complexity, dynamic performance, and energy efficiency are compared. In Section 3, some standard-cell-based active building blocks, comparators, and integrators, are presented with reference to their advantages and the main challenges during their integration in complex systems. Section 4 provides schematic details regarding the proposed standard-cell-based digital-ΔM employing NS and some simulation results. Lastly, the main conclusions are drawn in Section 5.

2. Most-Suited Analog-to-Digital Converter (ADC) Architectures for Internet of Things (IoT)

The most suited ADC architectures for IoT applications are described in this section. In spite of being an old-fashioned topology and not directly implemented in IoT applications, ΔM is mentioned because it is the basis of ΔΣM and has inspired some other hybrid architectures, such as SAR-ADC with NS, ΔΔΣM or the proposed digital-ΔM with NS ADCs.

Lastly, a qualitative comparison between them is provided considering complexity, dynamic performance, and energy efficiency.

2.1. Delta Modulator (ΔM) ADC

In a patent from 1946 submitted by Deloraine et al., delta modulation was referred to for the first time as a method to transmit analog data by means of a one-bit code [9].

As shown in Figure 1a, the basic ΔM transforms an analog input signal, V_{in}, into a synchronous digital output, D_{out}. It employs a 1-bit quantizer, a digital-to-analog (D/A) converter (DAC), and an integrator in the feedback path as an attempt to anticipate the input signal. Thus, this integrator acts as a predictor [10].

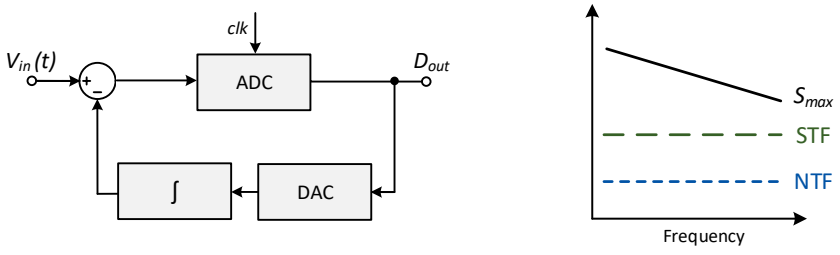

Figure 1. ΔM ADC: (**a**) block diagram and (**b**) illustrative magnitude of STF, NTF and S_{max}.

Noise can negatively impact ΔM performance in two different ways: through granular noise or slope overload. While the former results from the quantization of a continuous signal (the signal is forced to assume a discrete value), the latter is dominant when the step size of the integrator is too small, resulting in the incorrect tracking of the input signal [10,11].

Despite the good robustness to transmission errors, simple filtering requirements, and low associated complexity, the nonidealities associated with the integrator in the

feedback path can limit linearity, noise performance, and system accuracy. Furthermore, the amplitude of V_{in} and ADC performance are inversely proportional to the input signal frequency, F_{in}. Therefore, as Figure 1b illustrates, while the signal transfer function (STF) and the noise transfer function (NTF) are constant, the maximal signal, S_{max}, decreases with the frequency [5].

Both noise and nonidealities can be problematic and severely restrict the maximal dynamic performance of the converter [4].

2.2. SAR-ADC with Noise Shaping (NS)

SAR-ADCs are currently one of the most popular topologies to realize A/D conversion due to their energy efficiency, low die area, and low circuit complexity [12]. However, higher resolutions are difficult to achieve without sacrificing energy efficiency.

In conventional topologies, the circuit relies essentially on a 1-bit comparator, an N-bit DAC, and a sample-and-hold (S/H) block. A binary-search algorithm is used to reduce the analog residue to less than one least significant bit (LSB) [13].

Like in other architectures, the most critical building block is the DAC because its nonidealities, the associated noise, and its settling time dominated by the reference settling directly affect the ADC performance. This aspect is even more crucial for high-resolution converters.

In the last decade, the introduction of oversampling and NS in the conventional SAR-ADC allowed for better higher dynamic performance beyond 14 bits of resolution (i.e., 12.5 bits of effective number of bits (ENOB)) [3]. The main idea is to use the analog residue that still remains after the SAR operation, the residue voltage (V_{res}), and integrate it to perform a NS, spreading the noise through a higher BW than the band of interest. The block diagram of a SAR-ADC employing NS is shown in Figure 2a, in which the ADC can simply be a single comparator. In Figure 2b, the STF, NTF, and S_{max} magnitudes as a function of frequency are illustrated, with the NTF slope characteristic from systems employing NS being notable.

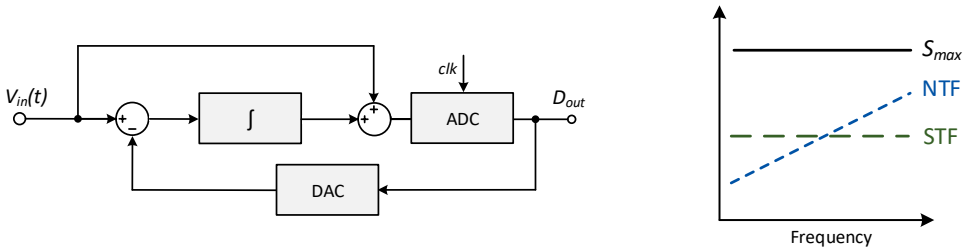

Figure 2. SAR-ADC employing NS: (**a**) block diagram and (**b**) illustrative magnitude of STF, NTF and S_{max}.

Given the absence of amplifiers in the pure topology (besides the comparator), in these hybrid structures, the same strategy has been pursued, maintaining the circuit simplicity, and relaxing the specifications of the comparator and DAC [14]. Thus, different works have been proposed using passive NS structures [15–17].

2.3. First-Order Delta–Sigma (ΔΣ) Modulator (ΔΣM) ADC

The ΔΣM topology emerged to avoid the shortcomings of the ΔM by moving the integrator from the feedback to the forward path. As illustrated in Figure 3a, in which the local quantizer (ADC) can again simply be a single comparator, the integrator operates over the error difference instead of the signal estimation, as in the ΔM case.

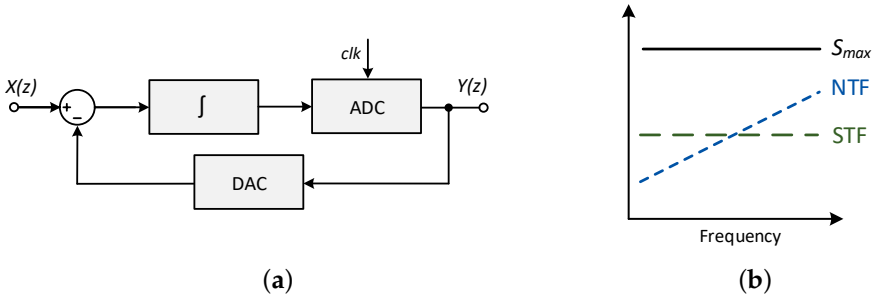

Figure 3. First-order ΔΣM ADC: (**a**) block diagram and (**b**) illustrative magnitude of STF, NTF and S_{max}.

This architecture relies essentially on an analog filter (integrator), a quantizer, and a DAC [4,11]. Using the linear additive white-noise model for the quantizer, this system can be represented in the Z domain, resulting in the following STF and NTF:

$$STF(z) = \frac{H(z)}{1 + H(z)} \tag{1}$$

$$NTF(z) = \frac{1}{1 + H(z)} \tag{2}$$

where $H(z)$ is the integrator transfer function. The NS effect is more effective for higher $H(z)$ filter orders, promoting higher-resolution converters; however, extra complexity is added to the system. These functions are represented in Figure 3b.

2.4. Delta–Delta–Sigma (ΔΔΣ) Modulator (ΔΔΣM) ADC

ΔΔΣM is another example of a hybrid architecture. Combining delta modulation with a 1st-order ΔΣM, ΔΔΣM was proposed in [5]. As depicted in Figure 4a, two integrators are used in this topology, one in the feedforward and another in the feedback paths.

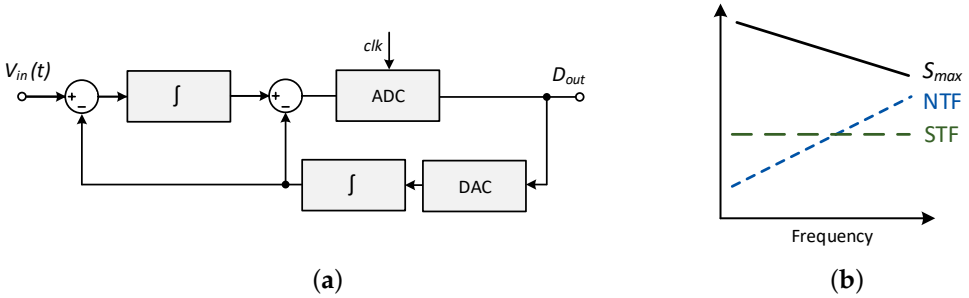

Figure 4. ΔΔΣM ADC [5]: (**a**) block diagram and (**b**) illustrative magnitude of STF, NTF and S_{max}.

Since two integrators are involved, the complexity of the architecture is higher. Furthermore, the nonidealities of the DAC (placed in the feedback path) impact the ADC linearity. Thus, a high dynamic resolution is difficult to achieve, especially with low energy efficiency. Despite the inherent complexity, small modifications can be performed to the architecture, such as changing the relative position of the DAC and integrator in the feedback path. The integrator becomes a digital accumulator, reducing the complexity and rendering the architecture more suitable for IoT.

As represented in Figure 4b, while the NS imposes an inclination to the NTF curve, shaping the noise for higher frequencies, delta modulation impacts the S_{max} (similarly to the ΔM topology).

2.5. Proposed Hybrid ADC: Digital–Delta (Δ) Modulator (ΔM) with Noise Shaping (NS)

A digital-ΔM employing NS was initially proposed by the authors of this paper in [18]. It utilizes oversampling and NS to improve the overall performance by minimizing

the impact of thermal and quantization noise. As depicted in Figure 5, it comprises a 1-bit comparator, an accumulator, an N-bit DAC, an S/H circuit, and an integrator in the NS section.

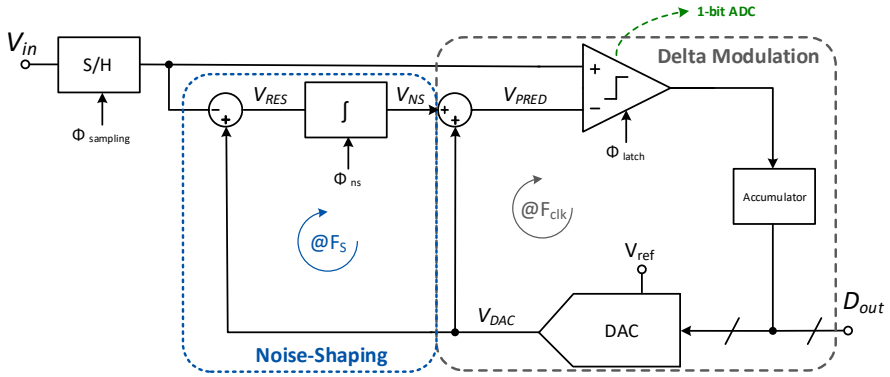

Figure 5. Diagram of the proposed digital-ΔM ADC employing NS.

This architecture was initially inspired by an SAR-ADC. However, instead of the typical SAR logic, this topology uses an accumulator in the digital domain. Therefore, the search algorithm is based on the prediction of the next V_{in} working as a ΔM.

Comparing the block diagram of the proposed ADC architecture, depicted in Figure 6a, with other topologies shows that the comparator also connects to the sampled V_{in} to perform a direct comparison with the estimation. Additionally, this architecture employs an accumulator placed between the comparator and the DAC, which is a relevant advantage to achieve a fully synthesizable ADC. However, since this topology utilizes delta modulation, S_{max} is dependent on the frequency (Figure 6b).

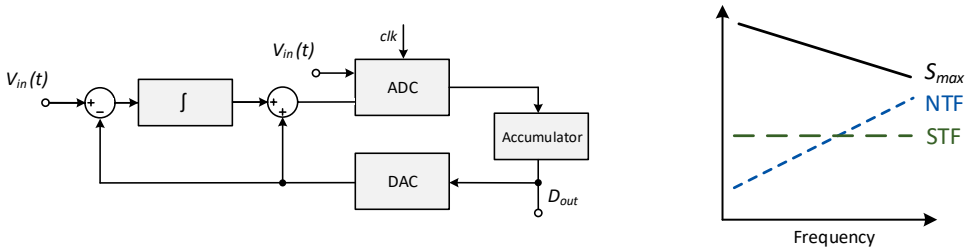

Figure 6. Proposed digital-ΔM employing NS: (**a**) block diagram and (**b**) illustrative magnitude of STF, NTF and S_{max}.

2.6. Comparison among the Most-Suited Architectures

All the described architectures are qualitatively compared in Table 1.

In all the described topologies, the most critical building blocks are the comparator, integrator, and the DAC, since their nonidealities impact ADC performance. However, depending on the ADC architecture and the circuit location, their effect can be distinct.

Generally, SAR-ADC and digital-ΔM, both employing NS, present higher complexity when compared with ΔΣM or ΔΔΣM ADCs because the specifications of the main building blocks (metastability, comparator's accuracy and comparison times, noise, etc.) have strong repercussions on ADC performance. However, they present very good energy efficiency, increasing their attractiveness. ΔΣM or ΔΔΣM ADCs are also popular for high-resolution applications. However, the integrator design can, in some cases, be problematic for circuit stability and efficiency.

The magnitude of S_{max} can show different behaviors depending on the architecture; therefore, despite the conclusions depicted in Table 1, this aspect should be taken into account to ensure that it does not represent a strong limitation for the specific IoT application.

Table 1. Comparison of the most-suited ADC architectures for IoT applications.

ADC Architecture	Complexity	Resolution	Energy Efficiency
ΔM	Low	Moderate	Low
SAR-ADC with NS	Moderate	Moderate/high	Very good
First-order ΔΣM	Low	Moderate/high	Good
ΔΔΣM	Moderate	Moderate/high	Good
Digital-ΔM with NS	Moderate	Moderate/high	Very good

3. Standard-Cell-Based Active Building Blocks

The implementation of the different architectures presented earlier demands different specific circuits to implement the distinct functional blocks that each topology requires. Typically, integrator synthesis encompasses the design of OTAs, and quantizers involve comparator design. Among others, these are fundamental building blocks of converters.

Over the years, different standard-cell-based circuits, recurring to automated digital design flows and standard cells, have been proposed to implement these well-known analog functions, enabling faster design, and synthesis and layout automation based on standard cells.

Despite the importance of the DAC in all architectures, its design has preferably been passive, facilitating the converter porting between different nodes or technologies. Furthermore, the passive characteristics allow for good energy efficiency, which is extremely relevant for IoT applications. For these reasons, this building block is not described here.

3.1. Dynamic Comparators Using Standard Logic Circuitry

A fully synthesizable dynamic voltage comparator was proposed by Weaver et al. in [19]. As depicted in Figure 7, the circuit relies on a two cross-coupled 3-input digital NAND gates and, when two NANDs are connected, assuming that the common-mode voltage of the input signal is high enough to cut off the input *PMOS* devices, an analog-input comparator is created. When the clock is low, the outputs are reset to the positive supply rail, V_{DD}, and when the clock goes high, the outputs start to discharge through the *NMOS* devices. Since the discharging rate is proportional to the input, once one of the outputs achieves a value below than the threshold voltage, the cross-coupled connection forces the outputs to assume the supply rail values. A static SR latch is also used to hold the output decision and it is buffered by an inverter to reduce the memory effect.

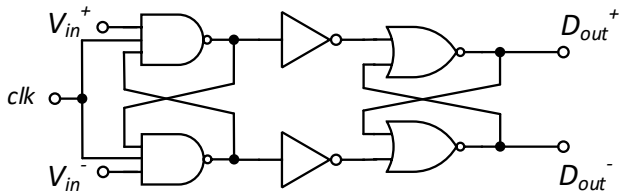

Figure 7. GATE-based comparator proposed by Weaver et al. [19].

In spite of being suitable for an all-digital implementation, this circuit is sensitive to the input common-mode range. Consequently, the usage of this comparator is restricted to stochastic ADCs [20].

Replacing NAND gates with NOR gates, as shown in Figure 8, the comparator only operates correctly if the input common-mode voltage is close to the ground. Thus, merging the 3-input NAND with 3-input NOR solutions, a rail-to-rail dynamic voltage comparator was proposed in [20]. In this case, NAND gates operate correctly for the portion of the common-mode towards V_{DD}, while NOR gates work properly for the portion towards the ground.

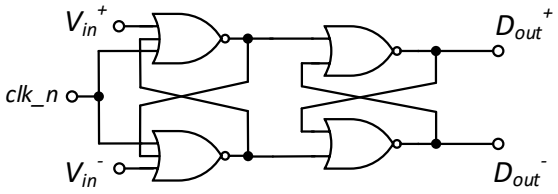

Figure 8. NOR-based comparator that was merged with the NAND-based circuit (shown in Figure 7), producing the proposed rail-to-rail dynamic voltage comparator by Aiello et al. described in [20].

Ojima et al. proposed an NAND-based 4-input clocked comparator to achieve a fully synthesizable SAR ADC [21]. As Figure 9 shows, the four 3-input NAND gates define the preamplifier and the first latch stage (the output of one pair of preamplifiers is fed back to the input of the other pair), while the following 2-input NAND gates form the second latch stage, enhancing the comparator gain and reducing the comparison time. In this scheme, the comparison is carried out on the basis of ($V_{IN}{}^{+} + V_{DAC}{}^{+}$) and ($V_{IN}{}^{-} + V_{DAC}{}^{-}$).

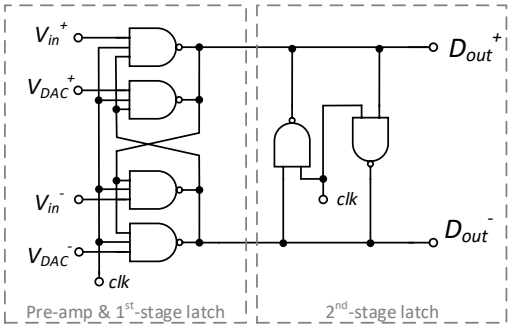

Figure 9. NAND-based four-input clocked comparator proposed by Ojima et al. [21].

In the previous scheme, when the V_{in} was low and the *clk* was disabled, the reset path of the *NMOS* of the preamplifier was cut off. Consequently, a residue voltage remained at the drain node that could be amplified during the next comparison, generating an error output. To resolve that, it was proposed to replace the NAND gates with OR–AND inverter (OAI) cells [6]. Thus, an explicit reset is performed on the drain nodes, eliminating the residue voltages and thereby reducing the probability of a wrong output.

On the basis of the described 4-input solution [6], a 2-input comparator based on the same OAI cells was designed (Figure 10). In addition to the obvious reduction in complexity and power dissipation, because fewer transistors are used, this topology presents satisfactory characteristics (comparison time, noise, and output error probability) for simple ADC topologies such as SAR-ADCs and digital-ΔM, both with NS.

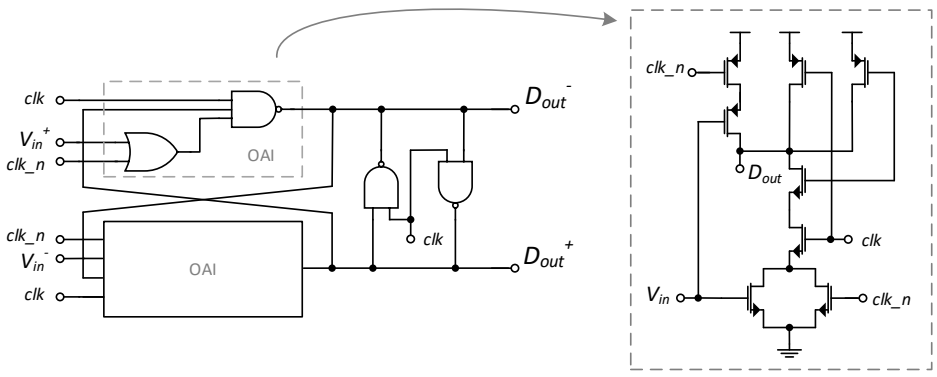

Figure 10. OAI-based comparator with 2 inputs.

Recently, different works have been proposed with the goal of achieving rail-to-rail dynamic voltage comparators with good energy efficiency [22,23].

3.2. Inverter-Based OTA Topologies

Amplifiers are also difficult to design and to port between technologies. Thus, standard-cell-based synthesizable solutions have been drawing attention in recent years. Inverter-based switched-capacitor (SC) circuits are one possibility that has been deeply studied due to the inherent simplicity and capability to operate with low V_{DD}, in contrast with other operational transconductance amplifiers (OTAs).

A simple inverter allows for a push–pull operation, a large output swing (OS), and good energy efficiency. Furthermore, both devices contribute to global transconductance [24]. However, taking into consideration that the inverter does not have an explicit reference virtual ground, different cancellation techniques have been investigated to compensate the offset voltage, V_{off}, and reduce its impact [25].

The technique proposed by Nagaraj et al. in [26] is one of the most used approaches. Besides the offset impact reduction, it requires a lower gain specification, facilitating its design. In this scheme, depicted in Figure 11, while capacitors C_S and C_F perform the integration, the C_{NAG} is used to compensate for the finite gain error and V_{off} [25–27].

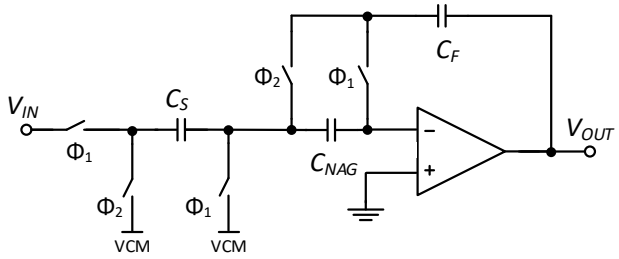

Figure 11. Scheme of the SC integrator proposed by Nagaraj et al. [26].

There are some relevant specifications with which OTAs need to comply in order to render them good candidates for employment in ADCs, namely, the gain and its linearity over V_{out}, since it affects ADC linearity, low complexity, and good energy efficiency. These are fundamental requirements to be observed, especially for IoT and fully synthesizable applications.

Thus, the key performance parameters of three different OTA topologies were evaluated in [28]. The circuits, *OTA 1*, *OTA 2* and *OTA 3*, can be described as follows:

- *OTA 1*: a single pseudodifferential Nagaraj integrator with a fully passive SC common-mode feedback (CMFB) circuit, as illustrated in Figure 12 [24].
- *OTA 2*: a pseudodifferential with a three-stage multipath inverter-based amplifier using a RC network as CMFB, as shown in Figure 13 [29].
- *OTA 3*: a single-path three-stage pseudodifferential Nagaraj integrator using a fully passive SC CMFB, as shown in Figure 14.

As summarized in Table 2, there are significant differences between these three OTA circuits. Since a cascade of inverters was used in *OTA 2* and *OTA 3*, a higher DC gain was achieved. However, this also increased the complexity. Furthermore, the RC network utilized in *OTA 2* as CMFB increased the current consumption. Regarding the linearity over V_{out}, significant differences were also noticed with *OTA 2* and *OTA 3* being the best options when the linearity of the OTA is extremely important in the system, such as in the case of ADCs.

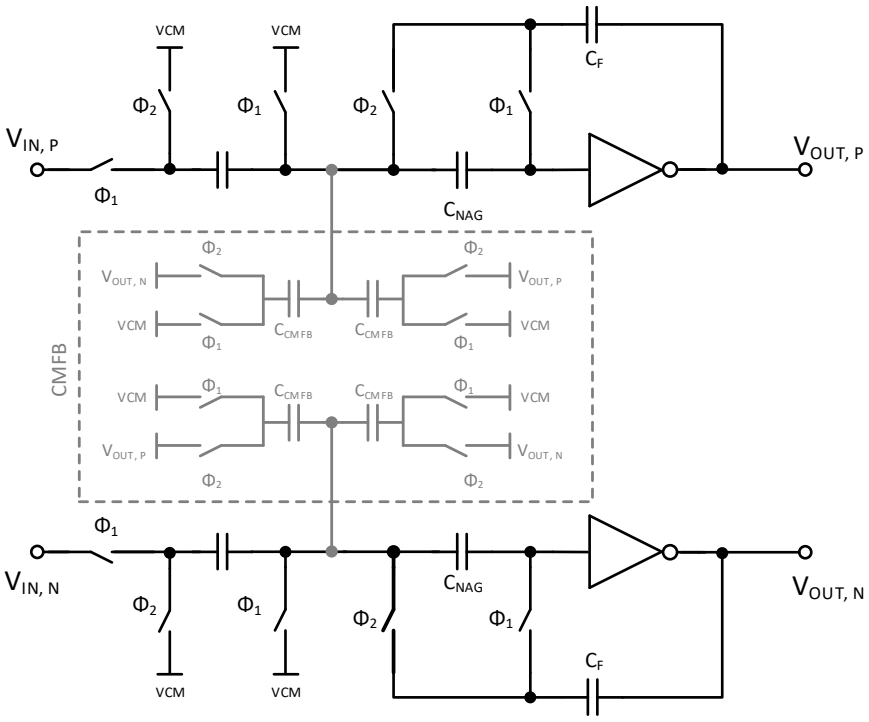

Figure 12. *OTA 1*: a pseudodifferential inverter-based Nagaraj integrator with a fully passive SC CMFB circuit [24].

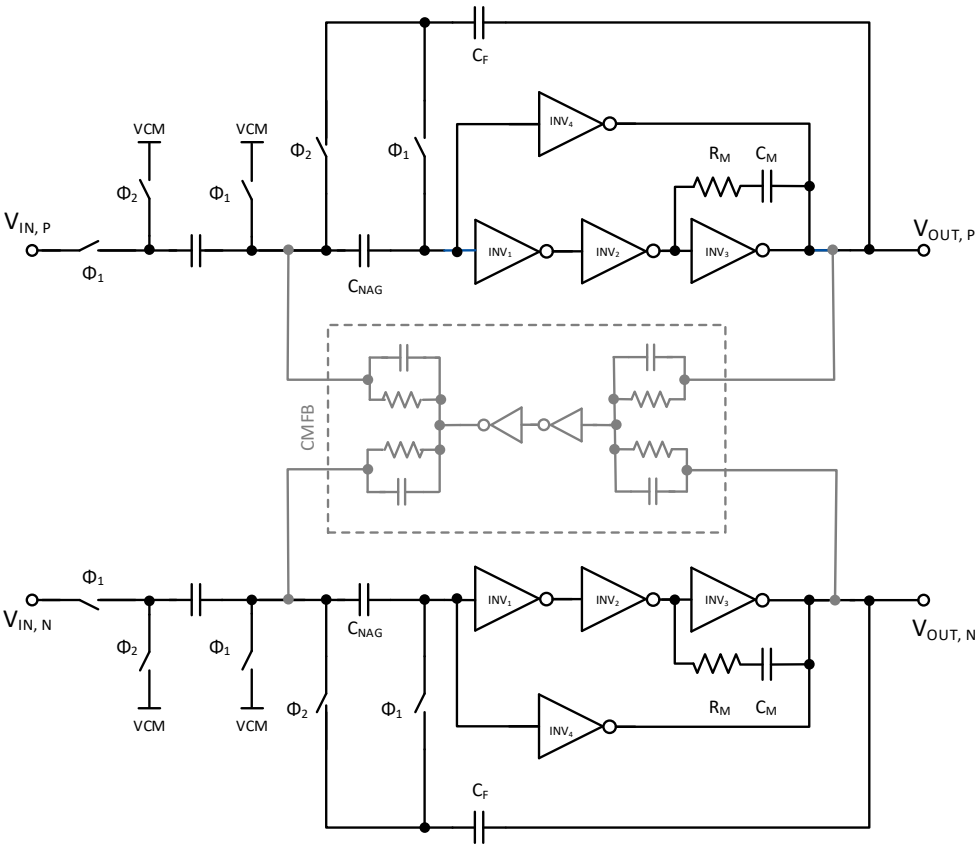

Figure 13. *OTA 2*: a pseudodifferential with a three-stage multipath inverter-based Nagaraj integrator [29].

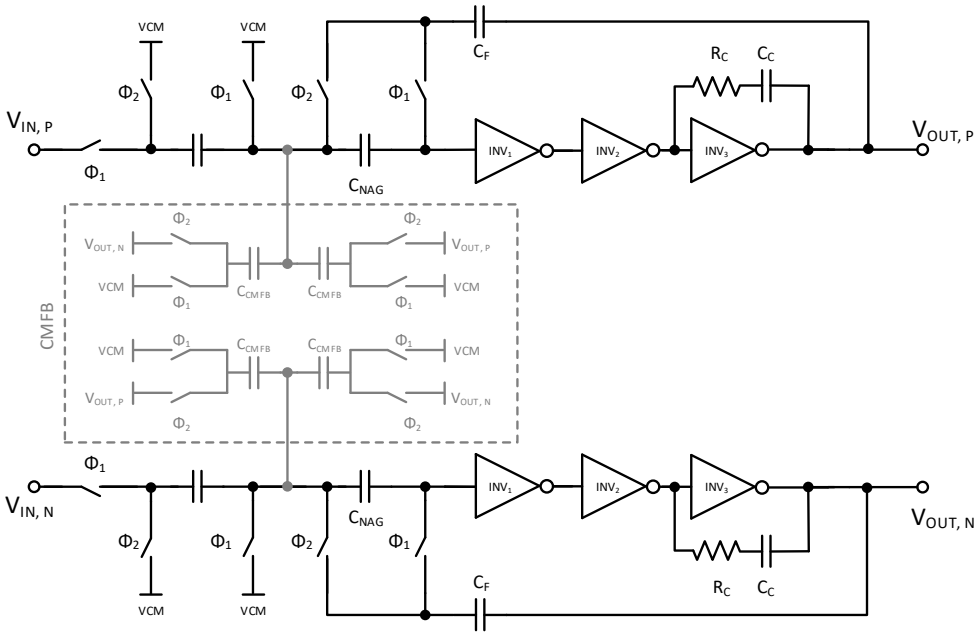

Figure 14. *OTA 3*: a single path three-stage pseudodifferential Nagaraj integrator using a fully passive SC CMFB circuit [28].

Table 2. Dynamic performance for the three described inverter-based OTA topologies.

	OTA 1	*OTA 2*	*OTA 3*
DC gain	Low	High	High
GBW	High	High	Moderate
Linearity [1]	Low	Moderate	Moderate
Current consumption	Low	High	Moderate
Circuit complexity	Two inverters	Ten inverters	Six inverters

[1] Considering 2/3 of the full-scale output.

4. A Standard-Cell-Based Digital–Delta (Δ) Modulator (ΔM) with Noise Shaping (NS)

A complete and differential electrical scheme of the proposed ADC topology, a digital-ΔM employing NS, is depicted in Figure 15, complementing the description in Section 2.5. It comprises a split-capacitor DAC with embedded S/H, a pseudodifferential inverter-based Nagaraj integrator with a fully passive SC CMFB circuit (shown in Figure 12), an OAI-based comparator (whose circuit is shown in Figure 10), an accumulator, and a phase generator. Thus, a fully synthesizable ADC is demonstrated, only recurring to passive and standard-cell-based circuitry.

As described in Figure 16, its operation is based on two different frequencies. The sampling and NS function at F_S, while the delta modulation is performed at a higher frequency.

After the DAC is reset, the sampling of the V_{in} and the noise-shaping voltage, V_{NS}, is simultaneously performed in the most significant bit (MSB) section of the DAC and on the dedicated capacitor, C_{NS}, respectively. After that, delta modulation starts: the comparator makes a decision that is transmitted to the accumulator to reconfigure the DAC for the next comparator decision. This action is performed during M averages, and the accumulator output is lastly ready. Before the new reset of the DAC, residue voltages $V_{RES,P}$ and $V_{RES,N}$ are integrated by the pseudodifferential inverter-based Nagaraj integrator scheme; consequently, $V_{NS,P}$ and $V_{NS,N}$ are updated. Then, a new sampling of the V_{in} and the V_{NS} is performed, and the process continues repeatedly.

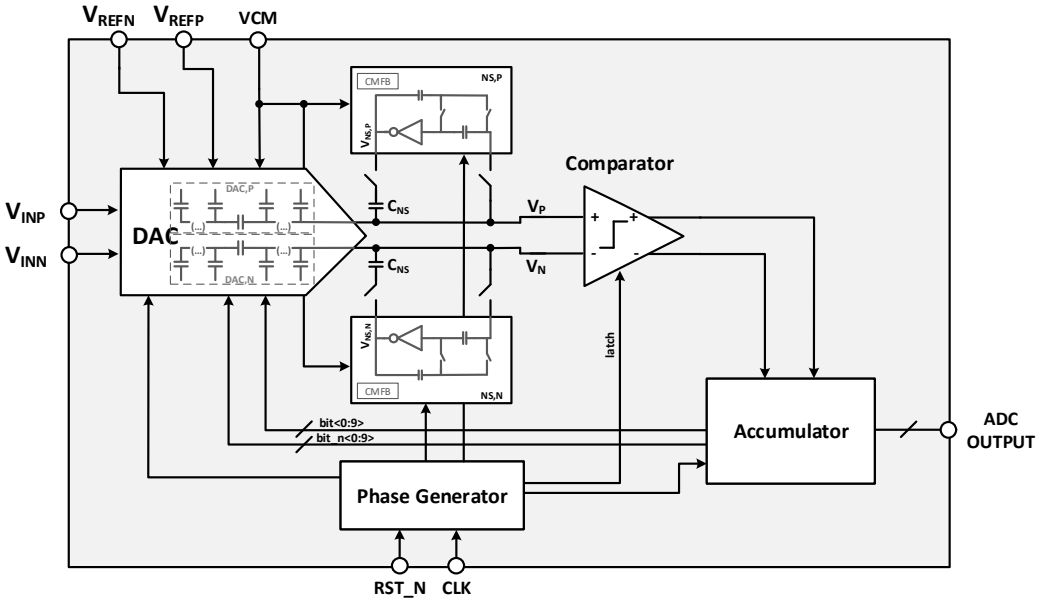

Figure 15. Scheme of the proposed standard-cell-based digital-ΔM with NS employing a split-capacitive DAC, an inverter-based OTA topology, to perform NS and an OAI-based comparator.

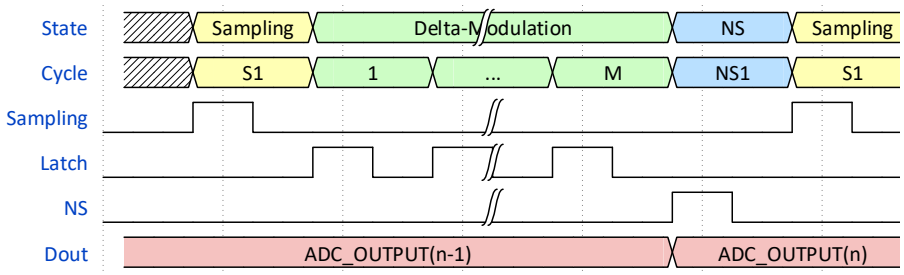

Figure 16. Illustrative timing of the proposed digital-ΔM ADC employing NS.

The simulated output spectrum of the proposed converter, fully implemented in a 28 nm CMOS technology, is shown in Figure 17. With an oversampling ratio (OSR) of 32 and a 10-bit DAC, a peak of 72.5 dB in the signal-to-noise and distortion ratio (SNDR) was achieved for a ≈113 kHz input signal and a 1 MHz BW. Table 3 summarizes the simulation results. The converter dissipated ≈112 µW, which could be translated into a Walden figure of merit, FoM_{Walden}, of 16.2 fJ/conv.-step.

These results are promising, allowing for a fully synthesizable ADC that is capable of achieving both high resolutions and good energy efficiency.

Table 3. Summary of simulated results of the proposed standard-cell-based digital-ΔM employing NS using a 28 nm CMOS technology.

Parameter	Unit	Digital-DM with NS
F_S	MHz	64
BW	MHz	1
OSR		32
SNDR	dB	72.50
ENOB	−bit	11.8
V_{DD}	V	0.9
Power dissipation	µW	112
FoM_{Walden}	fJ/conv.-step	16.2

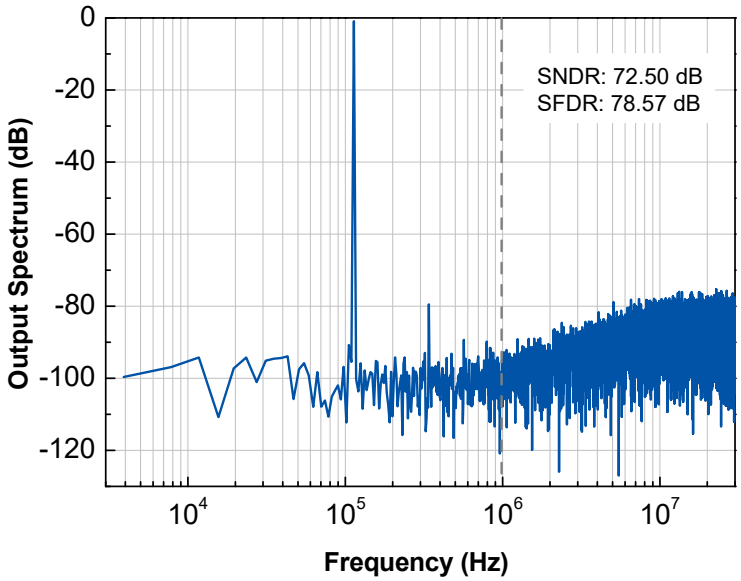

Figure 17. Simulated output spectrum of the schematic of the proposed standard-cell-based digital-ΔM employing NS. This result was achieved using 2^{14} points, $M = 8$, a BW of 1 MHz (OSR of 32), and a Fin of 113 kHz.

5. Conclusions

The most-suited high-resolution ADC topologies for IoT applications were described and compared in terms of complexity, overall performance, and energy efficiency. ΔM was described because it is the basis of some well-known topologies and has inspired others, such as SAR-ADC with NS or ΔΔΣM ADC. Taking into consideration the advantages of standard-cell-based synthesizable schemes, some schematics of comparators and amplifiers were reported, and their key performance parameters were compared. An innovative topology, a digital-ΔM ADC employing NS, was detailed employing passive and standard-cell-based circuitry. An SNDR of 72.5 dB was achieved for a 1 MHz BW (OSR of 32) with an estimated FoM_{Walden} of 16.2 fJ/conv.-step. Thus, a fully synthesizable ADC that is compatible with IoT applications was clearly demonstrated.

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