SiO_x patterned based substrates implemented in $Cu(In,Ga)Se_2$ ultrathin solar cells: optimum thickness

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***Abstract*— Interface recombination in sub-µm optoelectronics has a major detrimental impact on devices' performance, showing the need for tailored passivation strategies to reach a technological boost. In this work, SiO_x passivation based substrates were developed and integrated into ultrathin $Cu(In,Ga)Se_2$ (CIGS) solar cells. This study aims to understand the impact of a passivation strategy, which uses several SiO_x layer thicknesses (3, 8, and 25 nm) integrated into high performance substrates (HPS). The experimental study is complemented with 3D Lumerical finite-difference time-domain (FDTD) and 2D Silvaco ATLAS optical and electrical simulations, respectively, to perform a decoupling of optical and electronic gains, allowing for a deep discussion on the impact of the SiO_x layer thickness in the CIGS solar cell performance. This study shows that as the passivation layer thickness increases, a rise in parasitic losses is observed. Hence, a balance between beneficial passivation and optical effects with harmful architectural constraints defines a threshold thickness to attain the best solar cell performance. Analyzing their electrical parameters, the 8 nm novel SiO_x based substrate achieved a light to power conversion efficiency value of 13.2 %, a 1.3 % absolute improvement over the conventional Mo substrate (without SiO_x).**

***Index Terms*— $Cu(In,Ga)Se_2$ (CIGS), silicon oxide (SiO_x), rear passivation strategy, high performance substrate, ultrathin, optical simulations, electrical simulations.**

I. Introduction

The $Cu(In,Ga)Se_2$ (CIGS) semiconductor has already proved its potential as an absorber for ultrathin solar cells' application, fitting into a sustainable vision to meet the energy demand increase [1, 2, 3, 4]. Moreover, CIGS based solar cells have proven their success in the thin-film technology, outperforming their inorganic second generation counterparts [5]. Additionally, CIGS thin-film technology presents high reliability, a short energy pay-back time, and it is already commercialized in both rigid and flexible modules [6-10]. However, CIGS still does not have a prominent position in the photovoltaic (PV) market [11].

The CIGS thin-film technology benefits mostly from its active layer exquisite properties, assured by its large tolerance of compositional deviation from stoichiometry, which has been deeply explored [12-15], and subsequent implemented post deposition treatments mostly based on alkali doping [16-20]. While at the same time, the device architecture remained fundamentally the same from the '80s until recently [19, 21]. CIGS thin-film solar cells are developed with a substrate configuration, where the CIGS layer is deposited on molybdenum (Mo)-coated soda lime glass (SLG), followed by the n-type buffer and the transparent conductive oxide (TCO) layers sequential deposition [5, 19]. The move from thin (2 µm) to ultrathin (< 1 µm) film technology has followed the same path, with no significant changes in the device design [3]. This strategy contrasts with the one adopted by the market dominant

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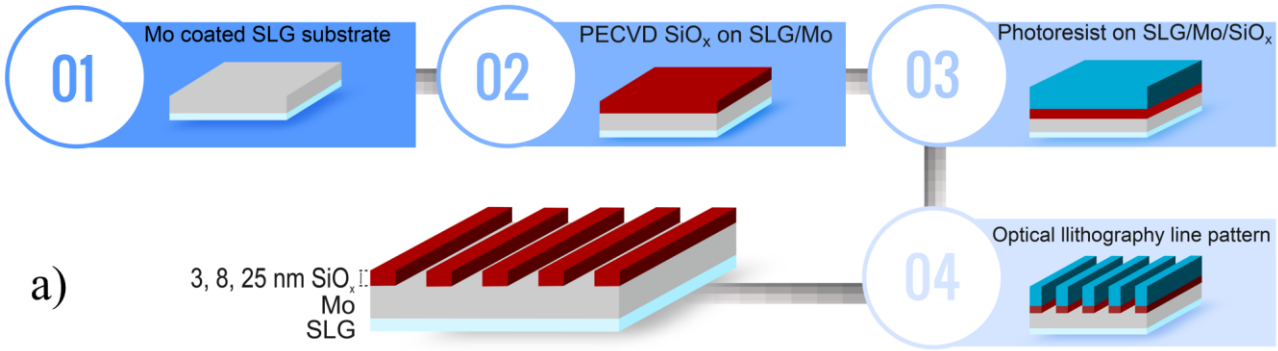
silicon (Si)-wafer technology, with continuous changes in its device design [22, 23]. That strategy has been a paramount factor for continuous performance improvement [24]. Hence, now that CIGS bulk properties reached a high quality, a shift in research focus to interface passivation is expected, to reduce interface recombination that prevents an efficient carrier collection. A similar path is well illustrated in the Si-wafer technology, by both scientific research community and industry, through its increasing efforts to study and launch a wide variety of single or combined oxide based passivating contacts [22, 24, 25]. The choice of the material has been considered and implemented based on its interface passivation quality, optical properties, thermal stability, deposition temperature, and industrial throughput [22]. Just recently, the integration of dielectric oxides as passivation layers in both CIGS interfaces has been studied, mostly in ultrathin devices, taking advantage of simulations [26-29] and experimental approaches [4, 30-34]. The inclusion of dielectric oxides, such as Al_2O_3, SiO_x, and HfO_x, through high performance passivation substrates in ultrathin CIGS devices, already outperformed their equivalent conventional devices, showing the need for rear interface passivation and the potential of these chosen materials [4, 31, 35, 36].

SiO_x high performance substrates (HPS) fabricated through photolithography, appear as strong candidates for a fully industrial upscalable interface passivation process [4]. From a fundamental point of view, SiO_x versatility has already been shown in a previous work [37], where it was demonstrated that by manipulating the deposition conditions, the polarity values of the fixed insulator charges (Q_f) can be changed. Nonetheless, the integration of HPS in CIGS solar cells can lead to a roll-over in current density vs. voltage (J-V) characteristic curves, i.e. a current sublinear voltage dependence or even a current density saturation, with additional high series resistance (R_S) values, indicating that there is a contact barrier being formed of still unknown origin. This anomaly has been associated with an unoptimized rear contact, due to either a high distance value between contacting areas and/or the thickness of the passivation layer, independently of the choice of the material. Alternatively, an inhomogeneous alkali doping distribution throughout the CIGS layer might also explain the rear barrier, as these elements may accumulate at the absorber interfaces [4, 31, 38-40]. Whilst, a line contact architecture with a width of ~1100 nm and a pitch of ~2800 nm were able to partially tackle the aforementioned issues [4], the study of the passivation layer thickness impact is yet to be done.

In this work, line contact optimized SiO_x based substrates were developed with different oxide thicknesses (3, 8, and 25 nm) and implemented in CIGS ultrathin solar cells. TEM analysis shows the formation of a $MoSe_2$ nanometric layer, at the contact areas in this type of HPS. The impact of SiO_x as a passivation layer, as well as the effect of its thickness value on the CIGS devices' performance, are addressed through a critical analysis of the electrical figures of merit compared with a SLG/Mo conventional device. Moreover, to further discuss the experimental results, Lumerical finite-difference time-domain (FDTD) and Silvaco ATLAS simulations were performed on equivalent structures. The novel SiO_x based HPS, allowed for light to power conversion efficiency (η) improvements over the conventional SLG/Mo substrate-based device. However, as the SiO_x layer thickness increases, parasitic losses arising from architectural constraints become more evident, suggesting the existence of a threshold thickness value that tackles these losses, whilst presenting positive passivation and optical effects. Therefore, the 8 nm SiO_x based substrates achieved the highest η value amongst the studied devices. This paper is an extended version, including 3D optical and 2D electrical simulations, of a manuscript submitted to the 2021 48th IEEE Photovoltaics Specialist Conference [41].

a)



b)

Device	Architecture	SiO_x thickness (nm)
Ref	SLG/Mo/CIGS/CdS/i-ZnO/ZnO:Al	X
3 – SiO_x	SLG/Mo/SiO_x/CIGS/CdS/i-ZnO/ZnO:Al	3
8 – SiO_x		8
25 – SiO_x		25

Fig.1- a) Detailed processing sequence followed in this study; and b) Final devices' architecture and passivation layers' thickness.

II. Experimental Details and Methods

The SiO_x based substrates processing flow is presented in Fig. 1 a). The HPS development started by depositing a SiO_x layer on top of 350 nm Mo coated SLG sample. To study the SiO_x thickness influence, four samples were used. One without SiO_x, as a conventional substrate (Ref) having Mo directly exposed, and three with different SiO_x thickness values, 3 nm (3-SiO_x), 8 nm (8-SiO_x), and 25 nm (25-SiO_x). The SiO_x layers were deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD) using an SPTS MPX CVD system, at 13.56 MHz and 300 ºC with SiH_4 and N_2O chemistry. Next, the samples were coated with 600 nm of photoresist (AZ1505) to be exposed using a direct write lithography 2000 laser photolithography system (Heidelberg), obtaining a nominal pattern of lines with 1100 nm of width and 2800 nm of pitch. The exposed photoresist was then developed (AZ 400K 1:4). After the photolithography process, the SiO_x in the contact areas was etched by reactive ion etching using a SPTS ICP system. To finalize, the remaining photoresist was removed with acetone. Note that the SLG/Mo conventional substrate, from the Ref device, follows as close as possible the HPS process flow, being subject to the same set of clean processes and storage conditions.

Ultrathin CIGS absorbers were co-evaporated at 550 ºC on all substrates in the same batch, previously evaporated with 15 nm of sodium fluoride (NaF) [42]. From an elemental point of view, [In] was kept constant (flat profile), a higher [Cu] was implemented at an intermediate region, with a continuous excess of [Se]. An estimated CIGS thickness of 750 nm and composition values of [Cu]/([Ga]+[In]) = 0.86 and [Ga]/([Ga]+[In]) = 0.41 were determined by X-ray fluorescence (XRF) performed in a Panalytical Epsilon 5. The devices were completed using the standard device layers, 50 nm of chemical bath-deposited CdS and 50/300 nm sputtered bi-layer ZnO (i-ZnO/ZnO:Al) [43]. Cells with an area of 0.1 cm^2 were separated by chemical etching of the CdS/i-ZnO/ZnO:Al stack after the deposition of a photolithography mask [44]. No post-deposition treatments or anti-reflection coating were applied in the studied devices. The final device architectures are presented in Fig. 1 b).

A scanning electron microscope (SEM) FEI Nova Nano SEM 650 system with an acceleration voltage of 5 keV and a Bruker Icon atomic force microscope (AFM) in tapping mode with a scan rate of 1 Hz, were both used to evaluate the SiO_x based substrates' architectures. Complete devices were characterized by *J-V* measurements under a simulated AM 1.5G with 1000 $W.m^{-2}$ illumination, calibrated by a standard Si reference cell. External quantum efficiency (EQE) measurements taken at 0 V without light bias were performed in a home-built system, using chopped monochromatic light scanned through the wavelength interval of 330–1090 nm, in 2 nm steps. Additionally, a solar cell with a 160 nm contact width patterned 25 nm SiO_x rear layer [4] was analyzed by Scanning Transmission Electron Microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDS), with a double corrected FEI Titan G3 Cubed Themis equipped with a Super-X EDX System, operating at 200 kV. EDS line scans of Mo, Si, and Se were performed, with the following spectrum lines: Mo L_α=2.294 keV, Si K_α=1.741 keV, and Se K_α= 11.223 keV. For the device lamella preparation on Mo grids, a focused ion beam (FEI Dual-Beam Helios 450S) system was used.

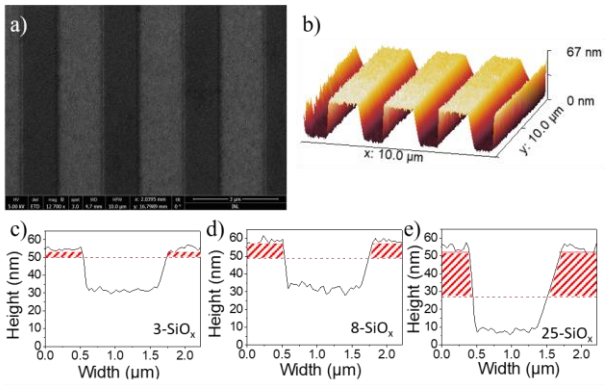
TABLE I

PARAMETER VALUES USED IN SILVACO ATLAS 2D ELECTRICAL SIMULATIONS.

Device	R_c ($\Omega.cm^2$)	R_b (%)	Defect density (cm^{-3})	Doping (cm^{-3})	SRV ($cm.s^{-1}$)	Q_f (cm^{-2})
Ref	1	20	$1x10^{14}$	$5x10^{16}$	$1x10^{7}$	-
Passivated	0.1	45	$1x10^{14}$	$5x10^{16}$	$1x10^{2}$	$-8x10^{12}$

Optical and electrical simulations were conducted to discuss the impact of the SiO_x layer thickness on the solar cell performance. Optical simulations were performed using the 3D FDTD method through the commercial software Lumerical to study: the electrical field intensity profiles and the absorption properties of the developed devices, considering a randomly polarized light source [28]. These simulations were conducted using the smallest mesh size considering simulation memory/time requirements, for critical interfaces 1 nm mesh size was considered. The simulation included both refractive index (n) and extinction coefficients (k) values ($n(\lambda)=n+ik$), accounting for the absorption of each layer, which were taken from the material properties obtained from the literature [45-48]. Electrical simulations were performed through Silvaco ATLAS 2D software, following the Lontchi baseline of reference [27]. The electrical simulation parameters are presented in Table I, which contains the values of the contact resistance (R_c), the rear reflectance (R_b), and the surface recombination velocity (SRV) for Ref and passivated devices. The biggest modelling difference between both Ref and passivated samples is the R_c and the SRV, parameters that consider the differences on the Mo/CIGS interface dimensions and properties [4, 27].

III. Results and Discussion



f) Device	Contact Width (nm)	Pitch (nm)	Passivation Area (%)
3 – SiOx	1189	2800	57.5
8 – SiOx	1202	2800	57.1
25 – SiOx	1075	2800	61.6

Fig. 2 – 25-SiO_x representative surface images of a) SEM (Mo is darker than the SiO_x), and b) AFM 3D. AFM profile of c) 3-SiO_x; d) 8-SiO_x; and e) 25-SiO_x, whereas the SiO_x thickness is presented by the dashed areas; f) Architecture dimensions extracted from the AFM analysis for the three developed HPS.

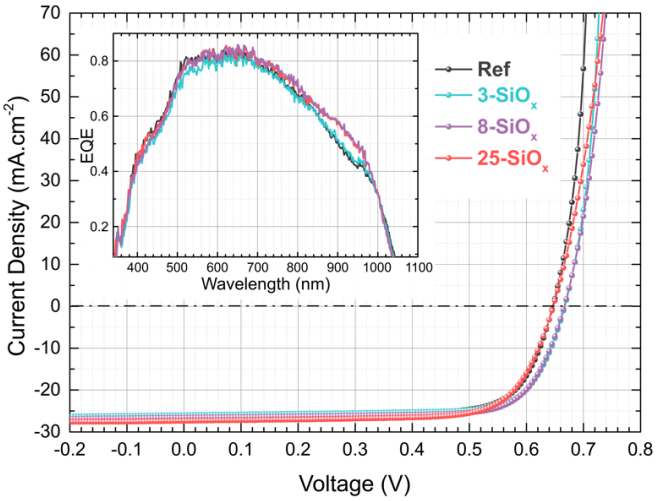


Fig. 3 - Representative illuminated *J–V* curves and EQE spectra (inset) of each type of device studied.

TABLE II
AVERAGES FROM 16 SOLAR CELLS, WITH STANDARD DEVIATION VALUES, OF *J–V AND EQE* (J_{SC}) FIGURES OF MERIT.

Device	V_{OC} (V)	J_{SC} (mA/cm²)	*FF* (%)	η (%)	R_S (Ω.cm²)	G_{SH} (mS/cm²)
Ref	0.644 ±0.008	25.96 ±0.54	72.8 ±5.29	11.90 ±1.19	1.88 ±0.23	1.79 ±0.44
3-SiO$_x$	**0.667** ±0.002	**25.04** ±0.33	**75.33** ±2.29	**12.58** ±0.52	**1.93** ±0.12	**1.62** ±0.65
8-SiO$_x$	**0.665** ±0.004	**26.54** ±0.53	**74.99** ±0.51	**13.23** ±0.28	**1.97** ±0.07	**1.17** ±0.45
25-SiO$_x$	**0.648** ±0.007	**27.03** ±0.46	**73.07** ±1.34	**12.79** ±0.25	**2.09** ±0.12	**1.69** ±0.53

The SiO_x based substrates architectures were evaluated through SEM and AFM topographic images. 25-SiO_x representative SEM and 3D AFM images are shown in Fig. 2 a) and b), respectively, to confirm the architecture of the developed HPS. From the AFM plots analysis presented in Fig. 2 c), d), and e) for samples 3-, 8-, and 25-SiO_x, respectively, where the thickness of the SiO_x layer is represented in red, the contact line width and the pitch values were evaluated to estimate the substrates' passivation area (see Table in Fig. 2 f)). A passivation area of 57 % was estimated for samples 3- and 8-SiO_x, whereas for sample 25-SiO_x an increase in the passivation area value (61 %) was observed, due to a decrease of the effective contact width value. The obtained passivation area values match the optimum range to obtain an enhancement in cells efficiency, as previously demonstrated [4].

All devices' representative *J-V* illuminated curves are presented in Fig. 3, being the figures of merit values extracted from those curves summarized in Table II. All *J-V* representative curves present similar and well diode-behaved characteristics. Hence, no evidence of unoptimized passivation contact is noted in the *J-V* characteristic curves, as observed in previous attempts to implement non-conventional substrates in CIGS solar cells, through a clear roll-over effect and loss of "squareness" in the *J-V* curves [4, 38, 49]. Therefore, to understand the impact of the SiO_x thickness on the device optoelectronic properties, the obtained figures of merit values were compared to those of Ref device. All devices with integrated SiO_x substrates present improvements in the open circuit voltage (V_{OC}), fill factor (*FF*), and shunt conductance (G_{SH}) values over the Ref ones, leading to higher η values - calculated considering the short circuit current density value (J_{SC}) from the EQE spectrum. Note that for all *J-V* parameters - excluding the G_{SH} - the standard deviation values obtained for the passivated devices are lower than the ones for the Ref device, this is particularly significant for the *FF* and η parameters, indicating that the passivation provides for more uniform solar cell devices. There are well behaved trends in the figures of merit values with the SiO_x thickness variation. As the SiO_x thickness increases, there is a smooth decrease of the V_{OC} and the *FF* values, while J_{SC} and R_S increase. The highest J_{SC} values obtained are for samples 8- and 25-SiO_x, resulting mostly from the improvement in the EQE NIR region.

The integration of the SiO_x layer in the solar cell had a strikingly positive impact on the recombination losses, mainly in the 3- and 8-SiO_x devices. For these, the V_{OC} values increased by more than 20 mV. Additionally, the introduction of the passivation layer allows for a shunting path reduction by breaking the pinholes path, leading to a decrease of the G_{SH} in the HPS devices, since only 40 % of the rear interface is a conductive layer [50]. The improvements in the V_{OC} and G_{SH} values, along with the increased charge collection in the NIR region for sample 8-SiO_x, led to a η value of 13.23 %, the highest amongst all the studied samples. However, the decrease in the *FF* and V_{OC} values with the increase of the passivation layer thickness still needs to be discussed. As the samples have nominally the same CIGS composition, their optical bandgap energy values are mostly the same (~1.2 eV), establishing an equivalent V_{OC} upper limit for all developed devices. Hence, this opens the discussion about the impact of the HPS thickness on parasitic and recombination losses. As expected, the V_{OC} follows the same trend of the *FF*, as well as the R_S values, supporting an increase in the parasitic losses due to the thicker SiO_x layer, since the pitch and contact width are approximately the same for every developed HPS. In fact, further factors may contribute for the well behaved trend between the V_{OC} and *FF* values, and might be the key discussion to establish an optimum thickness range for the SiO_x layer, to better benefit from passivation without losing from parasitic losses. Accounting for the line contact architecture introduced in the HPS, the SiO_x/CIGS interface area increases with the passivation layer thickness, due to the CIGS layer conformal growth over the trenches. The inclusion of HPS led to an increased SiO_x/CIGS interface area up to 3 % in the case of the 25-SiO_x sample in comparison to the Ref. This increased area in the rear contact corresponds to passivated regions, so it is not likely to increase significantly the SRV. However, as the HPS substrate topology is transferred to the upper solar cell layers, the very complex CIGS/CdS interface area is also extended [51]. Being the latter interface where the pn-heterojunction is established, any variations applied to the junction will unavoidably affect the solar cell performance. Alternatively, as the line contact is becoming deeper with thicker passivation layers, the step coverage of the line contacts is hampered [31]. The obtained solar cells' figures of merit trend might not be affected by one single cause, as all of the aforementioned problems could contribute to their variations. Notwithstanding, there is an improvement of the *FF* values from the Ref to the passivated devices and no roll-over is observed in the *J-V* curves, which is

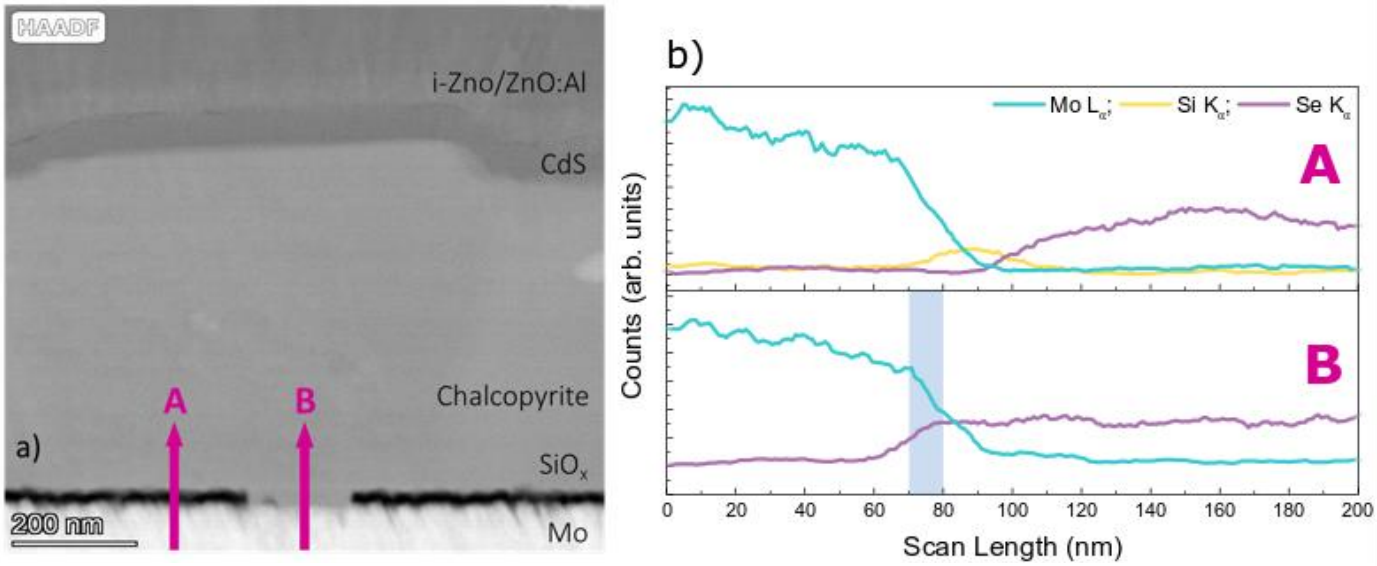


Fig. 4 – a) Passivated device a) HAADF STEM image of the final lamella; and b) EDS line profiles for Mo, Si, and Se elements in region A and B. The pink arrows corresponds to the EDS line scan regions. The blue shadow area highlights the potential $MoSe_2$ formation region.

a common indication of a rear contact barrier [52]. Furthermore, the J_{SC} improvement with increasing passivation layer thickness is compatible with an effective interface passivation, promoting a more efficient charge carrier collection [31, 51]. Nevertheless, optical gains as the SiO_x thickness value is increased, are also expected to have an impact on the J_{SC} value [4, 53]. Therefore, to extend the understanding on the impact of the SiO_x layer incorporation in the devices' figures of merit, complementary optical and electrical simulations should assist an efficient integration of non-conventional substrates in ultrathin solar cells devices. A deep knowledge of light propagation through the media and interface scattering, as well as carrier dynamics, is required.

The 3D optical and 2D electrical simulations were included in the study to better understand the devices' performance and to extend the experimental conclusions. The optical and electrical simulations, allow for an optical gain decoupling in the solar cell overall performance, which allows to discuss the predominance of optical or electronic effects in the J_{SC}.

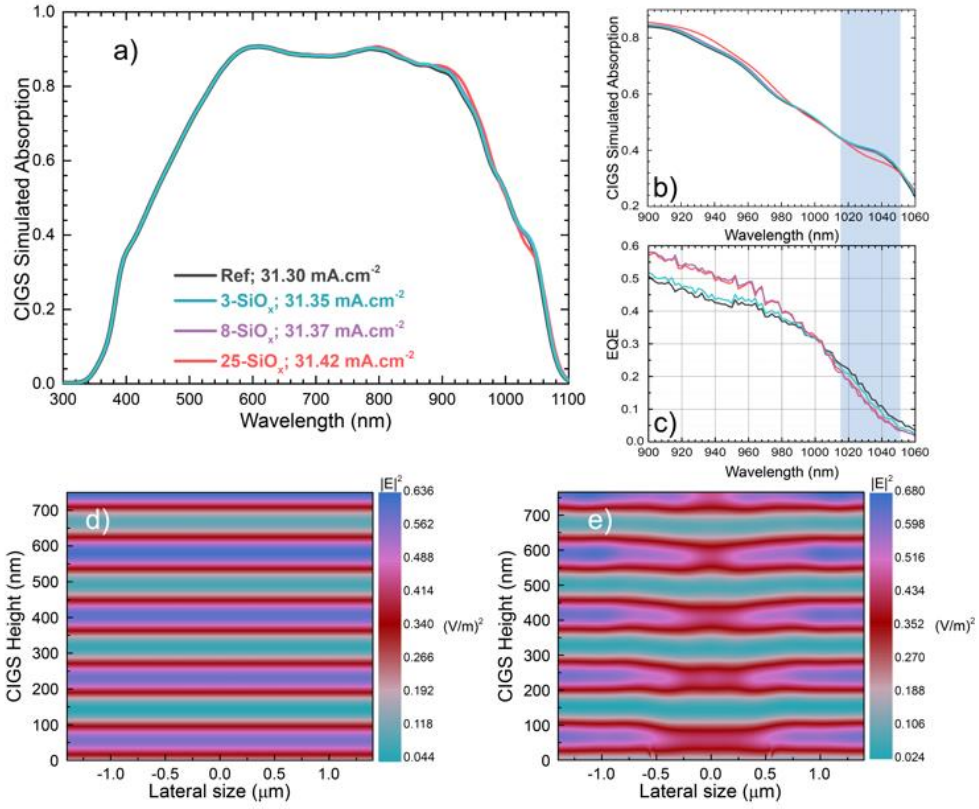


Fig. 5 – a) Simulated CIGS absorption of the developed devices; b) Simulated CIGS absorption and c) EQE spectrum for the 900-1060 nm range; Electric field intensity profile in the CIGS layer of the d) Ref and e) 25-SiO_x devices.

To establish the architecture of the simulated devices, the formation of the nanometric $MoSe_2$ interfacial layer at the Mo/CIGS region needs to be evaluated. A supplementary passivated cell with a contact width approximately seven times lower than the ones from the studied devices was developed, to test the limit conditions for the formation of the $MoSe_2$ layer. A high-angle annular dark field (HAADF) STEM representative image from the passivated device is presented in Fig. 4 a), showing the conformal growth of the layers, and the SiO_x patterned layer. The SiO_x layer is compact and without pinholes. Two different regions on the passivated solar cell were studied via EDS line profiles: region A - Mo/SiO_x/CIGS, and region B - Mo/CIGS as presented in Fig. 4 b). The EDS line profiles of region A show the presence of Si between the Mo and the Se signals. At region B it is clear that both the signals from Se and Mo are overlapped, strongly suggesting the existence of a nanometric $MoSe_2$ layer at the Mo/CIGS contact (blue shadow region in Fig. 4 b)), despite the opening width of circa 160 nm. These results confirm that when using the point contact approach, the Mo forms a $MoSe_2$ layer making the same electrical contact as conventional devices. Thus, a $MoSe_2$ layer was considered in the simulated solar cells, both in the Ref and passivated devices.

A. Optical Simulations

The simulated 750 nm CIGS absorption spectra that mimic each studied experimental device are shown in Fig. 5 a). All simulated spectra present higher absorption values, overall the wavelength values, than the experimental counterpart EQE, due to incomplete carrier collection existent in real solar cells not considered in these absorption spectra, as well as unaccounted electrical losses. Additionally, optical parameters, roughness, and thickness deviations from the nominal values, as well as bandgap and electrostatic fluctuating potentials that are well known to be present in CIGS, may potentially lead to differences between the simulated CIGS absorption values and experimentally obtained EQE ones [15, 28]. Despite these obvious and expected differences between simulated absorption vs. EQE, the simulated 750 nm CIGS absorption spectra is able to describe quite well the EQE's overall trend, allowing for an accurate discussion of the governing optical phenomena, and to compare the optical gains in the HPS employed devices [53]. The simulation accuracy is well demonstrated for ~1036 nm (Fig. 5 b)), where for the simulated absorption it is clearly observed a decrease in the absorption as the SiO_x thickness increases, which is a phenomenon observed in the EQE spectra (Fig. 5 c)). The absorption behavior can be described in terms of the field distribution inside the CIGS. The simulated cross-sectional electrical field intensity ($|E|^2$) distribution of the electromagnetic (EM) wave was calculated for 1036 nm and shown for Ref and 25-SiO_x devices in Fig. 5 d) and e), respectively. In the Ref device, the established electric field intensity distribution is translational invariant, exhibiting planar regions of constructive and destructive interference resulting from the interaction between the incident and rear reflected

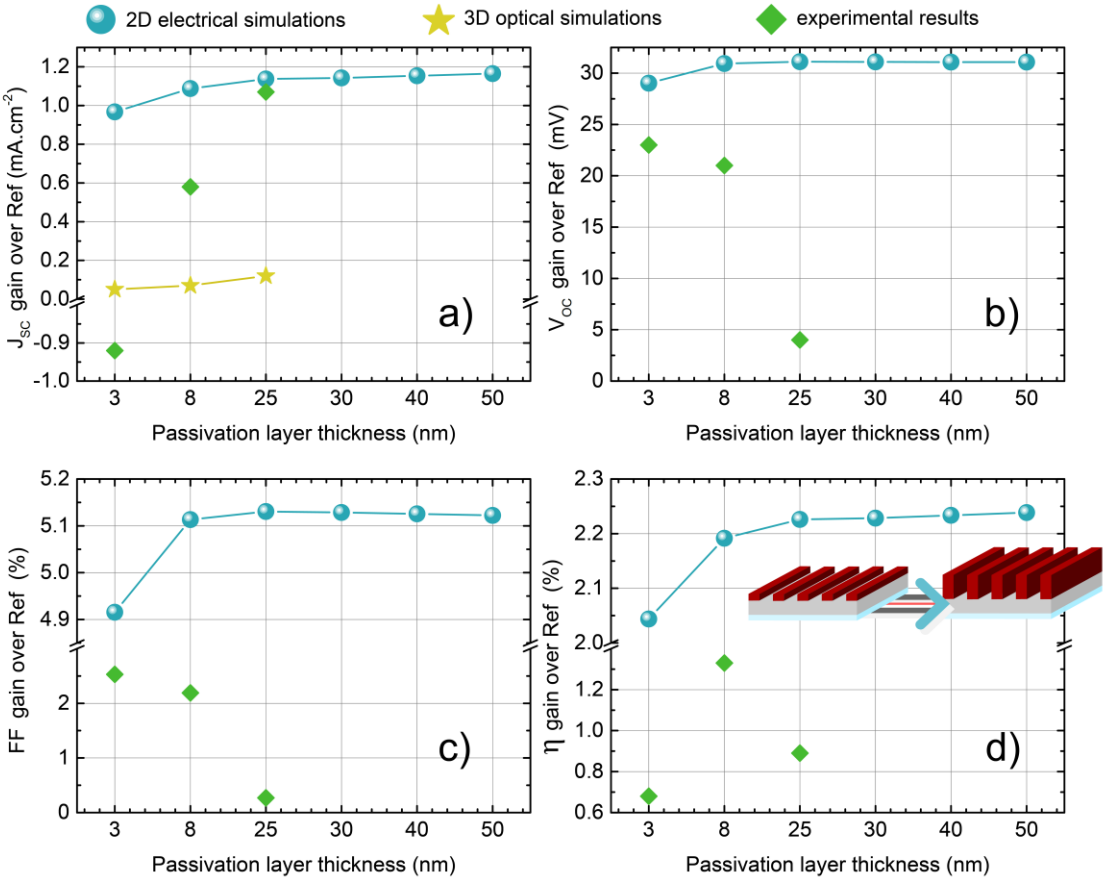


Fig. 6 - Figures of merit absolute gains of the HPS over the Ref devices: a) J_{SC} gains, b) V_{OC} gains, c) *FF* gains, and d) η gains. Green diamonds for experimental results, yellow stars for 3D optical simulations, and blue spheres for 2D electrical simulations. The connecting lines serve only as guiding lines.

light. On the other hand, the EM wave interaction with the line contact architecture promotes changes in the electric field distribution, since the periodic line grating will influence the interference pattern, disrupting the previously seen planar behavior. In this case, at 1036 nm the presence of a HPS promotes for a destructive interference that increases with increased SiO_2 thickness, as more light is reflected with the thicker layer [54]. An optical optimization of the HPS architecture is required in order to shift the destructive interference away from the solar spectrum region of interest (> 1100 nm). Despite the J_{SC} values obtained from the simulated absorption, those follow the experimental trend and increase with the SiO_x thickness value. Nevertheless, the J_{SC} gains over the Ref device obtained through the 3D optical simulations are much lower for the 8- and 25-SiO_x devices, than the ones experimentally obtained, as shown in Fig. 6 a). These results indicate that the J_{SC} experimental gains, mostly for the two aforementioned samples, overcome significantly the optical gains and are compatible with an effective passivation and improvement in the charge collection. Thus, 2D electrical simulations were ran to discuss the performance of the developed devices.

B. Electrical Simulations

A fixed passivation area of 60 % was used in 2D electrical simulations for different passivation layer thicknesses up to 50 nm, giving an insight on the thickness impact on the solar cell performances. The simulations assume the same interface properties of the passivation layer and vary only its thickness. Surprisingly, there is a variation of several figures of merit with the passivation layer thickness as demonstrated in Fig. 6. A gain is observed in all figures of merit when the passivation layer goes from 3 to 25 nm of thickness, whereas for thickness values over the latter value the gains tend to saturate mostly already at 8 nm, indicating that below this thickness the passivation effect is low. The electrical simulations show that the η absolute gain may go over 2 %, Fig. 6 d). However, the experimental figures of merit do not follow the electrical model, especially for the *FF* and V_{OC} values that decrease with the SiO_x thickness as shown in Fig. 6 b) and c), respectively. Once again pointing out that the ideal character of the model could not completely explain the behavior of the real device. Experimental results have revealed an increase of the R_S values with the SiO_x thickness, due to parasitic losses that may contribute to the decrease of the experimental *FF*, as compared to simulations where R_S values are kept constant. The difference in the trends for the experimental and simulated V_{OC} might be supported by the above-mentioned possible variation of the CIGS/CdS junction properties, resulting from the change of the HPS topology on the one hand, and a poor absorber step coverage over the SiO_x line contacts. Notwithstanding, the model confirms the trends in the J_{SC} values, supporting the positive effect of the passivation, i.e. increasing the collection of photogenerated charges by reducing the recombination losses.

The results obtained from the *J-V* analysis, as well as optical and electrical simulations, demonstrate that a compromise between beneficial passivation, optical effects, and architectural constraints should be considered when the HPS is fabricated, to attain an optimized solar cell performance. In this work, the 8 nm appears in an optimum thickness range of values for SiO_x to act as an effective passivation layer, promoting an enhanced charge carrier collection, for an overall better performance amongst all the studied devices.

IV. Conclusion

In this work, SiO_x patterned layers were developed on SLG/Mo samples, and incorporated as HPS in CIGS ultrathin devices. The integration of 3, 8, and 25 nm SiO_x layers in ultrathin CIGS devices were addressed and compared with a conventional CIGS solar cell without the HPS. Experimental results showed that despite the thickness of the SiO_x layer, the devices with a HPS outperformed the conventional solar cell. TEM results point out the existence of a $MoSe_2$ layer at the contact areas of the line patterned HPS, compatible with the electrical contact present in CIGS conventional devices. Optical and electrical simulations were conducted in order to support the experimental understanding of the studied samples. The use of these two simulation approaches allowed to discuss the decoupling between optical and electronic gains arising from the HPS integration. The optical simulations showed that only a marginal J_{SC} increase is achieved through the HPS optical benefits. Hence, the improved J_{SC} value in the experimental HPS resulted mainly from an effective passivation rather than optical reflection gains. Electrical simulations were performed for passivation thickness values up to 50 nm, and corroborate the latter hypothesis, as an initial improvement of all the solar cells' figures of merit is attained to thicknesses up to 25 nm; nonetheless, with a strong reduction of the improvement already around 8 nm. These results demonstrate an upper limit for the SiO_x layer thickness value, as for thicker layers the η value saturates. However, architectural constraints not considered in the electrical simulations, such as the transfer of the line pattern to the upper solar cell layers and a poor step coverage filling, lead to parasitic losses. Such losses, make the HPS with the 8 nm SiO_x layer capable of achieving the best solar cell performance, allowing a η of 13.2 %, achieving an improvement of 1.3 % (abs) over the conventional device. The presented 8 nm SiO_x HPS, takes advantage from the passivation effect through an increase of 20 mV in the V_{OC} over the Mo based substrate, without significant parasitic losses.

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