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$Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric devices for digital and analog non-volatile memories

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Doctoral dissertation

Athens 2022

Acknowledgments

First of all I would like to thank my supervisor and research director at the Epitaxy and Surface Science Lab (ESSL) Dr. Athanasios Dimoulas for our collaboration and the opportunity to work on this subject. I also thank Ass. Prof. Dr. Constantinos Simserides and Ass. Prof. Dr. Vlassios Likodimos for their help as members of my advisory committee.

My sincere thanks go to my project mates Dr. Polychronis Tsipas, Dr. Stefanos Chaitoglou and Nikitas Siannas for the excellent and enjoyable collaboration. I also own many thanks to the rest of my collaborators at ESSL during these years for making the everyday work easier and more pleasant; Sotirios Fragkos, Evgenia Symeonidou, Dr. Nikolaos Kelaidis, Dr. Panagiotis Pappas, Elli Georgopoulou-Kotsaki, Akylas Lintzeris, Dr. Alexandros El Sachat, Dr. Dimitra Tsoutsou, Dr. Evangelia Xenogiannopoulou and Dr. Ikaros Hauge†.

Finally, I cordially thank my friends Afroditi, Nikolas, Maria, Sofia, Gianna and Dimitris for their endless support, help and valuable discussions and my family Nikos, Evangelia, Konstantina, Sofia, Giorgos and Christina for their support and for always being there.

Abstract

The dielectric material HfO_2 has been extensively used in recent years and has entered industrial production since 2007 as a gate dielectric of CMOS technology transistors. HfO_2 has recently been found to be ferroelectric when it is crystallized at the non-centrosymmetric orthorhombic phase. Alloying it with Zr or doping it with Si, Ge, Al, Gd and other elements stabilizes the ferroelectric phase or turns it into antiferroelectric (tetragonal phase). This opens new opportunities for many applications, including integrated ferroelectric non-volatile memories, since HfO_2 and ZrO_2 are compatible with silicon technology.

In the present dissertation, the optimal fabrication conditions of $Hf_{1-x}Zr_xO_2$ (HZO) to achieve a ferroelectric material were investigated. TiN/HZO/Ge metal-ferroelectric-semiconductor (MFS) capacitor structures were prepared by atomic oxygen/nitrogen plasma-assisted molecular beam deposition in an ultrahigh vacuum chamber at the Laboratory of Molecular Epitaxy and Surface Science of NCSR-Demokritos. Physical characterization of the capacitors confirms the predominance of the orthorhombic/ferroelectric phase of HZO and the clean HZO/Ge interfaces, leading to good ferroelectric characteristics.

Subsequently, the depletion region in the surface of the Ge semiconductor, formed at lower temperatures, and its effect on the ferroelectric characteristics of HZO were studied. From measurements of polarization, displacement current and capacitor capacitance on p, n and n+ type germanium substrates the depolarization field as a function of temperature was calculated.

Two main issues in the reliability of ferroelectric devices are “wake-up”, that is the broadening/improvement of the P-V loop by applying a series of electrical cycles, and polarization imprint, which is the partial stabilization of one of the two possible ferroelectric states over time. From time and temperature depended electrical measurements of the polarization, conclusions about the mechanism of the phenomenon were drawn.

The above study led to the fabrication of ferroelectric field-effect transistors (FeFETs) with TiN/HZO gate structure on a p-type Ge channel. By replacing the gate dielectric of conventional

transistors with a ferroelectric material, the expected shift of the I_{ds}-V_g characteristic curve with the polarization switching was observed, showing a memory window of MW = 0.55 V. Due to the possibility of partial polarization switching in HZO, FeFETs in addition to the ON and OFF states, also present intermediate states. This phenomenon makes them suitable for application in analog non-volatile memories, and due to the low oxide thickness (15 nm), they operate at low voltage/power.

Finally, some first results on capacitors with 5 nm HZO on Nb:$SrTiO_3$ (NSTO) semiconductor substrates and metallic TiN or W as top electrode are presented, which show synaptic performance. The current of the capacitors is modulated by the polarization state in the ferroelectric, making it work as an analog memory. From current measurements at various temperatures and their analysis, the conductivity is attributed to thermionic Schottky emission and the change in current to the change in resistance in the surface of the semiconductor, due to modulation of the potential barrier. The devices show synaptic plasticity and are suitable for applications in neuromorphic networks.

Περίληψη

Το διηλεκτρικό υλικό HfO_2 έχει χρησιμοποιηθεί εκτενώς τα τελευταία χρόνια και έχει μπει σε βιομηχανική παραγωγή από το 2007 σαν διηλεκτρικό πύλης των τρανζίστορ τεχνολογίας CMOS. Πρόσφατα βρέθηκε ότι το HfO_2 είναι σιδηροηλεκτρικό υλικό, όταν κρυσταλλωθεί στη μη κεντροσυμμετρική ορθορομβική δομή. Η κραματοποίησή του με Zr ή ο εμπλουτισμός του με Si, Ge, Al, Gd και άλλες προσμίξεις σταθεροποιεί τη σιδηροηλεκτρική φάση ή τη μετατρέπει σε αντισιδηροηλεκτρική (τετραγωνική δομή). Αυτό ανοίγει νέους δρόμους για πολλές εφαρμογές, συμπεριλαμβανομένων των ενσωματωμένων σιδηροηλεκτρικών μη πτητικών μνημών, αφού το HfO_2 και το ZrO_2 είναι συμβατά με την τεχνολογία πυριτίου.

Στο πλαίσιο της παρούσας διατριβής διερευνήθηκαν οι βέλτιστες συνθήκες σύνθεσης $Hf_{1-x}Zr_xO_2$ (HZO) για την επίτευξη σιδηροηλεκτρικού υλικού. Δομές πυκνωτών μέταλλο-σιδηροηλεκτρικό-ημιαγωγός (MFS) TiN/HZO/Ge παρασκευάστηκαν με τη μέθοδο της εναπόθεσης με μοριακές δέσμες υποβοηθούμενης από πλάσμα ατομικού οξυγόνου/αζώτου σε θάλαμο υπερυψηλού κενού στο εργαστήριο Μοριακής Επιταξίας και Επιστήμης των Επιφανειών του ΕΚΕΦΕ-Δημόκριτος. Ο δομικός χαρακτηρισμός των πυκνωτών επιβεβαιώνει την επικράτηση της ορθορομβικής/σιδηροηλεκτρικής φάσης του HZO και τις καθαρές HZO/Ge διεπιφάνειες, οδηγώντας σε καλά σιδηροηλεκτρικά χαρακτηριστικά.

Στη συνέχεια, μελετήθηκε η περιοχή απογύμνωσης φορέων στην επιφάνεια του ημιαγωγού Ge, η οποία σχηματίζεται σε χαμηλότερες θερμοκρασίες, και η επίδρασή της στα σιδηροηλεκτρικά χαρακτηριστικά του HZO. Από μετρήσεις της πόλωσης, του ρεύματος μετατόπισης και της χωρητικότητας πυκνωτών σε υποστρώματα γερμανίου p, n και n^+ τύπου υπολογίστηκε το πεδίο αποπόλωσης συναρτήσει της θερμοκρασίας.

Δύο βασικά φαινόμενα που παίζουν ρόλο στην αξιοπιστία των σιδηροηλεκτρικών διατάξεων είναι η αφύπνιση («wake-up»), δηλαδή η διεύρυνση/βελτίωση του βρόχου P-V εφαρμόζοντας μια σειρά ηλεκτρικών κύκλων, και η αποτύπωση (imprint) της πόλωσης, η οποία είναι η μερική σταθεροποίηση της μίας εκ των δύο πιθανών σιδηροηλεκτρικών καταστάσεων με την πάροδο του χρόνου. Από ηλεκτρικές μετρήσεις της πόλωσης με χρονική και θερμοκρασιακή εξάρτηση, προέκυψαν συμπεράσματα για το μηχανισμό του φαινομένου.

Η παραπάνω μελέτη οδήγησε στην παρασκευή σιδηροηλεκτρικών τρανζίστορ επίδρασης πεδίου (FeFETs) με δομή πύλης TiN/HZO σε p-τύπου κανάλι Ge. Αντικαθιστώντας το διηλεκτρικό πύλης των συμβατικών τρανζίστορ με σιδηροηλεκτρικό, παρατηρήθηκε η αναμενόμενη μετατόπιση της χαρακτηριστικής καμπύλης I_{ds}-V_g με την αλλαγή της πόλωσης, εμφανίζοντας ένα παράθυρο μνήμης MW = 0.55 V. Χάρη στη δυνατότητα μερικής στρέψης της πόλωσης στο HZO, τα FeFETs εκτός από τις δύο ακραίες καταστάσεις ON και OFF, παρουσιάζουν και ενδιάμεσες καταστάσεις. Αυτό το φαινόμενο τα καθιστά κατάλληλα για εφαρμογή σε αναλογικές μη-πτητικές μνήμες, και χάρη στο μικρό πάχος οξειδίου (15 nm), λειτουργούν με χαμηλή τάση/ισχύ.

Τέλος, παρουσιάζονται κάποια αρχικά αποτελέσματα σε πυκνωτές με 5 nm HZO σε υποστρώματα ημιαγωγού Nb:$SrTiO_3$ (NSTO) και μεταλλικό TiN ή W ως πάνω ηλεκτρόδιο, τα οποία δείχνουν λειτουργία σύναψης. Η ένταση ρεύματος των πυκνωτών μεταβάλλεται αναλόγως με την κατάσταση πόλωσης του σιδηροηλεκτρικού, κάνοντάς το να λειτουργεί σαν αναλογική μνήμη. Από μετρήσεις ρεύματος σε διάφορες θερμοκρασίες και την ανάλυσή τους, η αγωγιμότητα αποδίδεται σε θερμιονική εκπομπή Schottky και η μεταβολή του ρεύματος στη μεταβολή της αντίστασης στην επιφάνεια του ημιαγωγού, λόγω μεταβολής του φράγματος δυναμικού. Οι διατάξεις παρουσιάζουν πλαστικότητα σύναψης και είναι κατάλληλες για εφαρμογές σε νευρομορφικά δίκτυα.

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Chapter 1

Introduction to ferroelectric hafnia

1.1 History

Ferroelectricity (FE) is a material property that has been studied a lot aiming to device applications like energy storage and nonvolatile memories, taking advantage of the two possible polarization states [1-5]. Despite all the interesting concepts, with the conventional FE materials, like perovskite-structured oxides, the integration into complementary metal–oxide–semiconductor process (CMOS) circuits was challenging [6, 7]. The discovery of FE in doped HfO_2 (hafnia), first reported by Qimonda and Namlab in 2011 [8], boosted the realization of these devices. HfO_2 is considered a key gate dielectric material for nanoelectronics since it enables the scaling of advanced CMOS devices and circuits, enhancing their performance. Ferroelectricity in Hf and Zr-based oxides opens new opportunities for Si-compatible embedded non-volatile ferroelectric memories [3, 9, 10] and creates the prospect for low power/high performance steep slope switches based on the concept of negative capacitance (NC) [11-13] in transistors with ferroelectric gates.

1.2 Origin of ferroelectricity in doped HfO_2

Despite the rapid progress of HfO_2-based ferroelectric devices over the last decade, the origin of FE in fluorite-structure oxides still remains an open issue. HfO_2 was already a widely studied material [14], but a polar phase had never been reported. So the first evidences of FE behavior, and especially in only a few nanometers thick layers, were unexpected.

It is now accepted that in hafnia/zirconia films, the ferroelectricity originates from the formation of the orthorhombic phase (FE o-phase) with a space group of $Pca2_1$ or the rhombohedral phase with the space group R3 [8, 15, 16].

Inside a typical ferroelectric material, a dipole tends to be oriented according to its nearest ones forming domain walls. In these regions in the bulk and the surface of the material depolarization electric fields are arising reducing the spontaneous polarization. As a result, the ferroelectricity becomes less stable and is totally suppressed in layer thicknesses at the nanometer scale [17].

Lee et al. [18] supported with theoretical calculations that the formation of FE in hafnia has a different mechanism. Domain walls have almost zero width and negligible energy cost, associated with a nearly flat phonon band. As a result, each FE domain can be switched independently from the neighboring domains (Figure 1). This separation makes it feasible to switch just one domain, enabling the partial switching. Also, it allows the scalability of FE hafnia layer even down to the angstrom regime. Indeed, this is verified by the recent report of enhanced ferroelectricity in ultra-thin 1-nm-thick films [19]. These characteristics open new opportunities for future technologies and brain-inspired computing applications.

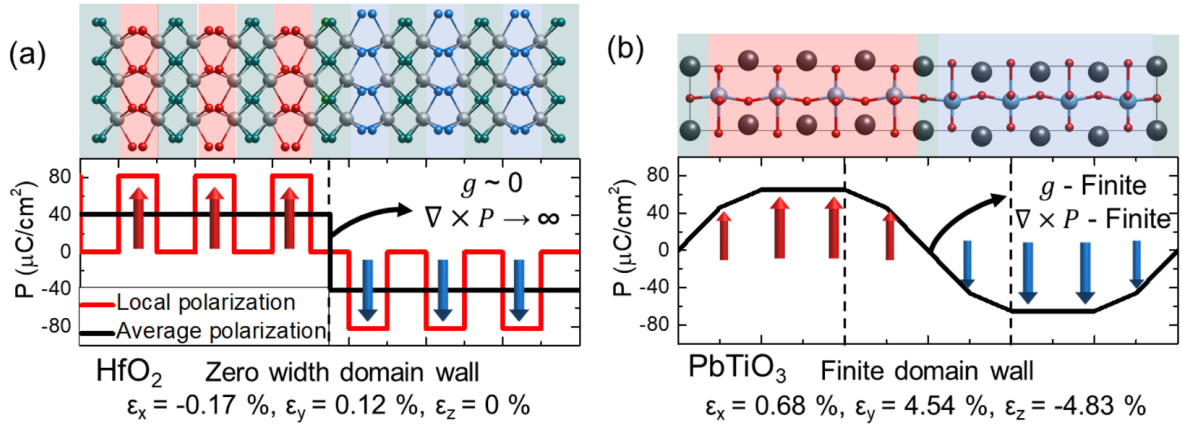

Figure 1: *Atomic structure of the domain wall and variation in local polarization perpendicular to the domain walls in (a) HfO_2 and (b) $PbTiO_3$, a typical ferroelectric material. In HfO_2 the energy cost g and the strain ε are almost zero, in contrast to what it was known for the ferroelectrics so far. Adapted from [18].*

1.3 Conditions to achieve ferroelectricity in hafnia

Ferroelectricity in hafnia is manifested in the orthorhombic non-centrosymmetric phase $Pca2_1$, which is achievable by proper doping and annealing conditions. Annealing at high temperatures leads to the tetragonal phase. During the cooling down after annealing, the monoclinic phase, which is energetically favorable, is normally stabilized. By using a capping layer, typically metal

TiN, and fast cooling rate, the expansion of m-phase is mechanically suppressed, and the orthorhombic/ferroelectric, which is an intermediate phase, is stabilized (Figure 2).

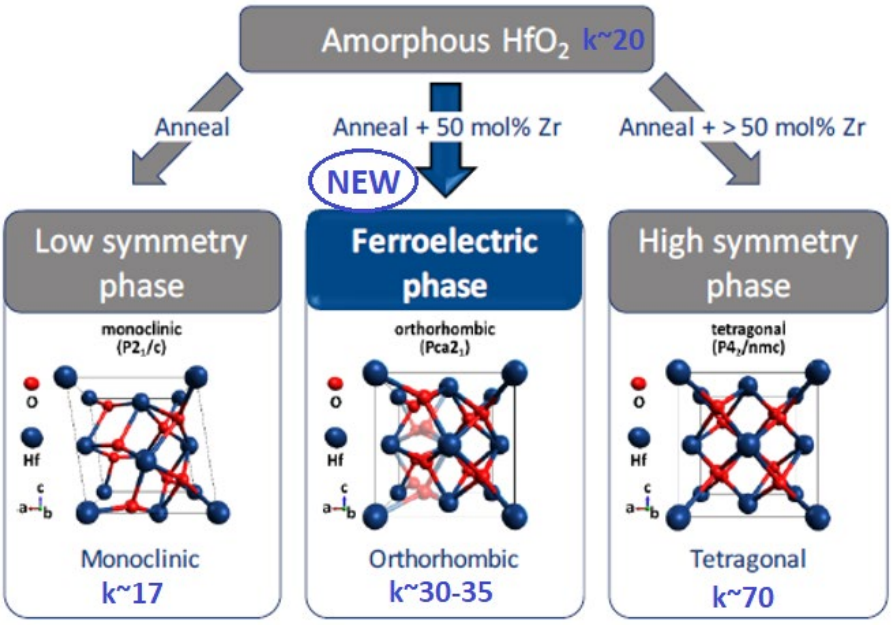

Figure 2: *Orthorhombic $Pca2_1$ (ferroelectric) phase is stabilized by using the proper doping and annealing conditions under stress. Source: FMC, adapted.*

1.4 Remaining Reliability Issues

There are some remaining critical issues in fluorite-structure ferroelectrics that affect the reliability of the devices and are associated with the presence of non-ferroelectric (dead) layers at the ferroelectric/semiconductor interface or oxygen vacancies both in the interfaces and the bulk of the ferroelectric.

A main reliability feature is the electrical endurance of the device until it breaks down. Leakage current is known to be the main reason for breakdown [4]. It is anticipated that the higher leakage induces more easily conducting paths after some cycling so the ferroelectric breaks faster (in less cycles), effectively becoming a resistor. There is a trend reported in the literature [4], according to which endurance increases with decreasing P_r.

Another big concern is imprint [4], that is a shift over time of the hysteresis loop along the voltage axis (Fig. 3a) and is already present at room temperature resulting in retention loss. The ferroelectric tend to be stabilized in the stored polarization state, making it hard to switch to the opposite state [20].

An equally important problem is the constricted (pinched) hysteresis loops [4] typically obtained in pristine devices. Such devices need extensive cycling to open the loop ("wake-up") which jeopardizes the performance of NVM (Fig. 3b). The origin and the possible correlation between imprint and wake-up effects are not known yet in detail [21-23]. These reliability issues are discussed in detail in Chapter 4.

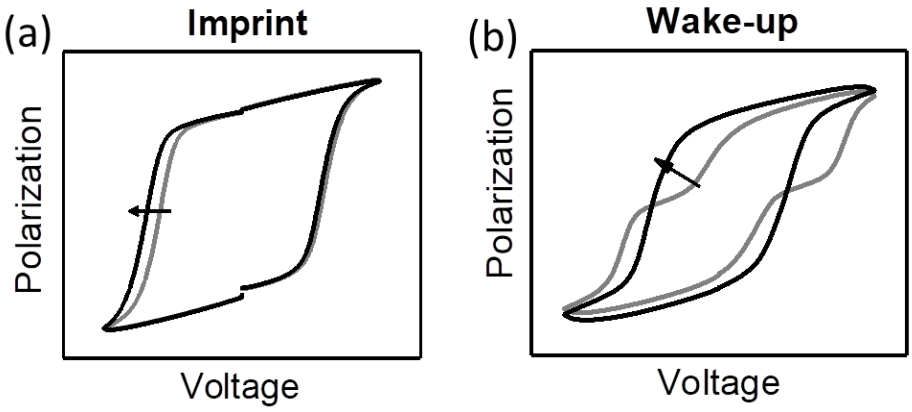

Figure 3: *(a) Shift of P-V loop over x-axis affected by imprint after storing the ferroelectric in P_{down} state. (b) Opening of a pristine pinched loop by electrical cycling (wake-up).*

1.5 Types of ferroelectric devices for non-volatile memories

The main types of ferroelectric devices used for non-volatile memories are presented in Figure 4. Ferroelectric hafnia boosted the realization of these devices due to its compatibility with CMOS technology, the low power operation and its stable ferroelectricity at reduced thickness ~ 10 nm in-line with technology scaling trends.

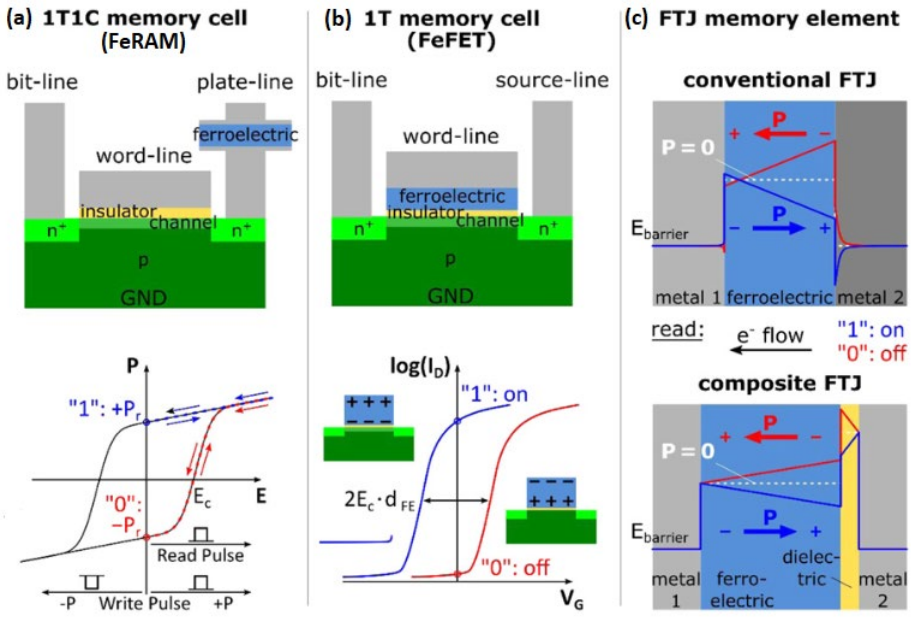

Figure 4: *Types of ferroelectric devices for non-volatile memories. Sketch and principle of memory operation of (a) a 1T1C memory cell (FeRAM) and (b) 1T memory cell (FeFET). (c) Scheme of the barrier modulation in a single or double layer FTJ. Adapted from [24].*

One type of ferroelectric memory device is the Ferroelectric Random Access Memory (FeRAM), which is a one transistor and one capacitor structure. The capacitive layer of a typical Dynamic Random Access Memory (DRAM) is replaced by a ferroelectric material to achieve non-volatility. FeRAM can hold data even after it is powered off but requires a memory restore after each read [4].

Ferroelectric Field-Effect Transistor (FeFET) is a typical FET, where the dielectric gate oxide is replaced by a ferroelectric material. In this structure, depending on the polarization state of the FE layer, the inversion in the channel becomes easier (ON-state) or more difficult (OFF-state). In this way the threshold voltage is modulated and a memory window between the transfer curves I_d-V_g of the two states is formed. This modulation is maintained when the external electric field is turned off, making the memory effect non-volatile. In contrast to FeRAM, in a FeFET the stored information is read non-destructively [4]. The research on HZO FeFETs [25] is currently accelerating [26-29] essentially driven by foreseen applications in the area of

neuromorphic devices [30-32] and circuits either as emulators of biological neurons [32] or as electronic synapses [30, 31] functioning as accelerators of deep neural network training [31].

Ferroelectric Tunnel Junction (FTJ) is based on the tunneling conduction of electrical carriers through an ultra-thin ferroelectric layer sandwiched between two electrodes with different screening lengths [4]. Depending on the polarization state (up or down) in the FE layer, the polarization charges in the interface with the semiconductor modulate the potential barrier, and as a result the resistance. The polarization state of the device is detected by measuring the current flow upon application of an electrical field that is lower than the coercive field of the ferroelectric, avoiding the polarization switching. In that way the FTJ can be used to store information and, like in FeFETs, it doesn't need to be refreshed after reading. FTJs also show great potential in non-volatile memories and neural network applications.

In this dissertation, we focused on the study of FeFET (Chapter 5) and FTJ (Chapter 6) devices.

1.6 Motivation for using Ge substrate

Neuromorphic devices have been demonstrated recently using Ge nanowire FeFET [33] with HZO ferroelectric, renewing interest in technologically important Ge channels/substrates with potential advantages for FeFET fabrication. Unlike HfO_2/Si where an unintentional (Hf)SiO_x interfacial layer is spontaneously formed, Hf(Zr)O_2/Ge interfaces are typically clean [34, 35] due to the fact that (Hf)GeO_x oxides are unstable, easily dissociating at moderate annealing temperatures thus leaving oxide-free crystalline interfaces. This could be beneficial for the improvement of endurance [9] and memory window [28] in FeFETs. In addition, Ge, as a low gap semiconductor has a large number of intrinsic free carriers which could screen the polarization charges thus stabilizing the FE domains in MFS structures. Unlike Si, work on Ge substrates [36-40] is rather limited to Ge FinFETs with HZO FE gates for NC FET [37], Y-doped HfO_2 [38, 39] and HZO on Ge for ferroelectric tunnel junctions (FTJ) [40]. Notably, in the latter work, 8 nm HZO MFS fabricated on Ge show the largest polarization of P_r ~ 18 $\mu C/cm^2$, compared to all others fabricated on TiN, Si, or SiGe substrates. It is anticipated that the low thermal expansion coefficient of Ge [40], and consequently the large thermal expansion

coefficient mismatch with HZO produces an appreciable residual thermal tensile strain during cooling down from crystallization temperature to room temperature (RT). The latter tensile strain could stabilize the orthorhombic FE phase against the non-FE tetragonal or monoclinic phases as previously suggested [41, 42] resulting in higher remanent polarization. For example, HZO sandwiched between thick TiN gate electrodes acting as tensile stressors [42] shows P_r ~ 26 $\mu C/cm^2$ which is the largest value obtained in MFM capacitors with atomic layer deposited (ALD) HZO [42-44]. There is increasing evidence that epitaxial strain influences ferroelectricity. For example, it has been recently reported [16] that HZO grown on crystalline LSMO templates adopts a rhombohedral phase as a result of epitaxial compressive strain which is ferroelectric yielding P_r~ 18 $\mu C/cm^2$ for a 9 nm thick HZO and a much higher P_r of 34 $\mu C/cm^2$ for a 5 nm-thick HZO. In addition, using microwave annealing of HZO/GeO_x/Ge, the P_r is significantly enhanced suppressing also gate leakage in FETs and Ge interdiffusion [37]. Achieving large values of P_r in HZO-based devices is important since it gives more flexibility for the design and sensing of memory cells.

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Chapter 2

Fabrication and characterization of TiN/HZO/Ge MFS capacitors

2.1 Experimental methods

Molecular Beam Epitaxy (MBE)

Molecular Beam Epitaxy (MBE) is a technique for growing thin epitaxial heterostructures. Although this method was developed in the early 1970s as a technique for developing high-purity semiconductors, in recent years it has undergone suitable modifications to be used for the development of III-V semiconductors as well as metals and insulators (oxides - metal oxide MBE) [1].

The development of heterostructures using the MBE method is carried out in an ultra-high vacuum (UHV) chamber (Fig. 1), necessary for high quality materials without defects and unwanted impurities. The total pressure in an MBE chamber is ~10^{-10} Torr, maintained using a cryogenic pump. Usually, the use of conventional and molecular pumps results in a reduction of the mechanical pressure in the chamber to values of ~10^{-6} Torr, while the final pressure values are achieved using the cryogenic pump (usually with liquid nitrogen).

The solid products are placed in Knudsen cells and are evaporated by heating them at the proper temperature. In the case of refractory metals, the evaporation is done by electron beam, produced by electron gun (e-gun), that locally heats the metal. The atoms or molecules beams of thermal energy produced by this evaporation are directed towards a crystalline substrate (Si, Ge, etc) with very little chance of scattering due to the prevailing vacuum conditions. Then, they interact near and on the substrate which is kept at a suitable temperature resulting in the growth of the respective material. Typical MBE systems have the ability to rotate the substrate during deposition for better coating uniformity.

The composition (stoichiometry) of the developing layer and the percentage of its impurities depends on the relative arrival rates of the atoms or molecules of the products on the substrate or in other words on the relative rates of evaporation of the sources. These rates can be determined with great precision by adjusting the temperature and energy of the incident electrons for the Knudsen cells and the electron gun respectively, thus enabling stoichiometry control.

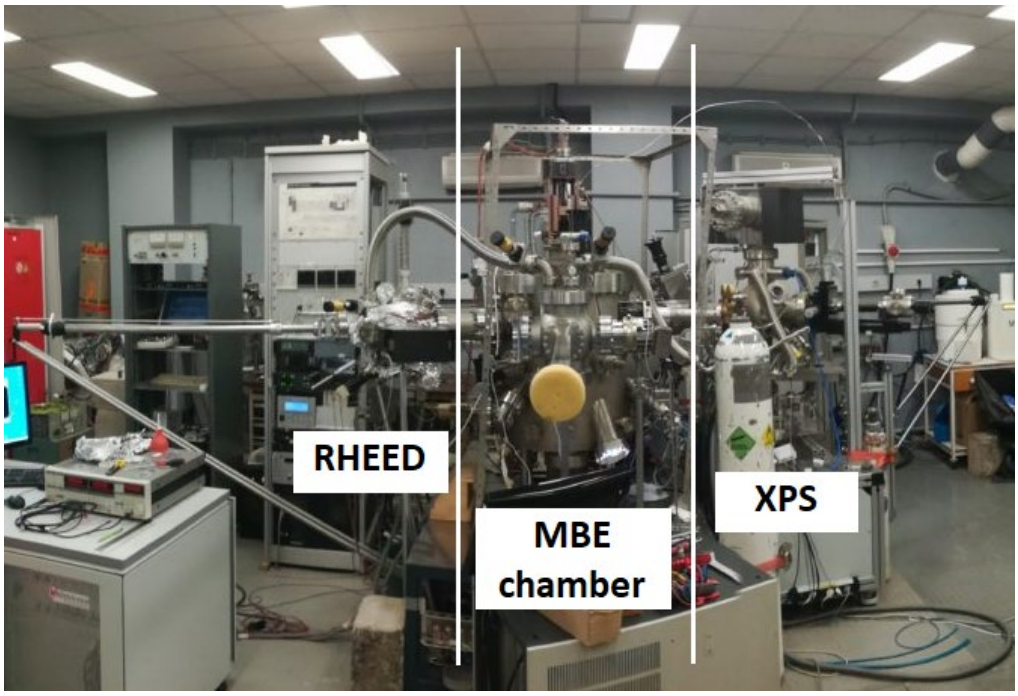

Figure 1: *The MBE system in the institute of nanoscience and nanotechnology (INN) of NCSR Demokritos, consisting of a vertical chamber, a 3-axis manipulator, a mass spectrometer (residual gas analyzer), two high temperature (~2000°C) effusion cells, an Al cell, two e-gun evaporators for refractory metal evaporation, a remote RF plasma source for plasma-assisted epitaxy/deposition of oxides and nitrides. The main MBE chamber is complemented by Reflection High-Energy Electron Diffraction (RHEED) for the in-situ, real-time monitoring of the grown surfaces.*

Contrary to other epitaxial growth techniques such as liquid phase epitaxy and vapor phase epitaxy, in which the growth of materials takes place in conditions close to thermodynamic equilibrium, the growth of materials with the MBE method is carried out under conditions of non-thermodynamic equilibrium due to ultrahigh vacuum conditions. Under these conditions, the composition of the material is dominated by the kinetics of surface processes that take place when the atomic or molecular beams of the products react with the upper atomic layers of the crystalline substrate. The rate of incidence of atoms or molecules on the substrate is

usually small (~ 1 monolayer/s) so as to allow their movement in order to obtain the appropriate positions that are particularly required in the growth of crystalline films.

Due to the vacuum conditions, the MBE method enables the on-site control and analysis of the material development process using diagnostic techniques such as Reflection High Energy Electron Diffraction (RHEED). The in-situ control of atomic-level growth and stoichiometry makes the MBE method a valuable technique for creating complex structures with applications in microelectronics and optoelectronics. MBE played a central role in the development of nanoscience and nanotechnology, allowing researchers to fabricate new structures by, in the words of the The New York Times, “spray painting with atoms” [2]. Although the MBE method presents several advantages compared to other development methods, it also presents some disadvantages which are mainly related to the difficulty of industrial use of the method [3].

Reflection High Energy Electron Diffraction (RHEED)

RHEED is a characterization technique of the surface of crystalline materials, that can be used for in-situ and real-time observation in an MBE chamber. A typical RHEED setup consists of an e-gun and a fluorescent screen as shown schematically in Figure 2. The e-gun is positioned in such a way that the produced high-energy electrons (energies between 10 and 100 keV) hit the sample surface with a small angle of incidence (~ 1° - 5°). The small angle of incidence results in the electrons interacting only with the upper atomic layers of the crystal (typically 2 to 3 atomic layers depending on the angle of incidence). The result of this interaction is a diffraction pattern which is collected on the fluorescent screen at corresponding angles. Usually, the diffraction pattern consists of streaks, instead of the ideally expected spots, corresponding to the sections of reciprocal lattice rod intersected [3, 4].

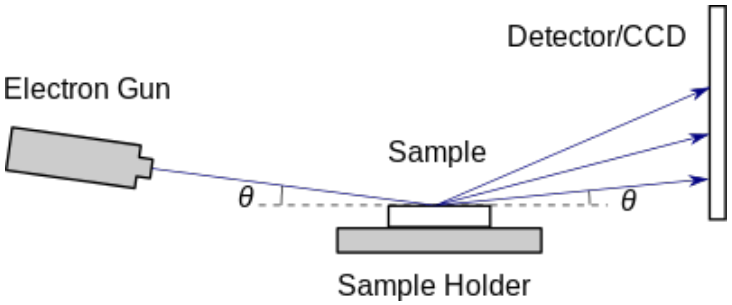

Figure 2: *Scheme of RHEED setup. Electrons from the e-gun, that are diffracted at the sample surface, reach the detector forming the RHEED pattern. (image from Wikipedia/RHEED).*

X-ray Photoelectron Spectroscopy (XPS)

The XPS technique [3, 5] uses X-rays of specific energy (wavelength) to excite electrons from atomic orbitals. Absorption of X-rays by an atom can result in electronic excitation of the atom. The photon absorption process conserves energy, removing an electron from the atom with a kinetic energy (KE) equal to the energy of the incident photon minus the initial binding energy (BE) of the electron, EK=hv-BE (Fig. 3a). The number of photoelectrons collected in a certain period of time is represented as a function of their kinetic energy. This creates an electron count spectrum (number of electrons per second) versus electron kinetic or binding energy (eV) (Fig. 3b). Peaks appear in the spectrum at specific energies due to the emission of electrons from states of specific binding energies (orbitals) in the material. The positions and shape of the peaks determine the chemical state of the elements of the examined material, including oxidation and hybridization states.

The XPS method is widely applied to all types of solids such as metals, ceramics, semiconductors and polymers. It has also been used to obtain spectra of compounds in the gas phase. Generally, it is a non-destructive technique. When applied to solids, the depth of resolution is in the order of ~1-10 nm. The surface sensitivity can be increased by collecting the emitted photoelectrons at various angles to the surface.

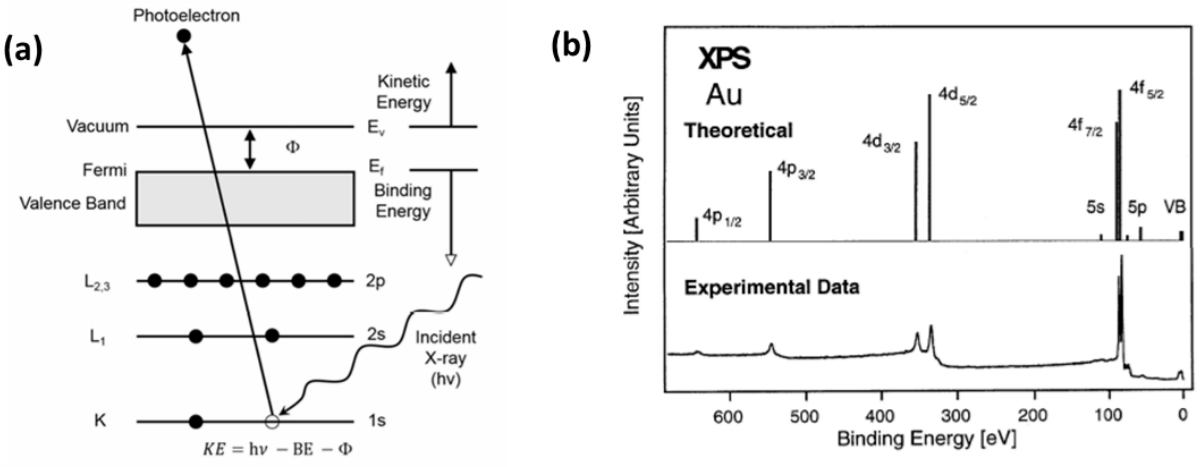

Figure 3: *(a) Schematic illustration of the photoemission process involved in XPS analysis [6]. (b) Theoretical and experimental XPS spectrum of Au [3].*

The penetration depth of X-rays is quite large (in the order of microns). However, the electrons that eventually leave the surface and are eventually detected come from a very small region near the surface. Photoelectrons excited from greater depths scatter inelastically and eventually lose their energy without being able to escape from the solid. Diagrams of the mean free path length for inelastic scattering with respect to the initial kinetic energy of the photoelectrons are used to improve the XPS measurement technique by choosing the appropriate photon energy in order to minimize the inelastic scattering free path length. The device that allows the continuous adjustment of the energy of the photons from the UV to the X-ray region and is used in the XPS technique is the synchrotron.

In our laboratory, Photoelectron Spectroscopy system by SPECS, is integrated with the MBE for ARPES and XPS measurements. The system is equipped with a μ-metal chamber for magnetic shielding, a He discharge plasma source for photon excitation at 21.22 eV, an Al and Mg X-ray source, a 100 mm hemispherical analyzer and a 2D CCD detector for the electronic band structure imaging.

Rapid Thermal Annealing (RTA)

RTA is used for the crystallization annealing of the HZO films after metal capping deposition. A 4-inch cold wall chamber is used (Fig. 4) where the sample is placed on a silicon wafer and heated using halogen lamps through a quartz window in N_2 atmosphere. A spring suspension is used to bring the sample in contact with cold bedplate for fast cooling after annealing. Fresh N_2 gas is injected to improve the cooling rate.

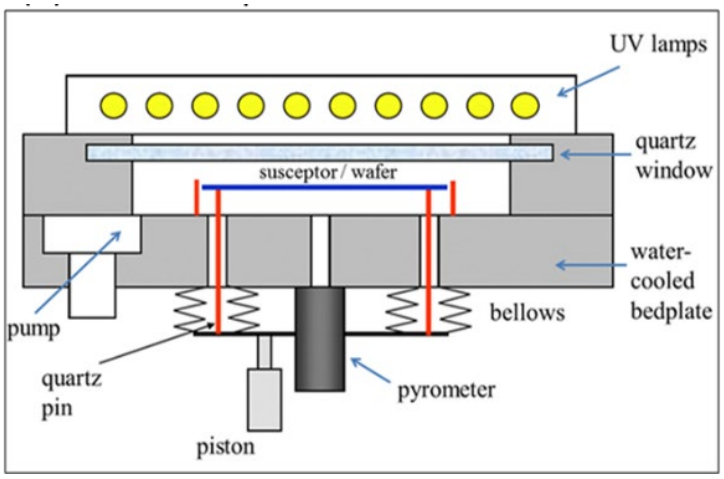

Figure 4: *Rapid Thermal Annealing set-up.*

X-Ray Diffraction (XRD)

XRD [3, 5] is a technique used to identify crystalline phases in various materials and to measure structural characteristics (size and shape of crystallites, internal stresses between crystallites) of these phases. Also, the XRD method is used to determine the thickness of thin films. It is a non-destructive method for the sample and is therefore ideal for in-situ measurements. Materials composed of any elements can be examined by the XRD method. However, it is more sensitive to elements with a large atomic number Z since the diffracted intensity from them is much greater than that of elements with a small atomic number. With suitable laboratory equipment, it is possible to examine samples with thickness 50 Å. However, the use of synchrotron radiation (high intensity radiation) allows the characterization of even thinner films.

When the sample is irradiated with X-rays and an constructive interference from the atomic planes of the crystal occurs, a peak in the intensity of the diffracted beam is observed. The condition for constructive interference from planes separated by a distance d_{hkl} (h, k, l are the Miller indices of the various planes) is given by Bragg's law: $n\lambda=2d_{hkl}\sin\theta_{hkl}$,where θ_{hkl} is the angle between the atomic planes and the incident X-ray beam (Figure 5). In order to observe diffraction, the detector must be positioned so that the diffraction angle is $2\cdot\theta_{hkl}$ and the crystal must be oriented so that the perpendicular to the diffracted plane is coplanar with the incident and diffracted rays.

There are several XRD methods. The Bragg-Brentano geometry (used in the XRD at INN of NCSR-Demokritos) is widely used for randomly oriented polycrystalline films. For ultrathin epitaxial films (smaller than ~100 Å), the Grazing Incidence XRD (GIXRD) method is preferred and is used to characterize monoatomic films. In this method the angle of incidence is small (~0.50) and the X-rays penetrate only ~100-200 Å into the sample. The angle of the diffracted X-rays is also small and the structural information is obtained from planes (hkl) which are perpendicular to the sample surface. Thus, the GIXRD method complements those methods where structural information is obtained from planes parallel to the sample surface (Bragg-Brentano geometry).

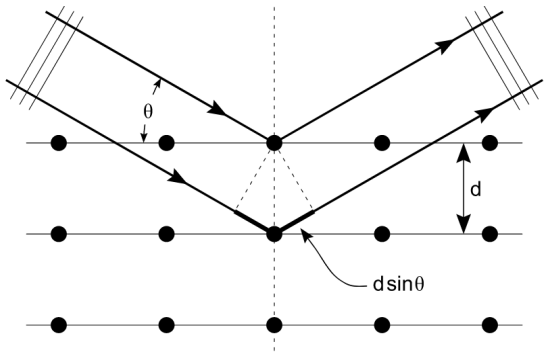

Figure 5: *X-ray diffraction from a crystal. A constructive interference occurs when the path difference of the two rays (2d·sinϑ) is an integer multiple of the wavelength of the radiation. (image from Wikipedia/XRD).*

Electrical characterization

Ferroelectric measurements are performed using an aixAcct Systems TF Analyzer 1000. Electrical measurements are performed in a Janis research ST-500 micromanipulated probe station. The system is equipped with a Helium liquid system and heaters that permit measurements at range temperatures from 4K to 475K.

Ferroelectric Hysteresis Measurement

A typical ferroelectric hysteresis loop is obtained by applying a sequence of triangular voltage pulses, as depicted in Figure 6a. The resulting current response is measured (Fig. 6b) and then integrated over time to produce the polarization (charge) vs voltage loop (Fig. 6c), according to the relationship:

$$Q = D \cdot A \approx P \cdot A \Rightarrow I = \frac{dQ}{dt} = A \cdot \frac{dP}{dV} \cdot \frac{dV}{dt} \quad (1),$$

where Q is the total polarization charge, D the electric displacement, P the polarization, I the measured current, A the area of the capacitor, V the applied voltage and dV/dt (proportional to the frequency) describes the slew rate of the signal. Due to the switching process around the coercive voltage V_c, dP/dV is not constant and the peak switching current will increase in one or two orders of magnitude.

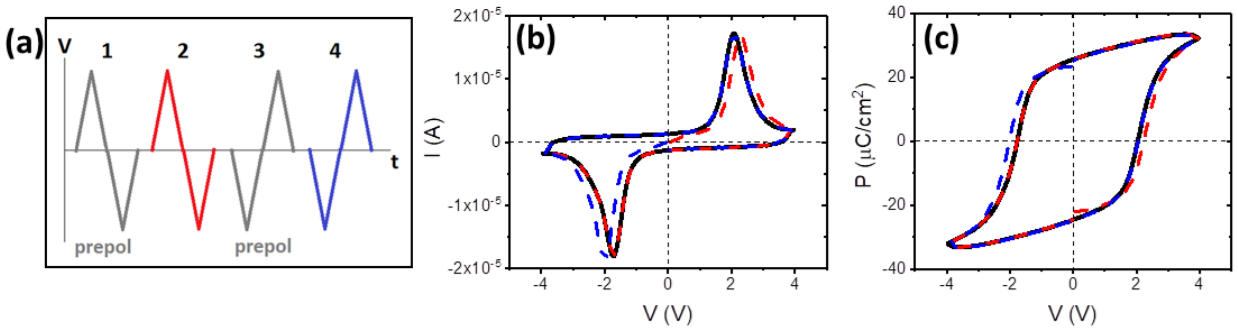

Figure 6: *(a) Voltage pulse sequence applied for a ferroelectric hysteresis measurement and the corresponding (b) current-voltage and (c) polarization-voltage response.*

Pre-polarization write pulses (1 and 3) are used to ensure that all the domains have the same direction, opposite to this of the following read pulses (2 and 4). The polarization is switched both ways for the measurement (pulses 2 and 4). The final hysteresis loop (black curve) is calculated from the second half of the red curve and the second half of the blue curve, that are the de-aged parts.

The measured current has three main contributions: capacitive, leakage and ferroelectric (Fig. 7) [7]. The capacitive current $i_C = C\frac{dV}{dt}$ has a constant value for measurements with constant frequency, as is typically done. The ferroelectric displacement current appears as a peak around the coercive voltage when the polarization switching occurs. The resistive leakage current has usually values lower than the other two components. However, if the capacitor becomes leaky starting to behave as a resistor, the ferroelectric peaks can be masked by the leakage current and the P-V loop is distorted. In any case, the resistive leakage current can be measured separately.

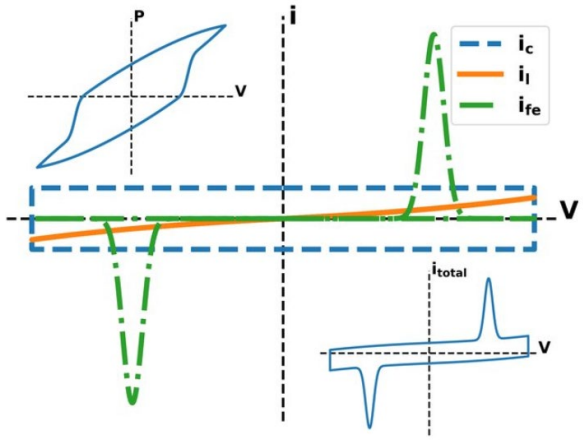

Figure 7: *Capacitive i_c, leakage i_l and ferroelectric i_{fe} contributions of the total measured current in a typical hysteresis measurement [7].*

Positive Up-Negative Down (PUND) method

To correct for leakage and possible contribution from parasitic charges, PUND method [8] is used comprising a write pulse and a sequence of positive and negative read pulses as shown in Fig. 8a. Fig. 8b, c show the main characteristics of an MFS capacitor. The red and blue pulses

give the total polarization, and the green and light blue excursions correspond to the non-ferroelectric contribution by parasitic charges and leakage. By subtracting the parasitic from total curves, we obtain the pure ferroelectric contribution.

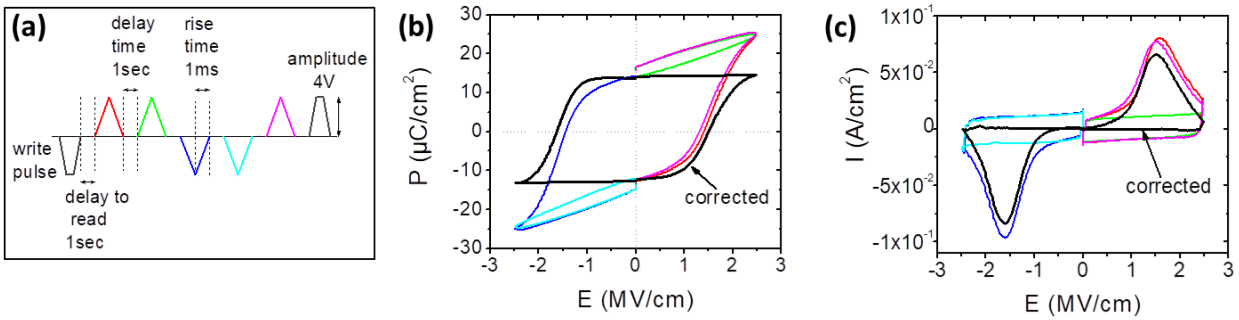

Figure 8: *(a) Sequence of applied electrical pulses in PUND measurement. Polarization P (b), displacement current I (c) versus electric field E. Red curve corresponds to a first positive switching read pulse, magenta and blue to switching read pulses, green and light blue to non-switching read pulses and black are corrected ferroelectric hysteresis curves obtained by subtraction of parasitic contributions (non-switching pulses) from total polarization (switching pulses).*

Electric field Cycling

In order to investigate the reliability and endurance of the ferroelectric devices, field cycling tests are carried out by applying a large number of rectangular pulses to electrically stress the ferroelectric, as shown in Fig. 9a. The cycling is interrupted regularly to perform a dynamic hysteresis measurement in order to gradually examine the influence of the electrical stress on the ferroelectric characteristics, for example the evolution of remanent polarization (Fig. 9b).

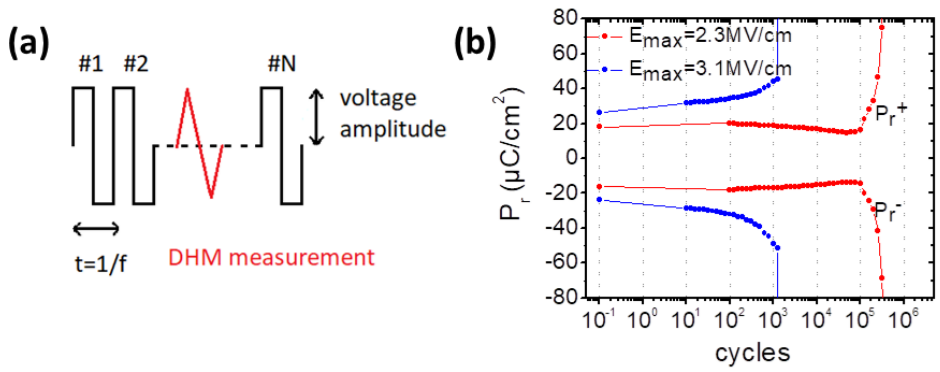

Figure 9: *(a) Voltage pulse sequence for cycling interrupted by dynamic hysteresis measurements. (b) Evolution of remanent polarization during cycling.*

2.2 Fabrication

HZO films are prepared by plasma assisted atomic oxygen deposition (PA-AOD) typically at 120 ^{o}C on single crystal p-type (0.03 Ω ·cm) Ge (100) substrates. Prior to deposition, Ge substrates are annealed at 450^{o}C for 30 min in vacuum to dissociate the native oxide (amorphous GeO_x layer on the surface) and obtain a clean surface free of C and O contaminants. Figure 10 shows the RHEED pattern (a) before cleaning, (b) during annealing at an intermediate temperature 350^{o}C and (c) after 30 min annealing at 450^{o}C. The (2x1) reconstruction after annealing is evidence of a clean surface. The native oxide is dissociated and the surface atoms form bonds.

The HZO films are deposited by co-evaporating Hf and Zr metals from two different electron guns in the presence of reactive atomic oxygen generated by a remote radio-frequency plasma source at 350 Watt and O_2 partial pressure of 6×10^{-6} Torr (Fig. 11a). In-situ RHEED (Fig. 10d) indicates amorphous material.

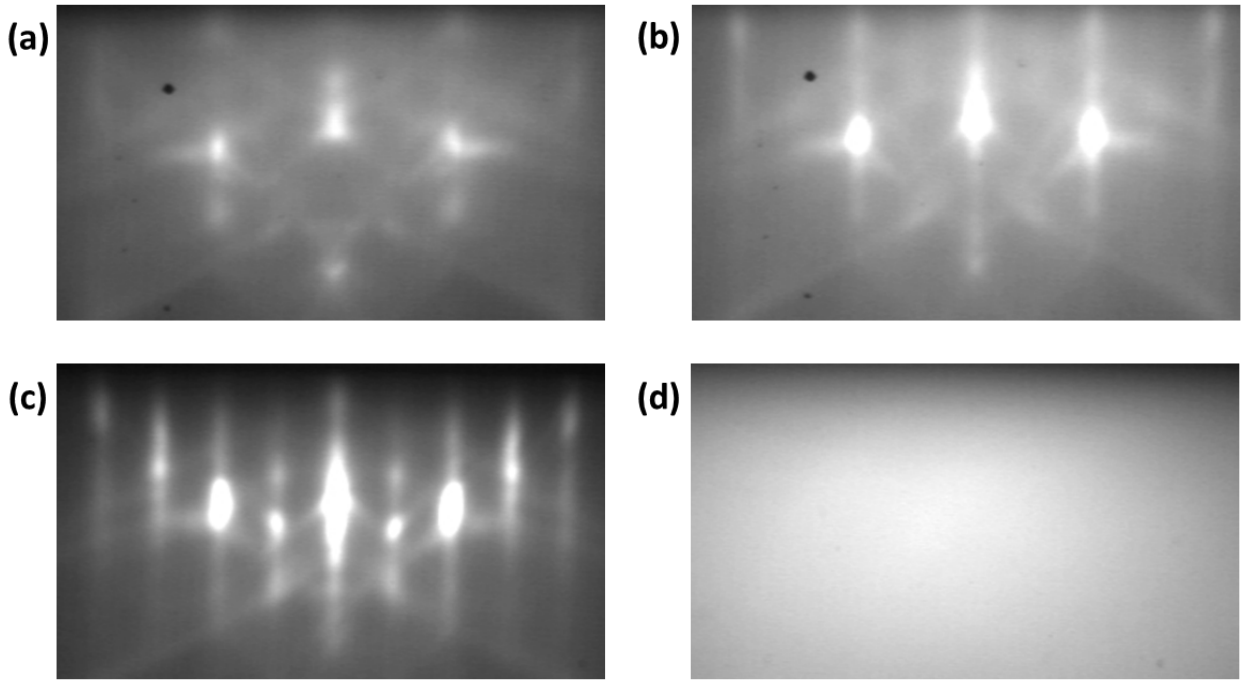

Figure 10: *RHEED spectrum of the surface of the Ge substrate (a) before cleaning, (b) after annealing at an intermediate temperature 350°C and (c) after annealing at 450°C, where the 2x1 reconstruction indicates the clean surface, free of native oxide. (d) In-situ RHEED of the amorphous as-grown HZO layer.*

Nominally 10-nm-thick TiN metal are grown on top of HZO films without breaking vacuum at room temperature, 270°C, 385°C with an evaporation Ti rate of 0.2 Å/sec and rf plasma at 350 Watt. To fabricate the MFS capacitors, Ti(5nm)/Pt(40nm) metal contacts are deposited on the Ge/HZO/TiN device layer structures either by shadow masking or by photolithography producing 300 µm and 50 µm dots, respectively. Subsequently, the samples receive rapid thermal annealing (RTA), typically at 750°C for 20 sec in N_2 and a ramp-up rate of 150°C/sec. In addition to the proper doping, the annealing process is also critical for the achievement of ferroelectricity in hafnia. Annealing at high temperatures leads to the tetragonal phase. During the cooling down after annealing, the monoclinic phase, which is energetically favorable, is normally stabilized. By using the TiN capping layer and fast cooling rate, the expansion of m-phase is mechanically suppressed, and the orthorhombic/ferroelectric, which is an intermediate phase, is stabilized.

Finally the TiN layer is selectively etched by $NH_4OH/H_2O_2/H_2O$ or H_2SO_4/H_2O_2 solution to finalize the Ge MFS capacitor (Fig. 11b).

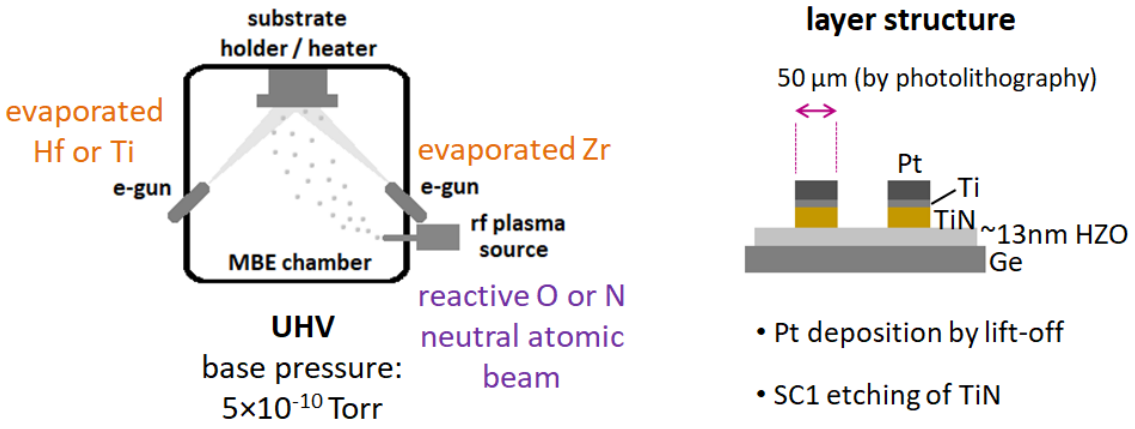

Figure 11: *(a) Deposition of HZO and TiN layers* by *PA-AOD in MBE chamber schematically. (b) Final layer structure of capacitors.*

The structure parameters and measured performance characteristics of the various MFS capacitors are summarized in Table I.

Zr composition x	Thickness (nm)	TiN growth T (°C)	Remanent polarization P_r (µC/cm²)	Coercive field E_c (MV/cm)
0.66	16	270	21.1(17.9)	1.5
0.58	13	RT	34.4(30.6)	1.8
0.50	16	385	21.7	1.9
0.70	9	RT	18.6	3.4

Table I: *In all samples HZO layers are grown at T_g=225 °C and received crystallization RTA at 750 °C for 20 sec with a ramp up rate of 150 °C/sec. The Zr composition x is determined by RBS. Thickness is nominal estimated from deposition rates which have been calibrated by XRR measurements, except for x=0.58 HZO whose thickness is measured by TEM. For remanent polarization, values corrected for leakage and parasitics by PUND measurements are given in parentheses.*

2.3 Physical characterization

Composition evaluation of HZO

The stoichiometry of HZO films was first estimated by in-situ XPS, right after the deposition. The Zr3d and Hf4f peaks were fitted and their areas were divided by their sensitivity factors (SF_{Zr3d}=2.1, SF_{Hf4f}=2.05). In this way, the Zr/Hf ratio was extracted (Fig. 12a). Also, Energy-dispersive X-ray spectroscopy (EDS) was carried out to some samples using a FEI Quanta Inspect SEM equipped with a thermionic gun and a tungsten cathode, operated at 5 kV. EDS spectra were collected over several spots on each sample. Quantitative analysis was performed using the EDAX Genesis software and the ZAF correction method. The ratio of atomic % (At %) elemental composition based on HfM and ZrL transitions/lines, provides a nominal stoichiometry of HZO (Fig. 12b).

In order to verify this estimation, Rutherford Backscattering Spectroscopy (RBS) was performed to selected samples, which is a more accurate technique (Fig. 12c). The measurements were conducted at the microprobe setup installed at the 5.5 MV Tandem accelerator of the Institute of Nuclear and Particle Physics, NCSR “Demokritos”, by Dr. Michail Axiotis and Dr. Anastasios Lagoyannis. The samples were irradiated with a 1.4 MeV deuteron which was focused to a beam spot of 50×50 μm^2 on target. The backscattered deuterons were detected with the aid of a SSB detector placed at 150^o with respect to the beam axis. The acquired spectra were analyzed using the SIMNRA code [9]. XPS results were in good agreement with RBS, so it was used for the rest of the samples.

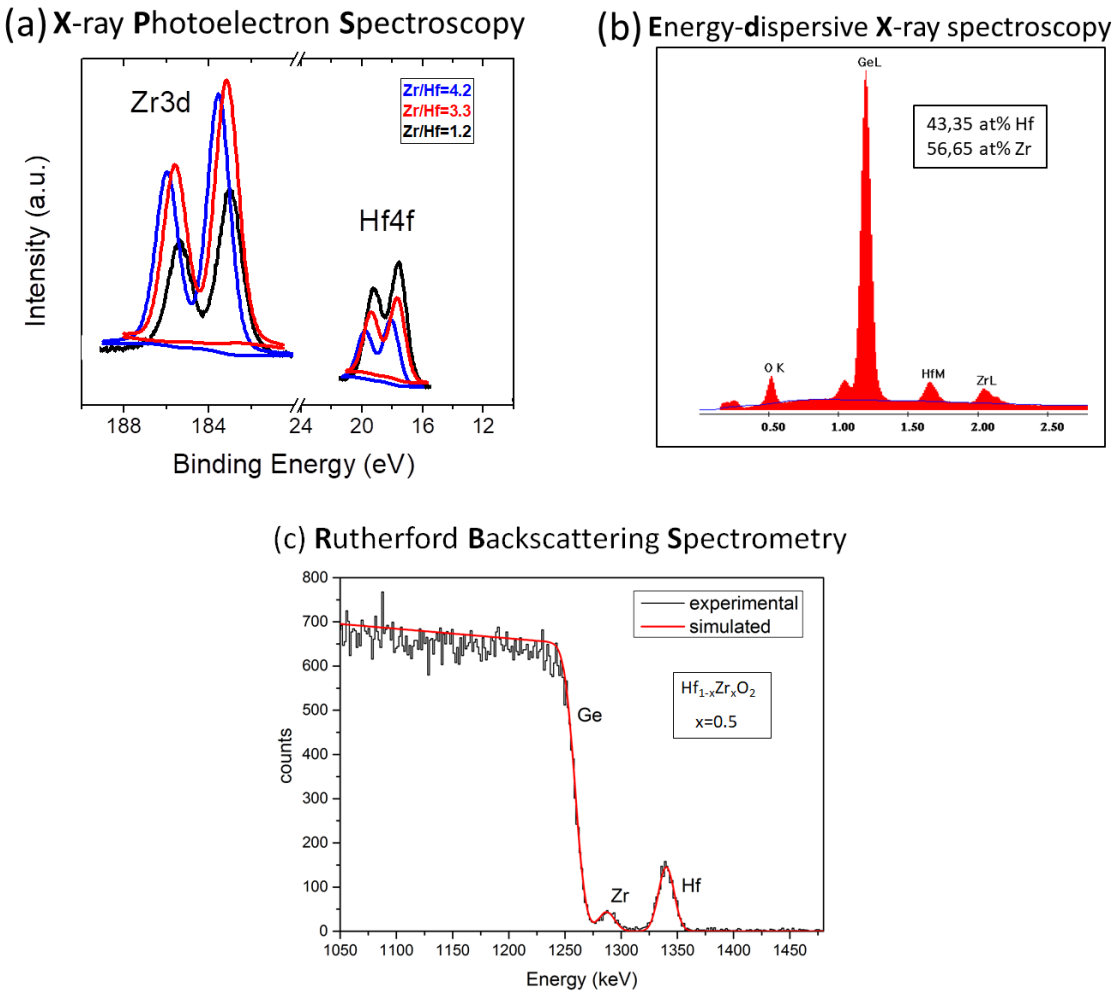

Figure 12*: (a) Composition evaluation of HZO films by (a) in-situ XPS, (b) EDS and (c) RBS.*

Physical Characterization of TiN

The TiN layer was also characterized by in-situ XPS using a Mg Kα radiation at 1253.6 eV. Gaussian-Lorentzian shapes (Voigt functions) were used for deconvolution of the recorded spectra after standard Shirley background subtraction. The core-level photoemission Ti 2p and N 1s spectra are presented in Fig. 13 (a) and (b) respectively.

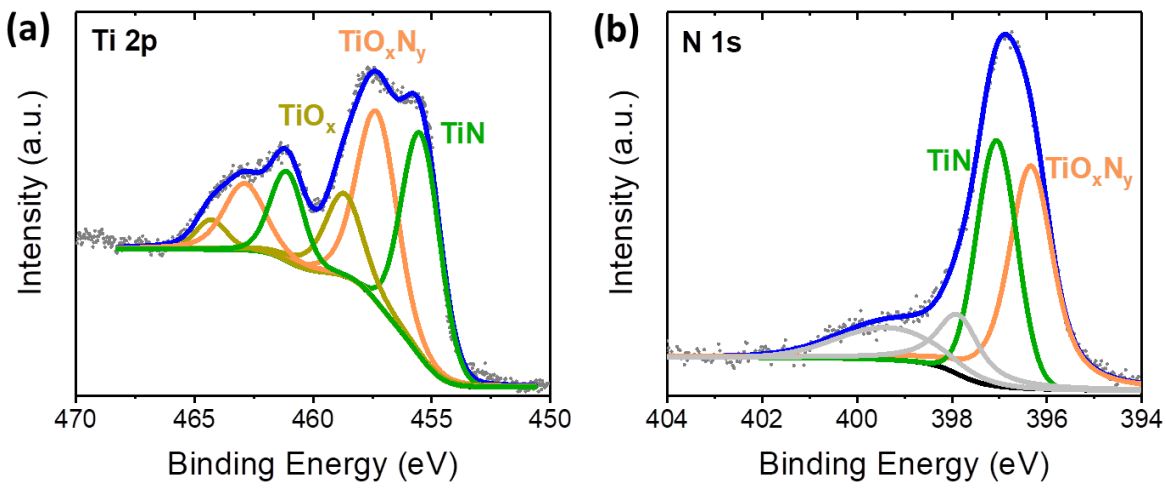

Figure 13: *(a) Ti 2p and (b) N 1s XPS spectra of the TiN top electrode.*

The Ti 2p spectrum is fitted with three spin-orbit split components. The first one located at the lowest binding energy 455.5 eV is assigned to metallic TiN. The second peak at 457.34 eV reveals the additional formation of an oxynitride phase (TiO_xN_y), and the third one at 458.74 eV is attributed to oxidized Ti (TiO_x). The energy split for each peak is $\Delta E(Ti2p_{1/2}\text{-}Ti2p_{3/2})$= 5.6 eV, as expected from the literature [10].

Analysis of the N 1s spectrum reveals two main peaks; the one at higher binding energy 397.1 eV indicates the Ti-N bonds of metallic TiN, while the peak at 396.4 eV the formation of TiO_xN_y phase, as found in Ti 2p spectrum. The two additional peaks at 397.9 and 399.4 eV are related to molecular nitrogen species, which are inherent features of TiN and other transition-metal nitride surfaces [11]. The TiO_xN_y phase is most probably related to the oxygen vacancies near the TiN/HZO interface, as a result of oxygen scavenging in the HZO by the top electrode, while the relatively small proportion of TiO_x is attributed to surface oxidation of the TiN layer.

These results are in good agreement with the extensive study by W. Hamouda et al. on the physical chemistry of the TiN/HZO interface in an MFM structure TiN/FE-HZO/TiN [12].

Finally, using the tabulated sensitivity factors SF (N 1s)=0.42 and SF (Ti 2p3/2)=1.2 for the peaks corresponding to the TiN component, and deriving their areas, the Ti/N ratio was found to be 1.12, that is nearly stoichiometric.

Thickness determination

Selected samples were measured by XRD, after crystallization annealing and TiN etching. Their thickness was determined based on X-ray Reflectivity (XRR) (Fig. 14). In this way, the nominal thickness calculated by rate monitor during HZO deposition was calibrated for the rest of the samples. The thickness was also verified by TEM.

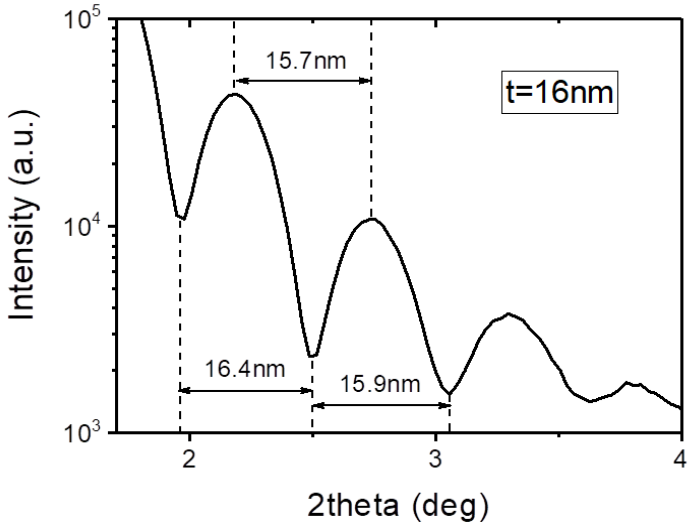

Figure 14*: Thickness determination of a 16-nm-thick HZO film by XRR.*

High Resolution Transmission Electron Microscopy (HRTEM)

The MFS structures with x=0.58 were characterized by High Resolution Transmission Electron Microscopy (HRTEM) and Selected Area Electron Diffraction (SAED) (Fig. 15) on specimens prepared by focused ion beam (FIB), by Raluca Negrea and Lucian Pintilie at NIMP. The HZO and TiN layers are uniform and continuous each with thickness of ~13 nm and have roughness less than 1 nm and 3 nm respectively (Fig. 15a). The HZO layers are polycrystalline (Fig. 15b,c) with a domain size in the range between 20 and 30 nm. Sharp crystalline interfaces are observed (Fig. 15c), free of interfacial amorphous oxide layers, in distinct contrast with the HZO/Si interfaces [13] where an amorphous interfacial oxide >1 nm is typically formed. The SAED diffraction pattern (Fig. 15b) reveals the presence of orthorhombic phase ((111)o diffraction spots), while

diffraction from monoclinic phase could not be detected. This indicates that the HZO film is predominately orthorhombic.

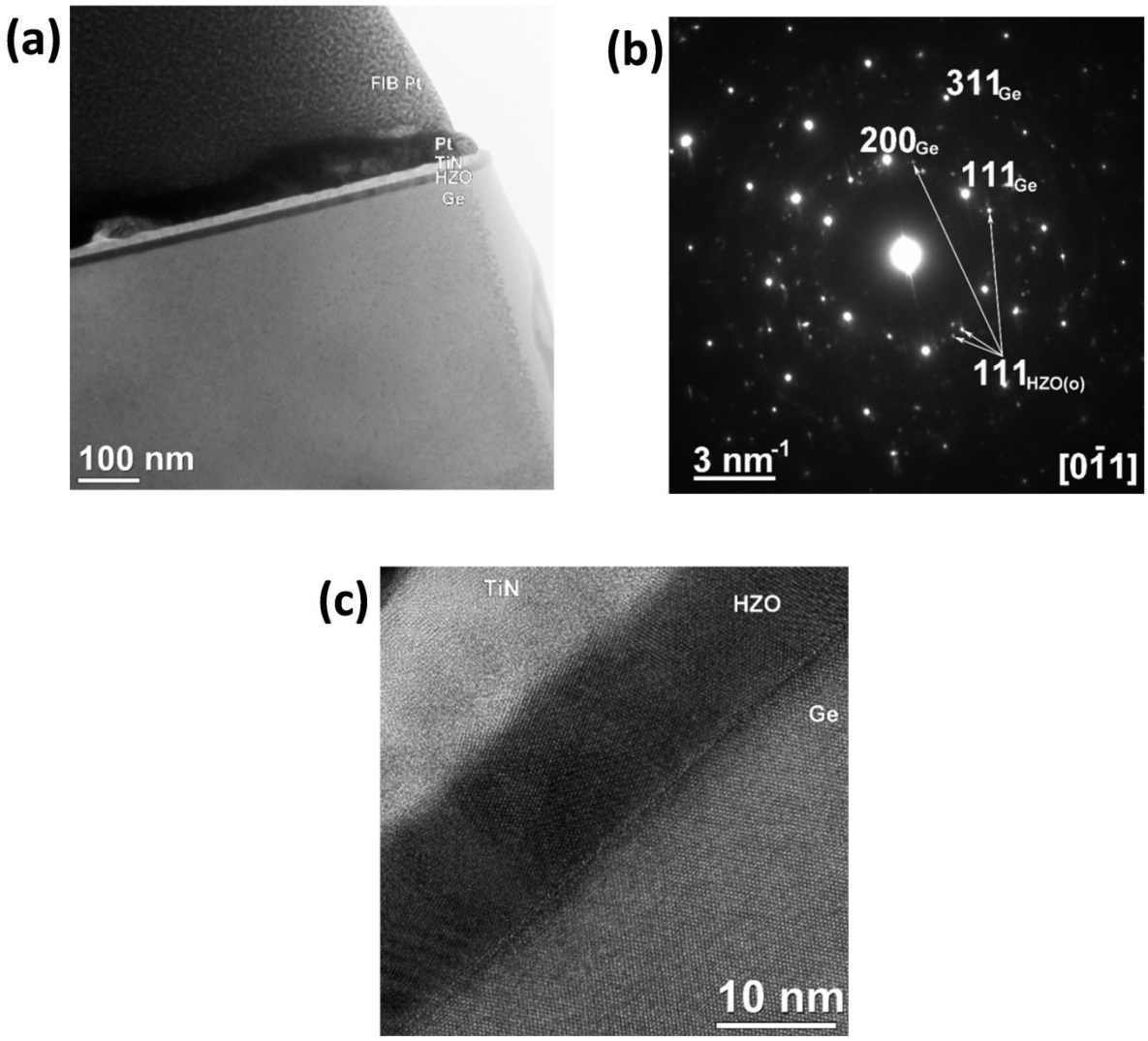

Figure 15: *(a) Cross section TEM image of MFS with Zr composition x=0.58 on a specimen prepared by FIB, (b) SAED pattern corresponding to TEM in (a). Arrows show the orthorhombic (111) diffraction spots. (c) HRTEM image of Ge/HZO/TiN/Ti-Pt heterostructure.*

Based on previous works on the role of tensile strain [14, 15], it is anticipated that a predominately orthorhombic phase here in this work is stabilized by residual thermal tensile strain $\varepsilon \approx +\delta\gamma \cdot \delta T \approx 0.3\%$ due to a sizeable thermal expansion coefficient mismatch $\delta\gamma \equiv \gamma_{HZO} - \gamma_{Ge} = 4.1 \cdot 10^{-6}\ K^{-1}$ ($\gamma_{HZO} \sim 1 \cdot 10^{-5}\ K^{-1}$ [16] and $\gamma_{Ge} = 5.9 \cdot 10^{-6}\ K^{-1}$ [14]) and a temperature difference

δT=725 K between the crystallization annealing temperature T_{ann}=1023 K and room temperature. It should be noted that the clean, crystalline interfaces (Fig. 15c) may promote the build-up of the thermal tensile strain as the HZO contracts faster than Ge during cooling down.

2.4 Electrical characterization

Dynamic P-E measurements at 1 kHz were performed using an aixAcct Systems TF Analyzer 1000 and the main hysteresis characteristics are shown in Fig. 16. The Ge MFS hysteresis in the present work is more symmetric compared to Si MFS [13]. All hysteresis curves show weak or no "wake-up" effects. In the MFS of Fig. 16, the coercive field E_c is 1.8 MV/cm. With an exception of the 9-nm-thick film where the E_c is abnormally high (3.4 MV/cm, Table I) more generally in our PA-AOD films E_c varies in the range between 1.3 and 2.0 MV/cm which is notably larger than the E_c values (~1 MV/cm) [17] reported for HZO MFM capacitors grown by ALD. We anticipate that the large value of E_c in our MFS is indicative of reduced (interfacial) defects typically obtained in high quality epitaxial [18] thin films. The high E_c of 1.8 MV/cm may be beneficial for FeFETs increasing the memory window (MW) [19] to about 4.7 V, according to $MW=2d_{HZO}E_c$.

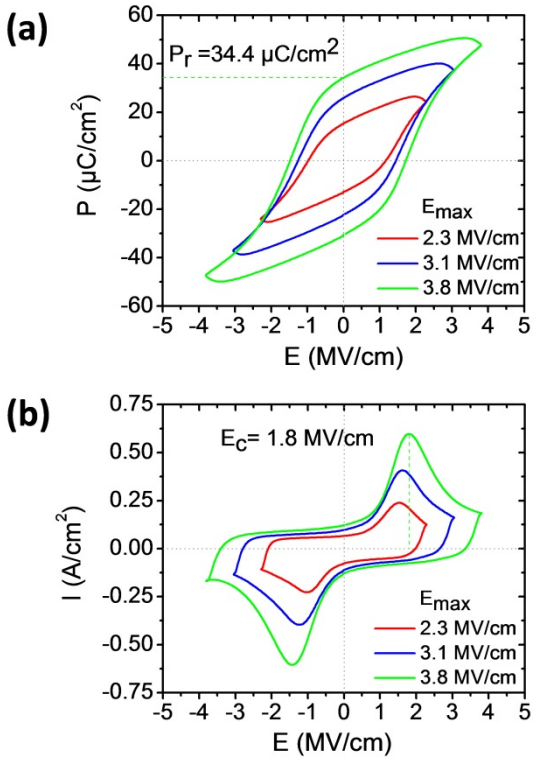

Figure 16: *(a) Polarization (P) and (b) displacement current (I) vs electric field measurements (1kHz) for 2.3, 3.1 and 3.8 MV/cm field amplitude for a pristine 13-nm-thick HZO with composition x= 0.58.*

The largest value of remanent polarization P_r=34.4 μC/cm^2 for E_{max}=3.8 MV/cm (V_{max} =5 V) is obtained (Fig. 16) in the 13-nm-thick sample with x=0.58. Other devices with higher (x=0.66, 0.7) and lower (x=0.5) Zr compositions also give robust and symmetric hysteresis, although with reduced but appreciable remanent polarization, typically larger than 20 μC/cm^2 (see Table I). The large P_r is attributed to the predominant FE orthorhombic phase as detected by TEM/SAED.

Despite the large P_r in Fig. 16 of the x=0.58 MFS capacitors the I-E measurements show that there is appreciable leakage, which may affect the P_r yielding erroneous results. To correct for leakage and possible contribution from parasitic charges, positive up-negative down (PUND) method [8] was used comprising a "write" pulse and a sequence of positive and negative "read" pulses as shown in Fig. 17a. Fig. 17b,c show the main characteristics of one of the MFS capacitors with x=0.58. It can be seen that the non-ferroelectric contribution (green and light blue excursions) is a small portion of the total polarization and displacement current, yielding,

after correction (black curves), a nearly ideal hysteresis (Fig. 17b) and current (Fig. 17c) with a small (12.1 %) reduction in the remanent polarization from a value of P_r = 34.8 μC/cm^2 to a value of $P_{r,\ corr}$= 30.6 μC/cm^2 after correction. This indicates that most of the measured polarization is due to the ferroelectric switching with only minor contribution from parasitic charges and leakage. The value of 30.6 μC/cm^2 is among the largest P_r reported for HZO. More specifically the attained P_r in the present work is larger than those obtained in ALD HZO MFM [15, 17] which are typically around 20 μC/cm^2 [17], only exceptionally reaching 26 μC/cm^2 [15]. Our P_r values are also larger than those measured in HZO Ge FTJ [20] devices. Ultrathin (5 nm) epitaxial HZO on LSMO substrates [18] show larger (corrected) P_r~ 34 μC/cm^2, but thicker (9 nm) HZO layers on LSMO [18] show much reduced values of P_r ~ 18 μC/cm^2, which are lower than the ones observed in the present work.

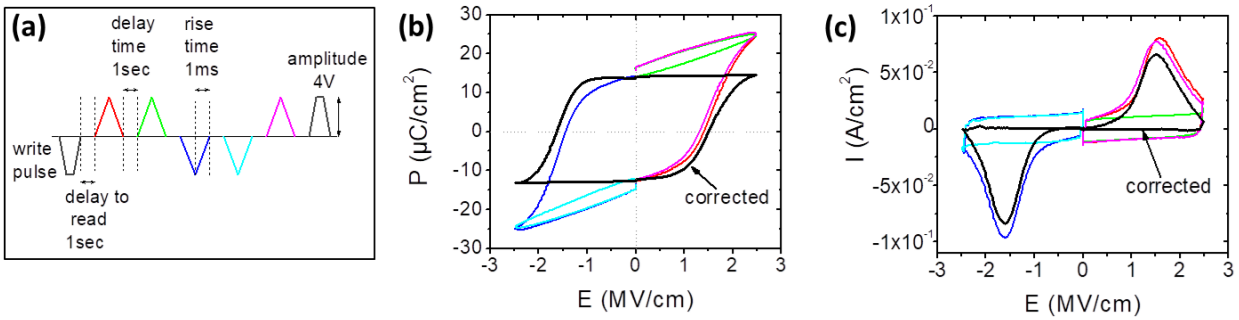

Figure 17: *(a) Sequence and shape of applied electrical pulses in PUND measurement. Polarization P (b), displacement current I (c) versus electric field E curves for a pristine 16-nm-thick HZO with composition x= 0.58 at Emax=2.8 MV/cm. Red curve corresponds to a first positive switching read pulse, magenta and blue to switching read pulses, green and light blue to non-switching read pulses and black are corrected ferroelectric hysteresis curves obtained by subtraction of parasitic contributions (non-switching pulses) from total polarization (switching pulses).*

In order to investigate the reliability and endurance of the ferroelectric devices, field cycling tests were carried out. The results for the 13-nm-thick sample with x=0.58 composition at two different cycling field amplitudes are shown in Fig. 18. Although the wake-up effects are relatively weak, fatigue appears after 1000 cycles for cycling field of 2.3 MV/cm before the

devices breakdown after 100 000 cycles. Note however that despite fatigue, the P_r value remains well above 10 µC/cm^2 maintaining an acceptable window until it reaches breakdown. For larger fields (3.1 MV/cm), the devices break down after ~1000 cycles. After this point and at negative bias corresponding to a forward-biased p-type MFS diode, the leakage current increases and the hysteresis is distorted (Fig. 18c) developing a pronounced bump. The dc leakage, confirmed by I-E measurements, is considered to be the primary reason for the breakdown of MFS capacitors since HZO becomes essentially a resistor after further cycling beyond 1000.

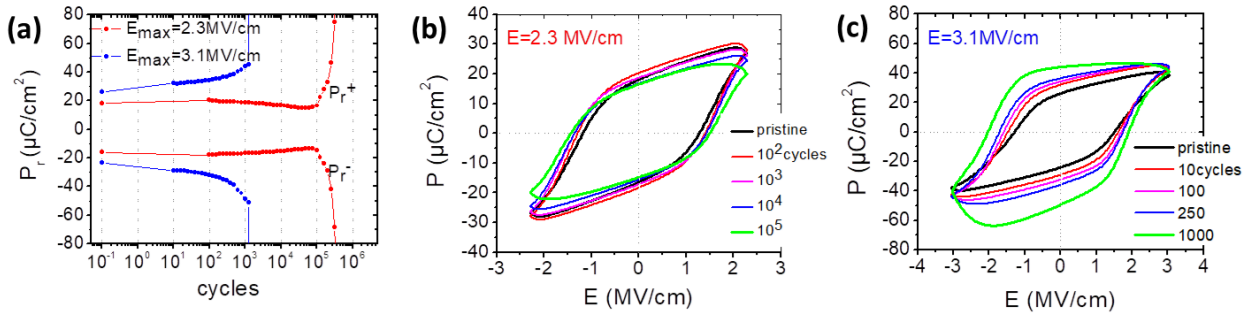

Figure 18: *(a) Field cycling measurement for a 13-nm-thick sample with composition x= 0.58. Impact of field cycling on hysteresis loop at (b) 2.3 and (c) 3.1 MV/cm.*

MFM devices with ALD HZO generally show endurance larger than 10^9 cycles [21, 22], however in MFS capacitors the situation is different. In the latter devices, the presence of a semiconductor (S) at the bottom electrode has adverse impact on endurance. Therefore FeFETs which are based on MFS structure show much lower endurance [19], typically in the order of 10^4 -10^5. Our endurance results (10^5 cycles at 2.3 MV/cm) compare favorably with the endurance in FeFETs. Our results also compare favorably with cycling behavior of 8 nm HZO FTJs with Ge bottom electrode [20] although charge transport and associated breakdown mechanisms in thin FTJs are different compared to the thicker HZO (>10 nm) Ge MFS diodes studied in the present work, so a direct and fair comparison is not feasible.

2.5 Conclusions

In summary, the Ge MFS capacitors with HZO and TiN top electrode, both grown by plasma assisted atomic oxygen deposition in one growth step, show excellent hysteresis characteristics with relatively high coercive field, little or no wake-up effects and with only small contribution from parasitic polarization effects, exhibiting a very large remanent polarization and good endurance when compared with the endurance of other MFS or FeFETs. It is anticipated that the high remanent polarization is due to predominance of the orthorhombic phase verified by TEM/SAED, which is likely stabilized as a result of residual thermal tensile strain originating from the Ge substrate. These performance and reliability characteristics in combination with the sharp crystalline HZO/Ge interfaces probed by TEM create the prospect that Ge FeFETs can be fabricated that overcome the short-comings of Si-based FeFETs which show limited endurance and reduced experimental memory window. The above study resulted in journal publication [23].

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Chapter 3

Depletion induced Depolarization Field and Interface Defect States

3.1 Introduction

Metal-Ferroelectric-Metal capacitors made of Si-compatible $Hf_{1-x}Zr_xO_2$ with x~0.5 (HZO) ferroelectric (FE) have been extensively studied [1-5] for low power 1T-1C non-volatile embedded memories integrated in the back-end-of-line (BEOL) of CMOS [6]. A different device layer structure, namely Metal-Ferroelectric-Semiconductor (MFS) is the main building block of 1T ferroelectric field effect transistor (FeFET) non-volatile memories [7] which have potential advantages in terms of scaling, non-destructive reading and front-end-of-line (FEOL) integration with CMOS. Moreover, they can be used to realize artificial ferroelectric integrate-and-fire neurons [8] and analog synapses [9, 10] for neuromorphic computing [11]. Si MF(I)S draw a lot of attention but the presence of Si bottom electrode in direct contact with the HZO produces interfacial SiO_x or Hf(Zr) silicate insulating layers which cause reliability problems for FeFETs [12]. Depolarization fields in particular can severely affect the hysteresis loop [11, 12] at room temperature (RT) by reducing the attainable switchable polarization as well as the memory window, thus directly impacting memory performance.

FeFETs on technologically important Ge [13] is an interesting alternative device that has already been successfully used for the fabrication of non-volatile analog memristive synapses functioning as accelerator for on-line learning in neuromorphic circuits [14]. Moreover, negative capacitance FETs with subthermionic steep slopes have been demonstrated in Ge/HZO FETs [15-17] suitable for low power/high performance applications.

Germanium MFS and FeFETs could help overcome some of the shortcomings of Si FeFETs. Notably, Ge/HZO interfaces are reported to be sharp and clean [18-20], free of interfacial oxides, which could mitigate some of the reliability issues. Despite the absence of an interfacial insulating layer, when the MFS is biased in depletion, the screening of polarization charge weakens, potentially creating a depolarization field in the ferroelectric which could adversely impact retention and imprint of memory states. This has motivated us to systematically investigate, as a function of temperature, the build-up of a depolarization field originating from depletion of Ge semiconductor near the interface. Our studies show that the formation of depletion in Ge at low temperatures (<160 K) creates a strong depolarization field which

severely distorts the hysteresis characteristics. However, at higher temperatures and especially at RT, due to its low energy gap (E_g), Ge has high minority carrier population, sufficient to screen the polarization charges in Ge MFS, essentially diminishing the depolarization field. As a result, nearly ideal, symmetric polarization curves are obtained [20-24].

3.2 Temperature dependence of Ge-MFS capacitors

TiN/HZO/Ge (100) MFS device layer structures were produced by plasma assisted atomic oxygen deposition in a molecular beam epitaxy chamber. In this work, three different samples are studied: a 12-nm-thick HZO film on a p-Ge substrate with resistivity ρ=(0.03-0.07) Ω·cm, a 13-nm-thick HZO on a highly doped n^+-Ge (0.004-0.006 Ω·cm) and a 13-nm-thick HZO on a lightly doped n-Ge (0.34-0.35 Ω·cm), all with Zr composition x~ 0.6.

As in our previous work [20], HZO is polycrystalline with grain size 15-20 nm, comparable to the thickness as seen in Fig. 1(a). The HZO/Ge interface is crystalline and clean (Fig. 1(b)), free of interfacial oxide or germanate layers as expected [18-20].

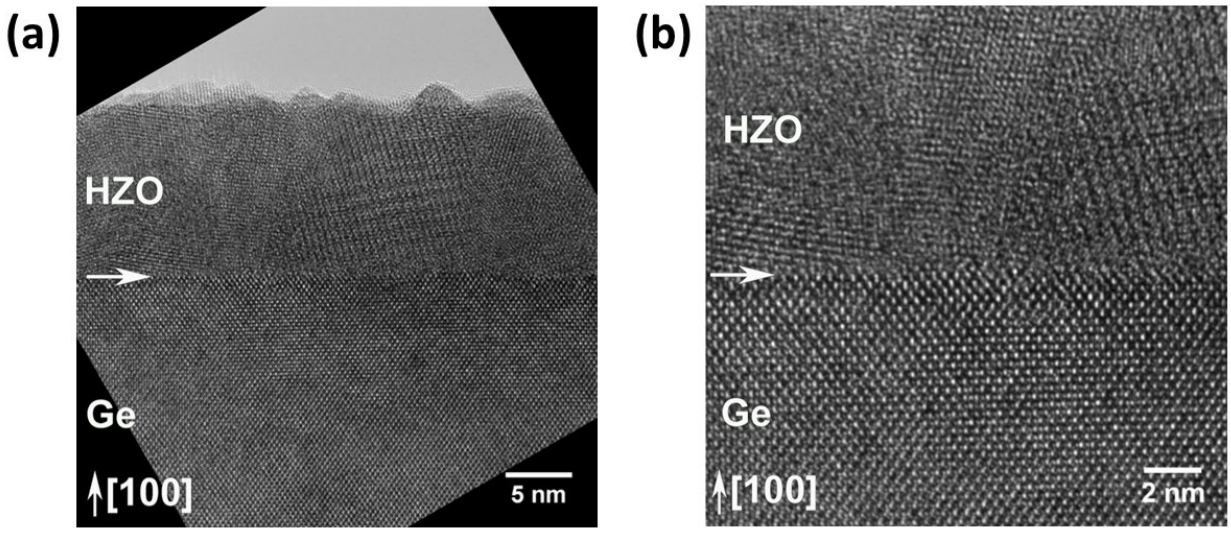

Figure 1: *HRTEM cross-sectional images of HZO on p-Ge (100) substrate. (a) Microstructure of 13 nm ferroelectric HZO layer and (b) the sharp HZO/Ge interface, free of interfacial amorphous oxide layers.*

Polarization (P) and displacement current (I) of the ferroelectric capacitors were measured using an aixAcct Systems TF Analyzer 1000. The capacitors showed robust and symmetric pristine hysteresis curves at RT with no wake-up effects and good electrical endurance of 10^5 cycles similar to those previously reported [20]. Temperature measurements from RT to 77 K were performed using a micromanipulator in high vacuum conditions.

Temperature and frequency data are presented in Figures 2 and 3. In the case of MFS on n^+-Ge substrate (Fig. 2(a)-(b)), as temperature decreases, a slight shift of coercive voltage V_c to higher values is observed ($\Delta V \sim 0.6V$), which is nearly the same for both V_c^+ and V_c^-. This weak variation is attributed to a temperature dependence of the coercive field E_c as predicted by Landau-Ginzburg mean-field theory [25] and previously reported [26]. For the MFS on n-Ge substrate (Fig. 2(c)-(f)), V_c^+ is slightly increased (only by ~ 0.4 V), whereas V_c^- shows a significant shift of about 2 V to higher negative values as the temperature is lowered. The polarization loop gradually becomes non-ideal and asymmetric with reduced P_r, similar to the one observed in Si based MF(I)S capacitor [11, 12]. It is worth noting that at higher frequencies (Fig. 2(c)-(f)), the degradation of hysteresis loop is more pronounced and the V_c^- shift is larger as the temperature is reduced (see detailed discussion later).

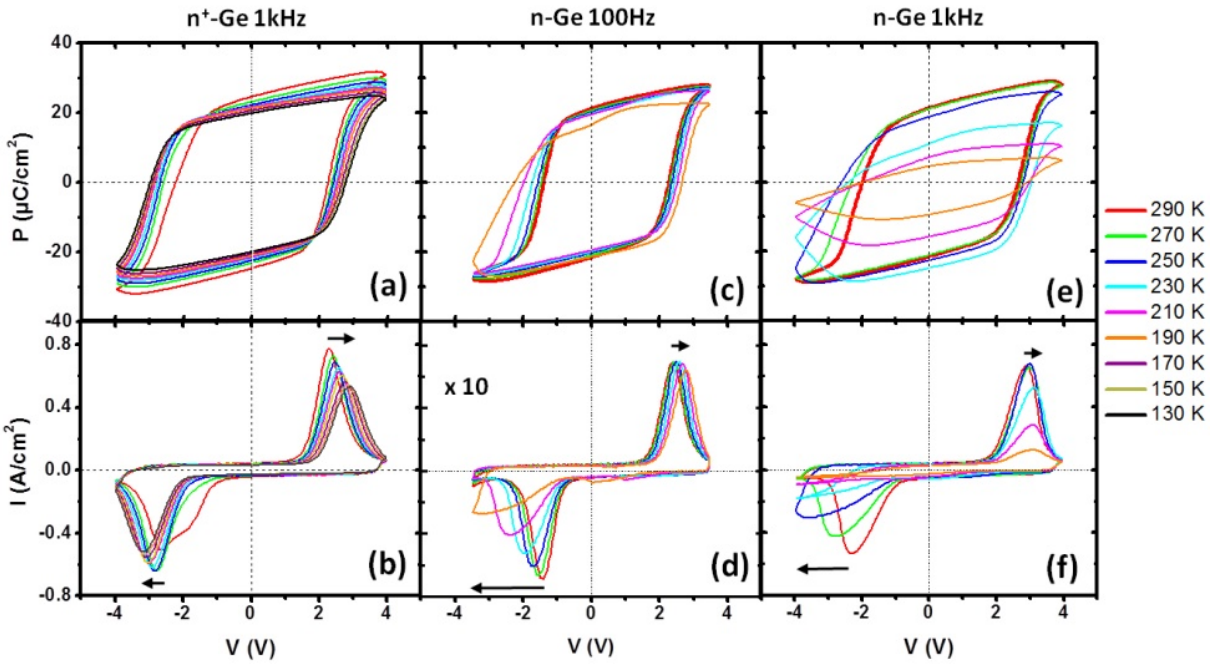

Figure 2: *Polarization and displacement current vs voltage measurements for MFS capacitors on (a)-(b) highly doped n^+-Ge and low doped n-Ge substrate at (c)-(d) 100 Hz and (e)-(f) 1 kHz. The arrows show the shift in the coercive voltages V_c^+ and V_c^- in accumulation and depletion/inversion, respectively.*

The opposite behavior is observed for the capacitor on p-Ge substrate (Fig. 3 (a)-(b)) where V_c^+ shows considerable shift of about 1.4 V as the temperature is lowered, while V_c^- remains nearly unchanged (maximum shift of ~0.5 V). For an in-depth investigation, high frequency capacitance-voltage (C-V) measurements were performed for p-Ge/HZO/TiN MFS capacitor (Fig. 3 (c)). At RT the characteristic "butterfly" ferroelectric peak configuration appears, indicating that the device essentially behaves like an MFM capacitor. With decreasing temperature, the gradual transition to a typical p-type MIS behavior is clearly seen which can be correlated with the evolution of the polarization curve.

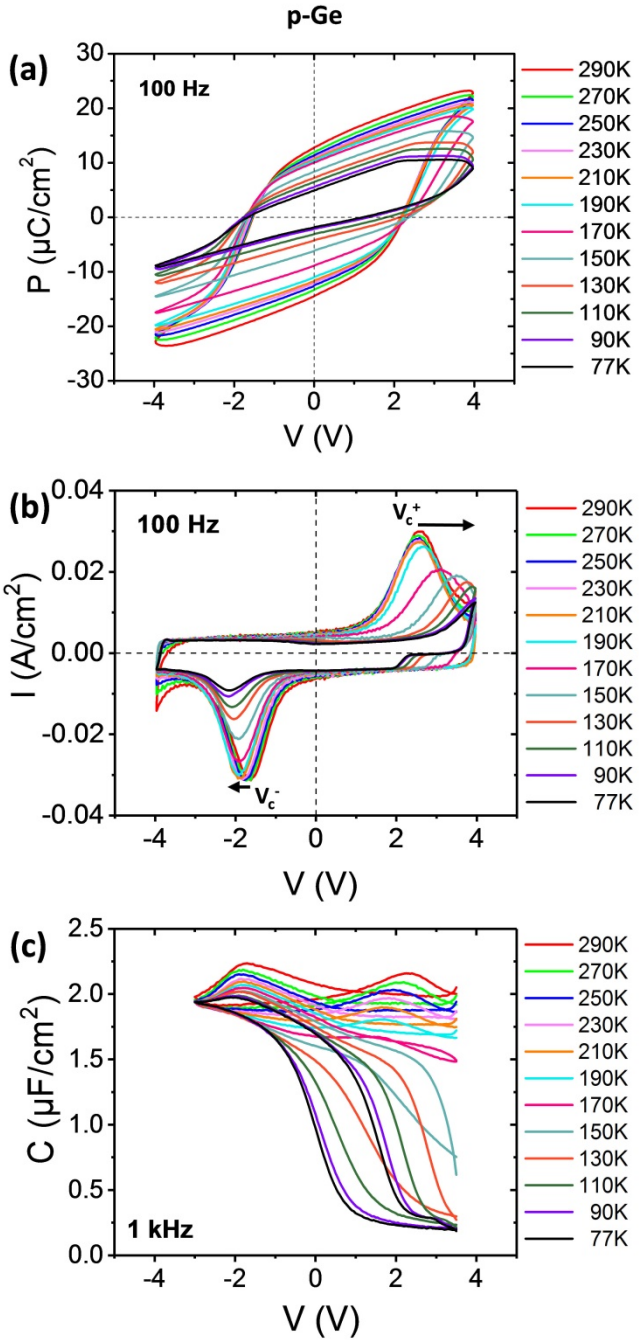

Figure 3: *(a) Polarization, (b) displacement current (at 100Hz) and (c) capacitance vs voltage measurements (1 kHz) at different temperatures for MFS capacitor on p-Ge substrate. The arrows in (b) show the shift of the coercive voltages V_c^+ and V_c^- in depletion/inversion and accumulation, respectively.*

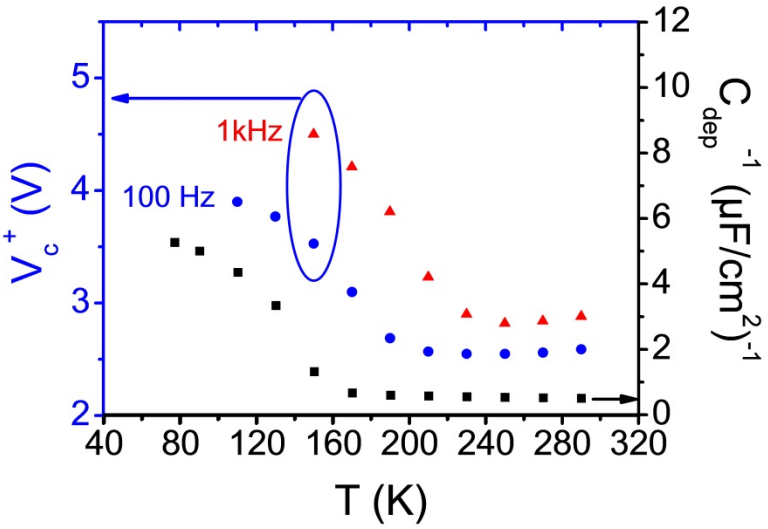

Figure 4: *Temperature dependence of positive coercive voltage V_c^+ at 100 Hz (circles) and 1 kHz (triangles) and inverse capacitance C_{dep}^{-1} (squares) measured at +3.5 V in depletion for p-Ge MFS.*

Figure 4 presents the comparison between inverse total capacitance measured at depletion (+ 3.5 V) C_{dep}^{-1} and V_c^+, as obtained by displacement current measurements at two different frequencies (1 kHz and 100 Hz), at each temperature. Notably, both quantities follow the same trend, which indicates that the origin of the significant V_c^+ increase is the creation of a depletion region in the Ge semiconductor at low temperatures. More specifically, when positive voltage is applied on TiN top electrode at RT, the conduction band is populated, as dictated by the Fermi Dirac distribution, by a large number of electrons (minority carriers), due to low E_g of Ge, resulting in surface inversion (Fig. 5 (a)). Therefore, the free negative charge in inversion screens efficiently the positive polarization charge in such a way that the Ge bottom electrode behaves like a metal, yielding symmetric nearly ideal hysteresis as in MFM capacitors. At low temperatures, the Fermi Dirac distribution narrows so the population of the conduction band by minority carriers is diminished, while majority carriers are repelled from the interface (Fig. 5b). Therefore, the region near the interface is depleted from free carriers so the electric field penetrates the semiconductor depletion region causing an additional voltage drop and an associated depolarization field in the ferroelectric. This voltage drop explains the larger V_c^+

required to attain the E_c in the HZO ferroelectric. In contrast, in accumulation at negative bias, the majority carrier concentration (holes) is not affected at lower temperatures, so V_c^- remains nearly the same. Similar description holds for n-type substrates where the role of V_c^+ and V_c^- is interchanged.

As already mentioned above, the effect of the depletion at low temperatures is more pronounced at higher frequencies of measurement. This is understood as follows: the few minority carriers do not respond fast enough to the electric field since electron-hole generation by interband transitions, typically mediated by mid-gap states near the interface, is a slow process. As a result, the inversion layer does not easily form at high frequencies, leaving the interface depleted from free carriers. The frequency effect could be mitigated or avoided by using highly doped substrates which show metallic behavior so the hysteresis remains near ideal at high frequency even at low temperatures (see n^+ Ge MFS in Fig. 2a).

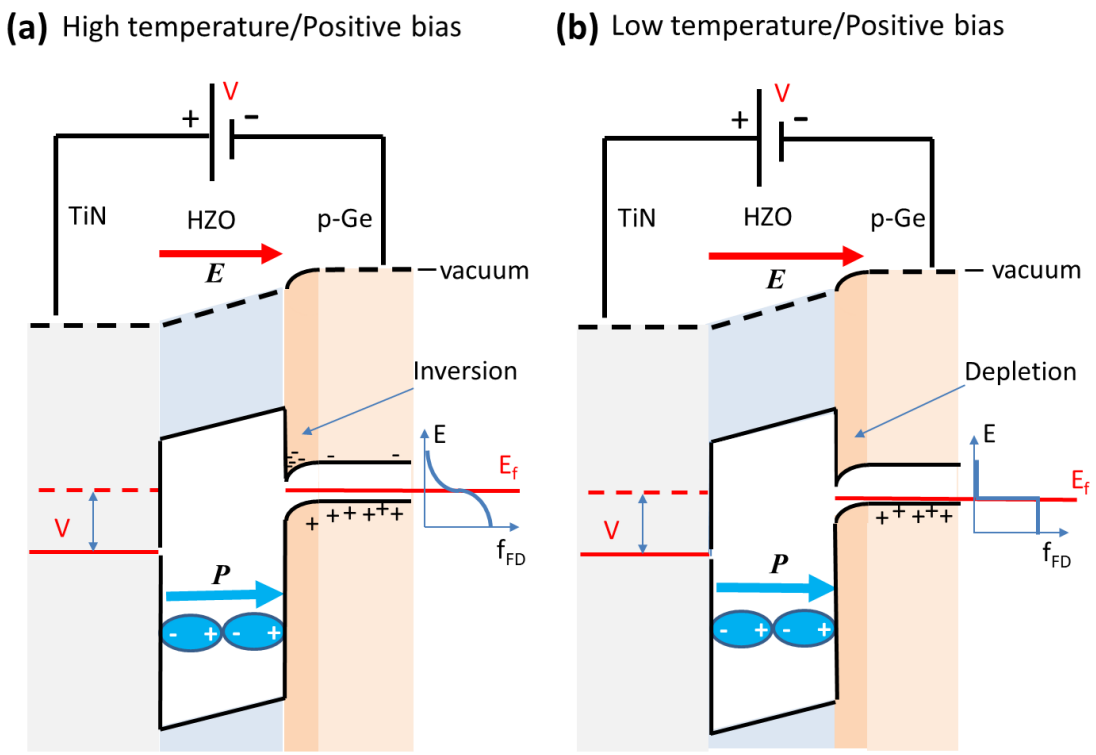

Figure 5: *Schematic energy band diagrams of TiN/HZO/p-Ge device layer structure corresponding to high frequency measurements at positive applied bias V at (a) high*

temperature (inversion), (b) low temperature (depletion). ***E*** *denotes the electric field vector which is largely confined in the HZO ferroelectric except in (b) where it penetrates the Ge depletion region giving rise to an additional voltage drop.* ***P*** *denotes the polarization vector in the ferroelectric.* f_{FD} *vs E is a schematic illustration of the Fermi Dirac distribution.*

3.3 Depletion induced depolarization field

For a quantitative analysis, the variation of V_c with the inverse total capacitance C per unit area at depletion is calculated as follows: The free charge per unit area Q_c stored in the capacitor can be expressed as $Q_c=CV_c$. On the other hand, from Gauss's law, $Q_c=D=\varepsilon_{FE}E_{FE}$, where D is the electric displacement, ε_{FE} is the dielectric constant and $E_{FE}=E_c+E_{dep}$ is the total electric field in the ferroelectric expressed as the sum of the E_c and the depolarization field E_{dep}. Then,

$$V_c = \varepsilon_{FE} C^{-1}\left(E_c + E_{dep}\right) \qquad (1)$$

which explains the similar behavior exhibited by V_c and C^{-1} in Fig. 4 as a function of temperature.

Equation (1) can be used to extract E_{dep} as a function of temperature from experimental data of V_c and C^{-1} as displayed in Fig. 4. This is particularly useful given that an estimate of E_{dep} is not easy to make. For example, the typically used expression $E_{dep}= -P/\varepsilon_{FE}(1+C_s/C_{FE})$ [27] for the depolarization field requires the knowledge of the semiconductor capacitance C_s which is not easy to extract experimentally (P is the remanent polarization and C_{FE} is the ferroelectric capacitance).

In order to extract E_{dep} from eqn (1), $\varepsilon_{FE}=\varepsilon_0\cdot\varepsilon_r$ is estimated from the accumulation capacitance C_{acc}=1.94 μF/cm^2 at -3 V (Fig. 3 (c)) and the ferroelectric thickness d_{FE}=12 nm using $\varepsilon_{FE}= C_{acc}\cdot d_{FE}=23.3\cdot10^{-11}$ F/m. This calculation yields a relative dielectric constant ε_r=26.3, which is in fair agreement with reported [3] values of ~27 for the orthorhombic crystalline phase of HZO. Moreover, E_c in eqn (1) is obtained at each temperature from $E_c= V_c^-/d_{FE}$ by measuring V_c^- in accumulation (negative bias).

The absolute value of E_{dep} as a function of temperature is plotted in Fig. 6 along with E_c for comparison. E_c varies weakly and increases roughly linearly with decreasing temperature following the linear temperature dependence previously predicted [28] on the basis of Ginzbourg-Landau theory [25]. On the other hand, $|E_{dep}|$ is nearly zero at RT which is expected considering the efficient screening of polarization charges and increases slightly as the temperature drops to about 160 K. At lower temperatures, $|E_{dep}|$ increases sharply, essentially following the rapid increase of C^{-1} in Fig. 4 which signifies the formation of a depletion region. At the lowest temperature range, $|E_{dep}|$ reaches high values ~2.2 MV/cm which is comparable to the E_c value of 2.55 MV/cm (Fig. 6).

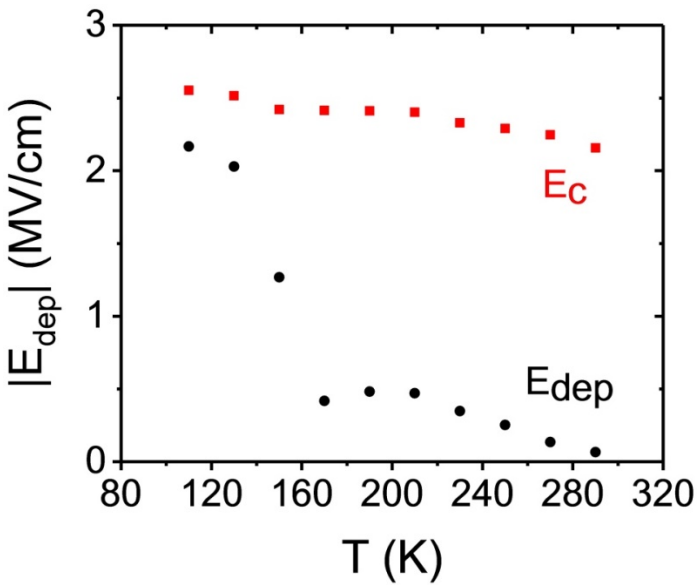

Figure 6: *Temperature dependence of experimentally determined absolute value of the depolarization field E_{dep} and coercive field E_c for p-Ge MFS.*

It should be noted that the formation of an inversion layer (Fig. 5a) may not be a roadblock for FeFET operation since the modulation from inversion to depletion can be controlled by the gate bias turning the transition from ON to OFF state as already demonstrated in the literature [15-17]. Any non-idealities such as low I_{ON}/I_{OFF} ratio may not affect the FeFET operation since the

memory window depends mainly on the threshold voltage shift controlled by the ferroelectric state at the gate.

3.4 Temperature dependence of antiferroelectric-like capacitors

Temperature depended polarization and capacitance measurements were also performed for a device with 5 nm HZO thickness on p-Ge substrate (Fig. 7). The device at RT shows antiferroelectric-like characteristics, related to its low thickness (explained in Chapter 4). By decreasing the temperature, a similar behavior is observed as before; the peaks in I-V curves are shifted to the right, until they are disappeared at 210 K.

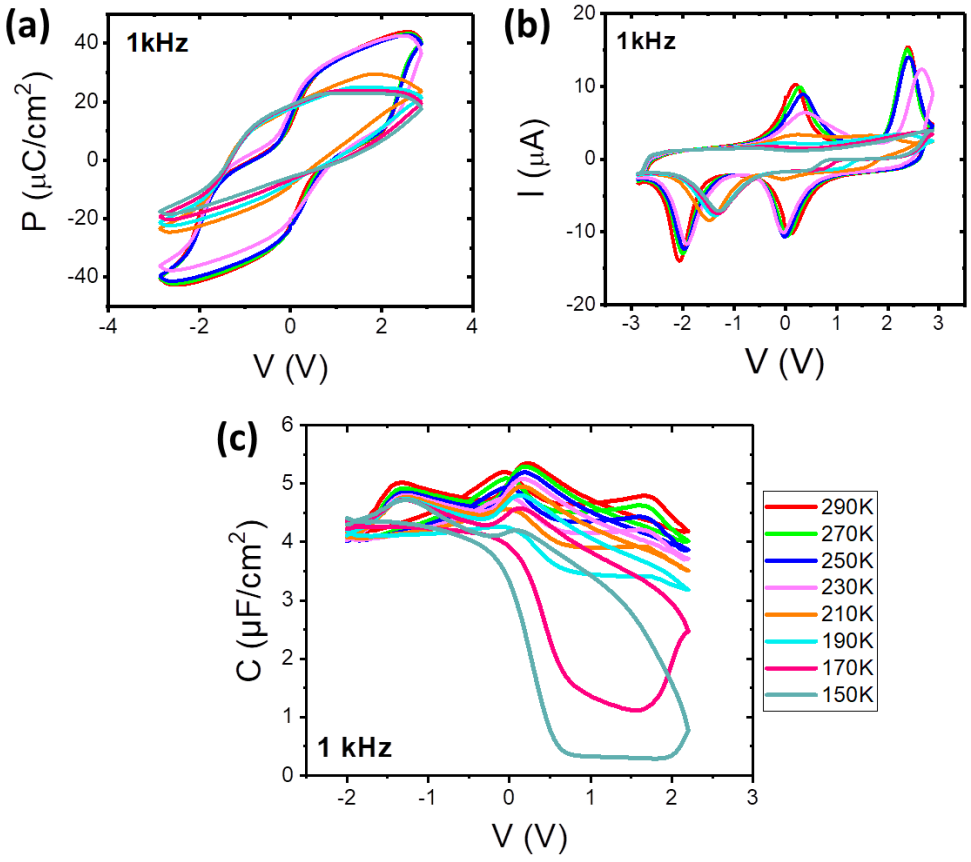

Figure 7: *(a) Polarization, (b) displacement current (at 1 kHz) and (c) capacitance (1 kHz) vs voltage measurements at temperatures in the range of 290 to 150 K for a 5-nm-HZO antiferroelectric-like capacitor on p-Ge substrate.*

As a result, below this temperature P-V loop shows a dielectric behavior for positive voltages and ferroelectricity with one peak at negative voltages. The same effect is depicted in C-V measurements, where the typical 4-peaks antiferroelectric curve is obtained at RT, and it is gradually transited to a p-type MIS capacitor.

3.5 Depletion layer in capacitors on n-type substrates

To test the presence of the depletion regions at low temperatures, C–V measurements were performed in a similar way as for HZO on p-Ge. The recorded C–V characteristics for HZO on n-Ge are shown in Figure 8.

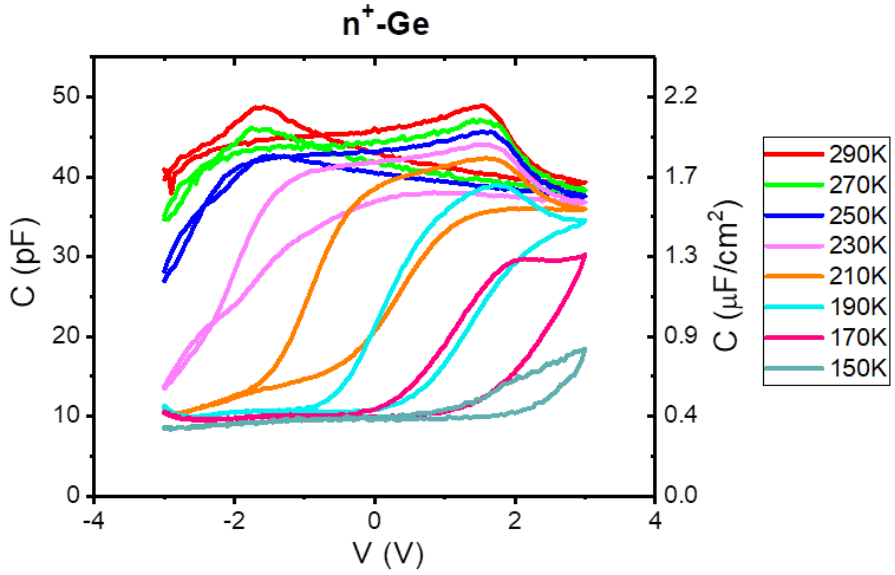

Figure 8: *Capacitance vs voltage measurements (1 kHz) at different temperatures for MFS capacitor on n^+-Ge substrate.*

At the first look, it appears that the behavior of the HZO on n-Ge is similar to that of HZO on p-Ge, meaning that the shape of the C–V characteristic is MFS-like at low temperatures and MFM-like at high temperatures. The similarity is only apparent because there is a striking difference compared to HZO on p-Ge, and this is the fact that the value of capacitance changes for both polarities of the maximum applied voltage. For HZO on p-Ge, the change is significant (from

about 5 pF to about 45 pF) only for positive polarity (depletion), whereas for negative polarity (accumulation), the capacitance value for maximum applied voltage has only a very small variation around the value of 45 pF. In the case of HZO on n-Ge, the capacitance value at maximum applied voltage has a significant increase (about four times) for both polarities as the temperature is increased. Normally, the value for maximum positive voltage (accumulation) should have only a very small variation, as it happens in the case of HZO on p-Ge for negative voltages. The fact that the variation is very large also for positive voltage suggests that the interface properties are not the same for HZO on p-Ge and n-Ge. A possible explanation is that there are interface states that are trapping electrons, building up a negative charge at the interface and forcing the n-Ge substrate in depletion even for positive voltage applied on the top contact.

Analyzing in more detail the C–V characteristics, one can observe a slight shift toward negative voltages. The hysteresis loop is also shifted with about 0.2 V toward negative voltages. This fact supports the presence of an internal electric field, oriented from the top electrode toward the interface. Such a field can be generated by negative charges (electrons) trapped at the interface. In any case, the presence of the internal electric field seems to have almost negligible impact on the polarization hysteresis loop, considering that the remanent polarization for up and down polarization are similar, around 25 $\mu C\ cm^{-2}$.

One can also notice that the capacitance of a MFS structure in accumulation should be equal with the capacitance of the ferroelectric layer, HZO in the present case [29]. This should not change with polarization orientation, and may have a small temperature variation considering that the dielectric constant of a ferroelectric increases with the temperature while approaching the transition from ferroelectric to paraelectric phases. This is the case for HZO on p-Ge, where the capacitance for negative voltages (accumulation) has only a small increase with temperature, from about 44 pF at 80 K to about 46 pF at 300 K. However, for HZO on n-Ge, the increase is from about 11 pF at 80 K to about 40 pF at 300 K, for positive voltages when the n-Ge should be in accumulation. There is no reason to assume that the temperature variation of the dielectric constant is different for HZO deposited on n-Ge compared to HZO deposited on p-

Ge. Such a drastic variation can be explained by the presence of interface traps. At low temperatures, the carriers are trapped and cannot follow the variation of the small amplitude a.c. signal used for capacitance measurements. As the temperature increases, the carriers will be more easily detrapped and can follow the a.c. signal leading to a larger capacitance value.

One can estimate the density of the carriers released from the interface traps by multiplying the capacitance difference of about 30 pF with the voltage of 2.5 V, where this difference was obtained, and dividing with area of the top electrode (2304 μm^2 in the present case). One obtains a density of about $2 \cdot 10^{13}$ cm^{-2} but this is only a very rough estimate and, actually, is underestimated considering that not all traps may be emptied at 350 K.

3.6 Admittance Spectroscopy Measurements

Admittance spectroscopy measurements are performed on 5-nm-HZO p-type Ge MFS for a number of temperatures and for an applied bias of 0.5V (Fig. 9) [30]. At a given frequency which depends on the temperature, the spectra show a peak due to conductance losses originating from charge trapping at interface defect states.

To estimate the trap density D_{it}, we use standard methodology described by Nicolian and Brews [31], according to which the D_{it} is expressed as a function of the maximum conductance G_p as,

$$D_{it} = \frac{1}{S\, q\, f_D} \left(\frac{G_p}{\omega}\right)_{max} \quad (2)$$

where S is the diode's area, q is the electron charge, ω is the frequency of the measurement and the universal function f_D describes the spatial inhomogeneity of band bending over the capacitor area with variance σ_s.

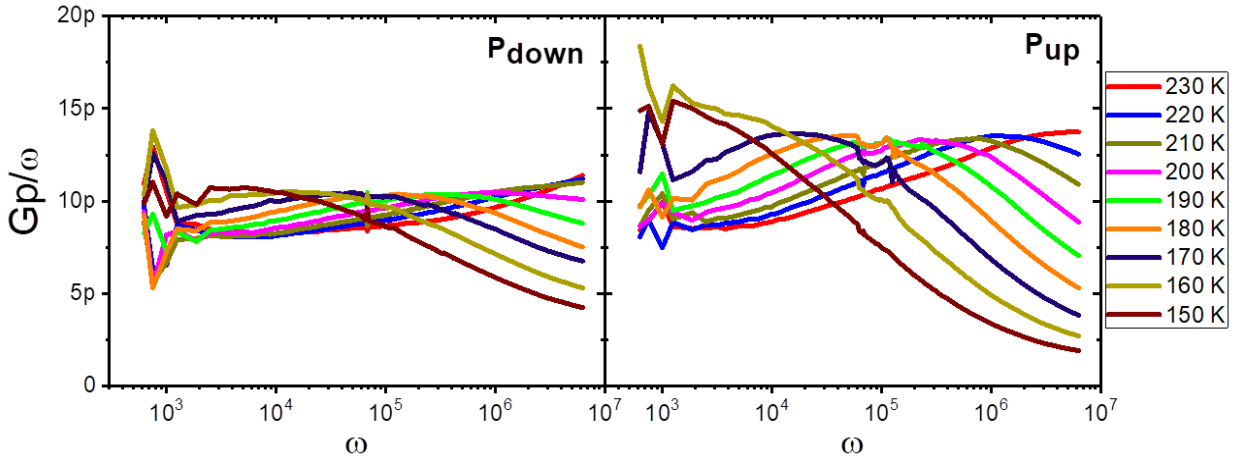

Figure 9: *Admittance measurements at different temperatures for polarization down (left) and polarization up (right).*

f_D shows a weak variation from 0.4 to 0.125 for homogenous (σ_s=0) and highly inhomogeneous (σ_s=5) capacitors, respectively. The D_{it} varies from a minimum value of 0.93 to a maximum 3.56 x 10^{13} $eV^{-1}cm^{-2}$, depending on temperature, degree of inhomogeneity and polarization state (P_{up} or P_{down}). An average D_{it} ~ 1-1.5 x 10^{13} $eV^{-1}cm^{-2}$ is obtained.

Impedance spectroscopy was also performed in n^+-Ge capacitors, by our collaborators Georgia Andra Boni, Cosmin M. Istrate, Ioana Pintilie and Lucian Pintilie (NIMP, Bucharest-Magurele, Romania).

By this study, two interface electrically active defects have been identified in the Ge energy gap. In p-Ge, a shallow donor level is located only 60 meV from the valence band (VB) and in n^+-Ge, an acceptor level is located 200–250 meV from the VB. It is characteristic that the donor level in p-Ge is active only at positive gate bias when the MFS is in depletion, whereas the acceptor level in n-Ge is always active for either positive or negative gate bias. These observations indicate that a pair of acceptor and donor levels, closely spaced in energy, is both located near the top of the VB, consistent with previous observations that the CNL in Ge is close to the VB. In p-Ge, the Fermi level at the interface is close to the CNL leaving the interface neutral, thus the influence of interface defects (traps) on the ferroelectric hysteresis and the C–V is minimum. In contrast, in n^+-type Ge, the Fermi level at the interface is located well above the acceptor level, thus filling the traps with electrons, negatively charging the interface.

3.7 Conclusions

A depletion region, formed at low temperatures, in Ge surface and its effect on ferroelectric characteristics of Ge-MFS capacitors have been studied. Although the present analysis for depolarization field has been performed based on Ge MFS which serves here as a model case study, the expression (1) is of general validity and holds for other semiconductor devices including Si MF(I)S, albeit with an additional complication in the analysis due to the presence of the insulating (I) layer. However, in the case of Si MF(I)S, due to the larger E_g of Si (~ 1.1 eV), a depletion layer and an associated finite E_{dep} are expected at RT, adversely affecting the P-E characteristics which show subloop behavior and increased operation voltages, as previously reported [11, 12, 24]. Therefore, compared to Si devices, Ge MFS offer advantages: The absence of an insulating interfacial layer and the low E_g of Ge which prevents depletion, make depolarization fields insignificant at RT. This allows a symmetric and robust P-E hysteresis loop of Ge MFS at RT with effectively zero E_{dep}, which is essential for FeFET performance at low voltages with improved reliability. Also, the different interface defect states in p and n type Ge have been studied and two interface electrically active defects have been identified in the Ge energy gap. The above study resulted in journal publications [32, 33].

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Chapter 4

Reliability aspects of ferroelectric capacitors

4.1 Introduction

The discovery of ferroelectricity in Si-compatible, HfO_2-based oxides [1] and the recent progress [2] in scaling the ferroelectric (FE) Zr-doped HfO_2 down to 1 nm, has ignited an immense interest of the scientific and engineering community to exploit these materials for the fabrication of low power embedded non-volatile memories (NVM) [3, 4]. Successful integration with CMOS of FeRAM comprising 1C-1T metal-ferroelectric-metal (MFM) capacitors with FE $Hf_{0.5}Zr_{0.5}O_2$ (HZO) has been demonstrated [5, 6].

Beyond MFM, the metal-ferroelectric-semiconductor (MFS) structures can be used for the fabrication of FE field effect transistors (FeFET) with applications in neuromorphic technologies [7-10], negative capacitance FET [11, 12] for low power logic and ferroelectric tunnel junctions (FTJ) NVM [13] with enhanced tunneling electroresistance.

Ge semiconductor could be a good choice for MFS since it is fully compatible with Si and, according to the recent IRDS update 2020 [14], it is considered as one of the channel material technology inflections for future nodes beyond the year 2028. Moreover, the dopant activation in Ge varies between 550 and 700 ^oC, therefore it is compatible with the HZO crystallization annealing, which also varies in the same temperature range, thus enabling Ge FeFETs processing in the preferred “gate first” flow. The importance of Ge has already been recognized [15] and a number of advanced devices such as Ge nanowire FET [10], NCFET [12] and FTJs [16] have been demonstrated.

An advantage of Ge is that it forms clean interfaces with HZO without an interfacial layer as evidenced in a number of earlier [17, 18] and more recent works [19-21]. This could mitigate [22] or totally alleviate some of the reliability problems [3, 23] such as endurance, imprint and wake-up behavior which are associated with the presence of non-ferroelectric (dead) layers at the HZO/semiconductor interface. A big concern is imprint [3, 23], that is a shift over time of the hysteresis loop along the voltage axis and is already present at room temperature resulting in retention loss. An equally important problem is the constricted (pinched) hysteresis loops [3, 23] typically obtained in pristine devices. Such devices need extensive cycling to open the loop (“wake-up”) which jeopardizes the performance of NVM. The origin and the possible

correlation between imprint and wake-up effects are not known yet in detail [24-31]. Here, we deepen our understanding of the mechanism driving imprint and wake-up effects in HZO Ge MFS. Then, we show that depending on the crystallization annealing method, either wake-up and imprint effects can be minimized or leakage current and endurance can be improved, making Ge MFS a prospective candidate for future NVM technologies.

4.2 Study of the reliability issues: wake-up, endurance and imprint

The device layer structure consists of 15 nm HZO/10 nm TiN grown on p-type (0.03-0.07 Ω·cm) Ge (100) substrate by plasma assisted atomic oxygen deposition in a ultra-high vacuum (UHV) system dedicated to molecular beam epitaxy (MBE) of oxides. HZO is grown amorphous at 120 ^{o}C.

The grown structures are cut in two pieces, then crystallization annealing is performed using two different methods: A two stage rapid thermal annealing (RTA) is performed on one piece with a 550 ^{o}C preheating for 30 sec followed by a second RTA step at 750 ^{o}C for 20 sec (150 ^{o}C/sec), then finished by a rapid cooling (85 ^{o}C/sec). The preheating is found to reduce the leakage current and improve the P-V characteristics. A millisecond flash annealing (FLA) is performed on the second piece: a preheat at 375 ^{o}C (previous study [32] shows that the 120 s pre-heat only is not sufficient to crystallize HZO) is followed by an energy flash of 70 J/cm^2. 50x50 μm^2 capacitors are then processed by optical lithography and lift off using Ti/Pt as the metal electrode, followed by TiN etching using a $NH_4OH/H_2O_2/H_2O$ solution, to define the capacitor areas.

Figure 1 shows the grazing incidence X-ray diffraction analysis of as-deposited (pink curve) and after FLA (black curve) films. The exponential background is subtracted. The as-deposited films are amorphous, while after FLA the HZO films are polycrystalline, and show a sharp diffraction peak centered at 2θ-ω = 30.52˚, characteristic of the pure FE orthorhombic phase or the tetragonal phase. No additional peaks are observed at ~28.3° nor at ~31.3°, indicating that no monoclinic phase has formed.

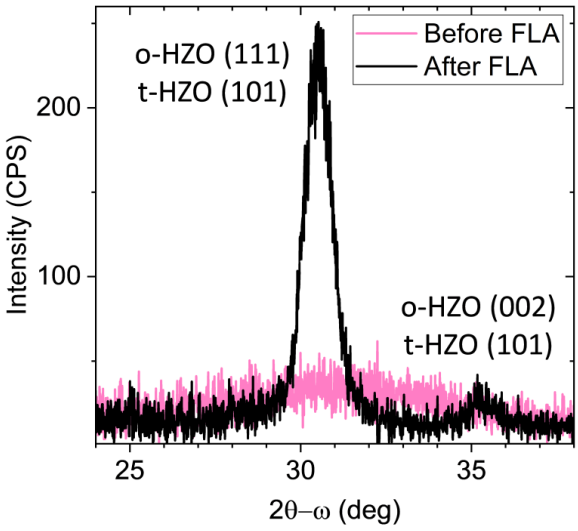

Figure 1: *GIXRD spectra before (pink) and after (black) FLA. ω is set to 0.37 deg and the exponential background is subtracted.*

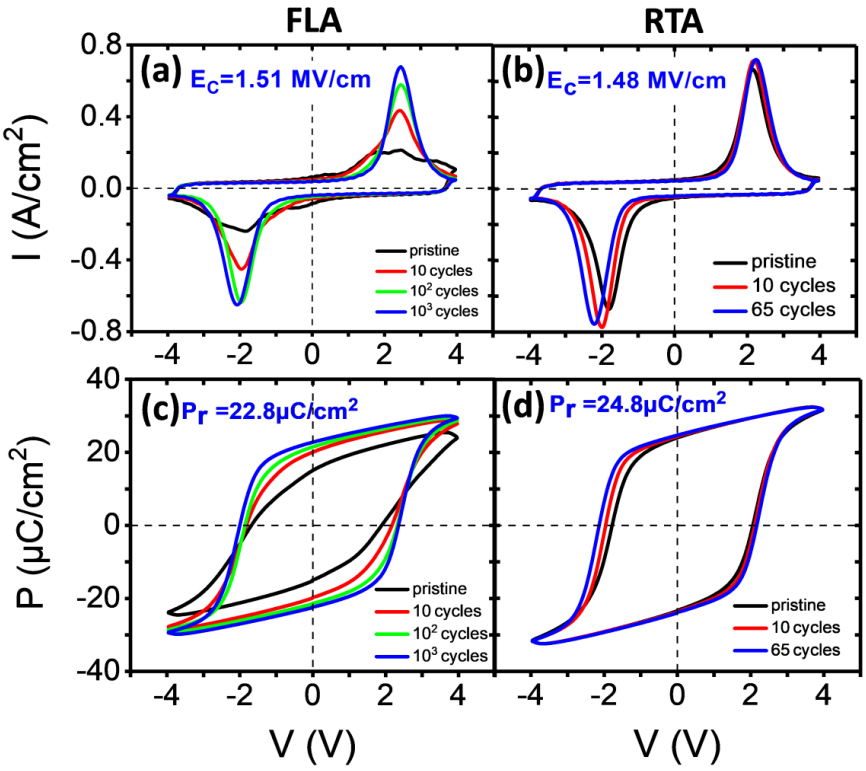

Figure 2: *Pristine and waked-up ferroelectric hysteresis loops obtained at 1kHz. Displacement current density (I-V) for FLA (a) aznd RTA (b) and polarization (P-V) for FLA (c) and RTA (d).*

Typical displacement current density (I-V) and polarization (P-V) hysteresis loops for RTA and FLA-annealed capacitors are shown in Figure 2 for comparison. It can be inferred that the RTA capacitors have weak or no wake-up effects since the pristine curve does not differ much from the fully open hysteresis loop after 65 cycles (Fig. 2(b), (d)). On the contrary, the FLA samples show a pristine P-V hysteresis curve which is slightly constricted and recovers to a fully open P-V characteristic only after 1000 cycles (Fig. 2(a), (c)).

After wake-up, the FLA is comparable to the RTA P-V curve albeit with a slightly lower P_r and slightly larger coercive field E_c. Moreover, pulsed measurements using the Positive Up Negative Down pulse sequence (as described in Chapter 2) is used to determine the parasitic polarization (Fig. 3). It is observed that the FLA capacitors show low parasitic polarization in both positive and negative bias. On the other hand RTA capacitors show larger parasitic polarization in the negative bias mainly due to excessive leakage when the capacitance is biased in accumulation.

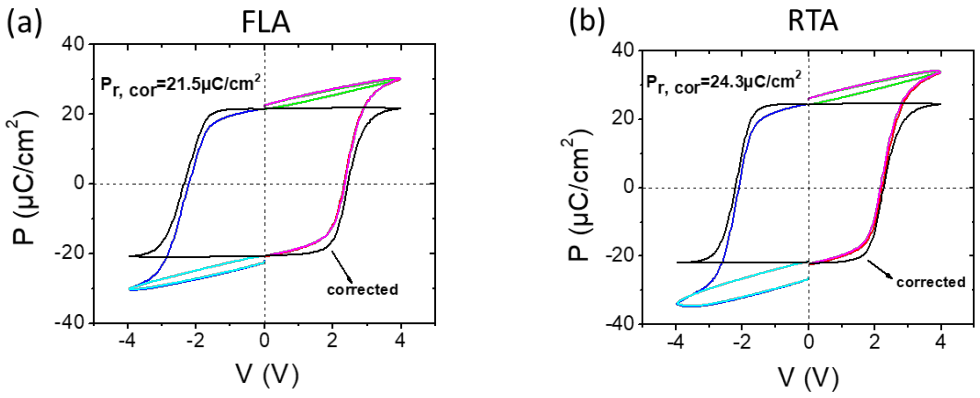

Figure 3: *PUND measurements for (a) FLA, (b) RTA capacitors.*

To be noted that an important factor that determines the pristine state (fully open or pinched) is the annealing temperature. A sample was cut in three pieces and each one was treated by a different RTA process for comparison; 1. at 550°C for 30 sec, 2. at 650°C for 30 sec and 3. the two-stage-annealing at 550 and 750 °C studied here (Fig. 4). The capacitors annealed at 550 and 650°C showed pinched P-V loops in the pristine state and required cycling to wake-up. On the other hand, the third RTA process resulted in wake-up free ferroelectric devices, and this is why they were preferred for this study.

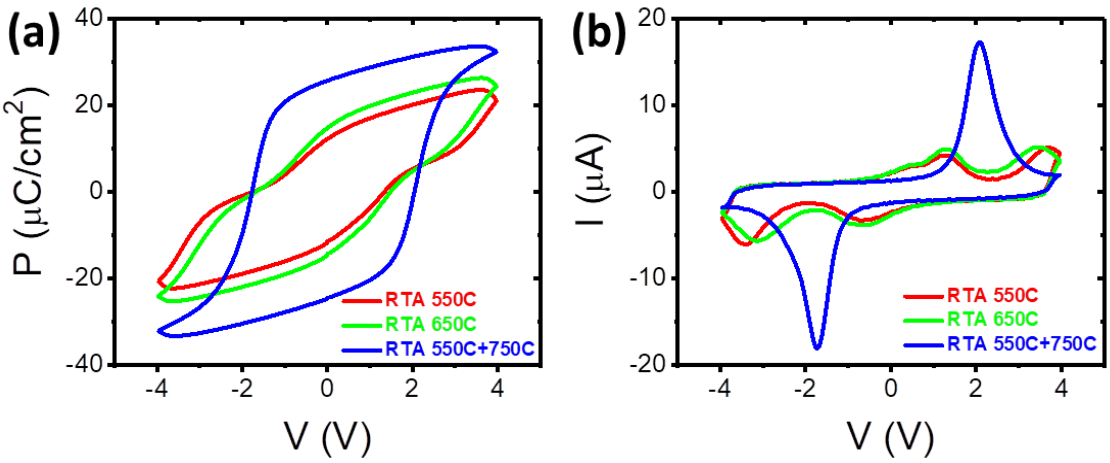

Figure 4: *(a) Polarization and (b) displacement current vs voltage pristine loops for devices annealed at three different temperatures.*

The wake-up effects in films annealed at lower temperatures or by FLA can be explained by several mechanisms, all related to the presence of oxygen vacancies at the interfaces between HZO and the electrodes, rather than in the bulk. First, the redistribution of oxygen vacancies [25, 28] during cycling can lead to depinning of FE domains [28]. Second, the vacancies could induce transformation of eventual tetragonal grains to the orthorhombic phase [23, 26, 27]. Note that a transformation from the monoclinic to the orthorhombic phase, here, is excluded (see the absence of monoclinic grains in the XRD in Fig. 1). Finally, electron trapping into deep states at oxygen vacancies [29, 31], causing local imprint fields [29] which pinch the ferroelectric domains, are considered to be the most probable cause for wake-up. Further, such fields are discussed in more detail below in connection to imprint behavior.

The DC leakage current density and the fatigue/endurance of the RTA and FLA capacitors are presented for comparison in Fig. 5. Before and after wake-up, the FLA capacitors clearly have a lower leakage current compared to RTA capacitors (Fig. 5(a)). After wake up, the leakage of the FLA capacitors increases but it remains an order of magnitude lower than for the RTA ones. It is considered [33, 34] that oxygen vacancies at the grain or domain wall boundaries in the bulk of HZO are the main cause of DC leakage currents. Given that oxygen vacancies are likely to occur primarily at the top TiN/HZO interface [35], it is anticipated that the short (ms) flash annealing

time is not sufficient to induce vacancy diffusion in the bulk, thus resulting in less leakage. Nevertheless, the possibility that the observed leakage differences partly originate from the different microstructures likely present in RTA and FLA capacitors cannot be excluded.

It can be inferred from Fig. 5(b) that the FLA capacitors have a better endurance of up to 2 x10^5 cycles compared to the RTA ones which break after 6 x10^4 cycles. Increased endurance in the FLA sample is probably due to less leakage (Fig. 5(a)) which is known to be the main reason for breakdown [23]. It is anticipated that the higher leakage induces more easily conducting paths after some cycling so the ferroelectric in RTA capacitors breaks faster (in less cycles), effectively becoming a resistor. As an alternative explanation it should be noted that the P_r in the FLA samples is lower, favoring a larger endurance. This behavior follows a trend already reported in the literature [23], according to which endurance increases with decreasing P_r.

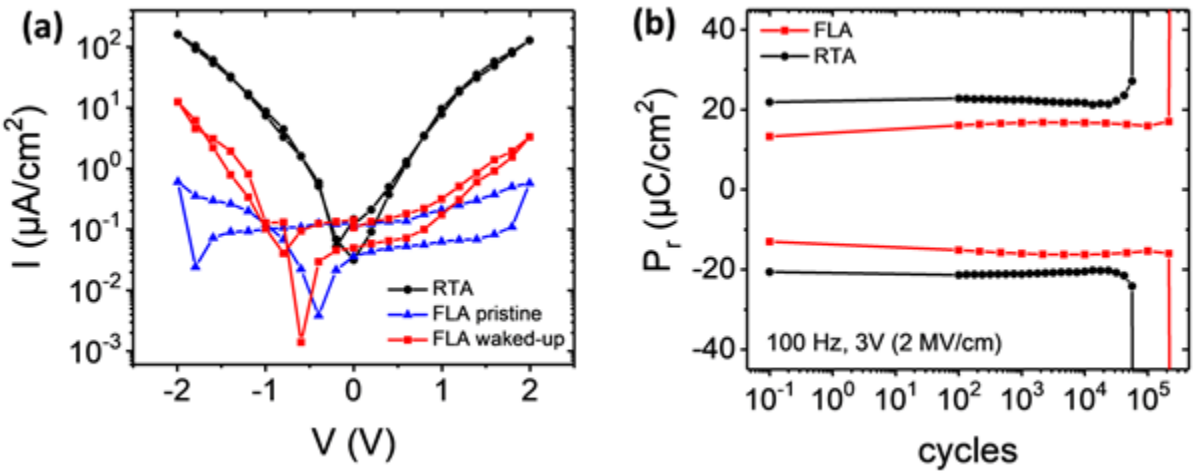

Figure 5: *(a) DC leakage current density (I-V) of RTA and FLA before and after the wake-up. (b) Fatigue/endurance measurements of RTA and FLA capacitors.*

Retention of programmed (stored) polarization states is mainly affected by depolarization mechanisms (e.g. depolarizing electric fields) and by imprint. The latter is thought to be the main cause of retention loss especially for the opposite state (the state opposite to the programmed one) [3].

One of the imprint scenarios [31, 36] is schematically illustrated in Fig. 6 and a phenomenological description is given below. The imprint is primarily due to the insufficient screening of polarization charges by the free carriers in the metal which creates depolarizing electric fields (E_{dep}) [37] inside the FE and electric fields E_d at the interfacial dielectric (dead) layer (Fig. 6(a), (c)). Without losing generality in our case, a TiO_xN_y dead layer is formed [29] by reaction at the top HZO/TiN interface, associated with a reduction of HZO by Ti, yielding interfacial oxygen vacancy defects. The dead layer acts as a tunneling barrier, regulating the trapping (P_{UP}) and detrapping (P_{DOWN}) of charges at interfacial defects.

It should be noted that in our MFS structure, the bottom electrode is the Ge semiconductor which forms a clean interface with HZO [19-21], as already mentioned. The absence of an interface dead layer makes the screening of the polarization charges more efficient reducing the depolarization field. Due to finite screening length in Ge semiconductor, the screening of polarization charges by the Ge free carriers is not as efficient as with a TiN metal (in the ideal case of a clean TiN/HZO interface) or with any other metal. However, Ge, unlike other larger gap semiconductors, is benefited from a large concentration of free carriers, thermally excited across the small band gap at room temperature, which facilitates the screening of polarization charges [21].

The built-in fields redistribute mobile charges over time, screen the polarization charges and establish internal imprint fields E_{imp} in the same direction as the polarization vector, thus stabilizing the stored state (Fig. 6(b), (d)). As a consequence, a larger bias is required to first screen E_{imp} before switching the polarization to the opposite state, manifesting imprint as an increase in V_c (or E_c). The charge redistribution mechanisms can be classified in two main categories. First, the bulk limited conduction [38] in the FE (Pool-Frenkel (P-F), trap assisted tunneling (TA), ohmic conduction etc.) under the influence of E_{dep}. Second, the electrode-controlled charge injection by direct tunneling through the interfacial potential barrier [38], associated with charge trapping/detrapping at the interfacial defects.

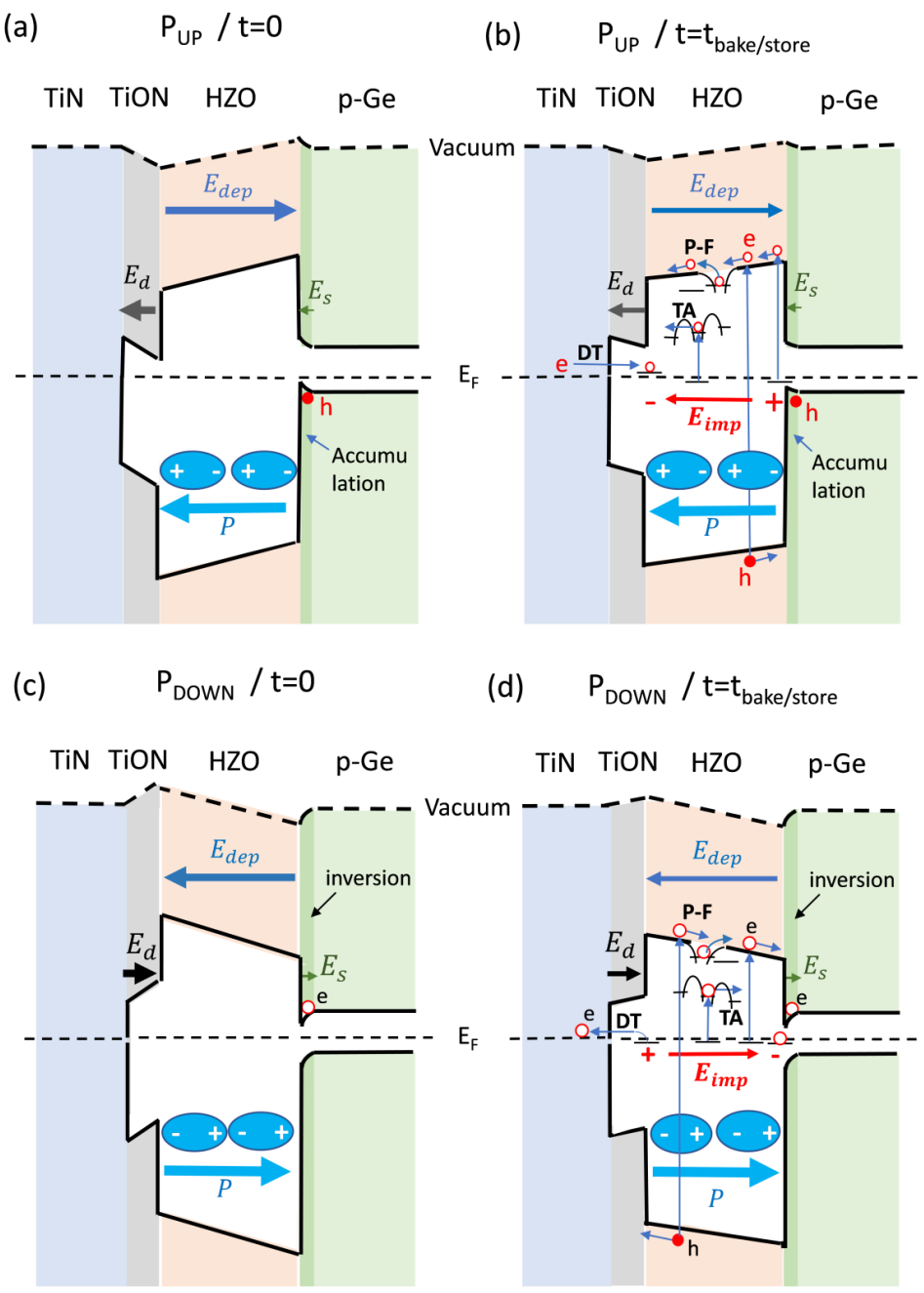

Figure 6: *Schematic illustration of charge redistribution giving rise to imprint field E_{imp}. (a) and (b) correspond to polarization up state immediately after writing and after a finite store time, respectively. (c) and (d) correspond to polarization down state. t denotes the time elapsed after the ferroelectric is poled in the UP or DOWN polarization state. P is the polarization vector and E_{imp} is the imprint electric field. E_{dep}, E_d and E_s are the depolarizing electric field, the electric field*

across the dielectric dead layer at the top interface, and the surface electric field in the semiconductor, respectively. P-F mark the Pool-Frenkel transport and TA mark conduction in the ferroelectric through trap assisted tunneling. DT denotes direct tunneling through the interfacial barrier.

Finally, it is noted that most of the bulk conduction methods (P-F, TA) involve electron transport via defect states in the gap of HZO and at energies which are much higher than the Fermi level (Fig.6(b), (d)). Therefore, bulk conduction mechanisms are thermally activated and at relatively low temperatures of the experiment (25-125 ^{o}C), the number of thermally excited carriers is small and the generation of imprint field over time is expected to be very slow processes. On the contrary, the electrode-controlled carrier exchange at the electrode/HZO interface is a temperature independent direct tunneling (DT) process and is expected to be very fast and efficient in building up the imprint fields. It should be mentioned that interface dangling bond states at the Ge/HZO interfaces could contribute as any other bulk state. More specifically, carriers trapped at the interface states could be thermally excited to the conduction band or to other defect levels inside the HZO gap, subsequently following the bulk-limited conduction mechanisms as illustrated in Fig. 6, contributing to imprint in longer time scales.

Alternative mechanisms as a source of imprint, involving oxygen vacancy diffusion [25, 28] among others, have also been proposed in the past.

Imprint results as well as programming and reading pulses are presented in Figure 7. The capacitors are programmed in the down (P vector pointing towards Ge) or up polarization state by applying positive or negative pulses on the gate, respectively. Subsequently, the capacitors are baked on the manipulator stage with no bias on the gate and at different temperatures in vacuum for a certain storage/bake time. Then they are measured at the same temperature (no cooling to RT) by applying a positive/negative triangular read pulse sequence (see Fig. 7(a)).

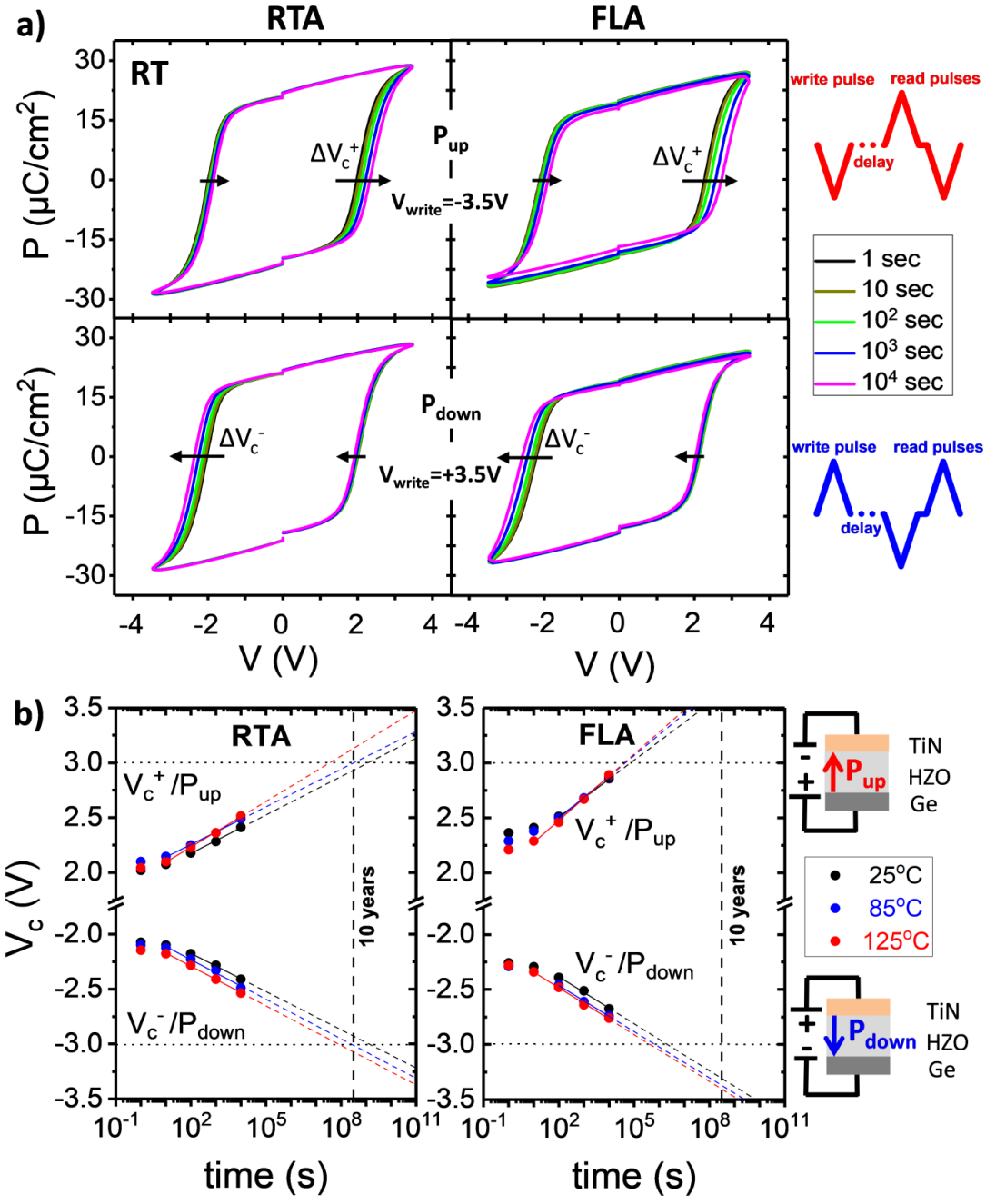

Figure 7: *(a) Hysteresis loops of RTA and FLA capacitors at room temperature (RT) showing the coercive voltage shifts ΔV_c^+ and ΔV_c^- indicated by arrows. The schematic on the right side shows the programming and reading pulses (rise time 1ms). (b) The V_c variation as a function of storage time t for different temperatures. The dashed lines are projections in time of the V_c^+, V_c^- variations. The schematics on the right side show the P_{UP} and P_{DOWN} configurations.*

After the storage/bake time of 10^4 sec, in both cases but more notably in the case of RTA, only the coercive voltages corresponding to the polarization-switching from the programmed to the opposite state shows a shift of ΔV_c^+~ 0.39-0.47 V for P_{UP} and ΔV_c^- ~0.34-0.39 V for P_{DOWN}. This is in line with the phenomenological description given above. The other coercive voltage from the opposite state to the initially programmed one shows negligible variation. This is understood as follows [39]: the first read (switching) pulse is sufficient to partially de-age the HZO, so the second read (switching) pulse reverses the polarization at the expected V_c. The fast de-aging with just one switching pulse is consistent with the notion of fast carrier exchange between TiN and HZO at the top interface (Fig. 6(b), (d)) as the main origin of imprint. At the relatively low experiment temperatures (25-175 ^oC), slower processes involving bulk charge conduction or possible oxygen vacancy diffusion [28], would require a longer de-aging with a larger number of switching pulses (cycling), which is not the case here. Such processes are expected to be thermally activated with a large activation barrier. However, in our case a weak temperature dependence is observed (Fig. 7(b)), further supporting the suggestion that temperature independent direct tunneling at the top interface controls the formation of imprint fields.

In the case of the FLA capacitors, a larger imprint of ΔV_c^+ ~0.49-0.68 V for P_{UP} and ΔV_c^- ~0.42-0.48 for P_{DOWN} is observed. It is possible that FLA results in larger concentration of oxygen vacancies at the interfaces and/or thinner TiO_xN_y barriers, facilitating the formation of imprint fields due to more efficient trapping/detrapping. To better understand the difference between the RTA and FLA, we consider the following. During RTA, the oxygen vacancies diffuse in the bulk, as opposed to the case of ultrafast (ms) FLA where most of the vacancies remain at the interface thereby enhancing the imprint. It is interesting to note that FLA capacitors also show larger wake-up effects (see Fig. 2), pointing to a possible correlation between the two effects (imprint and wake-up) as previously suggested [23, 29]. Both have their origin to the inhomogeneous distribution of oxygen vacancies with a preferred accumulation at the top interface.

It is also inferred from Fig. 7 (b) that the P_{UP} imprint is larger compared to P_{DOWN} imprint. This difference between P_{UP} and P_{DOWN} is more pronounced for FLA capacitors. Similar asymmetries

have been reported [40] for Si MFS with poly Si top electrode. This observation of larger P_{UP} imprint is related to the asymmetry between trapping and detrapping efficiency which is, in turn, a consequence of the electrode asymmetry. The bottom Ge electrode has the same screening efficiency in both polarizations (accumulation and inversion) due to a clean interface, hence it plays a minor role. On the other hand, the interface TiO_xN_y dielectric barrier at the top electrode is important since it regulates the trapping (P_{UP}) and detrapping (P_{DOWN}) of charges at interfacial defects. As seen from Fig. 6, trapping (carrier injection) occurs during P_{UP} (Fig. 6(a)) by tunneling through a smaller barrier compared to detrapping during P_{DOWN} (Fig. 6(b)). Thus, in the P_{UP} configuration, the top interface allows for a more efficient screening of polarization charges and thereby helps establishing larger imprint fields. It should be noted that in the case of an MFM structure there is a symmetry between top and bottom interfaces so a symmetric imprint for the P_{UP} and P_{DOWN} polarizations is expected.

The observed imprint, especially for RTA capacitors, is better than that observed in several ALD deposited Al:HfO_2 [40] Si MFS and (La-doped) HZO MFM [30, 31, 41]. Our thick (15nm) HZO are also comparable to the best reported [29] in the literature for MFM with thin (7nm) ALD HZO. The good imprint results obtained in our films are primarily attributed to the clean Ge/HZO bottom interface. This fact, combined with the abundancy of free carriers in the low gap Ge [21], allow the effective screening of the polarization charges. The rather weak imprint, primarily in the RTA capacitors, may also be due to the particular growth methodology of HZO and TiN. The use of reactive atomic oxygen and nitrogen results in efficient oxidation and nitridation, thus minimizing the oxygen vacancies at the interface.

Setting the criterion for failure to V_c^+/V_c^- not exceeding +/-3.5 V (the write voltage), it is inferred from the projections in Fig. 7(b) that RTA capacitors are not expected to fail before 10 years which is a figure of merit for reliability. Even with a stricter criterion for failure at only +/-3 V, the RTA capacitors comply with the 10-year limit, although marginally. FLA capacitors on the other hand, cannot meet the same standards of reliability (they are predicted to fail before 10 years) due to a slightly larger coercive voltage in the pristine state and a larger imprint.

4.3 Wake-up and polarization back-switching with thickness scaling

Typical capacitors with HZO thickness 10-15 nm show very weak or no wake-up effects. As shown in Fig. 8 (a, d), hysteresis loop of a 15-nm-thick device is already robust and functional in the pristine state. However, going to lower thicknesses ~5nm, pristine loops show pinched characteristics and a number of cycles are needed to wake them up (Fig. 8 (b, e)). Especially for films with higher Zr/Hf ratios, this effect is more severe, having an AFE-like behavior that is rather unaffected by cycling (Fig. 8 (c, f)).

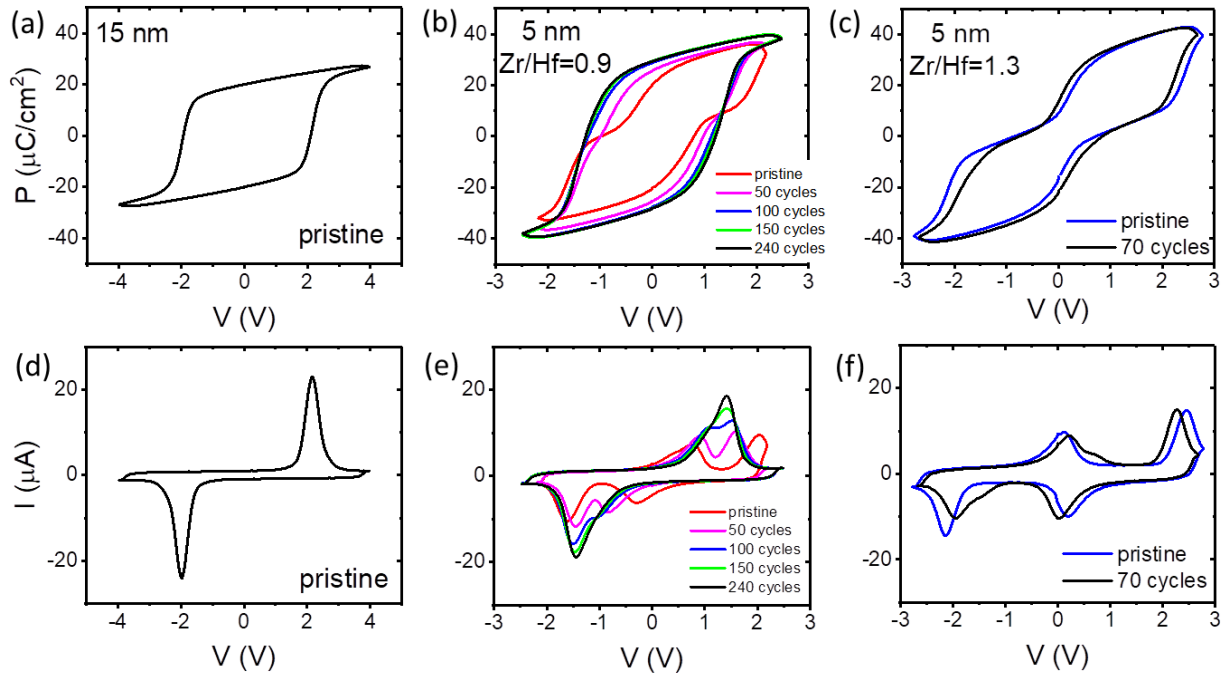

Figure 8: *Polarization and displacement current hysteresis loops before and after cycling for (a), (d) 15 nm HZO, (b), (e) 5 nm HZO and Zr/Hf=0.9 and (c), (f) 5 nm HZO and Zr/Hf=1.3, respectively.*

Various mechanisms have been proposed in the literature about the pinched loops and the wake-up, which is typical in these materials and critical for the operation of the devices [3, 23, 42]. A depolarization field in the ferroelectric layer, arising from unscreened charges and non-ferroelectric interfacial layers, leads to the backswitching of some dipoles. During cycling, charge

injection and trapping at pre-existing interface defects screen the depolarization field stabilizing ferroelectricity.

In order to investigate the evolution of backswitching with time, PUND measurements with increasing delay time from 25 ns to 100 s between the pulses were obtained. Current response to the U and D pulses (second positive/ negative) is expected to correspond to the non-switching contribution from parasitic charges in the interfaces or the HZO bulk, as the ferroelectric is already polarized by the P and N pulses (first positive/ negative). This is what we observe in the thick sample (Fig. 9). The red arrows show the shift of Vc with increasing delay time, effected by the imprint effect.

In the case of 5-nm capacitors, and especially in the pristine state, a part of ferroelectric dipoles are switched again with the U and D pulses, indicating that they were back switched during delay time between the pulses. This back-switching is increased for increasing delay time (Fig. 10). For the waked-up capacitor, this back-switching is slightly present after at least 100 s.

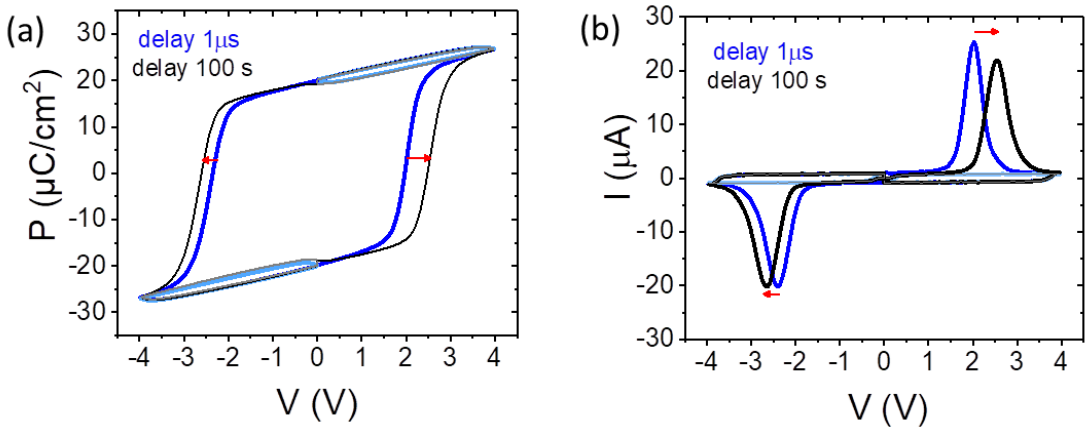

Figure 9: *PUND measurements with delay time between pulses 1 µs (blue curve by switching and light blue by non-switching pulses) and 100 s (black curve by switching and gray by non-switching pulses) for 15 nm thick HZO. The red vectors depict the shift of V_c caused by imprint.*

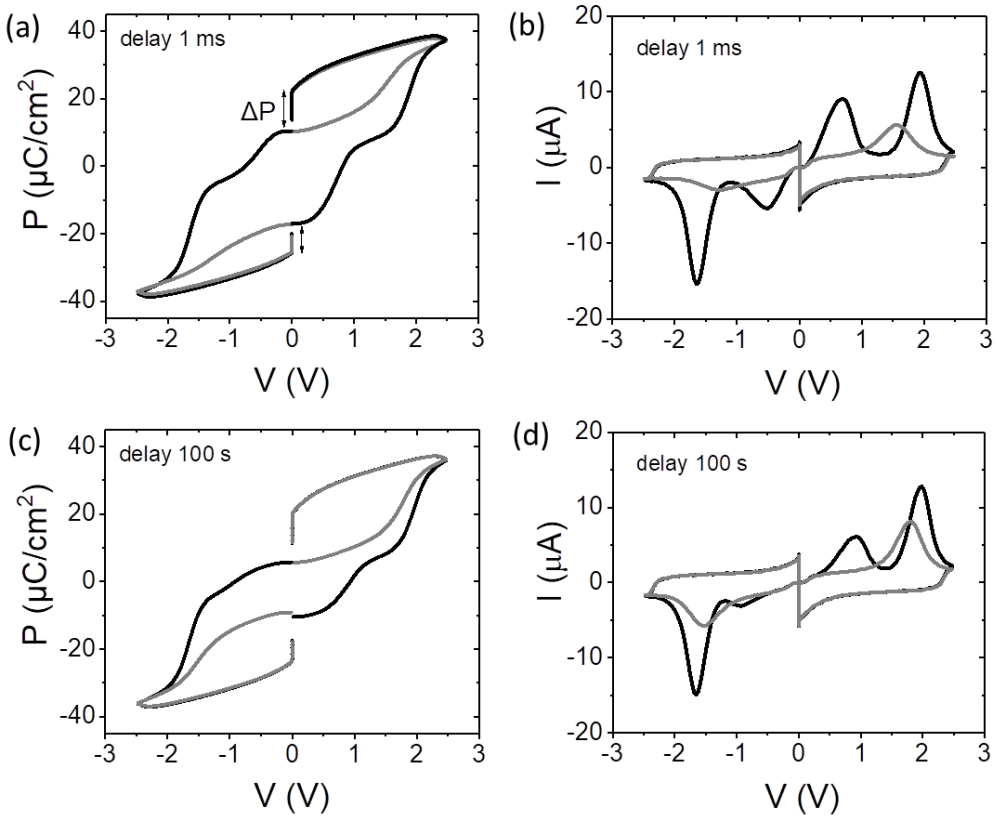

Figure 10: *PUND measurements with delay time (a), (b) 1ms and (c), (d) 100s for a pristine 5-nm-thick capacitor. Black curves were obtained by switching pulses (P-N) and gray curves by non-switching pulses (U-D).*

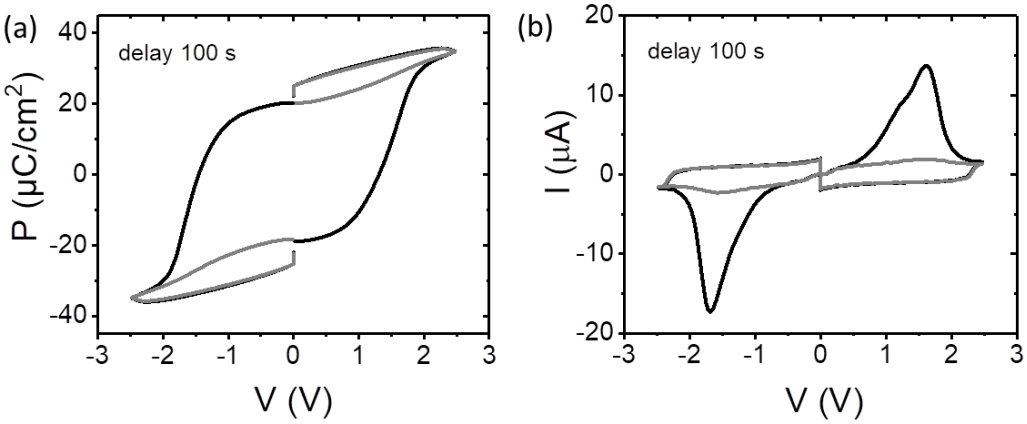

Figure 11: *PUND measurements with delay time 100s for a waked-up 5-nm-thick capacitor. Black curves were obtained by switching pulses (P-N) and gray curves by non-switching pulses (U-D).*

In order to distinguish the back switched charges from the total charges ΔP measured by U and D pulses, we consider that the non-switching parasitic charges ΔP_0 are the same for different HZO thicknesses and constant over time, as observed for the 15-nm capacitor: ΔP_0= 0.92 µC/cm^2 for polarization down (positive applied voltage at the top electrode) and ΔP_0= 1.35 µC/cm^2 for polarization up (negative applied voltage).

Thus, we can quantitatively estimate the time dependent depolarization field causing the back-switching by:

$$|E_{dep}| = (\Delta P - \Delta P_0)/(\varepsilon_0 * \varepsilon_{FE}) \quad (1)$$

where ε_0=8.85·10^{-12} F/m is the vacuum permittivity and ε_{FE} =32 the relative dielectric constant of the orthorhombic HZO.

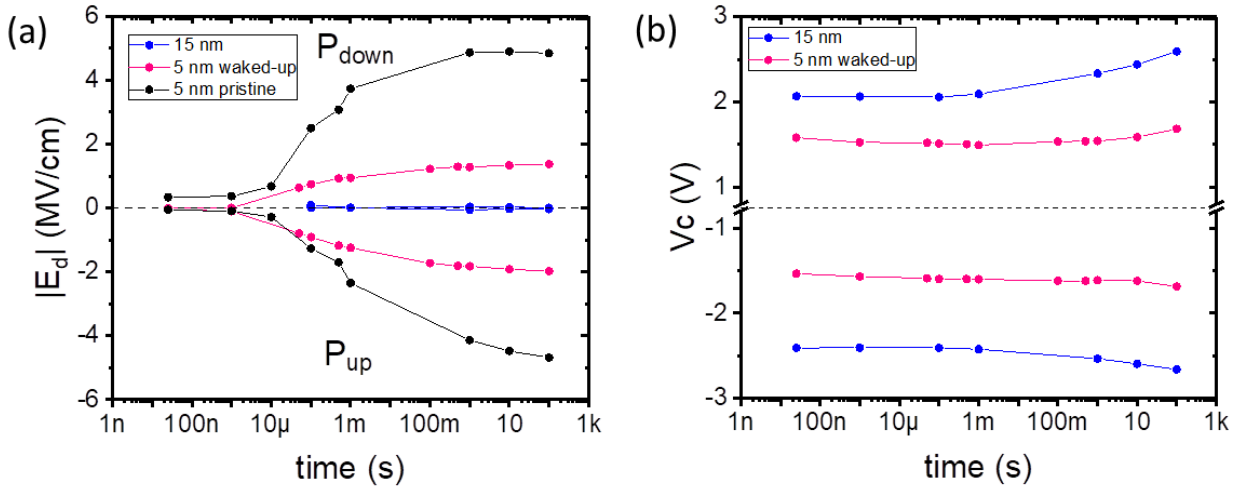

Figure 12: *Depolarization field causing the polarization backswitching and V_c shift (imprint) as a function of time.*

The results are shown in Figure 12 (a). For the 15-nm-thick capacitor E_{dep}=0, as expected. In the case of 5 nm in pristine state, a depolarization field arises after about 10 µs, reaching a maximum value of +4.85 and -4.68 MV/cm after a few seconds. These values are larger than the coercive field (~2.8 MV/cm) and the back-switching of the most part of total polarization results in the pinched characteristics of pristine loops. When the capacitor is waked-up, the depolarization is improved but not totally eliminated, causing a small portion of polarization to

back-switch after a few ms delay time. Nonetheless, E_{dep} remains lower than E_c, letting us obtain an open P-V loop (Figure 11).

On the other hand, the shift of V_c caused by imprint is more severe for the thick HZO, as expected from the higher P_r value, as depicted in Figure 12 (b).

Aiming to achieve FTJs with sufficient TER requires going on even lower thicknesses. A sample with 3 nm HZO (Hf/Zr~2.92) layer was fabricated and after Flash Lamp Annealing, it was crystallized at orthorhombic phase as confirmed by GI-XRD, while the monoclinic phase was not depicted.

The electrical measurements showed evidences of switching peaks in displacement current (Fig. 13), but this behavior was unstable. Below 5 nm, the depolarization field is significantly higher than the coercive field, thus the ferroelectricity is difficult to be stabilized.

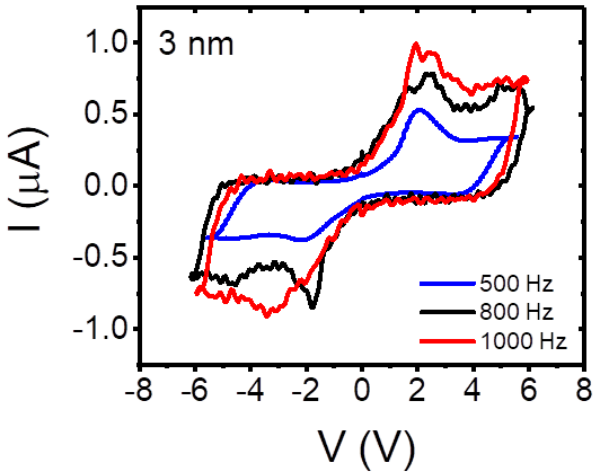

Figure 13: *Displacement current of 3-nm-HZO capacitor at 500, 800 and 1000 Hz.*

Since the effect of reducing the HZO thickness in the depolarization field is inevitable, the improvement or use of different electrodes is required in order to achieve ferroelectricity in sub-5 nm thicknesses.

4.4 Conclusions

In summary, reliability measurements of HZO Ge MFS capacitors show that imprint and wake-up effects are correlated and are influenced by the HZO/TiN plasma assisted atomic oxygen growth methodology as well as the crystallization annealing processing. The behavior of the V_c shifting with time and temperature, indicates that the top TiN/HZO electrode-controlled trapping/detrapping at interfacial oxygen-vacancy defects is the primary source of imprint fields. RTA results in MFS capacitors with very weak wake-up effects and small imprint which are very essential for the operation and reliability of Ge FeFET devices. On the other hand, FLA capacitors show better endurance and improved leakage which makes them suitable for low power applications, where ultrathin HZO is an essential requirement. Finally, it is shown that pinched characteristics become critical for the ferroelectric performance of thickness scaled capacitors below 5 nm. The above study resulted in journal publication [43].

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Chapter 5

Ferroelectric Field Effect Transistors for Non-Volatile Memory applications

5.1 Introduction

Ferroelectric Field-Effect Transistors (FeFETs) show great potential for non-volatile memory (NVM) [1] offering compact 1T memory cells for high integration. The fast operation speed, the inherent internal gain, the large current swing and the non-destructive read capability make FeFETs suitable for low-power NVM. Ferroelectric (FE) hafnia boosted the realization of the FeFET due to its compatibility with CMOS technology and its stable ferroelectricity at reduced thickness ~ 10 nm in-line with technology scaling trends. The hafnia based FeFET NVMs [2] show synaptic plasticity [3, 4] and provide a solution for the implementation of accelerator artificial neural networks for in-memory computing.

Early studies focusing on Si:HfO_2 based FeFETs yielded important results with MW ~1.2 V [5] and I_{on}/I_{off}~10^6 [2]. $Hf_{1-x}Zr_xO_2$ (HZO) further enhanced the FeFET performance due to better ferroelectric and reliability properties [1, 6]. However, there are obstacles in introducing HZO in Si-FeFET technology because HZO cannot sustain the high (>1000^{o}C) temperature of the source (S)/drain (D) dopant activation annealing in Si. Therefore, the preferred gate first, self-aligned junction definition, necessary for manufacturable scaled HZO Si-FeFETs, is difficult. A possible solution to this problem is the use of Ge channels where dopant activation annealing is performed at much lower temperatures (400-600^{o}C) allowing for a gate first definition of transistors with FE HZO gates. In fact, this temperature range is compatible with the crystallization annealing of HZO which is used to obtain the FE orthorhombic phase. Thus the two annealing steps can be performed in just one run simplifying processing flow and avoiding degradation of HZO and source and drain regions that might occur during multiple annealings. The use of Ge has additional benefits which are briefly mentioned here. Ge/HZO forms sharp interfacial oxide-free interfaces, as shown in our previous publications [7, 8] allowing for lower voltage operation of devices, mitigating, in parallel, charge injection and trapping in HZO near the interface. The latter is considered as the main factor that limits the endurance of Si-FeFETs due to a spontaneously formed thin SiO_x or silicate at the interface which sustains a high interfacial electric field under bias, thus accelerating charge injection via field assisted tunneling. In contrast, Ge-FeFETs with sharp Ge/HZO interfaces hold promise for improved reliability. It should be noted however that developing an interfacial oxide-free Ge/HZO FeFET

technology is challenging since the Ge surface needs to remain unpassivated. This has adverse effects on the transistor transfer characteristics since dangling bonds and other interfacial defects can trap charges which limit the channel mobility and degradate the subthreshold transistor characteristics [9]. Therefore, the main target in this work is to develop a Ge-FeFET technology with oxide free interfaces which reconciles the quality of ferroelectric gates with transistor functionality.

Research on Ge-FETs with FE gates is rather limited. Ge FE nanowire FETs as synaptic devices have been demonstrated using a composite Al_2O_3/HZO/Al_2O_3 gate [10]. Moreover, complex TaN/HZO/TaN/HfO_2 gate stack on Ge channel was used for the fabrication of negative capacitance NC-FET, demonstrating the operation with subthreshold slope (SS) values below the thermionic limit [11]. The ferroelectric field-effect in a FE BTO/STO/Ge gate stuck has been confirmed by microwave impedance microscopy [12]. Here we report on a FeFET using only a single FE HZO layer in the gate stack directly in contact with the Ge channel exhibiting a sharp Ge/HZO interface.

Ge/HZO/TiN capacitors fabricated by plasma assisted atomic oxygen deposition in a molecular beam epitaxy (MBE) chamber show robust ferroelectricity with weak wake-up and imprint effects, as presented in our previous works [7, 8, 13]. The wake-up effect is typically explained by redistribution of oxygen vacancies (V_o's) during electric field cycling into the bulk of HZO. In the pristine state these V_o's are mainly concentrated near the defective interfaces, like Ti-O-N or SiO_x interfacial thin layers, giving rise to depolarizing electric fields that oppose to polarization. In our case, due to the absence of a dielectric/dead layer at the bottom electrode, depolarizing fields in pristine HZO are reduced. In addition, Ge, as a low gap semiconductor, has a large concentration of free carriers that facilitates the screening of polarization charges. As a result, the wake-up effect is improved. In this paper we adopt the FE HZO gate to realize Ge p-channel FeFETs. We show that it is possible to reconcile ferroelectricity in HZO with FET operation in devices with interfacial oxide-free Ge/HZO interface. Despite omitting a critical surface passivation layer, necessary to maintain the required sharp HZO/Ge interface, fully

functional Ge-FeFETs with a well-defined memory window (MW) are produced showing the feasibility of our approach.

5.2 Fabrication of Ge-FeFETs

P-channel FeFETs were fabricated by e-beam lithography on n-Ge (ρ=0.01-0.1 Ohm·cm) substrates with different channel lengths from 0.5 to 50 µm and widths from 10 to 200 µm. The gate stack consists of 15-nm thick HZO with composition Zr/Hf=1.17, extracted by in-situ X-ray photoelectron spectroscopy (XPS), and ~8nm TiN deposited in the MBE chamber. Prior to deposition, Ge substrates were annealed at 450^{o}C for 30 min in vacuum to obtain a clean surface free of C and O contaminants. The HZO film was deposited at 120^{o}C by co-evaporating Hf and Zr with rates R_{Hf} ~R_{Zr} ~1/11 Å/sec from two different electron guns in the presence of reactive atomic oxygen generated by a remote rf plasma source at 350 Watt and an O_2 partial pressure of $8\cdot10^{-6}$ Torr. In-situ Reflection High-Energy Electron Diffraction (RHEED) confirmed the amorphous material. TiN was grown on top of HZO at 120^{o}C with an evaporation Ti rate of 0.1-0.2 Å/sec, an N_2 partial pressure of $8\cdot10^{-6}$ Torr and rf plasma at 350W. Two different process flows, gate first and gate last, were used. It is important to note that regardless of the process flow, dopant activation and crystallization annealing are performed in one step at 650^{o}C for 20 sec. Although both process flows resulted in functional transistors, gate last flow produced better results which are presented here. The process steps details are presented in Figure 1. At the end of the fabrication process, an extra forming gas annealing has been performed (20% H_2/Ar at 400 °C for 20 min) to passivate interfacial defects. The final device structure and an optical image of a Ge-FeFET are shown in Figure 2.

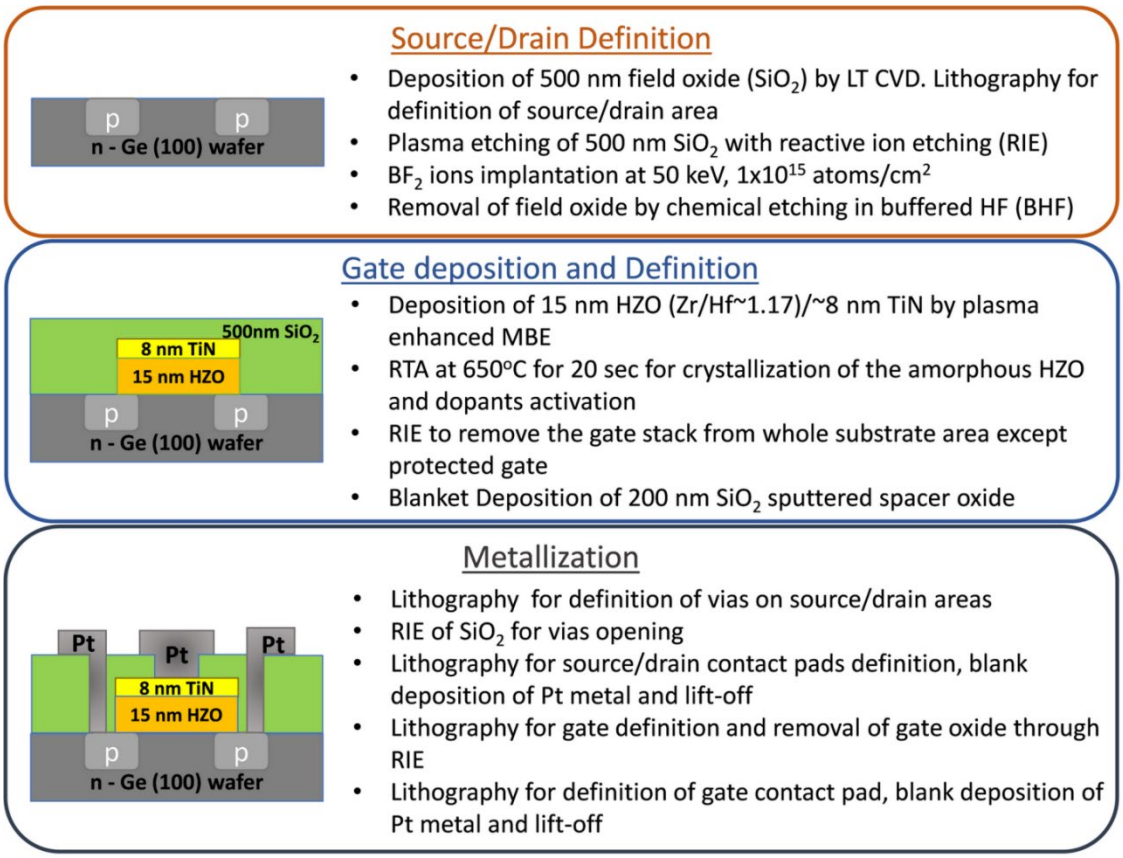

Figure 1: *Ge-FeFET device fabrication process steps.*

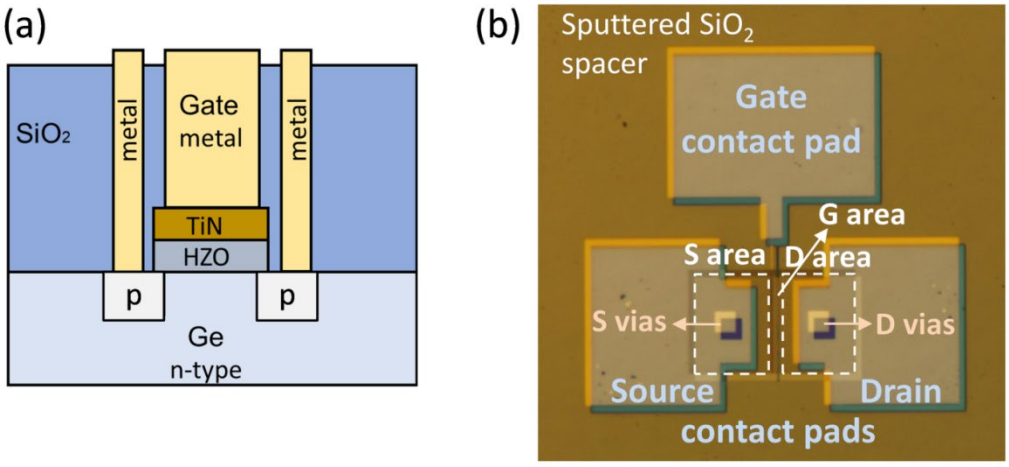

Figure 2: *(a) Side view illustration of the structure and (b) stereoscopic top view optical image of a Ge-FeFET device.*

5.3 Electrical characterization of Ge-FeFETs

First, the functionality of the pristine devices as transistors is presented, before polarizing the ferroelectric layer on the gate. Drain current vs gate voltage and drain voltage (I_{ds}-V_g and I_{ds}-V_d) characteristics of a pristine device with 200 µm width and 0.75 µm length channel are shown in Figure 3 (a) and (b) respectively. FETs with the shortest gate lengths (L=0.5, 0.75 and 1 µm) have an ON-current I_{ON}~10 mA/mm at V_d= -1V. This value is comparable to previously reported Ge FETs with an amorphous HfO_2 gate dielectric and similar channel dimensions [14]. Note however that while optimized Ge-FETs [14] are subject to surface passivation prior to gate deposition in order to increase the mobility and the I_{ON}, here in this paper, the surface passivation layer was omitted to avoid harming ferroelectricity in the HZO gate and to maintain a clean HZO/Ge interface. In addition, the maximum ON/OFF current ratio for the thinnest gate devices is ~$8 \cdot 10^2$ (Fig 3 (c)). This compares well with results values reported in the literature which show I_{ON}/I_{OFF} ~ 10^3 in Ge-FETs [11, 14]. It should be noted that the I_{ON}/I_{OFF} ratio in Ge-FETs is limited by high I_{OFF} current due to the low energy gap of Ge, as compared to Si-FeFETs which present I_{ON}/I_{OFF} ratios higher than 10^4 for similar device parameters. As expected, the current ratio is reduced as the channel length increases. The entire film is uniform and shows good reproducibility without significant variations among devices with specific gate dimensions.

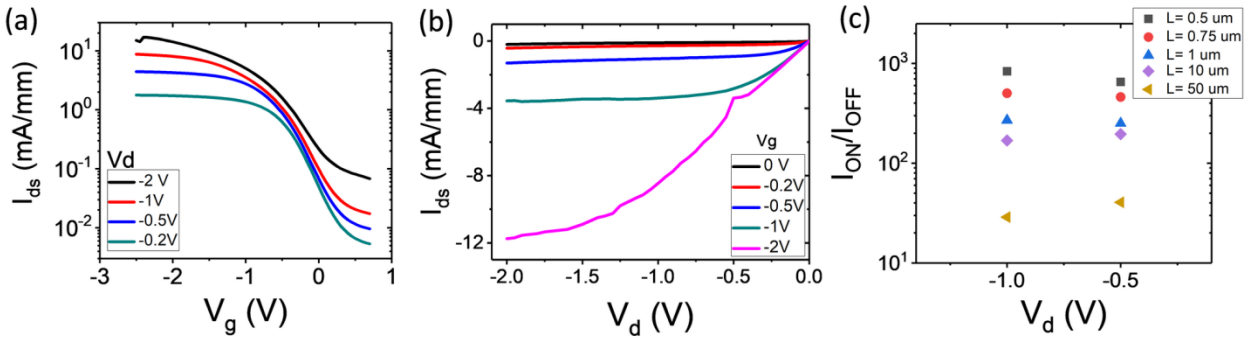

Figure 3: *(a) I_{ds}-V_g and (b) I_{ds}-V_d characteristics of a pristine device with 200 µm width and 0.75 µm length channel. (c) I_{ON}/I_{OFF} ratio of devices with varying channel length at V_d=-1 V and V_d=-0.5 V.*

The FET devices have HZO gates which show robust ferroelectric hysteresis, as seen below for a device with gate width 200 μm and length 0.75 μm. Dynamic hysteresis measurements (Figure 4 (a)) show a significant proportion of dielectric and parasitic charge. In order to obtain the pure ferroelectric contribution, typical PUND technique (Figure 4 (b)) was used by applying the pulse scheme of Figure 4 (c). A rectangular pre-polarization pulse with -5 V amplitude and 10 μs width was applied, that is similar to the write pulses we used to program the FeFETs. In that way we checked and ensured that these pulses are able to fully switch the polarization. By subtraction of non-ferroelectric charge (non-switching pulses) from total polarization (switching pulses), we obtain the corrected (blue) curve, that is the pure ferroelectric contribution in polarization (Figure 4 (d)). After 10 cycles, the switchable polarization has a value $2P_r$=22.4 μC/cm^2. The loop shows a shift of 0.5V to the left of V-axis, (V_c^+=+2.5V and V_c^-=-3.5V), probably attributed to the semiconductor depletion region of n-doped Ge [8].

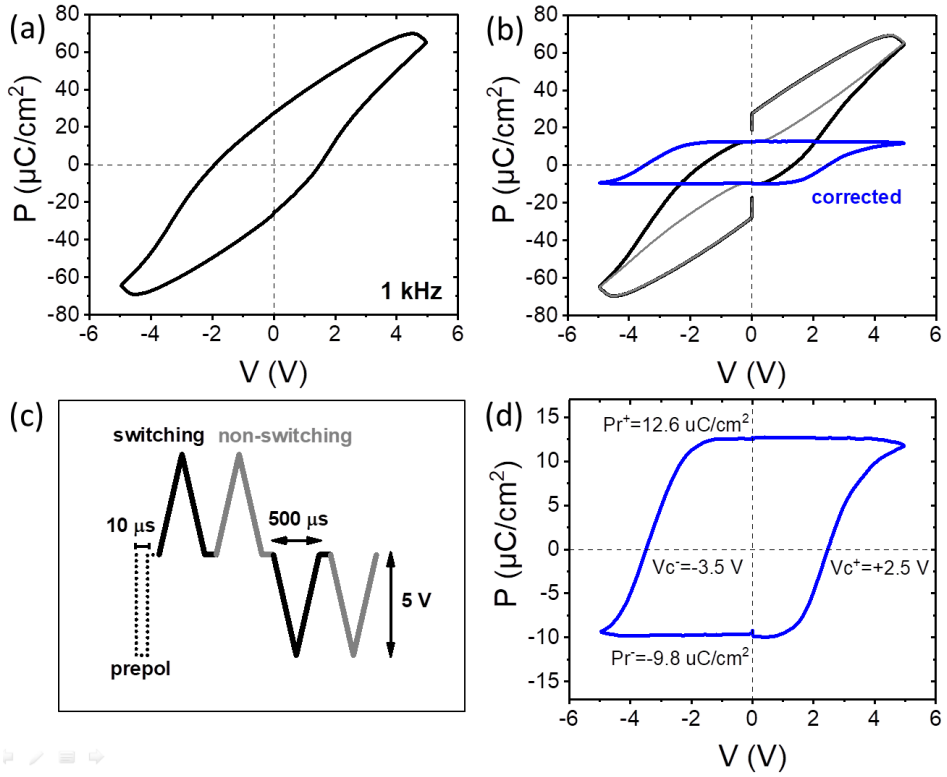

Figure 4: *(a) Polarization-voltage (P-V) dynamic hysteresis measurement of the gate with 200 μm width and 0.75 μm length at 1 kHz. (b) The P-V diagram at the same device obtained by*

PUND by applying the pulse sequence in (c) (d) Polarization-voltage (P-V) loop after corrected by PUND for non-ferroelectric charges for a device with gate width 200 µm and length 0.75 µm.

After verifying that the devices operate properly both as transistor and ferroelectric gates, we examine the ferroelectric field effect using Ge-FeFETs with short channel of 0.75 µm since these devices show best transistor performance (high I_{ON}/I_{OFF}) and sufficient remanent polarization (P_r). As a result of the gate oxide polarization, we expect to observe a shift in the threshold voltage, which will result in a hysteresis window on the I_{ds}-V_g graph for the two opposite states. The expected behavior for a p-channel FeFET is presented in Figure 5 (a). The pristine (purple) curve corresponds to a FeFET before the polarization is established in the HZO. When negative voltage is applied to the top of the gate, P_{up} is established and the negative charges at the bottom of HZO attract the holes at the surface of Ge. As a result, inversion is getting easier and lower gate voltage is needed to open the channel. That means that the threshold voltage shifts to the right (lower negative voltages). The reverse effect happens for P_{down} (Fig. 5 (b)). The horizontal distance of transfer curves for the two states (hysteresis) is defined as the Memory Window (MW).

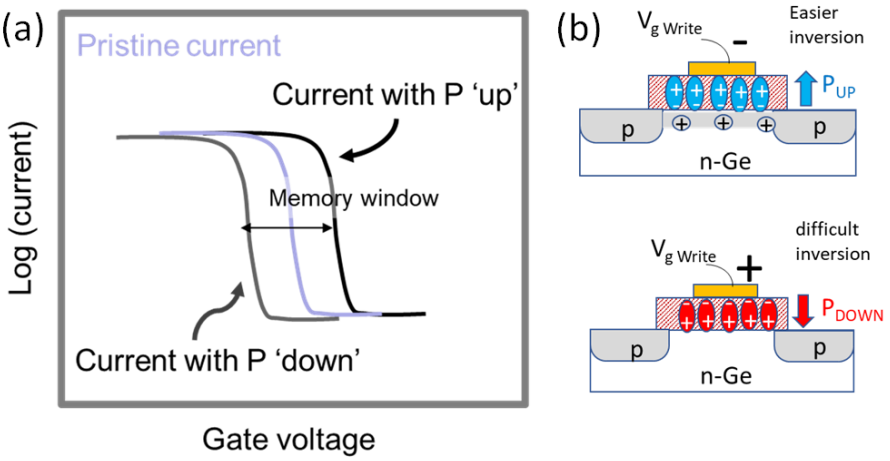

Figure 5: *(a) Shift of transfer curve depending on the polarization state (up or down) with respect to the curve of the pristine device for a p-channel FeFET. (b) When P_{up}/P_{down} is established in FE HZO, inversion in Ge channel is easier/more difficult respectively.*

The results for a device with gate dimensions W= 200 μm and L= 0.75 μm are presented in Figure 6 (a). The black curve shows the transfer characteristics of the pristine transistor with unpolarized gate. By applying a programming pulse of -/+ 5V for 100 μs on the gate the light red and blue curves at V_d= -0.5V are obtained which correspond to the pristine transfer characteristics of the FeFET in the up and down (see Figure 5) gate polarization state, respectively. A small MW of 0.1 V opens with P_{down} curve shifting to more negative bias, although both curves show an increased (degraded) SS. After only 10 cycles at 1 kHz and 5 V amplitude, the MW increases to about 0.5 V, although the transfer characteristics degradate further in such a way that SS increases and I_{ON} is reduced.

Then we polarize the gate by applying pulses of varying amplitudes (Figure 6 (b)). Pulses with amplitudes lower than +3 and -3.5 V are not enough to switch the polarization, hence there is no MW. By increasing the write pulse amplitude up to 6V, MW gradually opens. This behavior is ideally expected in ferroelectric HZO, where partial polarization switching is taking place for voltages close to the V_c. This behavior is promising for the realization of an analog memory, where, apart from the two ON, OFF states, we can also take advantage of the intermediate ones, provided that a sufficiently large MW is obtained to accommodate a sufficiently larger number of intermediate states. The excellent match of ferroelectric characteristics with the memory performance of devices, that is increase of MW as the ferroelectric wakes-up and shift of transfer curve above the V_c's, is strong evidence that the dominant mechanism of memory effect is the ferroelectricity.

Next, we examine the dependence on write pulse duration on a device with gate dimensions W=100 μm and L=0.75 μm (Fig. 6(c)). While P_{down} curve slightly shifts with extra pulse width (from 10 to 500 μs), P_{up} state is not really affected. We know from frequency dependent P-V measurements, that there is not such an asymmetry between the two states regarding their polarization switching that could explain this observation. So, it may be related to an extrinsic cause, probably to diffusion of positively charged oxygen vacancies into the ferroelectric, which is a relatively slow process. It is anticipated that when a positive bias is applied to the top TiN electrode for longer time (long pulse), oxygen vacancies from the Ti-O-N interface penetrate

further into the HZO moving towards the bottom. Hence, the inversion of the Ge channel is inhibited and the transfer curve further shifts to the left of voltage axis. Finally, after applying 1ms-long pulses, MW starts to close and on-current decreases.

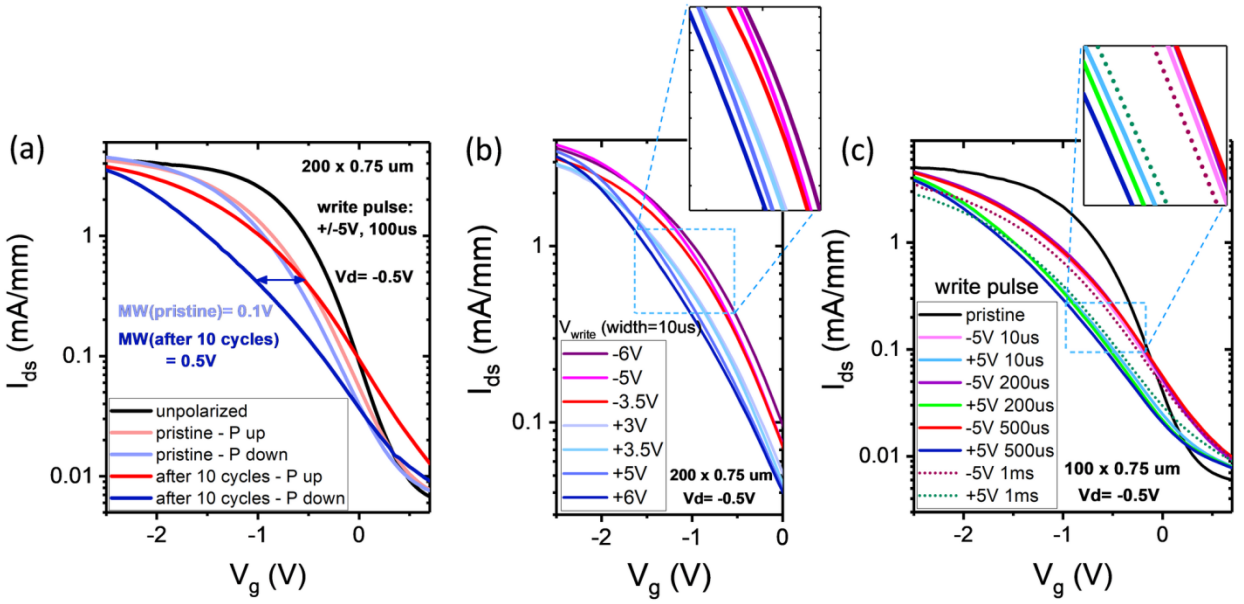

Figure 6: *(a) I_{ds}-V_g transfer curve of a pristine device, after applying only a write pulse and after applying 10 electrical cycles, for up and down polarization states. Modulation of transfer curve by varying (b) the amplitude and (c) the duration of write pulse.*

The other possible cause of the hysteresis in the transfer curve is the charge trap phenomenon between the channel and the insulator layer [1], but in that case an opposite shift would be expected; a positive /negative bias applied to the top electrode would attract negative/positive charges at the HZO/Ge interfacial defect states (electron/holes trapping) and as a result the transfer curve would shift to the right/left respectively [15]. Hence it cannot be the dominant mechanism here, but it disturbs the hysteresis caused by the polarization. Indeed, this is clearly observed in the case of ≥ 1 ms-long write pulses, where the duration is sufficient for charge trapping (Fig. 6 (c)).

Charge trapping remains a major issue for FeFETs, as it intensifies by polarization charges and competes the desired hysteresis of transfer curve related to polarization switching. It is known that high-k oxides have a high density of defects that create electronic states in the bandgap. The concentration of defects, particularly those near the interface, has serious consequences for channel mobility. Charges trapped in the defect centers scatter carriers in the channel leading to degradation of channel mobility [9]. Thus, on-current, which is proportional to mobility, is reduced as observed in our case. In addition, an extra capacitance term C_{int} is induced in parallel with the HZO by these interfacial states, increasing (degrading) the SS, according to the relationship:

$$SS = \frac{kT}{e} ln10 \left(1 + \frac{C_S + C_{int}}{C_{FE}}\right) \quad (1),$$

where C_S and C_{FE} are the capacitances of semiconductor Ge and FE-HZO respectively.

Concerning these devices, in a previous work [16] we had extensively examined the interface defect states in both n- and p-type Ge Metal-Ferroelectric-Semiconductor (MFS) capacitors by using impedance spectroscopy. The layer structure in those capacitors was identical with the gate structure used for FeFETs in the present work: TiN/15-nm HZO/Ge. In the case of n-Ge, an interfacial electrically active defect has been identified in Ge energy gap, 0.20-0.25 eV from the valence band, suggesting as probable defects associated to these traps are the dangling bonds, present in Ge at the interface [17-19]. Considering that the n-type Ge has a natural tendency to become inverted at the surface [20], we concluded that the level located at about 0.20 eV is acceptor type, being always filled by electrons. The negatively charged surface is the reason why the pristine I_{ds}-V_g curves are slightly shifted to the right (Figure 2(a)). In other words, when there is no applied bias to the gate (V_g=0), an amount of current passes through the spontaneously inverted channel [19, 21].

The FGA with 20% H_2/Ar at 400 °C for 20 min improved the interfaces, but did not totally eliminate the defect states. So the annealing conditions need optimization; alternative passivation should be considered. Since a passivating dielectric layer (e.g. GeO_2) could harm ferroelectricity inhibiting polarization screening by the metal electrodes, such passivation

scheme should be avoided. Sulfur passivation by a single monolayer of S atoms could be a good approach. As it is has been reported, S passivation of Ge [22] or surface nitridation [23] can reduce the interface-state density and can improve the electrical properties in terms of EOT and gate-leakage current.

Subsequently, we perform electrical endurance measurements by applying additional cycling to the gate. First, we stress the device at low frequency 100 Hz and 4V amplitude and after ~1000 cycles we continue the cycling at 1 kHz, 4.5 V. MW shows a maximum value of 0.55 V after 100 cycles, when ferroelectric hysteresis loop is fully open after wake-up. To be noted that the fact that our devices don't need significant cycling to wake-up, as it is usually required in ferroelectric hafnia, is an important advantage for the preparation of devices. In addition, the weak wake-up is promising for improved reliability in terms of imprint and retention [13], as expected by the oxide-free HZO/Ge interfaces.

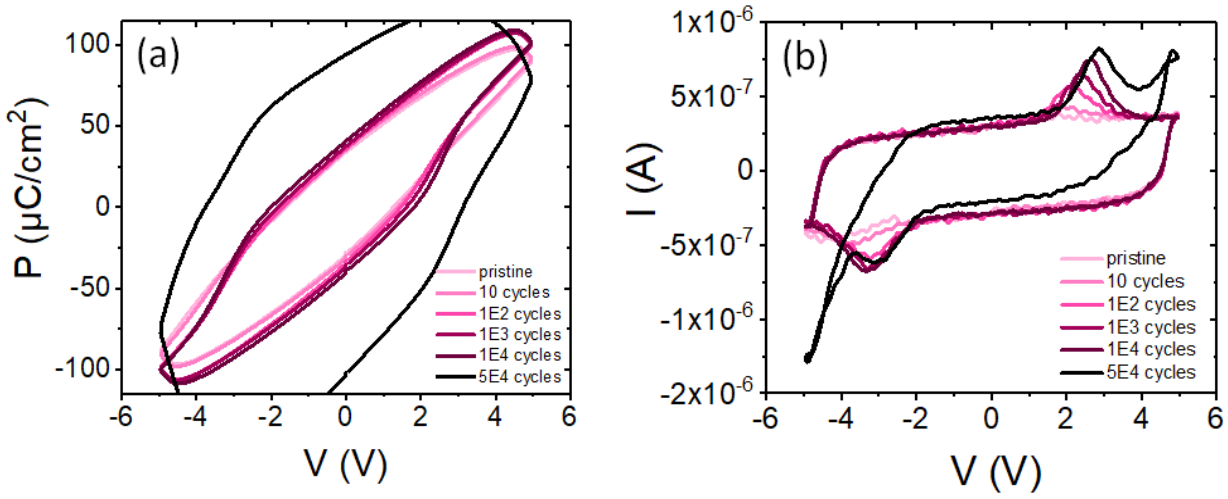

Figure 7: *(a) Polarization and (b) displacement current vs voltage loops at 1 kHz during electrical cycling.*

As observed in Figure 8 (a), since gate is electrically stressed, I_{ON} gradually decreases and SS increases for both states. However, the ferroelectric field effect is maintained and polarization hysteresis still dominates over trapping hysteresis. After $5 \cdot 10^4$ cycles, P-V loop starts to be distorted by leakage current, indicating that it is close to the electrical breakdown (Figure 7).

The values of I_{ON} for both states and MW as a function of cycles are presented in Figure 8 (b) and (c) respectively.

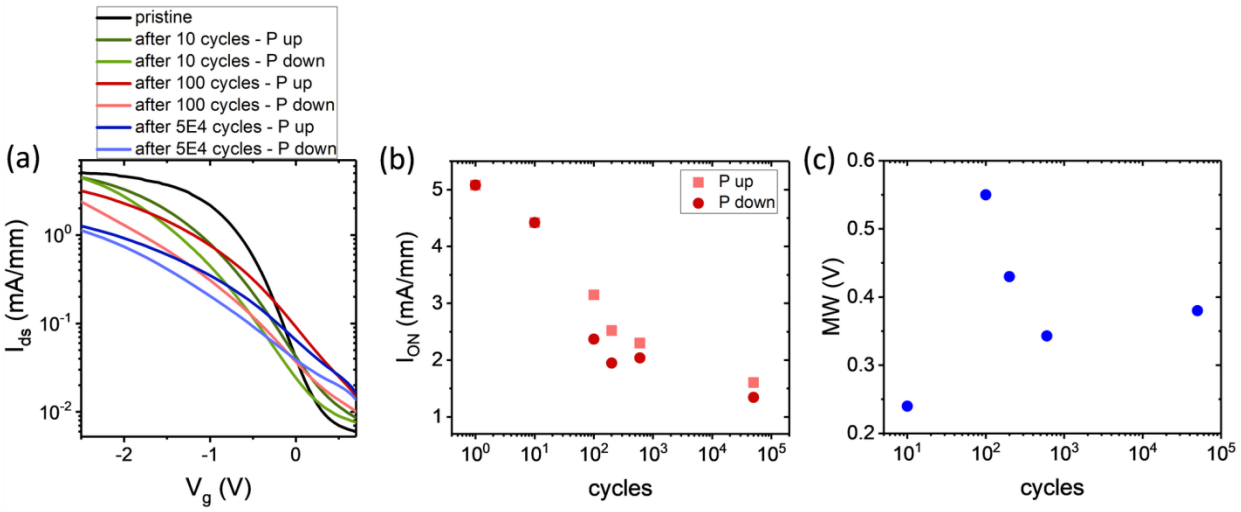

Figure 8: *(a) Transfer curve I_{ds}-V_g of FeFET with W=100 µm and L=0.75 µm channel at V_d= -0.5 V during electrical cycling. (b) ON-current for P_{up} and P_{down} and (c) MW as a function of cycles.*

Finally, the retention of memory performance is examined. After applying a V_{write}= ±5V to the gate, the transfer curve is measured after delay time varying from 1.5 min to 3 hours (Fig. 9(a)), showing only a slight variation with time. The time evolution of MW is presented in Figure 9 (b), where a small reduction from 0.55 V to 0.50 V is observed. Also, it is inferred from the projection in inset that the FeFETs are not expected to fail before 10 years, which is a figure of merit for reliability, showing a MW=0.4 V. This is in agreement with the stability of remanent polarization, as depicted in Figure 10. These good results are attributed to the good ferroelectric characteristics. The predominance of orthorhombic phase and the clean interfaces result in the maintenance of polarization.

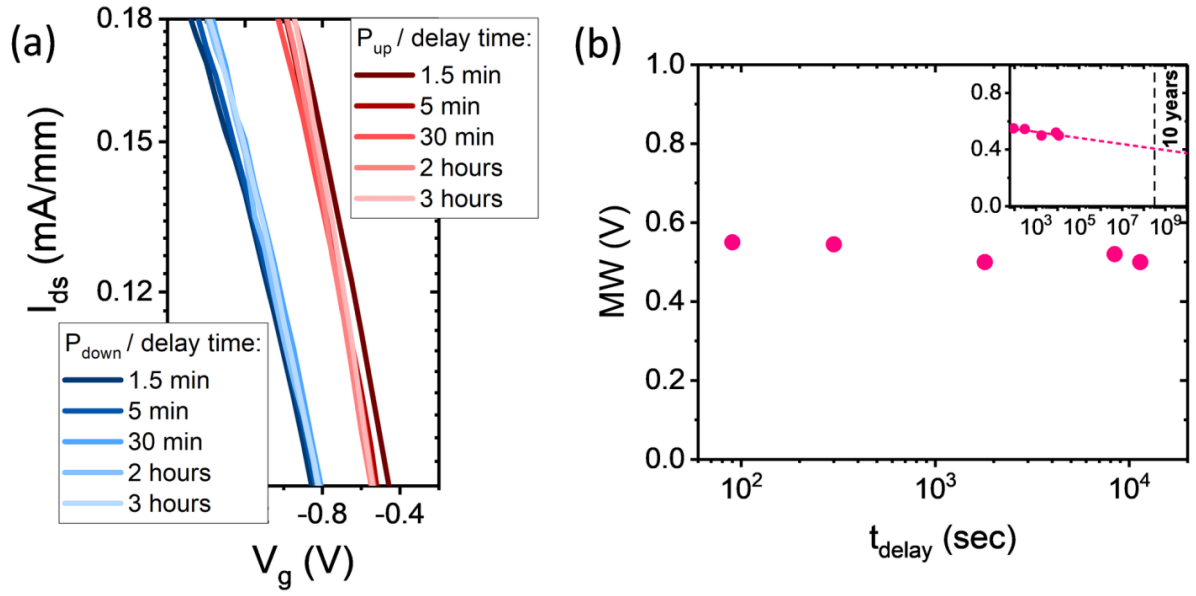

Figure 9: *Retention test of memory performance of FeFET with W=100 µm and L=2 µm channel. (a) Transfer curve I_{ds}-V_g at V_d= -0.7V for different delay times after polarizing the HZO to the up and down states. (b) MW as a function of delay time and the dashed line in the inset is the projection in time, showing that the devices are not expected to fail before 10 years.*

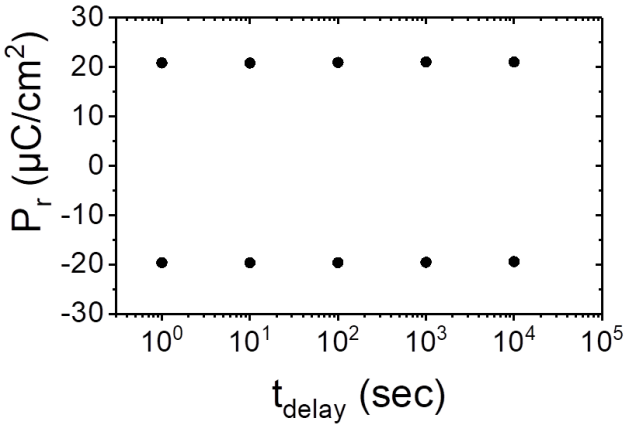

Figure 10: *Remanent polarization for the two states as a function of delay time for a TiN/15 nm HZO/Ge capacitor.*

The retention of a ferroelectric capacitor with the layer structure of the FeFETs TiN/15 nm HZO/Ge was examined. After applying a write pulse to the gate to polarize the ferroelectric HZO, we measured the remaining P_r for both states after different delay times. As presented in Figure 10, both positive and negative P_r are stable at least after 10^4 sec delay.

5.4 Conclusions

In this study, scaled down to 0.75 μm gate length ferroelectric pFETs with TiN/HZO gate stack and Ge channel are fabricated and characterized. Avoiding the typical passivation layer resulted in stable and robust ferroelectricity without severe wake-up effect. The penalty for the oxide-free HZO/Ge interface is the existence of interfacial defect states causing mainly degradation of the SS and gradual decrease in I_{ON} of transfer curves. The ferroelectric field-effect with maximum MW=0.55 V is clearly observed, but further process optimization is required. Retention measurements up to 10^4 sec show a small reduction to 0.5 V and from data projection it is inferred that the devices are note expected to fail before 10 years. The main challenge for future development is the passivation of the electrically active defects at HZO/Ge interface, without harming the ferroelectricity at the HZO gate, probably by sulfur passivation. These first results on Ge-FeFETs open new opportunities for the realization of gate-first process and lower total thermal budget by combining the dopant activation and the ferroelectric oxide crystallization annealings at 650^{o}C. The above study resulted in journal publication [24].

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Chapter 6

Low power Ferroelectric Tunnel Junctions for Neuromorphic technologies

6.1 Introduction

The FTJ configuration consists of an ultra-thin ferroelectric layer sandwiched between two electrodes with different screening lengths, typically a metal and a semiconductor. The main principle is that depending on the polarization state (up or down) in the FE layer, the polarization charges in the interface with the semiconductor modulate the potential barrier, and as a result the resistance (Fig. 1a,b).

The polarization state of the device is detected by measuring the current flow upon application of an electrical field that is lower than the coercive field of the ferroelectric, avoiding the polarization switching. In that way the FTJ can be used to store information and in contrast to FeRAM, it doesn't need to be refreshed after reading.

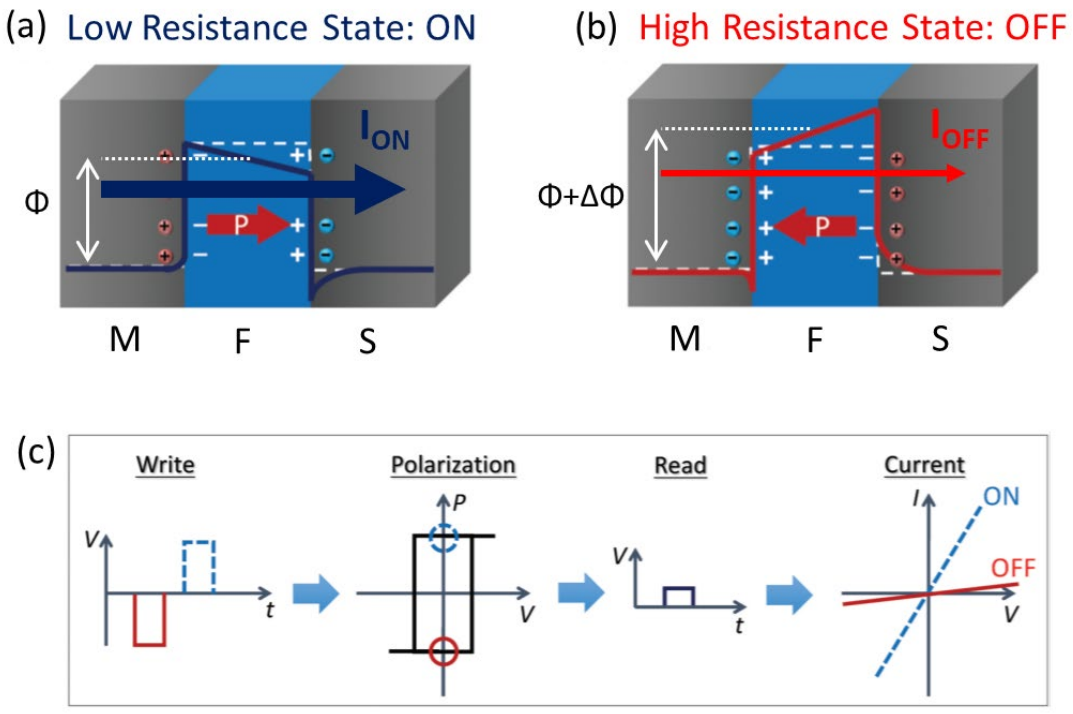


Figure 1: *Barrier profiles for (a) ON and (b) OFF states, modulated by polarization P in the FE. (c) After applying a positive/negative pulse to fully switch the FE, the current is measured at the ON and OFF state respectively, at a read voltage lower than V_c. Adapted from ref [1].*

In more detail, when P_{down} is established after applying a positive voltage, the potential barrier is lower so the current can pass more easily (ON-state). Accordingly, with the polarization upwards the OFF-state is obtained (Fig. 1c). This control of resistance by the polarization state makes these devices memristive. The change in the tunnelling current is often called the tunneling electro-resistance (TER) effect and is measured as the ratio between the low-resistance state (LRS) and high-resistance state (HRS). In the 1970s L. Esaki et al. proposed the concept of FTJ as a "polar switch" [2]. However, as the fabrication of an ultra-thin ferroelectric layer required for reasonable tunnelling currents [3] is challenging, the concept was first demonstrated only in 2009 based on an ultra-thin $BaTiO_3$ ferroelectric layer [4], and recently on $Hf(Zr)O_2$.

A typical approach to overcome the difficulty to obtain ferroelectricity in ultra-thin oxides, is the double layer FTJ, where at least one additional dielectric layer is inserted between one of the electrodes and the ferroelectric layer. In this configuration, the polarization switching in the FE modulates the tunneling barrier in the dielectric layer. The NaMLab group demonstrated the double layer FTJs, inducing a thin Al_2O_3 thin (~2 nm) dielectric layer in series with the FE-HZO [5-7], achieving a TER~14 and intermediate current levels. Recently, M. Hoffmann et al. in the same group reported a TER of about 2500, the highest reported so far for polycrystalline HZO-based materials, by reducing the thickness of ferroelectric film after crystallization, by using atomic layer etching [8]. Also, H. Ryu et al. showed symmetric potentiation/ depression characteristics and widely tunable conductance on a similar layer structure [9]. High TER ratio $\sim 10^3$ was measured in MoS_2/4.5 nm HZO/W heterojunctions as well [10], attributed to the Fowler–Nordheim tunneling mechanism and polarization-induced modulation of the potential at the MoS_2/HZO interface.

Despite these promising results, the single layer FTJs have the strong advantages of low operation voltages and the improved retention due to the absence of the thin dielectric layer. In 2017 F. Ambriz-Vargas et al. reported a FTJ with ultrathin 2.8 nm HZO with a TER ratio ~15 and I_{ON} ~10^{-6} A cm^{-2} at low read voltage +0.2V [11]. Other research groups also reported ferroelectric tunneling electroresistance in single layer junctions [12-14]. Moreover,

demonstration of scaled down to 1 nm HZO on Si by S. S. Cheema et al. [15] provided an important approach by combining the Si-compatibility with high polarization-driven electroresistance ~190 and large read current >1 A cm^{-2} at low voltage +0.2 V, for high-speed operation. Epitaxial ultra-thin FE-HZO on LSMO bottom electrode showed memristive and STDP placticity behavior by FE switching driving mechanism [16-18]. Another interesting approach was the fabrication of 3D TiN/9 nm FE-HZO/Pt vertical structures devices by L. Chen et al. [19] with TER~20, meeting the full functions of biological synapses.

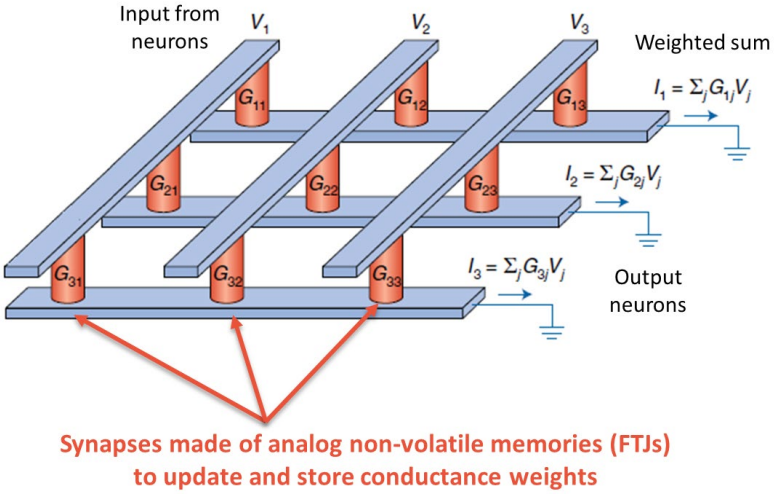


Figure 2: *Analog computing in crosspoint arrays. A schematic neural network consisting of input neuron signals (voltages V_j) connected to output row current I_i by an array of analog FE memristors to update and store conductance weights (G_{ij}). Adapted from ref [20].*

In this dissertation, we worked on single layer FTJ configuration and some first results are presented in this chapter. The low-power operation of the devices is essential for dense and big arrays in neural networks for future technologies (Fig. 2).

6.2 Memristive performance of 5 nm HZO on NSTO capacitors

5-nm-thick ferroelectric HZO capacitors were fabricated in a FTJ configuration on Nb-doped $SrTiO_3$ (NSTO) semiconductor substrates with TiN metal top electrodes by plasma assisted molecular beam deposition and annealed at 500°C for 45 s. After ~3000 cycles for wake-up,

capacitors show good ferroelectric characteristics, as seen in Figure 3. Switching polarization is 2Pr ~37 μC/cm^2 (Fig. 3(b)) and electrical endurance ~6 ·10^4 cycles at 1 kHz, 2 V (Fig. 3(c)).

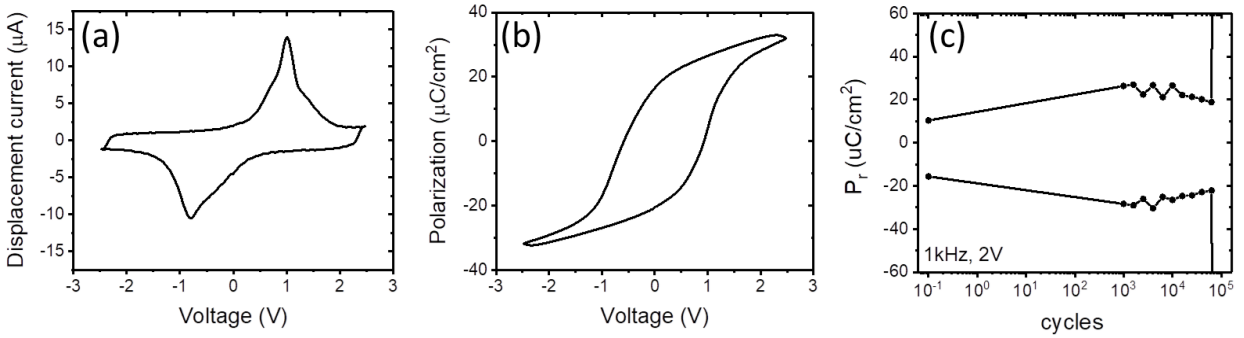


Figure 3: *(a) Displacement and (b) polarization hysteresis loops of a TiN/5 nm HZO/NSTO capacitor. (c) Remanent polarization values during electric field cycling at 1kHz, 2V.*

In order to examine the memristive performance of the devices, the pulse sequence of Fig. 4 (a) was applied to the gate. First, a negative pulse with 1.6 V amplitude and 500 μs duration was applied to fully switch the ferroelectric to the P_{up}. Then, a write pulse with the same duration and gradually varying amplitude up to ±1.6V was applied, followed by a measurement of the current at +0.4V. The read voltage was chosen to be lower than the coercive voltage, so that the measurement doesn't affect the polarization. The red I-V hysteresis loop of Figure 4b was obtained, in which the memristive performance is clearly observed. The same procedure was repeated for five different values of maximum V_{write} close to V_c^+.

The polarization switching in the HZO alters the resistance of the junction either due to the modulation of HZO barrier height or the Schottky barrier at the semiconductor/HZO interface. When the polarization points to bottom or top electrode, ON or OFF state is maintained respectively, with I_{ON}/I_{OFF} ratio~2-3 at +0.4 V. Non-volatile intermediate states are obtained by partial polarization switching for write voltages close to the coercive voltages making the devices operating as analog memories.

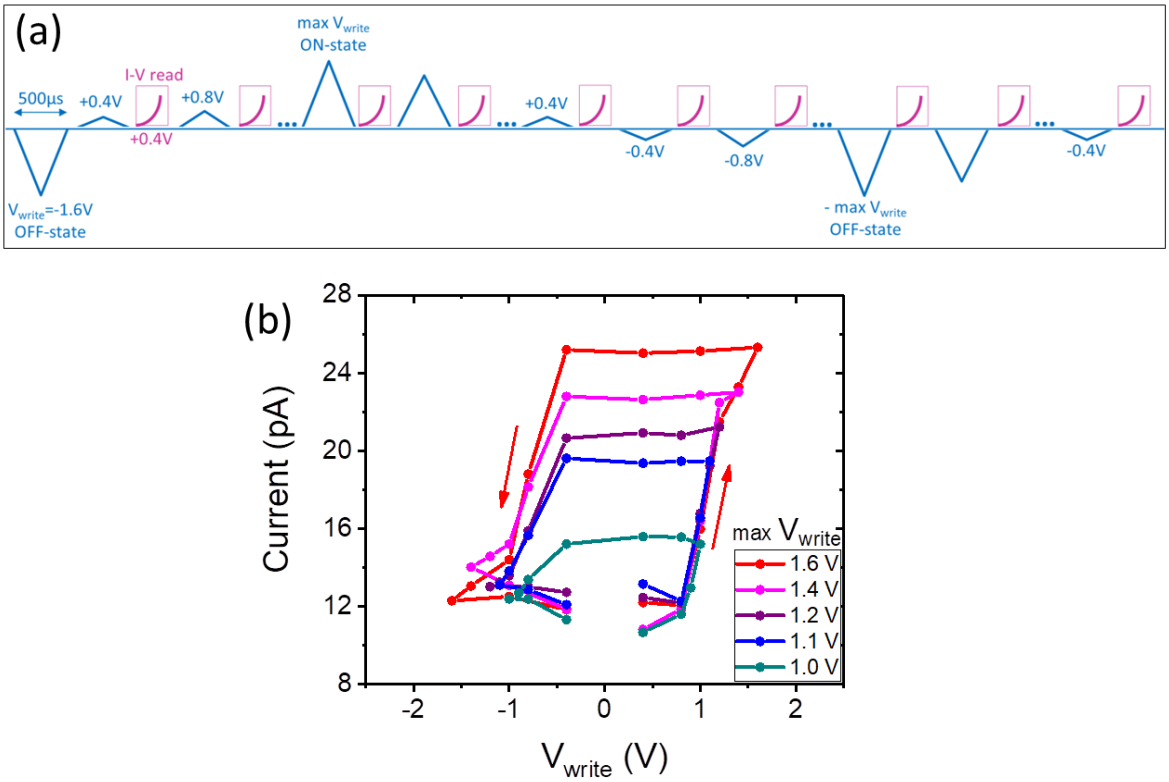


Figure 4: *I-V hysteresis loop. (a) Scheme of pulse sequence applied to the gate. (b) Current measured at V_{read}=+0.4V as a function of the pulse amplitude (V_{write}) applied before the measurement for a TiN/5 nm HZO/NSTO capacitor at different maximum write voltages.*

Synaptic plasticity in the form of long term potentiation (LTP) and long term depression (LTD) of the conductance synaptic weights is obtained by applying consecutive pulses of increasing amplitude [+(0.75-1.6) V and –(0.6-1.6) V, Fig. 5(a)] or width [(1.7 µs-1s), Fig. 5(b)]. The pulse sequences for variable amplitude and variable width are depicted schematically in Figures 5 (a) and (b) respectively. The LTP and LTD curves for varying amplitude are nearly symmetric and linear, as ideally preferred for artificial synapses.

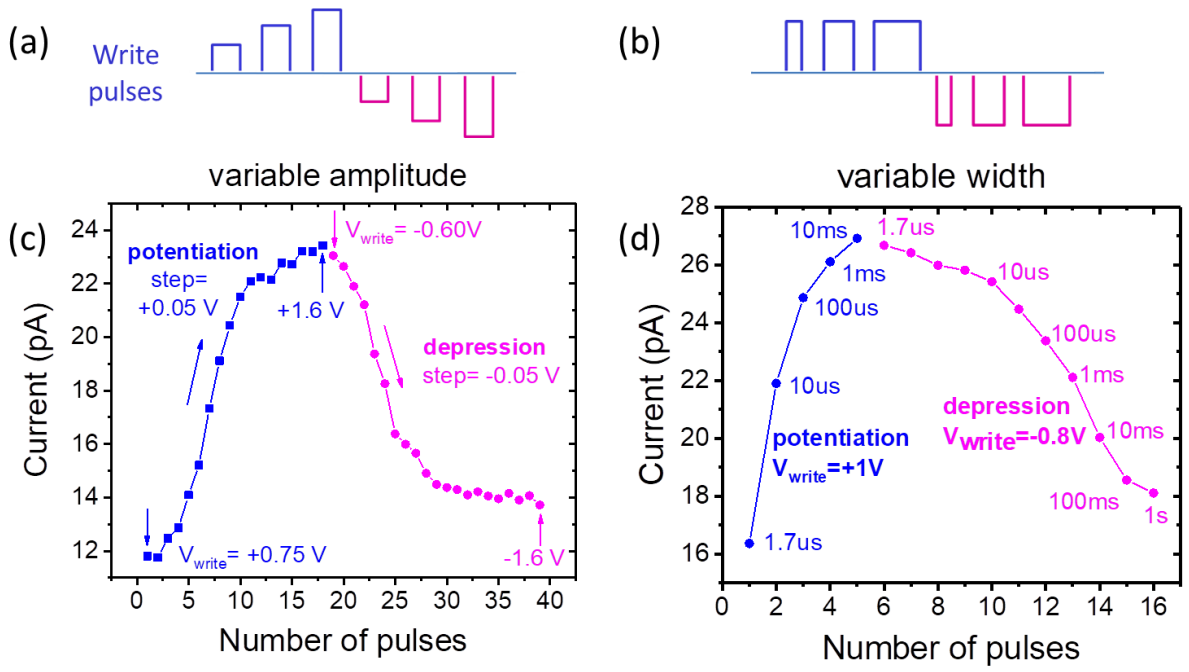


Figure 5: *Schemes of write pulse sequences with (a) increasing amplitude and (b) increasing pulse width applied for synaptic plasticity. (c) and (d) the resulting current as a function of pulse.*

Subsequently, we examined the reliability of the junctions. First, electrical endurance was tested at 1 kHz and 1.6 V. During cycling, for each data point the ON and OFF current was measured at +0.4V after polarizing the device at + and - 1.6 V respectively (Figure 6). Both values tend to increase almost the same, in such way that the TER ratio is slightly reduced. The junction breaks down after $2.5 \cdot 10^5$ cycles.

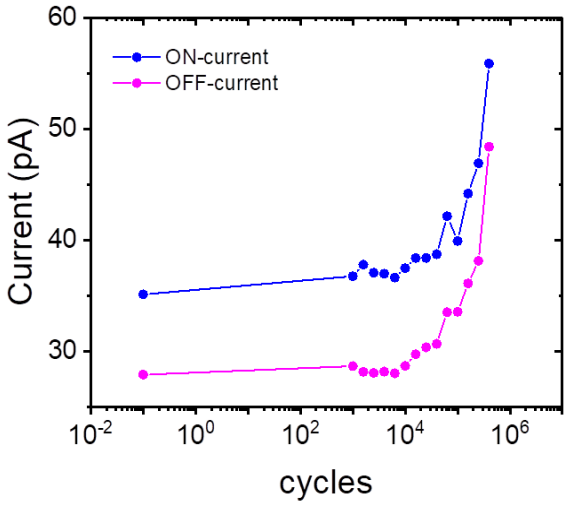


Figure 6: *Electrical endurance test of the memristor. (a) ON and OFF current values at V_{read}=+0.4V during field cycling at 1kHz and 1.6V. Before each data point a triangular pulse with amplitude= + or -1.6V and width= 250 μs was applied to the gate in order to switch the HZO to P_{down}/ON-state or to P_{up}/OFF-state respectively.*

Another critical issue for the reliability of the synapses is the stability of the current during storage time. Retention test was performed at 298 K (RT); after applying a write voltage corresponding to each intermediate state, the current was measured after delay time up to 10^4 sec (Figure 7). As it is observed, there is no significant retention loss for each state, with a maximum variation ~1.3 pA. That means that more than 8 states (=2^3→3 bits) can be obtained with good sense margin.

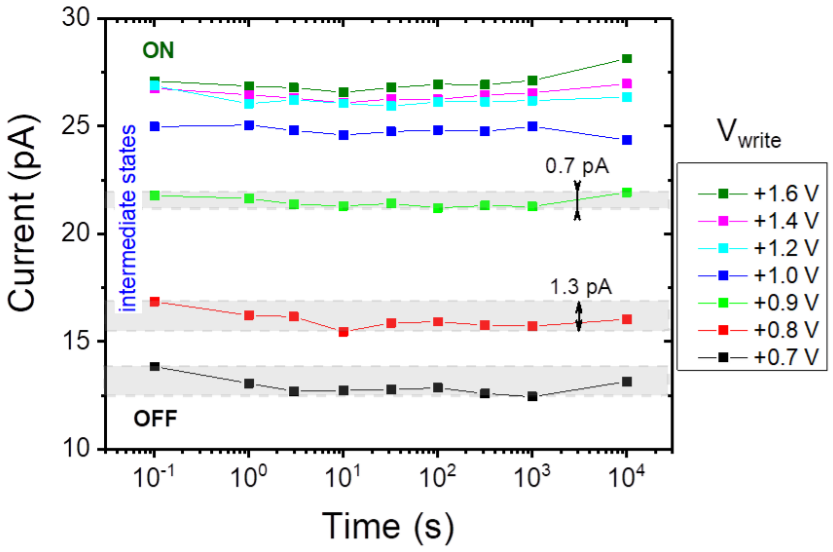


Figure 7: *Current retention test at 298 K for ON, OFF and intermediate states.*

It is also important to examine the performance at a higher temperature of 85°C (=358 K), at which electric circuits usually work. The I-V loop and current retention test are presented in Figure 8. The synapse show the same memristive performance, but with increased current values.

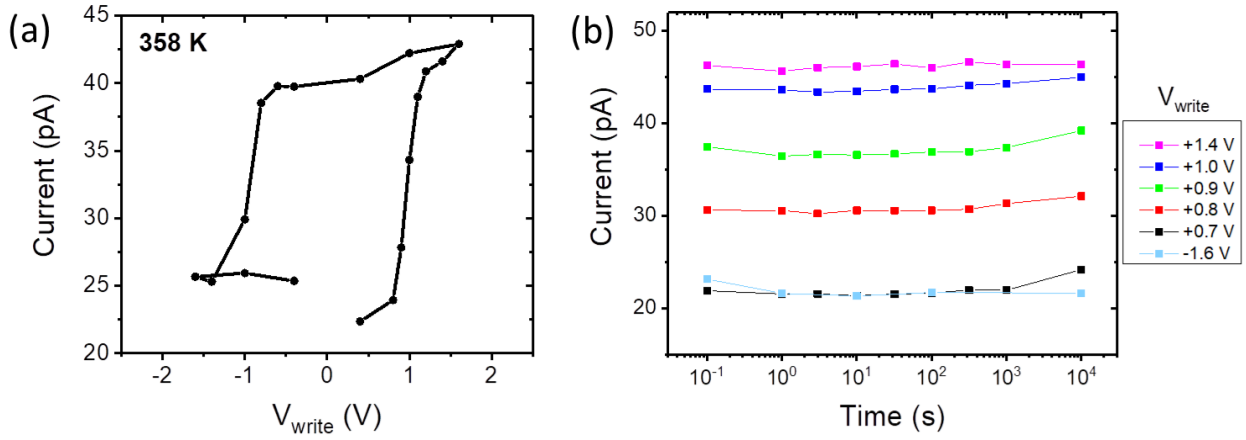


Figure 8: *(a) I-V hysteresis loop and (b) current retention test at 358 K.*

In order to increase the TER ratio and current values, we also tried different top metal electrodes. W showed significant improvement with TER~4 and I_{ON}~120 pA. The I-V loop and the displacement current are presented together in Figure 9, where the excellent match of DC-current and ferroelectric switching is clearly observed. The transition from OFF to ON and intermediate states occur in the voltage range of the V_c^+ peak. The same happens for the reverse transition (ON to OFF) at V_c^-. This agreement is strong evidence that ferroelectricity is the main mechanism of resistance switching.

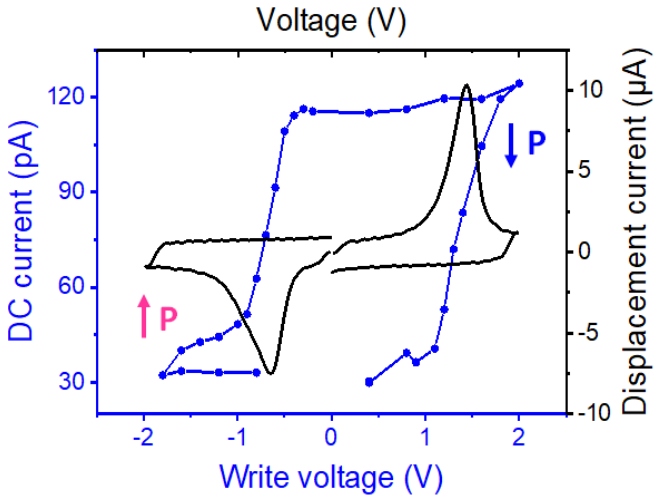


Figure 9: *Current hysteresis loop and displacement current of a W/5 nm HZO/NSTO capacitor.*

The larger TER in devices with W top electrode gave the opportunity for more intermediate states, as depicted in the linear region of LTP and LTD curves for varying amplitude in Figure 10 (a). In the case of varying width, the current reduces abruptly in the first step, noting the criticality of measurement conditions. This behavior can be improved by applying lower write amplitude, as in the case of TiN/HZO/NSTO device in Figure 5 (d), or by shorter pulses starting with w=50 ns.

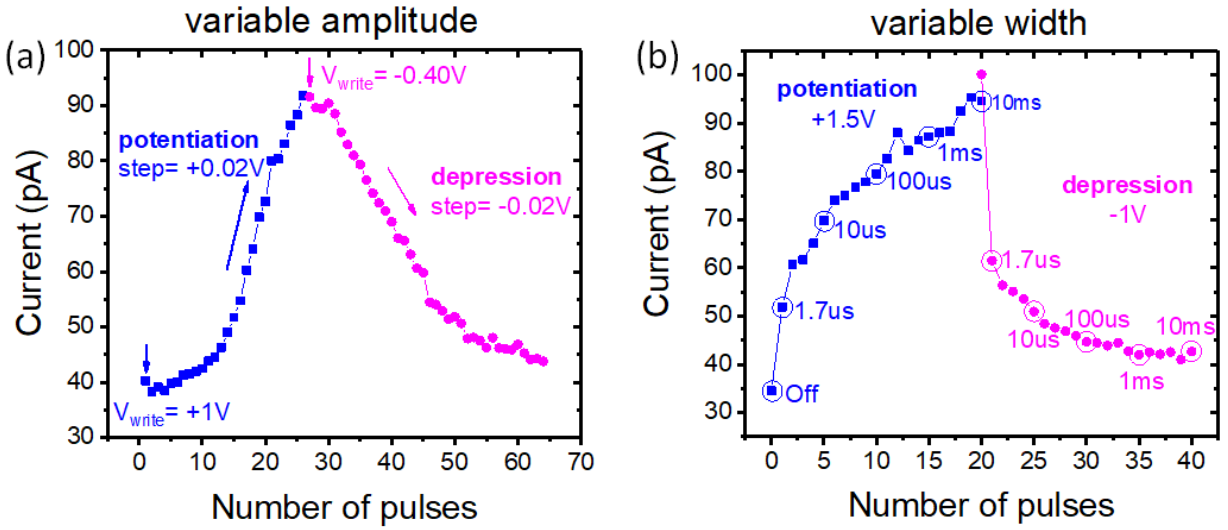


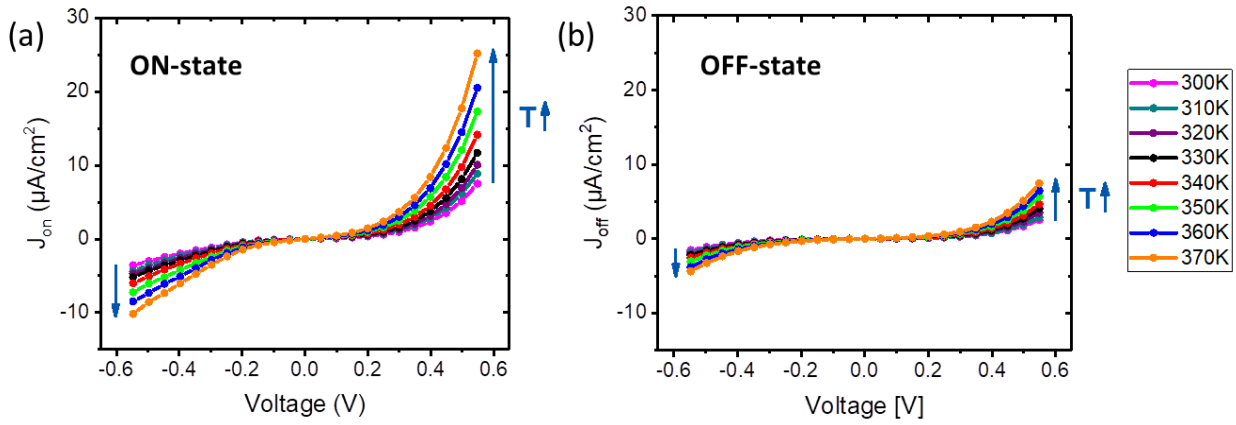
Figure 10: *Current as a function of pulse numbers with increasing (a) pulse amplitude and (b) pulse width.*

The third possible pulse scheme used in neuromorphic technology is a sequence of identical pulses, with constant both amplitude and width, but it was hard to obtain synaptic plasticity in this case.

6.3 Investigation of conduction mechanism

In order to investigate the current mechanism, I-V measurements were performed at different temperatures in the range of 300-370 K. The results for the W/HZO/NSTO device are shown in Figure 11 (a). The temperature dependence of current excludes the direct tunneling to be the

dominant current mechanism. Then, the Schottky emission was assumed as possible mechanism, because of the presence of the semiconductor NSTO as bottom electrode.



<u>Figure 11</u>: *Temperature dependent current density of (a) ON and (b) OFF-state vs voltage at range 300-370 K for W/HZO/NSTO capacitor.*

According to the relationship for the Schottky emission, the current density in the reverse direction (negative voltages), is:

$$J_{Schottky} = A^{**} T^2 exp\left[-\frac{1}{k_B T}\left(\varphi_B - \sqrt{\frac{e^3 V}{4\pi\varepsilon_0\varepsilon_{Fe} d}}\right)\right] \quad (1),$$

where A** is the Richardson constant of STO, T the temperature, k_B the Boltzmann constant, ϕ_B the activation barrier, e the elementary charge, V the applied voltage, ε_0 the vacuum permittivity, ε_{Fe} the dielectric constant of ferroelectric and d the oxide thickness.

If the conduction is dominated by Schottky emission, the quantity $\ln(J_{ON,\ rev})/T^2$ should be proportional to $\sqrt{V}$. By plotting the experimental data for each temperature, the linear behavior is confirmed for $|V| \leq 0.30$ V and more clearly at T ≥330 K (Figure 12(a)). In order to estimate the ϕ_B, the following analysis was made: by plotting the $\ln(J_{ON,\ rev})/A^{**}T^2$ vs $(kT)^{-1}$ for each V_{read}, the slope equals with the quantity $a = -\left(\varphi_B - \sqrt{\frac{e^3 V}{4\pi\varepsilon_0\varepsilon_{Fe} d}}\right)$, as shown in Figure 12 (b) for V_{read}=-0.15 V. Then, by linear fitting of $|\alpha|$ vs $\sqrt{V}$ for each V_{read}, the extracted intercept gives approximately the activation barrier for the ON-state ϕ_B=0.2 eV.

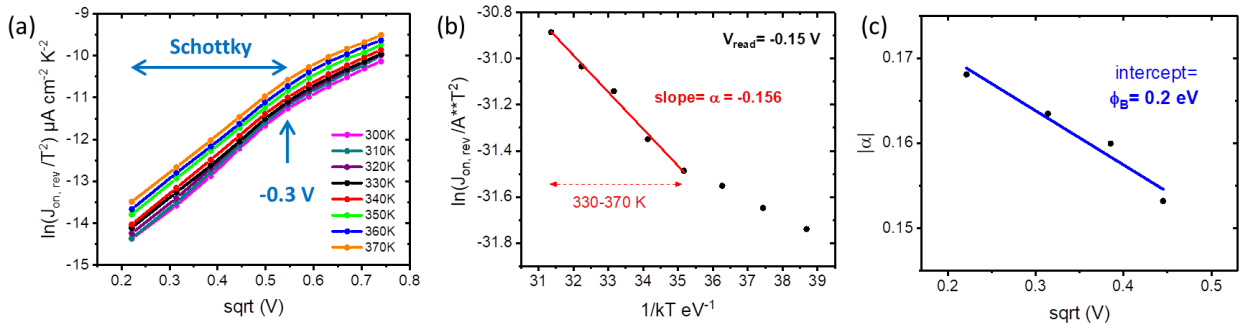


Figure 12: *(a) Linear dependence of $ln(J_{ON,\ rev})/T^2$ vs sqrt(V) at T≥330 K and $|V| \leq 0.30$ V, indicating that the dominant current mechanism is Schottky emission. (b), (c) A low activation barrier φ_B~0.2 eV for the ON-state is estimated.*

The Schottky barrier of NSTO semiconductor is modulated by polarization charges in HZO, resulting in the modulation of its resistance.

6.4 Conclusions

Single layer memristors consisting of 5 nm ferroelectric HZO on NSTO semiconductor substrates were fabricated operating in low voltages < 2 V. The conductance in devices is controlled by the polarization state in HZO, by modulating the resistance of NSTO depletion layer. The devices show synaptic plasticity and analog memory performance with intermediate states with no retention loss. However, the ON/OFF ratio ~4 and ON-current in the sub nA regime are quite low and they should be improved for better sensing in the devices. For this reason, future work will aim at improving the TER ratio, probably by using NSTO substrate with lower doping to reduce the I_{OFF}, or by proper engineering of the interfaces in order to achieve stable ferroelectricity in lower thicknesses.

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Summary

HZO grown by plasma assisted molecular beam deposition on Ge substrates showed robust ferroelectricity with remarkably improved wake-up and predominance of the orthorhombic $Pca2_1$ (ferroelectric) phase, mainly attributed to the clean oxide-free HZO/Ge interfaces. A depletion region, formed at low temperatures, in Ge surface and its effect on ferroelectric characteristics of Ge-MFS capacitors were studied. The absence of an insulating interfacial layer, like in the case of Si-devices, and the low E_g of Ge which prevents depletion, make depolarization fields insignificant at room temperature. This allows a symmetric and robust polarization hysteresis loop of Ge MFS. Subsequently, reliability measurements of HZO Ge MFS capacitors showed that imprint and wake-up effects are correlated and are influenced by the HZO/TiN plasma assisted atomic oxygen growth methodology as well as the crystallization annealing processing. The behavior of the V_c shifting with time and temperature, indicated that the top TiN/HZO electrode-controlled trapping/detrapping at interfacial oxygen-vacancy defects is the primary source of imprint fields. The robust ferroelectricity, resulting in high remanent polarization, stable performance without retention loss and improved wake-up, is inversely related to the electrical endurance.

The above study of the material led to the fabrication of electronic devices; ferroelectric field-effect transistors (FeFET) and ferroelectric tunnel junctions (FTJ) for energy efficient embedded non-volatile memories and neuromorphic technologies. The threshold voltage in FeFETs and the resistance in FTJs are controlled by the polarization state in HZO, making them perform as non-volatile synapses. Also, taking advantage of the unconventional ability to partially switch the polarization in HZO, the devices show analog memory performance with stable intermediate states. P-channel Ge-FeFETs make the use of the preferable ferroelectric hafnia, that is HZO, in the gate-first process feasible, as the temperature required for dopant activation in Ge ~650^{o}C coincides with the annealing temperature for crystallization of HZO. Moreover, single layer FTJs consisting of 5 nm ferroelectric HZO on NSTO semiconductor substrates aim to the integration in the back-end-of-line of CMOS and ultra-low power operation.

Overview

The recent discovery of ferroelectricity in hafnia, opened new horizons in the family of ferroelectrics. First of all, the realization of ferroelectric non-volatile memory devices for improved information and energy storage has been boosted due to the compatibility of HfO_2 and ZrO_2 with CMOS and their thickness scalability down to a few nanometers, essential for the fabrication process. Besides, it was revolutionary from the physical point of view. The unusual mechanism regulating the ferroelectricity in hafnia enables the partial polarization switching. As the domain walls have almost zero width, each dipole can be switched independently from its neighboring ones. As a result, the ferroelectricity in hafnia can be scaled down to sub 1 nm regime, even with polycrystalline structure. Despite the rapid progress of HfO_2-based ferroelectrics over the last decade, fundamental issues remain open regarding the origin of ferroelectricity in fluorite-structure oxides and the switching mechanism. Nonetheless, the idea that there might also be other materials with unknown ferroelectric properties emerged. Indeed, very recently, ferroelectricity was also verified in aluminum scandium nitride, further raising the possibility of future integrated electronics including a variety of ferroelectric functionalities.

List of publications

1. **C. Zacharaki**, P. Tsipas, S. Chaitoglou, S. Fragkos, M. Axiotis, A. Lagoyiannis, R. Negrea, L. Pintilie, and A. Dimoulas, "Very large remanent polarization in ferroelectric $Hf_{1-x}Zr_xO_2$ grown on Ge substrates by plasma assisted atomic oxygen deposition", *Appl. Phys. Lett.* **114**, 112901 (2019).

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